LC29H Series
Reference Design

GNSS Module Series

Version: 1.0

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Status: Released

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Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

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About the Document

Document Information	
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Subtitle	GNSS Module Series
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Document Status	Released

Revision History

Version	Date	Description
-	2022-03-21	Creation of the document
1.0	2022-06-10	First official release

Contents

1 Reference Design

1.1. Introduction

This document provides the reference design of Quectel LC29H GNSS module, including the design of block diagram, 3.3 V MCU and UART circuits, power supply and I2C circuits, module interfaces and antenna interface.

The LC29H series module includes five variants: LC29H (AA), LC29H (BA)*, LC29H (CA)*, LC29H (DA)* and LC29H (EA)*.

1.1.1. Special Mark

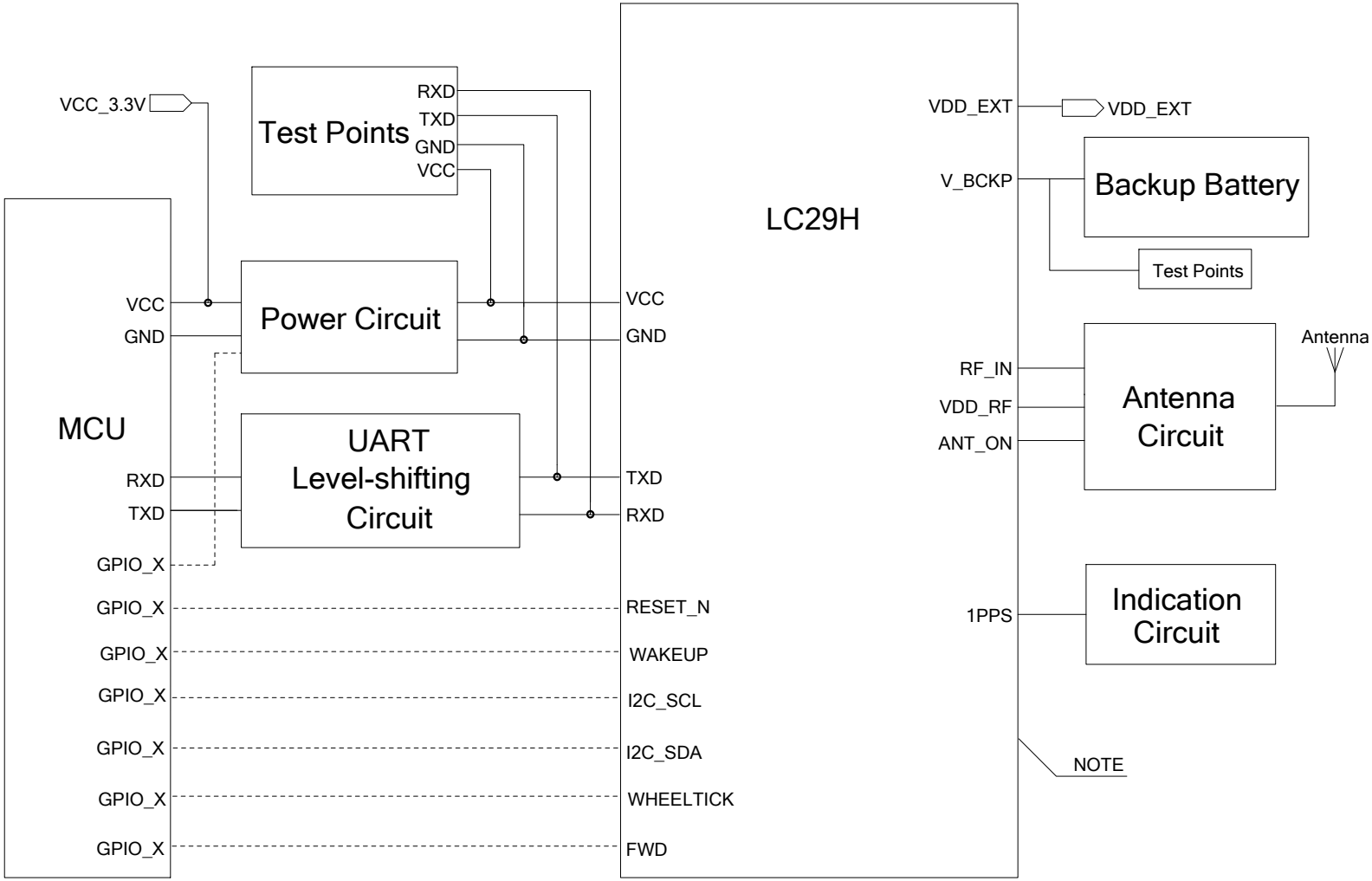
Table 1: Special Mark

Mark	Definition
*	The asterisk (*) after a model indicates that the sample of the model is currently unavailable.

1.2. Schematics

The schematics illustrated in the following pages are provided for your reference only.

Block Diagram



NOTE:

FWD and WHEELTICK are supported by LC29H (BA), LC29H (CA), LC29H (DA) and LC29H (EA).

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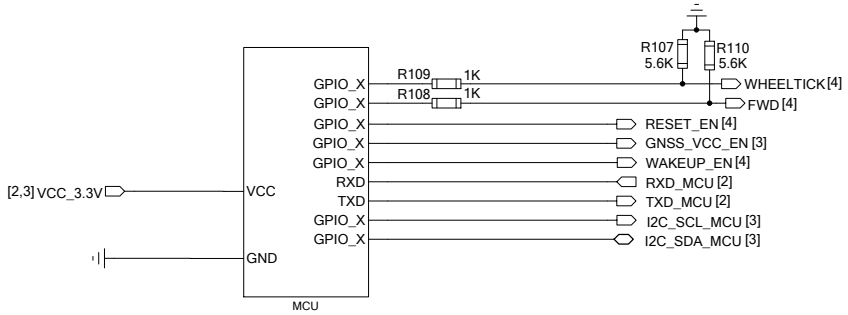
3.3 V MCU and UART Circuits

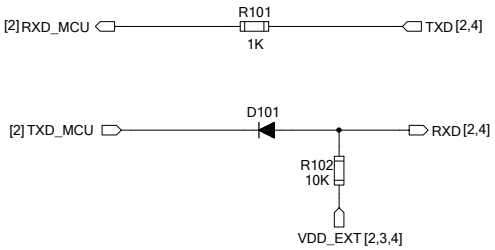
MCU Circuit



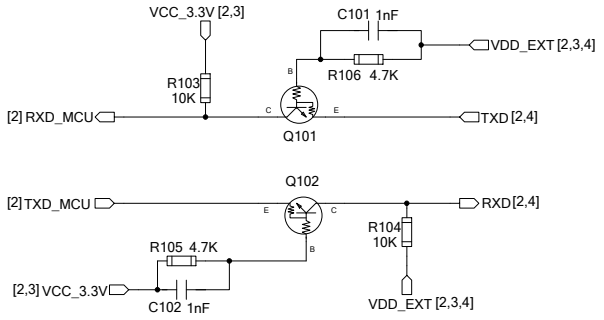
NOTE:

The MCU voltage is VCC_3.3V and the IO voltage of the module is 2.8 V.

UART Level-shifting Circuit - Diode Solution



UART Level-shifting Circuit - Triode Solution



NOTE:

You can refer to the above level-shifting circuit when the IO voltage of MCU does not match that of the module.

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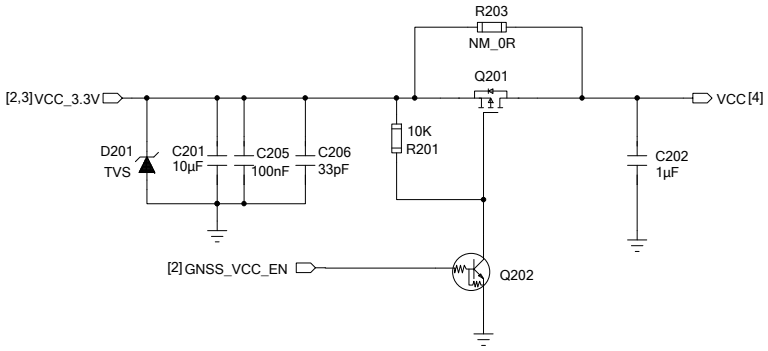
Power Supply and I2C Circuits

VCC Power Supply Control Circuit

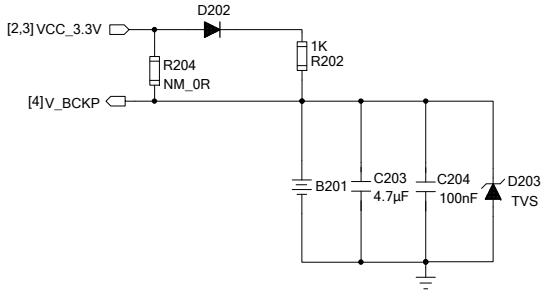


NOTE:

1. This circuit can control the power supply of the module through MCU.
2. The power supply design must meet the sequence requirements in hardware design.

   For more information, see *Quectel_LC29H_Series_Hardware_Design*.

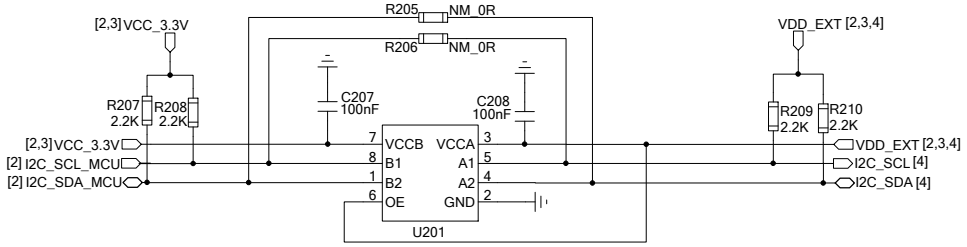
V_BCKP Circuit



NOTE:

1. V_BCKP must be powered before or simutaneously with VCC.
2. The V_BCKP pin should always be powered if hot (warm) start is needed.
3. A suitable resistor (R202) should be selected according to the charging current value of the battery.
4. Enter the Backup mode: Send commands to enter the Backup mode, and then cut off the power supply to the VCC pin and keep the V_BCKP powered.
5. Exit the Backup mode: Restore VCC and then pull the WAKEUP pin high to wake up the module.

I2C Level Converter IC Circuit



NOTE:

1. Generally, the level converter IC solution requires VCCA ≤ VCCB. Please pay attrntion to the voltage relation before using the above circuit.
2. The I2C circuit requires externally pull-up resistors.

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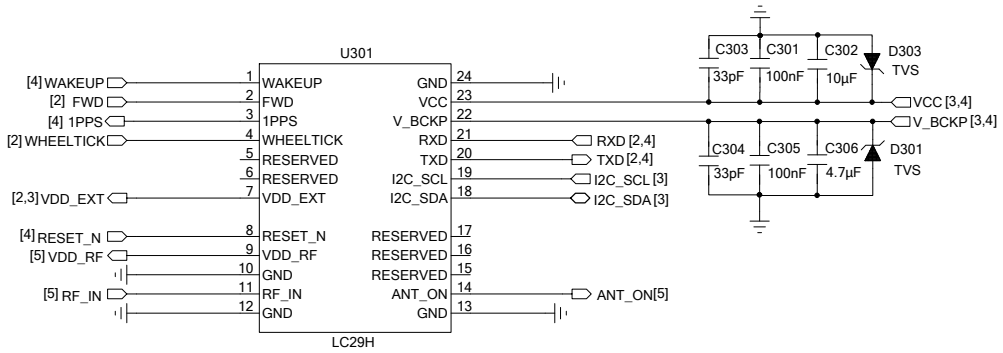
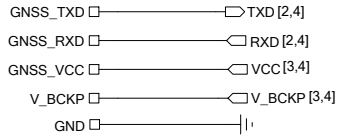
Module Interfaces

Module Interfaces



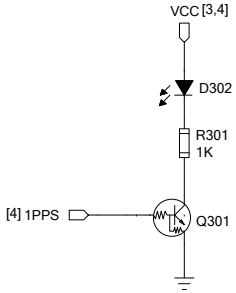
Test Points



NOTE:

1. The UART interface is used for standard NMEA message output, binary data input/output, PAIR/PQTM command input/output and firmware upgrade.
2. The module works normally only if both VCC and V_BCKP pins are powered.
3. If the IO voltage of MCU is not matched with that of the module, a level-shifting circuit must be selected.

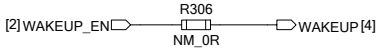
1PPS Indication Circuit



NOTE:

The 1PPS indicator blinks at the frequency of 1 Hz after successful positioning of the module.

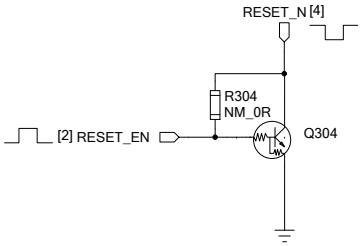
WAKEUP Circuit



NOTE:

1. Use a GPIO that supports push-pull output as WAKEUP_EN.
2. Restore VCC and pull the WAKEUP pin high for at least 10 ms to exit the Backup mode.

RESET_N Circuit



NOTE:

1. The RESET_N pin is pulled up internally to 1.8 V.
2. RESET_N must be connected so that it can be used to reset the module if the module enters an abnormal state.

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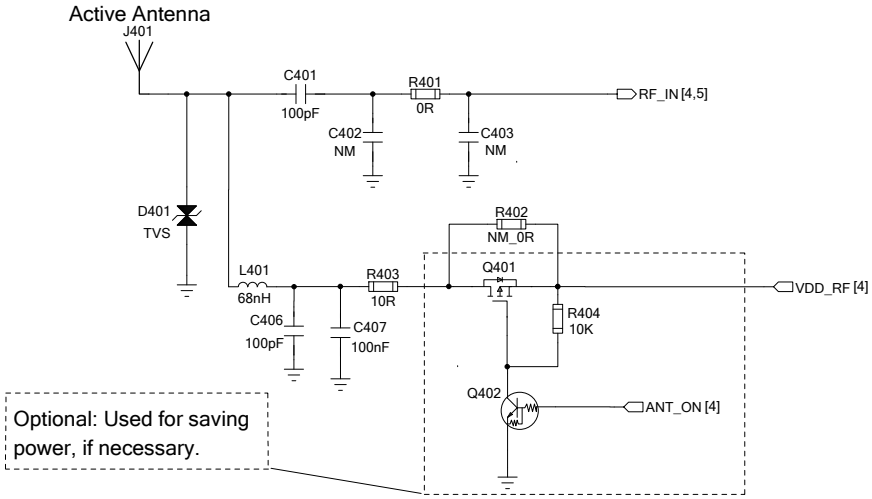
Antenna Interface

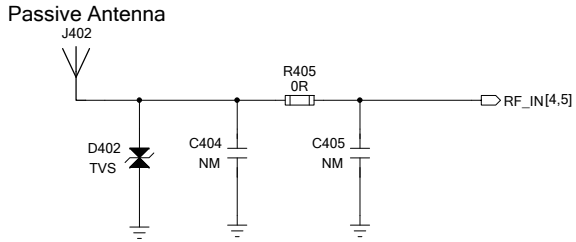
Active Antenna



NOTE:

1. D401 is an electrostatic discharge (ESD) protection device to protect the RF signal input from the potential damage caused by ESD.
2. L401 is used for preventing the RF signal from leaking into the VDD_RF and preventing noise propagation from the VDD_RF to the antenna. L401 routes the bias voltage to the active antenna without losses.
3. The resistor R403 is used for protecting the module in case the active antenna is short-circuited to the ground plane.
4. R401, C402 and C403 form a π matching circuit for antenna impedance modification. By default, R401 is 0 Ω, C402 and C403 are not mounted.
5. The impedance of the RF trace line on the main PCB should be controlled to 50 Ω and the trace length should be kept as short as possible.
6. For more information, see *Quectel_LC29H_Series_Hardware_Design*.

Passive Antenna



NOTE:

1. D402 is an electrostatic discharge (ESD) protection device to protect the RF signal input from the potential damage caused by ESD.
2. R405, C404 and C405 form a π matching circuit for antenna impedance modification. By default, R405 is 0 Ω, C404 and C405 are not mounted.
3. The impedance of the RF trace line on the main PCB should be controlled to 50 Ω and the trace length should be kept as short as possible.
4. For more information, see *Quectel_LC29H_Series_Hardware_Design*.

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