Unbalanced Power Amplifier: An Architecture for Broadband Back-Off Efficiency Enhancement

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***Abstract*— In this article, we present a new broadband power amplifier (PA) architecture with a back-off efficiency enhancement that supports very wide modulation bandwidths. The unbalanced PA is composed of two cooperating sub-PAs using the Lange couplers as input power splitter and output power combiner. The PA operation is controlled by the transistors' width ratio and coupling coefficients of the Lange couplers. The output power back-off (OPBO) level is given by the transistors' width ratio and coupling coefficient of the output coupler, while the maximum efficiency is achieved at the back-off point. These features provide more design flexibility compared with the conventional Doherty PA, where the OPBO can be set only by the transistors' width ratio, and the maximum efficiency is achieved at the peak power. Using broadband harmonic matching networks, the main and auxiliary sub-PAs operate in the continuous mode to improve efficiency over a broad bandwidth. A fully integrated unbalanced PA, implemented in a 250-nm GaN-on-SiC process, achieves 32.2–34.3-dBm output power, 27%–37% efficiency at peak power, and 27%–40% at 5–6-dB back-off, across 4.5–6.5 GHz. The PA provides 3.7/4.5% (−28.6/−26.9 dB) rms error vector magnitude (EVM_{rms}) and 30% average efficiency for a 256-QAM signal with 100-/200-MHz bandwidth, 7.2-dB PAPR, and 25.5-dBm average output power, without using any predistortion.**

***Index Terms*— Back-off, balanced amplifier, broadband circuit, coupler, fifth generation (5G), GaN, load modulation, power amplifier (PA).**

I. Introduction

THE rapid advances in mobile communication systems, such as the new fifth generation (5G) standard, pose stringent requirements on the transmitter and receiver radio frequency (RF) circuits. The power amplifier (PA), as the most critical component of the transmitter, should meet challenging conditions of 5G systems. For complex-modulated signals with large peak-to-average power ratio (PAPR) and wide bandwidth used in 5G, the PA should, first, provide high efficiency even at back-off and, second, maintain high amplitude and phase linearity to efficiently amplify and deliver high-quality signals.

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Several PA architectures are developed for back-off efficiency enhancement, most notably, Doherty PA, outphasing PA, envelope-tracking PA, load-modulated balanced PA, and reconfigurable PA [1]–[15]. The Doherty PA is the most popular architecture in modern communications, mainly as a result of its simple circuit architecture with single-input RF signal and potential of providing linear amplitude and phase characteristics by proper adjustment of bias and phase shift in the two amplifier paths, i.e., the main and auxiliary sub-PAs [2]. The Doherty PA relies on impedance inverters to provide optimum load impedance to the main transistor at both peak power and back-off. The impedance inverters are usually implemented as quarter-wavelength transmission lines or their equivalent lumped circuit elements. These circuits, however, suffer from narrow bandwidth that limits the overall DPA bandwidth [3]. Several techniques are developed to extend the bandwidth of the Doherty PA, including modified impedance of transmission lines in a load modulation network, two-section peaking network, compensation of parasitic capacitances, and dual-input Doherty PA structure [3]. A voltage-mode Doherty PA is proposed in [4] and [5], where two switched-capacitor PAs are combined using a transformer, and the back-off efficiency enhancement is achieved over a broad bandwidth as no impedance inverter is used. However, the circuit operation is predicated on switches that may not provide good performance at high frequencies, e.g., mm-wave, or might not be available in a given process with sufficiently low losses. The voltage-mode Doherty PA can provide wide bandwidth at low RF frequencies, but, at higher frequencies, it could be difficult to maintain a short-circuit output impedance of the auxiliary transistor over a broad bandwidth.

The outphasing PA operates based on splitting the input signal into two parallel signals with their phase dependent on the input amplitude and then combining the amplified (and saturated) signals through proper load impedances [6]. The bandwidth is mainly limited by the frequency response of the required load impedances. Consequently, the outphasing PA usually features a narrow bandwidth and is rarely used in wireless communications. The envelope-tracking PA is sensitive to timing alignment of the envelope signal that can be challenging for wide modulation bandwidths [7].

The load-modulated balanced amplifier architecture is a recently developed approach for the back-off efficiency enhancement [10]–[13], where the load impedance presented to transistors of a balanced PA is modulated using a signal

applied to an isolated port of the output hybrid coupler. This PA architecture can provide wider bandwidths compared with the Doherty PA as a result of a different load-modulation approach that does not rely on the impedance inverters. In the original implementation, the additional signal is generated through an auxiliary amplifier with an external RF signal and must maintain a specific amplitude/phase relationship with respect to the input signal to achieve the expected operation [10]. The additional signal can be generated from the input signal to achieve a single RF input PA [11]. However, an extra PA and a wideband phase shift circuit are required, which can increase the chip area, degrade efficiency, and limit bandwidth.

A reconfigurable PA can provide the back-off efficiency enhancement over a broad bandwidth and improve tolerance to the load's voltage standing wave ratio (VSWR) effects [14]–[16]. The Doherty PA can also use reconfigurable circuitry to extend the bandwidth of the load-modulation network and tune the input network for phase equalization to enhance the efficiency [17]. A disadvantage of these reconfigurable structures is the overhead associated with extra control and tuning circuitry.

In this article, we present a new PA architecture based on a modified balanced amplifier with a broadband back-off efficiency enhancement. The new PA architecture, named unbalanced PA, is composed of two cooperating sub-PAs with the Lange couplers used as the input power splitter and output power combiner. The PA operation is controlled by the transistors' width ratio and coupling coefficients of the couplers. This architecture does not require impedance inverters, such as in the Doherty PA or, and extra PA and phase shift circuitry, such as in the load-modulated balanced PA. It can, therefore, achieve a broadband operation. This article is structured as follows. In Section II, we present the operational theory of the unbalanced PA. The circuit design procedure and details are given in Section III. We provide the measurement results for a fully integrated GaN PA prototype in Section IV, followed by concluding remarks in Section V.

II. Unbalanced PA Architecture

A. Principles of Operation

The proposed unbalanced PA architecture is shown in Fig. 1, in which the quadrature hybrid couplers are used as signal splitter and signal combiner. We start with an intuitive description of the PA operation and then provide a rigorous analysis of its back-off efficiency enhancement and linear operation.

The input power is divided between the main and auxiliary sub-PAs based on the coupling coefficient of the input coupler. The main and auxiliary sub-PAs are, respectively, biased in class-B and class-C modes. Therefore, at low input power levels, only the main sub-PA is working, and the auxiliary sub-PA is OFF. By increasing the input power level, the auxiliary sub-PA gradually turns on and starts contributing to the output power. At this point, the main sub-PA can be either in linear operation or saturated. In order to maximize the efficiency at back-off, the main sub-PA should be at the onset of saturation there, i.e., when the auxiliary sub-PA turns on, the main

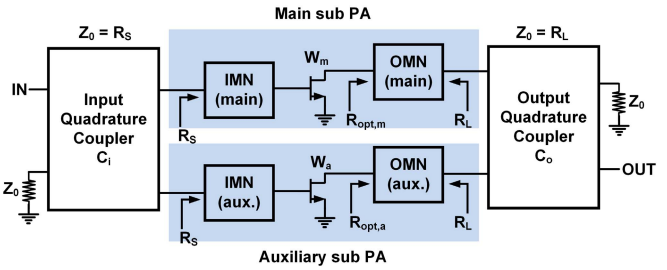


Fig. 1. Proposed unbalanced PA architecture.

sub-PA should be at the edge of saturation. Both sub-PAs would ultimately become saturated upon further increasing the input power level. A larger transistor is used in the auxiliary sub-PA to provide higher saturated output power. The contributions of the main and auxiliary sub-PAs in the total output power are dependent on the coupling coefficient of the output coupler. Therefore, the output power back-off (OPBO) level can be controlled by both the transistors' width ratio and the output coupler's coupling coefficient. This provides more design flexibility compared with the conventional Doherty PA.

The sub-PAs are connected to the input and output matching networks that maintain their impedance matching almost independently of the input power level. In the unbalanced PA architecture, these matching networks are broadband; thus, the impedance matching is not significantly affected by variations of the transistors' parasitic capacitances with the input power.[1] The output signals of the two sub-PAs are combined through the output coupler. The hybrid couplers can be implemented using broadband structures, e.g., the Lange couplers, leading to a broadband PA architecture with a back-off efficiency enhancement. These two features, i.e., using the broadband impedance matching networks and Lange couplers, are essential in improving the unbalanced PA bandwidth compared with the conventional Doherty PA using band-limiting impedance inverters.

It is noteworthy that as the two transistors operate in the class-B and class-C modes, nonlinearities of their transconductance and gate–source capacitance are, respectively, compressive and expansive with respect to power level and, therefore, can compensate for each other's effects [18]. This helps to mitigate the AM–PM distortion of the unbalanced PA, which is an important feature for complex-modulated signals conventionally used in modern communications. However, this requires a careful adjustment of the transistors' nonlinearity profiles.

B. Back-Off Efficiency Enhancement

We present a detailed analysis of the unbalanced PA structure to demonstrate its operational mechanisms. A directional coupler can be described by the following matrix of scattering

[1]This condition may not be valid in a narrowband PA where a change in parasitic capacitances can substantially degrade the impedance matching, e.g., ΔC_{gs} of the auxiliary transistor when it transits between the OFF- and ON-states.

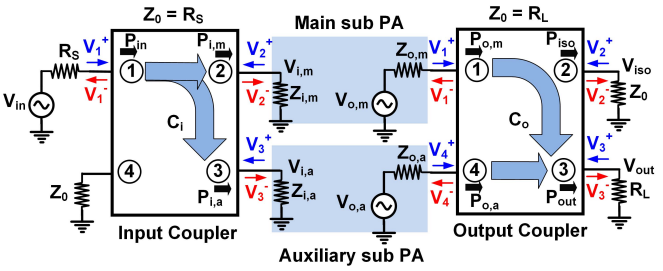


Fig. 2. Equivalent circuit used for the analysis of the unbalanced PA. The incident and reflected voltage wave components are, respectively, shown in blue and red. The desired power flow paths are shown by blue wide arrows.

parameters [19]:

$$[S] = \begin{bmatrix} 0 & a & -jb & 0 \\ a & 0 & 0 & -jb \\ -jb & 0 & 0 & a \\ 0 & -jb & a & 0 \end{bmatrix} \tag{1}$$

where a and b are related to the coupling coefficient of the coupler, $0 < C < 1$, as $a = C$ and $b = (1 - C^2)^{1/2}$. Using the circuit of Fig. 2 (output network) and assuming that the output impedances of the main and auxiliary sub-PAs are matched to the load impedance and the output coupler, i.e., $Z_{o,m} = Z_{o,a} = Z_0 = R_L$, the output voltage is derived as

$$V_{\text{out}} = V_3^- = S_{31}V_1^+ + S_{34}V_4^+ \tag{2}$$

leading to

$$V_{\text{out}} = -j\sqrt{1 - C_o^2}V_{o,m} + C_o V_{o,a}. \tag{3}$$

It should be noted that because the input hybrid coupler provides a 90° phase shift between the input voltages of the main and auxiliary amplifiers, there is also a 90° phase difference between their output voltages, i.e., these can be considered as $V_{o,m} = |V_{o,m}|$ and $V_{o,a} = -j|V_{o,a}|$. For small output coupling coefficients, $|V_{\text{out}}| \approx |V_{o,m}|$, while, for large coupling coefficients, $|V_{\text{out}}| \approx |V_{o,a}|$. Therefore, a moderate coupling coefficient should be chosen to achieve a proper back-off efficiency enhancement. The power delivered to the load $P_{\text{out}} = |V_{\text{out}}|^2/2R_L$ can be determined using (3) as

$$P_{\text{out}} = \left(1 - C_o^2\right)P_{o,m} + C_o^2 P_{o,a} + 2C_o\sqrt{1 - C_o^2}\sqrt{P_{o,m}P_{o,a}} \tag{4}$$

where $P_{o,m} = |V_{o,m}|^2/2R_L$ and $P_{o,a} = |V_{o,a}|^2/2R_L$, respectively, denote the output power of the main and auxiliary sub-PAs.

A part of the power generated by the main and auxiliary sub-PAs is delivered to the isolated port. Using Fig. 2 (output network), the voltage of the isolated port can be obtained as

$$V_{\text{iso}} = V_2^- = S_{21}V_1^+ + S_{24}V_4^+ \tag{5}$$

resulting in

$$V_{\text{iso}} = C_o V_{o,m} - j\sqrt{1 - C_o^2}V_{o,a}. \tag{6}$$

If the output voltage ratio of the main and auxiliary sub-PAs can be maintained as $|V_{o,a}|/|V_{o,m}| = C_o/(1 - C_o^2)^{1/2}$, then

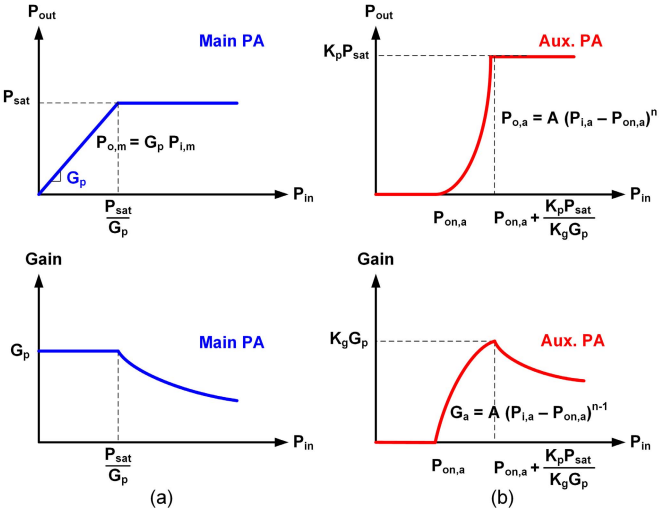


Fig. 3. Simplified models of the sub-PAs' output power and gain versus input power characteristics. (a) Main sub-PA. (b) Auxiliary sub-PA ($A = (K_g G_p)^n/(K_p P_{\text{sat}})^{n-1}$).

$V_{\text{iso}} = 0$, and the power delivered to the isolated port becomes zero. However, this is not a requisite to achieve a high efficiency at back-off where $V_{o,a} = 0$. The power delivered to the isolated port is derived as

$$P_{\text{iso}} = C_o^2 P_{o,m} + \left(1 - C_o^2\right)P_{o,a} - 2C_o\sqrt{1 - C_o^2}\sqrt{P_{o,m}P_{o,a}}. \tag{7}$$

It is noticed that $P_{\text{out}} + P_{\text{iso}} = P_{o,m} + P_{o,a}$, as expected from the power conservation law. In fact, this four-port output power combiner improves the PA bandwidth but at a cost of reduced efficiency due to the power loss in the isolated port. P_{iso} should be minimized to improve the efficiency of the output power combiner. We discuss this issue in detail shortly.

The output power and gain versus input power characteristics of the two sub-PAs can be modeled as shown in Fig. 3.[2] The main sub-PA biased in class-AB is modeled by a linear power gain of G_P up to saturation where the output power is assumed to be constant at P_{sat}. The input saturation power level is given by P_{sat}/G_p. The auxiliary sub-PA is biased in class-C with an input turn-on power level of $P_{on,a}$. Both the output power and gain are zero for the input power levels below $P_{on,a}$ and gradually increase after the turn on. The dependence of the output power and gain on the input power is nonlinear, and we describe this as

$$P_{o,a} = A(P_{i,a} - P_{on,a})^n \tag{8}$$

$$G_a = A(P_{i,a} - P_{on,a})^{n-1} \tag{9}$$

where n is a bias- and process-dependent parameter (typically $1 < n < 2$). Parameter A can be determined as follows. We assume that the output power at saturation and power gain of the auxiliary sub-PA are, respectively, given by $K_p P_{\text{sat}}$ and

[2]These models are fairly accurate in the linear and saturation power ranges. Their accuracy degrades in transitions from the OFF-state to ON-state and from linear to saturation. For the analysis presented here, these effects can be neglected.

$K_g G_p$. The parameters K_p and K_g are defined as

$$K_p = \frac{P_{\text{sat},a}}{P_{\text{sat},m}} \tag{10}$$

$$K_g = \frac{G_{p,a}}{G_{p,m}}. \tag{11}$$

Using (8)–(11), $A = (K_g G_p)^n/(K_p P_{\text{sat}})^{n-1}$, while the input saturation power of the auxiliary sub-PA is derived as $P_{on,a} + K_p P_{\text{sat}}/K_g G_p$, as shown in Fig. 3(b). The width of auxiliary transistor W_a is larger than that of the main transistor W_m by a factor of K_w

$$K_w = \frac{W_a}{W_m}. \tag{12}$$

Therefore, its linear power gain and saturated output power level are also scaled with respect to that of the main transistor. Relationship between the saturated power ratio K_p, power gain ratio K_g, and the transistors' width ratio K_w is dependent on the process and, somehow, the frequency of operation. The output power level of transistors is roughly scaled with their width, $K_p \approx K_w$, while the gain of transistors usually does not scale proportionally but tends to remain constant or even degrade for larger devices due to increased losses (in this design, $K_g \approx 1$). Furthermore, as the auxiliary transistor is based in class-C, its power gain can be lower than that of the class-AB biased main transistor. The auxiliary sub-PA can turn on either just before or after the saturation of the main sub-PA. We choose the PA parameters, such that the onset of the main sub-PA saturation coinciding with the turn-on of the auxiliary sub-PA, and define the associated input power to the PA as the input back-off power $P_{\text{in,bo}}$.

Using (4) and (10), the output power level at peak-power and back-off can be derived as

$$P_{\text{out,pp}} = \left(\sqrt{1 - C_o^2} + \sqrt{K_p} C_o\right)^2 P_{\text{sat}} \tag{13}$$

$$P_{\text{out,bo}} = \left(1 - C_o^2\right) P_{\text{sat}} \tag{14}$$

resulting in the OPBO level of

$$\text{OPBO} = 20 \log_{10}\left[1 + \frac{\sqrt{K_p} C_o}{\sqrt{1 - C_o^2}}\right]. \tag{15}$$

It is noted that the back-off level is dependent on the transistors' power ratio and the coupling coefficient of the output coupler. In Fig. 4, OPBO is shown versus parameters K_p and C_o. For a 3-dB coupler ($C_o = 1/\sqrt{2}$), the 6-dB back-off requires $K_p = 1$, which is the same as in the Doherty PA. For lower coupling coefficients, e.g., -4.8 dB ($C_o = 1/\sqrt{3}$), the transistors' power ratio should be greater ($K_p = 2$).

We will compare the features of the unbalanced PA and the Doherty PA throughout this article. At this point, we note that the back-off level can be controlled by two parameters in the unbalanced PA, while it can only be adjusted by the transistors' width ratio in the Doherty PA. If we assume that the width of the auxiliary transistor is twice of the main transistor and $K_p = K_w = 2$, the back-off level of the Doherty PA is derived as $\text{OPBO} = 20 \log_{10}(1 + K_p) = 9.5$ dB, while, in the unbalanced PA, it can be controlled within a wide range, as indicated by (15) and Fig. 4.

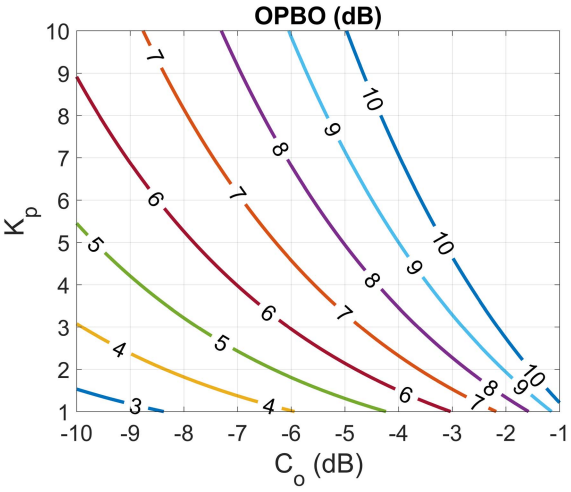


Fig. 4. OPBO level versus the transistors' power ratio K_p and the coupling coefficient of the output coupler C_o.

The output power combiner, as discussed earlier, features an imperfect efficiency due to the power loss in the isolated port. We derive the efficiency of the combiner and investigate effects of the output coupler's coupling coefficient on its performance. The combiner's efficiency is given by

$$\eta_{\text{comb}} = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{iso}}} = \frac{P_{\text{out}}}{P_{o,m} + P_{o,a}}. \tag{16}$$

Using (4), it can be expressed as

$$\eta_{\text{comb}} = \frac{\left(\sqrt{1 - C_o^2} + C_o \sqrt{P_{o,a}/P_{o,m}}\right)^2}{1 + P_{o,a}/P_{o,m}} \tag{17}$$

which is a function of C_o and the power ratio $P_{o,a}/P_{o,m}$. In Fig. 5, the combiner efficiency is shown versus normalized output power for different C_o values. In the back-off, $\eta_{\text{comb,bo}} = 1 - C_o^2$; therefore, using lower coupling coefficients is preferred for higher efficiency. At the peak power, $P_{o,a}/P_{o,m} = K_p$, where K_p is derived from (15) for a given OPBO. The combiner efficiency $\eta_{\text{comb,pp}}$ reduces for lower coupling coefficients. There is a power level between the back-off and peak power where the combiner efficiency becomes 100%. This is the point where power delivered to the isolated port is zero, which, per (7), is derived as $P_{o,a}/P_{o,m} = C_o^2/(1 - C_o^2)$. It can be shown that this happens at the normalized output power level of $-\text{OPBO} - 20 \log_{10}(1 - C_o^2)$, e.g., at -4.5-dB back-off level for $\text{OPBO} = 6$ dB and $C_o = -8$ dB.

The input power applied to the PA is distributed between the main and auxiliary sub-PAs. Using the circuit shown in Fig. 2 (input network), assuming that the input impedance of the sub-PAs is matched to the input coupler and input source impedances, i.e., $Z_{i,m} = Z_{i,a} = Z_0 = R_S$, it can be shown that

$$V_{i,m} = V_2^- = S_{21} V_1^+ = C_i V_{\text{in}} \tag{18}$$

$$V_{i,a} = V_3^- = S_{31} V_1^+ = -j\sqrt{1 - C_i^2} V_{\text{in}} \tag{19}$$

where C_i is the coupling coefficient of the input hybrid coupler. The input power delivered to the main and auxiliary

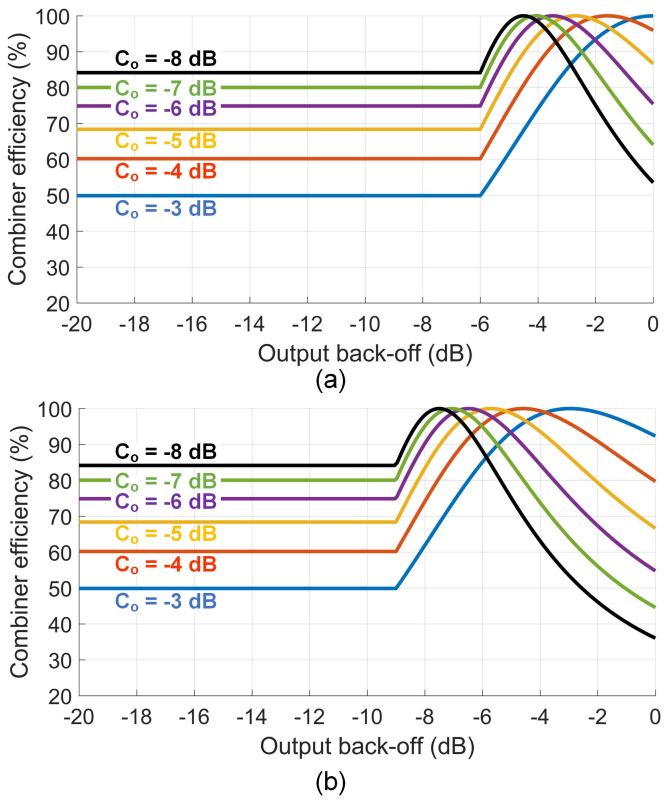


Fig. 5. Output combiner efficiency versus normalized output power for different coupling coefficients of the output combiner. (a) 6-dB OPBO. (b) 9-dB OPBO.

sub-PAs is given by

$$P_{i,m} = C_i^2 P_{\text{in}} \tag{20}$$

$$P_{i,a} = \left(1 - C_i^2\right) P_{\text{in}}. \tag{21}$$

Therefore, the output power of the main and auxiliary sub-PAs is derived in terms of the input power as follows:

$$P_{o,m} = \begin{cases} G_p C_i^2 P_{\text{in}} & P_{\text{in}} < P_{\text{in,bo}} \\ P_{\text{sat}} & P_{\text{in}} \geq P_{\text{in,bo}} \end{cases} \tag{22}$$

$$P_{o,a} = \begin{cases} 0 & P_{\text{in}} < P_{\text{in,bo}} \\ A\left(1 - C_i^2\right)^n (P_{\text{in}} - P_{\text{in,bo}})^n & P_{\text{in,bo}} \leq P_{\text{in}} < P_{\text{in,pp}} \\ P_{\text{sat},a} & P_{\text{in}} \geq P_{\text{in,pp}} \end{cases} \tag{23}$$

where $P_{\text{in,bo}}$ and $P_{\text{in,pp}}$ are, respectively, the input power levels at the back-off and peak-power, given by

$$P_{\text{in,bo}} = \frac{1}{C_i^2} \frac{P_{\text{sat}}}{G_p} = \frac{P_{on,a}}{1 - C_i^2} \tag{24}$$

$$P_{\text{in,pp}} = \left[\frac{1}{C_i^2} + \frac{K_p}{K_g} \frac{1}{1 - C_i^2}\right] \frac{P_{\text{sat}}}{G_p}. \tag{25}$$

Using (24), the required turn-on power level of the auxiliary sub-PA can be derived. The input–output power characteristic of the unbalanced PA can be derived using (4), (22), and (23).

The total efficiency of the unbalanced PA can be derived as

$$\eta = \frac{\left(1 - C_o^2\right) P_{o,m} + C_o^2 P_{o,a} + 2C_o \sqrt{1 - C_o^2} \sqrt{P_{o,m} P_{o,a}}}{\frac{1}{\eta_m} P_{o,m} + \frac{1}{\eta_a} P_{o,a}} \tag{26}$$

where η_m and η_a, respectively, denote the efficiencies of the main and auxiliary sub-PAs. Using (22), (23), and (26), the efficiency at back-off and peak-power is given by

$$\eta_{\text{bo}} = \left(1 - C_o^2\right) \eta_m \tag{27}$$

$$\eta_{\text{pp}} = \frac{\left(\sqrt{1 - C_o^2} + \sqrt{K_p} C_o\right)^2}{\frac{1}{\eta_m} + \frac{K_p}{\eta_a}}. \tag{28}$$

It is noted that the efficiency at back-off and peak-power can be different. Using (15), (27), and (28), it can be shown that

$$\frac{\eta_{\text{bo}}}{\eta_{\text{pp}}} = \left[1 + K_p \frac{\eta_m}{\eta_a}\right] 10^{-\text{OPBO}/20} \tag{29}$$

which is larger than unity for $K_p > (10^{\text{OPBO}/20} - 1)\eta_a/\eta_m$. For the 6-dB back-off level and $\eta_a = \eta_m$,[3] it can be satisfied for $K_p > 1$, i.e., $C_o < 1/\sqrt{2}$. Therefore, a smaller output coupling coefficient is preferred to achieve higher back-off efficiency.

At the output power levels other than the peak-power and back-off, the efficiency (26) is power-dependent through $P_{o,m}$, $P_{o,a}$, η_m, and η_a. To obtain η_m and η_a in terms of the input power, we first note that the drain current of a short-channel transistor in the saturation is given by

$$I_D \approx k_0 W (V_{\text{GS}} - V_T) \tag{30}$$

where k_0 is a process-dependent parameter, W is the transistor's width, V_{GS} is the gate–source voltage, and V_T denotes the threshold (pinch-off) voltage of the enhancement (depletion) mode transistor [20]. We assume that an RF signal in the form of

$$V_{\text{GS}}(t) = V_{\text{GS0}} + V_{\text{RF}} \cos(\omega_0 t) \tag{31}$$

is applied to the transistor. The drain current waveform is dependent on the bias mode. If the transistor is biased in the class-B mode, i.e., $V_{\text{GS0}} = V_T$, as intended for the main sub-PA, the resulting drain current is a half-wave sinusoid with a peak of $k_0 W V_{\text{RF}}$. Both the dc and fundamental components of this waveform, I_{D0} and I_{D1}, are proportional to V_{RF}. As a result, the dc and RF power components change as $P_{\text{dc}} = V_{\text{DD}} I_{D0} \propto V_{\text{RF}}$ and $P_{\text{RF}} \propto R_{\text{opt}} I_{D1}^2 \propto V_{\text{RF}}^2$, leading to $\eta = P_{\text{RF}}/P_{\text{dc}} \propto V_{\text{RF}}$. For a matched transistor, $P_{\text{in}} \propto V_{\text{RF}}^2$; thus, $\eta \propto \sqrt{P_{\text{in}}}$. Therefore, the efficiency of the main sub-PA can be expressed as

$$\eta_m = \begin{cases} \eta_{m,\max} \sqrt{\dfrac{P_{\text{in}}}{P_{\text{in,bo}}}} & P_{\text{in}} < P_{\text{in,bo}} \\ \eta_{m,\max} & P_{\text{in}} \geq P_{\text{in,bo}} \end{cases} \tag{32}$$

where $\eta_{m,\max}$ denotes the maximum efficiency at saturation, e.g., $\eta_{m,\max} = \pi/4 = 78.5\%$ in the class-B mode.

If the transistor is biased in the class-C mode, i.e., $V_{\text{GS0}} < V_T$, as intended for the auxiliary sub-PA, a different

[3] At back-off, in this unbalanced PA, the main and auxiliary sub-PAs operate, respectively, in their saturation and back-off; thus, typically $\eta_m > \eta_a$.

scenario should be considered. The conduction angle α of the current waveform is derived using (30) and (31) as

$$\alpha = 2\cos^{-1}\left[\frac{V_T - V_{GS0}}{V_{RF}}\right] \tag{33}$$

which is dependent on the RF voltage amplitude. Conventionally, the conduction angle is defined at the maximum RF voltage, which leads to the PA saturation. It can be shown that the current waveform components I_{D0} and I_{D1} are derived as

$$I_{D0}(\alpha) = \frac{k_0 W V_{RF}}{2\pi}\frac{2\sin\left(\frac{\alpha}{2}\right) - \alpha\cos\left(\frac{\alpha}{2}\right)}{1-\cos\left(\frac{\alpha}{2}\right)} \tag{34}$$

$$I_{D1}(\alpha) = \frac{k_0 W V_{RF}}{2\pi}\frac{\alpha - \sin(\alpha)}{1-\cos\left(\frac{\alpha}{2}\right)}. \tag{35}$$

The dc power is given by $P_{dc} = V_{DD} I_{D0}(\alpha)$, while the RF power is derived as $P_{RF} = (1/2)R_{opt}(\alpha)I_{D1}^2(\alpha) \approx (1/2)[V_{DD}/I_{D1,max}(\alpha)]I_{D1}^2(\alpha)$, where $I_{D1,max}$ denotes the fundamental drain current component at the maximum RF voltage $V_{RF,max}$. Therefore, using (34) and (35), the efficiency can be expressed as

$$\eta_a(\alpha) \approx \frac{1}{2}\frac{I_{D1}^2(\alpha)}{I_{D1,max}(\alpha) I_{D0}(\alpha)} = \eta_{a,max}(\alpha)\frac{V_{RF}}{V_{RF,max}} \tag{36}$$

where $\eta_{a,max}(\alpha)$ is the maximum efficiency of the class-C PA at saturation

$$\eta_{a,max}(\alpha) = \frac{1}{4}\frac{\alpha - \sin(\alpha)}{\sin\left(\frac{\alpha}{2}\right) - \frac{\alpha}{2}\cos\left(\frac{\alpha}{2}\right)}. \tag{37}$$

The parameter $V_{RF}/V_{RF,max}$ can be related to the input power using $V_{RF} \propto \sqrt{P_{in}}$ and noting that the auxiliary sub-PA turns on at $P_{in,bo}$ and reaches the saturation at $P_{in,pp}$. Therefore, the efficiency of the auxiliary sub-PA can be expressed as

$$\eta_a = \begin{cases} 0 & P_{in} < P_{in,bo} \\ \eta_{a,max}\sqrt{\dfrac{P_{in} - P_{in,bo}}{P_{in,pp} - P_{in,bo}}} & P_{in,bo} \le P_{in} < P_{in,pp} \\ \eta_{a,max} & P_{in} \ge P_{in,pp} \end{cases} \tag{38}$$

where $\eta_{a,max}$ is given by (37).

The total efficiency of the unbalanced PA (26) can be derived versus the output power, as shown in Fig. 6.[4] It is assumed that the maximum efficiencies of the main and auxiliary sub-PAs are, respectively, $\eta_{m,max} = 78.5\%$ (class-B) and $\eta_{a,max} = 85.5\%$ (class-C with conduction angle of $\alpha = 0.8\pi$), while the coupling coefficient of the input coupler is $C_i = -3$ dB. It is noted that by decreasing the coupling coefficient of the output coupler C_o, the back-off efficiency η_{bo} improves at the cost of the reduced peak-power efficiency η_{pp}. For small C_o, $\eta_{bo} \to \eta_m$, as expected from (27). It is also possible to achieve a Doherty-like behavior, e.g., for $C_o \approx -6$ dB, but higher efficiency at back-off is preferred for modulated signals with large PAPR, in which their probability density function (pdf) is mostly concentrated around the back-off.

[4]In practice, the power gain of the auxiliary sub-PA is also dependent on the conduction angle. This effect is neglected here to simplify the analysis.

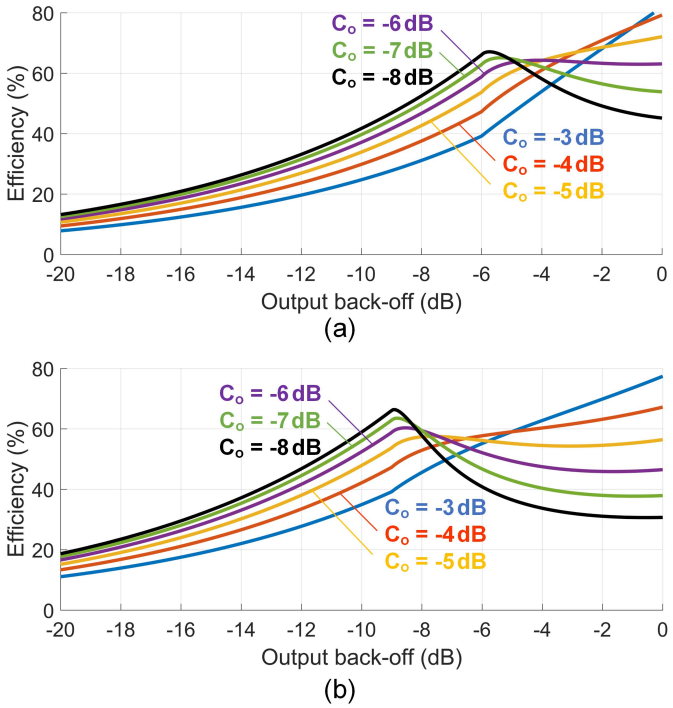


Fig. 6. Efficiency of the unbalanced PA versus normalized output power. (a) 6-dB OPBO. (b) 9-dB OPBO. The maximum efficiencies of the main and auxiliary sub-PAs are, respectively, $\eta_{m,max} = 78.5\%$ (class-B) and $\eta_{a,max} = 85.5\%$ (class-C with conduction angle of $\alpha = 0.8\pi$). $C_i = -3$ dB and $n = 1.5$ are assumed.

The gain of the unbalanced PA can be derived using the models developed for the output combiner (4), input splitter (20) and (21), and sub-PAs (22) and (23). Especially, the gain at output back-off and peak power, using (13), (14), (24), and (25), can be derived as

$$G_{bo} = C_i^2(1 - C_o^2)G_p \tag{39}$$

$$G_{pp} = \frac{\left(\sqrt{1-C_o^2} + \sqrt{K_p}C_o\right)^2}{\frac{1}{C_i^2} + \frac{K_p}{K_g}\frac{1}{1-C_i^2}}G_p. \tag{40}$$

In Fig. 7, the gain of the unbalanced PA is shown versus the output power. It is assumed that the gains of the main and auxiliary sub-PAs are, respectively, $G_p = 10$ and $G_{p,a} = K_g G_p$, where $K_g \approx 1$ and K_p is determined based on OPBO and C_o using (15). Also, $C_i = -3$ dB is considered in simulations.

The effects of the coupling coefficient of the input coupler on the efficiency and gain of the unbalanced PA are illustrated in Fig. 8. The efficiency is very slightly affected by C_i, while a larger C_i helps to achieve a higher gain. Furthermore, it is noted that for some C_i values, e.g., -5 dB $< C_i < -4$ dB, gain variations in the back-off range can be minimized. This reduces the AM–AM distortion of the PA, which is especially important for high-PAPR modulated signals. We can set C_i to achieve $G_{bo} = G_{pp}$, which, using (39), (40), and (4), results in

$$C_i = \left[\frac{10^{OPBO/10} - 1}{10^{OPBO/10} - 1 + K_p/K_g}\right]^{1/2}. \tag{41}$$

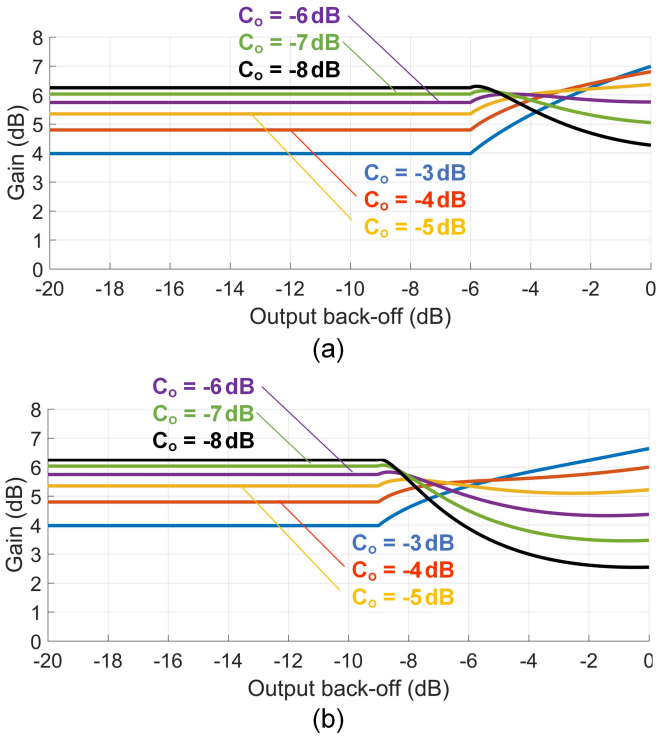


Fig. 7. Gain of the unbalanced PA versus normalized output power. (a) 6-dB OPBO. (b) 9-dB OPBO. Gains of the main and auxiliary sub-PAs are, respectively, $G_p = 10$ and $K_g G_p = 10$. $C_i = -3$ dB and $n = 1.5$ are assumed.

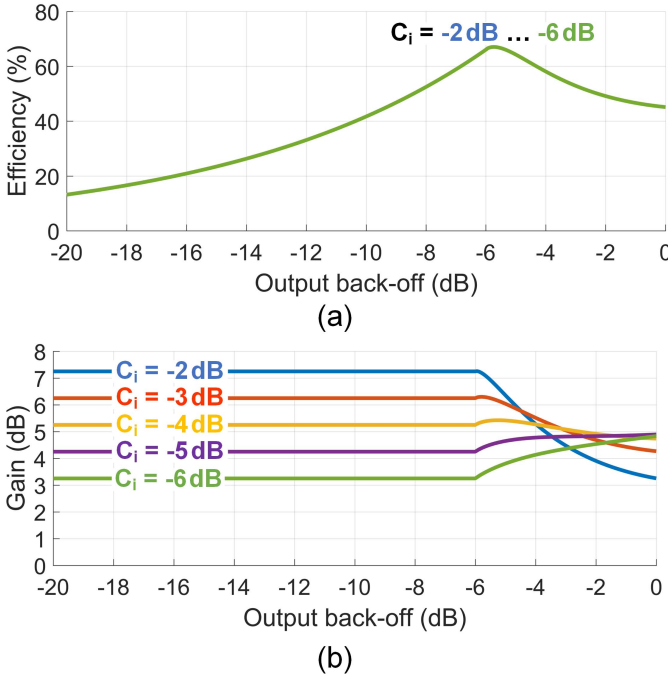


Fig. 8. Effects of the input coupler coupling coefficient on the efficiency and gain of the unbalanced PA. (a) Efficiency. (b) Gain. OPBO = 6 dB, $C_o = -8$ dB, and $n = 1.5$ are assumed.

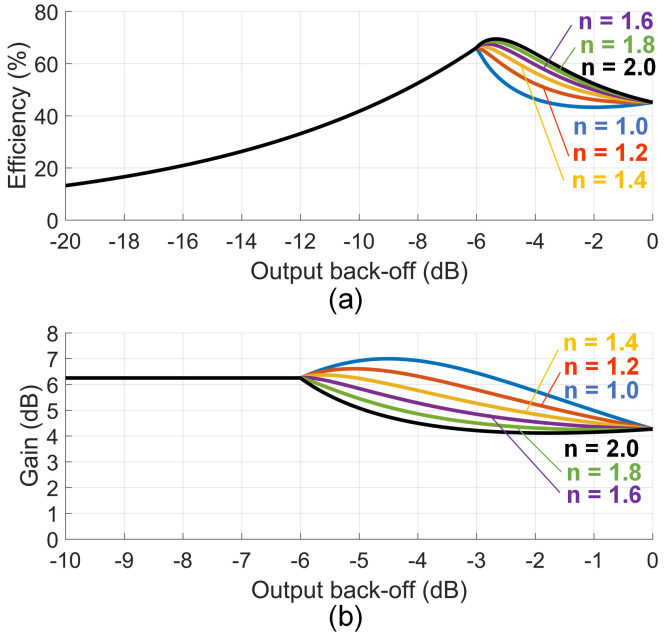


Fig. 9. Effects of the class-C auxiliary sub-PA nonlinearity parameter n, in $P_{o,a} = A(P_{i,a} - P_{on,a})^n$, on the efficiency and gain of the unbalanced PA. (a) Efficiency. (b) Gain. OPBO = 6 dB, $C_o = -8$ dB, and $C_i = -3$ dB are assumed.

For OPBO = 6 dB, $C_o = -8$ dB, and $K_g = 1$, the optimum C_i is derived as $C_i = -4.4$ dB. It should be noted that still there are some gain variations in the back-off to peak-power range, dependent on the nonlinearity profiles of two sub-PAs, e.g., the parameter n, but are usually small.

There is another important consideration to determine C_i based on the input power requirements of the main and auxiliary sub-PAs. Using (20) and (21) in saturation, C_i can be derived as

$$C_i = \frac{1}{\sqrt{1 + P_{i,a}/P_{i,m}}} = \frac{1}{\sqrt{1 + K_p/K_g}}. \tag{42}$$

For OPBO = 6 dB, $C_o = -8$ dB, and $K_g = 1$, this results in $C_i = -8.0$ dB. So far, we discussed three criteria to set C_i based on gain, gain variations, and input power drive requirements. If the sub-PAs are realized as single-stage amplifiers, C_i should be chosen based on the input power drive requirement to ensure proper operation of the unbalanced PA. However, in the case that the sub-PAs use multistage amplifiers, C_i can be set to minimize gain variations, while gain requirements are satisfied by driver stages.

The last point is the effect of auxiliary sub-PA's nonlinear model parameter n on the unbalanced PA performance. In Fig. 9, the efficiency and power gain versus output back-off are shown for $1 \leq n \leq 2$. Larger n results in slightly higher efficiency in the back-off to peak-power range, while the efficiency at the back-off and peak-power is independent of this parameter. Furthermore, minimum gain variations are achieved at moderate values of n.

C. Linear Operation

We derive small-signal scattering parameters of the unbalanced PA in terms of the sub-PAs' scattering parameters and hybrid couplers' coupling coefficients. It is assumed that the sub-PAs are unilateral, i.e., $S_{12} = 0$, to simplify the analysis.

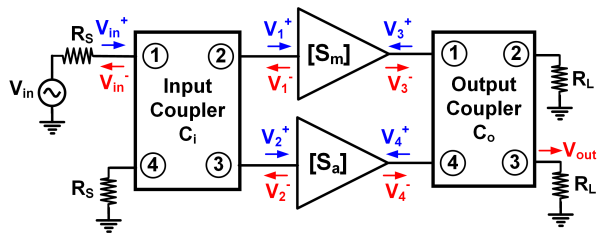


Fig. 10. Circuit used to derive scattering parameters of the unbalanced PA.

Using the circuit shown in Fig. 10 and (1), the incident voltage waves V_1^+ and V_2^+ are derived as

$$V_1^+ = C_i V_{\text{in}}^+ \tag{43}$$

$$V_2^+ = -j\sqrt{1-C_i^2}\,V_{\text{in}}^+. \tag{44}$$

Since the amplifiers are assumed to be unilateral, reflected voltage waves at their input ports are given by

$$V_1^- = S_{11,m} V_1^+ \tag{45}$$

$$V_2^- = S_{11,a} V_2^+. \tag{46}$$

Therefore, the input reflected wave is derived as

$$V_{\text{in}}^- = C_i V_1^- - j\sqrt{1-C_i^2}\,V_2^-. \tag{47}$$

The input reflection coefficient of the unbalanced PA can be derived using (43)–(47) and $S_{11,\text{UPA}} = V_{\text{in}}^-/V_{\text{in}}^+$ as

$$S_{11,\text{UPA}} = C_i^2 S_{11,m} - \left(1-C_i^2\right) S_{11,a}. \tag{48}$$

Similarly, it can be shown that the output reflection coefficient is derived as

$$S_{22,\text{UPA}} = -\left(1-C_o^2\right) S_{22,m} + C_o^2 S_{22,a}. \tag{49}$$

Moreover, voltage waves at output ports of the sub-PAs are given by

$$V_3^- = S_{21,m} V_1^+ \tag{50}$$

$$V_4^- = S_{21,a} V_2^+. \tag{51}$$

Therefore, the output voltage wave is derived as

$$V_{\text{out}} = -j\sqrt{1-C_o^2}\,V_3^- + C_o V_4^-. \tag{52}$$

Using (43), (44), and (50)–(52), the gain of the unbalanced PA $S_{21,\text{UPA}} = V_{\text{out}}/V_{\text{in}}^+$ is derived as follows:

$$S_{21,\text{UPA}} = -j\left[C_i\sqrt{1-C_o^2}\,S_{21,m} + C_o\sqrt{1-C_i^2}\,S_{21,a}\right]. \tag{53}$$

If the two sub-PAs are designed such that $S_{11,m} = S_{11,a}$ and $S_{22,m} = S_{22,a}$, (48) and (49) are simplified to

$$S_{11,\text{UPA}} = -\left(1-2C_i^2\right) S_{11,\text{PA}} \tag{54}$$

$$S_{22,\text{UPA}} = -\left(1-2C_o^2\right) S_{22,\text{PA}} \tag{55}$$

indicating that the input and output reflection coefficients of the unbalanced PA are smaller than that of the constituent sub-PAs by the factors of $|1-2C_i^2|$ and $|1-2C_o^2|$, respectively. It is noted that the unbalanced PA still partially inherits the impedance matching improvement feature of the conventional balanced PA. This feature alleviates the design of output and input matching networks of the sub-PAs. Furthermore, this reduces the sensitivity of the PA to the load (e.g., antenna) impedance variations, which is an important challenge in 5G applications. In the case of balanced PA with identical sub-PAs and 3-dB couplers, i.e., $C_i = C_o = 1/\sqrt{2}$, these results are simplified to $S_{11,\text{UPA}} = S_{22,\text{UPA}} = 0$ and $S_{21,\text{UPA}} = -jS_{21,\text{PA}}$, as expected [19].

D. Bandwidth Considerations

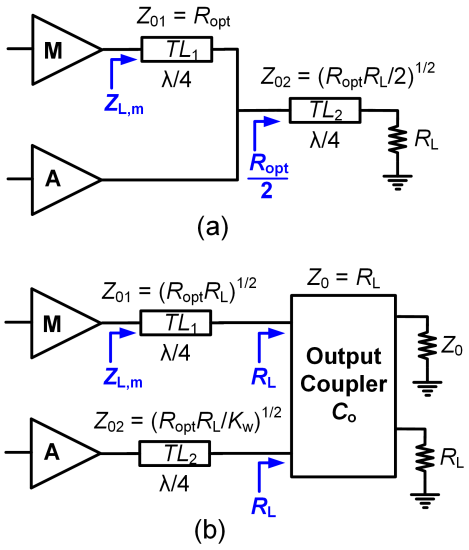
The unbalanced PA can potentially provide wider bandwidth compared with the Doherty PA as a result of using the broadband Lange couplers rather than the narrowband impedance inverters for load modulation. We elaborate on the bandwidth considerations for the unbalanced PA to clarify its advantages over the Doherty PA.

The Lange couplers can provide wide bandwidth, e.g., a full octave, dependent on their layout structure and implementation process. Their coupling coefficient and phase response deviate from the targeted values at the edges of the frequency band, leading to degraded performance of the unbalanced PA (it will be further discussed in Section III-A). The bandwidth of the Lange couplers is usually much higher than that of other sub-circuits of the unbalanced PA.

The Doherty PA has a limited bandwidth at back-off due to the high impedance transformation ratio of the impedance inverter [3]. For a simple comparison between the unbalanced and Doherty PAs, we assume that the output matching networks of the unbalanced PA are realized using $\lambda/4$ transmission lines. In the circuits shown in Fig. 11, the characteristic impedance of the transmission lines is chosen for a 6-dB OPBO level. The impedance transformation ratio of the transmission lines in the two architectures is summarized in Fig. 11(c). In the Doherty PA at back-off, the impedance transformation ratio of the transmission lines TL_1 and TL_2 are, respectively, derived as 4 and $R_{\text{opt}}/2R_L$; hence, the bandwidth would tend to be significantly limited by TL_1. In the unbalanced PA, the impedance transformation ratios are given by R_{opt}/R_L and $R_{\text{opt}}/K_w R_L$ (note that $W_a = K_w W_m$; thus, $R_{\text{opt},a} = R_{\text{opt}}/K_w$), at both back-off and peak-power, where TL_1 is mainly important at back-off. For typical circuit parameters, R_{opt}/R_L is usually lower than 4, which indicates the potential of the unbalanced PA in providing wider bandwidth at back-off.[5]

The output matching networks of the sub-PAs should transform the load resistance R_L to the optimum resistance of the transistors, $R_{\text{opt},m}$ and $R_{\text{opt},a}$, while absorbing the output parasitic capacitance of the transistors, $C_{\text{out},m}$ and $C_{\text{out},a}$. The bandwidth of these matching networks is dependent on their impedance transformation ratio, $R_{\text{opt},m}/R_L$ and $R_{\text{opt},a}/R_L$, as well as quality factors of the optimum load impedances, $Q_{L,m} = \omega_c R_{\text{opt},m} C_{\text{out},m}$ and $Q_{L,a} = \omega_c R_{\text{opt},a} C_{\text{out},a}$ (ω_c is center of the band) [21]. It should be noted that the bandwidth

[5]For small R_{opt} values, e.g., in low-voltage CMOS processes, R_{opt}/R_L can be lower than 1/4, indicating higher impedance transformation ratio of TL_1 and, therefore, narrower bandwidth of the unbalanced PA at back-off. However, the $\lambda/4$ transmission lines can be replaced with higher order matching networks to extend the bandwidth of the unbalanced PA, while this is not possible in the Doherty PA.



Impedance Transformation Ratio

	Doherty PA		Unbalanced PA	
	BO	PP	BO	PP
TL_1	4	1	$\frac{R_{opt}}{R_L}$	$\frac{R_{opt}}{R_L}$
TL_2	$\frac{R_{opt}}{2R_L}$	$\frac{R_{opt}}{2R_L}$	—	$\frac{R_{opt}}{K_wR_L}$

(c)

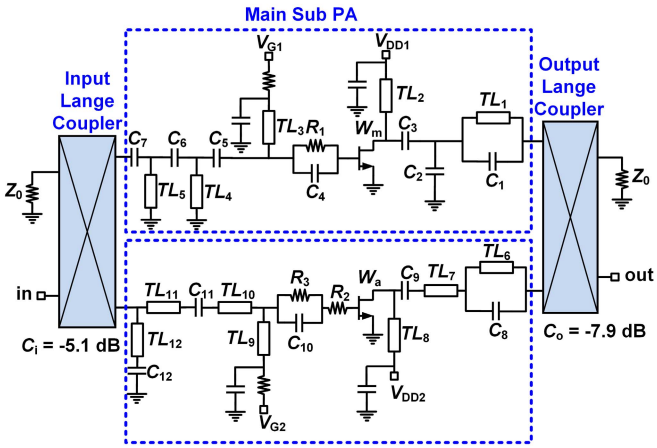
Fig. 11. Comparison of broadband performance of the Doherty and unbalanced PAs. (a) Doherty PA architecture. (b) Unbalanced PA architecture. (c) Impedance transformation ratio of transmission lines in the two architectures at back-off (BO) and peak-power (PP). In this comparison, it is assumed that the output matching networks of the unbalanced PA are realized using $\lambda/4$ transmission lines.

can be further extended by using higher order matching networks, while this is not possible for the impedance inverter in the Doherty PA. Nevertheless, there is a tradeoff between bandwidth and insertion loss of the output matching networks, dependent on their circuit structure and quality factor of passive components, which translates to an efficiency-bandwidth tradeoff for the unbalanced PA.

Furthermore, in the unbalanced PA, the impedance presented to the main sub-PA is independent of the output impedance of the auxiliary sub-PA. This is a fundamental feature of quadrature couplers that can be explained as follows. Using (1), for an incident voltage wave of V_1^+, when ports 2 and 3 are matched, i.e., $V_2^+ = V_3^+ = 0$, $V_1^- = 0$; thus, $\Gamma_{in} = V_1^-/V_1^+ = 0$. Therefore, port 1 is also matched independent of the port 4 termination impedance. However, in the Doherty PA, this impedance is affected by the output impedance of the auxiliary PA, which changes from peak-power to back-off and also with frequency. This leads to the additional improvement of the unbalanced PA's bandwidth over the Doherty PA.

III. PA Circuit Design

We now present the design of a broadband fully integrated unbalanced PA prototype with peak efficiency at 6 dB back-off for 4.5–6.5-GHz bandwidth. The PA is implemented using a 250-nm GaN-on-SiC process. Power GaN transistors feature



C_1: 0.3 pF	C_7: 2.9 pF	TL_1: 30/1940 µm	TL_7: 25/500 µm	R_1: 18 Ω
C_2: 0.1 pF	C_8: 0.4 pF	TL_2: 20/2770 µm	TL_8: 25/1830 µm	R_2: 1 Ω
C_3: 0.3 pF	C_9: 0.8 pF	TL_3: 25/990 µm	TL_9: 20/800 µm	R_3: 8 Ω
C_4: 0.5 pF	C_{10}: 3.0 pF	TL_4: 55/950 µm	TL_{10}: 20/1810 µm	W_m: 4x125 µm
C_5: 0.6 pF	C_{11}: 0.7 pF	TL_5: 10/1020 µm	TL_{11}: 15/1100 µm	W_a: 8x125 µm
C_6: 0.7 pF	C_{12}: 0.5 pF	TL_6: 25/1050 µm	TL_{12}: 25/400 µm	

Fig. 12. Schematic of the implemented unbalanced PA.

a large optimum load resistance and relatively small parasitic capacitances compared with other processes and, as a result, are widely used in the implementation of various broadband amplifier architectures [22]–[30]. The circuit schematic is shown in Fig. 12. The applications of the developed theory and practical considerations in the circuit design are presented in the following.

A. Output and Input Lange Couplers

The output and input couplers are realized using meandered Lange couplers to achieve broadband performance and save chip area [see Fig. 13(a)]. The coupling coefficient of the output coupler is determined based on the 6-dB OPBO requirement (see Fig. 4) and the efficiency versus output power profile (see Fig. 6). A coupling coefficient of ≈ -8 dB is chosen in this design to maximize back-off efficiency. A stronger coupling coefficient, e.g., -6 dB, could provide a more linear gain, as shown in Fig. 7(a), but at a lower back-off efficiency [$\eta_{bo} = (1 - C_o^2)\eta_m$]. In this design, however, a lower coupling coefficient is preferred to demonstrate the back-off efficiency enhancement feature of the unbalanced PA architecture. Furthermore, as indicated in Fig. 8(b), the coupling coefficient of the input coupler can be chosen such that the compressive gain of the main sub-PA can be compensated with the expansive gain of the auxiliary sub-PA in order to achieve a linear gain.

The Lange coupler layout structure, i.e., the width, spacing, and length of the transmission lines, is optimized using extensive EM simulations. The resulting performance of the output coupler is shown in Fig. 13(b). The transmission coefficients of two output ports are -7.9 dB ($=C_o$) and -1.2 dB at 5.5 GHz. The amplitude imbalance, ΔA, and the deviation of the phase difference from $-90°$, $\Delta\phi$, respectively, read as 0.6–1.3 dB and 3.2°–6.3°, across 4.0–7.0 GHz. The average insertion loss, defined as $\text{IL} = -10\log_{10}(|S_{21}|^2 + |S_{31}|^2)$, is 0.3–0.5 dB, and the reflection coefficients of three ports are $|S_{ii}| < -27$ dB.

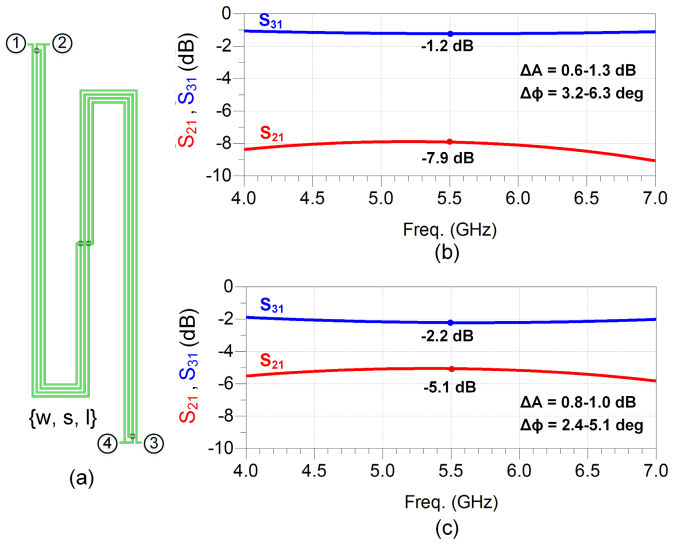


Fig. 13. Physical structure and simulated performance of the meandered Lange couplers. (a) Physical structure. (b) Output coupler. (c) Input coupler. Physical dimensions including metal width, spacing, and total length, $\{w, s, l\}$, are $\{10, 40, 5400\}$ μm for the output coupler and $\{10, 20, 5500\}$ μm for the input coupler. The average insertion loss of both couplers is 0.3–0.5 dB, and the reflection coefficients of their three ports are $|S_{ii}| < -27$ dB, across 4.0–7.0 GHz.

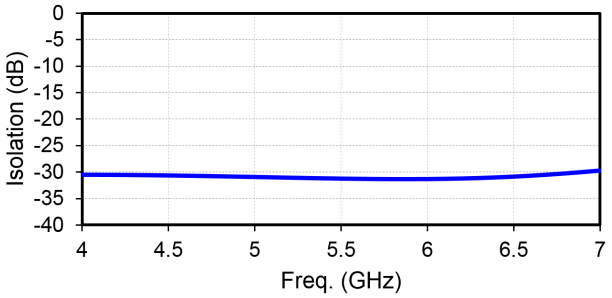


Fig. 14. Simulated isolation between the main and auxiliary sub-PAs.

The coupling coefficient of the input coupler is targeted as ≈ -5 dB based on the gain and input power drive considerations. The coupler performance shown in Fig. 13(c) indicates transmission coefficients of -5.1 dB ($=C_i$) and -2.2 dB at 5.5 GHz. Furthermore, ΔA of 0.8–1.0 dB, $\Delta\phi$ of 2.4°–5.1°, the insertion loss of 0.3–0.5 dB, and $|S_{ii}| < -27$ dB are achieved across 4.0–7.0 GHz.

Isolation between the main and auxiliary sub-PAs is an important parameter in the unbalanced PA. In Fig. 14, the simulated isolation, i.e., $|S_{14}|$ of the output Lange coupler, is shown versus the frequency. The isolation reads <-29.7 dB across 4.0–7.0 GHz, which confirms that the impedance presented to the main transistor is independent of the auxiliary sub-PA's output impedance.

B. Main and Auxiliary Sub-PAs

The width of transistors in the main and auxiliary sub-PAs can be determined based on the output power target for the unbalanced PA and the coupling coefficients of the couplers derived in Section III-A. From the required peak output power $P_{\text{out,pp}}$ and OPBO level, the back-off output power is given by $P_{\text{out,bo}} = P_{\text{out,pp}} - \text{OPBO}$. Using (14) and the estimated loss of the output matching network of the main sub-PA $L_{omn,m}$, the required output power of the main transistor can be derived as $P_{\text{tr},m} = P_{\text{out,bo}} - 10\log_{10}(1 - C_o^2) + L_{omn,m}$. This can be used in load–pull simulations to derive the width of the main transistor W_m. In this design, to achieve 36-dBm peak output power and 6-dB OPBO, with $C_o = -8$ dB and assuming $L_{omn,m} \approx 1$ dB, the required power of the main transistor is 31.8 dBm. This is satisfied using a transistor width of 4×125 μm.

Furthermore, with help of Fig. 4, with C_o chosen in Section III-A, parameter K_p is obtained, leading to the width of the auxiliary transistor as $W_a \approx K_p W_m$. In practice, larger transistors have higher losses, e.g., due to larger parasitic resistances, and, thus, lower efficiency that can degrade the efficiency of the unbalanced PA. Moreover, the larger parasitic capacitance of this transistor limits the PA bandwidth. The optimum width of the auxiliary transistor should, therefore, be smaller than the theoretical value. In this design, a transistor width of 8×125 μm results in the best-achieved efficiency and bandwidth performance. This choice shifts the OPBO level to roughly 5 dB.

The output matching networks of the main and auxiliary sub-PAs should provide the optimum load resistances $R_{\text{opt},m} \approx 150\ \Omega$ and $R_{\text{opt},a} \approx 70\ \Omega$ in the fundamental frequency band. In this design, we realize the output matching networks such that they enable the operation of the sub-PAs in the continuous mode. This improves the PA efficiency over a broad bandwidth by means of providing optimum load impedances in the fundamental and second harmonic bands [24]. The networks are implemented using stacked-metal microstrip transmission lines and metal–insulator–metal (MIM) capacitors.

The stability of the transistors is ensured using resistive–capacitive networks in series with their gate, i.e., R_1 and C_4 for the main transistor and $R_{2,3}$ and C_{10} for the auxiliary transistor. The resistors reduce the low-frequency gain of the transistors, which can be very high and lead to instability, while the capacitors bypass the resistors in the operational band to avoid unnecessary gain losses. The stability factor μ is used to evaluate the stability of the transistors [19]. Furthermore, the gate and drain bias pads are bypassed both internally using large on-chip capacitors and externally through multiple paralleled onboard capacitors.

Simulation results indicate that the main sub-PA provides 32-dBm output power, 56% efficiency, and 10-dB power gain, at 22-dBm input power and 5.5 GHz. For the auxiliary sub-PA, these are, respectively, 36 dBm, 49%, and 10 dB, at 26-dBm input power. The unbalanced PA achieves the peak output power of 34 dBm and the efficiency of 35% at peak power and 41% at ≈5-dB back-off. The efficiency reads 27%–38% at peak power and 28%–42% at back-off, across 4.5–6.5 GHz. In Fig. 15, simulated S_{11} and S_{22} of the main sub-PA, auxiliary sub-PA, and unbalanced PA are shown. It is noted that the unbalanced PA structure improves input and output return losses compared with the sub-PAs. In Fig. 16, the simulated AM–PM distortion is shown across

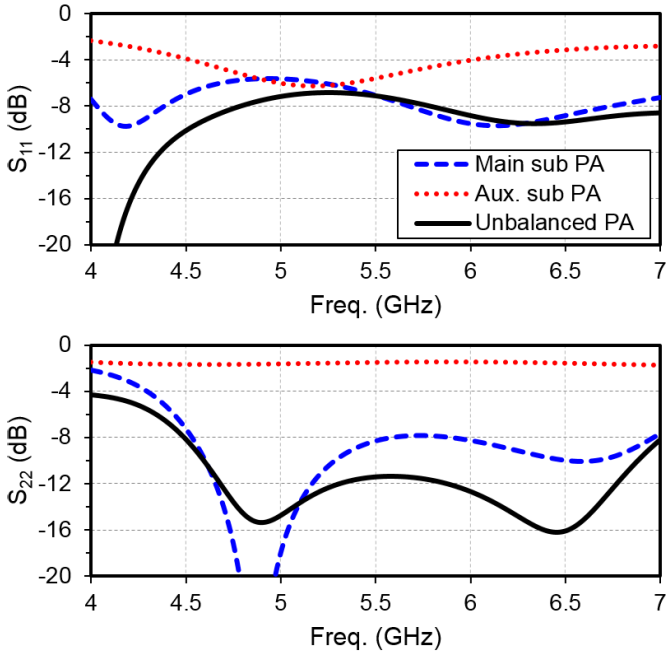


Fig. 15. Simulated S_{11} and S_{22} of the main sub-PA, auxiliary sub-PA, and unbalanced PA.

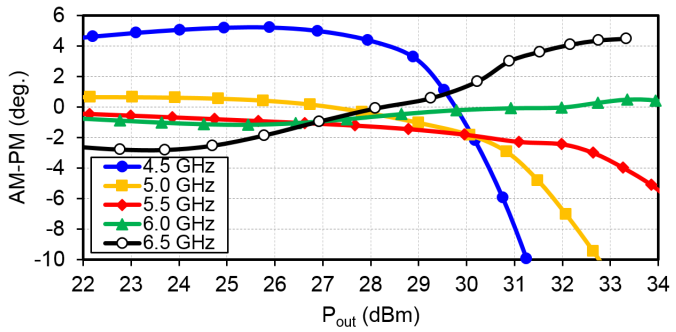


Fig. 16. Simulated AM–PM distortion across 4.5–6.5 GHz.

4.5–6.5 GHz. A lower AM–PM is achieved close to the center of the band, e.g., 5.5–6.0 GHz, as a result of proper compensation of the compressive nonlinearity of the main transistor with the expansive nonlinearity of the auxiliary transistor.

IV. Measurement Results

The PA chip is fabricated using a 250-nm GaN-on-SiC process from WIN Semiconductors. The chip is shown in Fig. 17, where the meandered Lange couplers are used to save the die area. The drains of transistors are biased at 28 V, while their gate biases are chosen as −2.3 and −4.0 V to achieve high back-off efficiency. The chip die is wire-bonded to the test PCB, and a heat-sink is used to improve the thermal stability in the measurements.

A. Continuous-Wave Measurements

The output power, efficiency, and gain of the PA versus frequency are shown in Fig. 18. The results are achieved at 24-dBm input power. This corresponds to about 1–3-dB

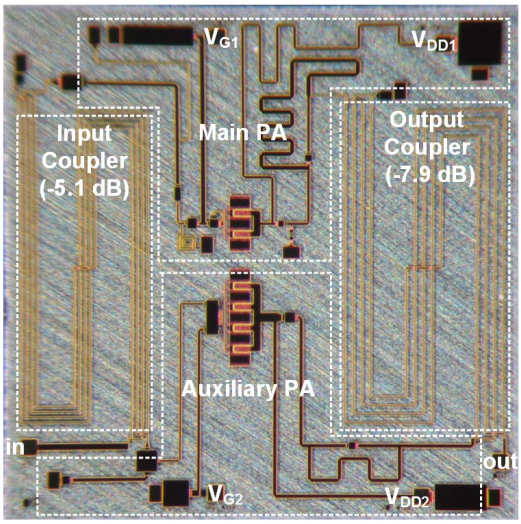


Fig. 17. Chip micrograph (2.8 × 2.8 mm^2).

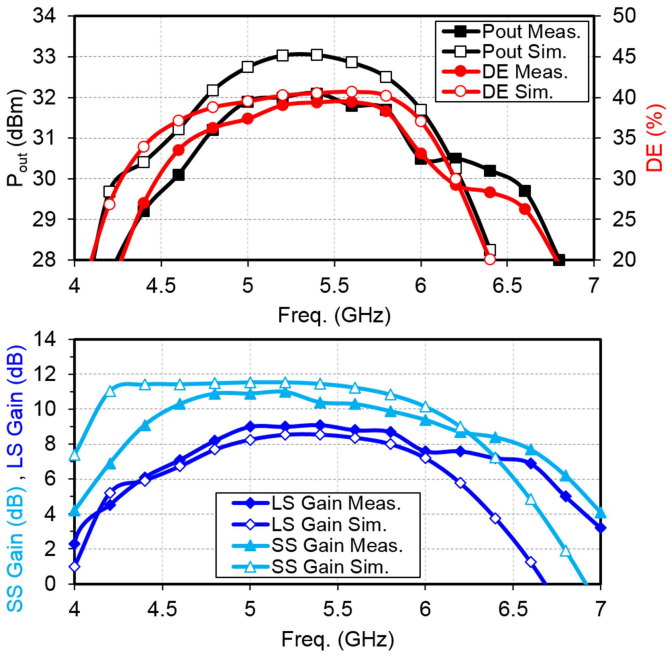


Fig. 18. Measured and simulated output power, DE, and gain (large-signal and small-signal, LS/SS) versus frequency at 24-dBm input power.

gain compression. It is noticed that there is an upward shift in the measured frequency response compared with simulation results. The 3-dB bandwidth of small-signal gain is 4.3–6.5 GHz (41.6%). The efficiency reads 28%–39% across 4.5–6.5 GHz.

The measured and simulated gain, DE, and PAE versus output power at 5.0 GHz are shown in Fig. 19. It is noted that the shape of the efficiency versus output power follows the theoretical characteristics of the unbalanced PA, i.e., the maximum efficiency is achieved at back-off. The DE of 34%/40% is obtained at peak-power/back-off, while PAE is 25%/35%.

The measured DE, PAE, and gain versus output power across 4.5–6.5 GHz are shown in Fig. 20. The PA provides 32.2–34.3-dBm output power, 27%–37% DE at peak power,

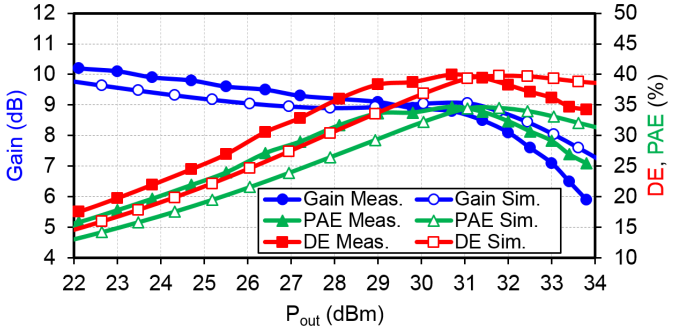


Fig. 19. Measured and simulated gain, DE, and PAE versus output power at 5.0 GHz.

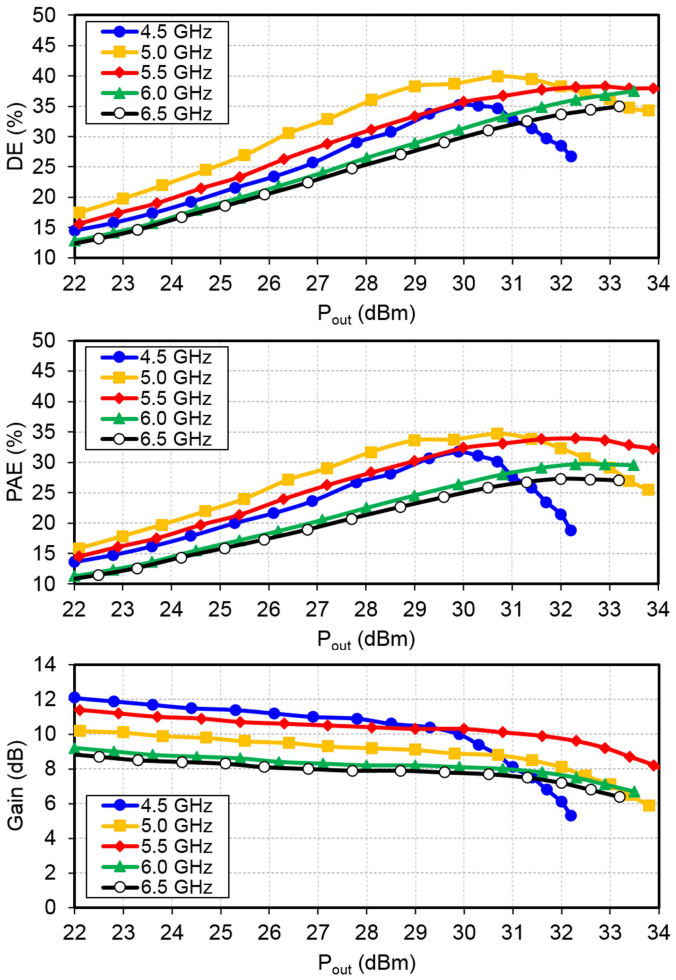


Fig. 20. Measured DE, PAE, and gain versus output power across 4.5–6.5 GHz.

and 27%–40% at 5–6-dB back-off. This PA prototype is presented as proof of the developed unbalanced PA architecture. The performance can be further improved by optimizing the PA circuitry.

B. Modulated-Signal Measurements

The PA operation is evaluated using a 256-QAM signal with up to 200-MHz modulation bandwidth (BW_m) and 7.2-dB PAPR. The modulated signal is generated using a MATLAB code, loaded into an R&S SMW200A vector signal generator,

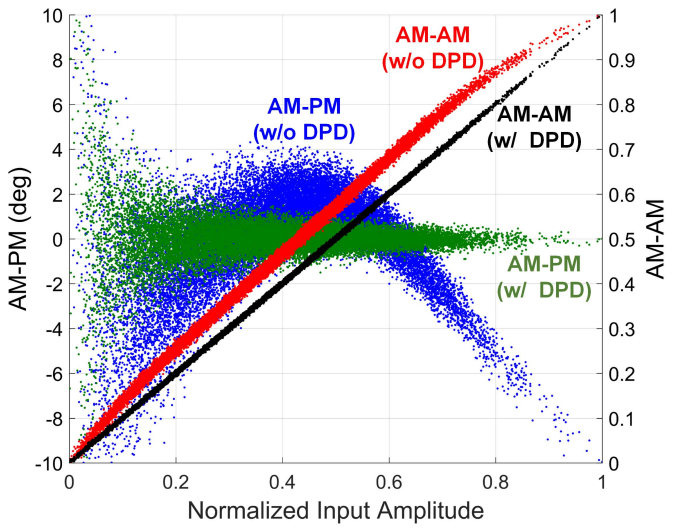


Fig. 21. Measured AM–AM and AM–PM distortion characteristics at 25.5-dBm average output power, with and without using DPD. The results are achieved using a 5.0-GHz, 256-QAM signal with 100-MHz bandwidth and 7.2-dB PAPR.

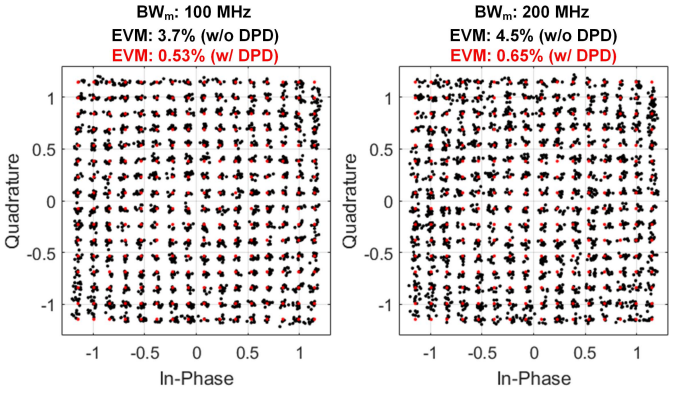


Fig. 22. Measured output constellation at 25.5-dBm average output power. The results are achieved using a 5.0-GHz, 256-QAM signal with 100-/200-MHz bandwidth and 7.2-dB PAPR.

and is applied to the PA. The output signal is captured using an R&S FSW45 vector signal analyzer and is processed in MATLAB to extract the output signal features.

The measured AM–AM and AM–PM distortion characteristics are shown in Fig. 21. Both distortions can be substantially alleviated using a digital predistortion (DPD). The output signal constellation is shown in Fig. 22, where an rms error vector magnitude (EVM_{rms}) of 3.7% (−28.6 dB) is achieved at 25.5-dBm average output power for $BW_m = 100$ MHz. EVM_{rms} increases to 4.5% (−26.9 dB) for $BW_m = 200$ MHz. Using the DPD, EVM_{rms} can be improved to, respectively, 0.53% (−45.5 dB) and 0.65% (−43.7 dB) in the two cases. The measured signal spectrum is shown in Fig. 23, where the adjacent channel leakage ratio (ACLR), for $BW_m = 100$ MHz, is −34.1/−34.1 dBc at lower/upper channels without DPD and improved to −45.7/−46.4 dBc after DPD is applied. For $BW_m = 200$ MHz, the ACLR is −32.5/−33.0 dBc without DPD and −42.1/−44.1 dBc with DPD.

In Fig. 24, the measured EVM and ACLR (average of lower and upper channels) are shown. The EVM and ACLR can be

TABLE I
COMPARISON OF BROADBAND FULLY INTEGRATED GaN PAs WITH BACK-OFF EFFICIENCY ENHANCEMENT

	This Work	[25]	[26]	[27]	[28]	[29]	[30]
Bandwidth (GHz)	4.5–6.5	4.5–6.0	2.1–2.7	6.8–8.5	5.8–8.8	5.1–5.9	4.5–5.2
Fractional BW (%)	37.0	28.9	25.2	22.4	42.0	14.6	14.5
$P_{out,pp}$ (dBm)	32.2–34.3	35–36	40–41	34.5–35.5	35–36	36.0–38.7	40.4–41.2
η_{pp} (%)	27–37	43–49	—	34–57	34–51	44–48	55–63
η_{bo} (%)	27–40	24–32	48–62	26–40	35–45	32–51	47–50
OPBO (dB)	5–6	6	7.6	9	9	6	6
Gain (dB)	6.7–9.1	7.6–11.6	12–14	5–9	8.5–9	14.4–17.3	7–9
Modulation	256-QAM	64-QAM	LTE	256-QAM	256-QAM	64/256-QAM	LTE
BW_m (MHz)	100/200	100	10	10	20	80	40
PAPR (dB)	7.2	8	7.2	7.8	8.5	—	7.7
Carrier Freq. (GHz)	5.0	5.0	2.14–2.65	7.4	7.0	5.8	4.9
EVM_{rms} (dB)	−28.6/−26.9	−30.5	—	—	—	−28/−32	—
$P_{out,avg}$ (dBm)	25.5	29.3	—	27.5	27.6	23.5/21.5	33.0
η_{avg} (%)	30	29	45–53	48	40	—	51
Chip Area (mm×mm)	2.8×2.8	3.0×2.8	2.65×1.9*	2.1×1.5	2.9×2.9	2.5×1.6	2.2×2.1
GaN Process (nm)	250	250	250	250	250	250	250

*Partially off-chip output matching network realized using bond wires.

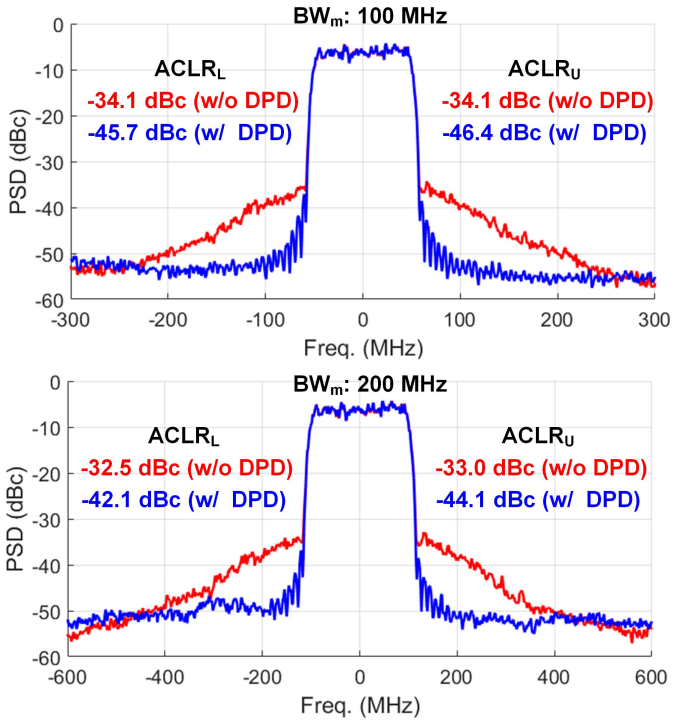


Fig. 23. Measured output spectrum for a 256-QAM signal with 100-/200-MHz bandwidth and 7.2-dB PAPR.

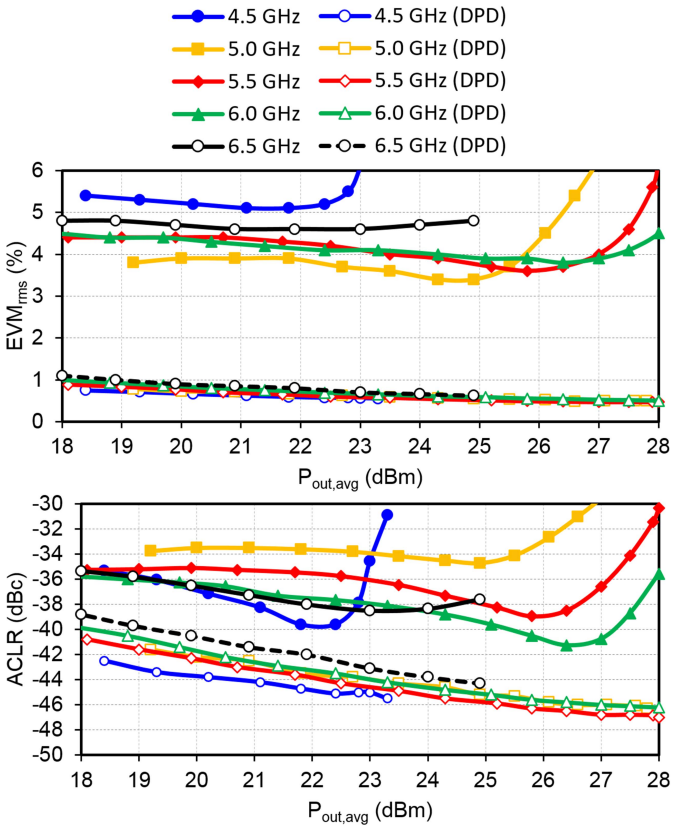


Fig. 24. Measured EVM and ACLR (average of lower and upper channels) versus the average output power for a 256-QAM signal with 100-MHz bandwidth and 7.2-dB PAPR. Swept across carrier frequencies and with DPD ON/OFF.

improved with the help of DPD to <1% and <−39 dBc, respectively, across the 18–28-dBm average output power range and the entire 4.5–6.5-GHz frequency band.

The effect of modulation bandwidth on the linearity performance is demonstrated in Fig. 25. Measured EVM and ACLR are shown versus average output power for BW_m = 100/200 MHz. The linearity degrades with the modulation bandwidth, but good performance can still be achieved.

In Fig. 26, the average drain efficiency versus average output power is shown. The efficiency reaches 30% at 25.5-dBm average output power and is almost independent of the modulation bandwidth. Higher efficiency can be achieved by operating the PA at higher output power and using the DPD to compensate for the increased nonlinearity.

In Table I, the performance of the implemented unbalanced PA is compared with prior fully integrated GaN PAs with

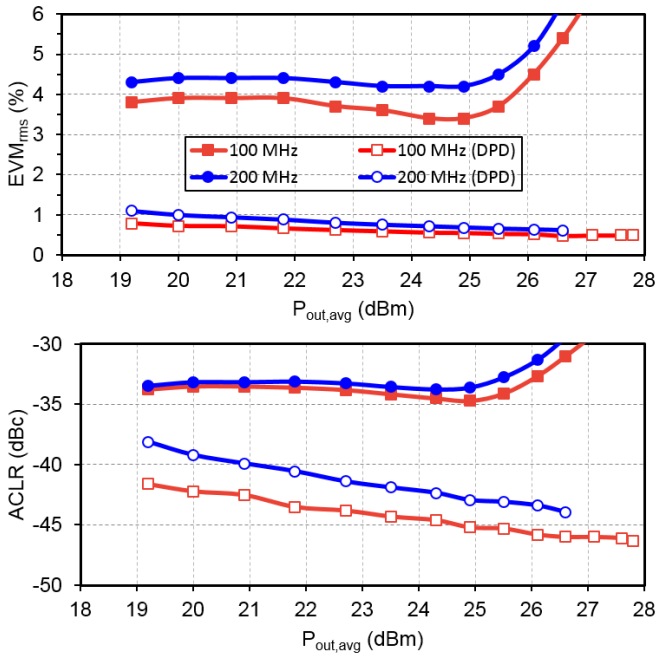


Fig. 25. Measured EVM and ACLR (average of lower and upper channels) versus the average output power for a 256-QAM signal with 100-/200-MHz bandwidth and 7.2-dB PAPR. Swept across the modulation bandwidth and with DPD ON/OFF.

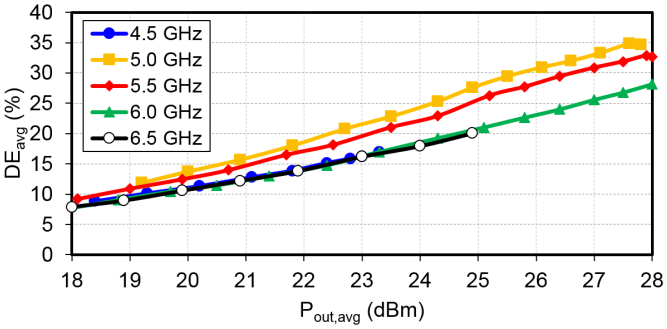


Fig. 26. Measured average drain efficiency versus the average output power for a 256-QAM signal with 7.2-dB PAPR.

back-off efficiency enhancement (all of those are Doherty PAs). A wide operation bandwidth (37%) is achieved. This is the main feature of the proposed PA architecture and is a result of using broadband Lange couplers and impedance matching networks, rather than impedance inverters. The linearity evaluated using a wideband 100-/200-MHz 256-QAM signal results in $\text{EVM}_{\text{rms}} \approx -28.6/-26.9$ dB without any predistortion. A record-high modulation bandwidth of 200 MHz (with 8 S $\times$ 200 MHz $=$ 1.6 GS/s data rate) is achieved while maintaining state-of-the-art performance. This is due to the aforementioned nonlinearity cancellation through compressive and expansive nonlinearity behaviors of the main and auxiliary sub-PAs, operating in the class-B and class-C modes.

V. Conclusion

In this article, we presented an unbalanced PA architecture for broadband back-off efficiency enhancement. The PA adopts two sub-PAs and Lange couplers as input power splitter and output power divider. It is shown that the OPBO level of this PA is controlled by the transistors' width ratio and coupling coefficient of the output Lange coupler. This PA architecture can achieve broadband operation, resulting from using the wideband output and input impedance matching networks for the sub-PAs, as well as the Lange couplers with an inherently broadband response. These two features are essential in improving the unbalanced PA bandwidth compared with conventional Doherty PA using band-limiting impedance inverters. A proof-of-concept fully integrated PA is implemented in a 250-nm GaN-on-SiC process and demonstrates the record modulation bandwidth of 200 MHz (1.6-GS/s data rate) in the sub-6-GHz band.

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References

[1] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*, 2nd ed. Boston, MA, USA: Artech, 2006.
[2] A. Grebennikov and S. Bulja, "High-efficiency Doherty power amplifiers: Historical aspect and modern trends," *Proc. IEEE*, vol. 100, no. 12, pp. 3190–3219, Dec. 2012.
[3] G. Nikandish, R. B. Staszewski, and A. Zhu, "Breaking the bandwidth limit: A review of broadband Doherty power amplifier design for 5G," *IEEE Microw. Mag.*, vol. 21, no. 4, pp. 57–75, Apr. 2020.
[4] V. Vorapipat, C. S. Levy, and P. M. Asbeck, "Voltage mode Doherty power amplifier," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1295–1304, May 2017.
[5] V. Vorapipat, C. S. Levy, and P. M. Asbeck, "A class-G voltage-mode Doherty power amplifier," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3348–3360, Dec. 2017.
[6] S. Moloudi and A. A. Abidi, "The outphasing RF power amplifier: A comprehensive analysis and a class-B CMOS realization," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1357–1369, Jun. 2013.
[7] P. Asbeck and Z. Popovic, "ET comes of age: Envelope tracking for higher-efficiency power amplifiers," *IEEE Microw. Mag.*, vol. 17, no. 3, pp. 16–25, Mar. 2016.
[8] X. A. Nghiem, J. Guan, and R. Negra, "Broadband sequential power amplifier with Doherty-type active load modulation," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 9, pp. 2821–2832, Sep. 2015.
[9] B. Merrick, J. King, and T. Brazil, "A wideband sequential power amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2014, pp. 1–3.
[10] D. J. Shepphard, J. Powell, and S. C. Cripps, "An efficient broadband reconfigurable power amplifier using active load modulation," *IEEE Microw. Wireless Compon. Lett.*, vol. 26, no. 6, pp. 443–445, Jun. 2016.
[11] P. H. Pednekar, E. Berry, and T. W. Barton, "RF-input load modulated balanced amplifier with octave bandwidth," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 12, pp. 5181–5191, Dec. 2017.
[12] R. Quaglia and S. Cripps, "A load modulated balanced amplifier for telecom applications," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 3, pp. 1328–1338, Mar. 2018.
[13] J. R. Powell, D. J. Shepphard, R. Quaglia, and S. C. Cripps, "A power reconfigurable high-efficiency *X* -Band power amplifier MMIC using the load modulated balanced amplifier technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 6, pp. 527–529, Jun. 2018.
[14] C. R. Chappidi, X. Wu, and K. Sengupta, "Simultaneously broadband and back-off efficient mm-wave PAs: A multi-port network synthesis approach," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2543–2559, Sep. 2018.
[15] G. Liu, P. Haldi, T.-J.-K. Liu, and A. M. Niknejad, "Fully integrated CMOS power amplifier with efficiency enhancement at power back-off," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 600–609, Mar. 2008.
[16] C. R. Chappidi, T. Sharma, and K. Sengupta, "Multi-port active load pulling for mm-wave 5G power amplifiers: Bandwidth, back-off efficiency, and VSWR tolerance," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 2998–3016, Jul. 2020, doi: 10.1109/TMTT.2020.2977342.

[17] S. Hu, F. Wang, and H. Wang, "A 28-/37-/39-GHz linear Doherty power amplifier in silicon for 5G applications," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1586–1599, Jun. 2019.
[18] G. Nikandish, R. B. Staszewski, and A. Zhu, "Broadband fully integrated GaN power amplifier with embedded minimum inductor bandpass filter and AM–PM compensation," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 9, pp. 159–162, Sep. 2019.
[19] D. M. Pozar, *Microwave Engineering*. Hoboken, NJ, USA: Wiley, 2012.
[20] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed. Boston, MA, USA: McGraw-Hill, 2017.
[21] H. Wang, C. Sideris, and A. Hajimiri, "A CMOS broadband power amplifier with a transformer-based high-order output matching network," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2709–2722, Dec. 2010.
[22] M. R. Duffy, G. Lasser, G. Nevett, M. Roberg, and Z. Popovic, "A three-stage 18.5–24-GHz GaN-on-SiC 4 W 40% efficient MMIC PA," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2402–2410, Sep. 2019.
[23] K. W. Kobayashi, D. Denninghoff, and D. Miller, "A novel 100 MHz–45 GHz Input-Termination-Less distributed amplifier design with low-frequency low-noise and high linearity implemented with a 6 inch 0.15 μm GaN-SiC wafer process technology," *IEEE J. Solid-State Circuits*, vol. 51, no. 9, pp. 2017–2026, Sep. 2016.
[24] G. Nikandish, R. B. Staszewski, and A. Zhu, "Design of highly linear broadband continuous mode GaN MMIC power amplifiers for 5G," *IEEE Access*, vol. 7, pp. 57138–57150, 2019.
[25] G. Nikandish, R. B. Staszewski, and A. Zhu, "Bandwidth enhancement of GaN MMIC Doherty power amplifiers using broadband transformer-based load modulation network," *IEEE Access*, vol. 7, pp. 119844–119855, 2019.
[26] S. Jee *et al.*, "Asymmetric broadband Doherty power amplifier using GaN MMIC for femto-cell base-station," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 9, pp. 2802–2810, Sep. 2015.
[27] D. Gustafsson, J. C. Cahuana, D. Kuylenstierna, I. Angelov, N. Rorsman, and C. Fager, "A wideband and compact GaN MMIC Doherty amplifier for microwave link applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 2, pp. 922–930, Feb. 2013.
[28] D. Gustafsson, J. C. Cahuana, D. Kuylenstierna, I. Angelov, and C. Fager, "A GaN MMIC modified Doherty PA with large bandwidth and reconfigurable efficiency," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 12, pp. 3006–3016, Dec. 2014.
[29] S.-H. Li, S. S. H. Hsu, J. Zhang, and K.-C. Huang, "Design of a compact GaN MMIC Doherty power amplifier and system level analysis with X-parameters for 5G communications," *IEEE Trans. Microw. Theory Techn.*, vol. 66, no. 12, pp. 5676–5684, Dec. 2018.
[30] G. Lv, W. Chen, X. Liu, F. M. Ghannouchi, and Z. Feng, "A fully integrated C-band GaN MMIC Doherty power amplifier with high efficiency and compact size for 5G application," *IEEE Access*, vol. 7, pp. 71665–71674, 2019.

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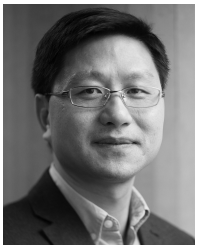

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