Hi3520D/Hi3515A/Hi3515C Hardware Design

Checklist

Issue 02

Date 2013-06-21

HiSilicon Technologies Co., Ltd.

Address: Huawei Industrial Base
Bantian, Longgang
Shenzhen 518129
People's Republic of China

Website: http://www.hisilicon.com

Email: support@hisilicon.com

About This Document

Purpose

This document describes the check items for Hi3520D/Hi3515A/Hi3515C solutions.

Related Version

The following table lists the product version related to this document.

Product Name	Version
Hi3520D	V100
Hi3515A	V100
Hi3515C	V100

Intended Audience

This document is intended for:

- Technical support personnel
- Board hardware development engineers

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 02 (2013-06-21)

This issue is the second official release, which incorporates the following changes:

The descriptions related to the Hi3515C are added.

Issue 01 (2013-05-21)

This issue is the first official release, which incorporates the following changes:

Chapter 1 Checklist

Section 1.7 "Design Requirements on the Embedded RTC" is added.

In section 1.9, a note is added.

Issue 00B02 (2013-04-03)

This issue is the second draft release, which incorporates the following changes:

The descriptions related to the Hi3515A are added.

Issue 00B01 (2013-02-28)

This issue is the first draft release.

Contents

1 Checklist

NOTE

Unless otherwise specified, this document applies to the Hi3520D, Hi3515A, and Hi3515C and uses the Hi3520D as an example.

1.1 Design Requirements on 2-Layer PCBs

√	Items
	You must design 2-layer PCBs by following section 2.1 in the *Hi3520D/Hi3515A/Hi3515C Hardware Design User Guide*.

1.2 Design Requirements on Power Supplies and GND

√	Items
	The core power pins (DVDD12) connect to the 1.25 V digital power. A DC-DC power chip that provides 2 A or larger current is required for the Hi3520D DVDD12.
	Power supplies are powered on in the sequence of high voltage to low voltage. That is, the 3.3 V, 1.5 V (or 1.8 V), and 1.25 V power supplies are powered on in sequence.
	PLL power pins must be isolated by using electromagnetic interference (EMI) beads, and filtering capacitors are connected close to these pins. Each EMI bead is 1000 R@100 MHz. For details about the circuit, see the schematic diagram and PCB design of the Hi3520D demo board.
	Ensure that the output voltage of power supplies meets the requirements of the Hi3520D when ripples and noises occur. For details about the requirements on the power supply of each module, see section 2.6 "Electrical Specifications" in the *Hi3520D/Hi3515A/Hi3515C CODEC Processor Data Sheet*.

1.3 Design Requirements on the Clock Circuit of the Master Chip

√	Items
	The Hi3520D requires a 24 MHz external clock, and the maximum deviation is ±30 ppm.

1.4 Design Requirements on the Reset Circuit

√	Items
	The level of the input power-on reset signal is low. Typically, the reset pulse width is 100 ms to 300 ms.
	The Hi3520D watchdog is open drain (OD) output. When the watchdog is used, pull-up resistors are required. The 4.7 kΩ pull-up resistors are recommended.

1.5 Design Requirements on the Small System

√	Items
	The power supplies of the DDR and master chip must be the same as those on the Hi3520D demo board. For details, see the schematic diagram and PCB design of the Hi3520D demo board.

1.6 Design Requirements on the SPI Flash

√	Items
	The serial peripheral interface (SPI) flash can boot only from CS1. If the single I/O mode is used, you are advised to connect 4.7 kΩ pull-up resistors to the CS1 and HOLD signals of the SPI flash, and connect a 4.7 kΩ pull-down resistor to the WP signal.

1.7 Design Requirements on the Embedded RTC

√	Items
	In fixed frequency-division mode, the timing accuracy of the embedded RTC depends on the external crystal oscillator. Select an appropriate crystal oscillator based on its frequency deviation and temperature offset. If high timing accuracy is required, the external integrated RTC is recommended.

1.8 Design Requirements on the I²C Circuit

√	Items
	The I^2C signals SCL and SDA are OD outputs, which need to connect to 1 kΩ pull-up resistors.
	I^2C addresses must be distinguished to avoid address conflict.

1.9 Design Requirements on VI Interfaces

√	Items
	The Hi3520D has two physical BT.656 input interfaces (Hi3515A/Hi3515C has one physical BT.656 input interface). The two BT.656 inputs can be combined into a BT.1120 input.
	The VI line sequence can be adjusted based on the actual AD line sequence. The CLK line sequence can be adjusted by configuring the multiplexing relationship. The DATA line sequence can be used to switch big and little endian modes. For details, see the *Hi3520D/Hi3515A/Hi3515C CODEC Processor Data Sheet*.
	When the BT.656 signal line connects to the Hi3520D, Hi3515A or Hi3515C VI interface, appropriate serial resistors must be selected based on the drive capability of the ADC and trace length.

1.10 Design Requirements on Video Interfaces

√	Items
	As the Hi3520D has an embedded HDMI PHY, the Hi3520D can directly output HDMI signals. The HDMI module has a dedicated I^2C interface. The HDMI_REXT pin connects to 1% 51 kΩ and 6.8 kΩ resistors in parallel, and then to GND.

√	Items
	The impedance of the external resistor connected to the VDAC_REXT and VDAC_REXTS pins must be the same as that specified on the schematic diagram of the Hi3520D demo board.
	Note that the HD picture-in-picture (PIP) function is multiplexed with the CVBS0 output function. If the HD PIP function is used, the CVBS0 output is unavailable. That is, if the HD PIP and SD CVBS output functions are required at the same time, the SD CVBS signals must be output from the CVBS1 interface.

1.11 Design Requirements on the Audio Circuit

√	Items
	The Hi3520D provides one I^2S audio signal input interface, one I^2S audio signal output interface, and one MCLK signal.
	The connection modes in master and slave modes are different when the two I^2S audio signal interfaces are combined into an audio input and output interface for intercom applications. Note that the BCLK and WCLK signals must connect to the two I^2S signals simultaneously in slave mode. For details, see section 1.2.8 in the *Hi3520D/Hi3515A/Hi3515C Hardware Design User Guide*.

1.12 Design Requirements on the SPI Control Interface Circuit

√	Items
	The Hi3520D SPI control interface provides the SPI CLK, SDO, and SDI signals and two CSs (active low).
	If the SPI connects to multiple devices such as GV7601s that are connected in daisy chain mode, the delay for each device caused by data transfer is taken into account when the working frequency of the SPI clock signal SCLK is configured.

1.13 Design Requirements on the USB Circuit

√	Items
	The Hi3520D provides two USB ports USB0 and USB1.

√	Items
	You are advised to connect USB_REXT to a 43.2 Ω±1% resistor, and then to GND. Note that the resistor needs to be placed close to the USB_REXT pin.
	When a 2-layer PCB is designed, each USB trace must be shorter than 5 inches.

1.14 Design Requirements on SATA Interface Circuit

√	Items
	The Hi3520D/Hi3515A provides two SATA 2.6 interfaces SATA 0 and SATA 1, whereas the Hi3515C provides only one SATA interface.
	The 10 nF surface mounting technology (SMT) capacitors are connected in series close to the SATA connector on the four SATA differential traces (including the TX and RX traces), and the impedance of each differential trace is less than or equal to 100 Ω.
	When a 2-layer PCB is designed, each SATA trace must be shorter than 3 inches.

1.15 Design Requirements on the ETH Circuit

√	Items
	When the embedded Ethernet PHY is used, measures must be taken to protect the chip against ESD and surge.
	The Hi3520D supports only one ETH port. To be specific, when the embedded PHY is used, the external PHY connected on the RMII cannot be used, and vice versa.

1.16 Design Requirements on JTAG and System Control Circuits

√	Items
	4.7 kΩ pull-up resistors connect to the TDI, TDO, and TMS pins; a 1 kΩ pull-down resistor connects to the TCK pin; a 10 kΩ pull-down resistor connects to the TRST pin. Note that the TRST pin can connect to a pull-up resistor for connecting to other emulators.
	The TESTMODE pin connects to a 10 kΩ pull-down resistor, and then to GND.
	The JTAG pin on the Hi3520D can be multiplexed as the GPIO pin by configuring JATG_EN.

1.17 Design Requirements on the UART Circuit

√	Items
	The debugging serial port must be connected. UART 0 is used for debugging by default.

1.18 Design Requirements on the eFUSE Module

√	Items
	The VDD25_EFUSE pin must connect to a 4.7 kΩ pull-down resistor, and then to GND.

1.19 Design Requirements on the HDMI

√	Items
	The 1.25 V analog power pins K21 and L21 of the HDMI (AVDD10_HDMI) must be isolated from the 1.25 V power by using 1000 Ω@100 MHz EMI beads, and 100 µF and 0.1 µF filtering capacitors are connected after the beads. For details, see the schematic diagram of the Hi3520D demo board.
	The length deviation of the internal differential signal traces must fall within 5 mils, and the spacing between each pair of differential signal traces must fall within 50 mils.

√	Items
	When a 2-layer PCB is designed, each HDMI trace must be shorter than 5 inches.

1.20 Design Requirements on Heat Dissipation

√	Items
	The product structure is considered during heat dissipation design. The size of the heat dissipation layer is as large as possible when the space is sufficient. The components that consume much power and generate much heat are placed in a distributed manner to avoid overheating of some parts and ensure the reliability and efficiency of components. In addition, you are advised to place the Hi3520D away from power supplies. The product architecture is optimally designed to ensure that the heat produced internally can be dissipated. If the chip has an exposed pad at the top layer of the PCB, the copper at the bottom layer should be exposed as well, which is good for heat dissipation.