Hi3520D/Hi3515A/Hi3515C Hardware Design

User Guide

Issue **03**

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About This Document

Purpose

This document describes the recommendations for Hi3520D/Hi3515A/Hi3515C schematic diagram design, PCB design, and board thermal design.

This document provides hardware design methods for the Hi3520D/Hi3515A/Hi3515C.

Related Version

The following table lists the product version related to this document:

Product Name	Related Version
Hi3520D	V100
Hi3515A	V100
Hi3515C	V100

Intended Audience

This document is intended for:

- Technical support personnel
- Board hardware development engineers

Change History

Changes between document issues are cumulative. Therefore, the latest document issue contains all changes made in previous issues.

Issue 03 (2013-07-31)

This issue is the third official release, which incorporates the following changes:

Chapter 1 Design Recommendations for Schematic Diagrams

In section 1.2.4, the descriptions of Ethernet port indicators are added.

In section 1.3.1, the pins HDMI_HOTPLUG, HDMI_CEC, HDMI_SCL, and HDMI_SDA are added to Table 1-5.

Issue 02 (2013-06-21)

This issue is the second official release, which incorporates the following changes:

The descriptions related to the Hi3515C are added.

Issue 01 (2013-05-21)

This issue is the first official release, which incorporates the following changes:

Chapter 1 Design Recommendations for Schematic Diagrams

Section 1.2.2 "RTC" is added.

In section 1.2.12, a note is added.

Chapter 2 PCB Design Recommendations

In section 2.1.1, the descriptions of the impedance design are updated.

Chapter 3 Recommendations for Board Thermal Design

The heat dissipation solution for the Hi3520D is added.

Issue 00B03 (2013-04-03)

This issue is the first draft release.

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1 Design Recommendations for Schematic Diagrams

NOTE

Unless otherwise specified, this document applies to the Hi3520D, Hi3515A and Hi3515C and uses the Hi3520D as an example.

1.1 Requirements on Circuits for the Small System

1.1.1 Clocking Circuit

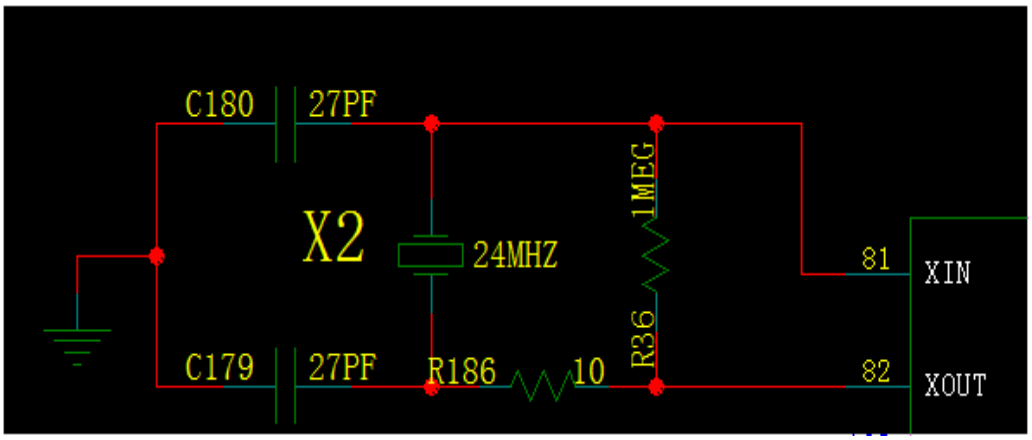
The system clock can be generated by combining the internal feedback circuit of the Hi3520D with an external 24 MHz crystal oscillator circuit.

Figure 1-1 shows the recommended connection mode of the crystal oscillator and component specifications for the system clock.

CAUTION

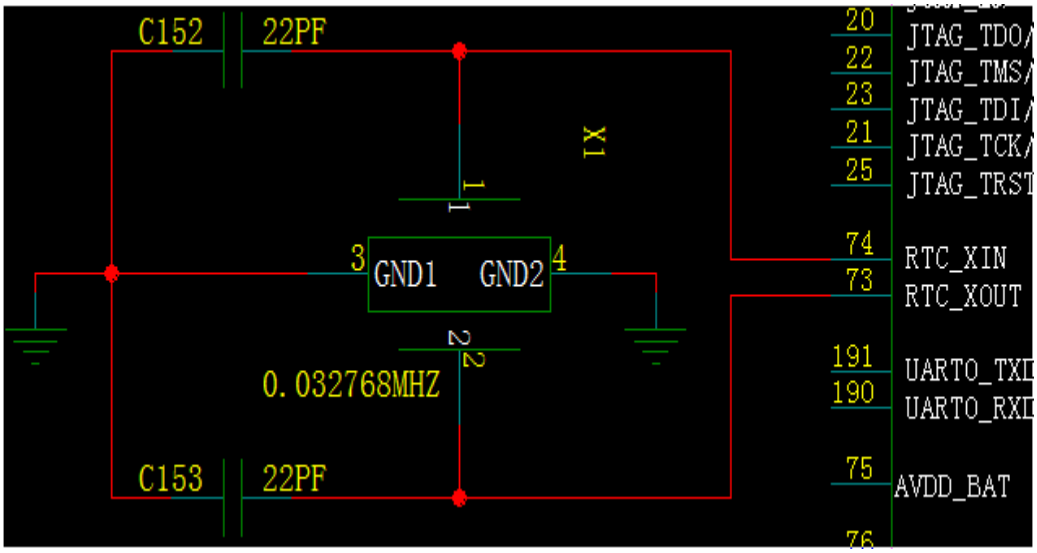
The selected capacitors must match the load capacitor of the crystal oscillator, and the capacitor material should be NPO.

Figure 1-1 Recommended connection mode of the crystal oscillator and component specifications for the system clock



The Hi3520D integrates an RTC, to which a crystal oscillator on the board must provide a clock circuit. Figure 1-2 shows the recommended connection mode of the crystal oscillator and component specifications for the RTC.

Figure 1-2 Recommended connection mode of the crystal oscillator and component specifications for the RTC



1.1.2 Reset and Watchdog Circuits

The Hi3520D RSTN pin is a reset signal input pin. The valid reset signal must have low-level pulses with a typical width of 100–300 ms.

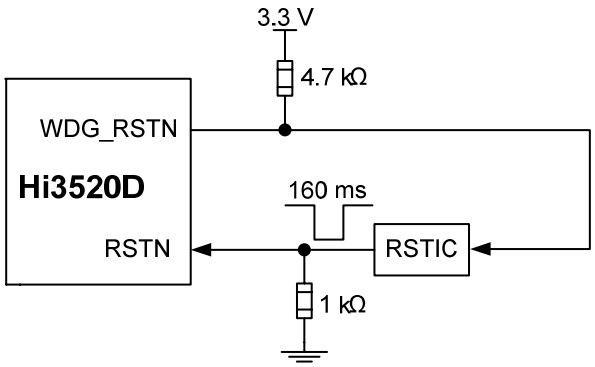
During board design, you are advised to use a dedicated reset chip to generate reset signals to ensure system stability. If a Hi3520D reset exception occurs, the Hi3520D can generate low-level pulses through the WDG_RSTN pin, which connects to an input pin on the reset chip to reset the Hi3520D system.

CAUTION

The WDG_RSTN pin is an OD output and must connect to an external pull-up resistor. This pin cannot directly connect to the RSTN pin.

Figure 1-3 shows the typical reset and watchdog circuit.

Figure 1-3 Typical reset and watchdog circuit



1.1.3 JTAG Debug Interface

The Hi3520D provides a JTAG debug interface that complies with the IEEE1149.1 standard. PCs can connect to a Realview-ICE simulator over this interface. Table 1-1 describes the signals over the JTAG debug interface.

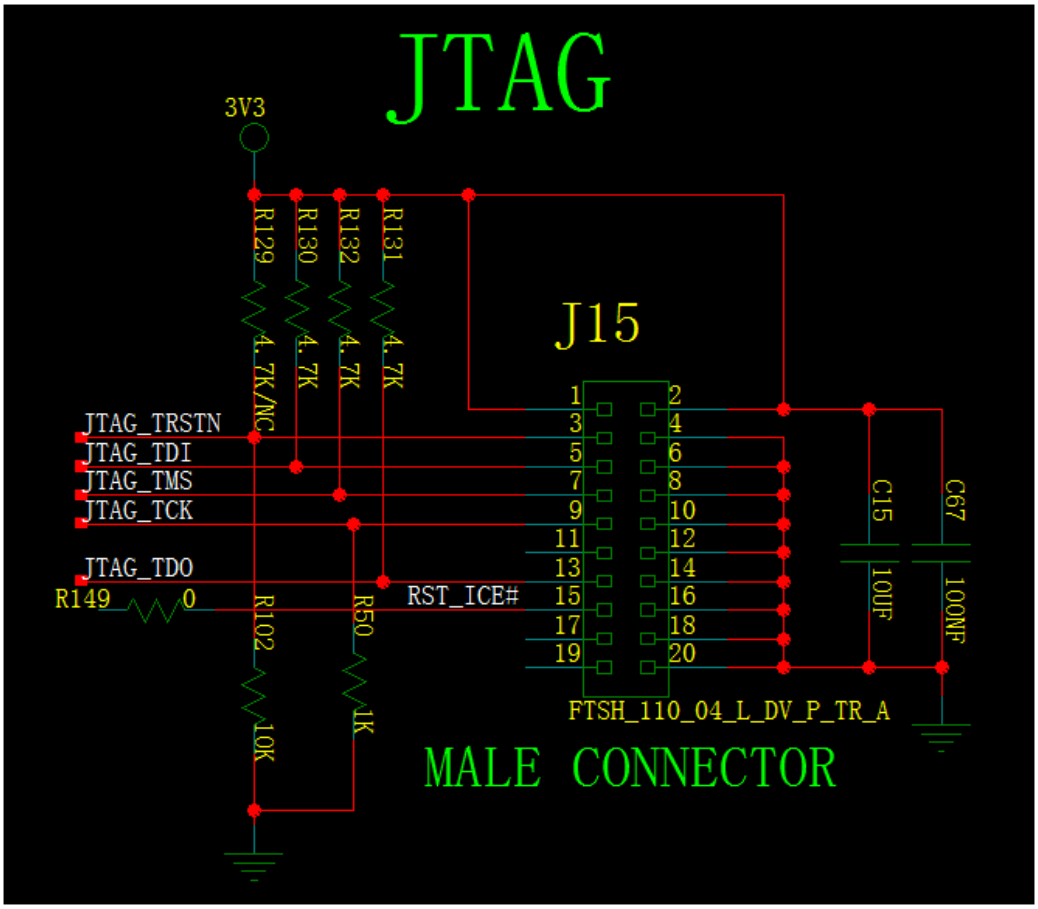
Table 1-1 Signals over the JTAG debug interface

Signal	Description
TCK	JTAG clock input, internal pull-down. A pull-down resistor must connect to this signal on the board.
TDI	JTAG data input, internal pull-up. A pull-up resistor must connect to this signal on the board.
TMS	JTAG mode select input, internal pull-up. A pull-up resistor must connect to this signal on the board.
TRSTN	JTAG reset input, internal pull-down. When the Hi3520D works properly, a pull-down resistor must connect to this signal on the board.
TDO	JTAG data output. A pull-up resistor must connect to this signal on the board.

NOTE

For details about the impedance of the external pull-up and pull-down resistors, see Figure 1-4.

Figure 1-4 JTAG connection mode and standard connector pins



The JTAG pins on the Hi3520D can be multiplexed with GPIO pins by configuring the JTAG_EN pin.

The Hi3520D works in normal or test mode, which is selected by configuring the TEST_MODE pin. If the Hi3520D works in normal mode, the pin must connect to a 10 kΩ pull-down resistor, as described in Table 1-2. The eFUSE pin must connect to GND through a 10 kΩ pull-down resistor.

Table 1-2 TEST_MODE pin configuration

TEST_MODE	Description
0	The Hi3520D works in normal mode.
1	The Hi3520D works in test mode.

1.1.4 System Configuration Circuit for Hi3520D Hardware Initialization

The Hi3520D integrates an A9 CPU and can boot from the SPI flash or BOOTROM.

The Hi3520D is compatible with various SPI flash memories, and you can select an address mode by configuring the SFC_ADDR_MODE pin.

The JTAG pins can be multiplexed with GPIO pins by configuring the JTAG_EN pin.

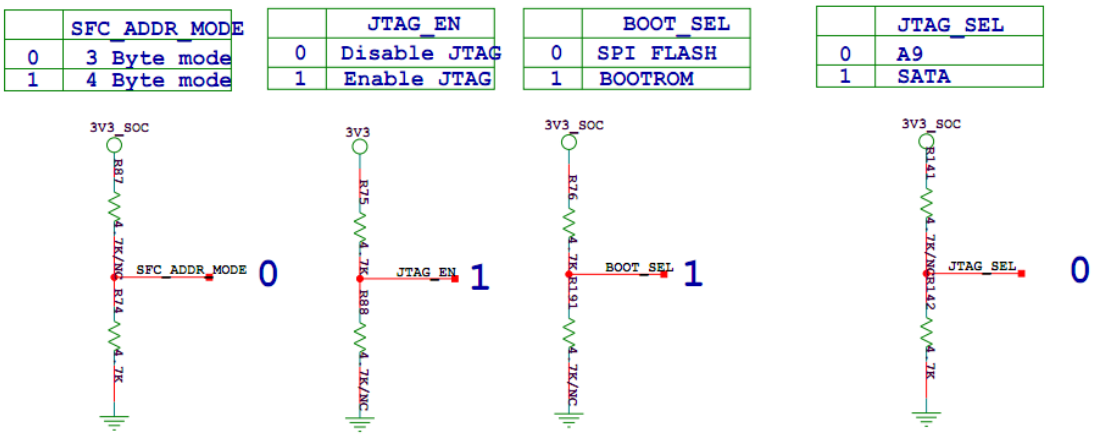
Table 1-3 describes hardware configuration signals.

Table 1-3 Hardware configuration signals

Signal	Direction	Description
BOOT_SEL	I	BOOT_SEL select. 0: The Hi3520D boots from the SPI flash. 1: The Hi3520D boots from the BOOTROM.
SFC_ADDR_MODE	I	SFC_ADDR_MODE select. 0: 3-byte mode 1: 4-byte mode
JTAG_EN	I	JTAG_EN select. 0: GPIO is selected. 1: JTAG is selected.
JTAG_SEL	I	JTAG_SEL select. 0: A9 1: SATA

The signals must be configured during Hi3520D hardware initialization. by connecting pull-up or pull-down resistors to their respective pins on the board, as shown in Figure 1-5.

Figure 1-5 Hardware initialization



1.1.5 Power Supply Circuit

For details about the requirements on the power supplies to the Hi3520D, see section 2.6 "Electrical Specifications" in the *Hi3520D/Hi3515A/Hi3515C H.264 CODEC Processor Data Sheet*.

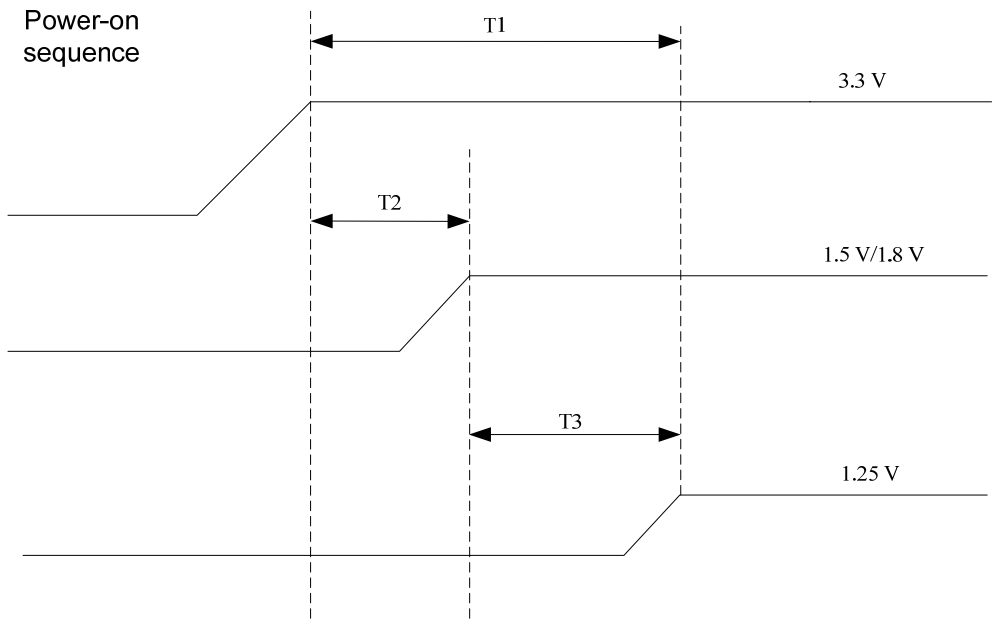
CAUTION

For details about the power parameters of the Hi3520D, see section 2.6 "Electrical Specifications" in the *Hi3520D/Hi3515A/Hi3515C H.264 CODEC Processor Data Sheet*.

Note the following when designing the power supply circuit:

- The core power pins DVDD12 connect to the 1.25 V digital power. Select a 2 A DC-DC converter for the DVDD12 pins.
- The I/O power pins DVDD33 connect to the 3.3 V digital power.
- The DDR power pins VCC15 connect to the 1.5 V (for the DDR3 SDRAM) or 1.8 V (for the DDR2 SDRAM) digital power. The pins must share the same power supply with the connected DDR SDRAM.
- The power supplies 3.3 V, 1.5 V or 1.8 V, and 1.25 V are powered on in sequence, as shown in Figure 1-6.

Figure 1-6 Power-on sequence



NOTE

As shown in Figure 1-6, T1, T2, and T3 are greater than 0 ms, and the maximum value for T1 is 100 ms. The voltage of the high level must be always higher than that of the low level.

- The PLL power pins AVDD12_PLL and AVDD33_PLL are isolated from the 1.25 V and 3.3 V power supplies by using EMI beads whose specifications are 1000 R@100 MHz. For details about the circuit design, see the schematic diagram of the Hi3520D demo board.
- Ensure that the output voltage of each power supply meets the Hi3520D requirements even when ripples and noises occur. For details about the power supply requirements of each module, see the "Electrical Specifications" section in the *Hi3520D/Hi3515A/Hi3515C H.264 CODEC Processor Data Sheet*.

1.2 Design of Hi3520D Interface Circuits

1.2.1 DDR2 or DDR3 Interface

1.2.1.1 Introduction

The Hi3520D DDR interface can be a DDR2 interface complying with the SSTL-18 standard or a DDR3 interface complying with the SSTL-15 standard.

The Hi3520D DDRC has the following features:

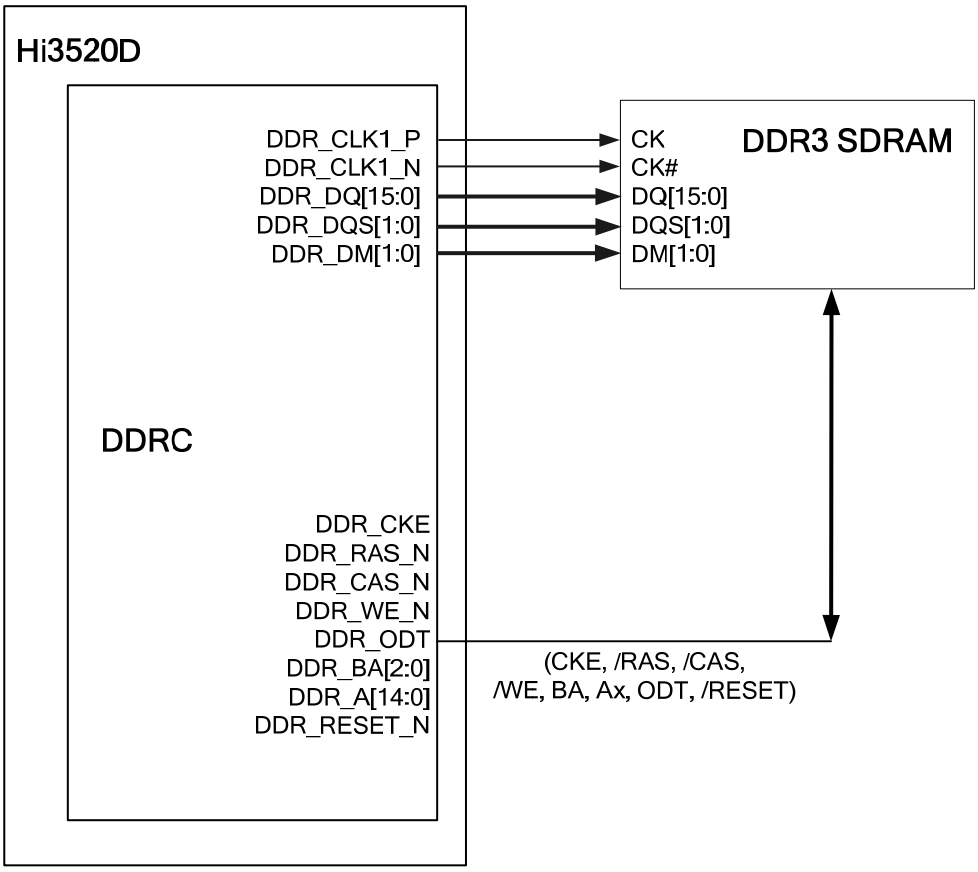
- Provides one DDRC interface without chip select (CS) signals and supports the 16-bit data bus and at most 15-bit address bus.
- Connects to a 16-bit DDR2 SDRAM with a maximum capacity of 128 MB at the 400–533 MHz bus frequency.
- Connects to a 16-bit DDR3 SDRAM with a maximum capacity of 512 MB at the 533–660 MHz bus frequency.

1.2.1.2 Circuit Design Recommendations

DDR Topology

Figure 1-7 shows the typical topology for connecting the Hi3520D to a DDR3 SDRAM. For details about the circuit design, see the schematic diagram of the Hi3520D demo board.

Figure 1-7 Typical topology for connecting the Hi3520D to a DDR3 SDRAM.



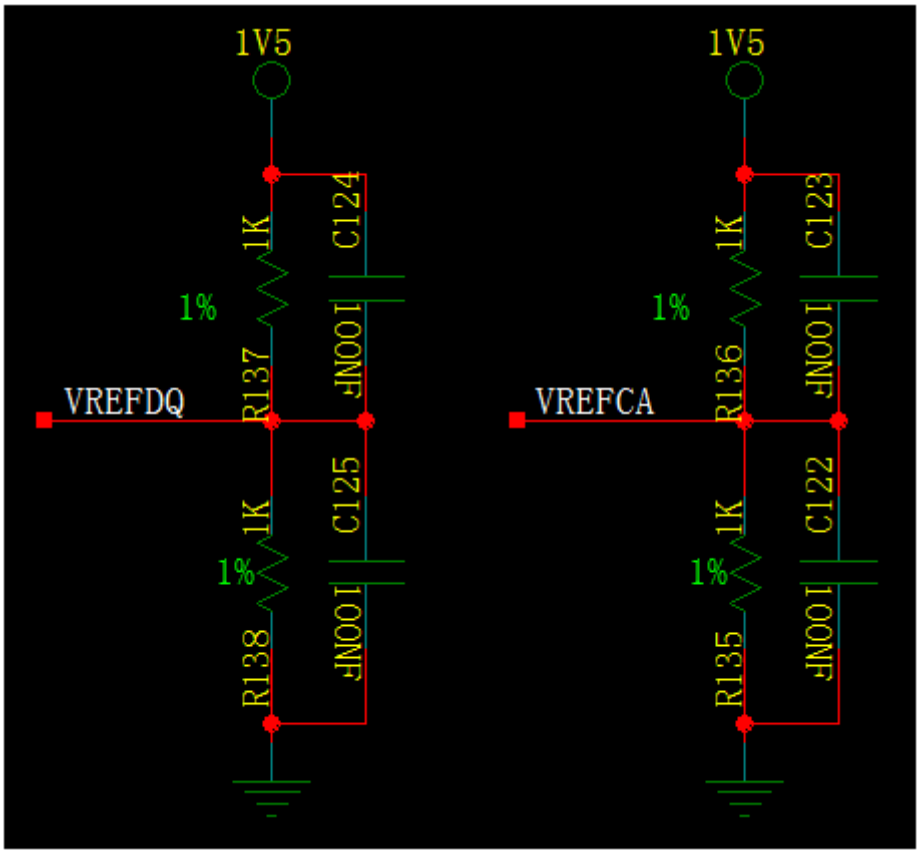
DDR Power Supply

The Hi3520D DDRC and its interface comply with the DDR3 SSTL-15 or DDR2 SSTL-18 standard. The 1.5 V or 1.8 V power supply and 0.75 V or 0.9 V reference voltage Vref are required. The Hi3520D and DDR SDRAM must share the 1.5 V or 1.8 V power.

A separate power chip must be provided on the board to supply power to the DDR3 or DDR2 SDRAM and the 1.5 V or 1.8 V power pin of the Hi3520D DDRC. The 0.75 V or 0.9 V reference voltage must be supplied to the DDR3 or DDR2 SDRAM and the reference power pin Vref by using a 1 kΩ±1% voltage-divider resistor. A 0.1 μF decoupling capacitor must be placed close to each power pin and reference power pin. VREFDQ and VREFCA must be powered separately.

Figure 1-8 shows the reference design of the DDR3 voltage-divider circuit. The DDR2 voltage-divider circuit is similar to the DDR3 voltage-divider circuit except that the voltage is 1.8 V.

Figure 1-8 Reference design of the DDR3 voltage-divider circuit



1.2.1.3 Design Recommendations for Matched Modes

Bidirectional DQ and DQS Signals

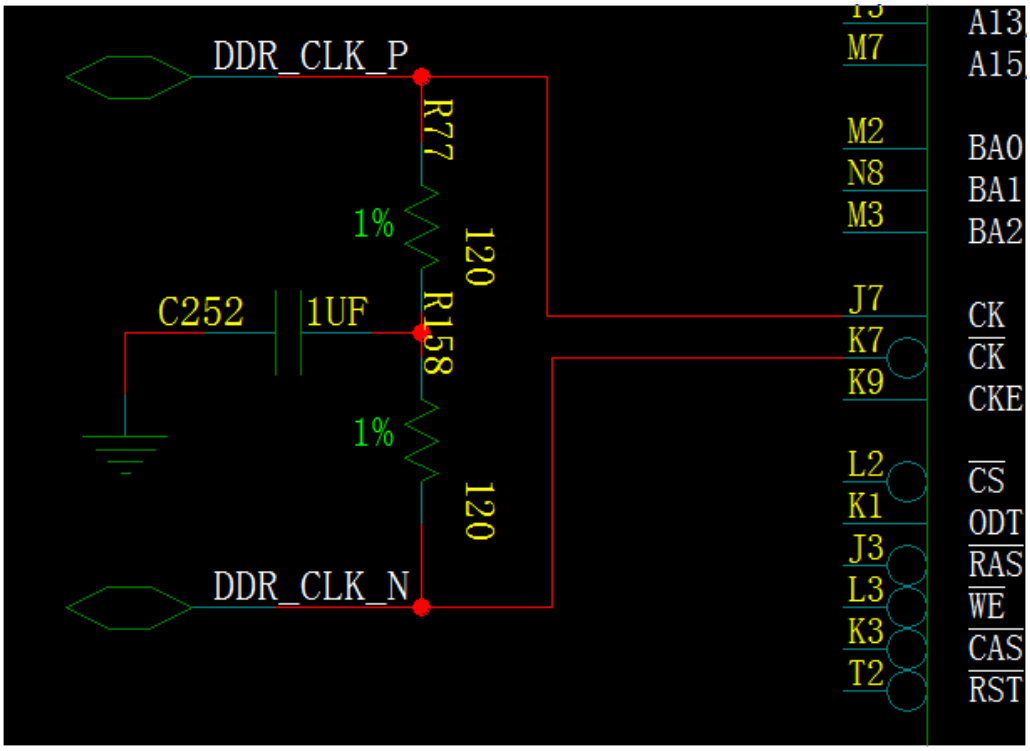
When the Hi3520D connects to a DDR SDRAM, the DQ, DQS_P, and DQS_N signals on the Hi3520D directly connect to the DQ, DQS_P, and DQS_N signals on the DDR SDRAM respectively.

Differential Clocks

When the Hi3520D connects to a DDR SDRAM, the DDR_CLK_N and DDR_CLK_P signals on the Hi3520D directly connect to the DDR_CLK_N and DDR_CLK_P signals on the DDR SDRAM respectively.

When a DDR3 SDRAM is connected, a matched 120 Ω±1% resistor must be added between the two differential clock signal traces at the terminal end, as shown in Figure 1-9.

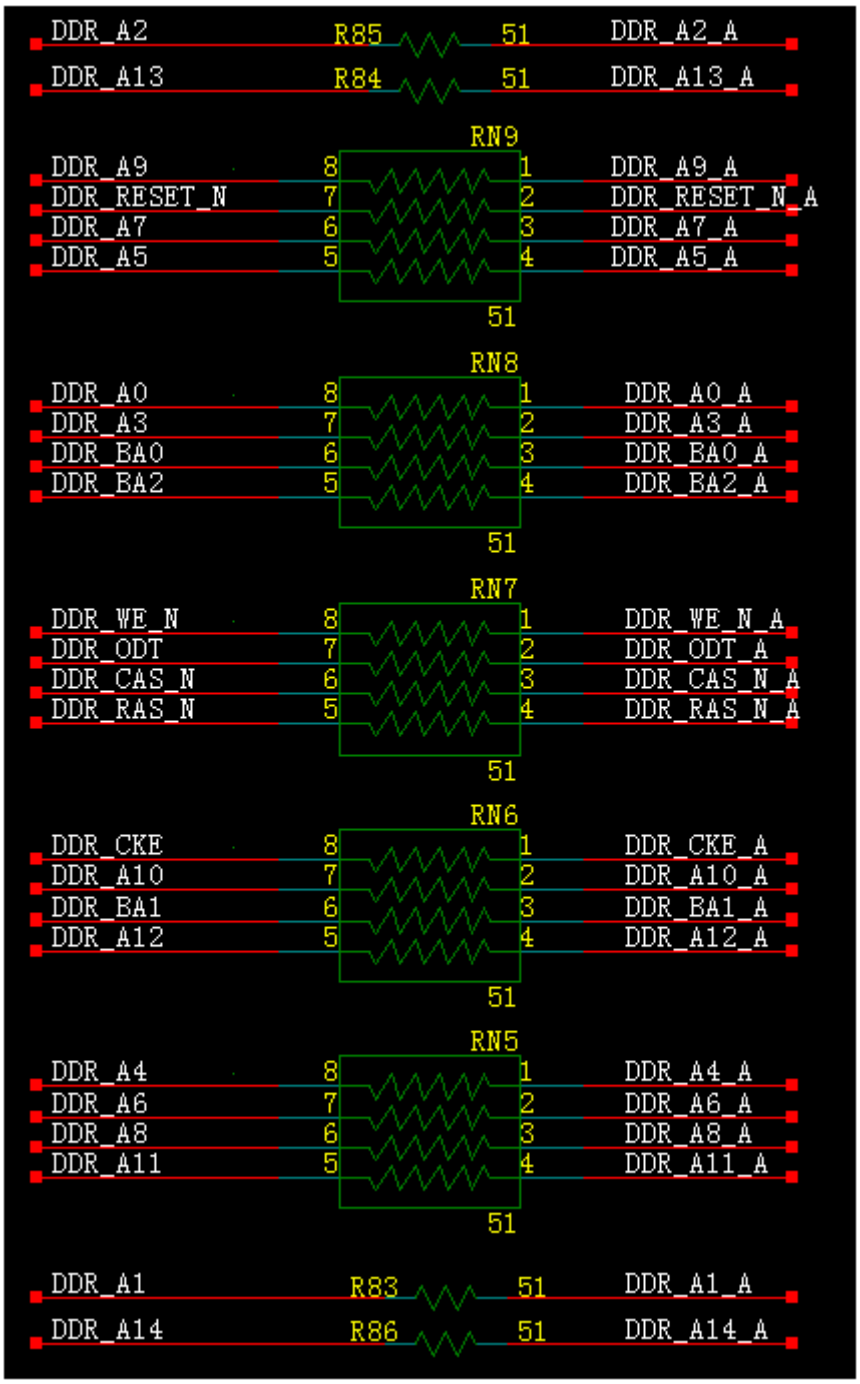
Figure 1-9 Connecting a matched resistor between the two differential clock signal traces at the terminal end



Address Signals and Control Signals

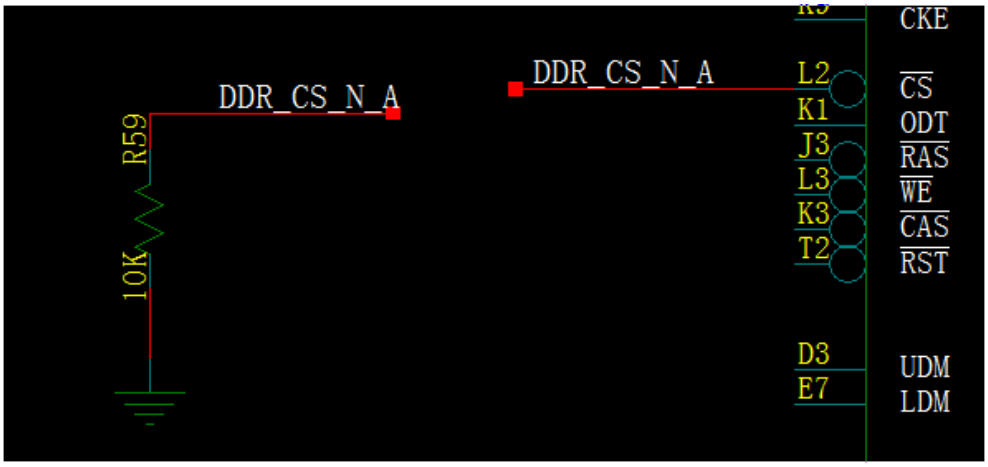
When the Hi3520D connects to the DDR3 or DDR2 SDRAM, the address signals and control signals on the Hi3520D directly connect to the address signals and control signals on the DDR SDRAM respectively. A 51 Ω series resistor must be added for connecting the Hi3520D and DDR SDRAM, as shown in Figure 1-10.

Figure 1-10 Connecting the address and control signals on the Hi3520D to those on the DDR SDRAM



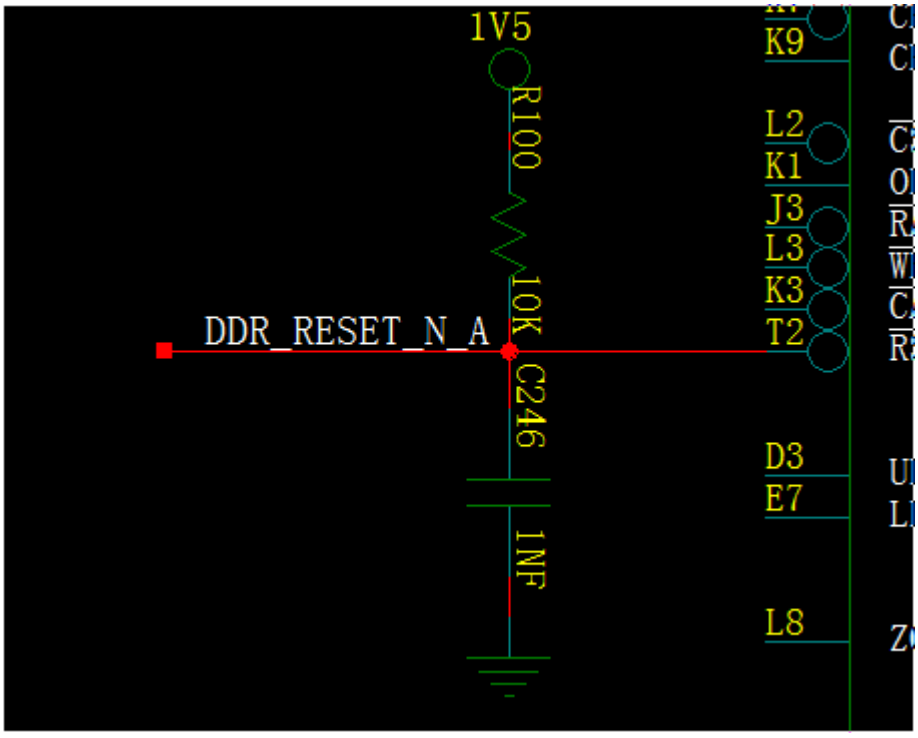
- Because the DDR_CS_N pin is not provided on the Hi3520D, the /CS pin on the DDR SDRAM must connect to GND through a 10 kΩ pull-down resistor, as shown in Figure 1-11.

Figure 1-11 Connection diagram of the DDR_CN_N pin



- The DDR_CKE pin must connect to GND through a 10 kΩ pull-down resistor.
- The DDR_RESET_N pin must connect to 1.5 V through a 10 kΩ pull-up resistor and connect to GND through a 1 nF capacitor, as shown in Figure 1-12.

Figure 1-12 Connection diagram of the DDR_RESET_N pin



DM Signals

When the Hi3520D connects to the DDR3 or DDR2 SDRAM, the data mask (DM) signals on the DDR2 or DDR3 SDRAM directly connect to those on the Hi3520D.

External Resistor for the DDR SDRAM

An external 240 Ω resistor (ZQ) connects to the ZQ pin on the DDR3 SDRAM.

1.2.2 RTC

In fixed frequency-division mode, the timing accuracy of the embedded RTC depends on the external crystal oscillator. Select an appropriate crystal oscillator based on its frequency deviation and temperature offset. If high timing accuracy is required, the external integrated RTC is recommended.

1.2.3 USB 2.0 Host Port

1.2.3.1 Introduction

The Hi3520D provides a USB 2.0 host port that complies with the USB 2.0 protocol and supports low-speed, high-speed, and full-speed modes. The independent USB 2.0 host module can be disabled when no data is transferred. This reduces the Hi3520D power consumption.

1.2.3.2 Circuit Design Recommendations

USB Power Supply

The analog power supply AVDD33_USB must be isolated from the digital power supply by using an EMI bead, and filtering capacitors must be placed close to the pins.

USB Protective Circuit

A protective circuit must be designed on the USB circuit to ensure electrostatic discharge (ESD) protection. To prevent USB traces from being affected by protective components, follow these guidelines:

- Place protective components close to the USB connector port.
- Ensure that the parasitic capacitors of protective components connected to the USB 2.0 host port are less than 1 pF and the response time is less than 1 ns.

1.2.4 Embedded FE PHY Interface

The Hi3520D provides an embedded 100M Ethernet PHY. The analog power supplies AVDD33_FE and AVDD12_FE must be provided on the board for supplying power to the embedded PHY. The two analog power supplies must be isolated from the digital power by using EMI beads, and filtering capacitors must be placed close to the pins.

CAUTION

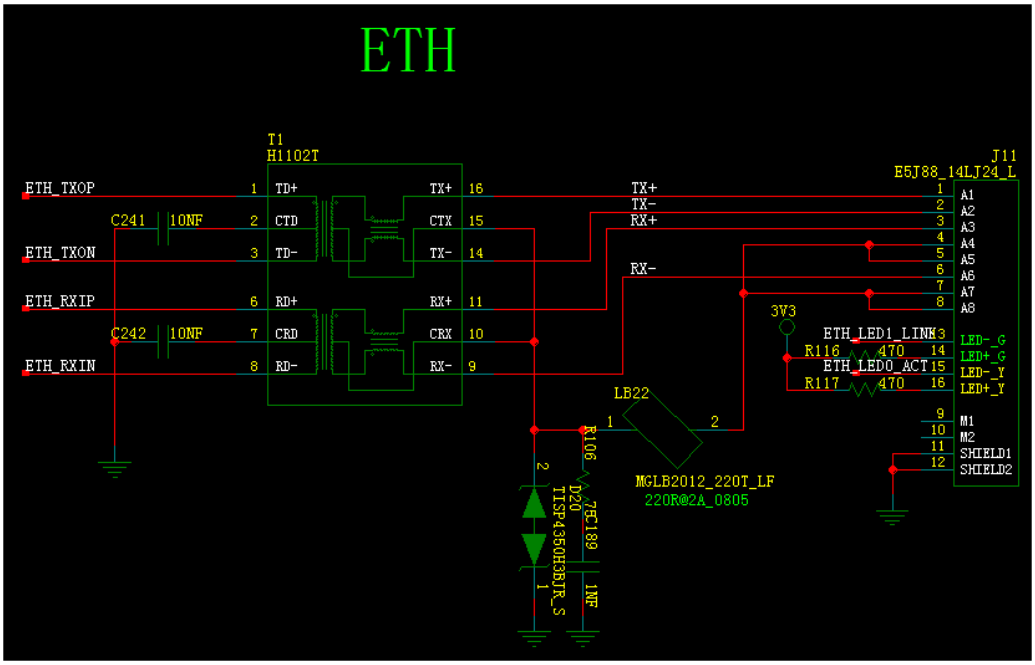
Take antistatic and anti-surge measures on the board to prevent the Hi3520D from being damaged by the network cable ESD or surge.

The external pin ETH_RSET must connect to GND though a 2.49 kΩ±1% resistor.

Figure 1-13 shows the circuit of the embedded FE PHY on the board. For details about the circuit design, see the schematic diagram of the Hi3520D demo board.

The pins 171 and 172 can be used to control Ethernet port indicators. The specific functions can be configured by using software.

Figure 1-13 Circuit of the embedded FE PHY on the board



1.2.5 RMII

The Hi3520D provides one reduced media independent interface (RMII) for connecting to an external Ethernet PHY.

CAUTION

The Hi3520D provides only one ETH port. To be specific, when the embedded PHY is used, the external PHY connected on the RMII cannot be used, and vice versa. The switching is based on software configuration.

1.2.6 Flash Interface

The Hi3520D supports the SPI NOR flash.

The Hi3520D SPI NOR flash controller (NFC) provides two CSs to support two flash memories or a flash memory with two CS pins.

CAUTION

If the Hi3520D boots from the SPI NOR flash, the CS of the SPI NOR flash must connect to SFC_CS1N on the Hi3520D.

1.2.7 SATA Interface

The Hi3520D/Hi3515A provides two SATA interfaces, whereas the Hi3515C provides only one SATA interface. The SATA interface supports PM, eSATA, and clock gating. When the SATA interfaces are not in use, they can be powered down to reduce power consumption.

- The SATA interface power supplies AVDD12_SATA and AVDD33_SATA must be isolated from the 1.25 V and 3.3 V power supplies by using EMI beads, and filtering capacitors must be placed close to the pins.
- The 10 nF X7R multilayer ceramic capacitor connecting to the Rx and Tx differential signals in series must be placed close to the SATA connector.
- The impedance of the SATA differential traces must fall within 100 Ω, and the maximum trace length is 3 inches.

1.2.8 SPI Control Interface

The Hi3520D provides one SPI clock signal, one data input pin, one data output pin, and two CS signals, which are used to connect peripherals that provide SPI control interfaces. The maximum clock frequency of SPI_CLK is 40 MHz.

- For a single load, connect a 33 Ω resistor to the SPI_CLK at the source end in series and directly connect the two data lines.
- For multiple loads, if the recommended daisy chain connection mode is used, consider a trace delay and a delay of passing through components when setting the working frequency for SPI_CLK. The reference value of the 1000 mil trace delay is 180 ps.

1.2.9 Audio Interface

The Hi3520D provides one I^2S audio signal input interface, one I^2S audio signal output interface, and an MCLK signal. The connection modes in master and slave modes are different when the two I^2S audio signal interfaces are combined into one audio input and output interface for intercom, as shown in Figure 1-14 and Figure 1-15. In slave mode, the BCLK and WCLK signals must connect to the two groups of I^2S signals simultaneously.

Figure 1-14 Connection mode when the Hi3520D works in master mode

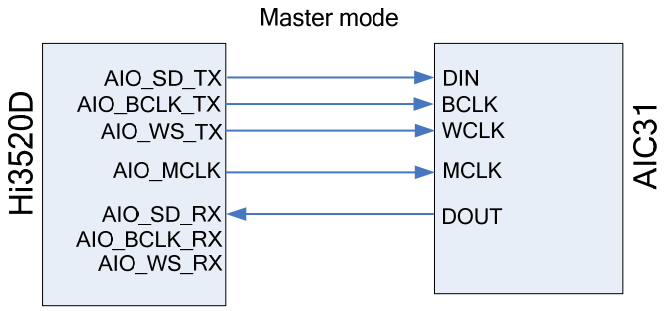
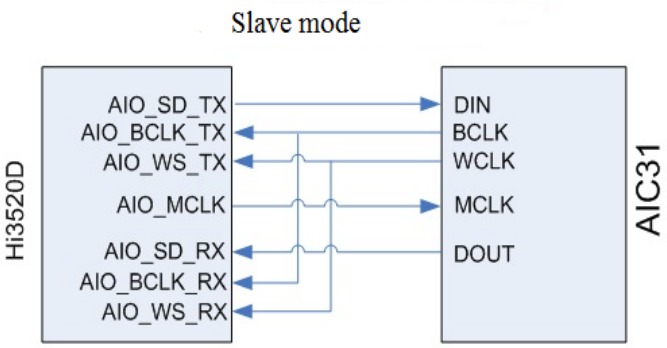


Figure 1-15 Connection mode when the Hi3520D works in slave mode



1.2.10 HDMI Output Interface

The Hi3520D has an embedded HDMI PHY that directly outputs HDMI signals.

- The 1.25 V power supply to the HDMI module must be isolated from the 1.25 V system power supply by using an EMI bead, and sufficient filtering capacitors must be placed close to the Hi3520D pins. You are advised to use an EMI bead with the specifications of 1 kΩ@100 MHz. A 100 μF/6.3 V ceramic capacitor must be added between the Hi3520D and the EMI bead.
- It is recommended that the HDMI_REXT pin externally connect to a 11 kΩ±1% resistor and a 39 kΩ±1% resistor in parallel.
- The four sets of HDMI differential signals must be protected by ESD components that are placed close to the HDMI interface.

1.2.11 Analog VDAC Interface

The Hi3520D provides two groups of VDAC signals.

- VDAC_R, VDAC_G, and VDAC_B in the first group act as video graphics array (VGA) outputs. Ensure proper impedance matching during design. The VDAC_COMP pin is pulled up to AVDD33_VDAC through a 10 nF capacitor and a 10 μF capacitor in parallel. The VDAC_REXT pin connects to GND through a 390 Ω±1% resistor and a 3.01

kΩ±1% resistor in parallel. The R, G, B signals and VGA_HS or VGA_VS can be output as a VGA signal. For details, see the schematic diagram of the Hi3520D demo board.

- VDAC_ CVBS0 and VDAC_ CVBS0 in the second group act as CVBS outputs. Ensure proper impedance matching during design. The VDAC_COMPS pin is pulled up to AVDD33_VDAC through a 10 nF capacitor and a 10 μF capacitor in parallel. The VDAC_REXTS pin connects to GND through a 191 Ω±1% resistor in parallel.
- The 3.3 V power supply to the two groups of video DACs must be isolated from the 3.3 V system power supply by using an EMI bead, and sufficient filtering capacitors must be placed close to the pins of the analog DAC 3.3 V power supply.
- Note that the HD picture-in-picture (PIP) function is multiplexed with the CVBS0 output function. If the HD PIP function is used, the CVBS0 output is unavailable. If both the HD PIP and SD CVBS output functions are required, the SD CVBS signals must be output from the CVBS1 interface.

1.2.12 VI Interface

The Hi3520D provides two BT.656 interfaces: VIU0 and VIU1. The Hi3515A/Hi3515C provides one BT.656 interface: VIU0.

- VIU0 and VIU1 act as BT.656 input interfaces.
- Big-endian and little-endian modes are supported. The sequence of DATA[0:7] can be reverse. The VIU_CLK sequence can be selected by multiplexing configuration. The AD pins described in Table 1-4 can be connected.
- The two BT.656 interfaces can be combined into a BT.1120 interface. The upper eight bits, the low eight bits, and the clock can be configured by using a register.
- VI_ADC_CLK can output 24 MHz, 27 MHz, and 54 MHz clocks, which are used for different AD pins.
- When the BT.656 signal line connects to the Hi3520D, Hi3515A or Hi3515C VI interface, appropriate serial resistors must be selected based on the drive capability of the ADC and trace length.

Table 1-4 Sequence of the connected AD pins

Pin No.	Sequence of Pins on the Hi3520D	Sequence of Connected AD Pins			
		Normal DATA Sequence	Reverse DATA Sequence	Adjusted CLK Sequence and Normal DATA Sequence	Adjusted CLK Sequence and Reverse DATA Sequence
114	VIU0_DAT7	VIU0_DAT7	VIU0_DAT0	VIU0_CLK	VIU0_CLK
113	VIU0_DAT6	VIU0_DAT6	VIU0_DAT1	VIU0_DAT7	VIU0_DAT0
112	VIU0_DAT5	VIU0_DAT5	VIU0_DAT2	VIU0_DAT6	VIU0_DAT1
111	VIU0_DAT4	VIU0_DAT4	VIU0_DAT3	VIU0_DAT5	VIU0_DAT2
109	VIU0_DAT3	VIU0_DAT3	VIU0_DAT4	VIU0_DAT4	VIU0_DAT3
108	VIU0_DAT2	VIU0_DAT2	VIU0_DAT5	VIU0_DAT3	VIU0_DAT4

Pin No.	Sequence of Pins on the Hi3520D	Sequence of Connected AD Pins			
		Normal DATA Sequence	Reverse DATA Sequence	Adjusted CLK Sequence and Normal DATA Sequence	Adjusted CLK Sequence and Reverse DATA Sequence
107	VIU0_DAT1	VIU0_DAT1	VIU0_DAT6	VIU0_DAT2	VIU0_DAT5
106	VIU0_DAT0	VIU0_DAT0	VIU0_DAT7	VIU0_DAT1	VIU0_DAT6
104	VIU0_CLK	VIU0_CLK	VIU0_CLK	VIU0_DAT0	VIU0_DAT7
103	VIU1_DAT7	VIU1_DAT7	VIU1_DAT0	VIU1_CLK	VIU1_CLK
102	VIU1_DAT6	VIU1_DAT6	VIU1_DAT1	VIU1_DAT7	VIU1_DAT0
101	VIU1_DAT5	VIU1_DAT5	VIU1_DAT2	VIU1_DAT6	VIU1_DAT1
100	VIU1_DAT4	VIU1_DAT4	VIU1_DAT3	VIU1_DAT5	VIU1_DAT2
99	VIU1_DAT3	VIU1_DAT3	VIU1_DAT4	VIU1_DAT4	VIU1_DAT3
98	VIU1_DAT2	VIU1_DAT2	VIU1_DAT5	VIU1_DAT3	VIU1_DAT4
97	VIU1_DAT1	VIU1_DAT1	VIU1_DAT6	VIU1_DAT2	VIU1_DAT5
96	VIU1_DAT0	VIU1_DAT0	VIU1_DAT7	VIU1_DAT1	VIU1_DAT6
94	VIU1_CLK	VIU1_CLK	VIU1_CLK	VIU1_DAT0	VIU1_DAT7

1.3 Descriptions of Special Pins

1.3.1 Pins with the 5 V Withstand Voltage

Table 1-5 describes pins with the 5 V withstand voltage.

Table 1-5 Pins with the 5 V withstand voltage

No.	Pin	Withstand Voltage
115	I2C_SCL	3.3 V/5.0 V
116	I2C_SDA	3.3 V/5.0 V
190	UART0_RXD	3.3 V/5.0 V
191	UART0_TXD	3.3 V/5.0 V
29	IR_IN	3.3 V/5.0 V
30	SATA_LED_N0	3.3 V/5.0 V

No.	Pin	Withstand Voltage
31	SATA_LED_N1 (the Hi3515C supports only SATA0)	3.3 V/5.0 V
27	GPIO1_0	3.3 V/5.0 V
28	GPIO1_1	3.3 V/5.0 V
131	HDMI_HOTPLUG	3.3 V/5.0 V
135	HDMI_CEC	3.3 V/5.0 V
134	HDMI_SCL	3.3 V/5.0 V
133	HDMI_SDA	3.3 V/5.0 V

1.3.2 Pins Not Multiplexed with GPIOs

The pins described in Table 1-6 are used as outputs by default and cannot be multiplexed with GPIOs. If the pins are multiplexed with GPIOs, both ends may act as outputs after being powered on and conflict occurs.

Table 1-6 Pins not multiplexed with GPIOs

No.	Pin
88	AIO_MCLK
85	AIO_SD_TX
69	SPI_SDO

1.3.3 Unused Pins During the Design

Table 1-7 describes how to process unused pins.

Table 1-7 Methods for processing unused pins

Module	Pin	Processing Mode
JTAG	JTAG_EN	Connect to a 4.7 kΩ pull-down resistor.
	JTAG_TCK JTAG_TMS JTAG_TRSTN JTAG_TDO JTAG_TDI	Set them as output GPIOs, which can be floated.
SATA (the Hi3515C supports	AVDD12_SATA	Keep its power on.
	AVDD33_SATA	Keep its power on.

Module	Pin	Processing Mode
only SATA0)	SATA_TX0P	These pins can be floated.
	SATA_TX0M	
	SATA_RX0P	
	SATA_RX0M	
	SATA_TX1P	
	SATA_TX1M	
	SATA_RX1P	
	SATA_RX1M	
	SATA_REXT	Connect to a 191 Ω±1% resistor.
	SATA_LED_N0	This pin can be floated.
	SATA_LED_N1	This pin can be floated.
USB	AVDD33_USB	Keep its power on.
	USB0_DP	These pins can be floated.
	USB0_DM	
	USB1_DP	
	USB1_DM	
	USB_REXT	Connect to a 43.2 Ω±1% resistor.
	USB0_OVRCUR	Set them as output GPIOs, which can be floated.
	USB0_PWREN	
	USB1_OVRCUR	
	USB1_PWREN	
FE PHY	AVDD12_FE	Keep its power on.
	AVDD33_FE	Keep its power on.
	ETH_RXIN	These pins can be floated.
	ETH_RXIP	
	ETH_TXON	
	ETH_TXOP	
	ETH_RSET	Connect this pin to a 2.49 kΩ±1% pull-down resistor.
SPI	All pins on the	These pins can be floated.

Module	Pin	Processing Mode
	module	
VI	All pins on the module	These pins can be floated.
AIO	All pins on the module	These pins can be floated.

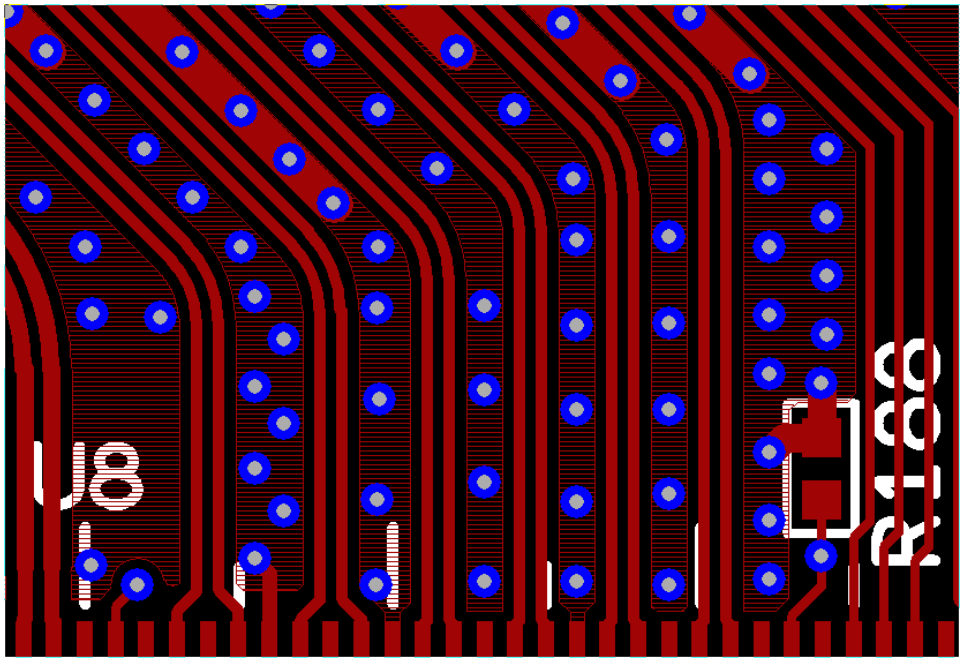
2 PCB Design Recommendations

2.1 Design Requirements on a 2-Layer PCB

2.1.1 Impedance Control

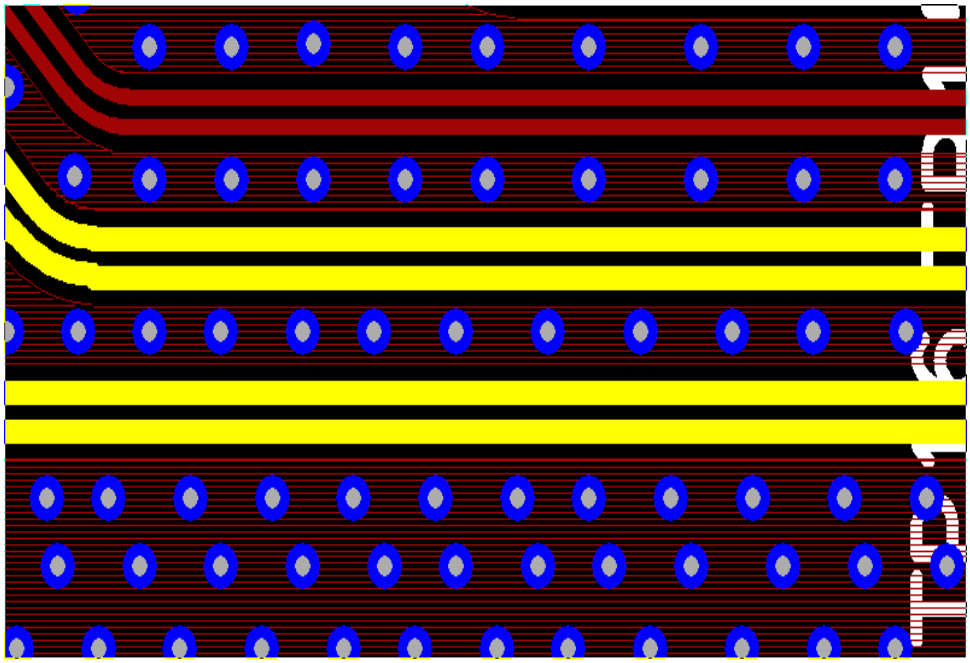
- The layouts and routing of power supplies to the DDR SDRAM and Hi3520D must be the same as those on the Hi3520D demo board.
- For details about the impedance design for the 2-layer PCB, see the actual impedance of the Hi3520D demo board as follows:
  - The impedance of high-speed traces such as SATA, HDMI, and network port differential traces must fall within 100 Ω±10%. The impedance of differential traces on a 2-layer PCB can be controlled by surrounding the differential traces with GND traces. The 100 Ω differential trace width is 6 mils, the trace spacing is 5 mils, and the spacing between a differential trace and GND copper is 6 mils, as shown in Figure 2-1.

Figure 2-1 Differential traces within 100 Ω



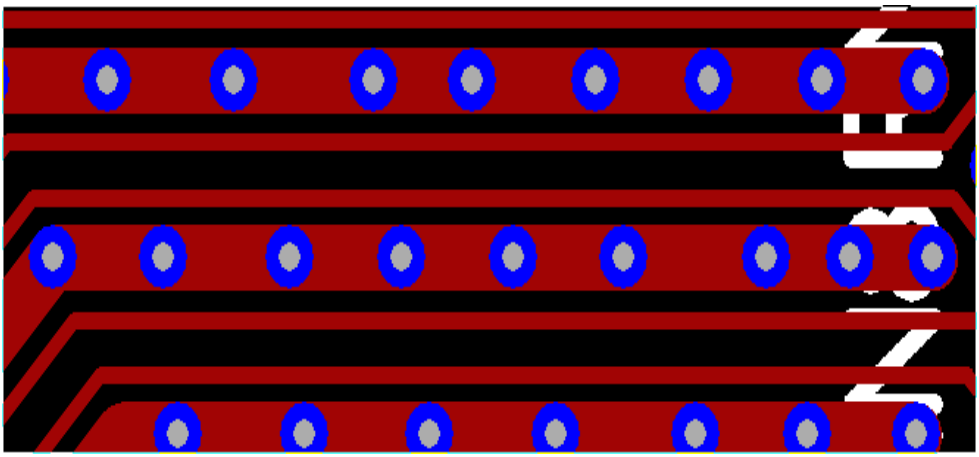
- The impedance of USB differential traces must fall within 90 Ω±10%. The impedance of USB differential traces on a 2-layer PCB can be controlled by surrounding the differential traces with GND traces. The 90 Ω differential trace width is 9 mils, the trace spacing is 5 mils, and the spacing between a differential trace and GND copper is 6 mils, as shown in Figure 2-2.

Figure 2-2 Differential traces within 90 Ω



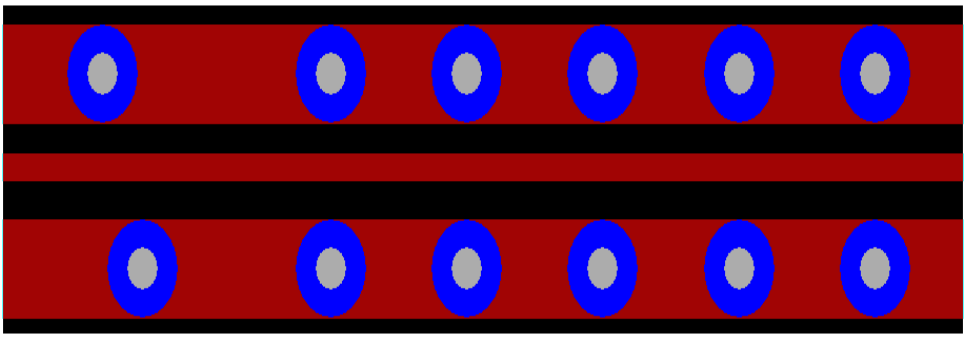
- The 5-mil single-ended signal trace is surrounded with GND traces on one side, and the impedance of the single-ended signal trace must be 85 Ω±10%. See the DDR data trace, DDR address trace, or DDR command trace in Figure 2-3. The spacing between the GND trace and the DDR data trace, DDR address trace, or DDR command trace is 5 mils.

Figure 2-3 Impedance control when the single-ended signal trace is surrounded with GND traces on one side



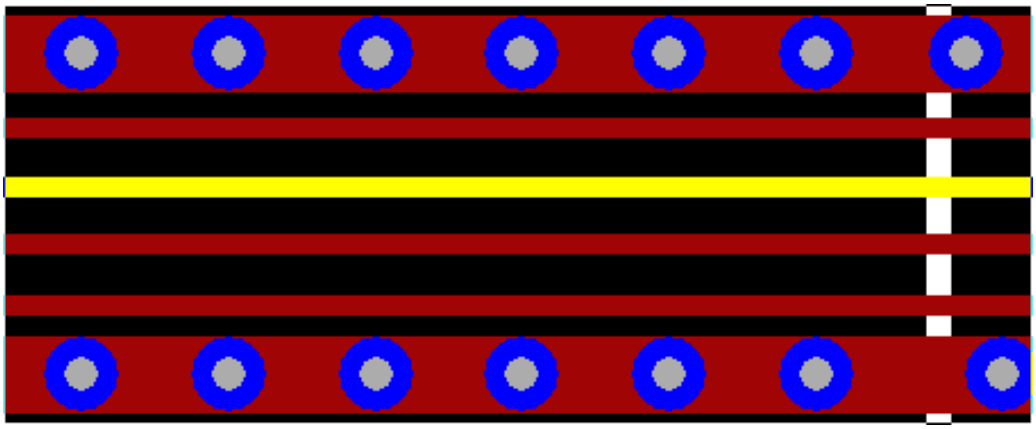
- The 5-mil single-ended signal trace is surrounded with GND traces on both sides, and the impedance of the single-ended signal trace must be 70 Ω±10%. See the CLK trace in Figure 2-4. The spacing between the GND trace and the CLK trace is 5 mils.

Figure 2-4 Impedance control when the single-ended signal trace is surrounded with GND traces on both sides



- The 5-mil single-ended signal trace is surrounded with other signal traces but not GND traces, and the impedance of the single-ended signal trace must be 100 Ω±10%. See the yellow trace between the VI traces in Figure 2-5.

Figure 2-5 Impedance control when other signal traces are routed around the single-ended signal trace

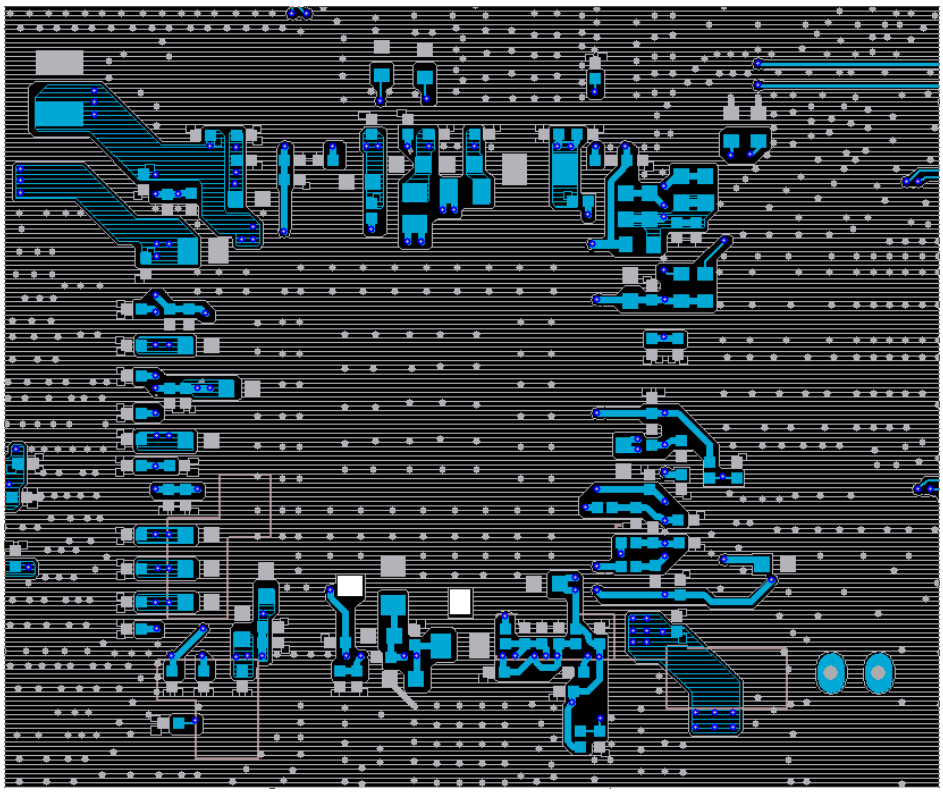


2.1.2 Signal Integrity

A 2-layer PCB has no separate GND plane. To ensure connectivity and integrity of the GND plane, meet the following requirements:

- Place few components or never place components at the bottom layer (especially under the Hi3520D) to ensure that the bottom layer has a complete GND plane. Figure 2-6 shows the connectivity diagram of the GND plane under the Hi3520D demo board.

Figure 2-6 Connectivity diagram of the GND plane under the Hi3520D



- Punch more GND vias in areas where traces are not routed to ensure that the GND coppers at the top layer connect to those at the bottom layer.
- Ensure that no GND copper island exists and as many as possible coppers are connected to shorten signal return paths.
- Ensure that the bottom layer has a complete GND plane under high-speed signal traces and no traces pass through this plane.
- Key signal traces such as crystal oscillator, system reset, I^2C, and CLK traces must be surrounded with GND traces to ensure impedance continuity and to guard against interference and electromagnetic radiation.
- The Hi3520D has an exposed pad at the top layer of the PCB. Therefore, the copper at the bottom layer should be exposed as well, which is good for heat dissipation.

2.2 Design Recommendations for Power Supplies and Filtering Capacitors

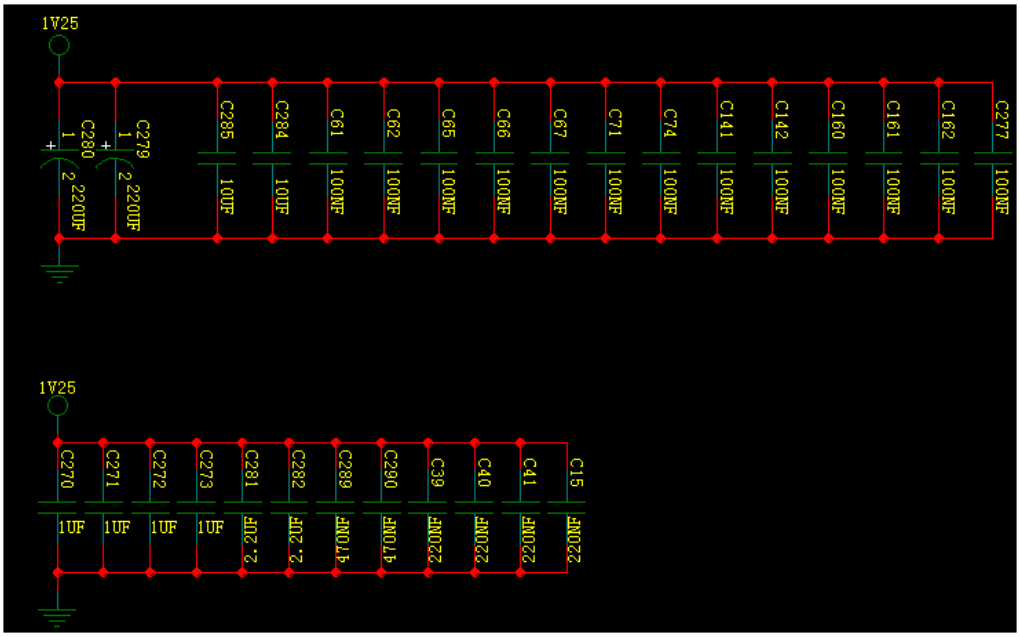
2.2.1 Core Power Supply

Type and Number of Filtering Capacitors

The type, number, and layout of filtering capacitors for the core power supply must be the same as those on the Hi3520D demo board. The recommended material for the filtering

capacitors is X7R. For details, see the schematic diagram of the Hi3520D demo board. Figure 2-7 shows the number and type of filtering capacitors for the core power supply.

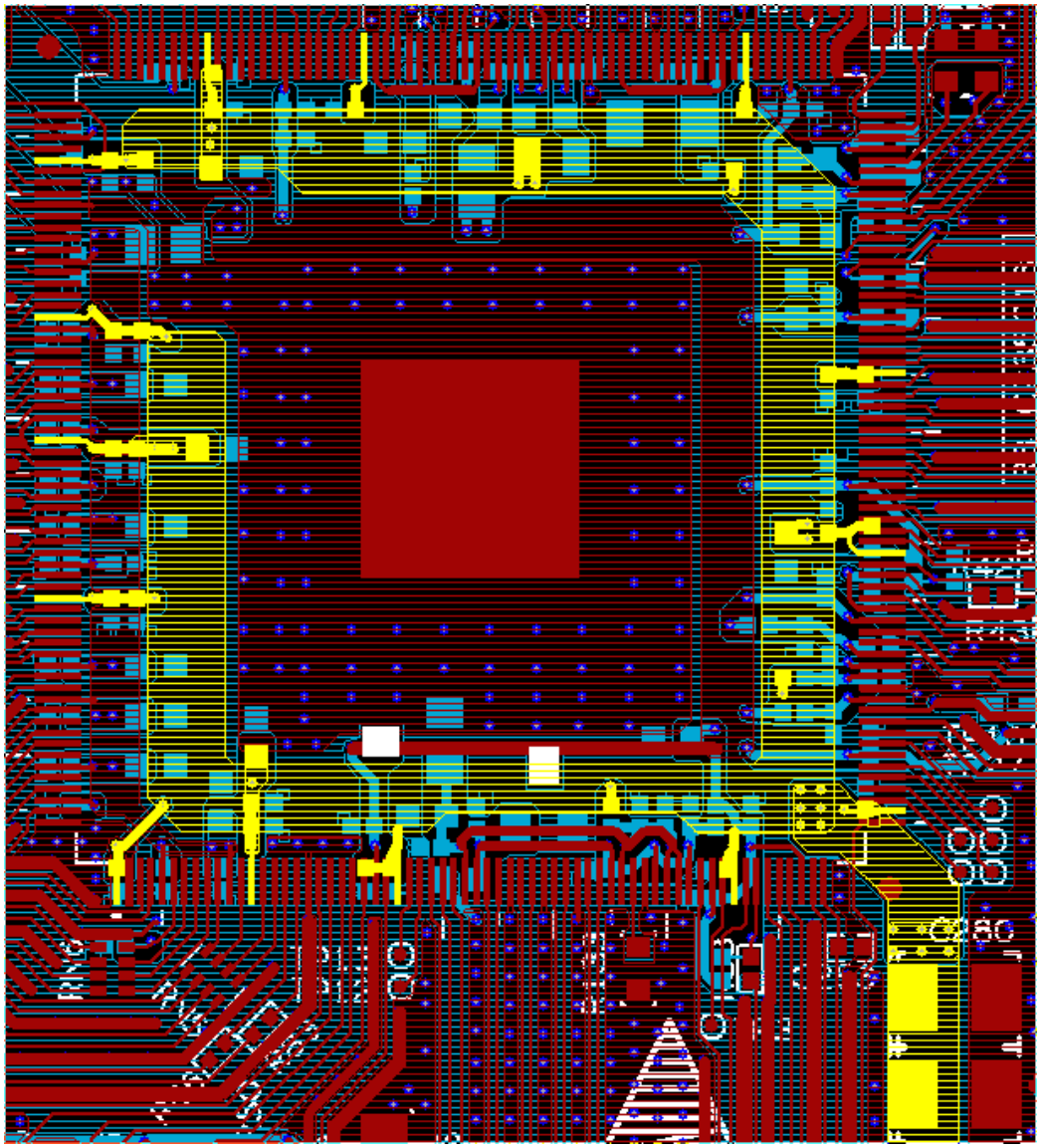
Figure 2-7 Number and type of filtering capacitors for the core power supply



Routing Mode and Filtering Capacitor Layout

The routing mode and filtering capacitor layout for the core power supply must be the same as those on the Hi3520D demo board. Figure 2-8 shows the core power supply design.

Figure 2-8 Core power supply design

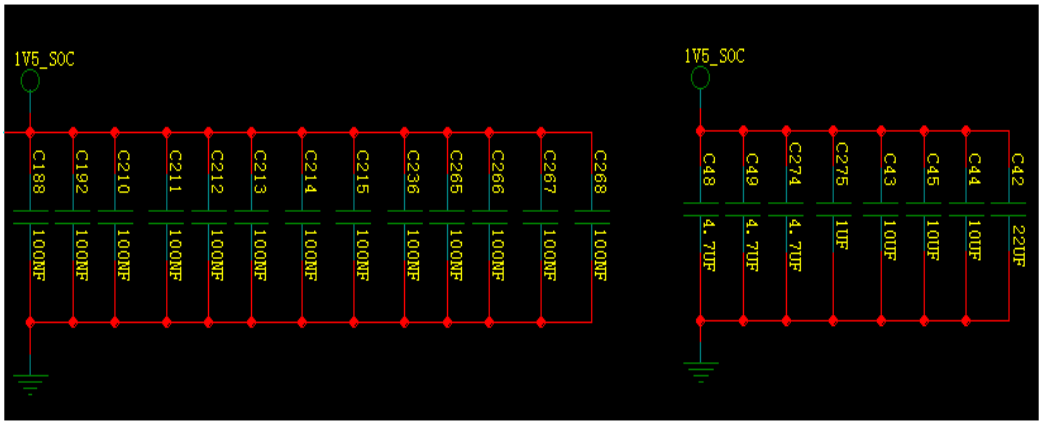


2.2.2 DDR 1.5 V Power Supply

Type and Number of Filtering Capacitors

The type and number of filtering capacitors for the DDR 1.5 V power supply must be the same as those on the Hi3520D demo board. For details, see the schematic diagram of the Hi3520D demo board. Figure 2-9 shows the number and type of filtering capacitors for the DDR 1.5 V power supply.

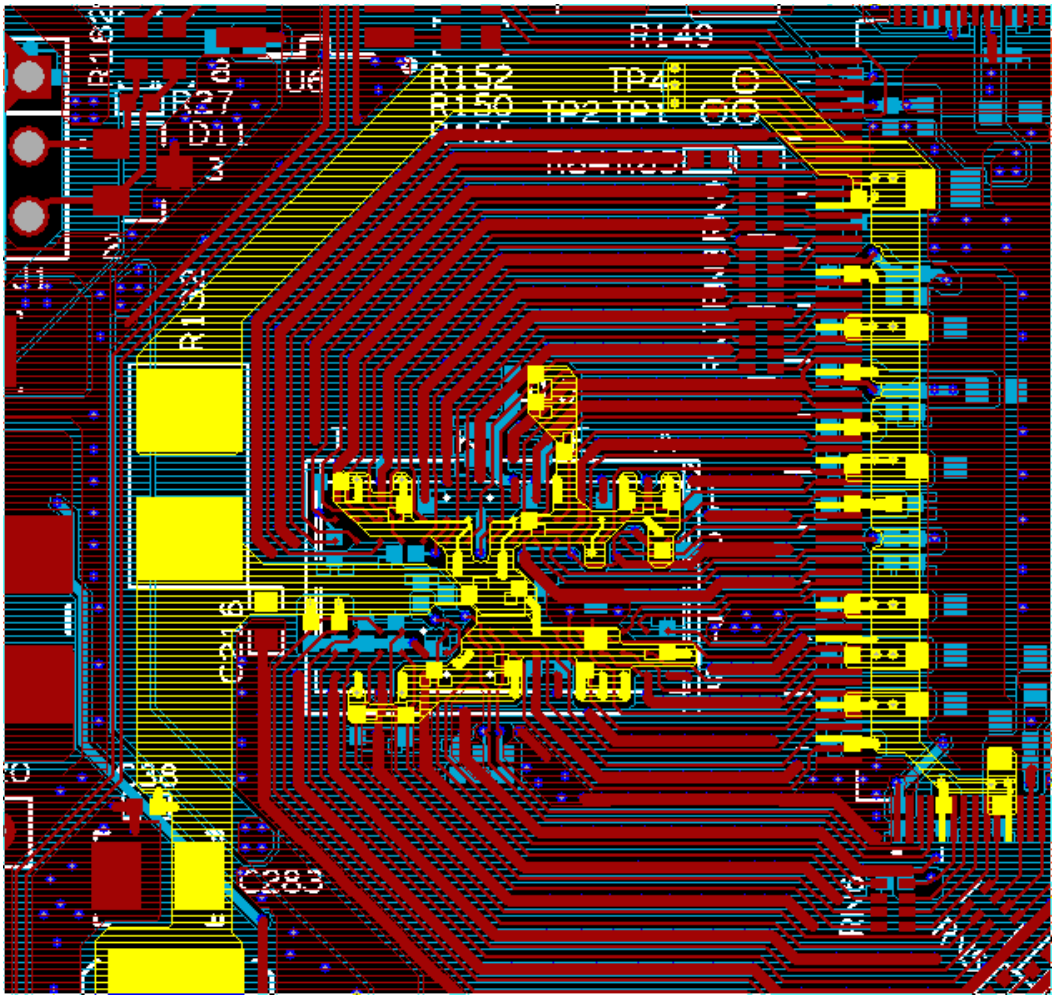
Figure 2-9 Number and type of filtering capacitors for the DDR 1.5 V power supply



Routing Mode and Filtering Capacitor Layout

The routing mode and filtering capacitor layout for the DDR 1.5 V power supply must be the same as those on the Hi3520D demo board. Figure 2-10 shows the DDR 1.5 V power supply design.

Figure 2-10 DDR 1.5 V power supply design

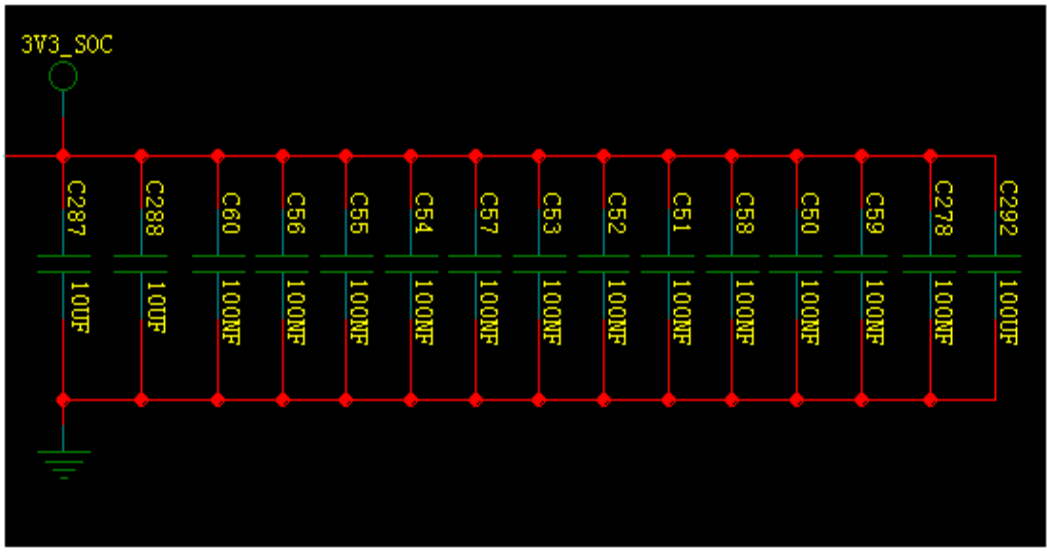


2.2.3 I/O 3.3 V Power Supply

Type and Number of Filtering Capacitors

The type and number of filtering capacitors for the I/O 3.3 V power supply must be the same as those on the Hi3520D demo board. For details, see the schematic diagram of the Hi3520D demo board. Figure 2-11 shows the number and type of filtering capacitors for the I/O 3.3 V power supply.

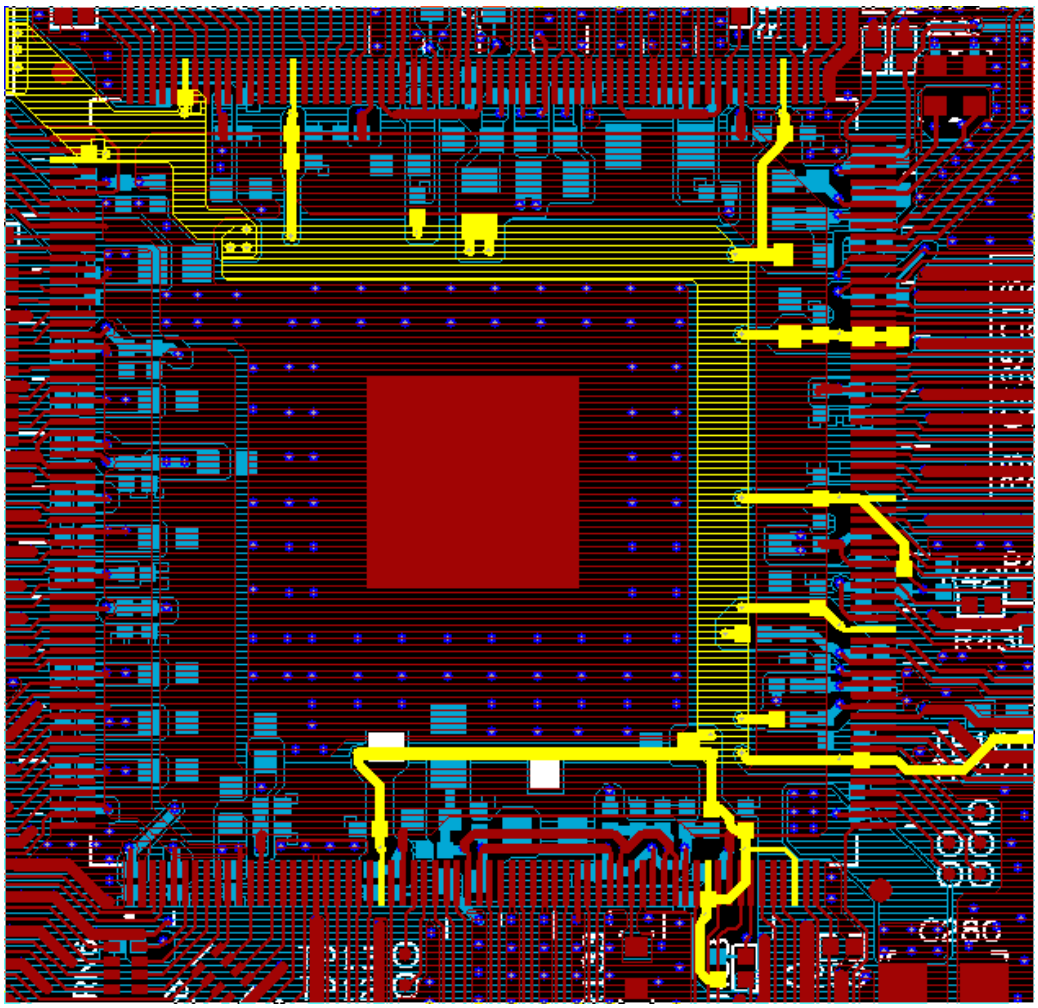
Figure 2-11 Number and type of filtering capacitors for the I/O 3.3 V power supply



Routing Mode and Filtering Capacitor Layout

The routing mode and filtering capacitor layout for the I/O 3.3 V power supply must be the same as those on the Hi3520D demo board. Figure 2-12 shows the I/O 3.3 V power supply design.

Figure 2-12 I/O 3.3 V power supply design



2.3 Design Requirements on DDR2 or DDR3 SDRAM Interface Routing

The design of the DDR SDRAM interface on the Hi3520D must be the same as that on the Hi3520D demo board. The items to be designed include the trace width, trace spacing, the spacing between a trace and GND, trace length, surrounding with GND traces, filtering capacitor position, and matching mode.

2.4 Design Requirements on Network Port Routing

2.4.1 External RMII Routing

You are advised to route external RMII signals on the PCB based on the following requirements to reduce signal crosstalk:

- Two signal traces must be surrounded with a GND trace and a clock trace must be surrounded with a GND trace to ensure complete signal return paths.
- Determine the signal trace length based on the clock trace length, and ensure that the length deviation is ±200 mils.
- Ensure that the GND under the transformer chip is void.
- The length deviation between the network port differential traces must fall within 5 mils, and the differential impedance must be 100 Ω±10%. For details about impedance control modes, see section 2.1.1 "Impedance Control."

2.4.2 Embedded FE PHY Routing

- Take antistatic and anti-surge measures on the board to prevent the Hi3520D from being damaged by the network cable ESD or surge.
- The length deviation between the network port differential traces must fall within 5 mils, and the differential impedance must be 100 Ω±10%. For details about impedance control modes, see section 2.1.1 "Impedance Control."
- Route the network port differential traces as an arc in a corner and surround the traces with GND traces.
- Ensure that the GND under the transformer chip is void.

2.5 Design Requirements on USB Interface Routing

To ensure good signal quality, route the data lines of the USB 2.0 host port in differential mode. To match the 480 Mbit/s USB 2.0 port, you are advised to route USB traces on the PCB based on the following guidelines:

- The differential data traces must be short and straight, and the internal differential traces must have the same length. It is recommended that the length deviation fall within 5 mils.
- The differential impedance must be 90 Ω±10%. For details about impedance control modes, see section 2.1.1 "Impedance Control."
- Route the network port differential traces as an arc in a corner and surround the traces with GND traces.
- The length of USB traces must be less than 5 inches.

2.6 Design Requirements on SATA Interface Routing

The Hi3520D/Hi3515A provides two SATA interfaces, whereas the Hi3515C supports only one SATA interface (SATA0). The routing recommendations are as follows:

- The differential impedance must be 100 Ω±10%. For details about impedance control modes, see section 2.1.1 "Impedance Control."
- Route the SATA differential traces as an arc in a corner and surround the traces with GND traces.
- The 10 nF multilayer ceramic capacitor connected to the differential signal lines in series must be placed close to the SATA connector.
- It is recommended that the length deviation for each pair of differential signal traces fall within 5 mils.

- The length of the SATA differential traces must be less than 3 inches.

2.7 Design Requirements on HDMI Routing

The Hi3520D has an HDMI interface, which can output HDMI signals directly. The routing recommendations are as follows:

- The differential impedance of the four pairs of HDMI differential signal traces must be 100 Ω±10%. For details about impedance control modes, see section 2.1.1 "Impedance Control."
- ESD components must be placed close to the HDMI connector.
- Route the HDMI differential traces as an arc in a corner and surround the traces with GND traces.
- The length deviation for each pair of differential signal traces must fall within 5 mils, and the length deviation between each pair of differential signal traces must fall within 50 mils.
- The length of the HDMI differential traces must be less than 5 inches.

2.8 Design Requirements on VI Interface Routing

The Hi3520D has two BT.656 input interfaces that can be combined into a BT.1120 interface. The routing recommendations are as follows:

- The VI data signal traces must be routed based on the CLK signal trace. It is recommended that the length deviation fall within 200 mils.
- The VIU0_CLK and VIU1_CLK traces must be surrounded with separate GND traces. It is recommended that four data signal traces are surrounded with a GND trace. It is optimal if every two data signal traces are surrounded with a GND trace.
- The VI_ADC_CLK trace must be surrounded with a separate GND trace.
- The VI line sequence can be adjusted based on the actual AD line sequence. For details, see section 1.2.11 "Analog VDAC Interface."

2.9 Design Requirements on VDAC Interface Routing

The Hi3520D has two VDAC interfaces that support one VGA output and two CVBS outputs. The routing recommendations are as follows:

- External configuration resistors and configuration capacitors must be placed close to the Hi3520D.
- The analog output signal traces (such as CVBS0, CVBS1, VGA_R, VGA_G and VGA_B) must be surrounded with GND traces.
- At most one via can be punched.

2.10 Design Recommendations on PCB Signal Integrity Simulation

By using board-level simulation tools, PCB designers can simulate signals and analyze signal integrity based on the input/output buffer information specification (IBIS) models of the Hi3520D interfaces, IBIS models of components, transmission line models, and board topologies.

Based on the simulation results, the PCB designers can adjust the typologies to meet the signal quality requirements, such as the requirements for overshoot, undershoot, ringtone, and monotonicity.

3 Recommendations for Board Thermal Design

3.1 Operating Condition

For details about power supply parameters, temperature parameters, and thermal resistance parameters, see section 2.6 "Electrical Specifications" in the *Hi3520D/Hi3515A/Hi3515C H.264 CODEC Processor Data Sheet*.

3.2 Reference Design for Heat Dissipation

The thermal resistance of heat sinks must meet the following condition:

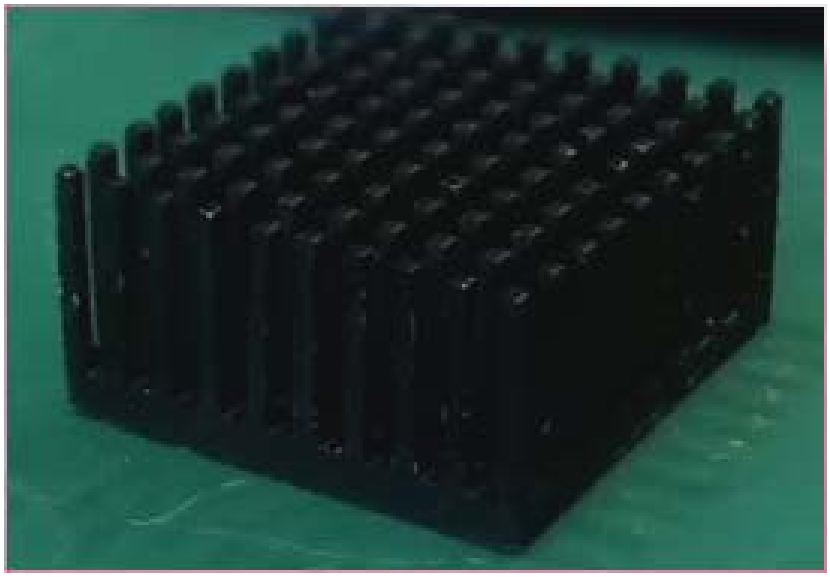
$$\theta_{sa} < (T_{j\_max} - T_a)/P - \theta_{jc} - \theta_{cs}$$

where

- T_{j_max} is the maximum junction temperature of a component.
- P is power consumption.
- T_a is the maximum ambient temperature.
- θ_{jc} is the junction-to-case thermal resistance of a component.
- θ_{cs} is the thermal resistance between a component and a heat sink.

For the Hi3520D, the heat sink with the dimensions of 31 mm x 31 mm x 16 mm (1.22 in. x 1.22 in. x 0.63 in.) or larger is recommended. The dimensions of the heat sink fin are 1.0 mm x 1.5 mm x 13 mm (0.04 in. x 0.06 in. x 0.51 in.). You are advised to paint the heat sink surface black. Ensure that the chip surface temperature is always lower than 100ºC (212ºF) by taking heat dissipation measures. Apply thermally conductive silicone to the contact surface between the heat sink and the Hi3520D. Install insulation gaskets as required. See Figure 3-1.

Figure 3-1 Heat sink



NOTE

The preceding specifications are for reference only. You need to select heat sinks based on the board design.

3.3 Reference Thermal Design for Circuits

3.3.1 Schematic Diagram

Power Supplies

Ensure that the efficiency of the board power tree is the highest as long as the power supplies are stable. To this end, design the board power supplies optimally and use fewer LDO components with large voltage difference to reduce heat produced during power conversion.

Low-Power Configurations for Idle Modules

Modules such as the USB and SATA modules may not be used in an actual application. If so, set these modules to power-down mode or default mode.

CAUTION

Enable clock gating for the Hi3520D to reduce power consumption.

3.3.2 PCB

Component Layout

Lay out components based on the product architecture and thermal design as follows:

- Place components that consume much power and generate much heat in a distributed manner to avoid local overheating and ensure the reliability and efficiency of components. In addition, you are advised to place the Hi3520D away from power supplies.
- Design an optimal product architecture to ensure that heat produced internally can be dissipated.
- If a chip has an exposed pad at the top layer of the PCB, the copper at the bottom layer should be exposed as well, which is good for heat dissipation.

Routing

The routing recommendations are as follows:

- For the connection style of vias under the Hi3520D, select the full connection style but not the thermal connection style to improve the board heat dissipation efficiency.
- Connect the GND signals and 1.25 V, 1.5 V or 1.8 V, and 3.3 V power signals over copper planes. When the signal over-current performance is ensured, you are advised to punch more vias and then connect these vias to the copper planes.
- Increase the size of copper planes under and around components that produce much heat to ensure that PCB heat can be effectively dissipated. Place inductors and power chips in a distributed manner and increase the size of copper planes around them.