1 Differences

1.1 Differences Among Specifications

Table 1-1 describes the differences among the specifications of the Hi3520D, Hi3515A, Hi3515C, and Hi3520A.

Table 1-1 Differences among the specifications of the Hi3520D, Hi3515A, Hi3515C, and Hi3520A

Item	Hi3520D	Hi3515A	Hi3515C	Hi3520A
Physical specifications	• Package type: EPAD-LQFP256 • Body size: 28 mm x 28 mm (1.10 in. x 1.10 in.) • Lead pitch: 0.4 mm (0.02 in.) • Operating voltage: 1.25 V/1.5 V/3.3 V. The 2.5 V power is not required. • Power consumption: 2.5 W typical power consumption. The core power is 2 A DC/DC.	• Package type: EPAD-LQFP256 • Body size: 28 mm x 28 mm (1.10 in. x 1.10 in.) • Lead pitch: 0.4 mm (0.02 in.) • Operating voltage: 1.25 V/1.5 V/3.3 V. The 2.5 V power is not required. • Power consumption: 2.5 W typical power consumption. The core power is 2 A DC/DC.	• Package type: EPAD-LQFP256 • Body size: 28 mm x 28 mm (1.10 in. x 1.10 in.) • Lead pitch: 0.4 mm (0.02 in.) • Operating voltage: 1.25 V/1.5 V/3.3 V. The 2.5 V power is not required. Power consumption: 2.5 W typical power consumption. The core power is 2 A DC/DC.	• Package type: EHS-FCBGA449 • Body size: 19 mm x 19 mm (0.75 in. x 0.75 in.) • Ball pitch: 0. 8 mm (0.03 in.) in the core area and 0.65 mm (0.026 in.) in other areas • Operating voltage: 1.0 V/1.5 V/2.5 V/3.3 V • Power consumption: 3.5 W typical power consumption. The core power is 4 A DC/DC.

Item	Hi3520D	Hi3515A	Hi3515C	Hi3520A
New specifications	• 2-layer printed circuit board (PCB) • Real-time clock (RTC) supporting an independent power supply system • Output video AD clock • Audio CODEC clock. The external clock chip is not required.	• 2-layer PCB • RTC supporting an independent power supply system • Output video AD clock • Audio CODEC clock. The external clock chip is not required.	• 2-layer PCB • RTC supporting an independent power supply system • Output video AD clock Audio CODEC clock. The external clock chip is not required.	2-layer PCB (not supported)
Processor	ARM Cortex A9@Max. 660 MHz 128 KB L2 cache	ARM Cortex A9@Max. 600 MHz 128 KB L2 cache	ARM Cortex A9@Max. 600 MHz 128 KB L2 cache	ARM Cortex A9@Max. 930 MHz 256 KB L2 cache
H.264 encoding/decoding performance	4xD1+4xCIF encoding+4xD1 decoding 8xCIF encoding+8xD1 decoding	4xD1+4xCIF encoding+1xD1 decoding	4xD1+4xCIF encoding+1xD1 decoding	4xD1+4xCIF encoding+4xD1 decoding
	4x960H+4xCIF encoding+1x960H decoding	4x960H@20fps +4xCIF@20fps encoding+1x960H @20 fps decoding	4x960H@20fps +4xCIF@20fps encoding+1x960H @20 fps decoding	4x960H+4xCIF encoding+1x960H decoding
	8xCIF encoding +8xCIF decoding	Not supported	Not supported	8xCIF encoding +8xCIF decoding
	16xCIF encoding +16xCIF decoding	Not supported	Not supported	16xCIF encoding +16xCIF decoding
	8xD1 decoding	4xD1 decoding	4xD1 decoding	8xD1 decoding
	4x720p decoding	2x720p decoding	2x720p decoding	4x720p decoding
	2x1080p decoding	1x1080p decoding	1x1080p decoding	2x1080p decoding
Limitation on H.264 encoding/decoding APIs	• At most 64 encoding channels • At most 64 D1 encoding channels • At most 64 decoding channels	• At most eight encoding channels • At most four D1 encoding channels • At most four decoding channels	• At most eight encoding channels • At most four D1 encoding channels • At most four decoding channels	• At most 72 encoding channels • At most 72 D1 encoding channels • At most 64 decoding channels

Item	Hi3520D	Hi3515A	Hi3515C	Hi3520A
Video input (VI)	• Two VI devices • Configurable VI data line sequences (The traces cannot cross when the ADCs with various line sequences are connected. For details, see section 1.2.11 "VI Interface" in the *Hi3520D Hardware Design User Guide*.) • Luminance statistics	• One VI device. Only VIU0 is available, and the VIU1 pins are used as GPIO pin. • BT.1120 timing (not supported) • Luminance statistics	• One VI device. Only VIU0 is available, and the VIU1 pins are used as GPIO pin. • BT.1120 timing (not supported) • Lum	• Four VI devices • Configurable VI data line sequences (not supported) • Luminance statistics (not supported)
Video output (VO)	• Digital output interfaces such as BT656 and BT1120 (LCD) (not supported) • The picture in picture (PIP) is multiplexed with an SD video layer. Only the PIP with a single area is supported. • Scaling at the HD video layer. The maximum width of the input picture is 1440 pixels during enlargement. • Data source selection for HD data writeback. The data of the video layer or combined data of the video layer and graphics layer are selected for HD writeback.	• Digital output interfaces such as BT656 and BT1120 (LCD) (not supported) • The PIP is multiplexed with an SD video layer. Only the PIP with a single area is supported. • Scaling at the HD video layer. The maximum width of the input picture is 1440 pixels during enlargement. • Data source selection for HD data writeback. The data of the video layer or combined data of the video layer and graphics layer are selected for HD writeback.	• Digital output interfaces such as BT656 and BT1120 (LCD) (not supported) • The PIP is multiplexed with an SD video layer. Only the PIP with a single area is supported. • Scaling at the HD video layer. The maximum width of the input picture is 1440 pixels during enlargement. • Data source selection for HD data writeback. The data of the video layer or combined data of the video layer and graphics layer are selected for HD writeback.	• Digital output interfaces such as BT656 and BT1120 (LCD). • The PIP is multiplexed with an SD video layer. The PIP with multiple areas is supported. • Scaling at the HD video layer. The maximum width of the input picture is 1280 pixels during enlargement. • Data source selection for HD data writeback (not supported). Only combined data of video layer and graphics layer is supported.

Item	Hi3520D	Hi3515A	Hi3515C	Hi3520A
Video processing	• Sharpening and scaling for channel 0 • A maximum of 960-pixel image width during de-interlacing and pre-scaling • Optimized algorithms for denoising, de-interlacing, and sharpening, which improves the picture quality	• Sharpening and scaling for channel 0 • A maximum of 960-pixel image width during de-interlacing and pre-scaling • Optimized algorithms for denoising, de-interlacing, and sharpening, which improves the picture quality	• Sharpening and scaling for channel 0 • A maximum of 960-pixel image width during de-interlacing and pre-scaling • Optimized algorithms for denoising, de-interlacing, and sharpening, which improves the picture quality	• Sharpening and scaling for channel 0 (not supported) • There is no limit on the image width during de-interlacing and pre-scaling.
Video encoding/decoding	H.264 High Profile encoding	H.264 High Profile encoding	H.264 High Profile encoding	H.264 High Profile encoding (not supported)
Graphics	• ROP (not supported) • Mirror operation (not supported)	• ROP (not supported) • Mirror operation (not supported)	• ROP (not supported) • Mirror operation (not supported)	• ROP (supported) • Mirror operation (supported)
Audio	Two I^2S interfaces: one input interface (a maximum of 16 input channels) and one output interface	Two I^2S interfaces: one input interface (a maximum of 16 input channels) and one output interface	Two I^2S interfaces: one input interface (a maximum of 16 input channels) and one output interface	Three I^2S interfaces: two input interfaces (a maximum of 32 channels) and one input and output interface
Flash	SPI NOR flash	SPI NOR flash	SPI NOR flash	SPI NOR flash and NAND flash
DDR	• A maximum of 660 MHz frequency • A maximum of 512 MB capacity	• A maximum of 600 MHz frequency • A maximum of 512 MB capacity	• A maximum of 600 MHz frequency • A maximum of 512 MB capacity	• A maximum of 620 MHz frequency • A maximum of 512 MB capacity

Item	Hi3520D	Hi3515A	Hi3515C	Hi3520A
Ethernet port	• Full-duplex mode or half-duplex mode or at 10 Mbit/s or 100 Mbit/s; duplex mode at 1000 Mbit/s (not supported) • Embedded FE PHY; physical management data input (MDI) interface or MAC reduced media-independent interface (RMII)	• Full-duplex mode or half-duplex mode or at 10 Mbit/s or 100 Mbit/s; duplex mode at 1000 Mbit/s (not supported) • Embedded FE PHY; physical MDI interface or MAC RMII	• Full-duplex mode or half-duplex mode or at 10 Mbit/s or 100 Mbit/s; duplex mode at 1000 Mbit/s (not supported) • Embedded FE PHY; physical MDI interface or MAC RMII	• Full-duplex mode at 10 Mbit/s, 100 Mbit/s, or 1000 Mbit/s, or half-duplex mode at 10 Mbit/s or100 Mbit/s • RGMII or MII mode.
Peripheral interface	• One serial peripheral interface (SPI), supporting two CSs. • Two SATA 2.5 interfaces • No secure digital input/output (SDIO) interface	• One SPI, supporting two CSs. • Two SATA 2.5 interfaces • No SDIO interface	• One SPI, supporting two CSs. • One SATA 2.5 interface • No SDIO interface	• One SPI, supporting four CSs • One SDIO 2.0 interface, supporting a maximum of 32 GB capacity
Boot mode	System boots only from the BOOTRAM or SPI NOR flash.	System boots only from the BOOTRAM or SPI NOR flash.	System boots only from the BOOTRAM or SPI NOR flash.	System boots from the BOOTROM, SPI NOR flash, or NAND flash.
Chip ID	0b11	0b01	0b10	0b10

1.2 Differences Among the SDKs of the Hi3520D/Hi3515A/Hi3515C and the Hi3520A

The Hi3520D, Hi3515A, and Hi3515C use the same SDK and have the same interfaces.

Table 1-2 describes the differences among the SDKs of the Hi3520D/Hi3515A/Hi3515C and the Hi3520A.

Table 1-2 Differences among the SDKs of the Hi3520D/Hi3515A/Hi3515C and Hi3520A

Component	Hi3520D/Hi3515A/Hi3515C	Hi3520A
GCC	The same as the Hi3520A	gcc-4.4 compiler

Component	Hi3520D/Hi3515A/Hi3515C	Hi3520A
Linux	The common code of the Hi3520D Linux and Hi3520A Linux is the same. However, the chip configurations of the Hi3520D and the Hi3520A are different. The source code of the Hi3520D and Hi3515A/Hi3515C is the same.	Linux-3.0.y, supporting single-core Cortex A9
U-boot	The common code of the Hi3520D U-boot and Hi3520A U-boot is the same. However, the chip configurations of the Hi3520D and the Hi3520A are different. The source code of the Hi3520D and Hi3515A/Hi3515C is the same, but their configuration sheets are different.	
Driver	The same as the Hi3520A	
MPP	The Hi3520D and Hi3520A APIs are the same. However, some APIs are restricted. For details, see Table 1-3.	

Table 1-3 describes the API differences between the Hi3520D/Hi3515A/Hi3515C and Hi3520A by module. For details, see the *HiMPP Media Processing Software Development Reference*.

Table 1-3 Differences of MPIs between the Hi3520D/Hi3515A/Hi3515C and Hi3520A by module

Module	Change Extent of the Hi3520D/Hi3515A/Hi3515C Compared with the Hi3520A	Description
System control	Same	None
I/O bind	Same	None
Video input	Slight different	An MPI for supporting data input in reverse sequence is added for the Hi3520D/Hi3515A/Hi3515C. The Hi3515A/Hi3515C does not support the BT.1120 timing.
VO	Slight different	An MPI for supporting data source selection for HD data writeback is added for the Hi3520D/Hi3515A/Hi3515C.
Video pre-processing (VPP)	Same	None
On-screen display (OSD) overlay	Same	None

Module	Change Extent of the Hi3520D/Hi3515A/Hi3515C Compared with the Hi3520A	Description
Video encoding	Slight different	An MPI for specifying the number of encoding video frames is added for the Hi3520D/Hi3515A/Hi3515C. There are limitations on Hi3515A/Hi3515C encoding channels.
Video decoding	Slight different	There are limitations on Hi3515A/Hi3515C encoding channels.
Motion detection (MD)	Same	None
Intelligent video engine (IVE)	Same	None
Audio	Same	None
Frame buffer (FB)	Same	None
2D acceleration module	Same	None

1.3 Difference Between OSs and Drivers

Table 1-4 describes differences between the OSs and drivers of the Hi3520D/Hi3515A/Hi3515C and Hi3520A.

Table 1-4 Differences between the OSs and drivers of the Hi3520D/Hi3515A/Hi3515C and Hi3520A

Item	Change Extent of the Hi3520D/Hi3515A/Hi3515C Compared with the Hi3520A
U-boot table	The source code related to the critical parts of the chip such as clocks is modified.
Kernel	The source code related to the critical parts of the chip such as clocks is modified.
Drivers such as Ethernet port driver	The source code related to the critical parts of the chip such as clocks is modified.
File system	None