

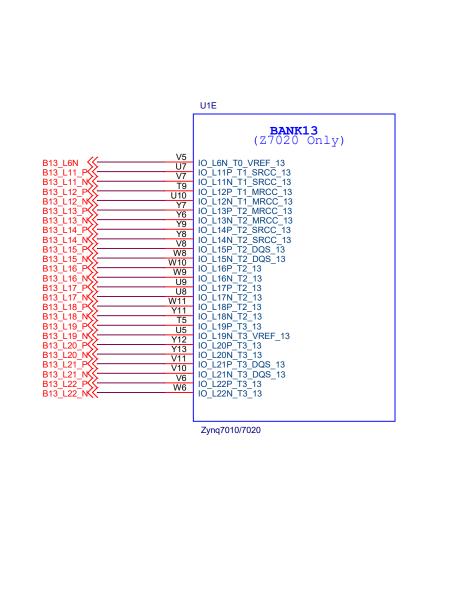
→ FPGA

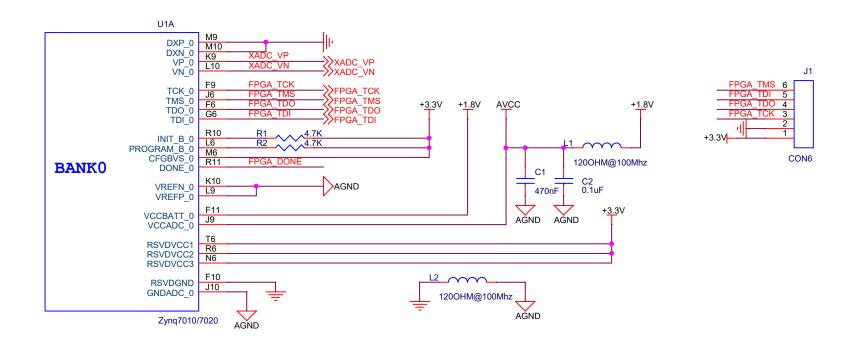
Flash/DDR

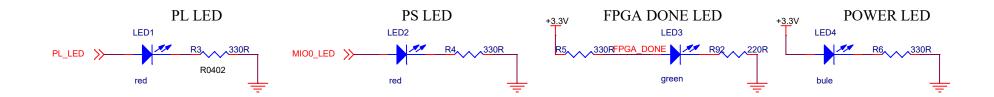
Connector

Others

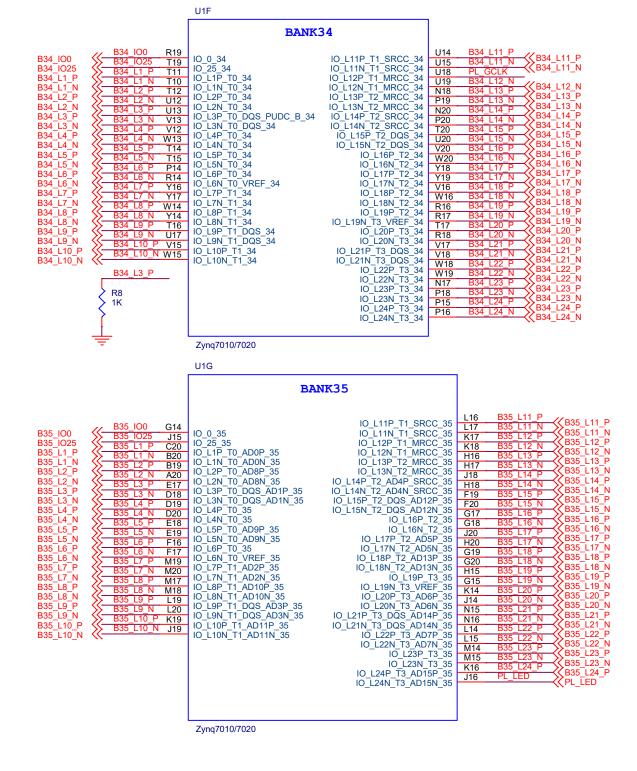
Design	Design Name ZYNQ-CORE							
Size A4	Page Name 01_Block Diagram		Rev 1.0					
Date:	Wednesday, September 08, 2021 Sheet 1 o	f '	11					

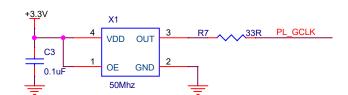


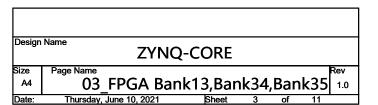


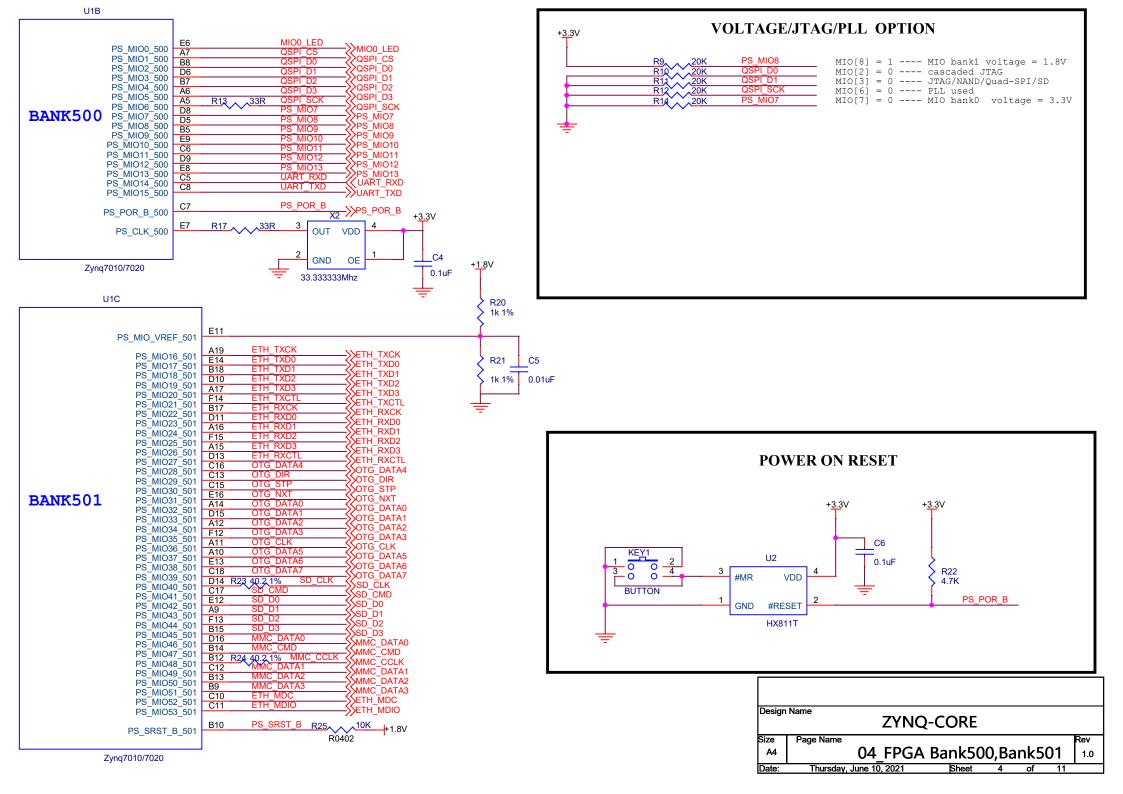


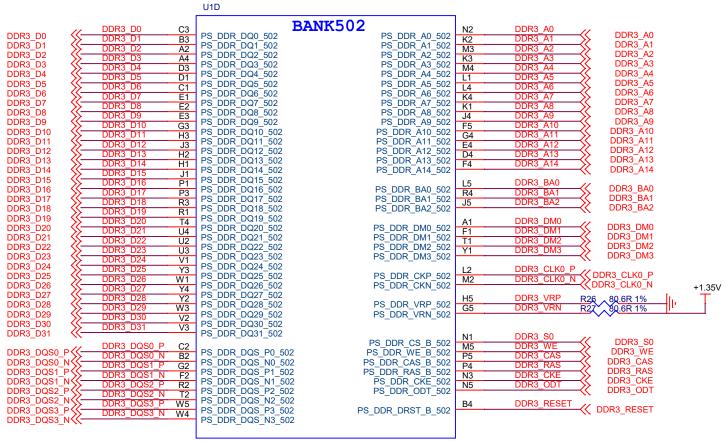
Design	Design Name ZYNQ-CORE								
Size A4	Page Name 02_FPGA Bank0 Rev 1.0								
Date:	Thursday, June 10, 2021 Sheet 2 of	11							



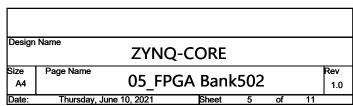


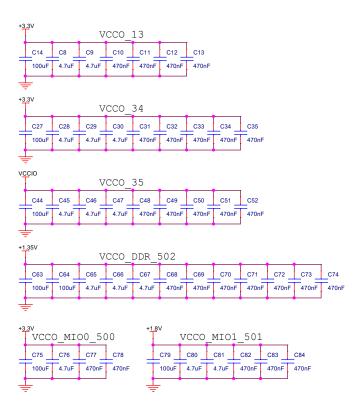


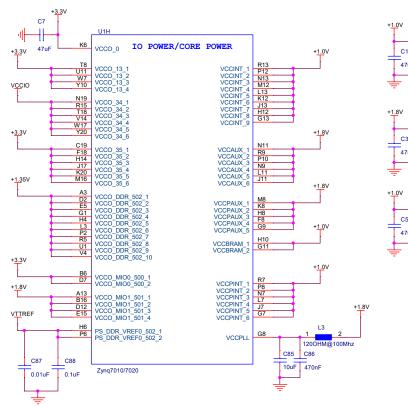


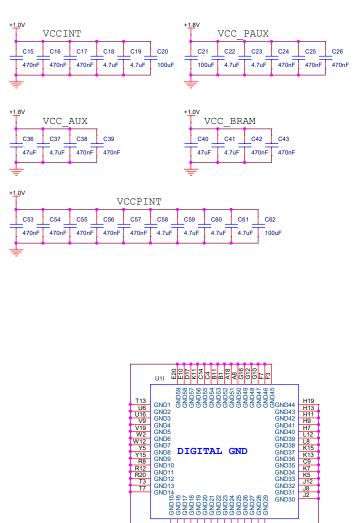


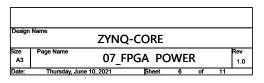
Zynq7010/7020



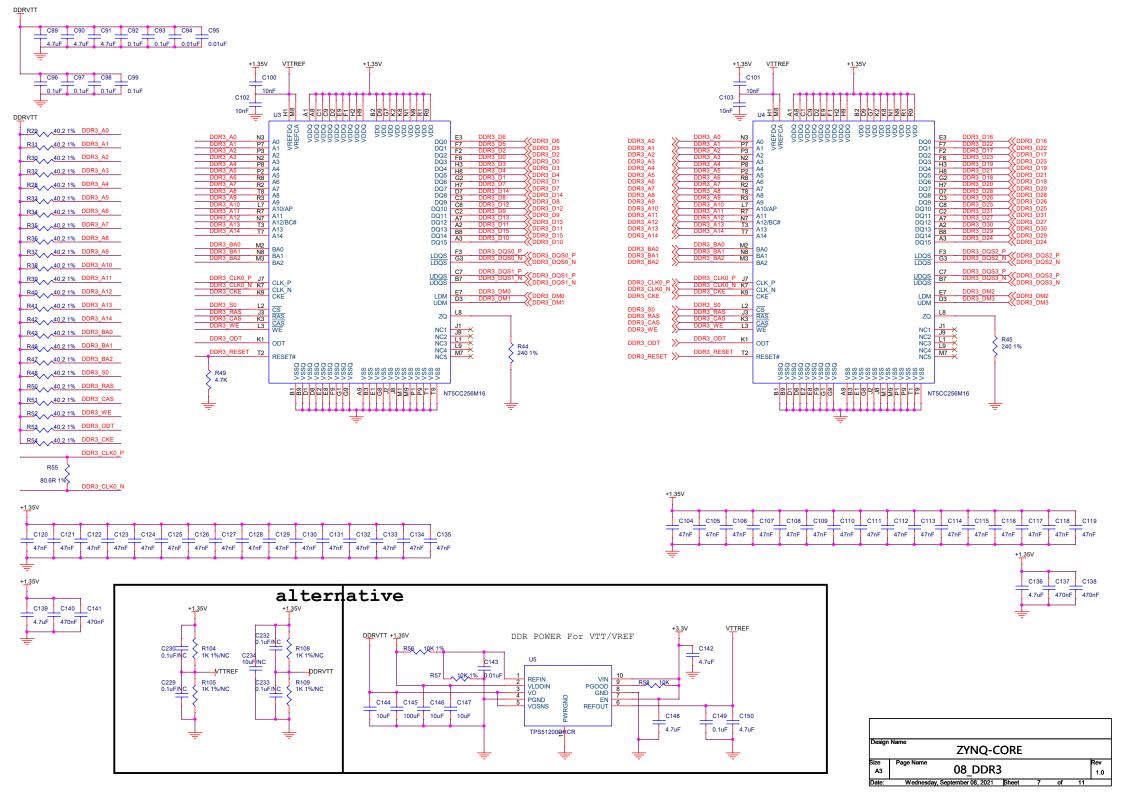


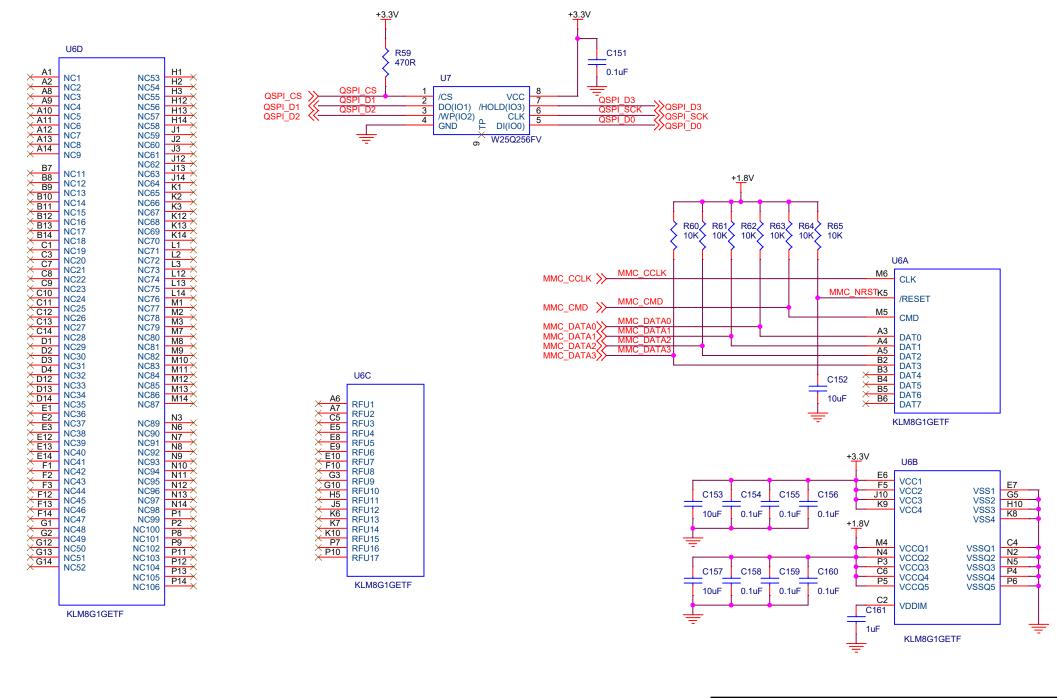




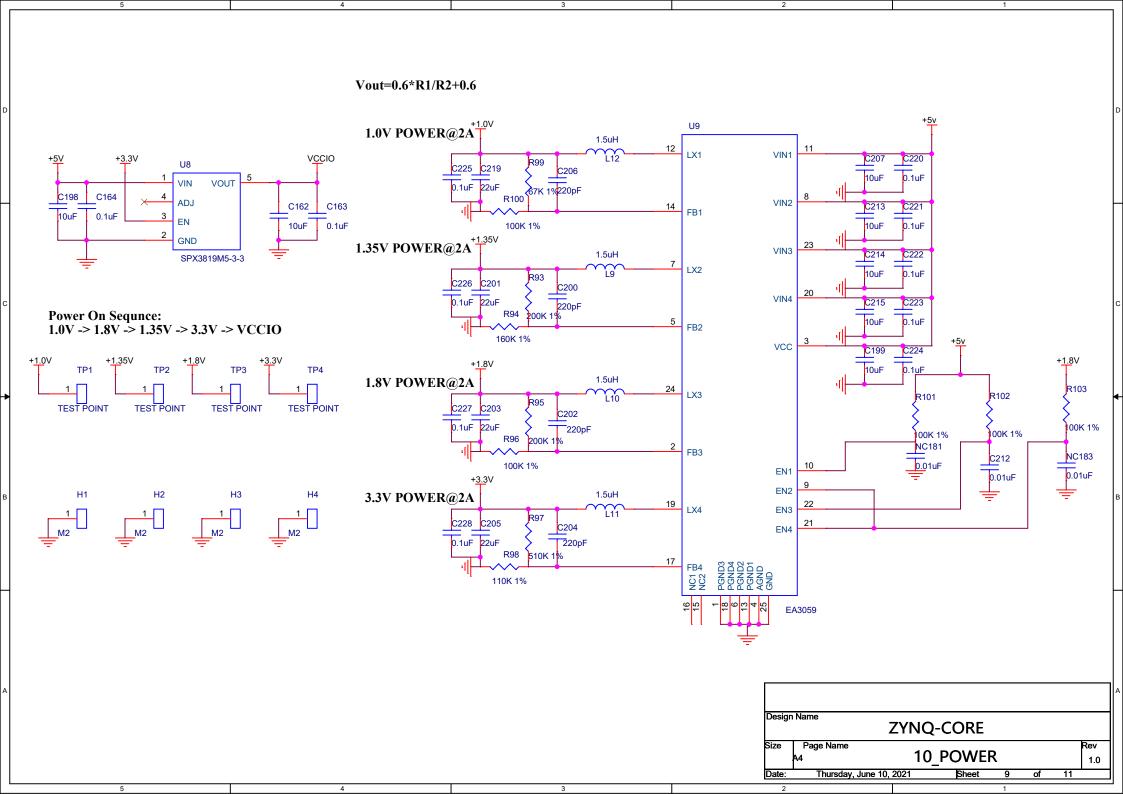


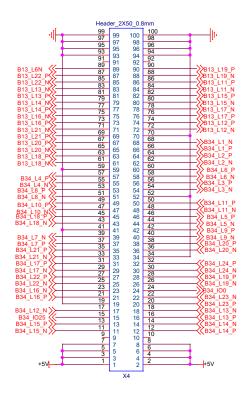
Zynq7010/7020





Design Name ZYNQ-CORE							
Size	Page Name						Rev
A4		09	_eMMC				1.0
Date:	Thursday, J	une 10, 2021	Sheet	8	of	11	





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FPGA TCK <<-	FPGA_TCK	99	99	100	100	FPGA_TMS	>>> FPGA TMS
EPGA TOO	FPGA_TDO	97	97	98	98	FPGA_TDI	FPGA TDI
PS MIOS X	PS_MIO8 PS_MIO13	95	95	96	96	PS_MIO9 PS_MIO11	PS MIO9
PS MIO13 <<─	PS_MIO10	93 91	93	94	94	PS_MIO7	PS MIO11
PS_MIO10 <<-	UART RXD	89	91	92	90	PS MIO12	PS_MIO7
UART_RXD <<	UART TXD	87	89	90	88	SD D3	PS_MIO12
UART_TXD >>	XADC VP	85	87	88	86	SD D2	—→>>> SD_D3
XADC_VP <	XADC_VN	83	85	86	84	SD_D1	
XADC_VN (QSPI_D2	81	83	84	82	SD_D0	+
QSPI_D2	QSPI_D3	79	81	82	80	SD_CLK	→ >>> SD_D0
QSPI_D3XX		77	79 77	80 78	78	SD_CMD	SD_CLK
OTG DATA3 <<	OTG_DATA3	75	75	76	76		→>>> SD_CMD
OTG DATAS	OTG_DATA6	73	73	74	74	OTG_DATA5	>>> OTG_DATA5
OTG CLK	OTG_CLK	71	71	72	72	OTG_DATA2	SOTG DATAS
OTG DIR ((-	OTG_DIR OTG_STP	69 67	69	70	70 68	OTG_DATA0 OTG_DATA1	OTG DATA0
OTG STP <	OTG NXT	65	67	68	66	OTG DATA1	OTG DATA1
OTG NXT <	OTG_NXT	63	65	66	64	OTG_DATA7	OTG DATA4
::		61	63	64	62	OTO_DATAI	OTG_DATA7
B35_L21_P >>-		59	61	62	60		
B35_L21_N >>		57	59	60	58		B35_L23_P
B35_L22_P		55	57	58	56		B35_L23_N
B35_L22_N		53	55	56	54		B35_L20_P
B35_L24_P		51	53	54	52		B35_L20_N B35_L11_P
B35_L6_P B35_L6_N		49	51 49	52 50	50		B35 L11 N
B35 L5 P		47	49	48	48		B35 IO25
B35_L5_N		45	45	46	46		B35_IO23
B35 T16 P		43	43	44	44		₩B35_L19_P
B35 I 16 N \$>		41 39	41	42	42 40	ETH1 TXC	₩ B35 L19 N
B35 8 P <<─		37	39	40	38	ETH1_TXD0	₩ B35_L13_P
B35_L8_N <<		35	37	38	36	ETH1 TXD1	B35_L13_N
B35_L9_N <<		33	35	36	34	ETH1 TXD2	→>>> B35_L2_N
B35_L9_P		31	33	34	32	ETH1 TXD3	→>>> B35_L2_P
D00_E/_1 \$\$		29	31	32	30	ETH1_TXCTL	→>>> B35_L3_P
B35_L7_N <<	HDMI_CLK_N	27	29	30	28	ETH1_RXC	B35_L3_N
B35_L14_N B35_L14_P	HDMI_CLK_P	25	27	28	26	ETH1_RXD0	B35 L12 P
B35 L18 N	HDMI_D2_N	23	25 23	26 24	24	ETH1_RXD1	B35_L12_N B35_L1 N
B35 L18 P	HDMI_D2_P	21	21	24	22	ETH1_RXD2	B35_L1_N B35_L1_P
B35_L10_N	HDMI_D1_N	19	19	20	20	ETH1_RXD3	→ S B35 L4 P
B35 L10 P	HDMI_D1_P	17	17	18	18	ETH1_RXCTL ETH1_MDIO	→S B35 L4 N
B35_L17_N >>	HDMI_D0_N HDMI_D0_P	15 13	15	16	16 14	ETH1_MDIO	₩ B35 L15 P
B35_L17_P >>-	HDIWII_DU_P		13	14	12	ETHT_MDC	B35_L15_N
	PHY MDI1 N	11 9	11	12	10	PHY MDI3 N	⊣ − −
PHY_MDI1_N <	PHY MDI1 P	7	9	10	8	PHY MDI3 P	>>> PHY_MDI3_N
PHY_MDI1_P <	PHY MDI0 N	5	7	8	6	PHY MDI2 N	PHY_MDI3_P
PHY_MDI0_N SS—	PHY_MDI0_P	3	5	6	4	PHY_MDI2_P	PHY_MDI2_N
PHY_MDI0_P	PHY_ADO/LED0	1	3	4	2	PHY_AD1/LED1	PHY_MDI2_P
PHY_AD0/LED0 >>			1	2			PHY_AD1/LED1
			>	(3			

Design	Design Name ZYNQ-CORE								
Size A3	Page Name 12_CONNECTOR Rev 1.0								
Date:	Thursday, Ju	ne 10, 2021	Sheet	10	of	11			

