

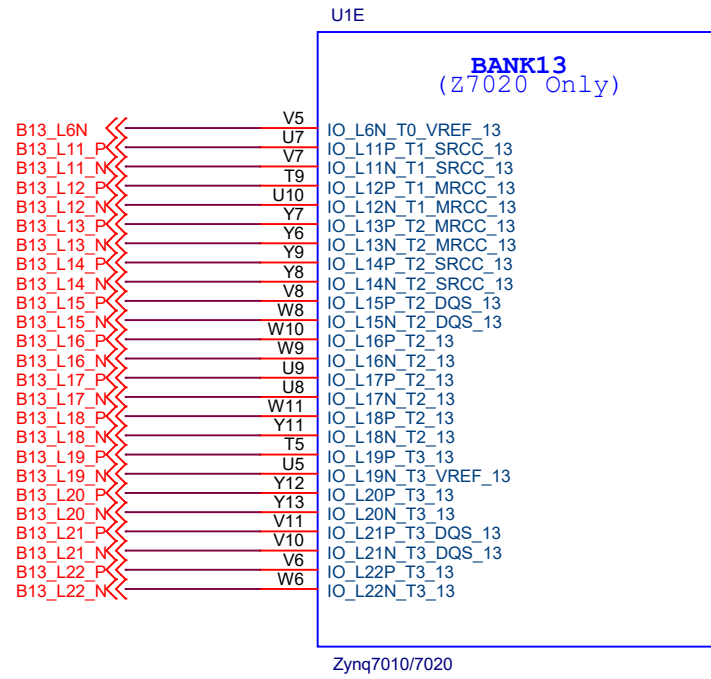
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A4	01_Block Diagram	1.0
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D

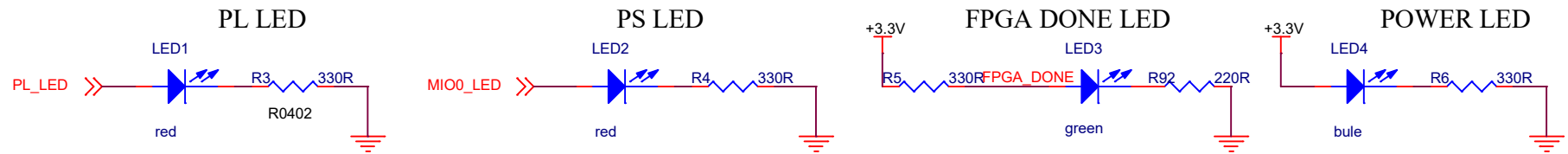
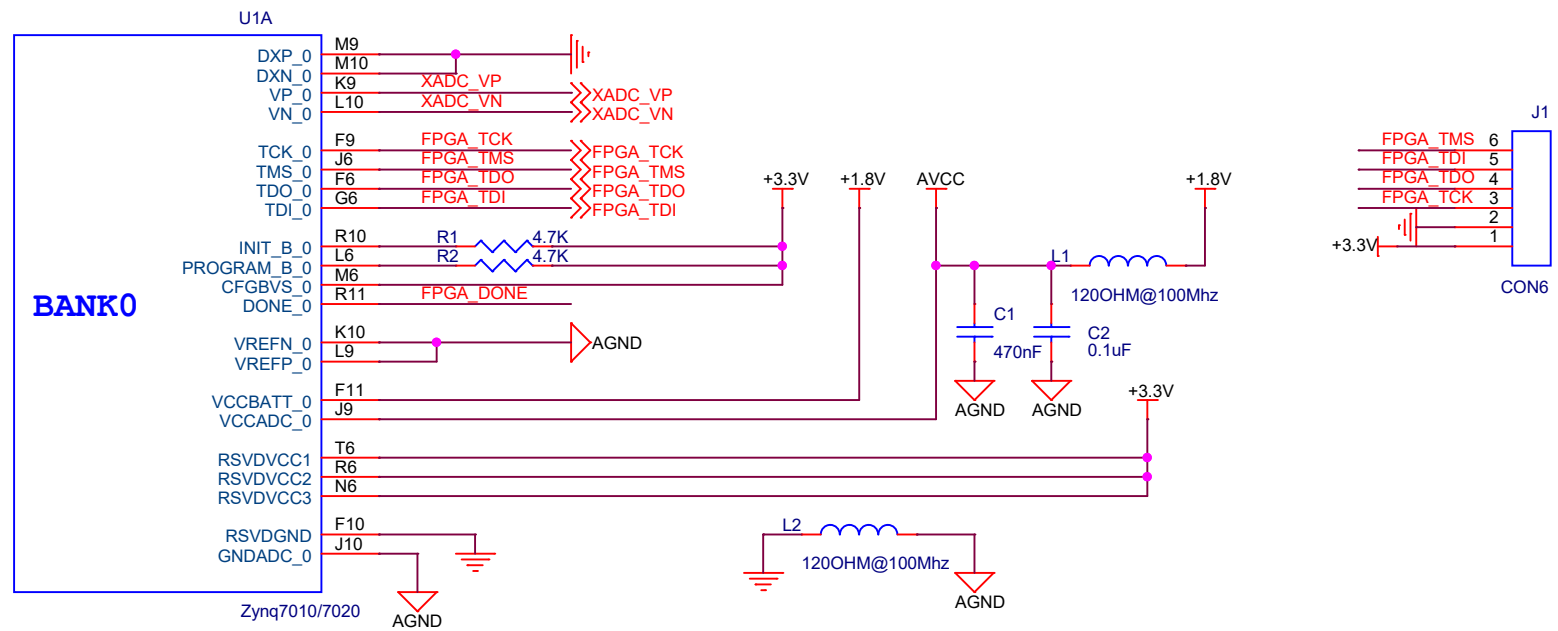
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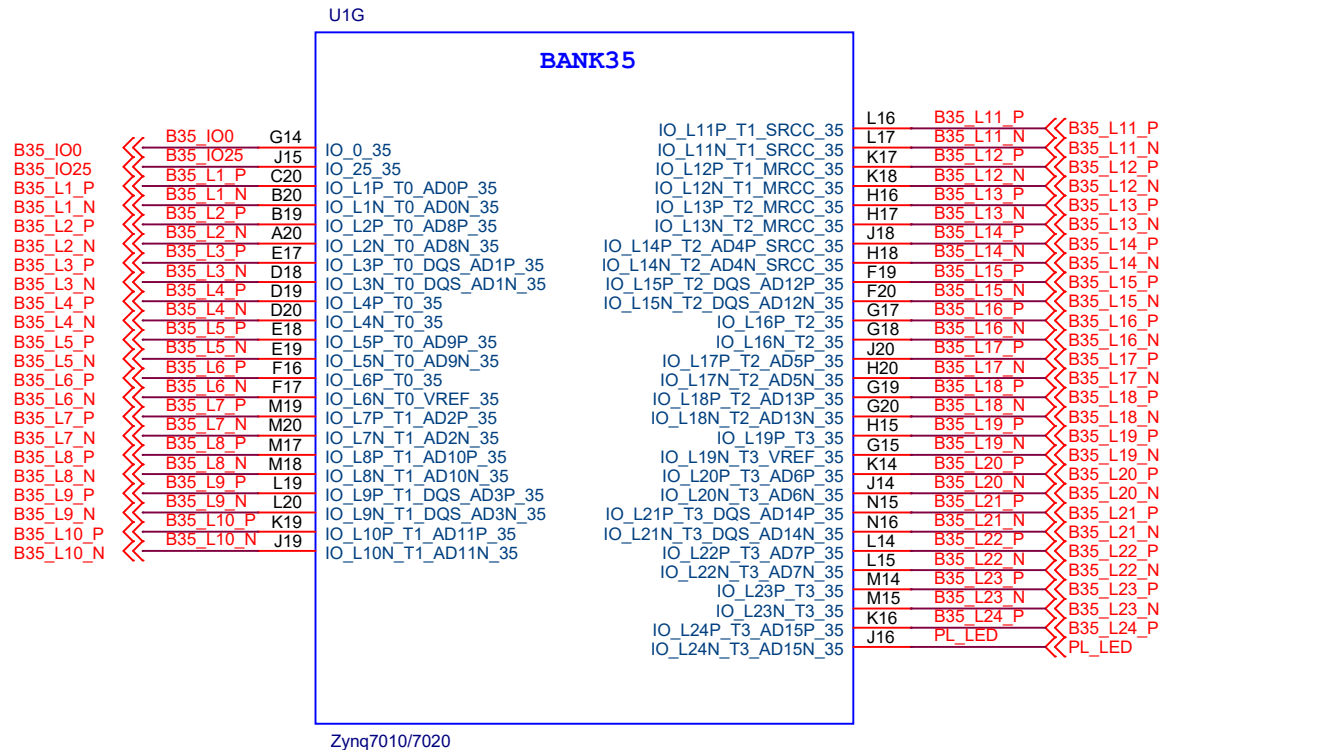
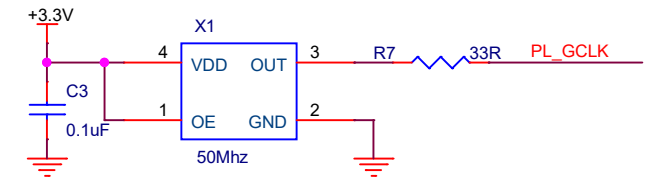
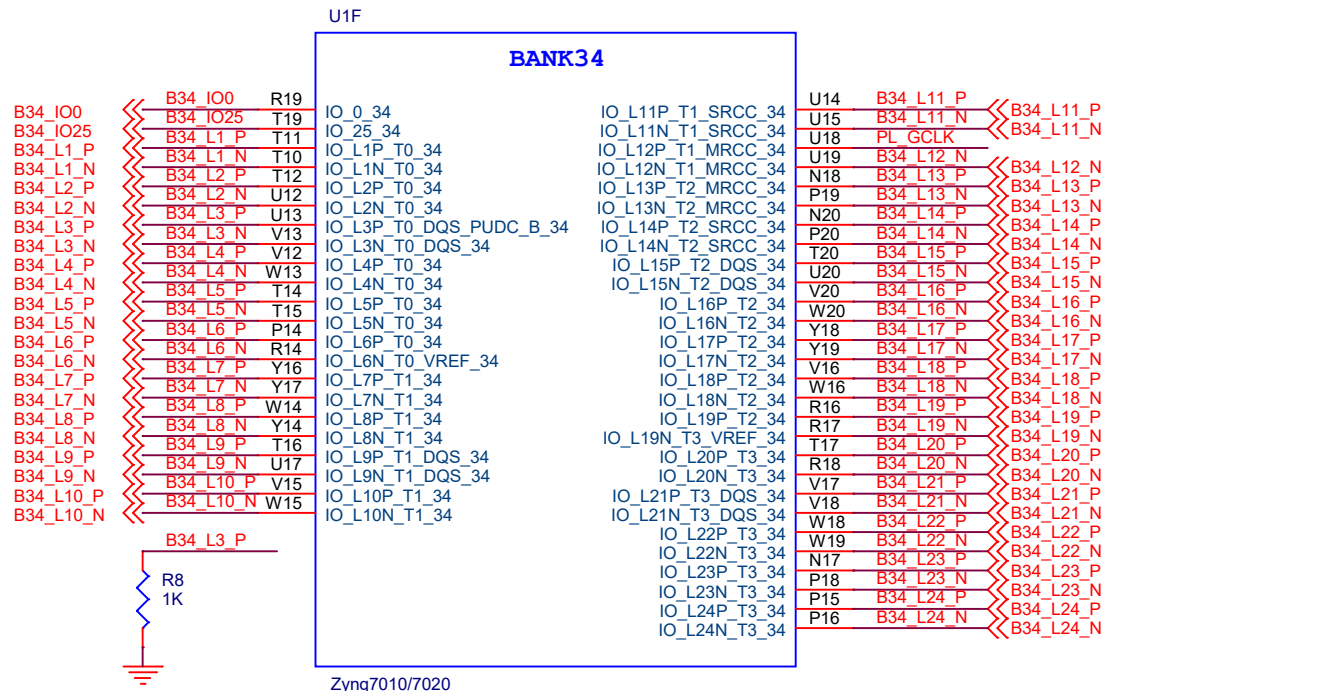
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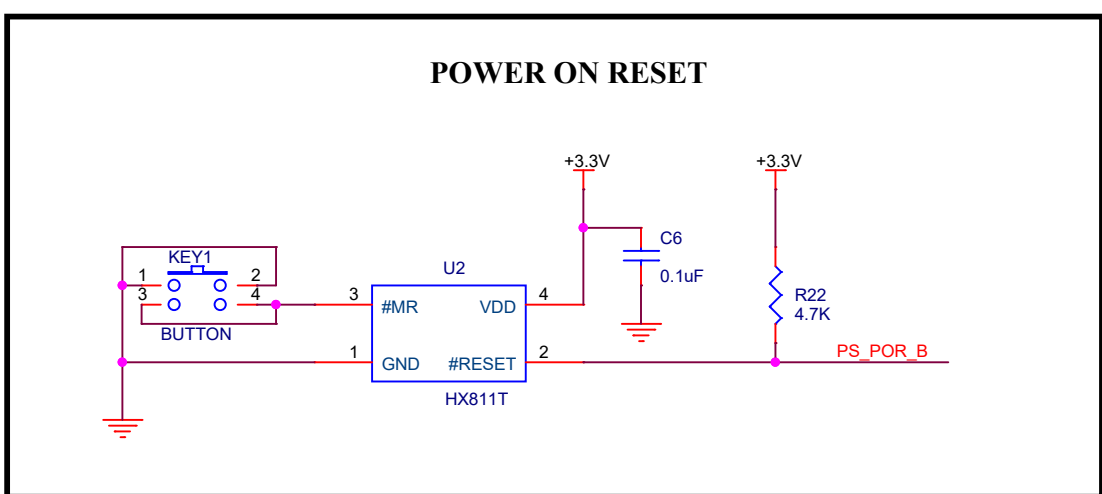
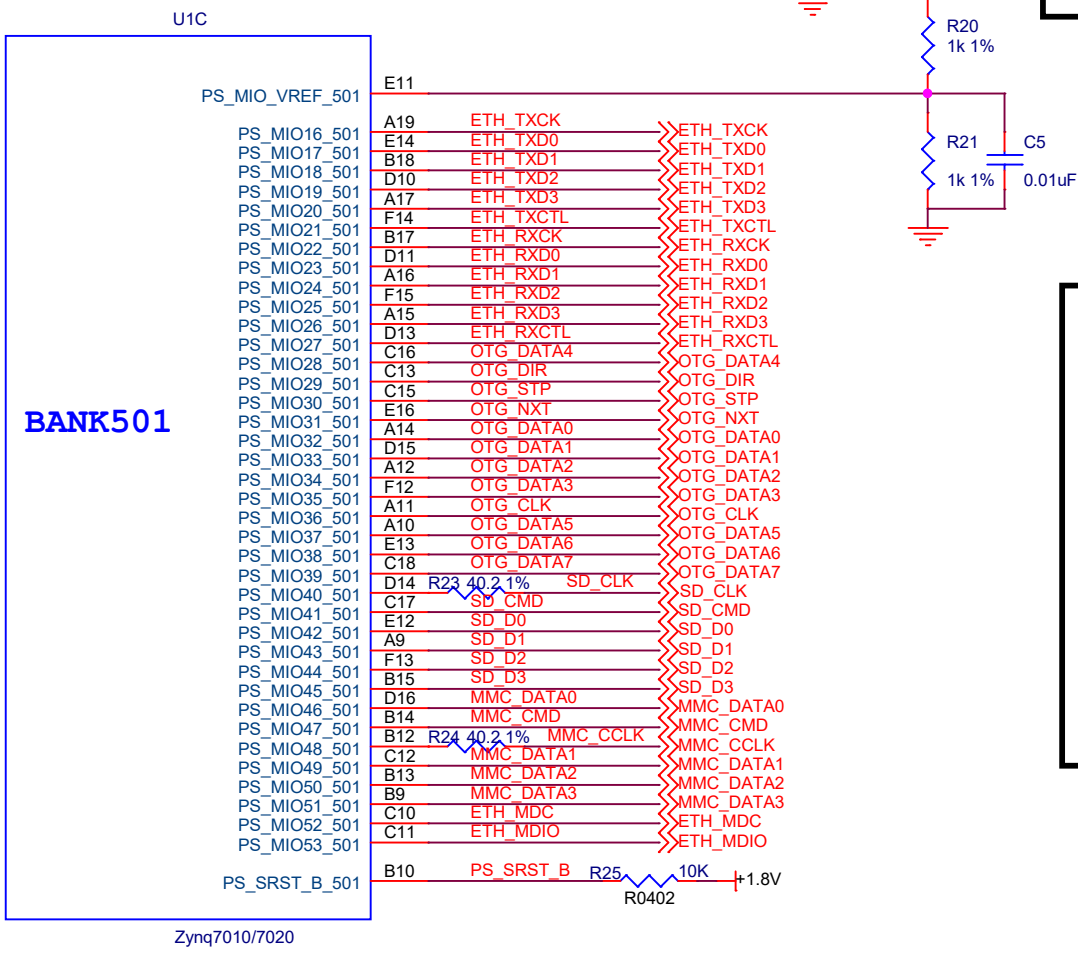
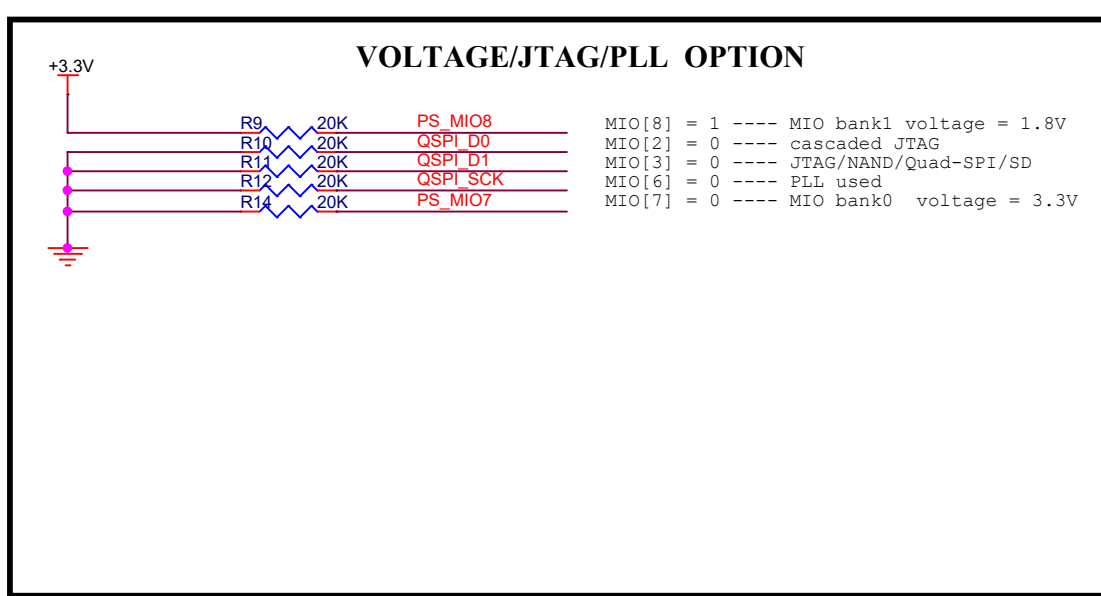
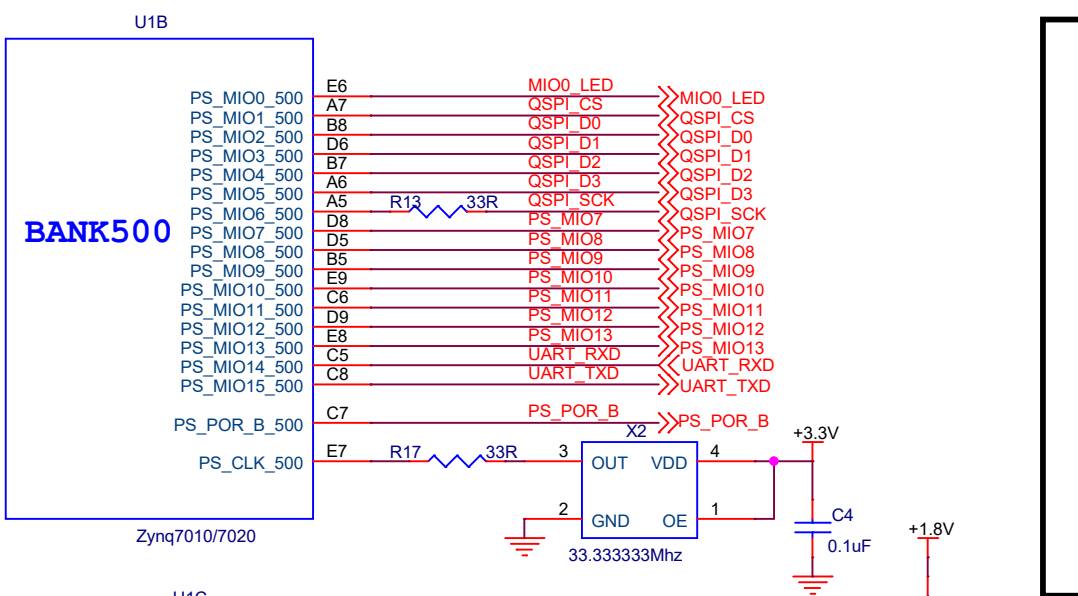
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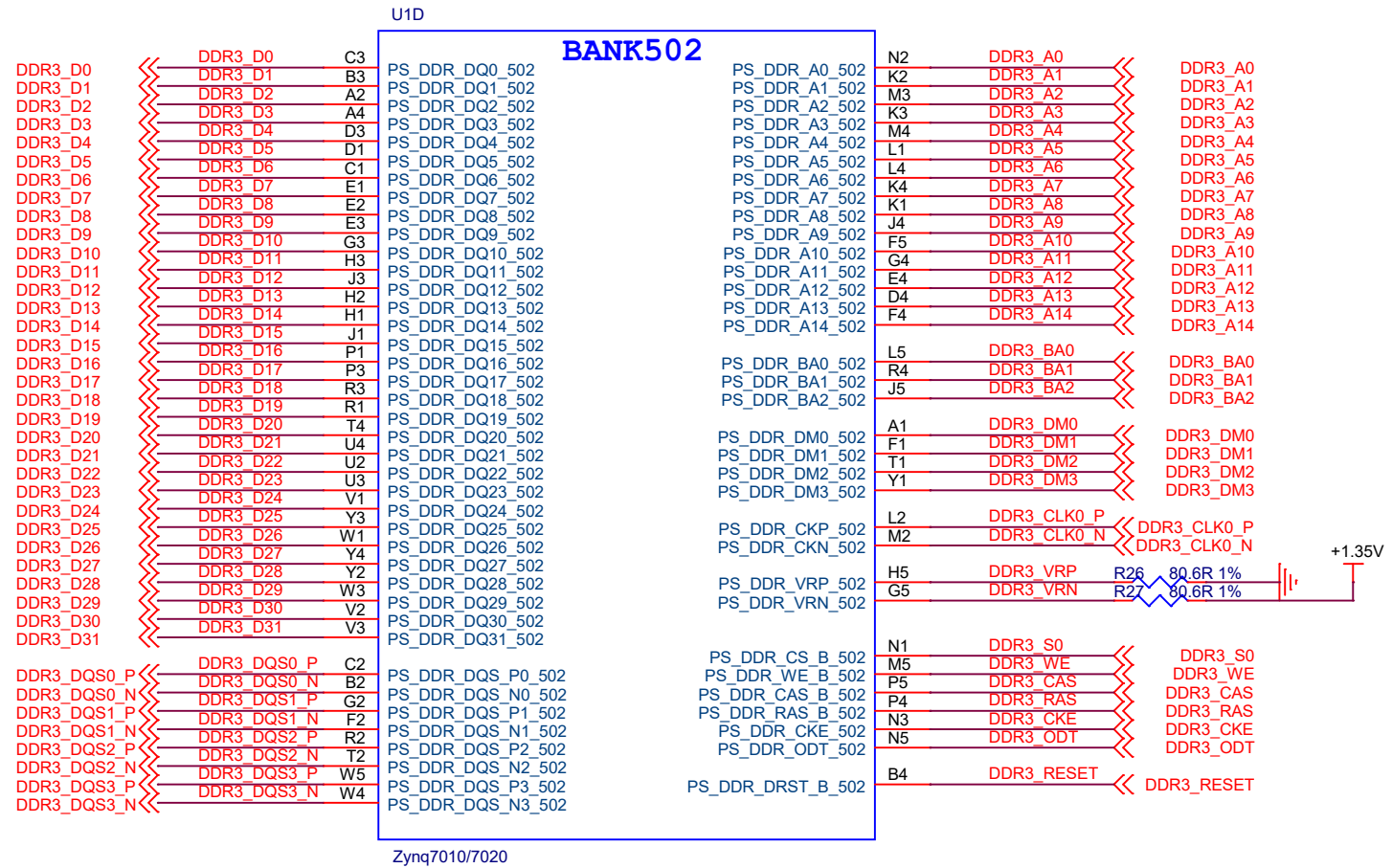
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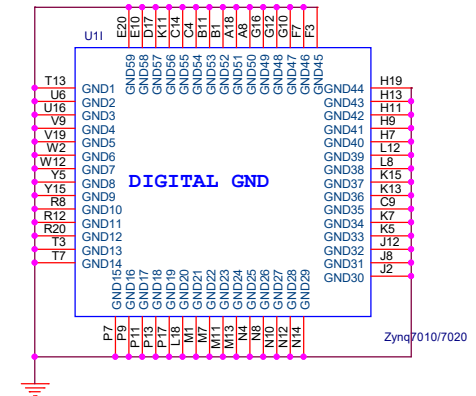
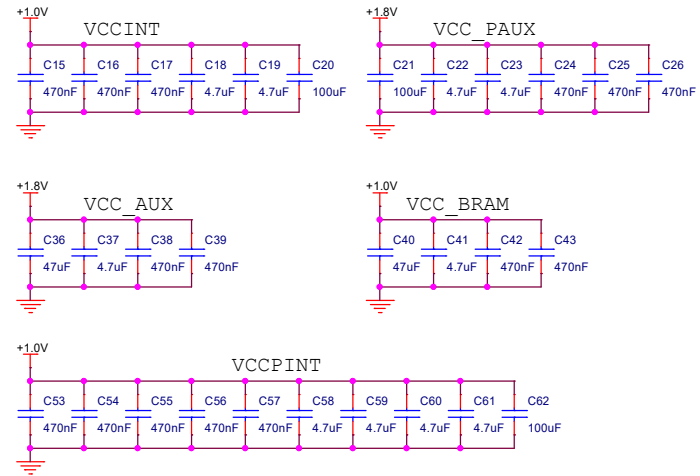
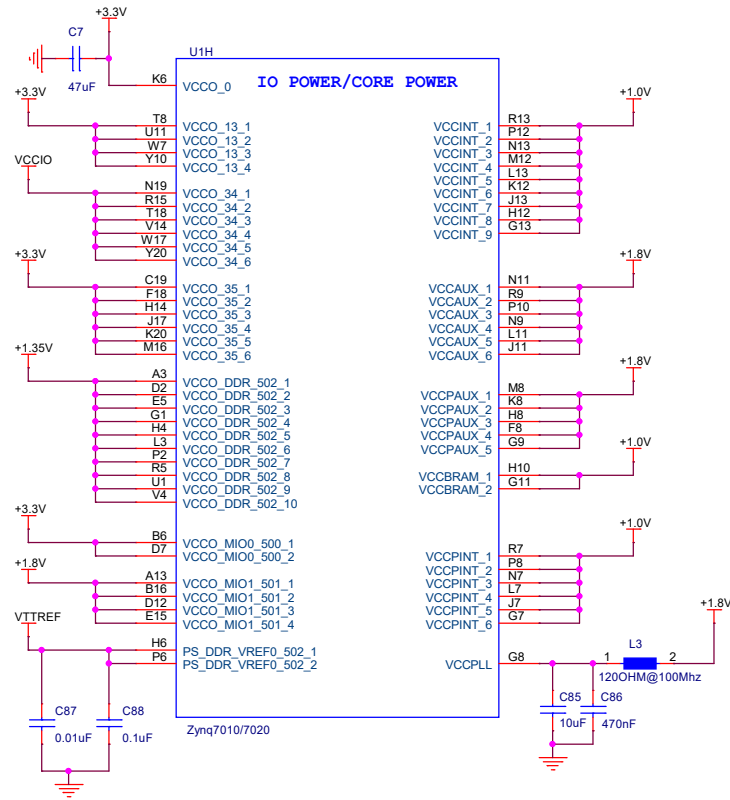
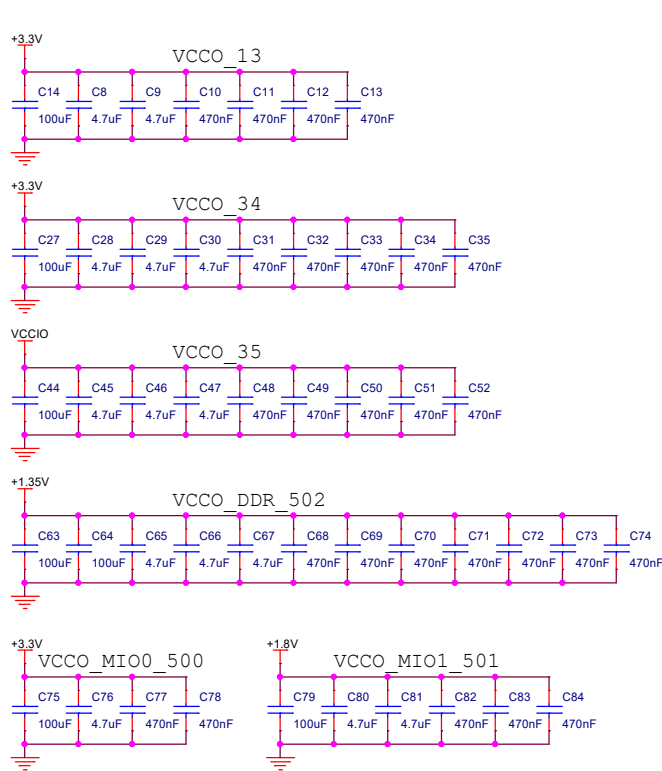


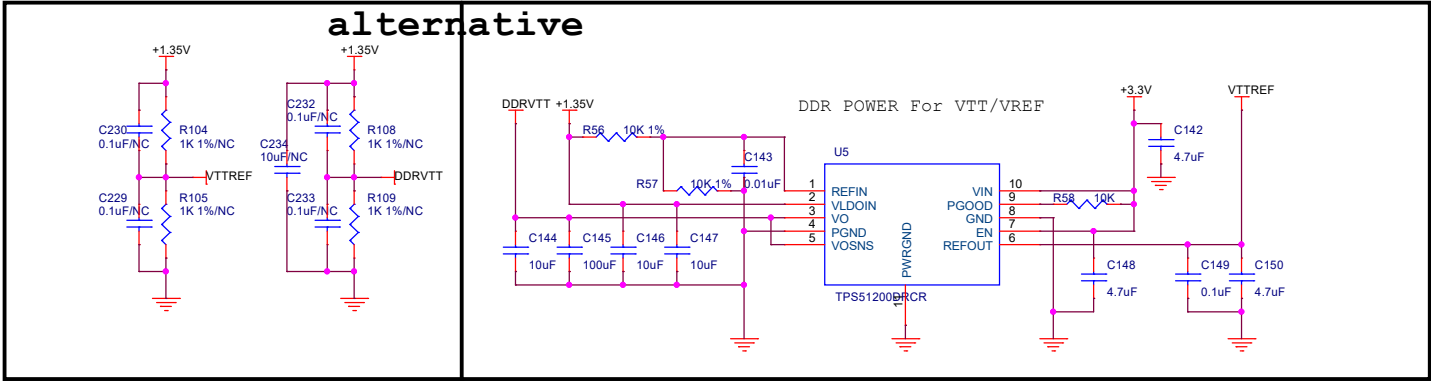
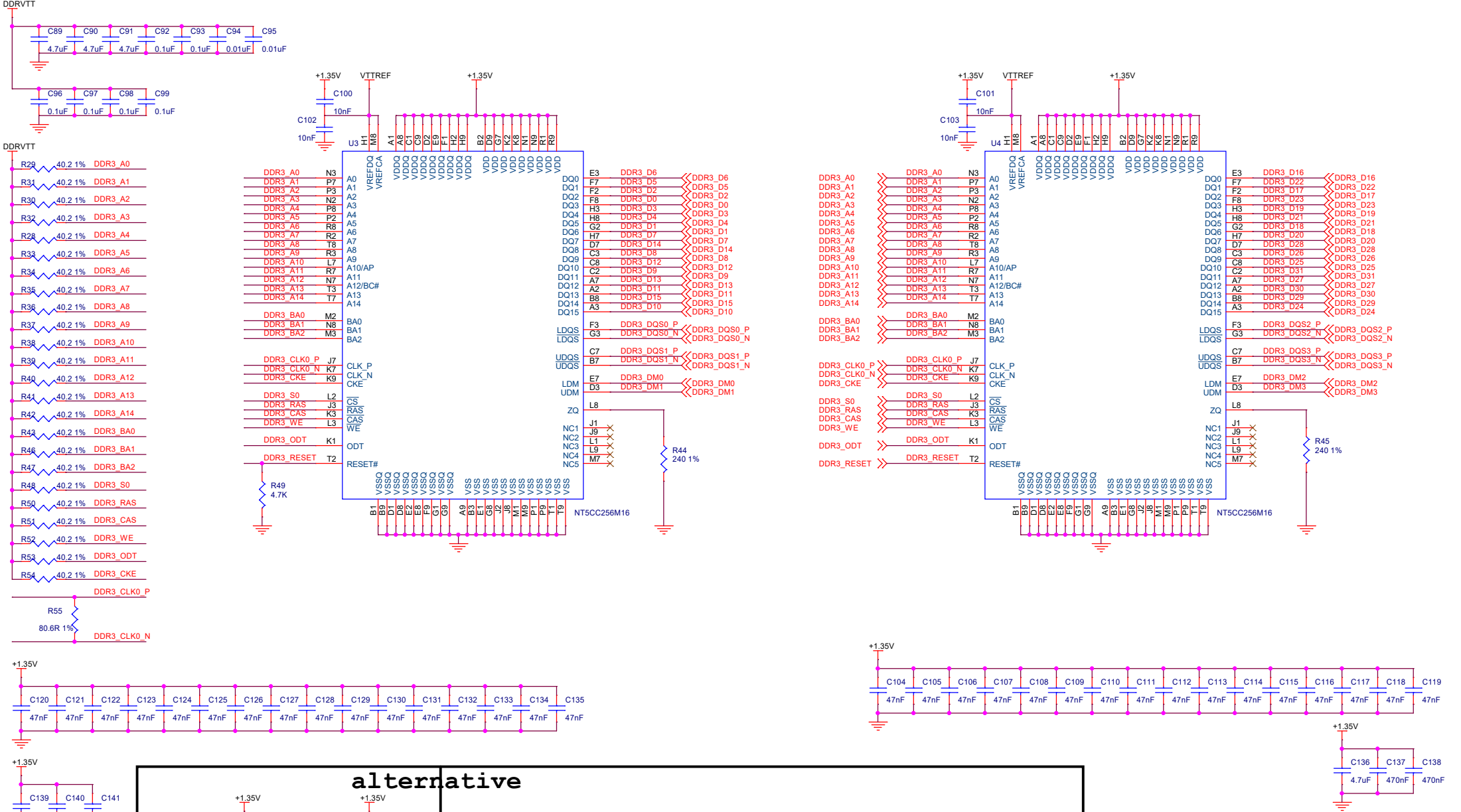
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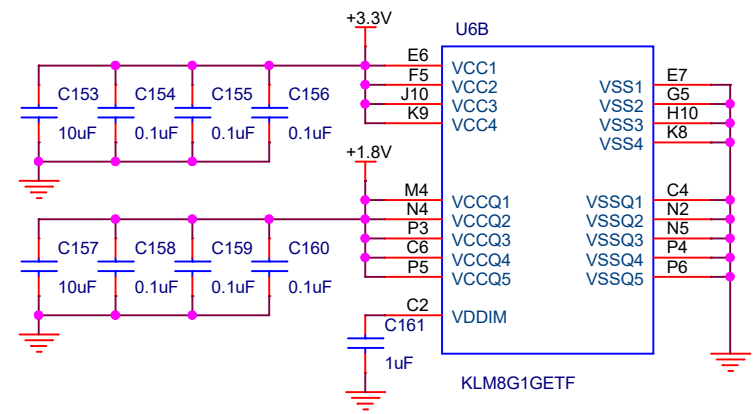
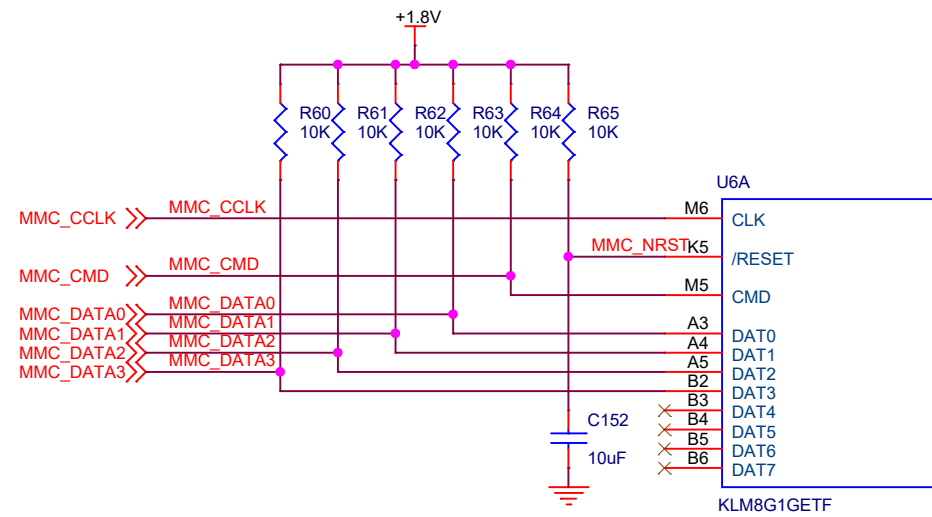
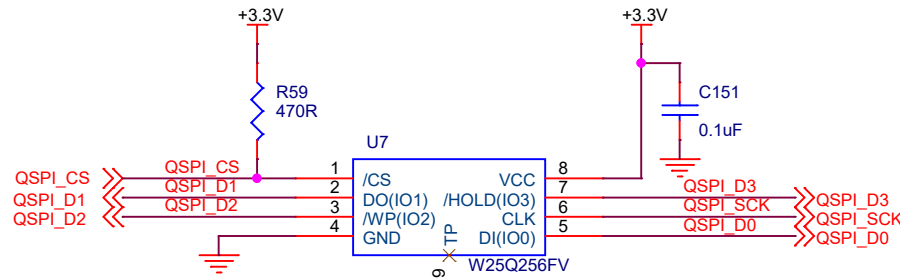
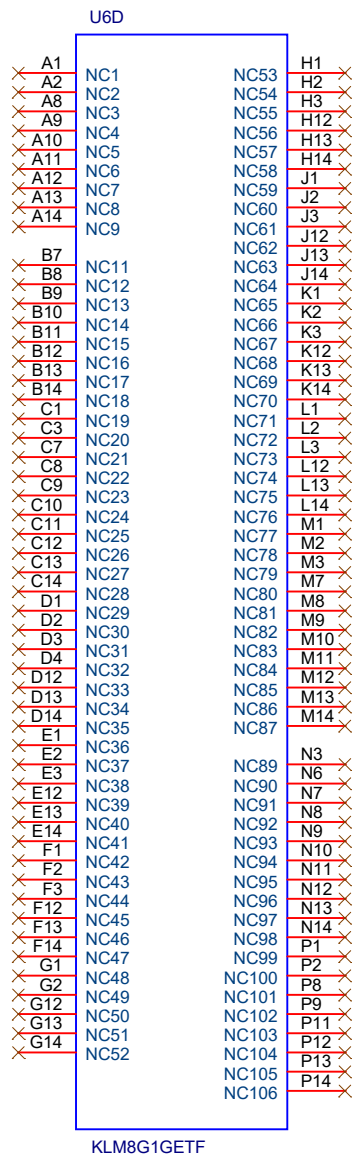


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A4	04 FPGA Bank500,Bank501	1.0	
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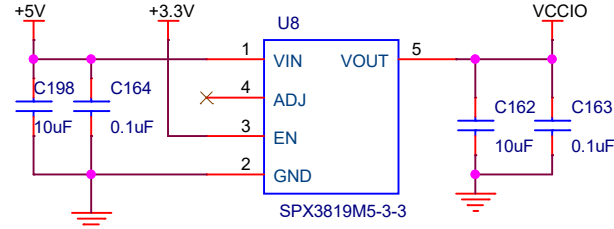
$$V_{out}=0.6 \cdot R1/R2+0.6$$

1.0V POWER@2A

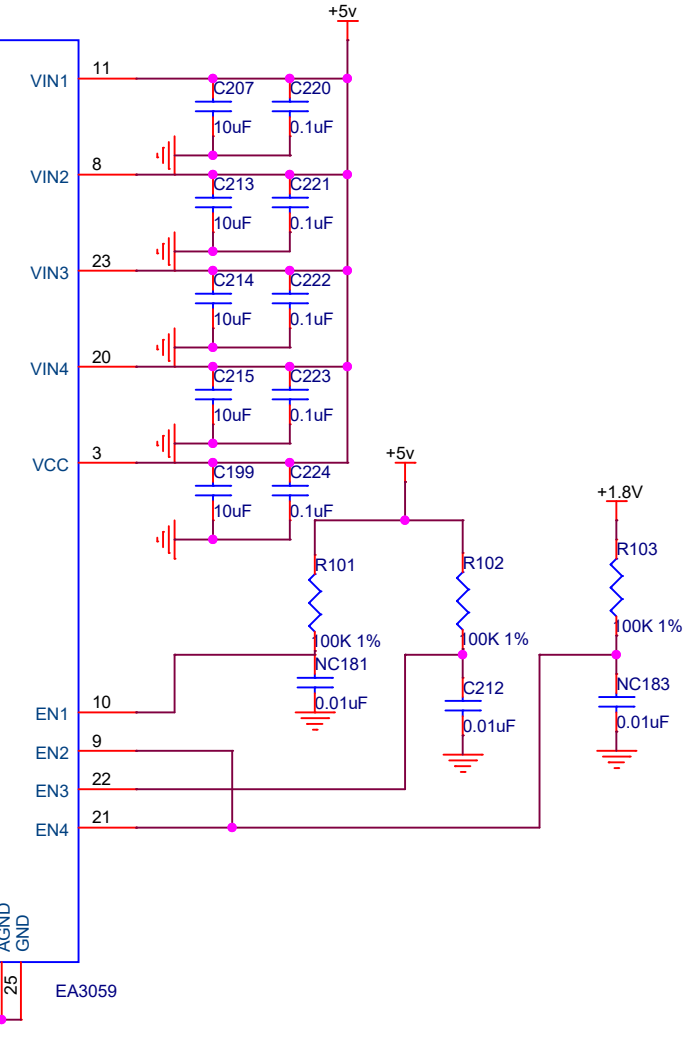
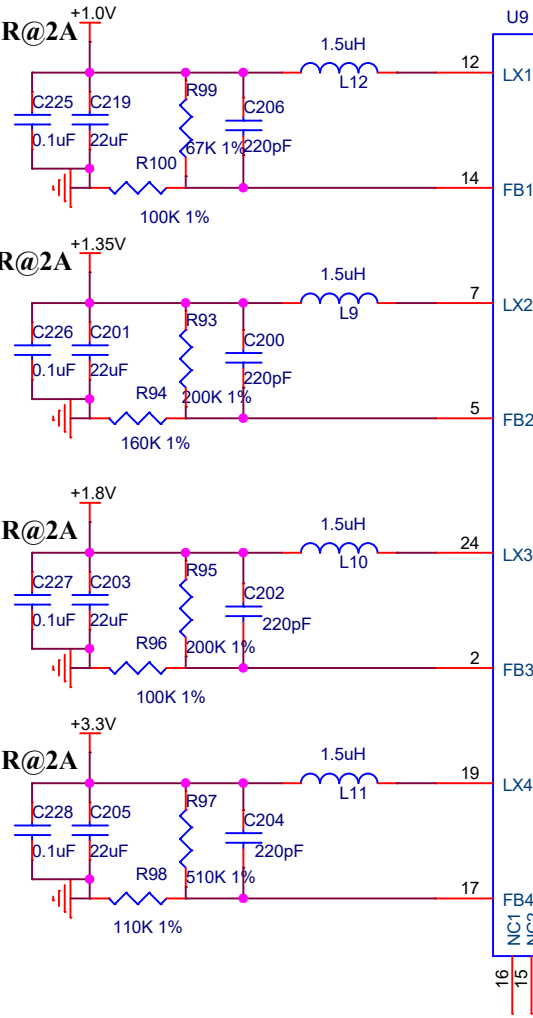
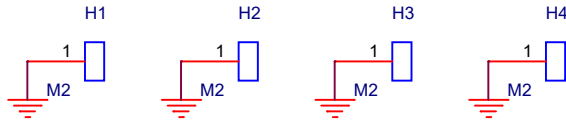
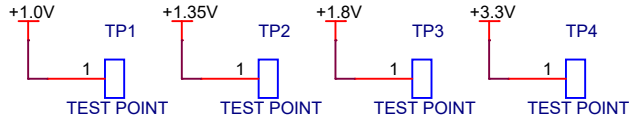
1.35V POWER@2A

1.8V POWER@2A

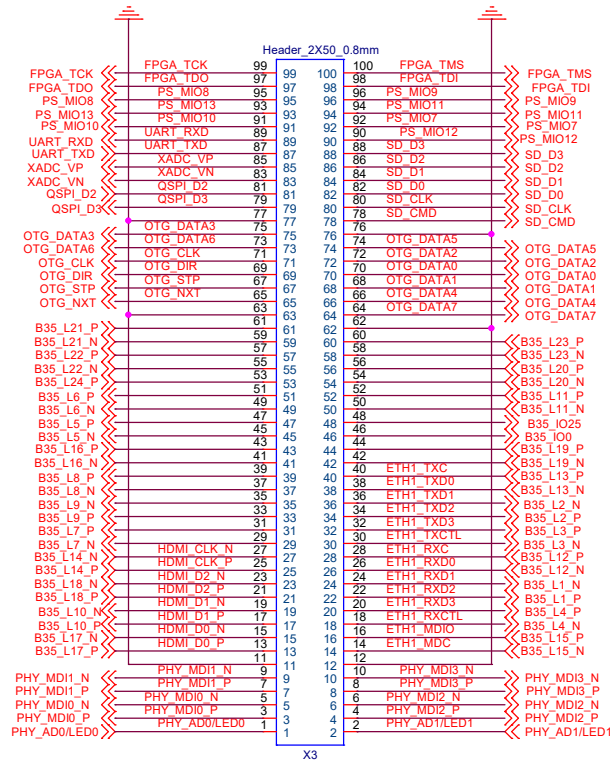
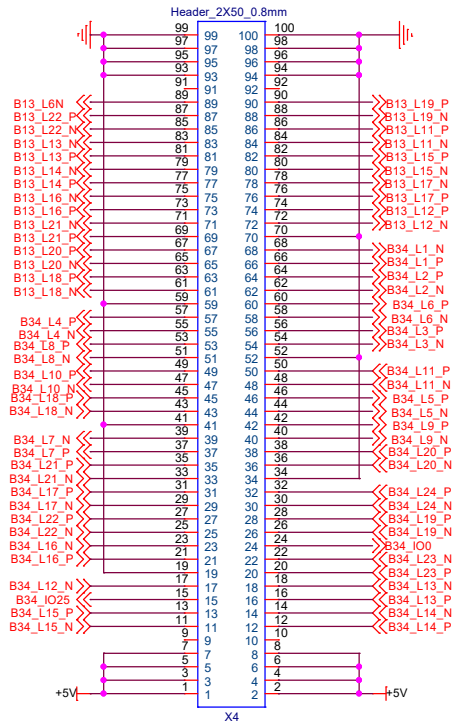
3.3V POWER@2A



Power On Sequence:
1.0V -> 1.8V -> 1.35V -> 3.3V -> VCCIO



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