MOTOROLA

SEMICONDUCTORS

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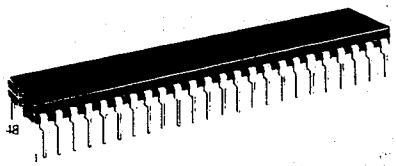
MC68486

Advance Information

RASTER MEMORY INTERFACE

BIPOLAR LSI-MOSAIC



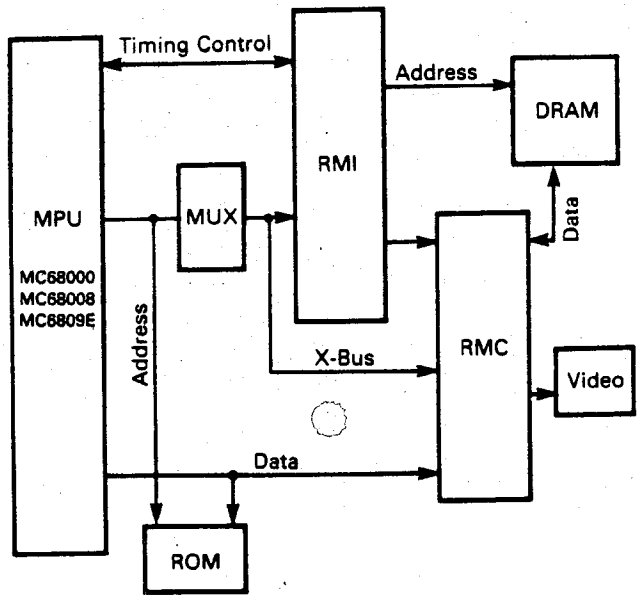
PLASTIC PACKAGE
CASE 767-02

TECHNICAL SUMMARY

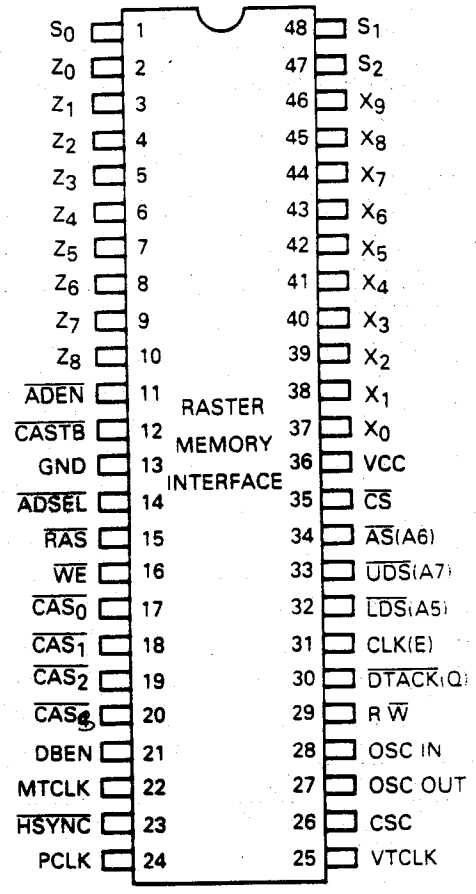
DESCRIPTION — The MC68486 Raster Memory Interface (RMI) circuit combined with the MC68487 Raster Memory Controller (RMC) results in a sophisticated video display controller and memory management tool, designated the Raster Memory System (RMS). The RMI is an LSI Bipolar circuit that performs several functions within the RMS structure. It is a clock generator and master oscillator that provides timing control to the RMS. In addition, the RMI translates addresses of the MPU to DRAM, generates handshaking signals for the MC68000 microprocessor family, and performs memory management functions for MC6809E-based systems.

- Intended for Personal and Home Computers and Teletext/Videotex Terminals
- Controls Refresh and Addressing Functions for 16K to 1Mbyte of DRAM
- Functions as Address Decoder for Devices Other Than RMS
- Supports Video Overlay Applications
- Provides Memory Management for MC6809E Systems
- Compatible with NTSC/PAL Displays and Supports Interlaced and Noninterlaced Video
- Generates All Timing Signals Required By the DRAM, RMC and MPU
- RMI Outputs are Designed to Drive Up to 32 DRAM Parts Directly
- Extensive Use of Page Mode to Efficiently Utilize DRAM
- Can Operate with 16K x 1, 16K x 4, 64K x 1 and 256K x 1 DRAMs
- Maintains Synchronization Between All Interfacing Chips

SIMPLIFIED SYSTEM DIAGRAM



PIN ASSIGNMENT



MOSAIC is a trademark of Motorola Inc.

ADI1115

This document contains information on a new product. Specifications and information herein are subject to change without notice.

SPECIFICATIONS

I. ABSOLUTE MAXIMUM RATINGS: (Above which the useful product life may be impaired).

Parameter		Symbol	Value	Units
Supply Voltage		V_{CC}	−0.5 to 7.0	V
Input Voltage	OSC & X_i Inputs	V_{in}	−0.5 to V_{CC}	V
	Other Inputs		−0.5 to 7.0	
Input Current (dc)	OSC Inputs	I_I	−0.5 to 5.0	mA
	Other Inputs		−30 to 5.0	
Output Voltage	Open-Collector	V_O	5.5	V
	Other Outputs		5.5	
Storage Temperature Range		T_{stg}	−55 to 150	°C
Junction Temperature		T_J	150	°C

II. THERMAL CHARACTERISTICS

Characteristics	Symbol	Value (Typical)	Units
Thermal Resistance, Junction to Ambient (P Suffix)	θ_{JA}	40	°C/W

III. GUARANTEED OPERATING RANGES

Parameter		Symbol	Min	Typ	Max	Units
Supply Voltage		V_{CC}	4.75	5.0	5.25	V
Operating Ambient Temperature Range		T_A	0	25	70	°C
Output Current HIGH	Z_n, $\overline{CAS}_n$, $\overline{RAS}$, $\overline{WE}$	I_{OH}	—	--	−3.0	mA
	CLK, E and Q		—	—	−0.2	
	Other Outputs		—	—	−0.4	
Output Current LOW	Z_n, $\overline{CAS}_n$, $\overline{RAS}$, $\overline{WE}$	I_{OL}	—	—	24	mA
	CLK, E and Q		—	—	4.0	
	Other Outputs		—	—	8.0	
Output Voltage HIGH	$\overline{DTACK}$	V_{OH}	—	—	5.5	V

IV. DC CHARACTERISTICS: (Over operating temperature range.)

Parameter		Symbol	Limits			Conditions
			Min	Max	Units	
Guaranteed Input HIGH Voltage		V_{IH}	2.0		V	
Guaranteed Input LOW Voltage		V_{IL}		0.8	V	
Input Clamp Voltage		V_{IK}		−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
Output Current HIGH	$\overline{DTACK}$	I_{OH}		100	μA	V_{CC} = MIN, V_{OH} = 5.5 V
Output Voltage HIGH	CLK, E, and Q	V_{OH}	V_{CC} − 0.75 V		V	V_{CC} = MIN, I_{OH} = −0.2 mA
	Z_n, $\overline{CAS}_n$, $\overline{RAS}$ & $\overline{WE}$		2.4		V	V_{CC} = MIN, I_{OH} = −3.0 mA
	Other		2.7		V	V_{CC} = MIN, I_{OH} = −0.4 mA
Output Voltage LOW	CLK, E, and Q	V_{OL}		0.5	V	V_{CC} = MIN, I_{OL} = 4.0 mA
	Z_n, $\overline{CAS}_n$, $\overline{RAS}$ & $\overline{WE}$			0.5	V	V_{CC} = MIN, I_{OL} = 24 mA
	Other			0.5	V	V_{CC} = MIN, I_{OL} = 8.0 mA
Input Current LOW	X_i Inputs*	I_{IL}		−8.0	mA	V_{CC} = MAX, V_{IN} = 0.5 V
	Other Except OSC IN			−0.2	mA	V_{CC} = MAX, V_{IN} = 0.5 V
Input Current HIGH	Except OSC & X_i Inputs	I_{IH}		20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	Except OSC & X_i Inputs*			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
Output Short Circuit Current		I_{OS}	−30	−225	mA	V_{CC} = MAX, V_O = 0.0 V
Power Supply Current		I_{CC}		300	mA	V_{CC} = MAX

*The X_i inputs have internal 850 Ω (typical) pullup resistors connected to V_{CC}. These inputs should not be forced above V_{CC}. The OSC inputs must also be kept below V_{CC}.

INTRODUCTION TO RMS

The Raster Memory Interface (RMI) is a clock generator and memory management unit which is combined with the Raster Memory controller (RMC — MC68487) to create a powerful chip set designated the RASTER MEMORY SYSTEM (RMS). When interfaced with a microprocessor and memory, the Raster Memory System becomes a sophisticated video display controller and memory management tool which offers the user a great deal of application flexibility. This flexibility is inherent in the RMS due to the variety of operating modes available. RMS is backwards compatible with the MC6847 and MC6883. In addition, it supplies several new, innovative modes which allow the programmer to zero in on high resolution color graphics, teletext/videotex, word processing, and game applications. With this kind of versatility, a designer can create a low end, low cost text and graphics computer with impressive game capabilities. With the addition of memory and more sophisticated software, evolve the system into a high level, high resolution work station.

The RMS is a state-of-the art chip set that includes features unavailable in less sophisticated video controllers. The RMS's multi-mode video provides three sources of video generation: Bit plane graphics, list mode graphics and true objects. The displayed modes are highly programmable allowing optimization of display memory size, color selection and resolution. The RMS operates with most popular CRTs, and supports two popular video standards; NTSC and PAL. RMS's operational differences for these two standards are shown in Table 1. The selection of PAL or NTSC operation is explained under the Reset and Initialization section.

RMS always operates in a full color mode, and using a Color Mapping RAM, can simultaneously display 32 colors from its palette of 4096 colors. The RMS can accommodate a Virtual Screen much larger than the monitor's displayed screen. Smooth scrolling of the displayed screen within the virtual screen can be accomplished horizontally and vertically using a minimum of actual MPU involvement. Only a few registers are used to define the size and location of both the virtual and displayed screens. The RMS provides all support required by the system DRAM. Systems can be configured with as little as 16 Kbytes, up to a full 1 Mbyte.

RMS operates with any of three Motorola microprocessors; the MC6809E, MC68008 or the MC68000. Memory can be expanded up to 1 Mbyte with any of the aforementioned MPU's, however thru-put is higher with the MC68000. Because of time division multiplexing on the data bus, the MPU has transparent access to memory even during active display. RMS also provides DRAM refresh automatically.

TABLE 1. RMS OPERATIONAL DIFFERENCES

Feature	PAL	NTSC
Number of Video Lines	625	525
Color Subcarrier (CSC) Frequency	4.43618 MHz	3.579545 MHz
Screen Refresh Rate	50 Hz	60 Hz
Maximum Screen Resolution: Interlaced	640 x 500	640 x 420
Maximum Screen Resolution: Non-Interlaced	640 x 250	640 x 210

PIN DEFINITIONS

OSC IN, OSC OUT (Master Oscillator) [Input]
The master oscillator [illegible]ed on the RMI, is used to generate the color subc[illegible]r, MPU clock, and all internal clocks required by RMS. For NTSC applications (3.579545 MHz sub-carrier), the master oscillator is ten times the sub-carrier or 35.79545 MHz. For PAL applications (4.43618 MHz sub-carrier), the master oscillator is eight times the sub-carrier or 35.48944 MHz. A crystal and tank tuning circuit are connected between these pins to generate the master oscillator clock.

VTCLK (Video Timing Clock) [Output]
VTCLK is a free running clock and is equal to the master oscillator divided by five. The RMC uses this clock supplied by the RMI for internal timing and to generate horizontal sync, vertical sync and blanking pulses.

PCLK (Picture Element Clock) [Output]
The Picture Element Clock is used by RMC to shift video information to the display. PCLK has an approximate duty cycle of 50%, and in some modes may be stretched during horizontal retrace to be resynchronized with VTCLK.

MTCLK (Memory Timing Clock) [Output]
MTCLK is generated by RMI and used by RMC to keep track of memory cycles. Each memory cycle is made up of 9 MTCLK cycles. Depending on horizontal resolution, a memory cycle, which provides one MPU and one RMC memory access, is either 16 or 8 PCLK cycles long. The first 8 MTCLK cycles are equal to the master oscillator divided by four, and the ninth is stretched, if necessary, to match the PCLK cycles. MTCLK is also stretched near the trailing edge of horizontal sync to resynchronize the memory cycle to VTCLK.

CLK(E) (MPU Clock or E Clock) [Output]
CLK(E) is supplied by RMI to the MPU. The type of clock provided depends on whether a MC6809E or MC68000 family MPU is in use.

For the MC6809E, CLK(E) is used as the MPU's E clock and runs at the memory frequency. E's duty cycle depends on the horizontal resolution. It is HIGH for the first 4 X-Bus cycles and LOW for the last 5 X-Bus cycles within a memory cycle. This clock is also stretched at the end of each horizontal line the same way as the memory clock to resynchronize to VTCLK.

For the MC68000 family MPU's, CLK(E) is a free running clock equal to the master oscillator divided by 4.5.

$\overline{\text{DTACK}}$(Q) (Data Acknowledge) [Output open-collector] (Q Clock) [Output standard]
$\overline{\text{DTACK}}$(Q) is supplied by RMI to the MPU. It is a dual purpose pin providing a Q clock output in MC6809E systems, and is an open-collector handshaking line in MC68000 family systems.

CSC (Color Sub-Carrier) [Output]
CSC is supplied by the RMI for use by other parts of the system, principally a video modulator. It is equal to the master oscillator divided by 8 or 10, depending on whether NTSC or PAL video is selected.

$\overline{\text{CS}}$ (Chip Select) [Input]
The $\overline{\text{CS}}$ pin on RMI is an active LOW input and causes the RMS to be enabled. The MPU may then access RMS control registers, video memory, or I/O decoded by RMI.

$\overline{\text{AS}}$(A6) (Address Strobe) [Input]
When a MC68000 family MPU is used, its address strobe is connected to this RMI input pin. The falling edge of $\overline{\text{AS}}$ identifies the start of an MPU bus cycle.

$\overline{\text{UDS}}$(A7) (Upper Data Strobe) [Input] and $\overline{\text{LDS}}$(A5) (Lower Data Strobe) [Input]
These RMI input pins are similar to the $\overline{\text{AS}}$(A6) input when used with the MC6809E. If a MC6809E system uses the RMI S-Bus, then $\overline{\text{UDS}}$(A7) must be connected to address bit 7 of the MPU, and $\overline{\text{LDS}}$(A5) must be connected to address bit 5 of the MPU. If a MC6809E system is not using the S-Bus outputs, these pins may be left unconnected.

If the system is using the MC68000 MPU, then $\overline{\text{UDS}}$(A6) must be connected to the $\overline{\text{UDS}}$ output of the MPU, and $\overline{\text{LDS}}$(A5) must be connected to the $\overline{\text{LDS}}$ pin of the MPU. If the system is using the MC68008 MPU, then $\overline{\text{LDS}}$ must be connected to the $\overline{\text{DS}}$ output of the MPU. $\overline{\text{UDS}}$(A6) may be left unconnected.

R/$\overline{\text{W}}$ (Read/$\overline{\text{Write}}$) [Input]
R/$\overline{\text{W}}$ is an input pin that must be connected to the MPU R/$\overline{\text{W}}$ signal. It is used to control the direction of data flow for MPU accesses to either DRAM or RMS control registers.

$\overline{\text{HSYNC}}$ (Horizontal Sync) [Input]
$\overline{\text{HSYNC}}$ is used internally to resynchronize all RMS clocks at the end of each horizontal video line. It must be connected to the $\overline{\text{HSYNC}}$ output pin on the RMC.

DBEN (Data Bus Enable) [Output]
This RMI output pin is used in conjunction with R/$\overline{\text{W}}$ to determine when and in which direction the RMC should enable the MPU data bus to avoid conflict with other devices on that bus.

PIN DEFINITIONS (continued)

X_0–X_9 (XBUS) [Inputs]
The RMI X-Bus pins (X_0 through X_9) are inputs that connect to the RMC and MPU address multiplexing logic. Eight different words are passed to the RMI during each memory cycle. The first two words contain the multiplexed MPU high and low address output, which are read by both the RMI and RMC to determine where the MPU is accessing memory. The third and fourth words passed on the X-Bus are from the RMC to the RMI and contain the display address for the RMC DRAM access. The fifth through eighth words are passed from the RMC to the RMI and contain control information for the RMI to operate together with the RMC as a system.

$\overline{ADEN}$ (Address Enable) [Output]
This is an RMI active LOW output signal that enables the external MPU address multiplexers to place the MPU address information on the X-Bus.

$\overline{ADSEL}$ (Address Select) [Output]
This RMI output pin is used in conjunction with $\overline{ADEN}$ to enable either the HIGH or LOW MPU address word onto the X-bus. (HIGH = MSB's, LOW = LSB's)

S_0–$_2$ (Device Select) [Outputs]
This RMI 3-bit output bus (S_0, S_1, S_2) can be used to access devices other than the RMS. The RMS offers several different memory maps to the user, who can use the S-bus outputs to perform the device selects. The S-bus should be decoded by a 3-to-8 line decoder to provide the individual chip selects.
Note: Decode 7 is reserved for internal addressing of the RMS system.

Z_0–$_8$ (DRAM Address Bus) [Outputs]
The RMI's Z-bus is a multiplexed nine-wide output bus (Z_0 through Z_8) that connects directly to the DRAM address lines. Translation to the correct format of multiplexed addresses is internal to the RMI.

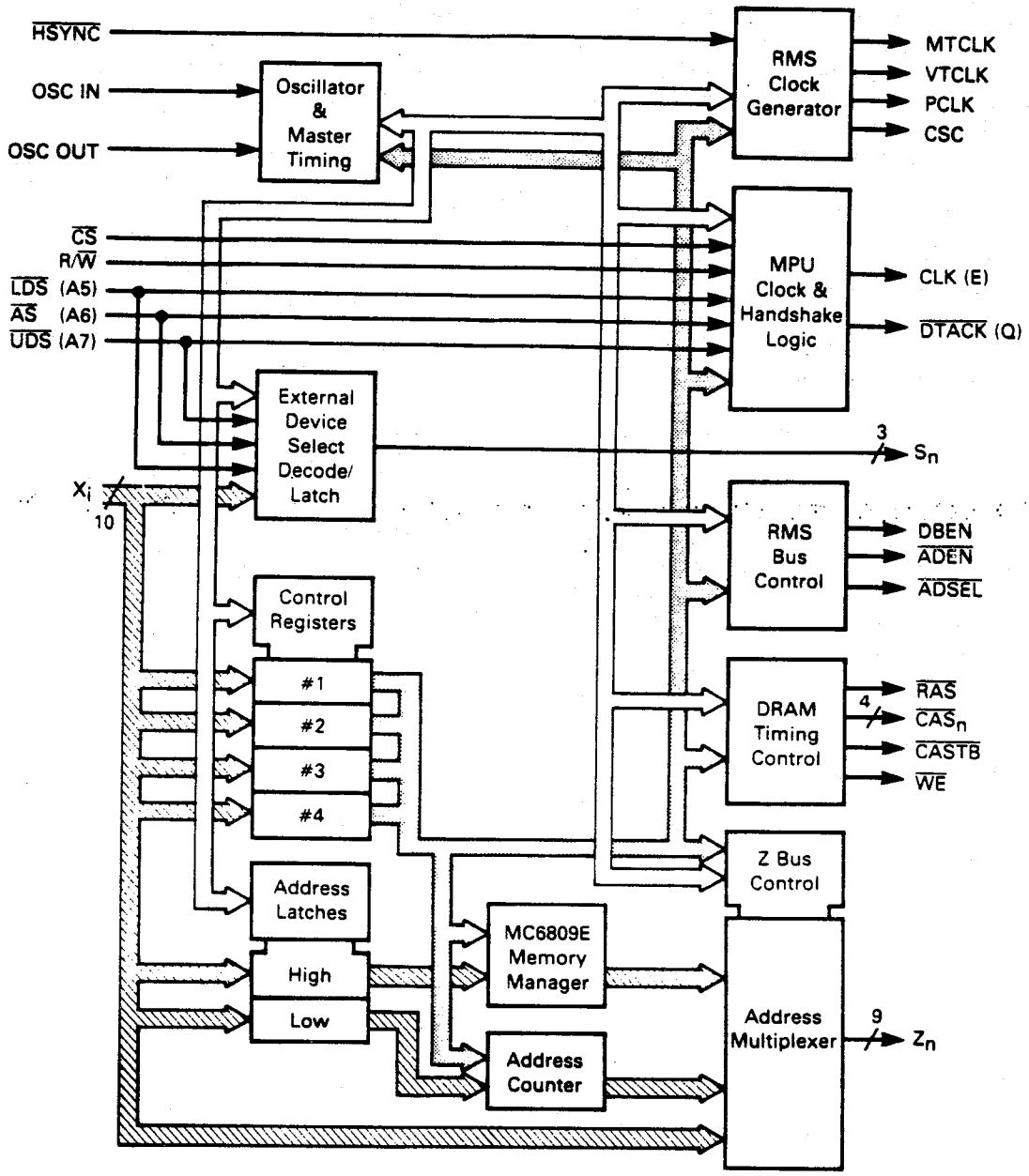
$\overline{RAS}$ (Row Address Strobe) [Output]
The RMI's $\overline{RAS}$ output pin is used to strobe the most significant bits of address from the Z-bus to the DRAM. It connects directly to the $\overline{RAS}$ input on all DRAM devices controlled by the RMS.

$\overline{CAS}_{0-3}$ (Column Address Strobe) [Outputs]
The RMI's $\overline{CAS}$ output pins ($\overline{CAS}_0$, $\overline{CAS}_1$, $\overline{CAS}_2$, $\overline{CAS}_3$) are used to strobe the least significant bits of address from the Z-bus to the DRAM. Each $\overline{CAS}$ pin drives a different bank of DRAM directly.

$\overline{CASTB}$ ($\overline{CAS}$ Strobe) [Output]
This RMI output pin is connected to the RMC $\overline{CASTB}$ input and strobes display data into the RMC from DRAM.

$\overline{WE}$ ($\overline{Write\ Enable}$) [Output]
This RMI output pin is used to write data to the DRAM. It connects directly to the $\overline{WE}$ input on all DRAM devices controlled by RMS.

FIGURE 1 — RMI BLOCK DIAGRAM



RMI ARCHITECTURE

The primary function of the Raster Memory Interface is to control dynamic memory and system timing. A secondary function is chip select address decoding for peripherals external to RMS. The RMI can be broken into eleven logic blocks as shown in Figure 1, each of which is explained below.

Oscillator and Master Timing

This block contains an amplifier between OSC IN and OSC OUT which provides the gain required for oscillation (by using a crystal and LC tank circuit as shown in Figure 2). The OSC IN input can also be driven by an external clock source as shown in Figure 3. This is useful for device testing. For video overlay applications, horizontal synchronization may be achieved by "Tuning" the RMI master oscillator or by providing an external clock source. Vertical synchronization is provided directly by the RMC.

RMS Clock Generator

The Clock Generator contains counters and control logic which generate clock outputs used by the RMS. The function of each of these clock outputs is explained under RMI pin definitions.

MPU Clock and Handshake Logic

This logic generates MC6809E clocks (E and Q) or a MC68008/MC68000 clock and $\overline{DTACK}$ signal. This logic provides MC6809E systems with 745 to 994 (NTSC) kHz clocks (E & Q), which enable the MPU to access any peripheral including video memory or RMS control registers at this rate. In some video modes, the RMS will stretch MC6809E MPU clocks occasionally as required. The RMS will provide MC68000 MPUs with a 7.93 MHz clock, and provide handshaking via the $\overline{DTACK}$ output to allow access to RMS registers and video memory at a 745 to 994 kHz rate (NTSC), depending on screen resolution. For PAL systems, the frequencies are 739 kHz to 985 kHz and 7.88 MHz.

External Device Select Decode/Latch

This logic block decodes the MPU address bus and provides a 3-bit output which, when decoded externally by a 3-to-8 line decoder, provides chip selects for devices external to the RMS system. The decoded value of S=7, (S0=S1=S2=HIGH) is reserved for internal addressing of the RMS system.

There are several system memory maps available to the user to fit different needs. The map in use at any time is determined by the state of the $MACH_2$, MAPA, UF and LPI_0 bits in the RMI control registers.

The various memory maps are shown in Tables 3 through 6. A detailed discussion of how to use the different memory maps is covered in the RMS User's Manual.

RMS Bus Control

The timing and DATA source on the X-Bus is controlled by this logic block. The X-Bus provides the multiplexed MPU address to the RMI and RMC and also is used to transfer the video address and control information from the RMC to the RMI.

The functional state of the X-Bus is described in Table 2.

A third output of the RMS bus control logic is DBEN. This output is used by RMC in conjunction with the MPU R/$\overline{W}$ line to determine the source and direction of information on the system DATA bus. When DBEN is HIGH, the MPU will have access to read from or write to display memory or RMS control registers.

FIGURE 2 — CRYSTAL CIRCUIT

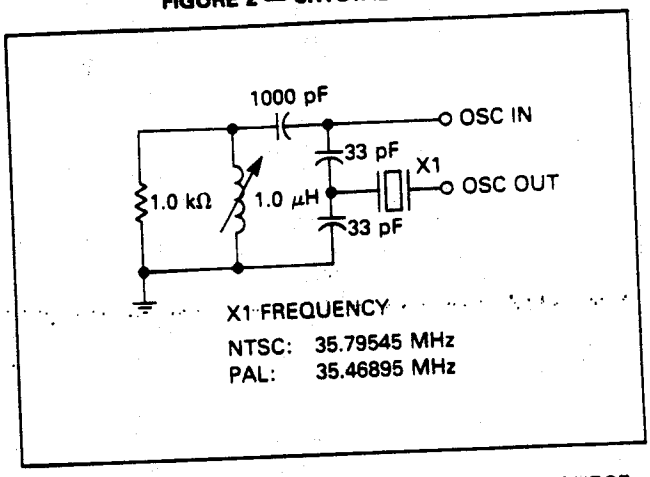


FIGURE 3 — PROVIDING AN EXTERNAL CLOCK SOURCE FOR RMI

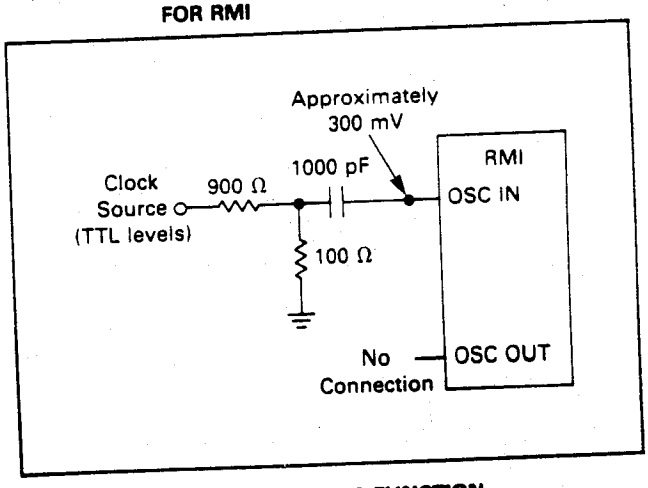


TABLE 2. X-BUS FUNCTION

ADEN	ADSEL	X-BUS FUNCTION
L	H	Send MPU HIGH address to RMI/RMC.
L	L	Send MPU LOW address to RMI/RMC.
H	H	Send video address or control information from RMC to RMI.

TABLE 3. MACHINE 1 — MC6809E MEMORY MAPS

RMI Control Bits		Memory Address		S		
MAPA	Unfold	Start	End	Bus	Name	Size
0	0	00000 —	F7FFF	7	DRAM	992K
		F8000	F9FFF	1	ROM 0	8K
		FA000	FBFFF	2	ROM 1	8K
		FC000	FFEFF	3	ROM 2	16K — 256
		FFF00	FFF1F	4	I/O 0	32
		FFF20	FFF3F	5	I/O 1	32
		FFF40	FFF5F	6	I/O 2	32
		FFF60	FFF7F	7	Reserved	32
		FFF80	FFFBF	7	RMS Registers	64
		FFFC0	FFFDF	7	Reserved	32
		FFFE0	FFFFF	2	ROM 1 (Vectors)	32
0	1	00000 —	F7FFF	7	DRAM	992K
		F8000	F9FFF	1	ROM 0	8K
		FA000	FBFFF	2	ROM 1	8K
		FC000	FFDFF	3	ROM 2	16K — 512
		FFE00	FFEBF	7	RMS Registers	192
		FFEC0	FFEFF	7	Reserved	64
		FFF00	FFF1F	4	I/O 0	32
		FFF20	FFF3F	5	I/O 1	32
		FFF40	FFF5F	6	I/O 2	32
		FFF60	FFFDF	7	Reserved	128
		FFFE0	FFFFF	2	ROM 1 (Vectors)	32
1	0	00000 —	FFEFF	7	DRAM	1M — 256
		FFF00	FFF1F	4	I/O 0	32
		FFF20	FFF3F	5	I/O 1	32
		FFF40	FFF5F	6	I/O 2	32
		FFF60	FFF7F	7	Reserved	32
		FFF80	FFFBF	7	RMS Registers	64
		FFFC0	FFFDF	7	Reserved	32
		FFFE0	FFFFF	2	ROM 1 (Vectors)	32
1	1	00000 —	FFDFF	7	DRAM	1M — 512
		FFE00	FFEBF	7	RMS Registers	192
		FFEC0	FFEFF	7	Reserved	64
		FFF00	FFF1F	4	I/O 0	32
		FFF20	FFF3F	5	I/O 1	32
		FFF40	FFF5F	6	I/O 2	32
		FFF60	FFFDF	7	Reserved	128
		FFFE0	FFFFF	2	ROM 1 (Vectors)	32

TABLE 4. MACHINE 2 MEMORY MAP
Type #0 — Primarily for ROM Based Systems.

PHYSICAL ADDRESS*			S		
Start		End	Bus	Name	Size
00000	—	F7FFF	7	RAM	992K
F8000		F9FFF	1	ROM 0	8K
FA000		FBFFF	2	ROM 1	8K
FC000		FFEFF	3	ROM 2	16K–256
FFF00		FFF1F	4	I/O 0	32
FFF22		FFF22	5	Machine 2 Register	1
FFF20		FFF3F	5	I/O 1	32
FFF40		FFF5F	6	I/O 2	32
FFF60		FFF7F	7	Reserved	32
FFF80		FFFBF	7	RMS Registers	64
FFFC0		FFFDF	7	Machine 2 Control Bits	32
FFFE0		FFFFF	2	ROM 1	32

*Physical address generation is explained in the section on the MC6809E memory manager.

TABLE 5. MACHINE 1 — MC68000 MEMORY MAPS

RMI Control Bits		Memory Address		S		
MAPA	LPIO/VEC	Start	End	Bus	Name	Size
0	0	00000 —	003FF	0	Excp Vector	1K
		00400	BFFFF	7	DRAM	767K
		C0000	CFFFF	1	ROM 9	64K
		D0000	DFFFF	2	ROM A	64K
		E0000	EFFFF	3	ROM B	64K
		F0000	FEFFF	4	ROM C	60K
		FF000	FF7FF	5	*I/O D	2K
		FF800	FFBFF	6	*I/O E	1K
		FFC00	FFDFF	7	Reserved	256
		FFE00	FFEBF	7	RMS Registers	192
		FFEC0	FFFFF	7	Reserved	576
0	1	00000 —	BFFFF	7	DRAM	768K
		C0000	CFFFF	1	ROM 9	64K
		D0000	DFFFF	2	ROM A	64K
		E0000	EFFFF	3	ROM B	64K
		F0000	FEFFF	4	ROM C	60K
		FF000	FF7FF	5	*I/O D	2K
		FF800	FFBFF	6	*I/O E	1K
		FFC00	FFDFF	7	Reserved	256
		FFE00	FFEBF	7	RMS Registers	192
		FFEC0	FFFFF	7	Reserved	576
1	0	00000 —	003FF	0	Excp Vectors	1K
		00400	EFFFF	7	DRAM	959K
		F0000	FEFFF	4	ROM C	60K
		FF000	FF7FF	5	*I/O D	2K
		FF800	FFBFF	6	*I/O E	1K
		FFC00	FFDFF	7	Reserved	256
		FFE00	FFEBF	7	RMS Registers	192
		FFEC0	FFFFF	7	Reserved	576
1	1	00000 —	EFFFF	7	DRAM	960K
		F0000	FEFFF	4	ROM C	60K
		FF000	FF7FF	5	*I/O D	2K
		FF800	FFBFF	6	*I/O E	1K
		FFC00	FFDFF	7	Reserved	256
		FFE00	FFEBF	7	RMS Registers	192
		FFEC0	FFFFF	7	Reserved	576

*RMS does not supply $\overline{\text{DTACK}}$ for these areas of the Memory Map.

TABLE 6. MACHINE 2 MEMORY MAP
Type #1 — Primarily for RAM Based Systems.

PHYSICAL ADDRESS*			S		
Start		End	Bus	Name	Size
00000	—	FFEFF	7	RAM	1M–256
FFF00		FFF1F	4	I/O 0	32
FFF22		FFF22	5	Machine 2 Register	1
FFF20		FFF3F	5	I/O 1	32
FFF40		FFF5F	6	I/O 2	32
FFF60		FFF7F	7	Reserved	32
FFF80		FFFBF	7	RMS Registers	64
FFFC0		FFFDF	7	Machine 2 Control Bits	32
FFFE0		FFFFF	2	ROM 1	32

*Physical address generation is explained in the section on the MC6809E memory manager.

org $C000
dc.l $0
dc.l $C0008
start jmp start

Control Registers

These registers contain information pertaining to RMS configuration, MPU type, etc. Specific bits pertaining to MPU type and video timing are loaded during system reset. The remaining information is passed from RMC to RMI via the X-Bus as follows.

During each RMS memory cycle, four control words are passed along the X-Bus from the RMC to the RMI control registers. Within the memory cycle, nine MT Clock cycles/states (MT_0–MT_8) occur. The four control words are placed on the X-Bus during MT_3–MT_6, and latched by RMI on the rising edge of the MT Clock.

The control registers are 10 bits wide. The contents of these registers are described below.

TABLE 7. REGISTER 1

Bit No.	Name	Function
0	$HRES_0$	Horizontal Resolution Bit "0"
1	$HRES_1$	Horizontal Resolution Bit "1"
2	$HRES_2$	Horizontal Resolution Bit "2"
3	LSTCYC	Last memory cycle
4		Reserved
5		Reserved
6	$MTYP_0$	Memory Type Bit "0"
7	$MTYP_1$	Memory Type Bit "1"
8	$MTYP_2$	Memory Type Bit "2"
9	$MTYP_3$	Memory Type Bit "3"

$HRES_{0-2}$ are required to generate a proper PEL (Picture ELement) clock. They define the number of PELs per horizontal line as indicated in Table 11.

LSTCYC is associated with clock resynchronization. It is a signal to RMI that the current memory cycle will be the last one on this horizontal line. After the memory cycle is complete, RMI should stretch MT Clocks until one VTCLK time after the trailing edge of $\overline{HSYNC}$.

The MTYP bits inform RMI what type of dynamic RAM is in use, and how it is organized in the system. See Table 12 for an explanation of how the bits are coded.

TABLE 8. REGISTER 2

Bit No.	Name	Function
0		Reserved
1		Reserved
2		Reserved
3		Reserved
4		Reserved
5	SWAP	M6809E paging bit
6	PG_0	M6809E paging bit
7	PG_1	M6809E paging bit
8	PG_2	M6809E paging bit
9	PG_3	M6809E paging bit

The SWAP and paging bits provide MC6809E memory management information to the RMI. (In Machine 2, P1 replaces the SWAP bit). The purpose of these bits are defined in the discussion of the MC6809 memory management block.

TABLE 9. REGISTER 3

Bit No.	Name	Function
0	LPI0	Lower page independent block Bit "0"
1	LPI1	Lower page independent block Bit "1"
2	LPI2	Lower page independent block Bit "2"
3	LPI3	Lower page independent block Bit "3"
4	UPI0	Upper page independent block Bit "0"
5	UPI1	Upper page independent block Bit "1"
6	UPI2	Upper page independent block Bit "2"
7	UPI3	Upper page independent block Bit "3"
8	DB0	Number of memory banks Bit "0"
9	DB1	Number of memory banks Bit "1"

Page independent block bits also help provide memory management for MC6809E systems and are explained later.

DB0 and DB1 indicate the number of dynamic RAM banks controlled by RMI. This information is used to enable $\overline{CAS}_n$ outputs. The meaning of DB0 and DB1 is encoded as indicated in Table 13.

TABLE 10. REGISTER 4

Bit No.	Name	Function
0		Used only at reset
1		Used only at reset
2		Used only at reset
3		Used only at reset
4	MODE0	Memory cycle type Bit "0"
5	MODE1	Memory cycle type Bit "1"
6	MODE2	Memory cycle type Bit "2"
7	UF	Unfolded control register map
8	MAPA	Memory map select
9	$MACH_2$	Machine 2 mode

The mode bits define what operations will take place in the next memory cycle. The coding of those bits is shown in Table 14. The type of memory cycle to be performed is determined by RMC and will depend on the video line time and the display mode in use. For more information on memory cycle types, consult the RMS users manual.

The $MACH_2$ bit enables the RMS to operate in a mode which is backwards compatible to the MC6883/MC6847 chip set. While operating in the Machine 2 mode ($MACH_2$ = HIGH), the RMS is MC6883/MC6847 backwards compatible. When operating in the Machine 1 mode ($MACH_2$ = LOW), the full advanced capabilities of the RMS may be realized. This allows new software to make use of advanced features without obsoleting the existing software base.

The RMI uses the $MACH_2$ bit along with the map type, MAPA bit (TY bit in Machine 2) and unfolded map, UF bit, to select between various system memory maps. The existence of different user selectable memory maps gives the designer options on where and how much RAM, ROM and I/O are included in a system. The logical address of control registers is also affected by memory map selection.

The memory maps supported by RMS are shown in Tables 3 through 6. For more information on RMS memory maps, consult the users manual.

The four least significant bits in Table 10 (Control Register 4) are used by the reset circuitry. They define the type of MPU and number of lines on the video display. See the section on Reset and Initialization for more details.

TABLE 12. MTYP CODING BITS

MTYP				
3	2	1	0	Meaning
0	0	0	0	16K x 1 DRAM's, 8 bits wide
0	0	0	1	16K x 4 DRAM's, 8 bits wide
0	0	1	0	64K x 1 DRAM's, 8 bits wide
0	0	1	1	Reserved
0	1	0	0	256K x 1 DRAM's, 8 bits wide
0	1	0	1	Reserved
0	1	1	0	Reserved
0	1	1	1	Reserved
1	0	0	0	16K x 1 DRAM's, 16 bits wide
1	0	0	1	16K x 4 DRAM's, 16 bits wide
1	0	1	0	64K x 4 DRAM's, 16 bits wide
1	0	1	1	Reserved
1	1	0	0	256K x 1 DRAM's, 16 bits wide
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

ADDRESS LATCHES

This block latches HIGH and LOW MPU and video display addresses. The multiplexed MPU address is placed on the X-bus when $\overline{ADEN}$ is LOW. The falling and rising edges of $\overline{ADSEL}$ latch the HIGH and LOW MPU addresses into the RMI. Video display HIGH and LOW addresses, calculated by RMC, are placed on the X-Bus during MT1 and MT2 respectively. Video address latching occurs on the positive edge of the MT Clock.

TABLE 11. PELs PER HORIZONTAL LINE

$HRES_2$	$HRES_1$	$HRES_0$	Pixels Per Line	HRES Mode
0	0	0	64	0
0	0	1	128	1
0	1	0	256 (Narrow)	2
0	1	1	256 (Wide)	3
1	0	0	320	4
1	0	1	Reserved	5
1	1	0	512	6
1	1	1	640	7

TABLE 13. DYNAMIC RAM BANKS CONTROLLED BY RMI

DB0	DB1	No. Banks
0	0	1
0	1	2
1	0	Reserved
1	1	4

TABLE 14. MODE BITS

MODE2	MODE1	MODE0	Cycle Type
0	0	0	MPU & single $\overline{CAS}$ display access
0	0	1	MPU & double $\overline{CAS}$ display access
0	1	0	MPU & four $\overline{CAS}$ display access
0	1	1	MPU & two refresh cycles
1	0	0	Triple refresh cycles
1	0	1	Four $\overline{CAS}$ display only
1	1	0	MPU only
1	1	1	Reserved

MC6809E Memory Manager

This logic block enables the MC6809E (which by itself can address only 64K of memory) to utilize up to the full one megabyte of memory supported by RMS. RMI utilizes several sets of control bits to support memory management. The function of each of these is described below.

The first set of control bits, the paging bits, define which 64K block of RAM the MPU is accessing at any point in time. These bits, PG_0 to PG_3 become the most significant MPU address bits (A_{16}–A_{19}). When combined with the 16 MC6809E address bits (A_0–A_{15}), they form a 20-bit address capable of accessing 1 Mbyte.

The lower and upper page independent block control bits, LPI_{0-3} and UPI_{0-3}, define sections of RAM that permanently reside at the bottom or top of the MPU's 64K address space. These blocks allow the MPU to address memory at the bottom or top of the RMS physical memory regardless of the value of the paging bits. The lower page independent block is normally used for scratch RAM while the upper page independent block is normally used for control registers, I/O, and possibly some ROM. The LPI_{0-3} and UPI_{0-3} bits define the size of lower and upper Page Independent Blocks as shown in Table 15.

The SWAP bit in the RMI is used to invert the meaning of MPU address bit A_{15}. This feature can be used to enable the MPU to access DRAM locations that are hidden underneath the upper and lower Page Independent Blocks. This is illustrated in Figure 4.

TABLE 15. LOWER and UPPER PAGE INDEPENDENT BLOCKS

Bit 2	Bit 1	Bit 0	PIB Size
0	0	0	256 bytes
0	0	1	512 bytes
0	1	0	1 Kbyte
0	1	1	2 Kbytes
1	0	0	4 Kbytes
1	0	1	8 Kbytes
1	1	0	16 Kbytes
1	1	1	32 Kbytes

Address Counter

The address counter increments the lower address bits in order to perform multiple $\overline{CAS}$ video accesses and multiple $\overline{RAS}$ refresh cycles. For other types of memory access, the counter is transparent.

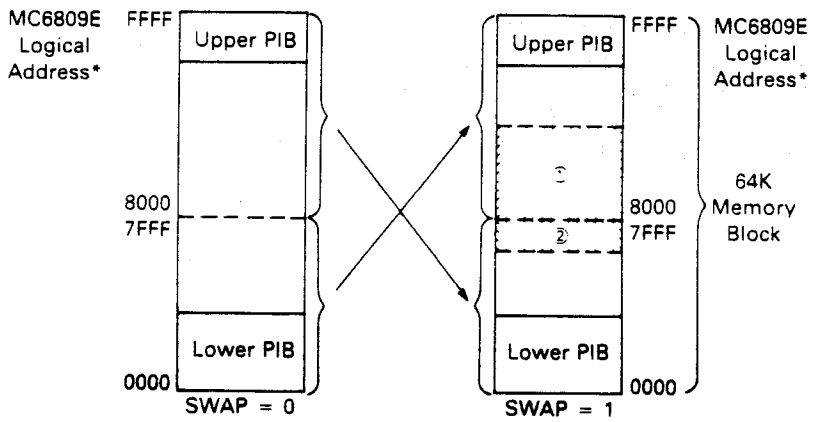
DRAM Timing Control

This block generates all timing necessary to access DRAM. The timing is dependent on the memory cycle type which is specified by control words in the previous memory cycle.

Z-Bus Control and Address Multiplexer

This logic controls the multiplexing of information on the Z-bus (Memory Address) outputs. The multiplexer selects information from the MC6809E MEMORY MANAGER, the ADDRESS COUNTER or the X-Bus depending upon the type of memory access and the state of internal timing logic.

FIGURE 4 — USING THE SWAP BIT



1. Memory hidden by lower Page Independent Block (PIB).
2. Memory hidden by upper PIB.

*Physical address depends on PAGE bits.

RESET AND INITIALIZATION

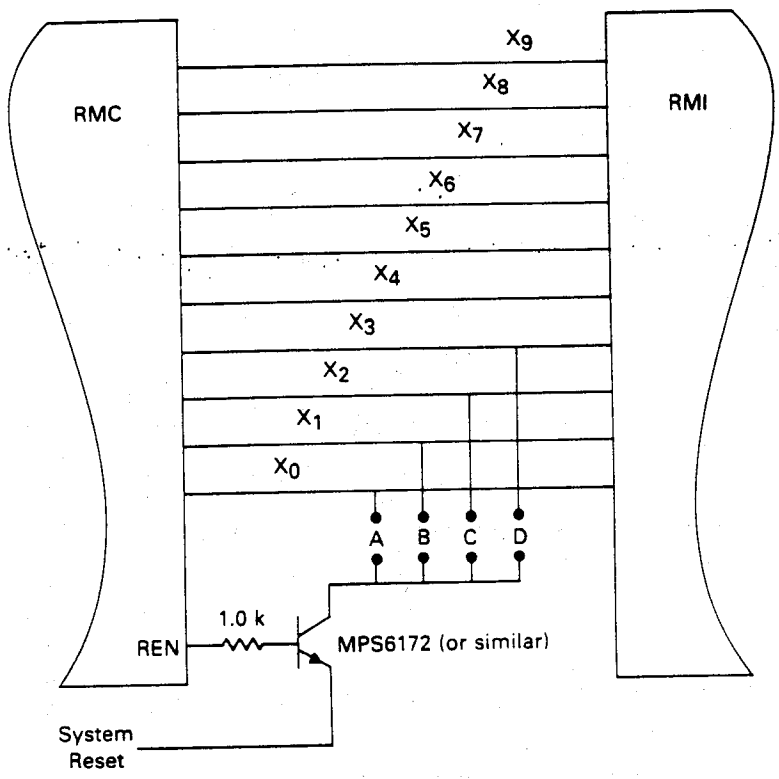
RMI contains circuitry to reset itself at power up. This circuit is entirely self contained and requires no external components.

The RMI requires a certain amount of initial information, which is supplied via the X-bus and a minimal amount of external circuitry as shown in Figure 5. Reset circuitry is arranged so that if the MPU reset line is active, and REN is active, then one of the four X-Bus lines will be low. This signals the RMS that a reset has been requested. The RMS will be initialized differently depending on which X-Bus line is used.

The selection of 625 (PAL) or 525 (NTSC) line video timing will also select the proper divide circuit for generating color subcarrier (CSC) and screen refresh rate. See Table 1 for details.

A system reset may occur at times other than application of power. REN will become active during every MT_6 time. Both RMC and RMI will be sampling the X-Bus then, and if any of the four X-Bus lines go low, they will reset themselves. The conditions defined after a reset by means of REN are the same as after a power-up reset.

FIGURE 5 — X-BUS RESET



Use Jumper A for MC6809E MPU and 625 line (PAL) video timing.
Use Jumper B for MC6809E MPU and 525 line (NTSC) video timing.
Use Jumper C for MC68000 family MPU and 625 line (PAL) video timing.
Use Jumper D for MC68000 family MPU and 525 line (NTSC) video timing.

FIGURE 6 — MC6809E SYSTEM BLOCK DIAGRAM

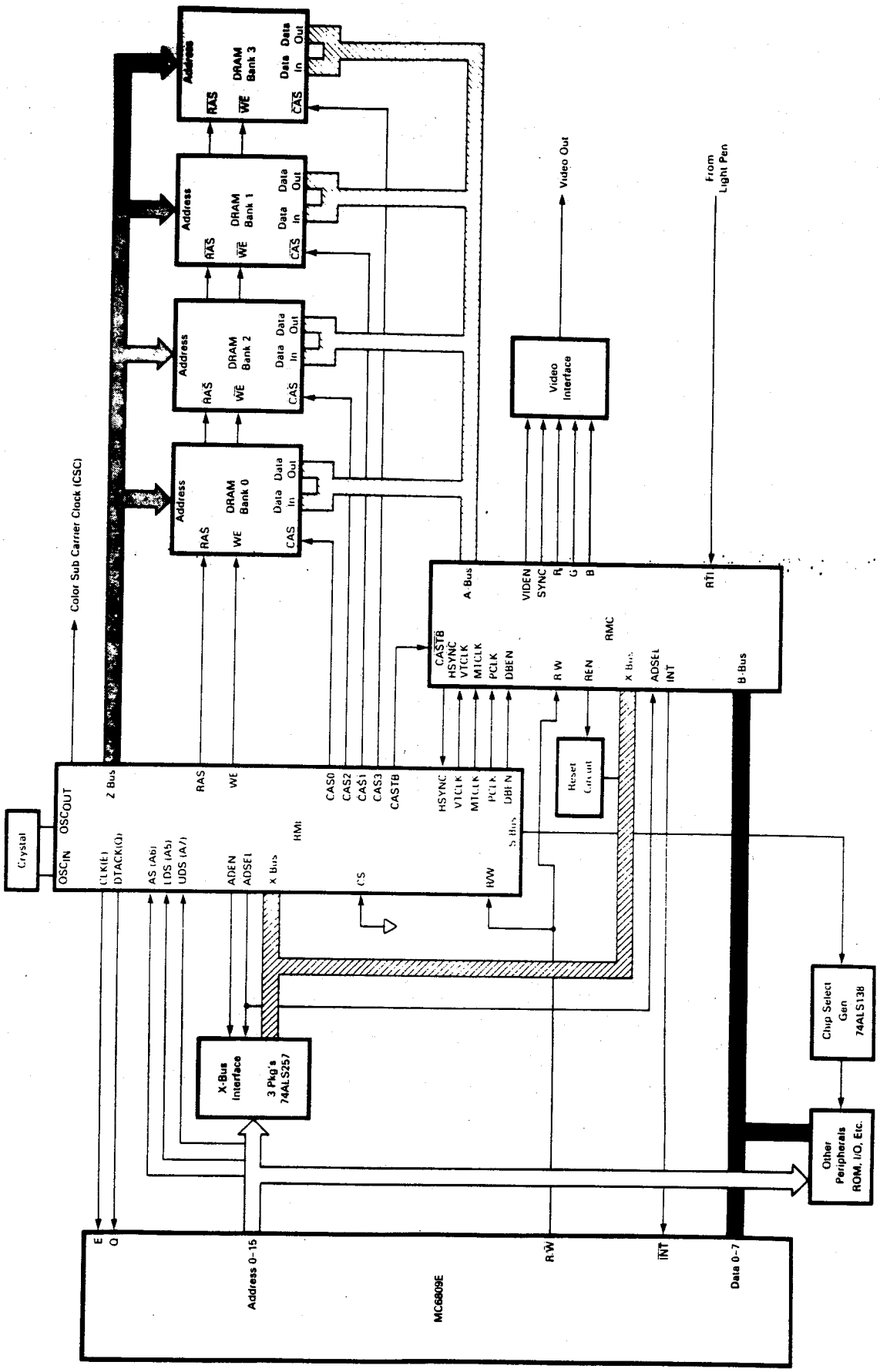


FIGURE 7 — MC68000 SYSTEM BLOCK DIAGRAM

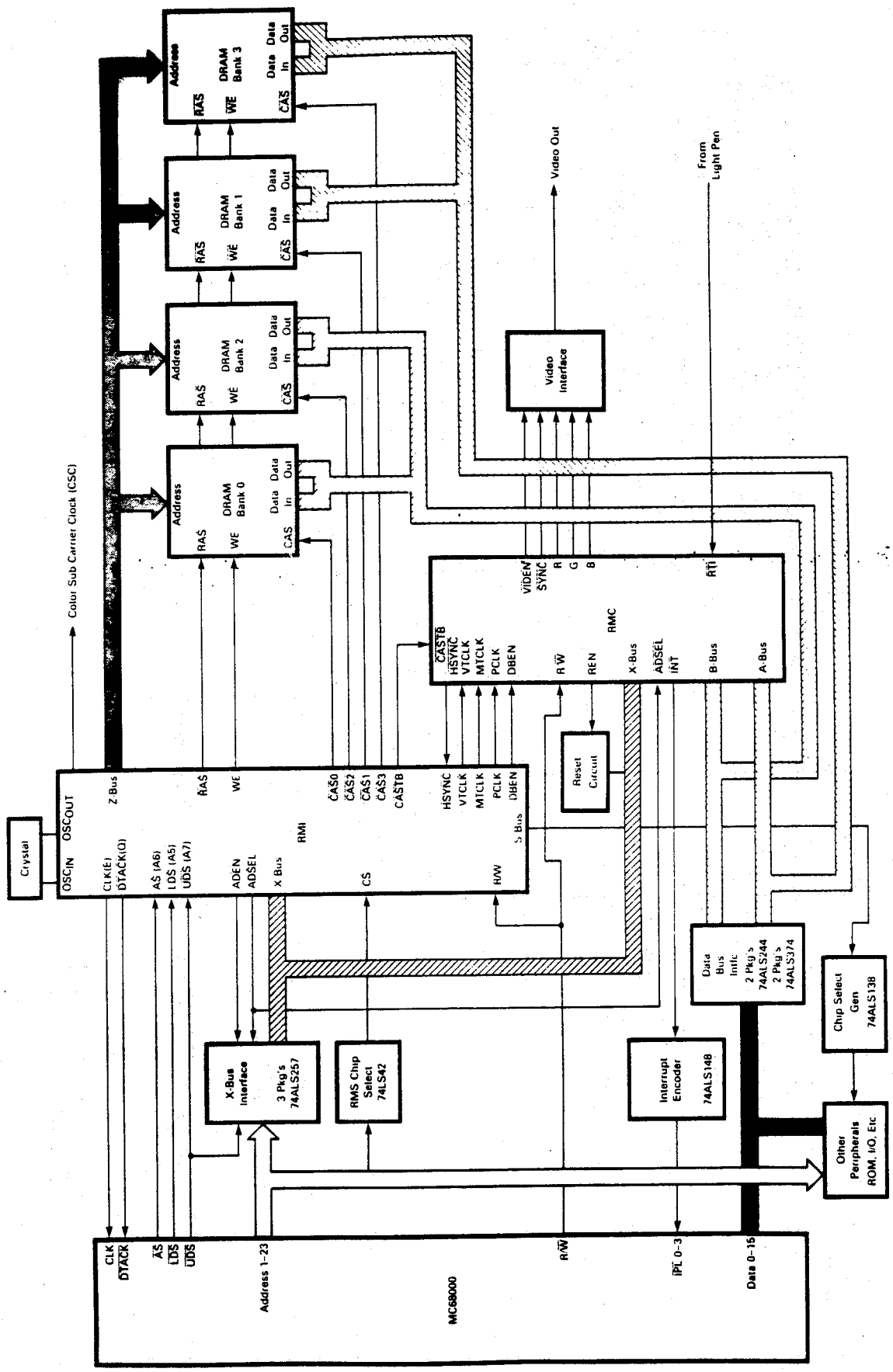


FIGURE 8 — MC68008 SYSTEM BLOCK DIAGRAM

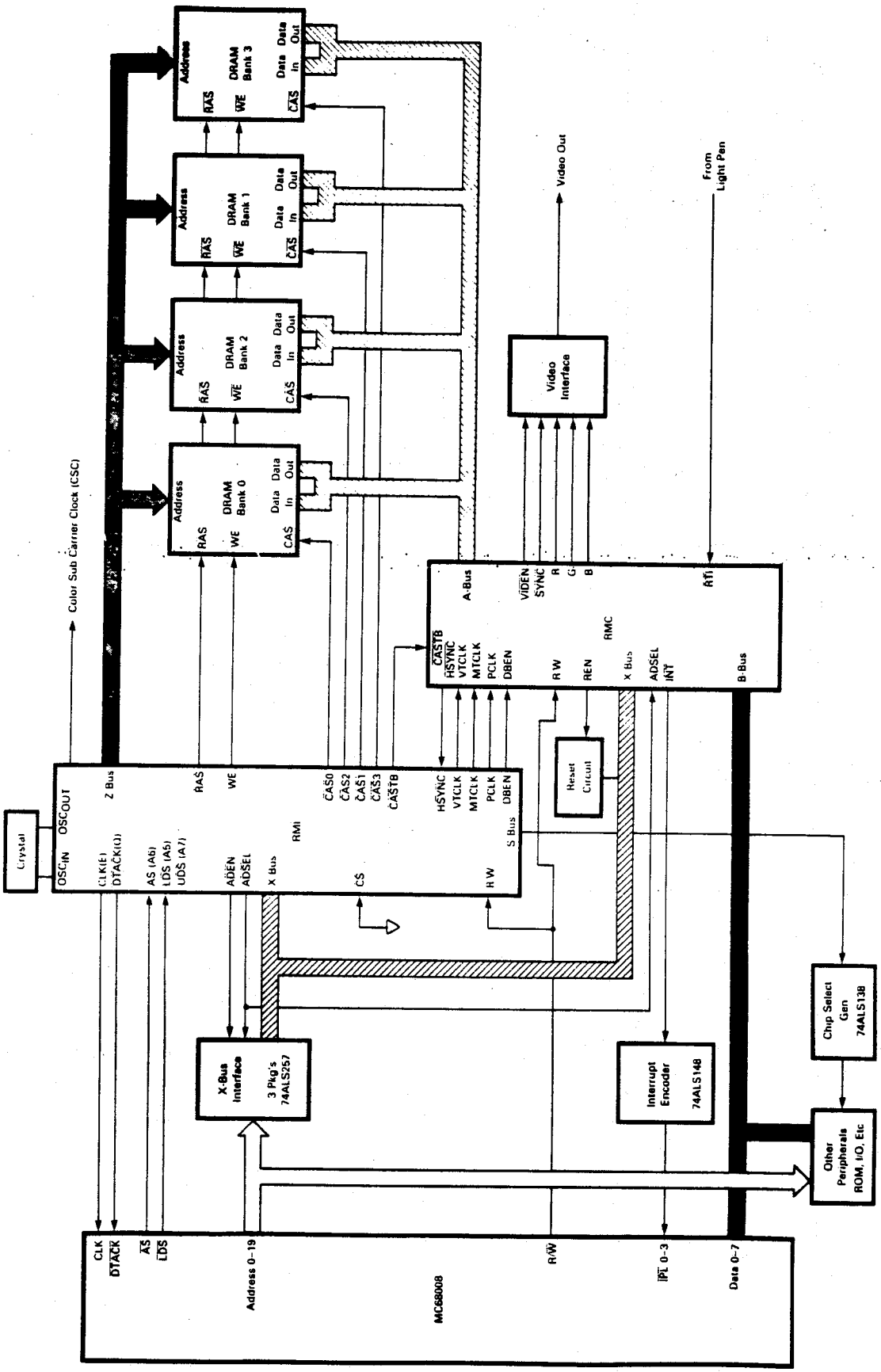


FIGURE 9 — MTCLK AND PCLK versus HRES MODES

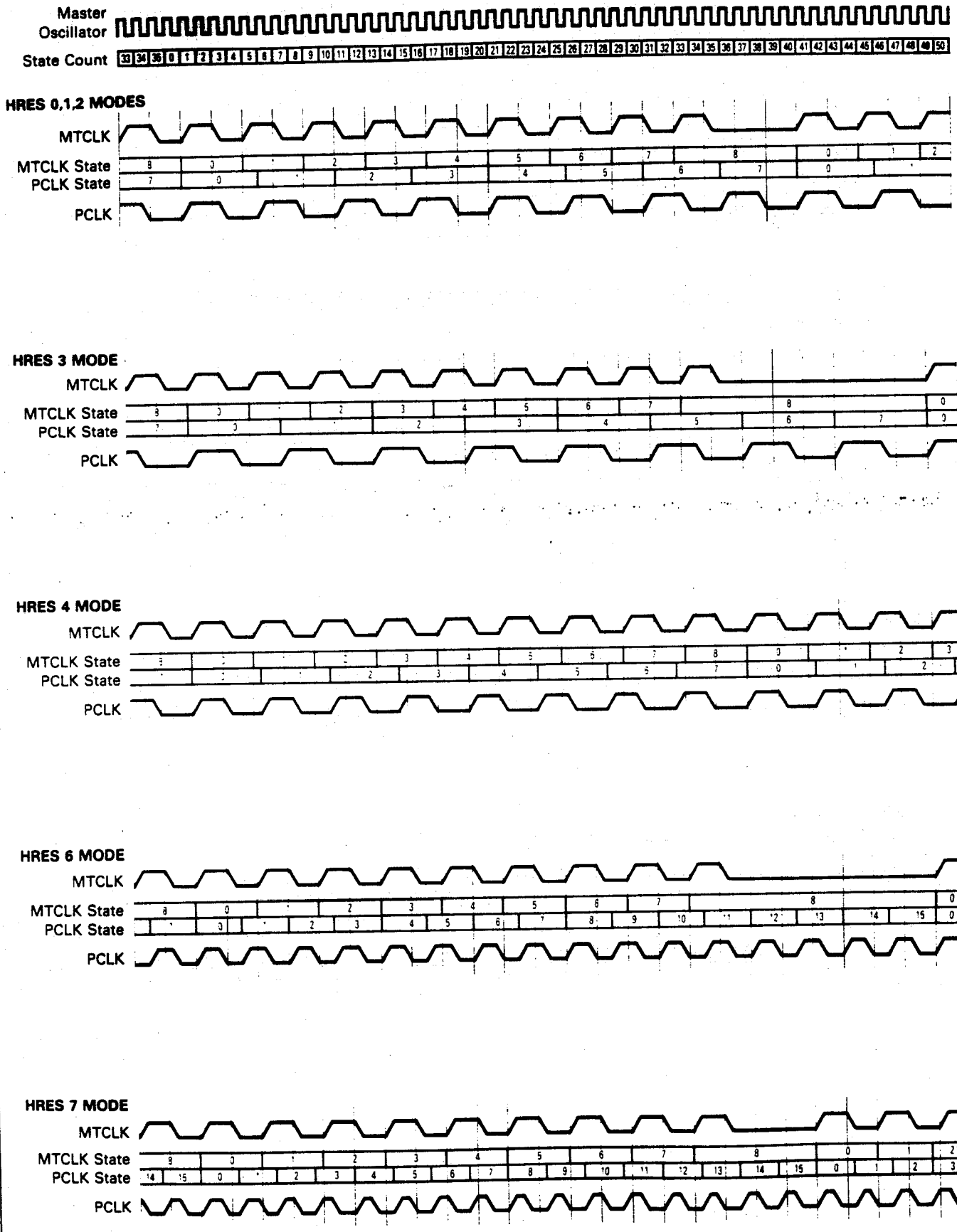
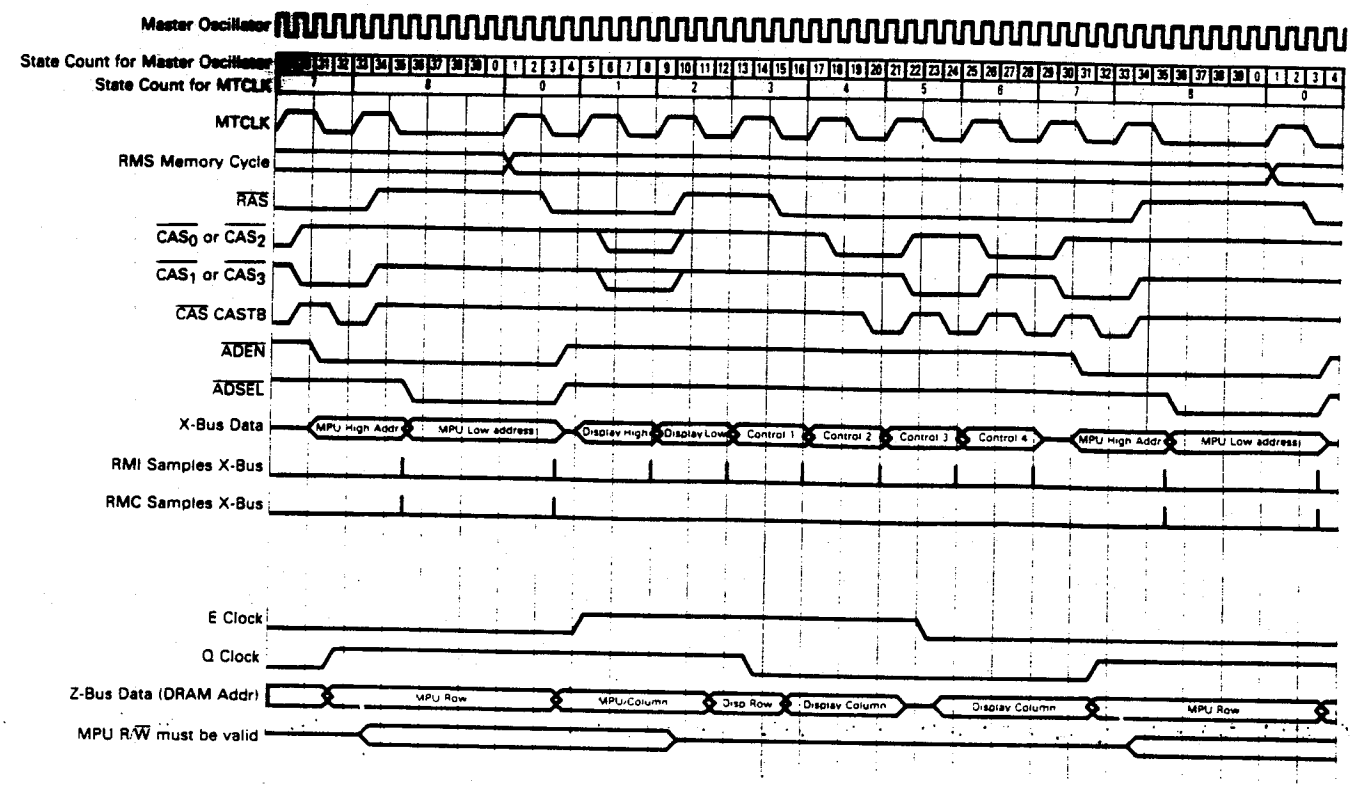
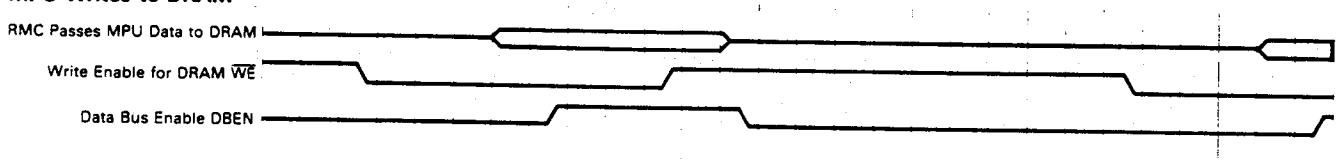


FIGURE 10 — MC6809E X-BUS TIMING FOR HRES 0,1,2,7



MPU Writes to DRAM



MPU Reads from DRAM

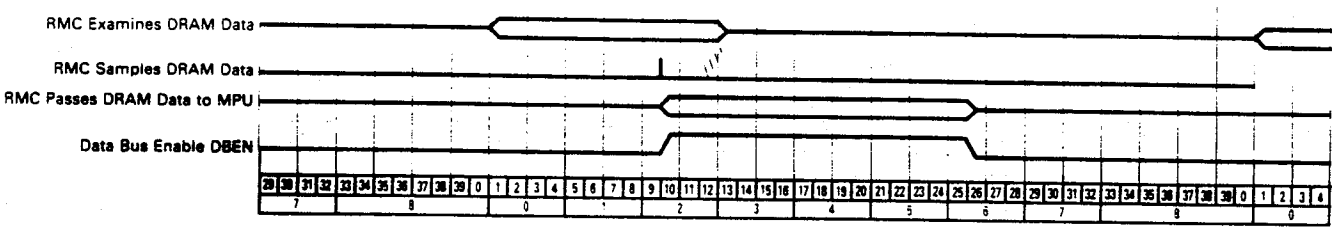


FIGURE 11 — MC6809E X-BUS TIMING FOR HRES 3,6

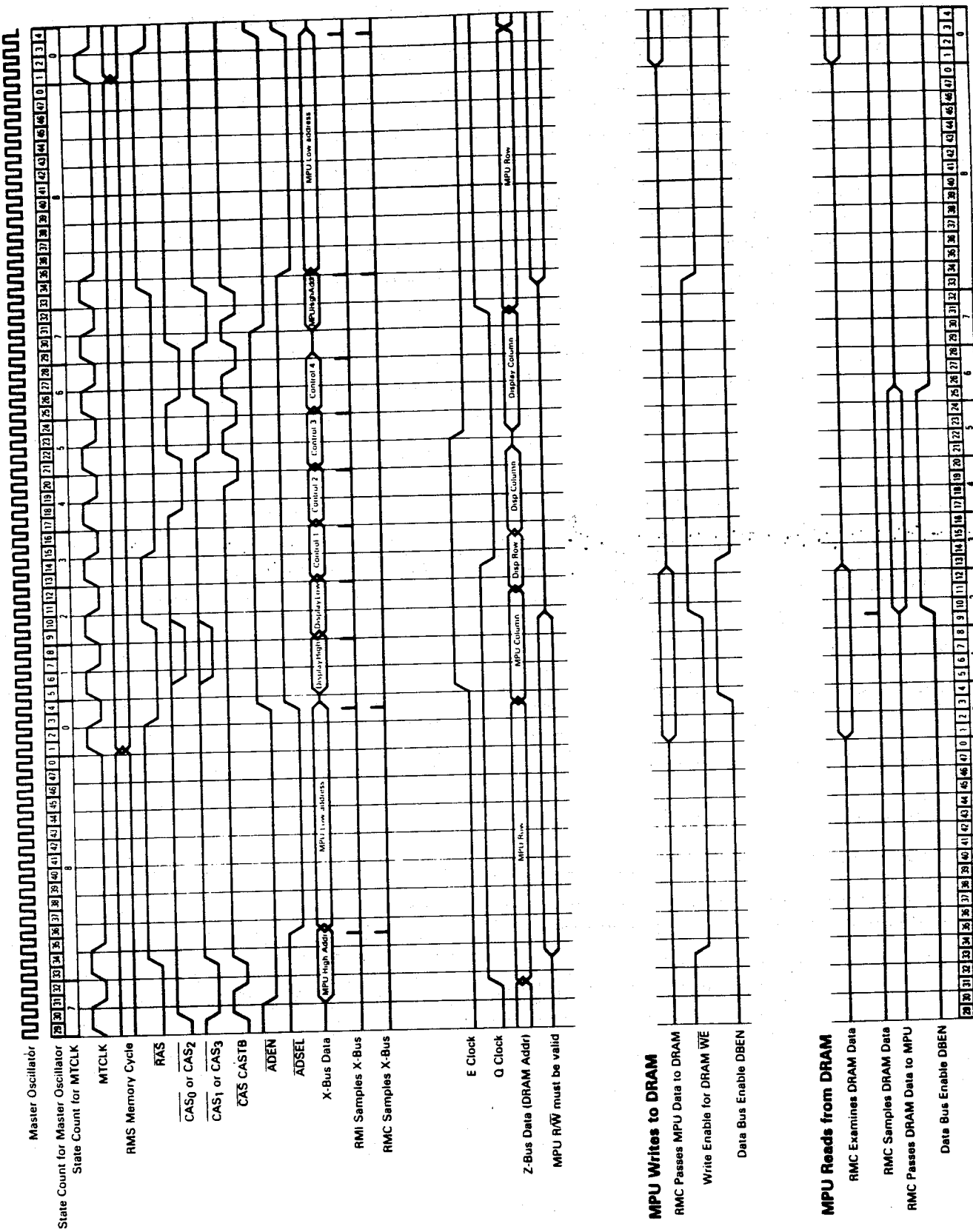
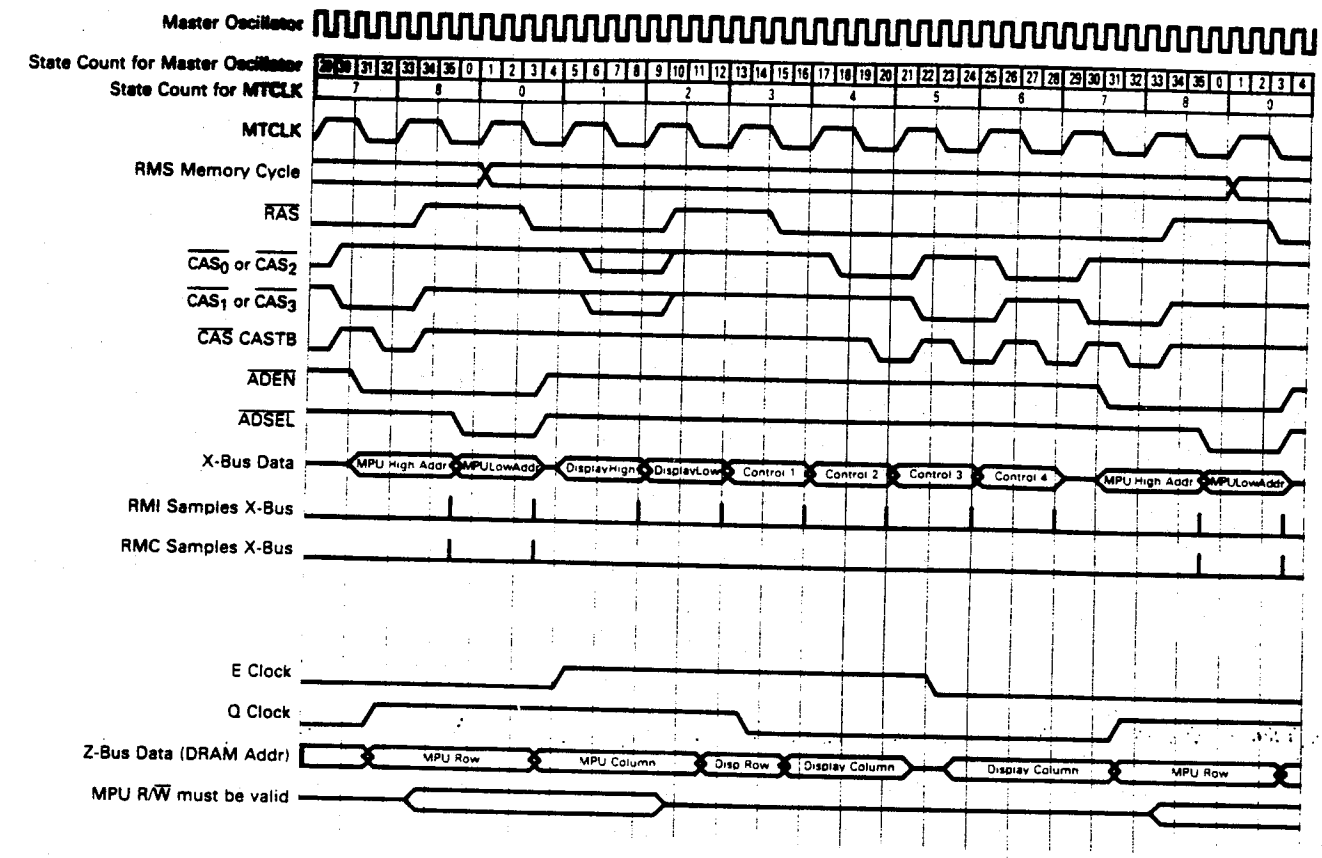
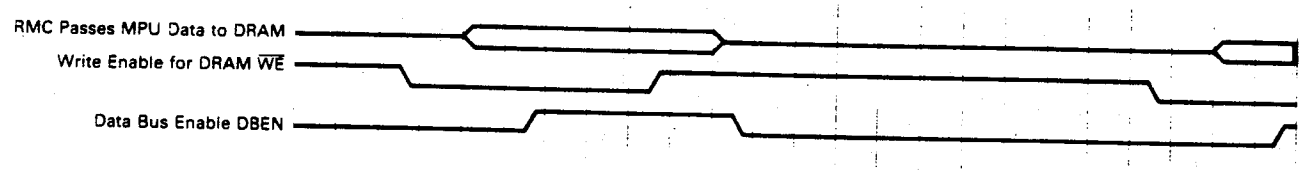


FIGURE 12 — MC6809E X-BUS TIMING FOR HRES 4



MPU Writes to DRAM



MPU Reads from DRAM

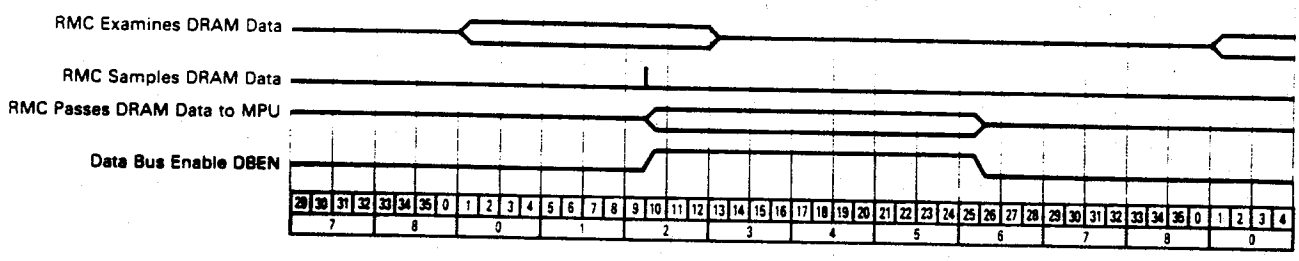
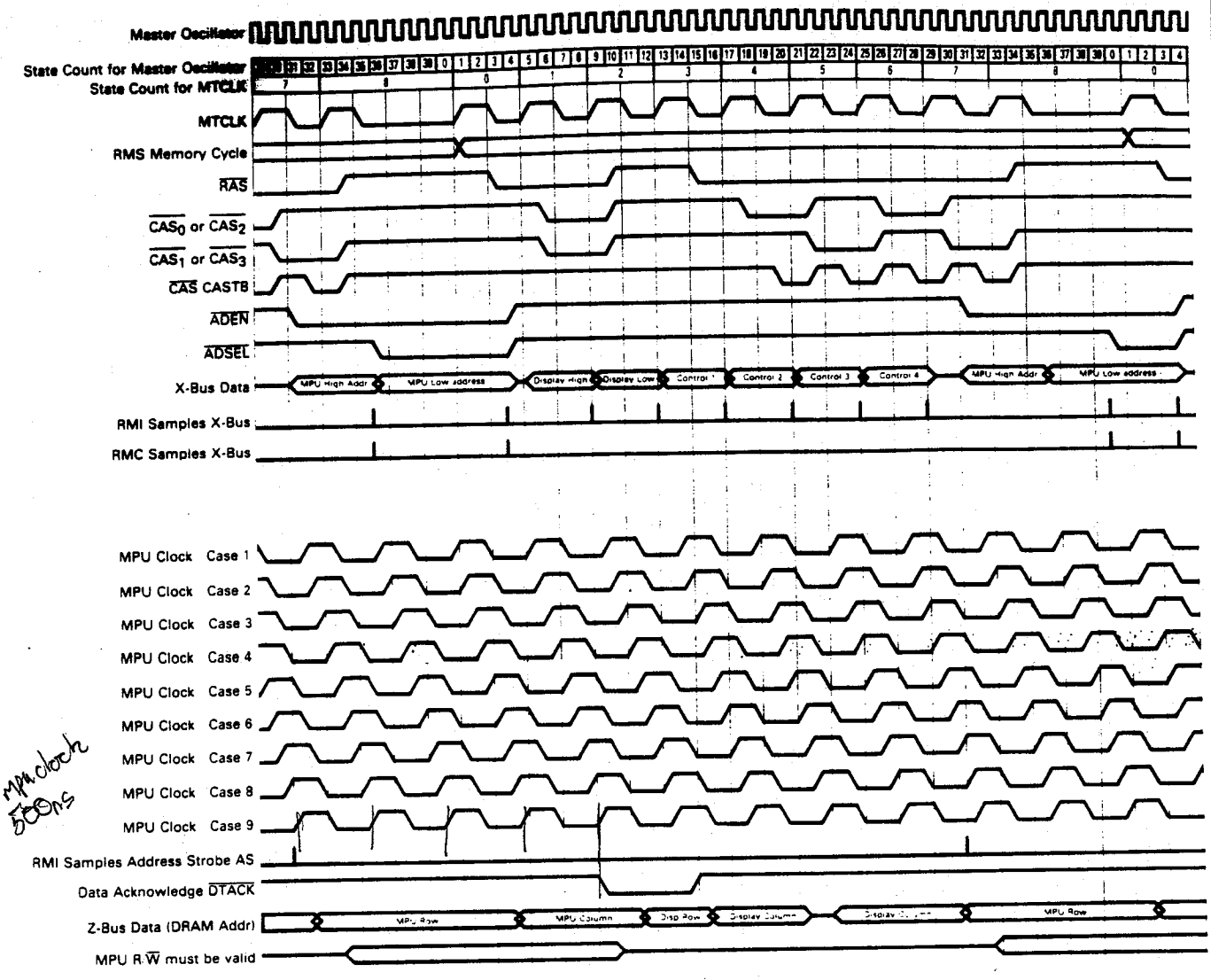
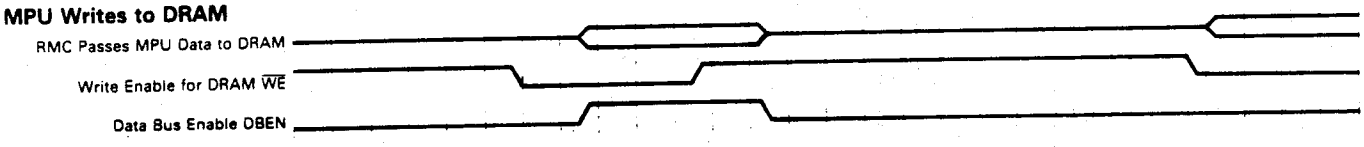


FIGURE 13 — MC68000/8 X-BUS TIMING FOR HRES 0,1,2,7



4x MPU clock 500ns

MPU Writes to DRAM



MPU Reads from DRAM

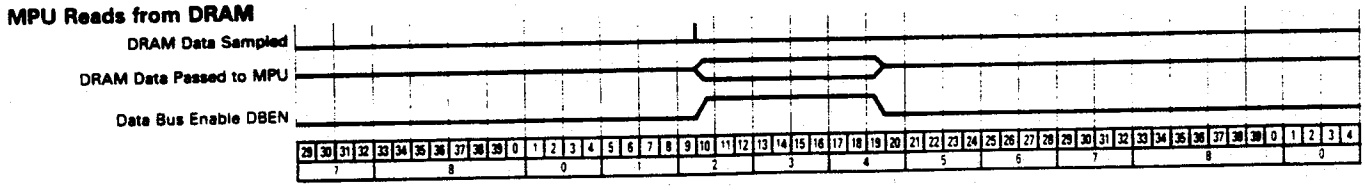


FIGURE 14 — MC68000/8 X-BUS TIMING FOR HRES 3,6

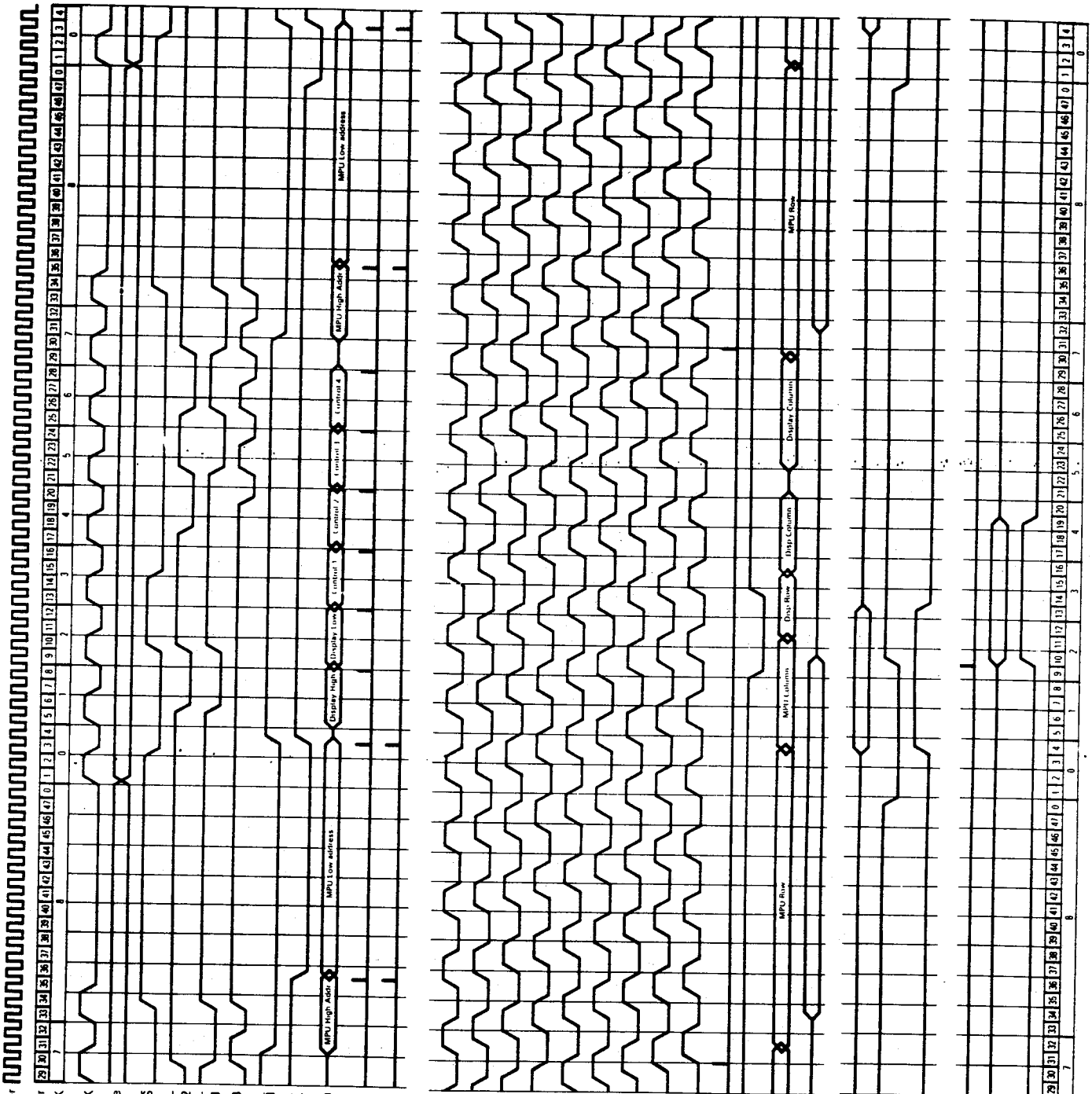
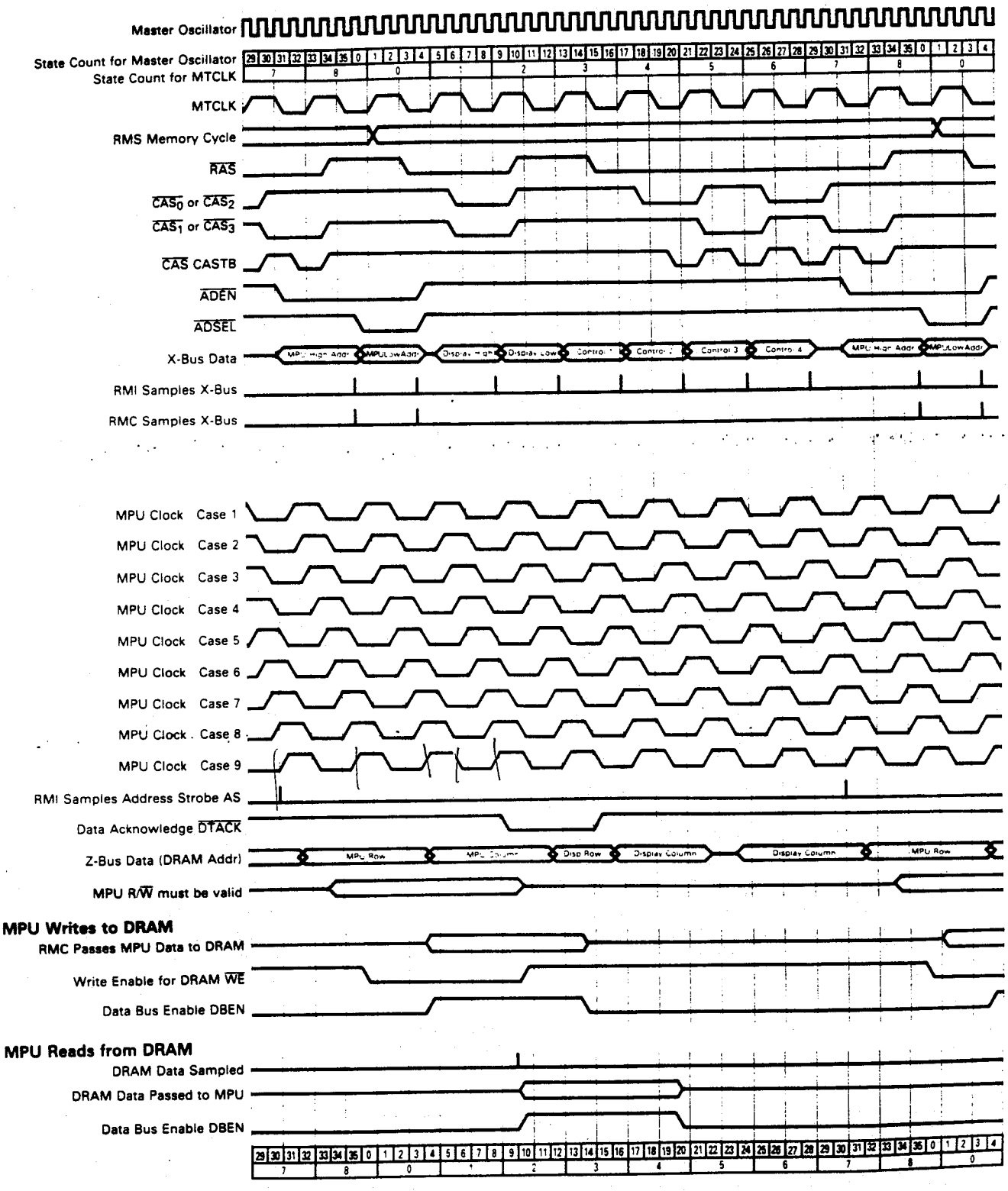
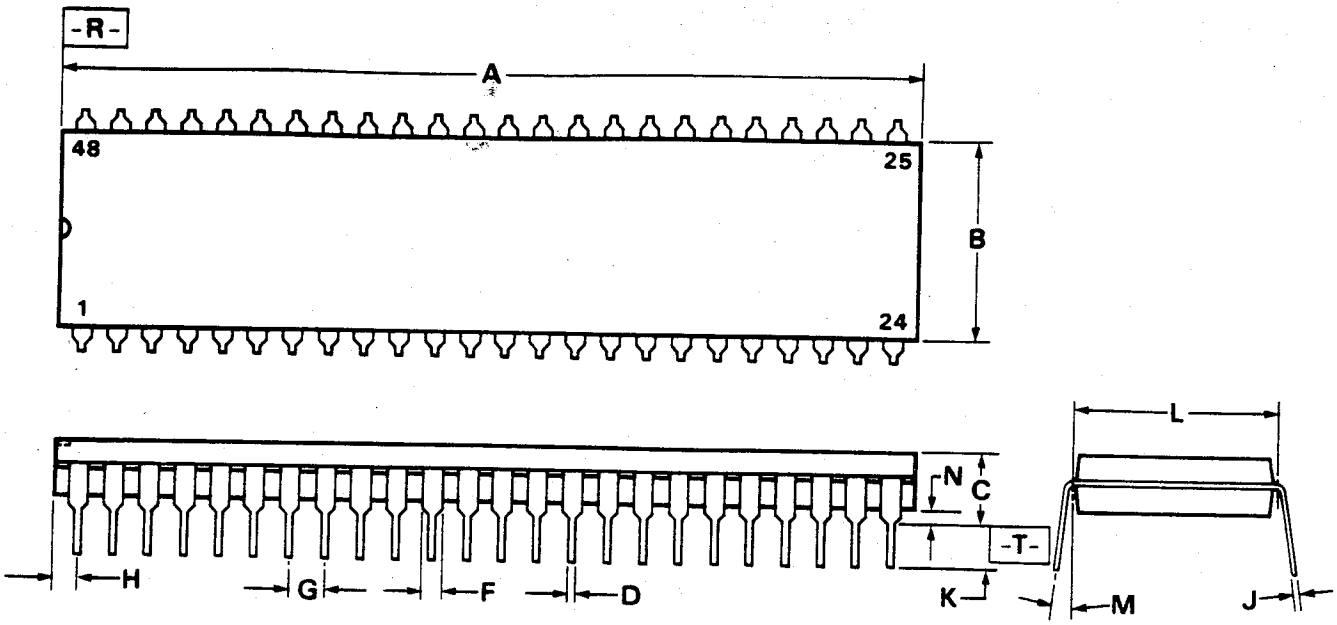


FIGURE 15 — MC68000/8 X-BUS TIMING FOR HRES 4





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	61.34	62.10	2.415	2.445
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.55	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.79 BSC		0.070 BSC	
J	0.20	0.38	0.008	0.015
K	2.92	3.42	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

NOTES:

1. -R- IS END OF PACKAGE DATUM PLANE. -T- IS BOTH A DATUM AND SEATING PLANE.
2. POSITIONAL TOLERANCE FOR LEADS 1 AND 48:
   ⌖ | 0.51 (0.020) | T | B Ⓜ | R
   POSITIONAL TOLERANCE FOR LEAD PATTERN:
   ⌖ | 0.25 (0.010) | T | B Ⓜ
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. DIMENSION L IS TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1982.
6. CONTROLLING DIMENSION: INCH.

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ADI 1115