AN18.15

PCB Design Guidelines for QFN and DQFN Packages

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INTRODUCTION

This application note provides specific guidelines for Printed Circuit Board (PCB) layout considerations and related solder stencil considerations when implementing Microchip products in Quad Flat No-lead (QFN) and Dual Quad Flat No-lead (DQFN) packages. This application note is intended for users who are familiar with PCB design, including signal integrity and thermal management implementation concepts.

Successful implementation of QFN-style packages, including QFNs and DQFNs, requires special consideration for PCB Footprint design, PCB layout, and solder paste stencil design. This application note describes these important considerations.

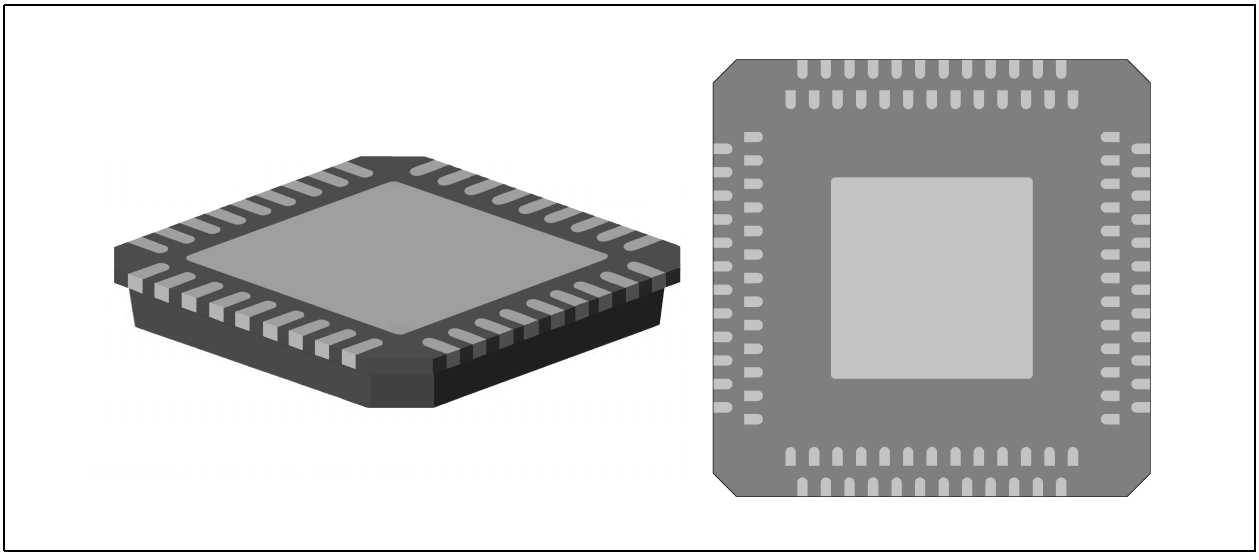
The following guidelines are based on Microchip's experience and knowledge, and may be accepted or rejected. Microchip does not guarantee any design. The user is ultimately responsible for determining the suitability of their own design. Microchip suggests that the user's PCB fabricator and PCBA assembler confirm all implementations.

These guidelines for using QFN-style devices supersede prior guidance from Microchip. See *AN2086 - Package Application Note for Dual Row Quad Flat No-Leads (DQFN)* for additional reference.

QFN-STYLE DEVICES

QFN-style packages (see Figure 1) are physically robust and thermally efficient, and they occupy much less PCB space than equivalent QFP-style packages. They typically also have superior lead inductance characteristics. They do present particular design constraints to improve production yield.

FIGURE 1: QFN AND DQFN PACKAGES



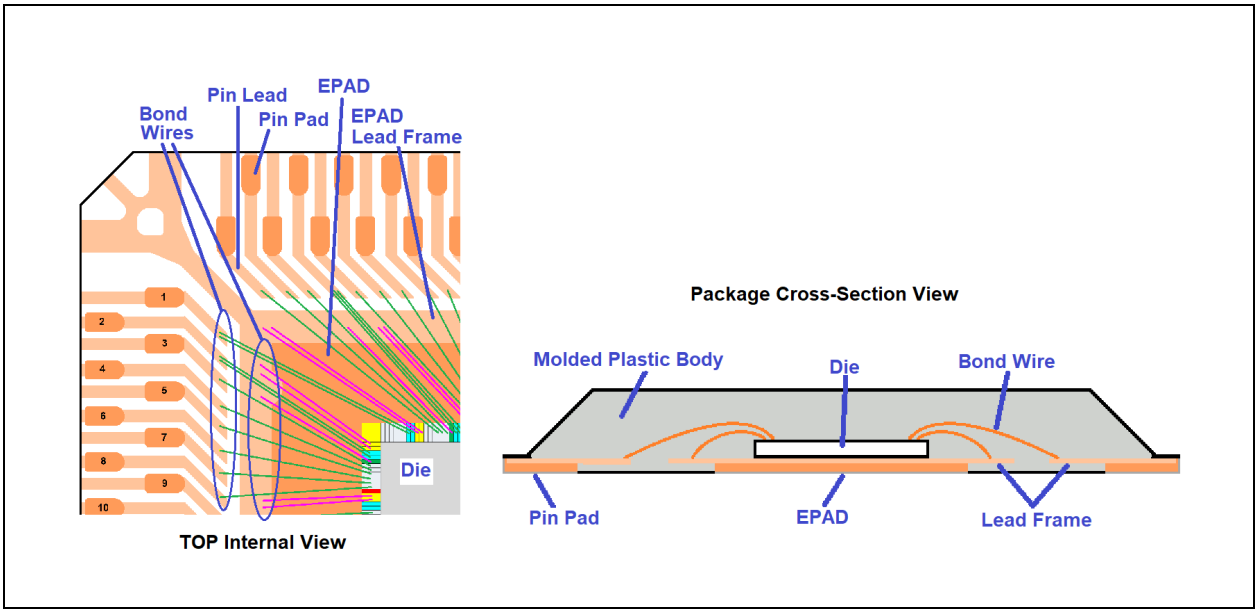
QFN-style packages generally have a single row (QFN) or two rows (DQFN) of perimeter pads around one or more larger center pads ("flag" or "EPAD"), all encapsulated in a plastic body. These packages are surface-mounted to the target system PCB by a solder reflow process.

QFN Device Construction

Figure 2 illustrates the construction of QFN and DQFN devices. The die is attached to the EPAD with thermally conductive adhesive.

Bond wires are connected between the bond sites on the die to the bond sites on the lead frame. These lead frame sites are available for the individual pin pads and for the EPADs.

FIGURE 2: QFN AND DQFN CONSTRUCTION



The perimeter pads are typically used for signal assignment.

The EPAD is used for two things: as the primary thermal conduction path to remove package heat, *and for device VSS (GND)*. This is standard for Microchip QFN and DQFN packages.

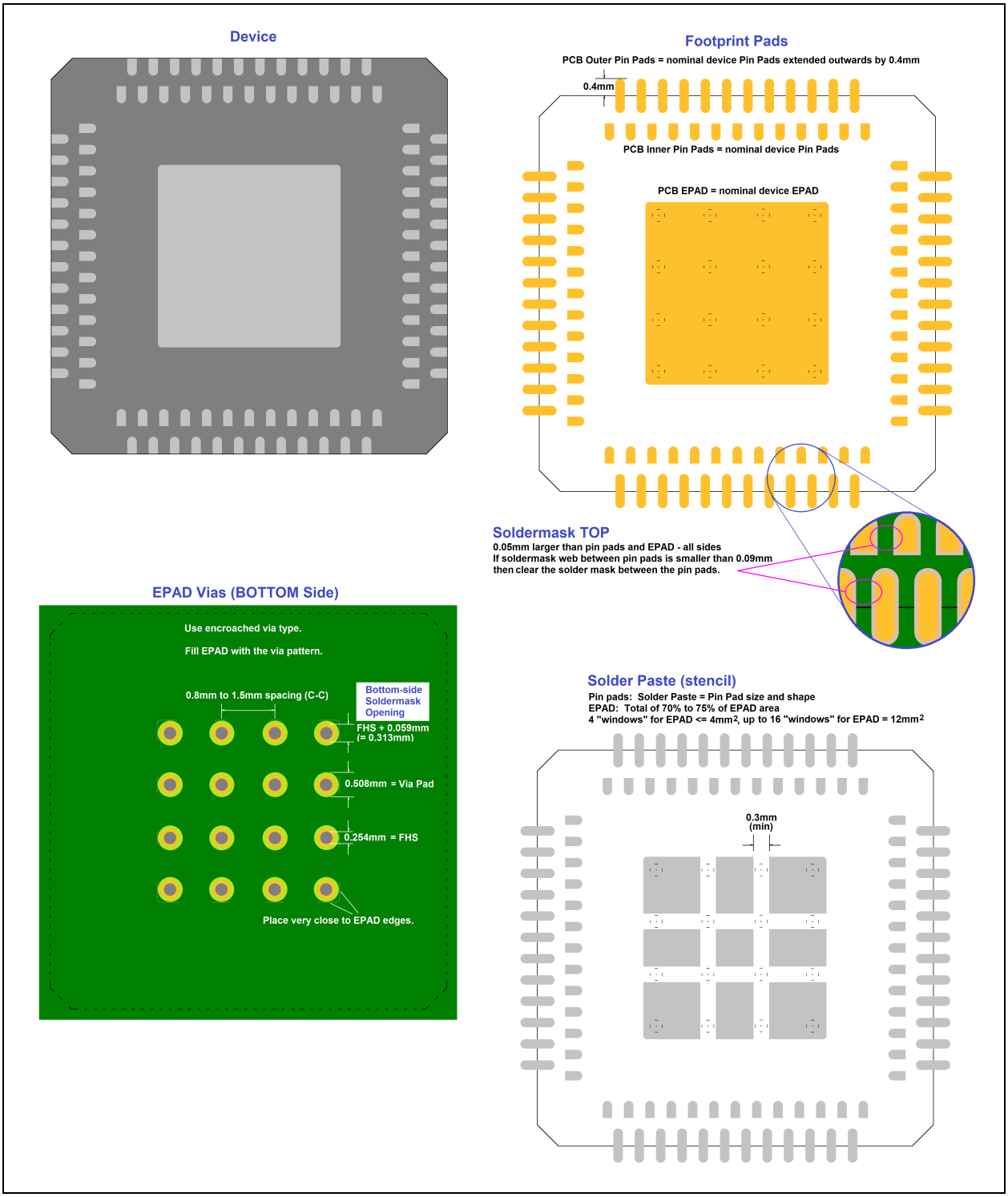
Critical Note:	Many Microchip QFN devices use the EPAD as either the primary connection or the *ONLY* connection to the device's VSS (GND) signal, as well as the primary thermal conduction path. Good connection to the PCB's VSS is crucial for proper device function.

Some Microchip devices, especially regulators, may have signals other than VSS on some EPADs. Carefully note this from the data sheet and make proper connections accordingly.

QFN AND DQFN SOLUTIONS

Figure 3 illustrates the summary of Microchip's guidance for using QFN-style packages.

FIGURE 3: MICROCHIP'S STANDARD QFN/DQFN DESIGN SOLUTION SET



QFN AND DQFN ISSUES

PCB Footprint Issues

If the PCB footprint pads do not closely match the device pads in size and shape, the device may not self-center on the footprint correctly. This includes the EPADs and the pin pads.

The outer row of pin pads should be extended to allow for inspection, pad wetting, and rework purposes. The extension should be done with round-ended pads to reduce solder shorts.

1. Make the PCB EPADs equal to the nominal device EPADs.
2. Make the PCB pin pads equal to the nominal pad device pad.
3. Extend the outer row PCB pads by 0.4 mm with rounded ends.

Soldermask Issues

The Soldermask-Top layer for the side of the board where the QFN-style device is mounted (top-side) needs some adjustment compared to other SMT devices.

Expand the Soldermask pads to be 0.05 mm larger than the footprint pads on all sides.

If the resulting web of Soldermask between the pin pads is less than 0.09 mm, then remove the webs between the pads. See **Section "EPAD Vias"** for treatment of the Soldermask-Bottom (opposite-side).

Solder Paste Stencil Issues

PIN PADS

Create the solder paste stencil opening for the pin pads the same as with other SMT pin pads; make them identical to the pin pads.

EPADS

The EPADs of QFN-style devices have specific solder paste stencil needs.

During soldering, the QFN device will float too high if too much solder paste is deposited under the device. This may not allow the PCB perimeter pad solder to reach the device pins, causing signal opens. This excessive "float" may also inhibit proper device alignment.

Alternately, the QFN will sink too low if too little solder paste is under the EPAD. This can cause the perimeter pads to "squeeze-out" solder, causing shorts between adjacent signal pads or between the EPAD and signal pads.

Depending on the size of the EPAD and the type of vias used to connect the EPAD to the VSS (GND) layers, the total area of the stencil opening should be between 65% and 90% of the EPAD area. *When using encroached-style EPAD vias, target 75% of the EPAD area.*

The most effective pattern for the EPAD stencil openings is a set of symmetrical "windows", as illustrated in Figure 3.

The stencil web between "windows" should be 0.3 mm at minimum to extend the life of the stencil.

EPAD Via Issues

The vias that are used within the EPAD affect device function, signal integrity, thermal performance, soldering and stencil development, soldermask, routing and copper pours, and related PCB and assembly costs. See **Section "EPAD Vias"** for more details.

Routing Issues

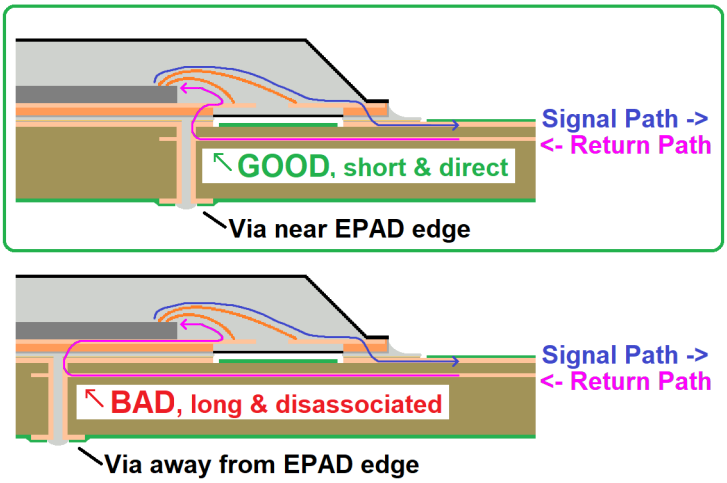
Controlling the routing of signals near and under QFN-style devices can significantly improve yields through fabrication and assembly. See **Section "Routing Issues"** for more details.

EPAD VIAS

Signal Loop Area

The more vias placed in the EPAD near the edges, the shorter the return path (GND) loop area to the internal device circuitry will be. Make sure to have complete periphery via coverage to reduce signal return lengths for the device.

FIGURE 4: SIGNAL LOOP CONTROL WITH EPAD VIA PLACEMENT



Thermal Performance

The more vias placed within the flag, the better the thermal conduction through the board and to internal VSS (GND) planes will be. Thermal connection to thermal radiation and conduction floods or features on the opposite side of the PCB is likewise improved with a higher via count in the EPAD.

Use as many vias as can practically fit within the EPAD. For example, this number should be at least eight vias for 36-pin devices and at least 16 vias for 6x6 mm EPADs. For best results, use vias with a finished hole size (FHS) of 0.25 mm to 0.30 mm and a pad size of 0.5 mm to 0.6 mm. Spacing the vias by 0.8 mm to 1.5 mm (center-to-center) allows floods and traces to go between them as needed on other copper layers.

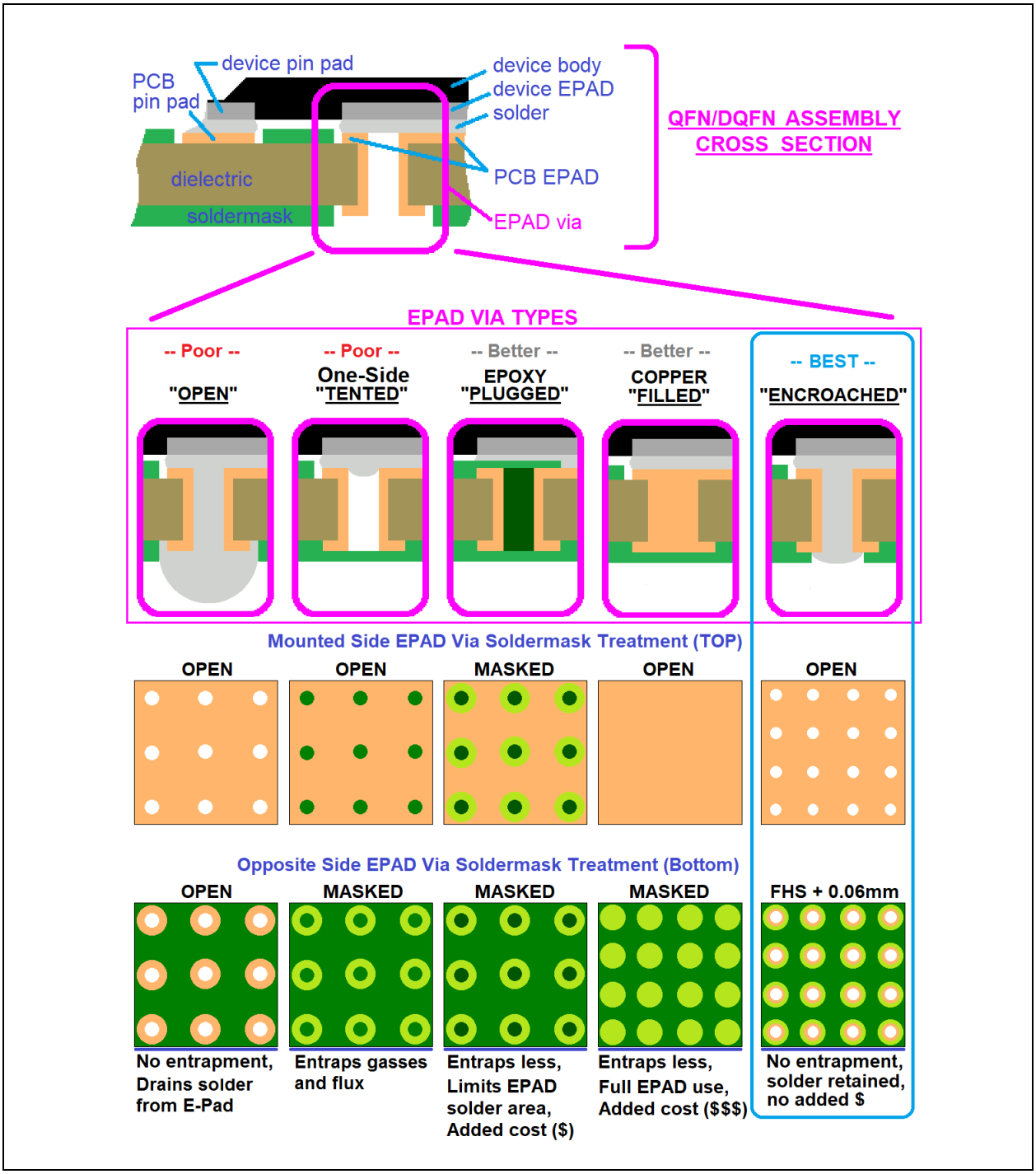
EPAD Via Types

There are five typical types of treatment for vias within EPADs, as shown in Figure 5.

- OPEN
- One-side TENTED
- Epoxy PLUGGED
- Copper FILLED
- ENCROACHED

Two of these types can cause major assembly problems, and two of the others add extra fabrication costs and can still cause assembly issues. Microchip recommends using “Encroached” vias, per IPC-7093, (Soldermask-Top = Open, Soldermask-Bottom = FHS + 0.06 mm).

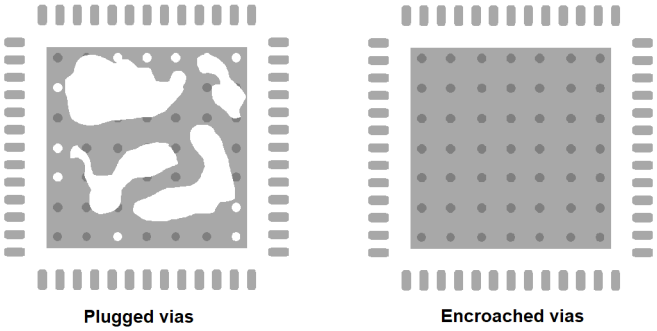
FIGURE 5: TYPICAL VIA TREATMENTS WITHIN EPADS



EPAD Solder Voids

EPADs are prone to solder voids during the attachment process (reflow soldering) due to their relatively large area and position between the device body and the PCB surface, as shown in Figure 6.

FIGURE 6: SIMULATED X-RAY IMAGES OF SOLDERED EPADS



These voids are caused by improper solder paste openings in the solder stencil (“windowing” must be used), by using an improper profile through the reflow oven, or by having trapped flux volatiles or other gases under the EPAD.

Encroached EPAD Vias Address Trapped Gas and Flux

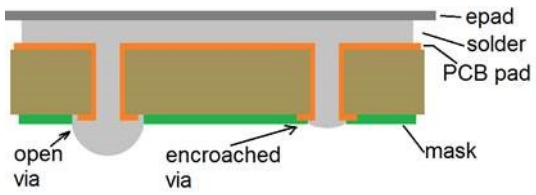
The encroached via concept is one that uses soldermask on the bottom via pad without filling the via’s plated-through hole. Encroachment-type vias have the top-side soldermask open and the bottom-side soldermask opening adjusted, so that it is slightly larger than the via hole size (typically +0.06 mm).

This treatment will permit any trapped flux, gas, or other contaminants to flow out of the via while surface tension keeps the solder from flowing out. Encroached vias also provide more coverage of adjacent bottom-side traces by the bottom-side soldermask.

Encroached Vias Compared to Open Vias

If the mask is opened all the way around an EPAD via (OPEN via), then solder can flow out from under the QFN EPAD onto the bottom-side via pad as a big drop, as in Figure 7. This drop often drips off during the motion of the unit through the reflow oven, pulling solder from the EPAD joint. This solder “scavenging” can make the EPAD connection unreliable and/or tilt the device, making the pin connections unreliable.

FIGURE 7: OPEN VERSUS ENCROACHED EPAD VIA FUNCTION



If the exposed via pad is “encroached” with soldermask, thereby making the soldermask opening smaller and the via pad “mask-defined”, then the volume of solder it will draw is much smaller. This is because of the relationship of the surface tension of melted solder compared to the area of the via pad and the diameter of the via hole. Jostling on the conveyor during production assembly is also considered.

For best results, use vias with an FHS of 0.25 mm to 0.3 mm and a bottom-side soldermask opening of 0.055 mm to 0.075 mm larger than the FHS.

See Figure 3 for Microchip’s typical values.

SOLDER PASTE STENCIL DESIGN

The solder paste stencil is used for applying solder paste to the PCB just prior to placing SMT parts for reflow soldering.

Because EPADs are different than other SMT pads, the stencil openings (also called solder paste openings) must be designed differently.

Pin Pad Solder Paste Design

The pin pad solder paste openings should, by default, be equal to the pad shapes, sizes, and positions as the pads themselves.

EPAD Solder Paste Design

Unlike most SMT solder joints, an EPAD's solder does not have any vertical pad edge to wet and form a fillet with. *Therefore, less solder must be used than with a typical pad to prevent the QFN device from floating too far from the PCB pads.*

Note:	The area of the solder paste openings should be between 65% and 90% of the EPAD area.

An EPAD solder joint is confined between the device body and the PCB surface. Flux volatiles and other gases can be trapped between the device EPAD and the PCB EPAD. This entrapment causes solder voids. (See Figure 6.) *Therefore, channels must be provided between solder paste locations on the EPAD to allow gas to escape during the reflow process.*

Note:	Using encroached EPAD vias also helps with this issue.

The types, sizes, and number of vias under an EPAD will change the ideal amount of solder paste that should be applied to an EPAD. *Therefore, the solder paste openings should be tailored to the EPAD via details used.*

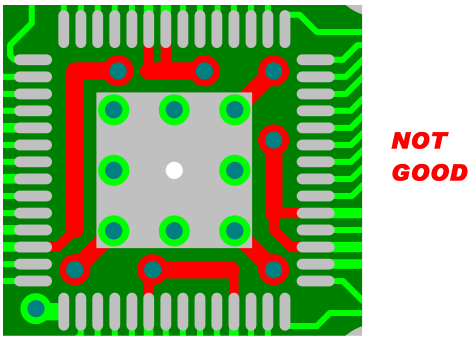
To address these needs, use "windowed" solder paste openings. When using encroached vias in the EPAD, target 70% to 75% of the EPAD area for the solder paste, with a minimum web of 0.3 mm for extended stencil life.

ROUTING ISSUES

QFN Packages

Avoid routing between the EPAD and the pads of a QFN device, as shown in Figure 8.

FIGURE 8: INCORRECT ROUTING UNDERNEATH QFN PACKAGE



Trace edges (crowns), via pad edges, and especially via hole edges can be exposed through broken soldermask, particularly after thermal cycling during soldering processes. Routing and vias between the EPAD and the pads can then easily short to either the pin pads, or especially to the EPAD because of the movement of the solder under the device during soldering.

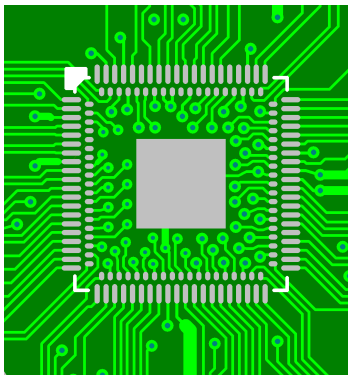
Via tenting (capping) and via plugging can reduce the occurrences of these effects, but it is less expensive and more beneficial to avoid putting traces or vias under the device in the first place.

If routed traces or vias are required under the QFN-style device, move any required routing or vias away from the EPAD as far as possible.

DQFN Packages

Take special care when routing between the EPAD and the pads of a DQFN device. It is usually desirable to break out the inner pads of a DQFN to the inside and drop vias to escape the part. As mentioned in the previous section, this can cause shorts under the device, but the DQFN devices have a larger gap between the pads and the EPAD, making this problem less likely. Again, keep any required routing or vias away from the EPAD as far as possible.

FIGURE 9: EXAMPLE ROUTING OF TRACES AND VIAS FOR DQFN PACKAGE



CLEANING ISSUES

Flux Residues

Many Microchip devices have very sensitive circuits such as PLLs that are adversely affected by small current leaks on the PCB. It is vital that all flux be completely cleaned from around the QFN/DQFN pin pads to avoid these current leak possibilities.

As an example, Microchip often uses no-clean solder paste formulations on its own designs, and then has them cleaned very thoroughly to remove all flux residues from around and under the pin pads.

APPENDIX A: APPLICATION NOTE REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00001843B (08-19-21)	All	Major content rework/changes in all sections.
DS00001843A (10-16-14)	Initial release	

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
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