



HDMI_ZC702

Vivado IP Integrator

1. Generating image patterns by PL.
2. Transferring Data to PS via VDMA.
3. Using DDR as buffer , and returning control signals and image data to PL via VDMA.
4. Image formatting.(AXIS)
5. Generate timing information.
6. Merge the image data with the timing information to output the video data. (AXIS > Video)
7. Output Interface.

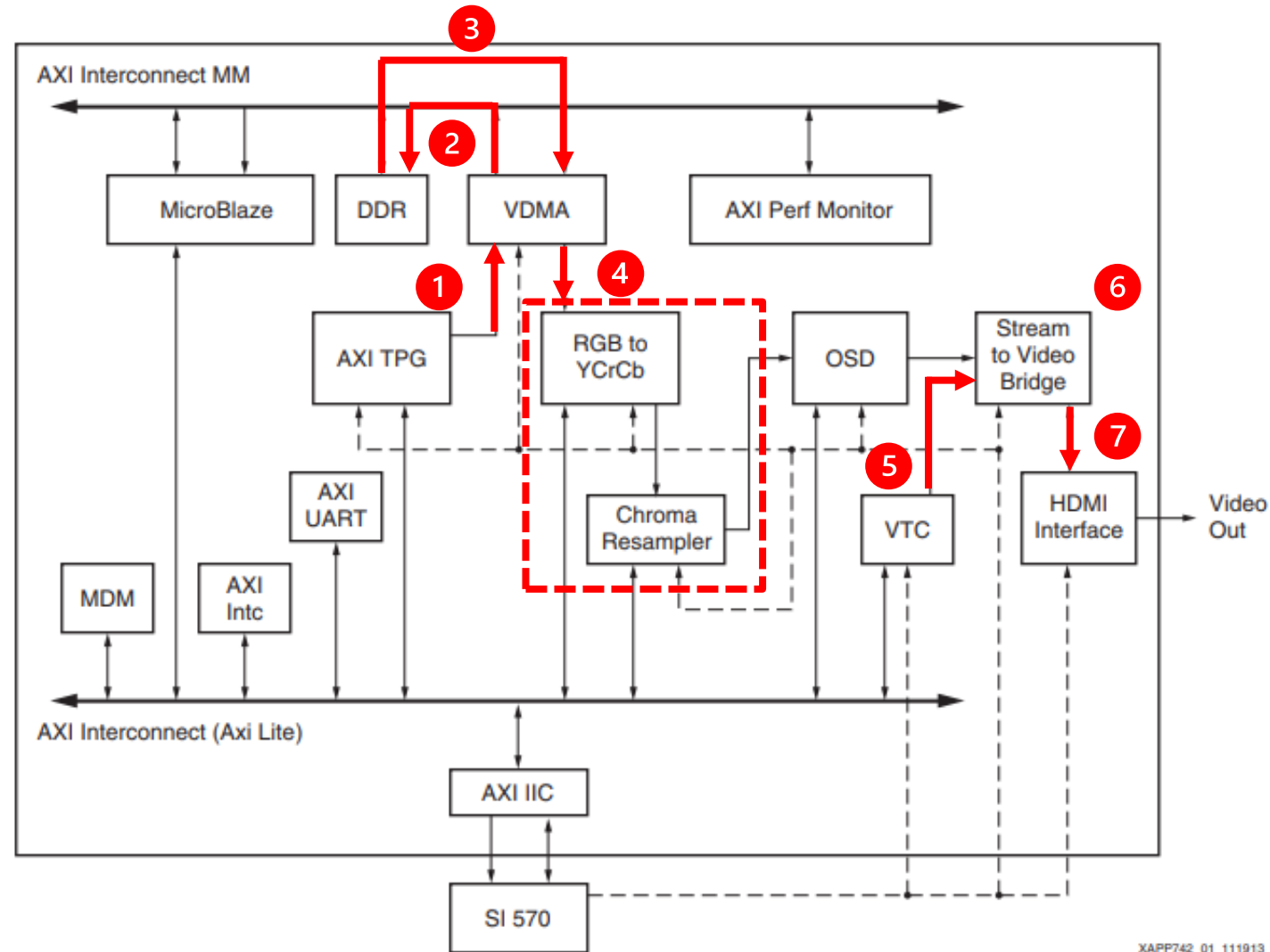


Figure 1: Reference System Block Diagram

XAPP742_01_111913

Block Diagram

AXI VDMA

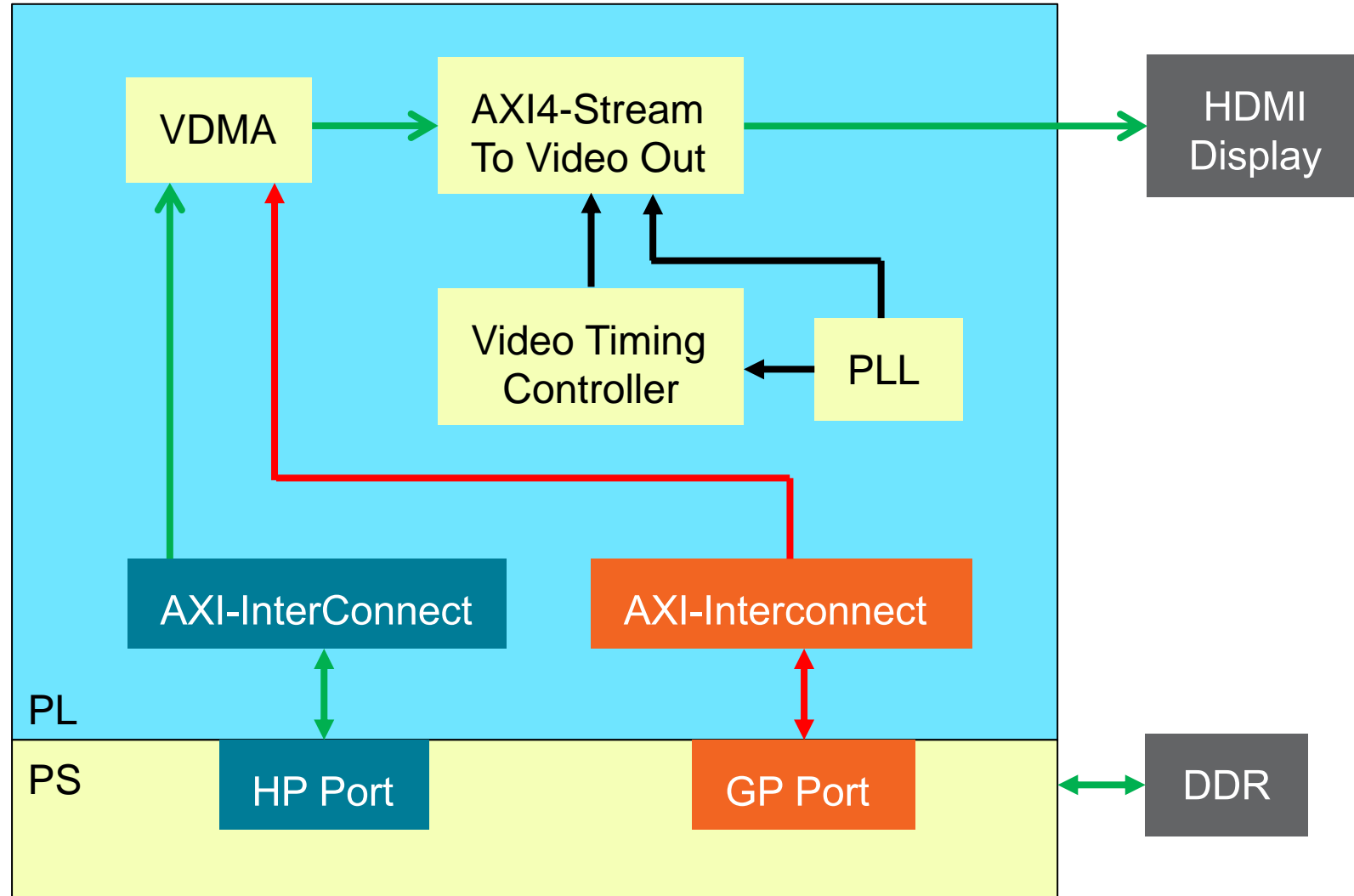
provide video read/write transfer capabilities from the AXI4 memory-mapped domain to the AXI4-Stream domain.

Video Timing Controller

The VTC LogiCORE™ IP is a general-purpose video timing generator and detector. The output side of the core generates the horizontal and vertical blanking and synchronization pulses used in a standard video system and includes support for programmable pulse polarity.

Video Timing Controller

The TPG block can generate several video test patterns that are commonly used in the video industry for verification and testing. In the reference design, the TPG is used as a replacement to a video source because only the amount of traffic generated to demonstrate the performance of the system is of interest



Block Diagram

AXI VDMA

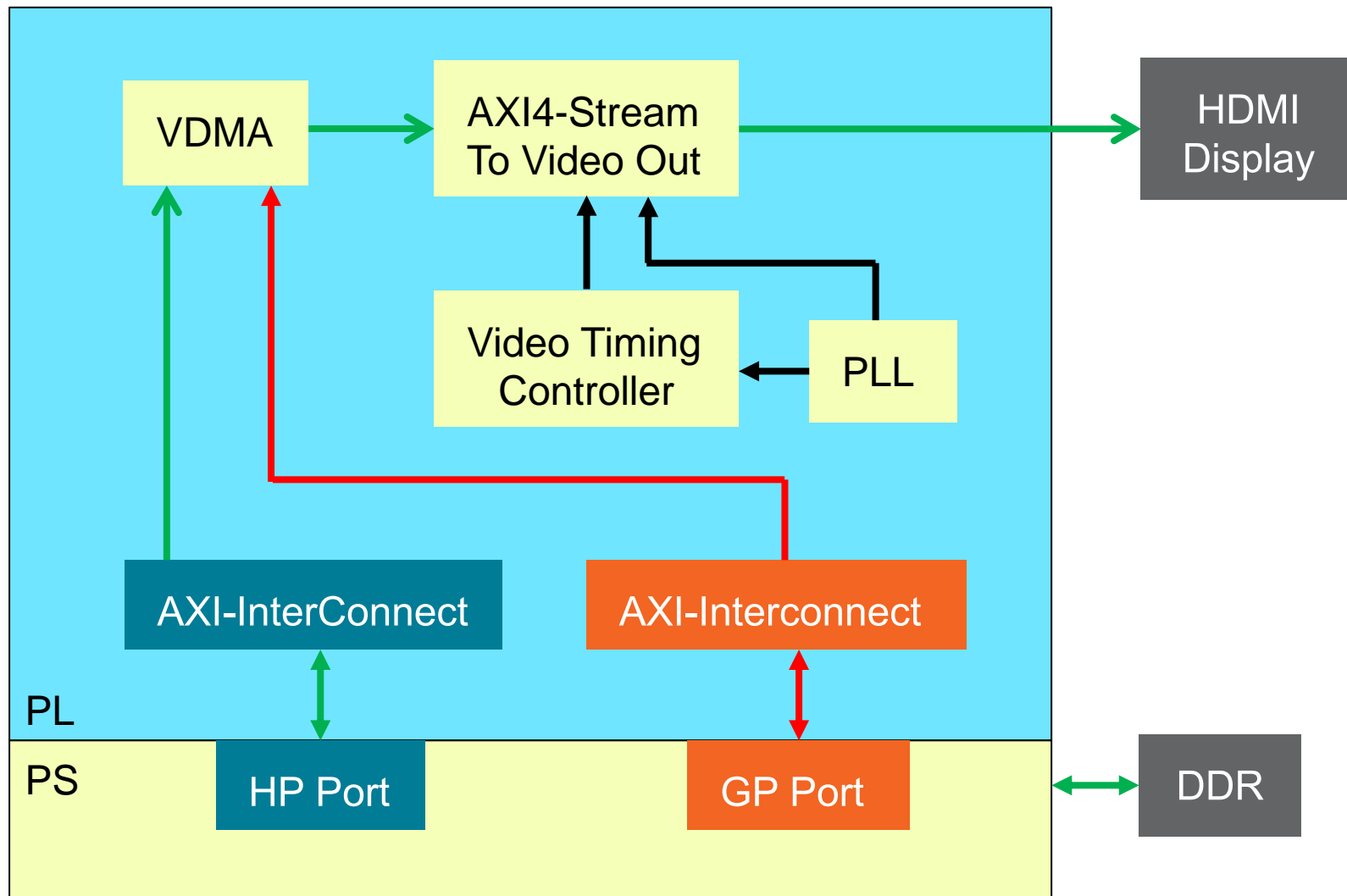
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Zynq

Click [Run Block Automation](#) to configure the settings for DDR and IO.
(Ensure that the UART interface is enabled.)

The screenshot displays the Vivado IDE interface. On the left, the 'Diagram' tab shows a block diagram of the 'processing_system7_0' with a 'ZYNQ7 Processing System' block. A red arrow points from the 'Run Block Automation' link in the top toolbar to the 'UART 1' checkbox in the 'Peripherals' list on the right. The 'Peripherals' list includes USB 1, SD 0, SD 1, SPI 0, SPI 1, UART 0, UART 1 (checked), I2C 0, and I2C 1. Below this, the 'MIO Configuration' section is expanded, showing the 'DDR Controller Configuration' table. The table lists various parameters for the DDR interface, including Memory Type, Memory Part, Effective DRAM Bus Width, ECC, Burst Length, DDR frequency, and Internal Vref.

Name	Select	Description
DDR Controller Configuration		
Memory Type	DDR 3	Type of memory interface. Re
Memory Part	MT41J256M8 HX-15I	Memory component part num
Effective DRAM Bus Width	32 Bit	Data width of DDR interface, t
ECC	Disabled	Enables error correction code
Burst Length	8	Minimum number of data bea
DDR	533.333333	Memory clock frequency. The
Internal Vref	<input checked="" type="checkbox"/>	Enables internal voltage refer
Juntion Temperature (C)	Normal (0-85)	Intended operating temperatu
Memory Part Configuration		
Training/Board Details		
Enable Advanced options	<input type="checkbox"/>	Enable Advanced DDR QoS

Zynq

- Enable M AXI GP0 port for communication control on the PS side.
- Enable S AXI HP0 port for high-speed data transmission.
- Change the PL Fabric Clocks to 100MHz.

The diagram shows the ZYNQ7 Processing System block with its pins. On the left, the PS pins are: S_AXI_HP0_FIFO_CTRL, S_AXI_HP0, M_AXI_GP0_ACLK, and S_AXI_HP0_ACLK. On the right, the PL pins are: DDR, FIXED_IO, USBIND_0, M_AXI_GP0, TTC0_WAVE0_OUT, TTC0_WAVE1_OUT, TTC0_WAVE2_OUT, FCLK_CLK0, and FCLK_RESET0_N. Blue arrows indicate connections from the PL pins to the PS pins.

The Vivado configuration windows are shown on the right. The PS-PL Configuration window has tabs for PS-PL Configuration, Peripheral I/O Pins, and SMC Timing Calculation. The PS-PL Configuration tab is active, showing the following settings:

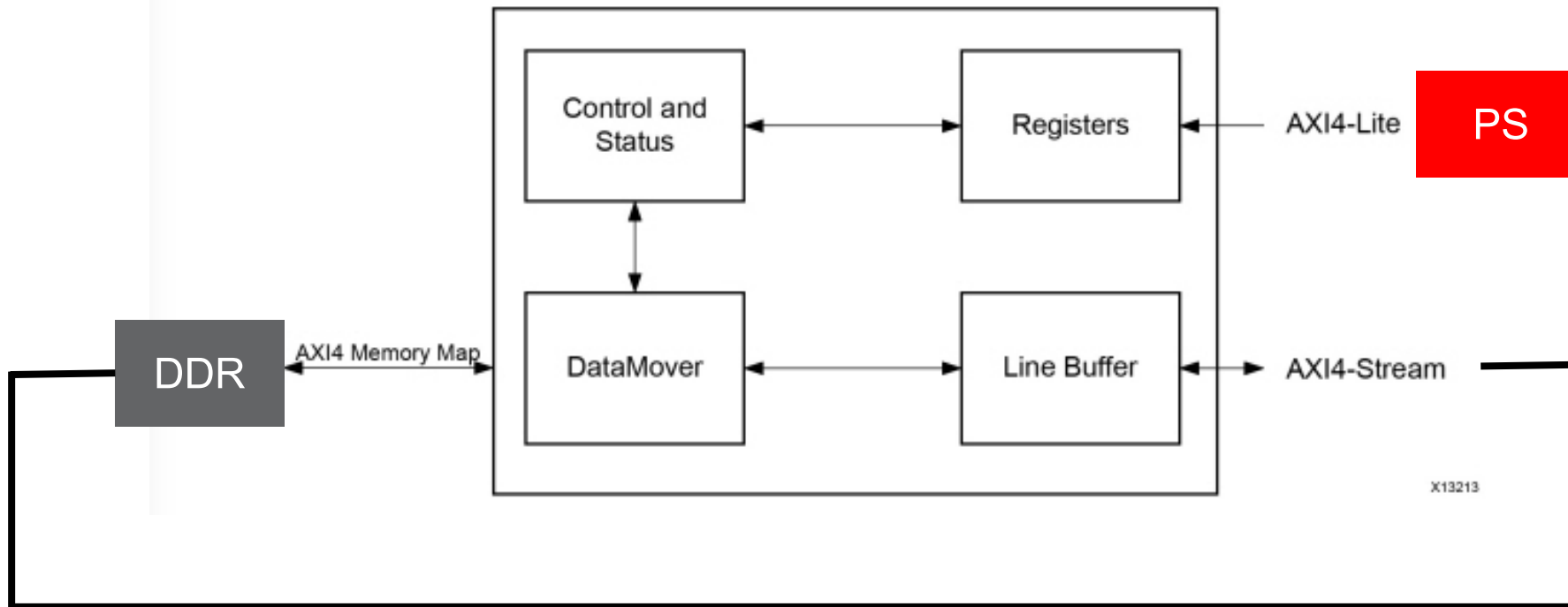
Name	Select	Description
General		
AXI Non Secure Enablement	0	Enable AXI Non Secure Transaction
GP Master AXI Interface		
M AXI GP0 interface	<input checked="" type="checkbox"/>	Enables General purpose AXI master interface 0
M AXI GP1 interface	<input type="checkbox"/>	Enables General purpose AXI master interface 1
GP Slave AXI Interface		
S AXI GP0 interface	<input type="checkbox"/>	Enables General purpose 32-bit AXI Slave interface 0
S AXI GP1 interface	<input type="checkbox"/>	Enables General purpose 32-bit AXI Slave interface 1
HP Slave AXI Interface		
S AXI HP0 interface	<input checked="" type="checkbox"/>	Enables AXI high performance slave interface 0
S AXI HP1 interface	<input type="checkbox"/>	Enables AXI high performance slave interface 1

The Clock Configuration window is also shown, with the following settings:

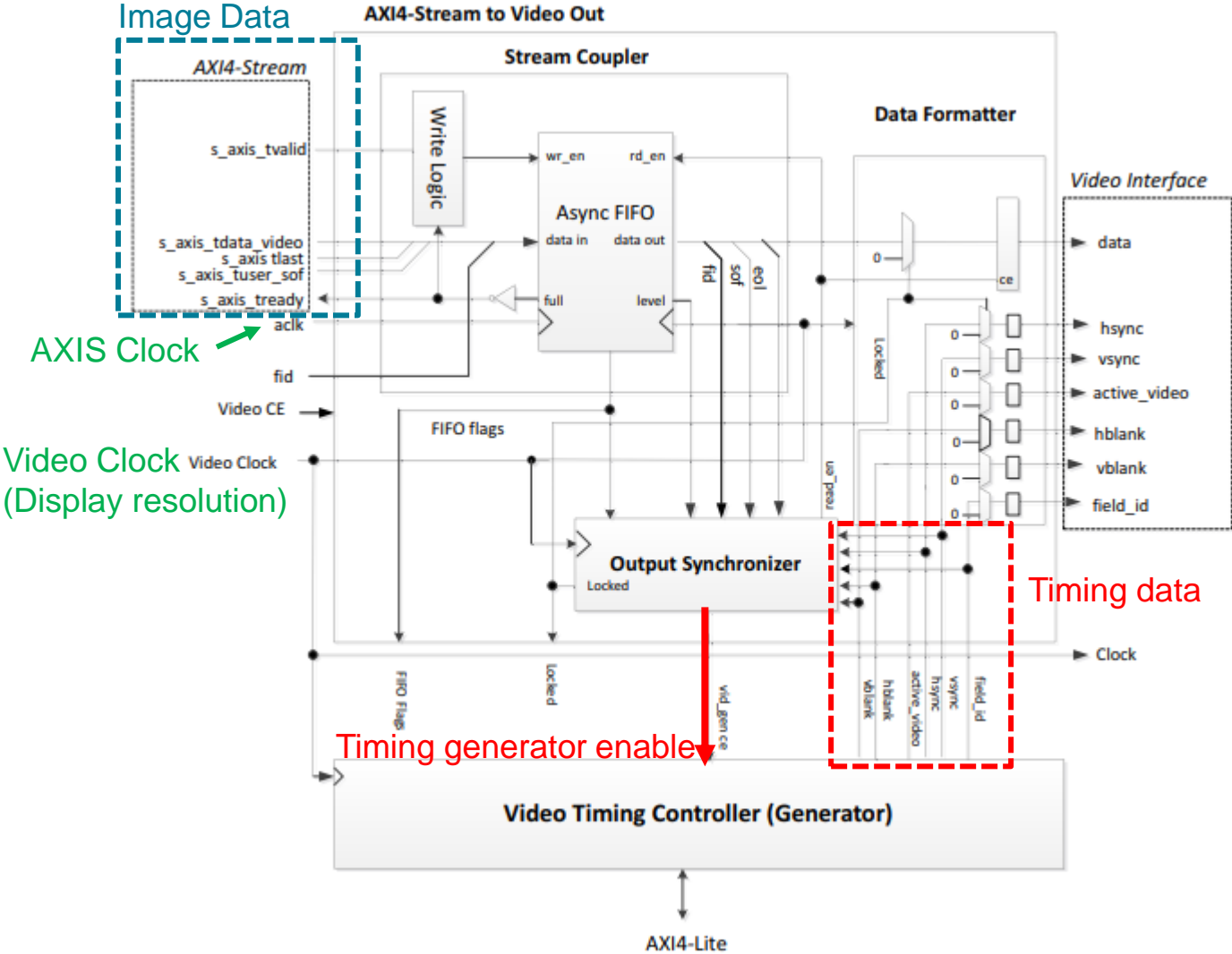
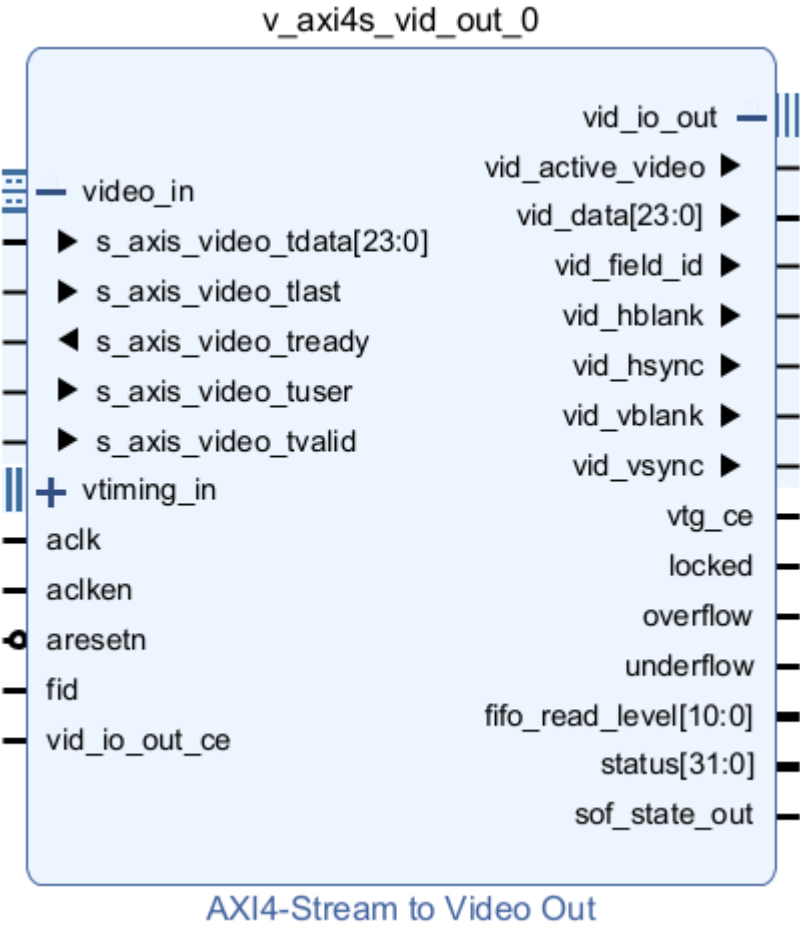
Component	Clock Source	Requested Frequency	Actual Frequency
Processor/Memory Clocks			
IO Peripheral Clocks			
PL Fabric Clocks			
<input checked="" type="checkbox"/> FCLK_CLK0	IO PLL	100	100.000000
<input type="checkbox"/> FCLK_CLK1	IO PLL	50	10.000000
<input type="checkbox"/> FCLK_CLK2	IO PLL	50	10.000000
<input type="checkbox"/> FCLK_CLK3	IO PLL	50	10.000000

AXI Video Direct Memory Access(VDMA)

Figure: AXI VDMA Block Diagram



AXI Stream to Video



AXI Stream to Video

Re-customize IP

AXI4-Stream to Video Out (4.0)

Documentation IP Location

Show disabled ports

video_in

vtiming_in

aclk

aclken

aresetn

fid

vid_io_out_clk

vid_io_out_ce

vid_io_out_reset

vid_io_out

vtg_ce

locked

overflow

underflow

fifo_read_level[10:0]

status[31:0]

sof_state_out

Component Namev_axi4s_vid_out_0

Pixels Per Clock1

AUTOVideo FormatRGB

AUTOAXI4S Video Input Component Width8

Native Video Output Component Width8

FIFO Depth1024

Clock Mode

CommonIndependent

Timing Mode

SlaveMaster

Hysteresis Level120 - 1023

v_axi4s_vid_out_0

video_in

vtiming_in

aclk

aclken

aresetn

fid

vid_io_out_ce

vid_io_out

vid_active_video

vid_data[23:0]

vid_field_id

vid_hblank

vid_hsync

vid_vblank

vid_vsync

vtg_ce

locked

overflow

underflow

fifo_read_level[10:0]

status[31:0]

sof_state_out

AXI4-Stream to Video Out

xlconstant_0

dout[0:0]

Constant

lcd_De

lcd_rgb[23:0]

lcd_hs

lcd_vs

lcd_b[0:0]

Video Timing Controller

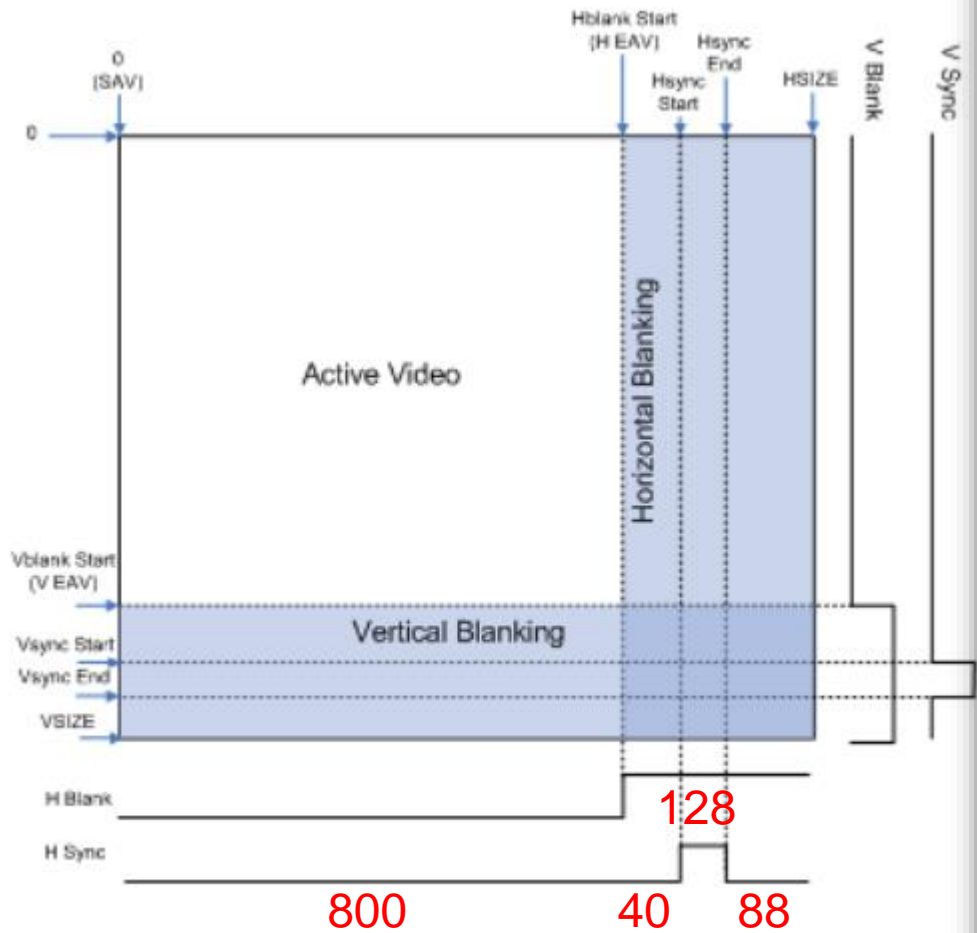


Figure 1-1: Example Video Frame and Timing Signals

Video Timing Controller (6.2)

Documentation IP Location

☐ Show disabled ports

Component Name `v_tc_0`

Detection/Generation **Default/Constant** **Frame Sync Position**

Video Format

Video Mode `Custom`

Horizontal Settings

Active Size	800	[0 - 4095]
Frame Size	1056	[0 - 4095]
Sync Start	840	[0 - 4095]
Sync End	968	[0 - 4095]

Frame/Field 0 Vertical Settings

Active Size	480	[0 - 4095]
Frame Size	525	[0 - 4095]
Sync Start	488	[0 - 4095]
Sync End	494	[0 - 4095]

Field 1 Vertical Settings

☐ Interlaced

Frame Size	750
Sync Start	724
Sync End	729

Frame/Field 0 Horizontal Fine Adjustment

Vblank Start	800	[0 - 4095]
Vblank End	800	[0 - 4095]
VSysc Start	800	[0 - 4095]
VSysc End	800	[0 - 4095]

Field 1 Horizontal Fine Adjustment

Vblank Start	640
Vblank End	640
VSysc Start	695
VSysc End	695

Inputs:

- `ctrl`
- `vtiming_in`
- `clk`
- `clken`
- `s_axi_aclk`
- `s_axi_aclken`
- `det_clken`
- `gen_clken`
- `sof_state`
- `resetrn`
- `s_axi_aresetrn`
- `fsync_in`

Outputs:

- `vtiming_out`
- `irq`
- `fsync_out[0:0]`

Video Timing Controller

Video Timing Controller (6.2)

Documentation

IP Location

Show disabled ports

+ ctrl

clk

clken

s_axi_aclk

s_axi_aclken

gen_clken

sof_state

resetrn

s_axi_aresetrn

fsync_in

vtiming_out

irq

fsync_out[0:0]

Component Namev_tc_0

Detection/Generation

Default/Constant

Frame Sync Position

Optional Features

☒ Include AXI4-Lite Interface

☐ Include INTC Interface

☐ Interlaced Video Support

☐ Synchronize Generator to Detector or to fsync_in

Max Clocks Per Line4096

Max Lines Per Frame4096

Frame Syncs1

☒ Enable Generation

☐ Enable Detection

Generation Options

☐ Field ID Generation

☒ Vertical Blank Generation

☒ Horizontal Blank Generation

☒ Vertical Sync Generation

☒ Horizontal Sync Generation

☒ Active Video Generation

☐ Active Chroma Generation

☐ Auto Generation Mode

Detection Options

☐ Field ID Detection

☒ Vertical Blank Detection

☒ Horizontal Blank Detection

☒ Vertical Sync Detection

☒ Horizontal Sync Detection

☒ Active Video Detection

☐ Active Chroma Detection

Component Namev_tc_0

Detection/Generation

Default/Constant

Frame Sync Position

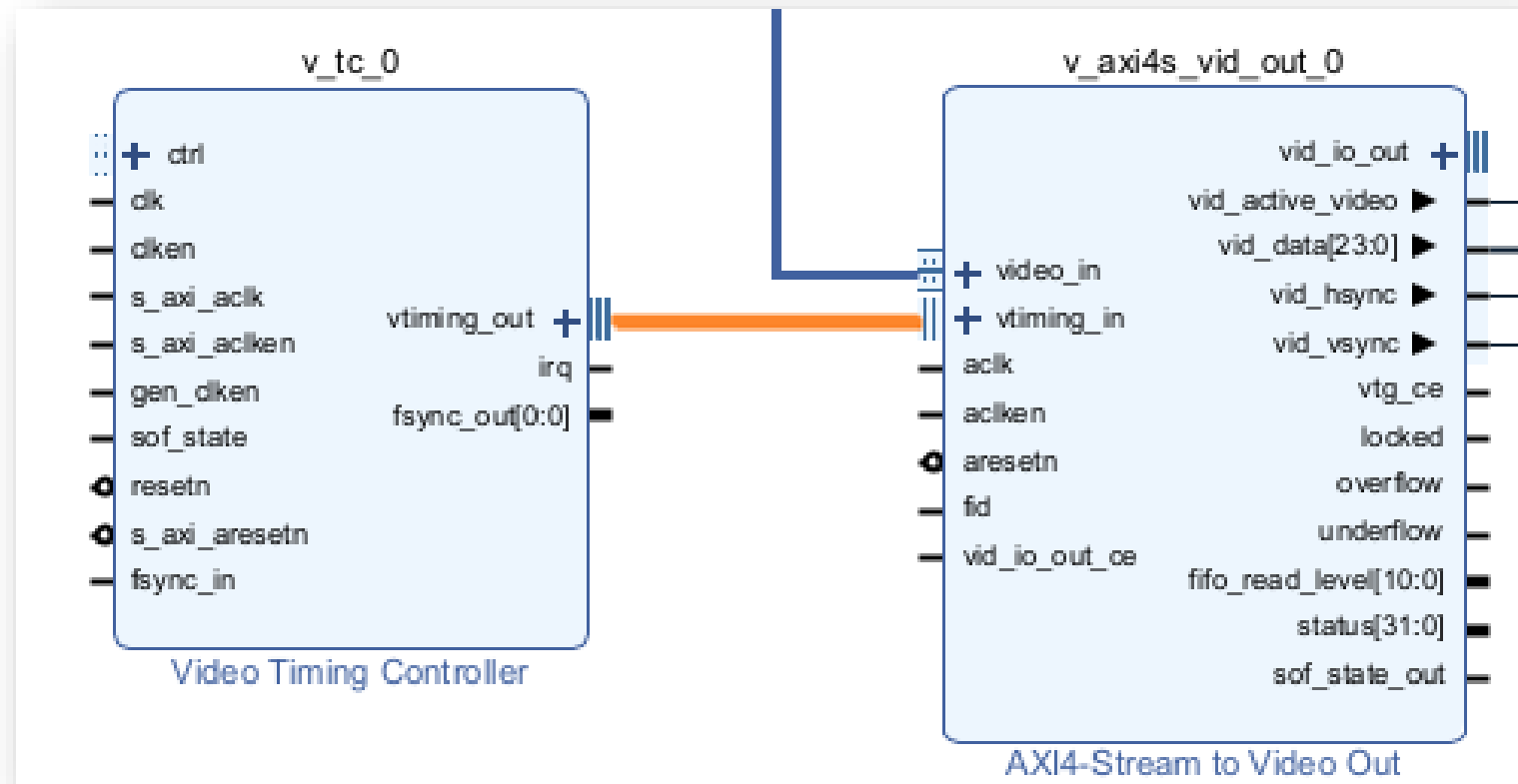
Frame Sync	Horizontal Position (Range: 0...4095)	Vertical Position (Range: 0...4095)
0	0	0

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AMD

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Video Timing Controller



Clocking Wizard

Clocking Wizard (6.0)

Documentation

IP Location

IP Symbol

Resource

Show disabled ports

clk_in1

clk_out1

Component Name

clk_wiz_0

Board

Clocking Options

Output Clocks

MMCM Settings

Summary

MMCM

PLL

Clocking Features

Jitter Optimization

Dynamic Reconfig Interface Options

Input Clock Information

Frequency Synthesis

Minimize Power

Phase Alignment

Spread Spectrum

Dynamic Reconfig

Dynamic Phase Shift

Safe Clock Startup

Balanced

Minimize Output Jitter

Maximize Input Jitter filtering

AXI4Lite

DRP

Phase Duty Cycle Config

Write DRP registers

Input Clock	Port Name	Input Frequency(MHz)		Jitter Options	Input Jitter	Source
Primary	clk_in1	<div>AUTO</div> 100.000	10.000 - 800.000	UI	0.010	Single ended c
<input type="checkbox"/> Secondary	clk_in2	<div>AUTO</div> 100.000	100.000 - 200.000		0.010	Single ended c

Board

Clocking Options

Output Clocks

MMCM Settings

Summary

The phase is calculated relative to the active input clock.

Output Clock	Port Name	Output Freq (MHz)		Phase
		Requested	Actual	
<input checked="" type="checkbox"/> clk_out1	clk_out1	33.33	33.33333	0.0

Enable Optional Inputs / Outputs for MMCM/PLL

☐ reset

☐ power_down

☐ input_clk_stopped

☐ locked

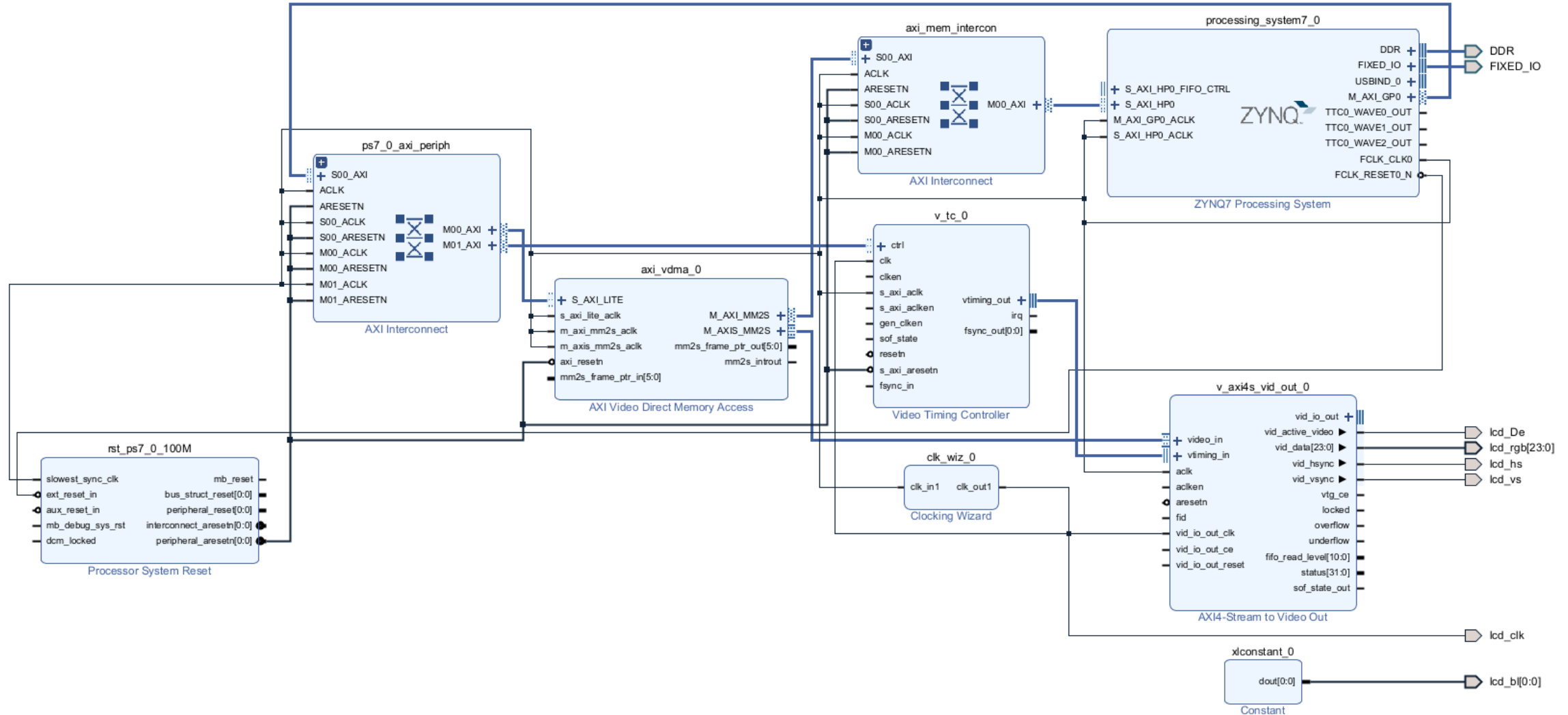
☐ clkfbstopped

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Final Block Design



Final Block Design

