



Board Interface Test

Course Agenda
2024.2

Board Interface Test

Xilinx的開發版都會提供相關的介面測試bitstream檔，可在該開發版的resource頁面下載

RESOURCES

DocumentationTools & IPTraining & Support

Filter Documentation

Step 1: Board Revision ⓘ

- Rev 1.0

Step 2: Tools Version ⓘ

- Most Recent Documents
- Vivado Design Suite 2015.1
- Vivado Design Suite 2014.4

Step 3: Show Documentation

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Document Type

- ☒ Board Files 10
- ☐ Example Designs +9


Document Type: Board Files ×

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Title ^ Date v

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XTP205 - VC707 BIST Tutorial (v12.0)


May 01, 2015

Document Type: Example Designs

Run, compile, and program the BIST Flash Application for the VC707

 See All Versions

Associated File(s):

 rdf0195-vc707-bist-c-2015-1.zip

Board Interface Test

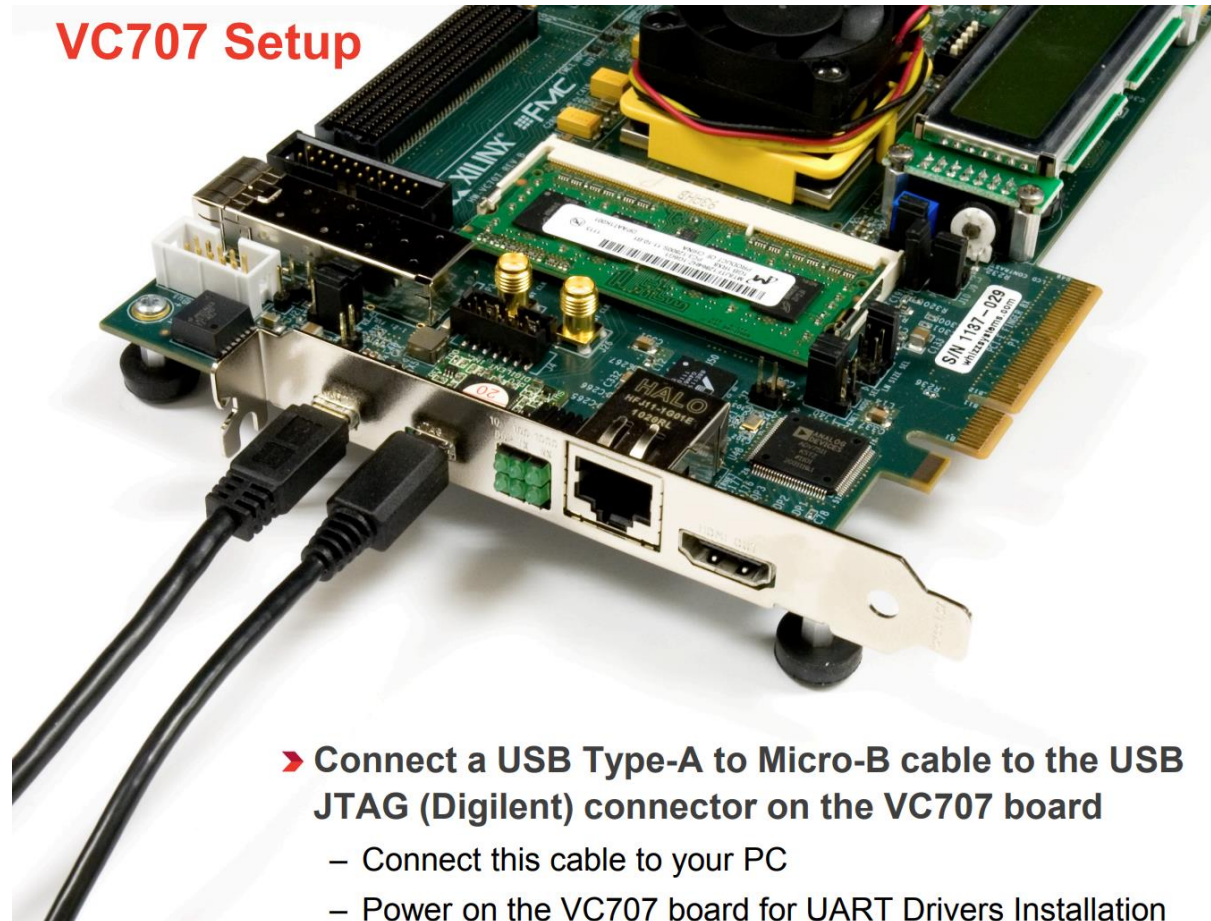
依據說明文件(此圖為XTP205)可安裝Vivado 2014.1 Lab板來燒錄

Revision History

| Date | Version | Description |
|----------|---------|--|
| 04/30/14 | 12.0 | Recompiled for 2015.1. |
| 11/24/14 | 11.0 | Recompiled for 2014.4. Fixed AR62666. |
| 10/08/14 | 10.0 | Recompiled for 2014.3. Added AR62666. |
| 06/09/14 | 9.0 | Recompiled for 2014.2. |
| 04/16/14 | 8.0 | Recompiled for 2014.1. |
| 12/18/13 | 7.0 | Recompiled for 2013.4. |
| 10/23/13 | 6.0 | Recompiled for 2013.3. Converted to IPI, added SGMII interface and LwIP. |
| 06/19/13 | 5.0 | Recompiled for 2013.2. AR55939, AR55738, AR55531, and AR55431 fixed. |
| 04/03/13 | 4.0 | Recompiled for 2013.1. Added AR55939, AR55738, AR55531, and AR55431. |
| 02/22/13 | 3.1 | Added AR53420. |
| 12/18/12 | 3.0 | Recompiled for 2012.4. |
| 10/23/12 | 2.0 | Recompiled for 2012.3. AR51180 fixed. |
| 09/20/12 | 1.0 | Initial version for 2012.2. Added AR51180. Added AR51758. |

Board Interface Test

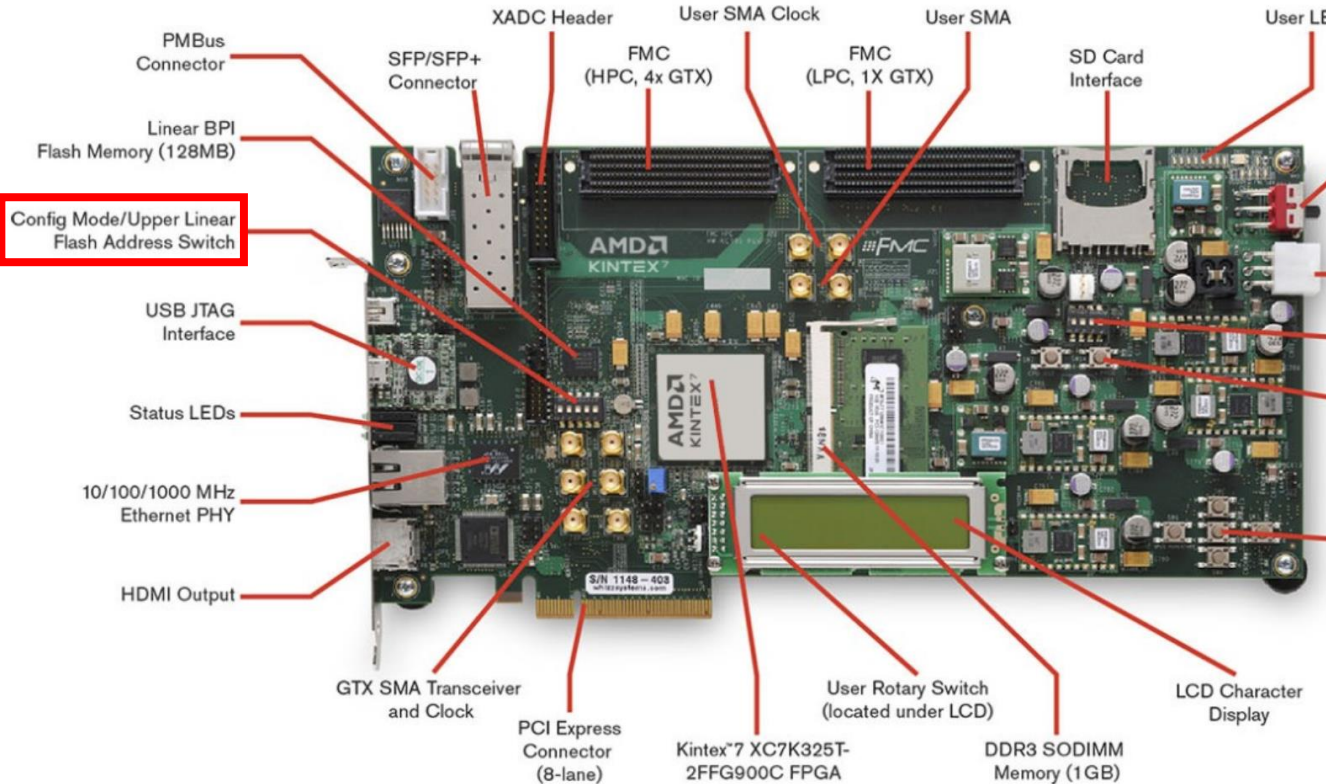
依據說明文件(此圖為XTP205)安裝好開發版，



- **Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the VC707 board**
 - Connect this cable to your PC
 - Power on the VC707 board for UART Drivers Installation

Board Interface Test

將Boot Mode轉為JTAG，Mode Pin可參考該開發版的User Guide



FPGA Configuration

The VC707 board supports two of the five 7 series FPGA configuration modes:

- Master BPI using the onboard Linear BPI Flash memory
- JTAG using a type-A to micro-B USB cable for connecting the host PC to the VC707 board configuration port

Each configuration interface corresponds to one or more configuration modes and bus widths as listed in [Table 1-2](#). The mode switches M2, M1, and M0 are on SW11 positions 3, 4, and 5 respectively as shown in [Figure 1-3](#).

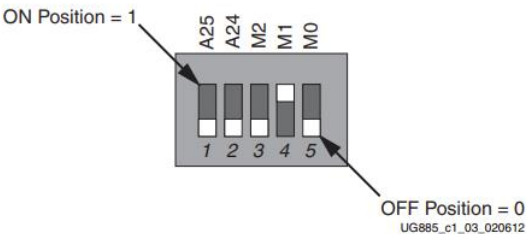


Figure 1-3: SW11 Default Settings

The default mode setting is M[2:0] = 010, which selects Master BPI at board power-on. See [Configuration Options](#) for detailed information about the mode switch SW11.

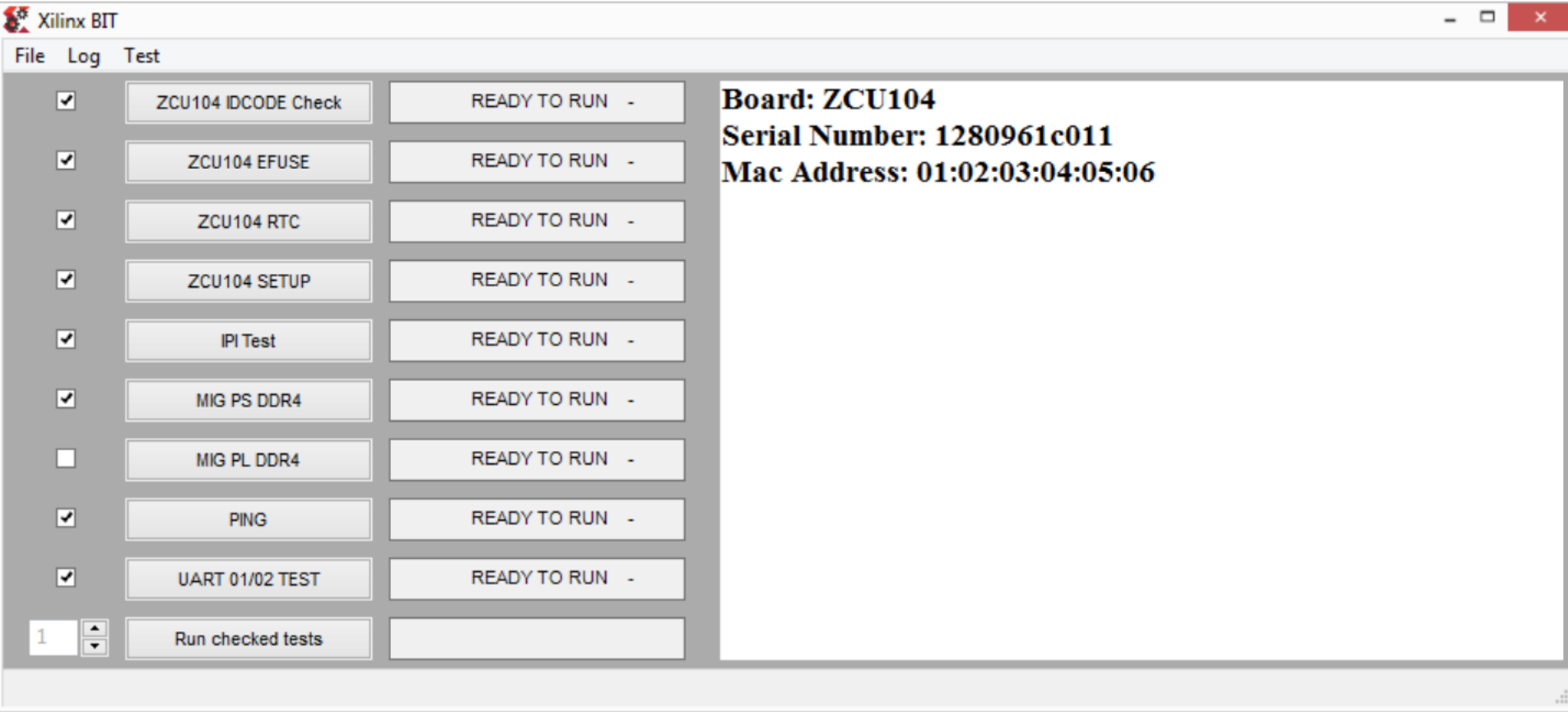
Table 1-2: VC707 Board FPGA Configuration Modes

| Configuration Mode | SW13 DIP switch Settings (M[2:0]) | Bus Width | CCLK Direction |
|--------------------|-----------------------------------|-----------|----------------|
| Master BPI | 010 | x8, x16 | Output |
| JTAG | 101 | x1 | Not Applicable |

For full details on configuring the FPGA, see *7 Series FPGAs Configuration User Guide* (UG470) [\[Ref 3\]](#).

Board Interface Test

部分開發版會提供GUI程式，依照官方附的開發文件操作即可



Board Interface Test

若未提供GUI或是GUI測試失敗，則可以直接燒錄Bist檔案。有的是一個專案，有的會提供Bist或tcl檔

gtxe2_top_v1_00_a

ready_for_download

vc707_bist.cache

vc707_bist.hw

vc707_bist.runs


vc707_bist.sdk

vc707_bist.srds





readme








system.tcl

system.xdc

 vc707_bist

rdf0387-vcu118-bit-c-2019-1 > vcu118_bit > tests > VCU118 >

 |  排序 ▾  檢視 ▾ ...

| 名稱 | 修改日期 ▾ | 類型 |
|--|-------------------|-----------|
| ▽ 今天 | | |
|  defaults | 2024/5/2 下午 10:27 | JSON 來源檔案 |
|  logs | 2024/5/2 下午 10:28 | 檔案資料夾 |
|  tcl | 2024/5/2 下午 10:28 | 檔案資料夾 |
|   bitstream | 2024/5/2 下午 10:28 | 檔案資料夾 |
|  elf | 2024/5/2 下午 10:28 | 檔案資料夾 |
|  bat | 2024/5/2 下午 10:27 | 檔案資料夾 |

Board Interface Test

觀察語法，若為一般的tcl寫法則可以直接在vivado source(一般會測試ipi及ibert)

| File Name | Modified | Type | Size |
|--------------------------------------|-------------------|--------|------|
| kcu105_ipi.tcl | 2024/5/2 下午 10:36 | TCL 檔案 | 1 KB |
| kcu105_mig_dds4.tcl | 2024/5/2 下午 10:36 | TCL 檔案 | 1 KB |
| kcu105_mig_dds4_status.tcl | 2024/5/2 下午 10:36 | TCL 檔案 | 3 KB |
| KCU105_N25Q256_Verify.tcl | | | |
| kcu105_ping.tcl | | | |
| kcu105_program_spi.tcl | | | |
| kcu105_verify_spi.tcl | | | |
| vivado_clear_fpga.tcl | | | |
| vivado_cse_mig_1gb.tcl | | | |
| vivado_cse_mig_2gb.tcl | | | |
| vivado_ibert_reset.tcl | | | |
| vivado_read_fpga_efuse.tcl | | | |
| vivado_read_fpga_efuse_status.tcl | | | |
| kcu105_eeprom.tcl | | | |
| kcu105_ibert_bank_fmc_hpc.tcl | | | |
| kcu105_ibert_bank_fmc_hpc_status.tcl | | | |
| kcu105_ibert_bank_fmc_lpc.tcl | | | |
| kcu105_ibert_bank_fmc_lpc_status.tcl | | | |
| kcu105_ibert_bank_pcie.tcl | | | |
| kcu105_ibert_bank_pcie_status.tcl | | | |
| kcu105_ibert_bank_sfp.tcl | | | |
| kcu105_ibert_bank_sfp_status.tcl | | | |


```
1 open_hw
2 connect_hw_server -url localhost:3121
3 current_hw_target [get_hw_targets */xilinx_tcf/Digilent/*]
4 set_property PARAM.FREQUENCY 15000000 [get_hw_targets */xilinx_tcf/Digilent/*]
5 open_hw_target -jtag_mode 1
6 scan_ir_hw_jtag 6 -tdi 0b
7 scan_ir_hw_jtag 6 -tdi 3f
8 close_hw_target
9 open_hw_target
10 current_hw_device [lindex [get_hw_devices] 0]
11 set_property PROGRAM.FILE {[pwd]/../bitstream/kcu105_ipi_app.bit} [lindex [get_hw_devices] 0]
12 program_hw_devices [lindex [get_hw_devices] 0]
13 close_hw_target [current_hw_target [get_hw_targets */xilinx_tcf/Digilent/*]]
14 disconnect_hw_server localhost:3121
15 close_hw
16
```


Board Interface Test

Source前須先將路徑改為該檔案的絕對路徑，注意vivado習慣路徑是使用 /

```
≡ kcu105_ipi.tcl ×
C: > Users > Orthr > Downloads > rdf0311-kcu105-bit-c-2017-3 > kcu105_bit > tcl > ≡ kcu105_ipi.tcl
1  open_hw
2  connect_hw_server -url localhost:3121
3  current_hw_target [get_hw_targets */xilinx_tcf/Digilent/*]
4  set_property PARAM.FREQUENCY 15000000 [get_hw_targets */xilinx_tcf/Digilent/*]
5  open_hw_target -jtag_mode 1
6  scan_ir_hw_jtag 6 -tdi 0b
7  scan_ir_hw_jtag 6 -tdi 3f
8  close_hw_target
9  open_hw_target
10 current_hw_device [lindex [get_hw_devices] 0]
11 set_property PROGRAM.FILE {[pwd]/../bitstream/kcu105_ipi_app.bit} [lindex [get_hw_devices] 0]
12 program_hw_devices [lindex [get_hw_devices] 0]
13 close_hw_target [current_hw_target [get_hw_targets */xilinx_tcf/Digilent/*]]
14 disconnect_hw_server localhost:3121
15 close_hw
16
```

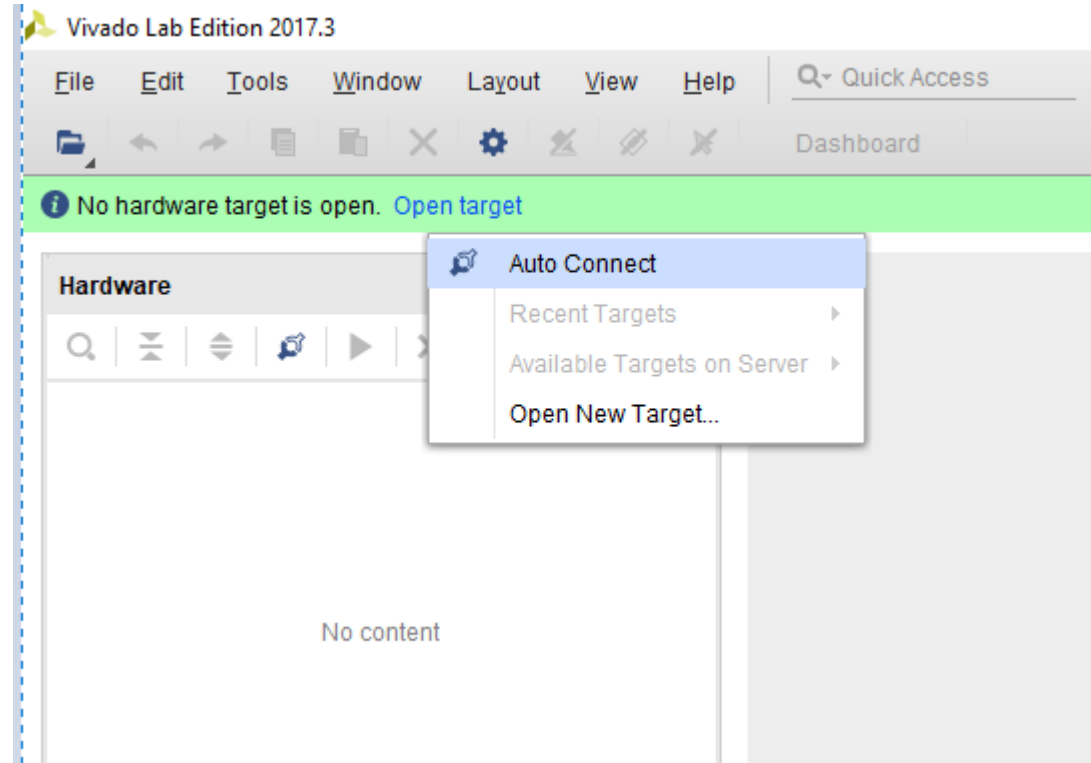
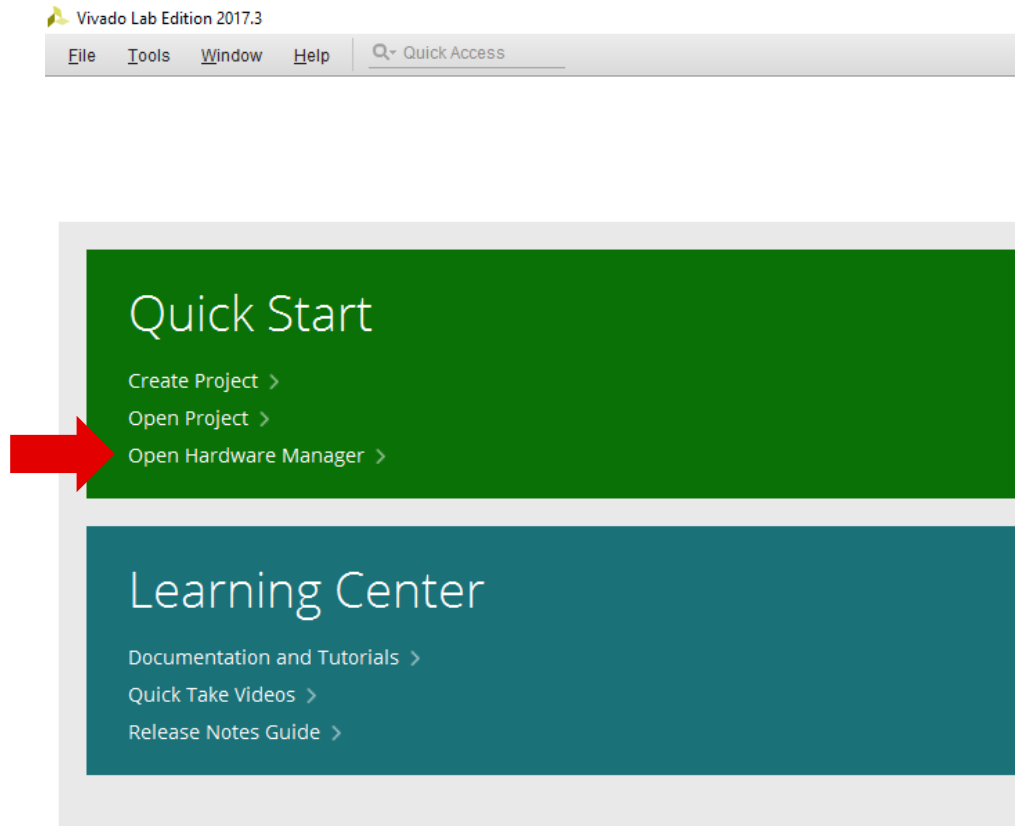
Board Interface Test

之後便可在Vivado Source該tcl



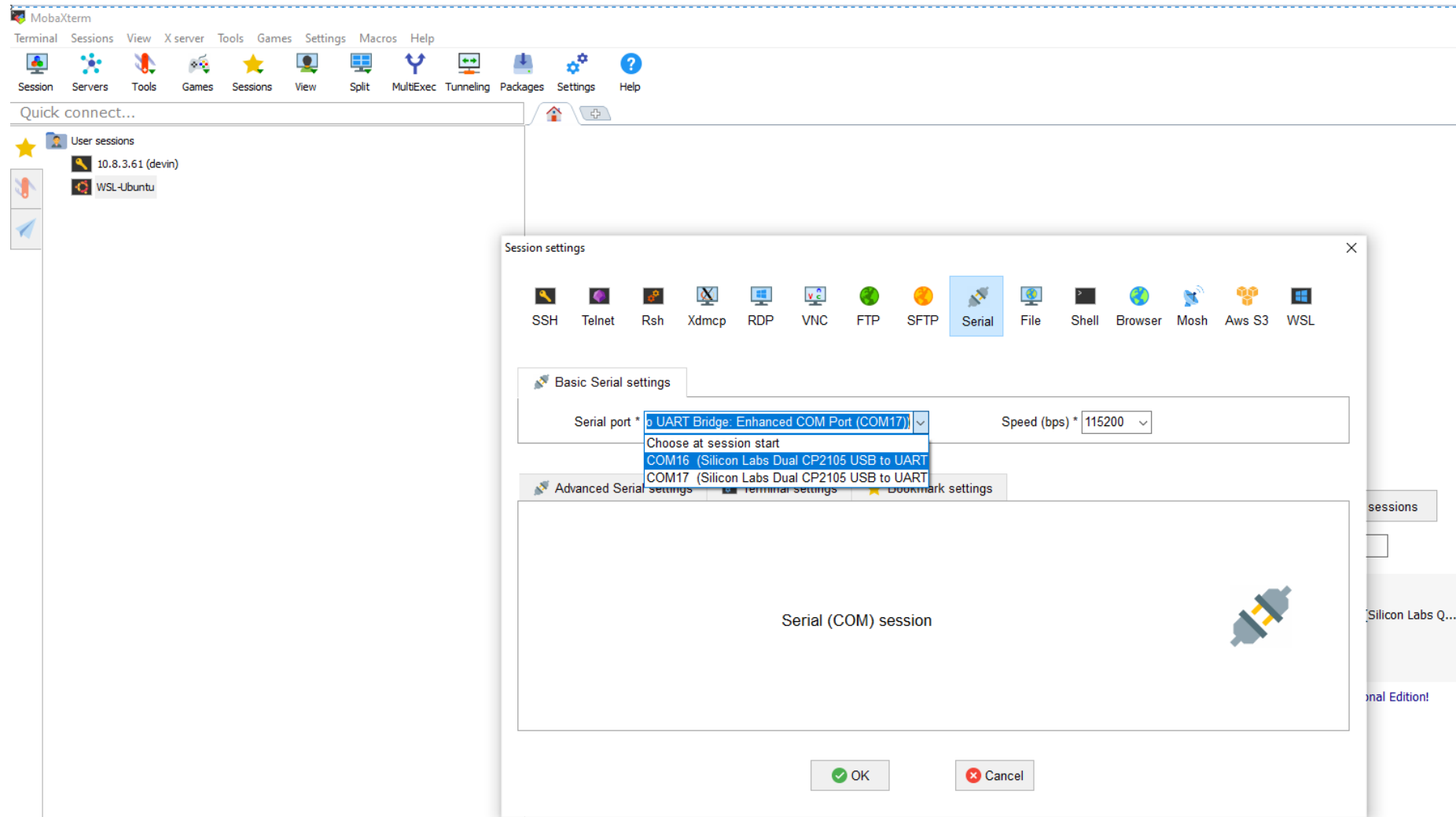
Board Interface Test

或是直接連接並燒錄bit檔案做測試



Board Interface Test

開啟Moba 並連接com port與bps(一般多為115200或9600)，燒錄後即可看見bist測試項目



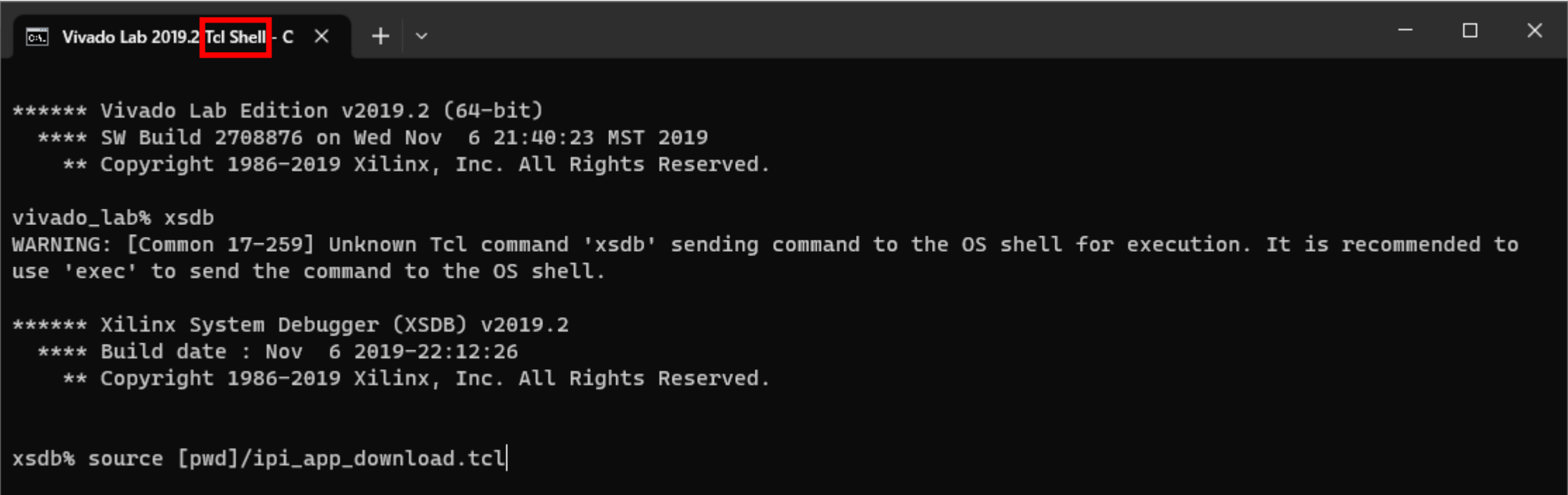
Board Interface Test

若tcl打開並非tcl寫法則需打開tcl shell

```
❏ ipi_app_download.tcl X
C: > Xilinx > boardtest > zcu102_bit > BoardUI > tests > ZCU102 > ipi_app > ❏ ipi_app_download.tcl
1  puts "There are $argc arguments to this script"
2  puts "The name of this script is $argv0"
3  # setup all defaults here in case an argument is not passed
4  if {$argc > 0} {
5      set i 0
6      foreach arg $argv {
7          puts "Argument $i is $arg"
8          incr i
9      }
10 }
11
12 puts "There should be at least 7 arguments at all times (0-6):"
13 puts "Argument 0 is [lindex $argv 0]"
14 puts "Argument 1 is [lindex $argv 1]"
15 puts "Argument 2 is [lindex $argv 2]"
16 puts "Argument 3 is [lindex $argv 3]"
17 puts "Argument 4 is [lindex $argv 4]"
18 puts "Argument 5 is [lindex $argv 5]"
```

Board Interface Test

與之前一樣，需要把tcl內的路徑修改為絕對路徑，並打開tcl shell輸入xsdb後source



```
Vivado Lab 2019.2 Tcl Shell - C × + ▾

***** Vivado Lab Edition v2019.2 (64-bit)
**** SW Build 2708876 on Wed Nov  6 21:40:23 MST 2019
** Copyright 1986-2019 Xilinx, Inc. All Rights Reserved.

vivado_lab% xsdb
WARNING: [Common 17-259] Unknown Tcl command 'xsdb' sending command to the OS shell for execution. It is recommended to
use 'exec' to send the command to the OS shell.

***** Xilinx System Debugger (XSDB) v2019.2
**** Build date : Nov  6 2019-22:12:26
** Copyright 1986-2019 Xilinx, Inc. All Rights Reserved.

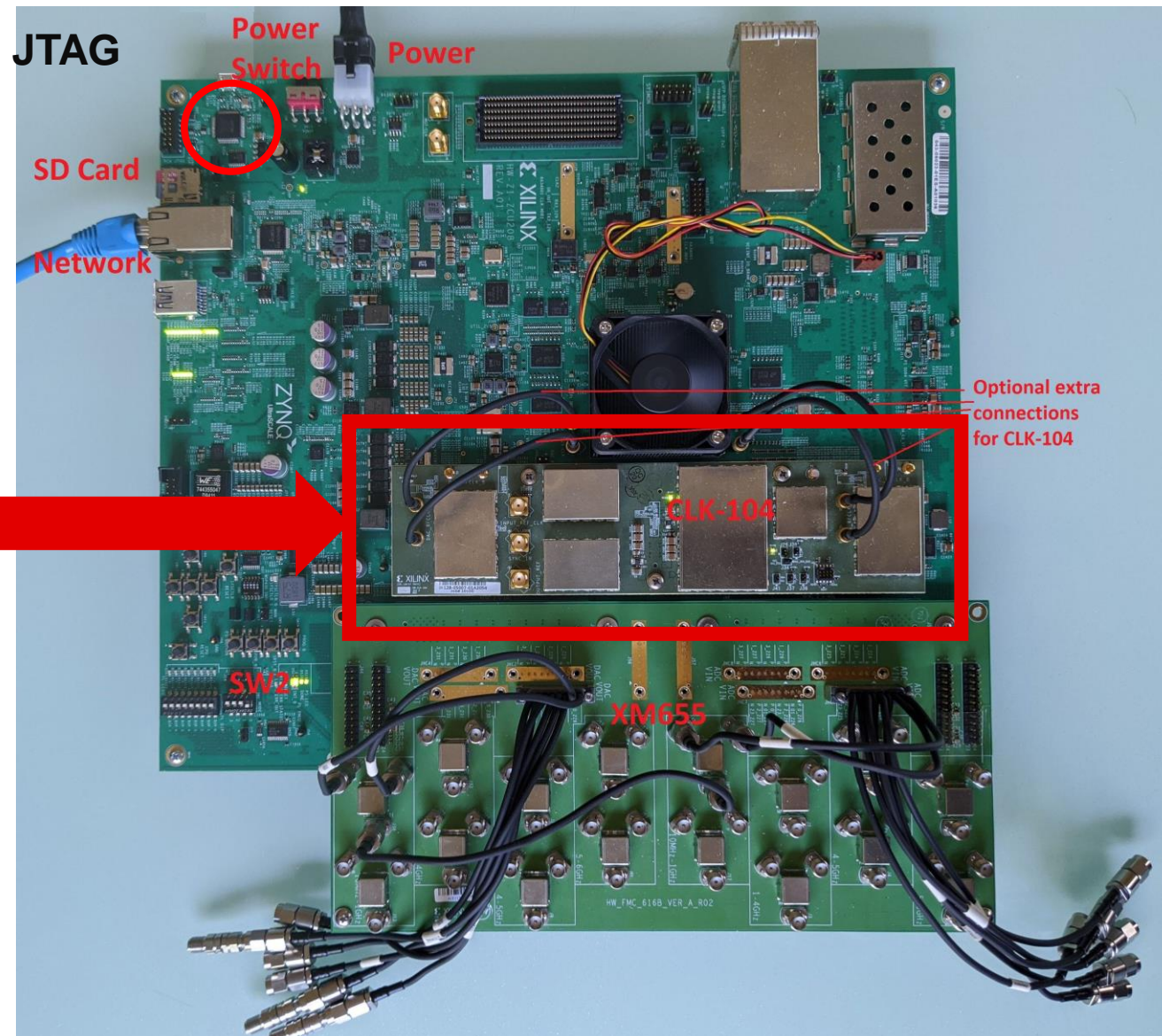
xsdb% source [pwd]/ipi_app_download.tcl|
```




RF_Analyzer

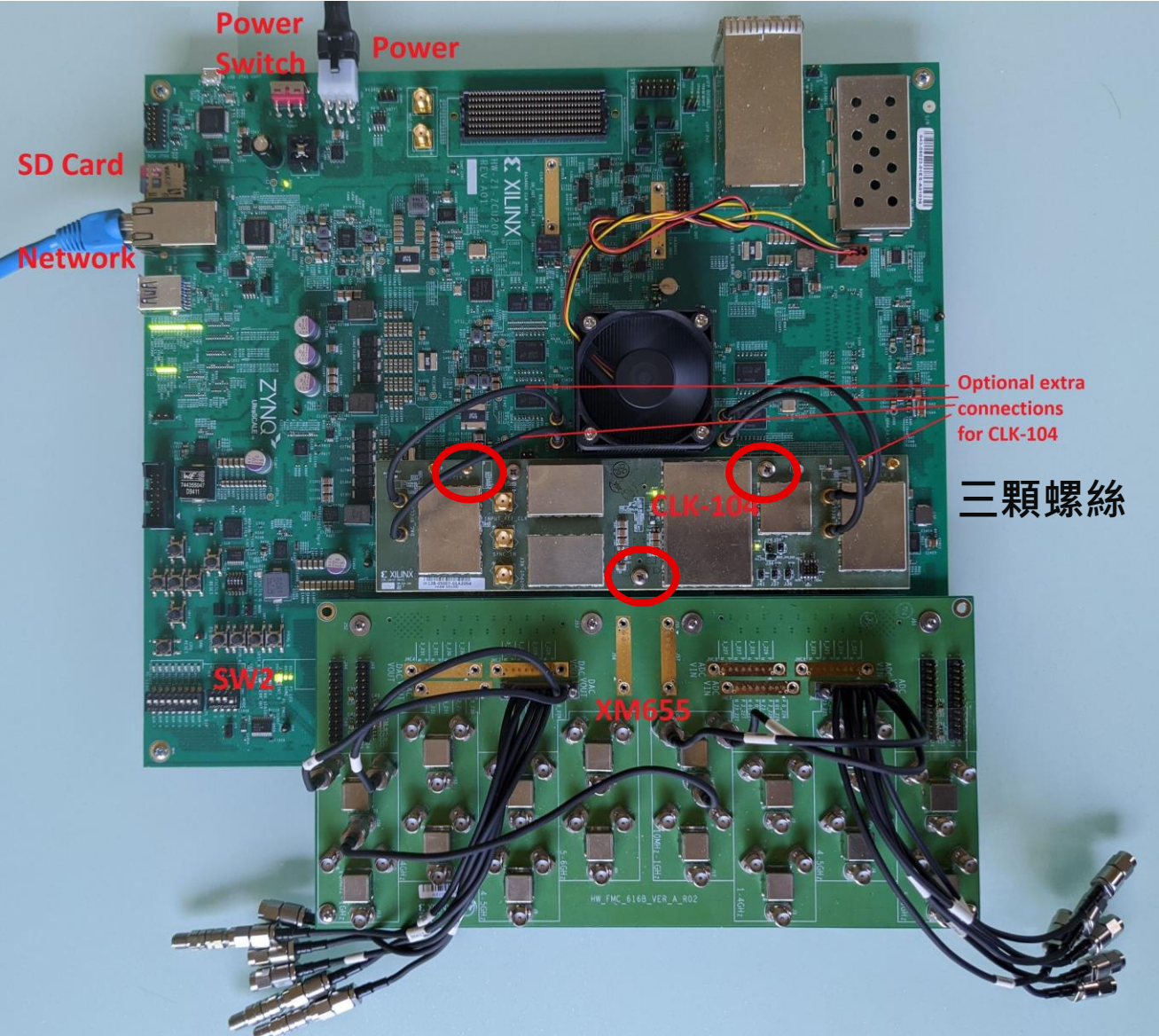
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2024.2

RF SoC ADC/DAC測試流程

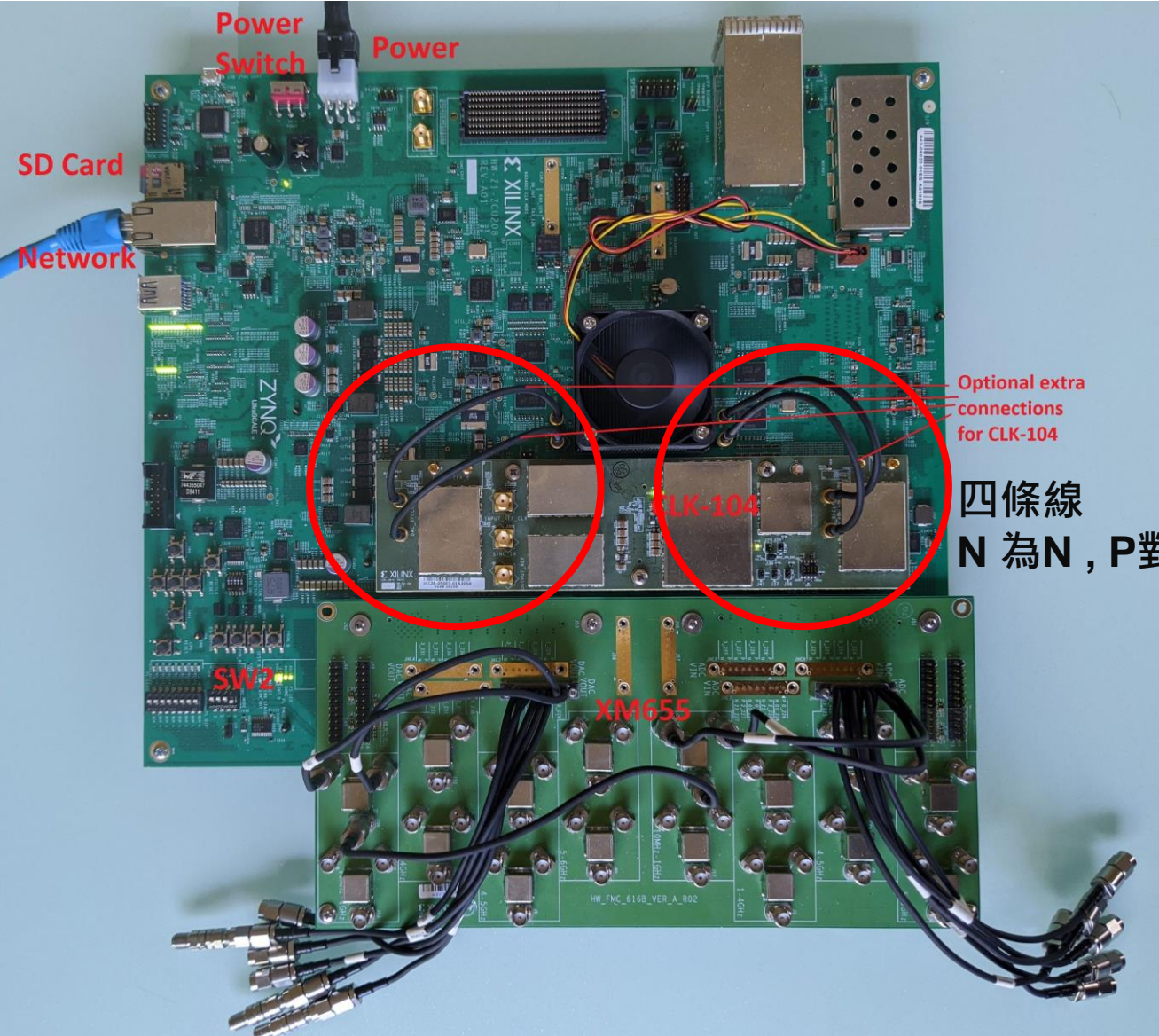


安裝這塊CLK_104就好

RF SoC ADC/DAC測試流程



RF SoC ADC/DAC測試流程

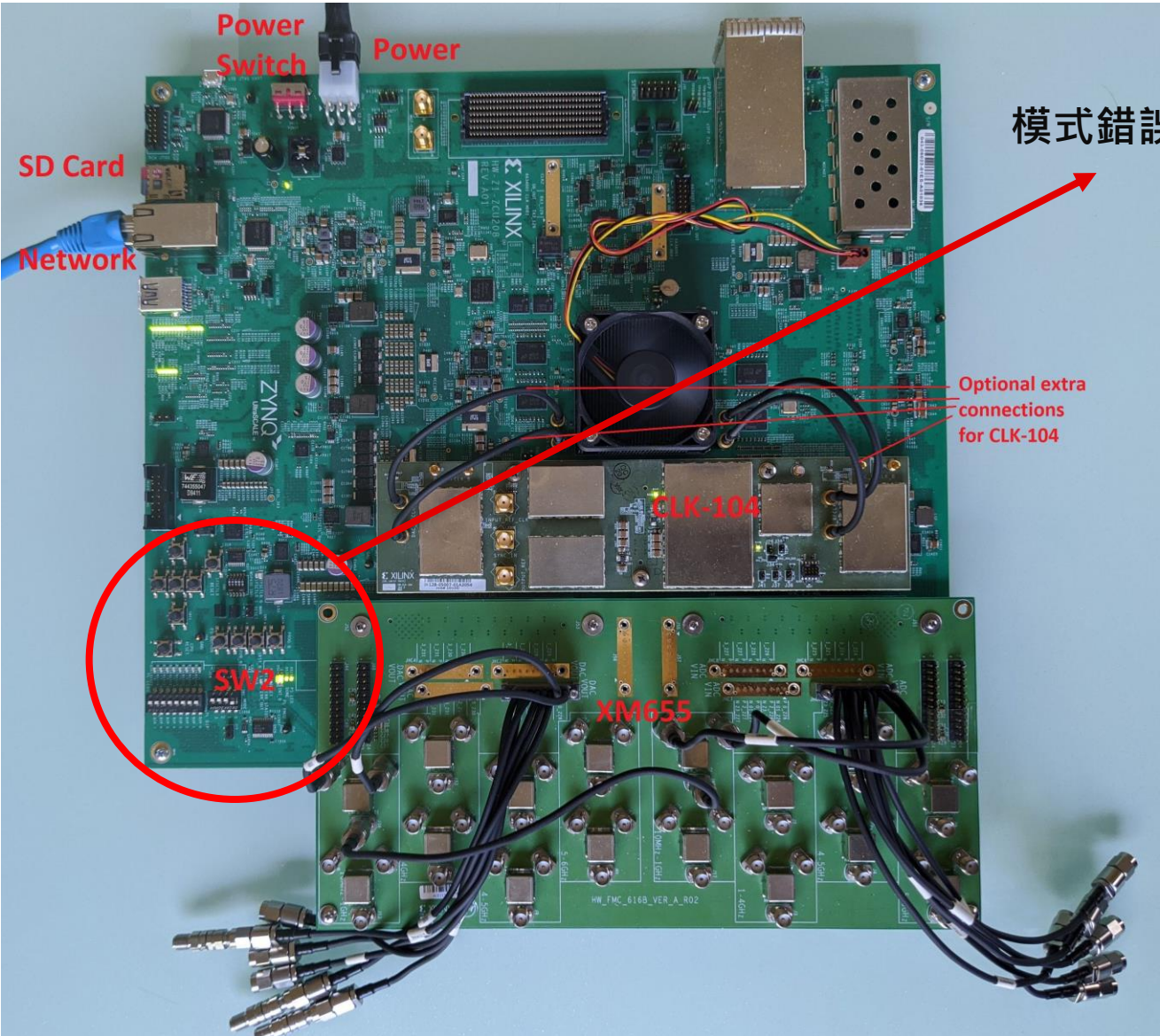
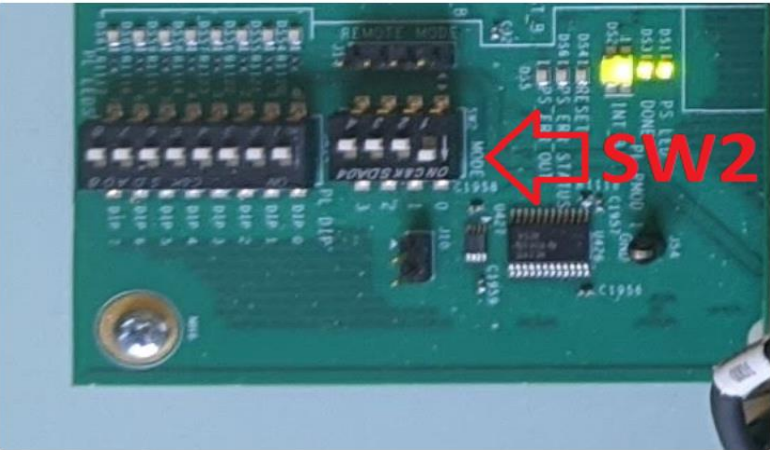


RF SoC ADC/DAC測試流程

JTAG

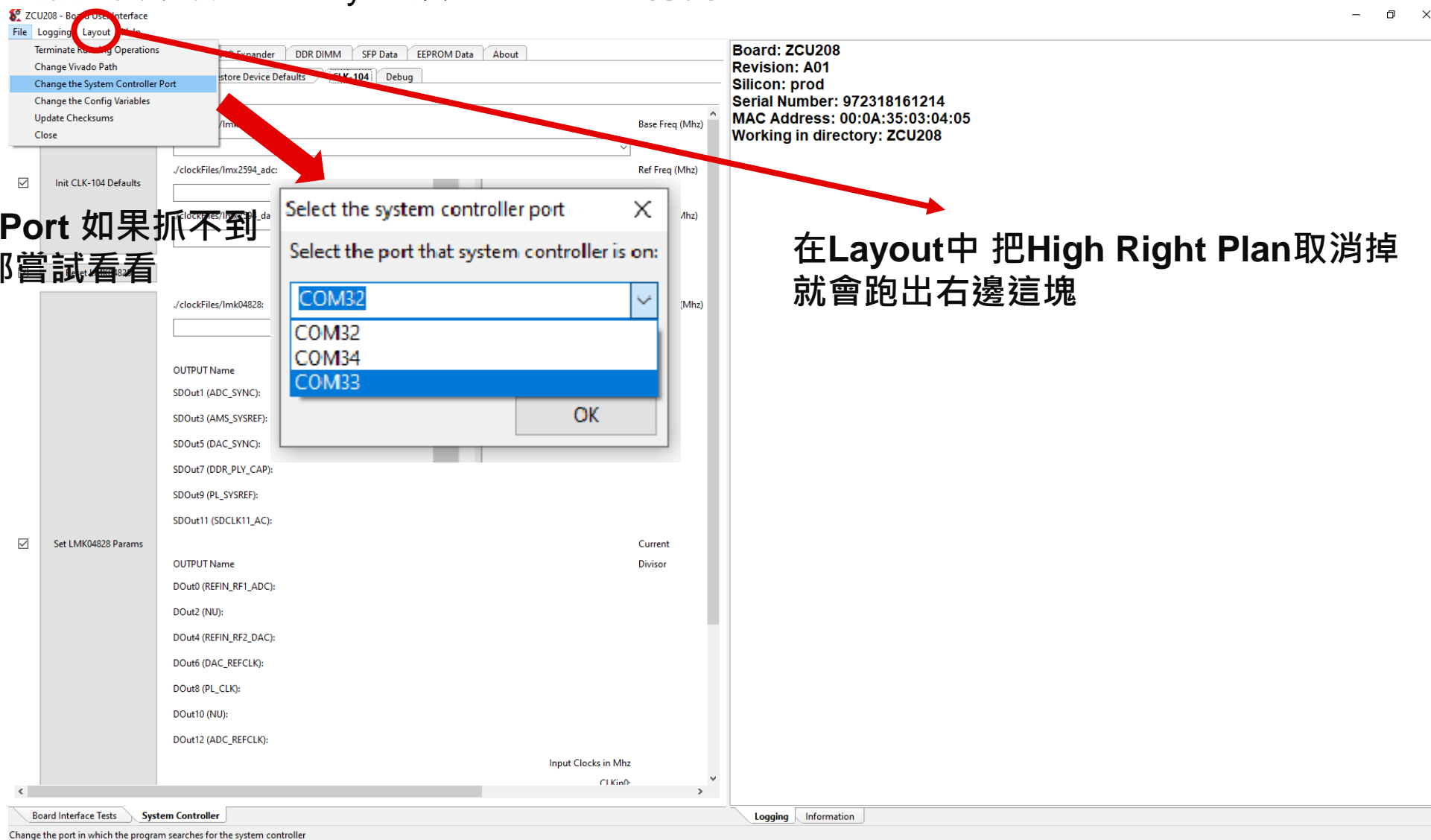


SD Card



打開ZCU208 Board User Interface

在該開發版頁面下載RF Analyzer及BIST GUI 並打開BIST GUI



總共有3個Port 如果抓不到
建議三個都嘗試看看

在Layout中 把High Right Plan取消掉
就會跑出右邊這塊

打開ZCU208 Board User Interface

在System Controller下修改時鐘頻率(若失敗請注意是否有其他中文設備 像藍芽耳機.無線滑鼠等)

滑鼠點擊這區塊
設定頻率

這裡選擇tcs檔案來設定CLK 104的頻率
以這個檔為例就是設定成491.52MHz

觀察這區
確定是否設定成功

1 2 3 4 5

Board Interface Tests **System Controller**

PASSED Set LMK04828 Params at: 2023-07-05 17:03:10.480000
Finished

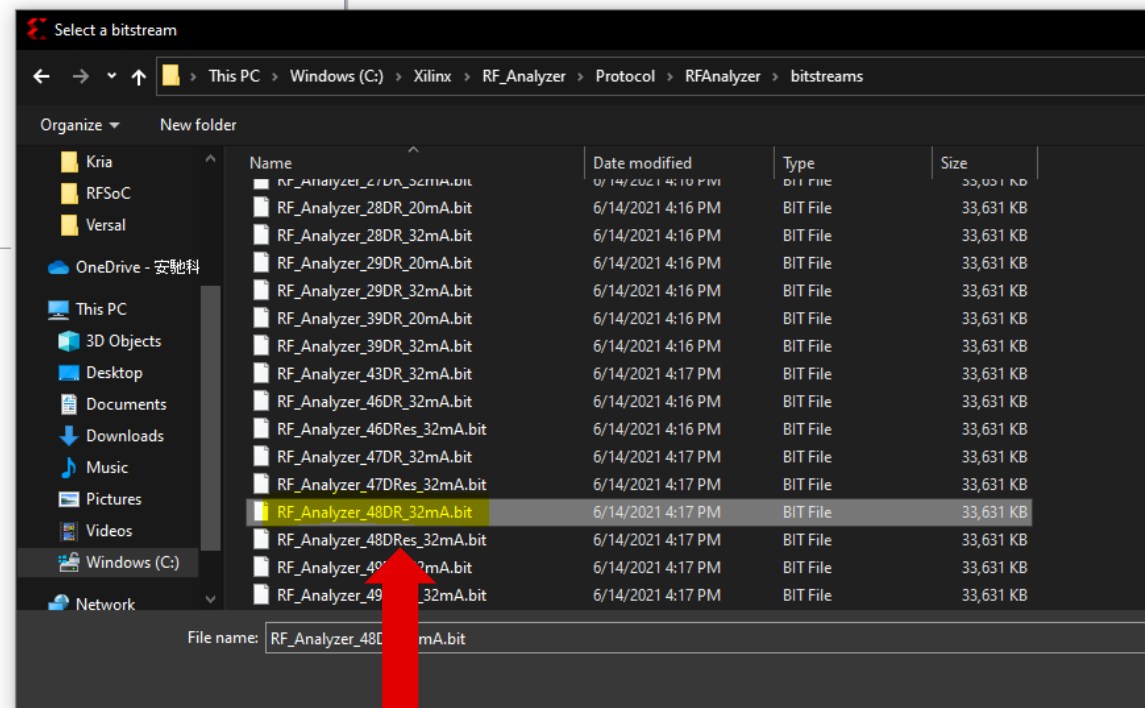
打開ZCU208 Board User Interface

設定完成即可打開RF_Analyzer



1
Connect to:
Local Server (target is on local machine) **Connect**
連結開發版 如果一直連接失敗
可考慮連筆電一起重開機

2
Hardware
Type/Serial Number Status
ZCU208/972318161214A Freq: 30MHz
xczu48dr Not Configured
JTAG Frequency
30MHz
Bitstream Path
C:\Xilinx\RF_Analyzer\Protocol\RFAnalyzer
Download Bitstream

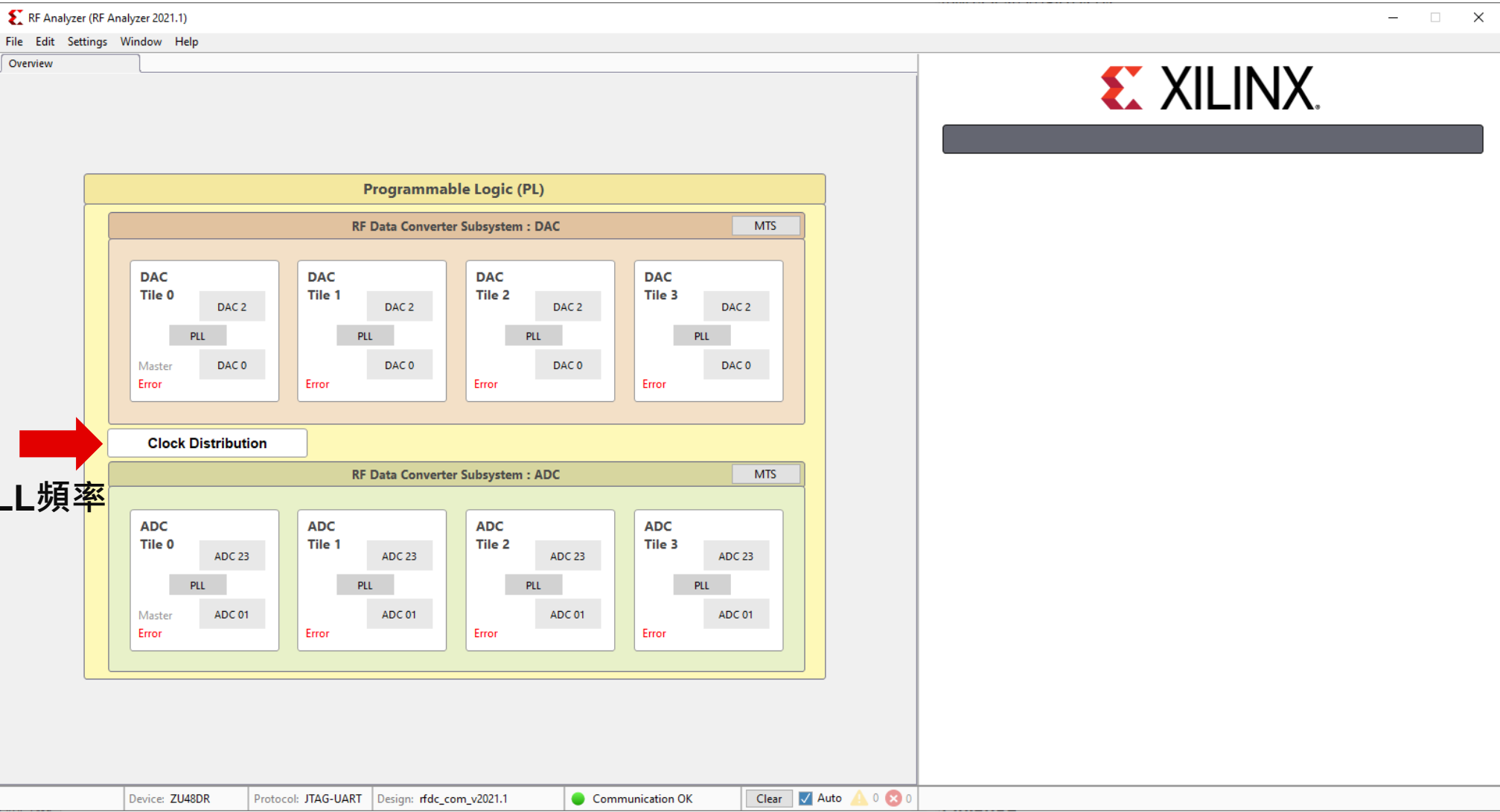


4
RF Analyzer裡面應該會附Bit檔
選擇檔名48DR (for ZCU108)

Board Interface Test

一開始全白為正常現象，需修改PLL頻率

點這裡更改PLL頻率



Board Interface Test

將各個PLL 的頻率設置的與剛剛CLK 104設置的頻率一樣

RF Data Converter Evaluation User Interface (RFEvalTool v2020.2)

File Edit Settings Window Help

Overview ClockDistribution

按這裡修改

兩個都要改

Ref. Clock (MHz) 245.760

Output Divider (M) 1

Sample Clock (MHz) 7864.320000

Ref. Clock (MHz) 245.760

Output Divider (M) 1

Sample Clock (MHz) 7864.320000

Ref. Clock (MHz) 245.760

Output Divider (M) 1

Sample Clock (MHz) 7864.320000

Ref. Clock (MHz) 245.760

Output Divider (M) 1

Sample Clock (MHz) 7864.320000

Ref. Clock (MHz) 245.760

Output Divider (M) 2

Sample Clock (MHz) 4423.680000

Ref. Clock (MHz) 245.760

Output Divider (M) 2

Sample Clock (MHz) 4423.680000

Ref. Clock (MHz) 245.760

Output Divider (M) 2

Sample Clock (MHz) 4423.680000

Ref. Clock (MHz) 245.760

Output Divider (M) 2

Sample Clock (MHz) 4423.680000

| Tile | Sample Clock (MHz) | PLL | Ref. Clock (MHz) | Output Divider (M) | Source Tile | Distribute Clock |
|------------|--------------------|-------------------------------------|------------------|--------------------|-------------|------------------|
| DAC Tile 3 | 7864.320000 | <input checked="" type="checkbox"/> | 245.760 | 1 | DAC Tile 0 | None |
| DAC Tile 2 | 7864.320000 | <input checked="" type="checkbox"/> | 245.760 | 1 | DAC Tile 0 | None |
| DAC Tile 1 | 7864.320000 | <input checked="" type="checkbox"/> | 245.760 | 1 | DAC Tile 0 | None |
| DAC Tile 0 | 7864.320000 | <input checked="" type="checkbox"/> | 245.760 | 1 | DAC Tile 0 | Input Ref. Clock |
| ADC Tile 3 | 4423.680000 | <input checked="" type="checkbox"/> | 245.760 | 2 | ADC Tile 2 | None |
| ADC Tile 2 | 4423.680000 | <input checked="" type="checkbox"/> | 245.760 | 2 | ADC Tile 2 | Input Ref. Clock |
| ADC Tile 1 | 4423.680000 | <input checked="" type="checkbox"/> | 245.760 | 2 | ADC Tile 2 | None |
| ADC Tile 0 | 4423.680000 | <input checked="" type="checkbox"/> | 245.760 | 2 | ADC Tile 2 | None |

Refresh

Apply

改完按套用

Board Interface Test

此為表示正常的畫面

