



VC707 Built-In Self Test Flash Application

April 2015

XTP205

Revision History

Date	Version	Description
04/30/14	12.0	Recompiled for 2015.1.
11/24/14	11.0	Recompiled for 2014.4. Fixed AR62666.
10/08/14	10.0	Recompiled for 2014.3. Added AR62666.
06/09/14	9.0	Recompiled for 2014.2.
04/16/14	8.0	Recompiled for 2014.1.
12/18/13	7.0	Recompiled for 2013.4.
10/23/13	6.0	Recompiled for 2013.3. Converted to IPI, added SGMII interface and LwIP.
06/19/13	5.0	Recompiled for 2013.2. AR55939, AR55738, AR55531, and AR55431 fixed.
04/03/13	4.0	Recompiled for 2013.1. Added AR55939, AR55738, AR55531, and AR55431.
02/22/13	3.1	Added AR53420.
12/18/12	3.0	Recompiled for 2012.4.
10/23/12	2.0	Recompiled for 2012.3. AR51180 fixed.
09/20/12	1.0	Initial version for 2012.2. Added AR51180. Added AR51758.

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Overview

- Xilinx VC707 Board
- Software Requirements
- VC707 Setup
- VC707 BIST (Built-In Self Test)
- Run the USB Design
- Compile VC707 BIST Design
- Program VC707 with BIST Design
- Run the USB2 Design
- Run the LwIP Ethernet Design
- References

VC707 BIST Design Description

► Description

- The Built-In System Test (BIST) application uses an IPI MicroBlaze system to verify board functionality. A UART based terminal program interface offers users a menu of tests to run.

► Block Design Source

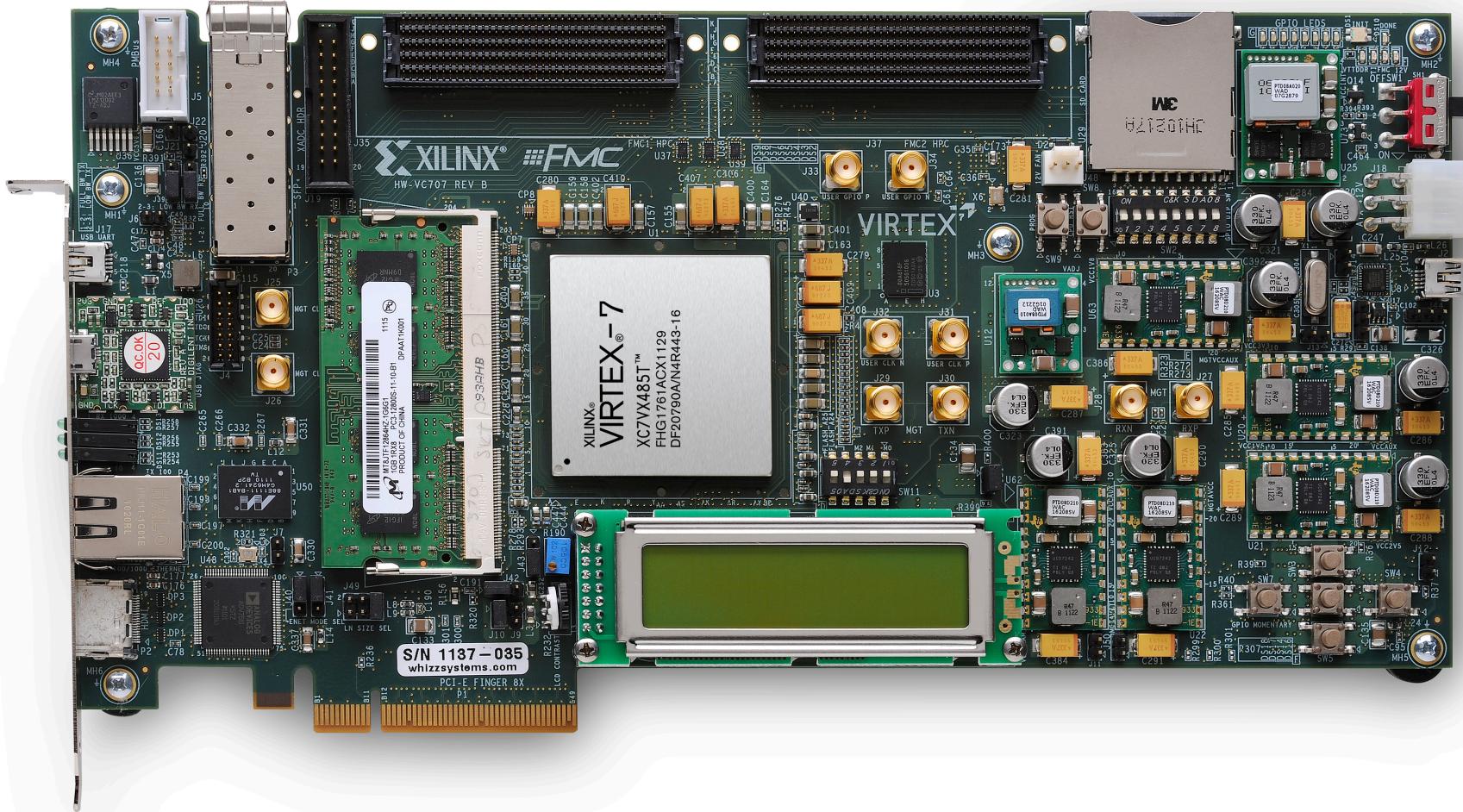
- VC707 BIST Design Files (2015.1 C) ZIP file
- Available through <http://www.xilinx.com/vc707>

VC707 BIST Design Description

► Block Design IP

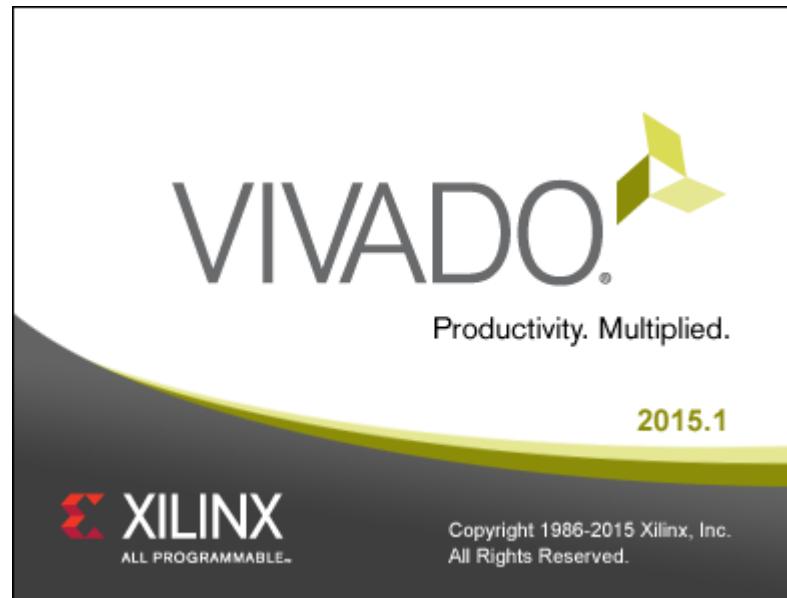
- Processor and Subsystems: MicroBlaze, MicroBlaze Debug Module (MDM), Local Memory Bus, LMB BRAM Controller, Block Memory Generator, Proc Sys Reset, AXI Interrupt Controller
- AXI Bus: AXI Interconnect, AXI Timer
- Memory: AXI BRAM Controller, MIG 7 Series, AXI DMA
- Peripherals: AXI USB2, AXI Ethernet, AXI EMC, AXI IIC, AXI GPIO, AXI UART 16550, XADC Wizard
- Other IP: Constant, Concat, gte2_top
 - [Vivado Design Suite Tcl Command Reference Guide](#) (UG835)
 - [Designing IP Subsystems Using IP Integrator](#) (UG994)

Xilinx VC707 Board

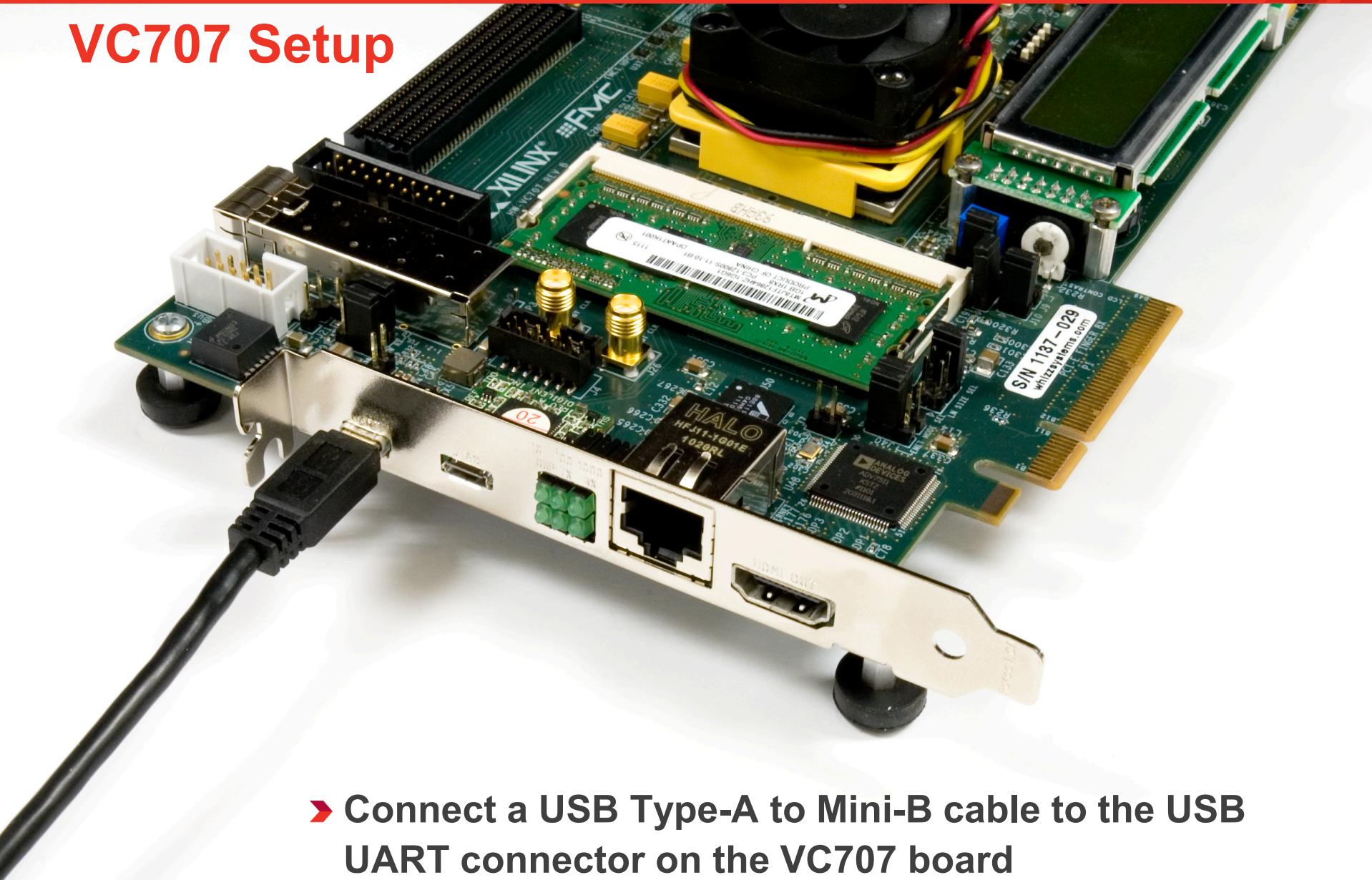


Vivado Software Requirements

- Xilinx Vivado Design Suite 2015.1, Design Edition + SDK
 - Combined installer

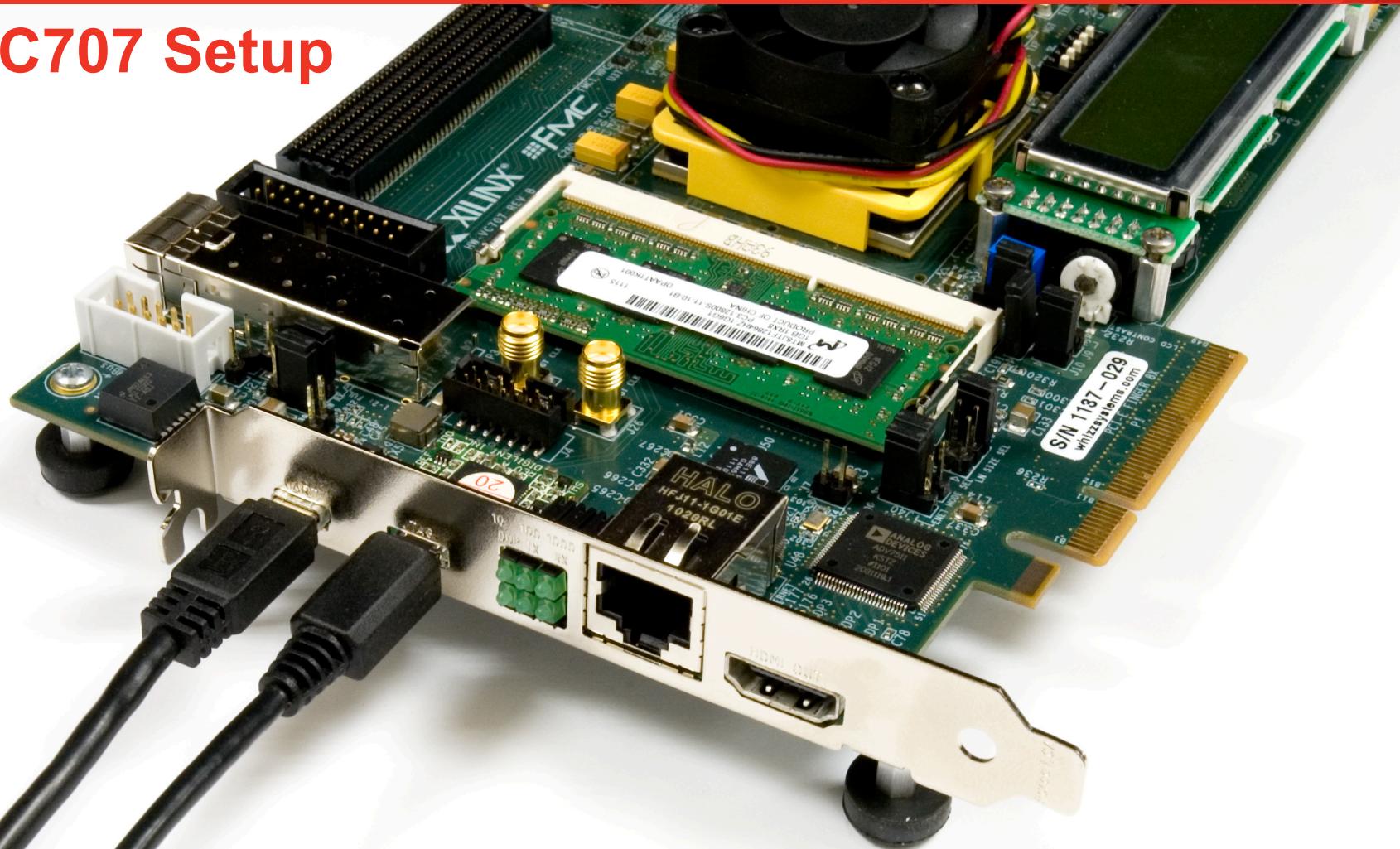


VC707 Setup



- **Connect a USB Type-A to Mini-B cable to the USB UART connector on the VC707 board**
 - Connect this cable to your PC

VC707 Setup

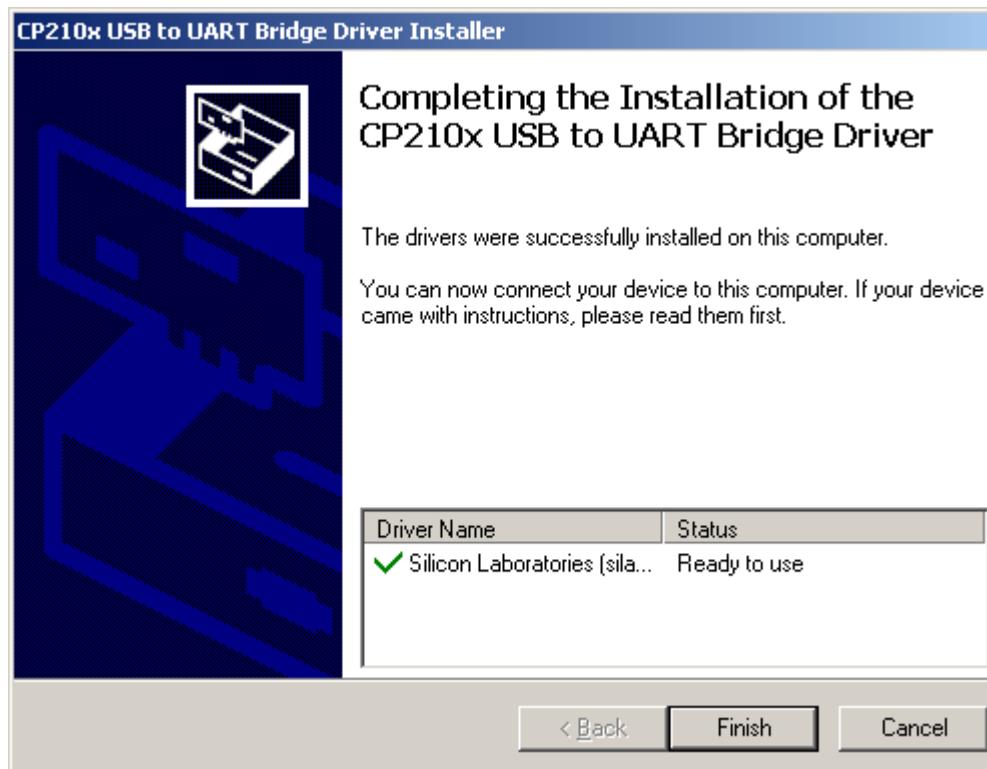


- **Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the VC707 board**
 - Connect this cable to your PC
 - Power on the VC707 board for UART Drivers Installation

VC707 Setup

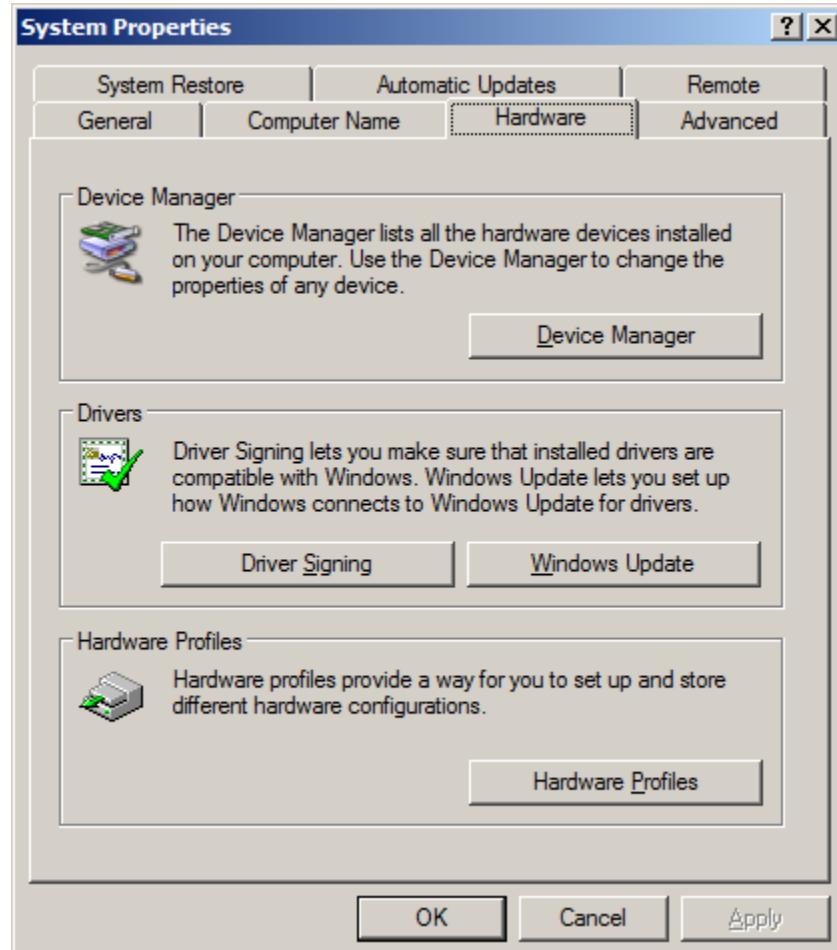
► Install USB UART Drivers

- Refer to [UG1033](#) for details on installing the USB to UART Drivers



VC707 Setup

- Reboot your PC if necessary
- Right-click on My Computer and select Properties
 - Select the Hardware tab
 - Click on Device Manager

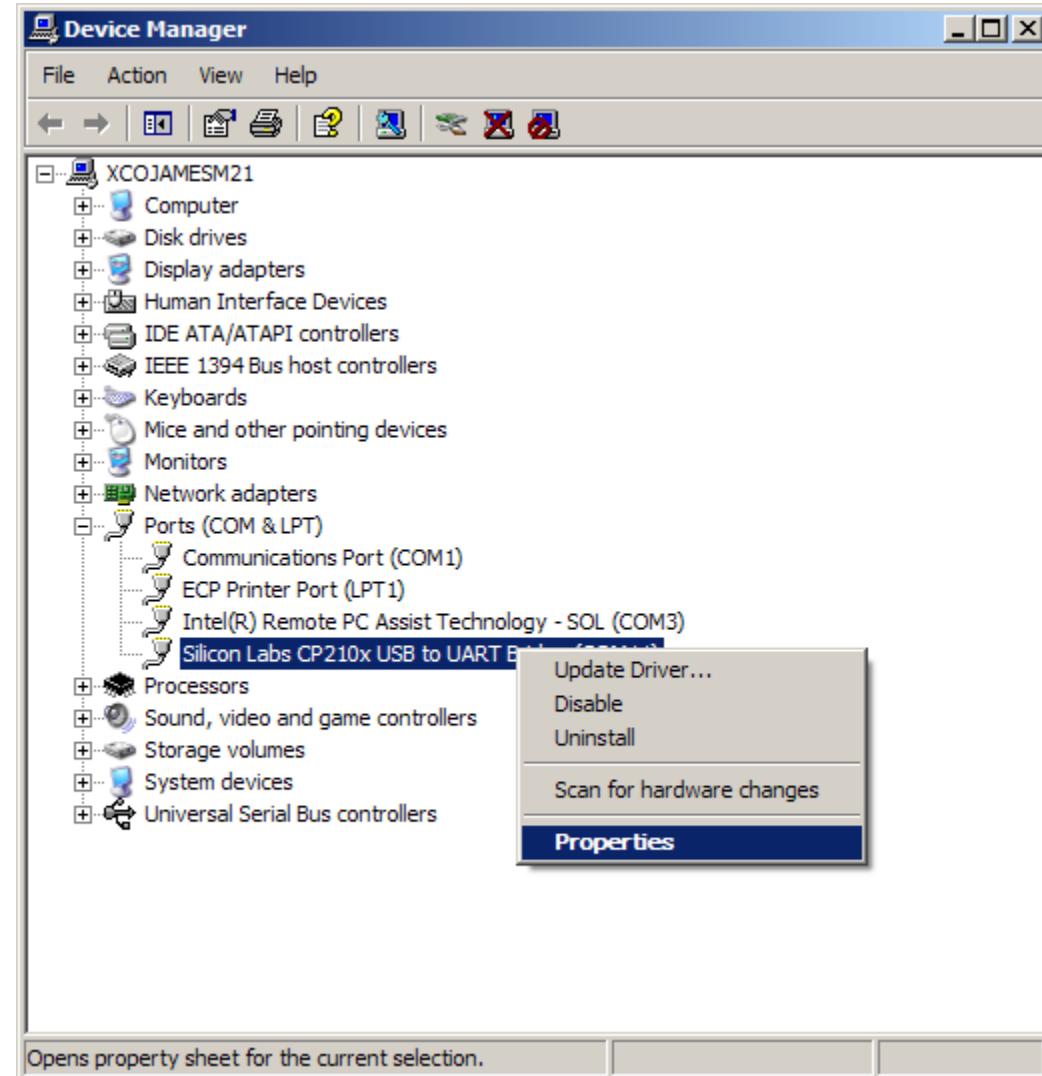


VC707 Setup

► Expand the Ports

Hardware

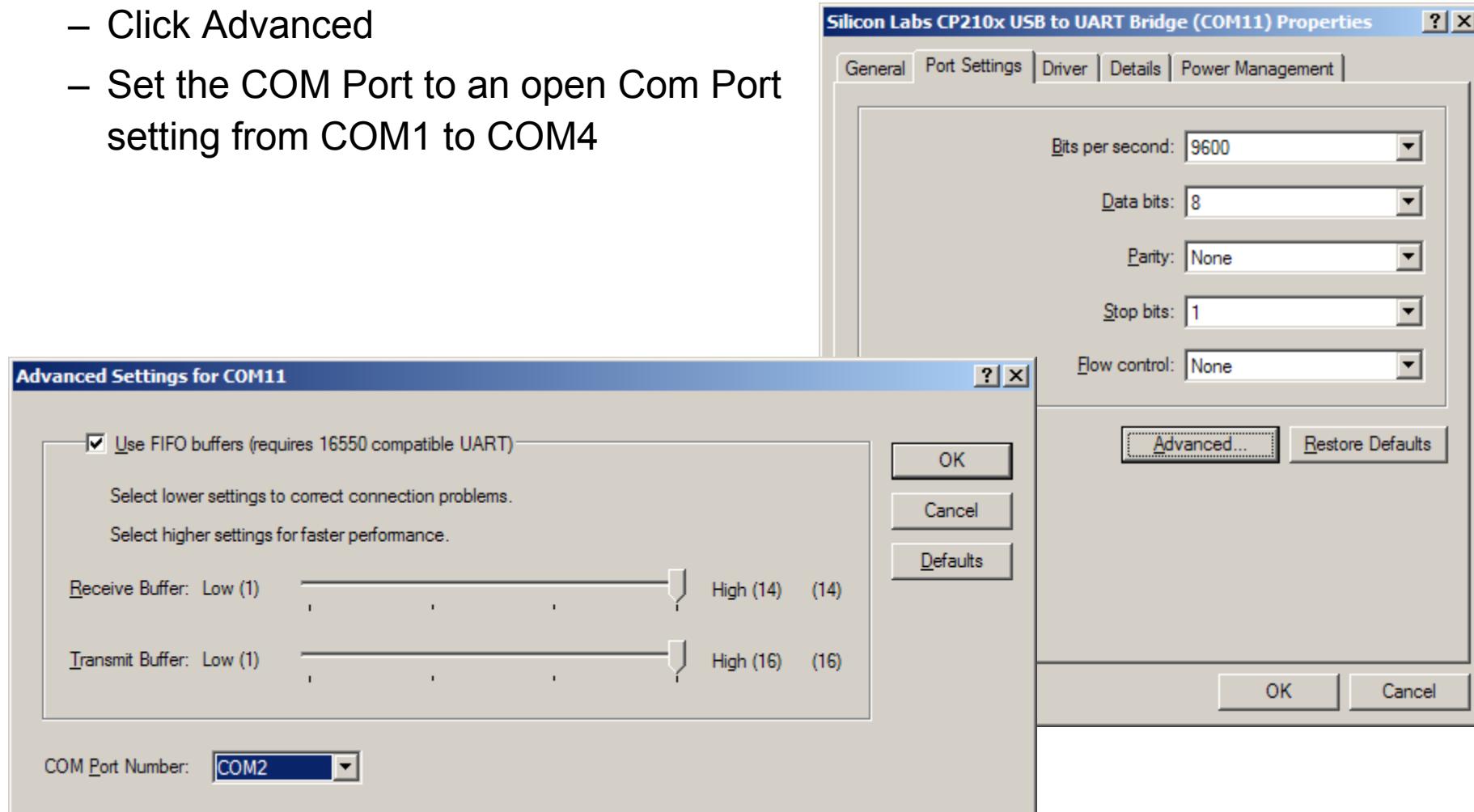
- Right-click on Silicon Labs CP210x USB to UART Bridge and select Properties



VC707 Setup

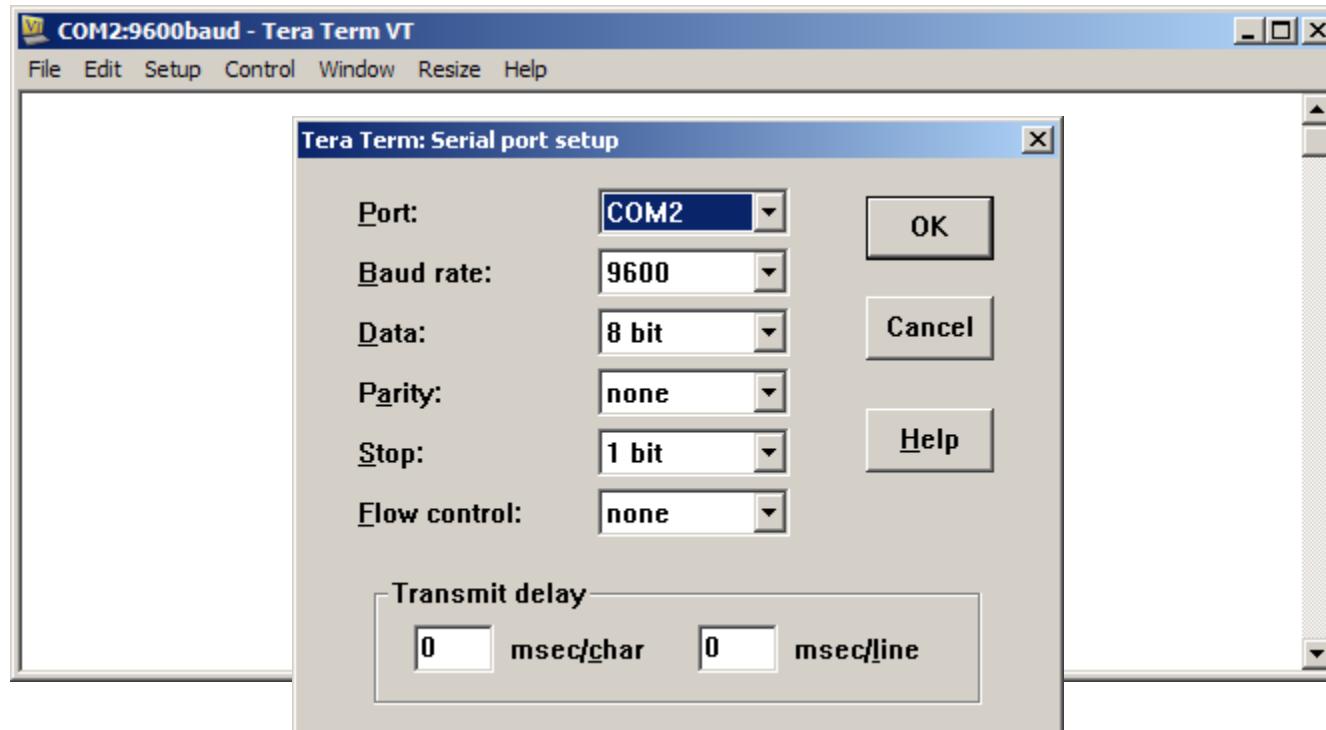
► Under Port Settings tab

- Click Advanced
- Set the COM Port to an open Com Port setting from COM1 to COM4



VC707 Setup

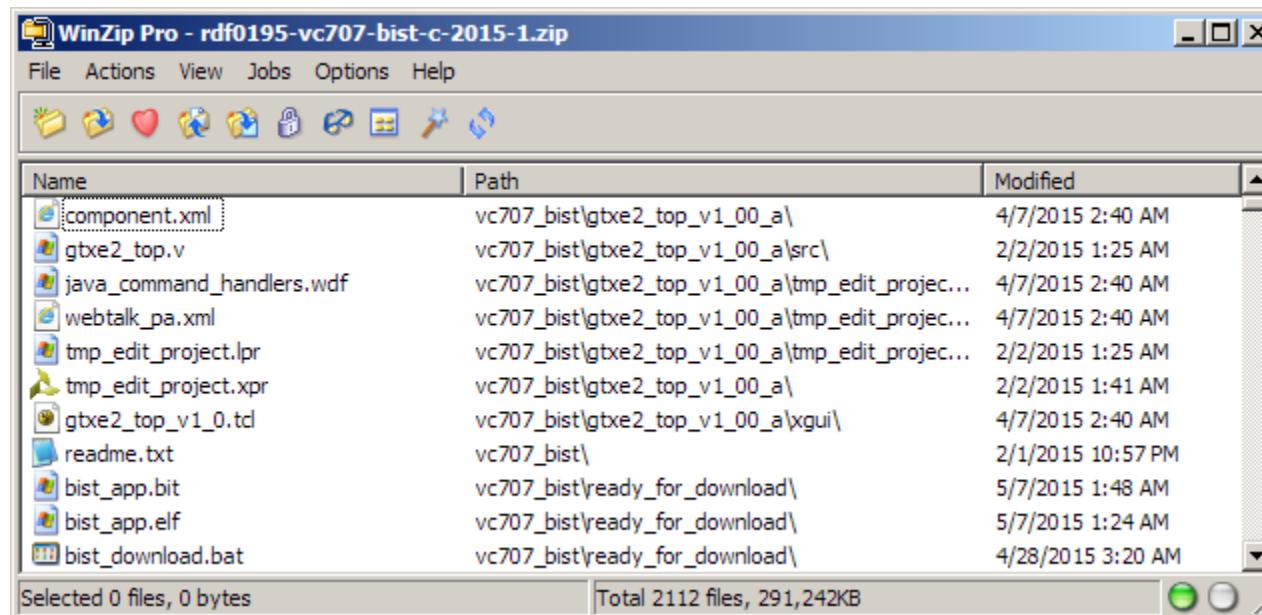
- Refer to [UG1036](#) regarding Tera Term installation
- Board Power must be on before starting Tera Term
- Start the Terminal Program
 - Select your USB Com Port
 - Set the baud to 9600



VC707 Setup

► Unzip the VC707 BIST Design Files (2015.1 C) ZIP file

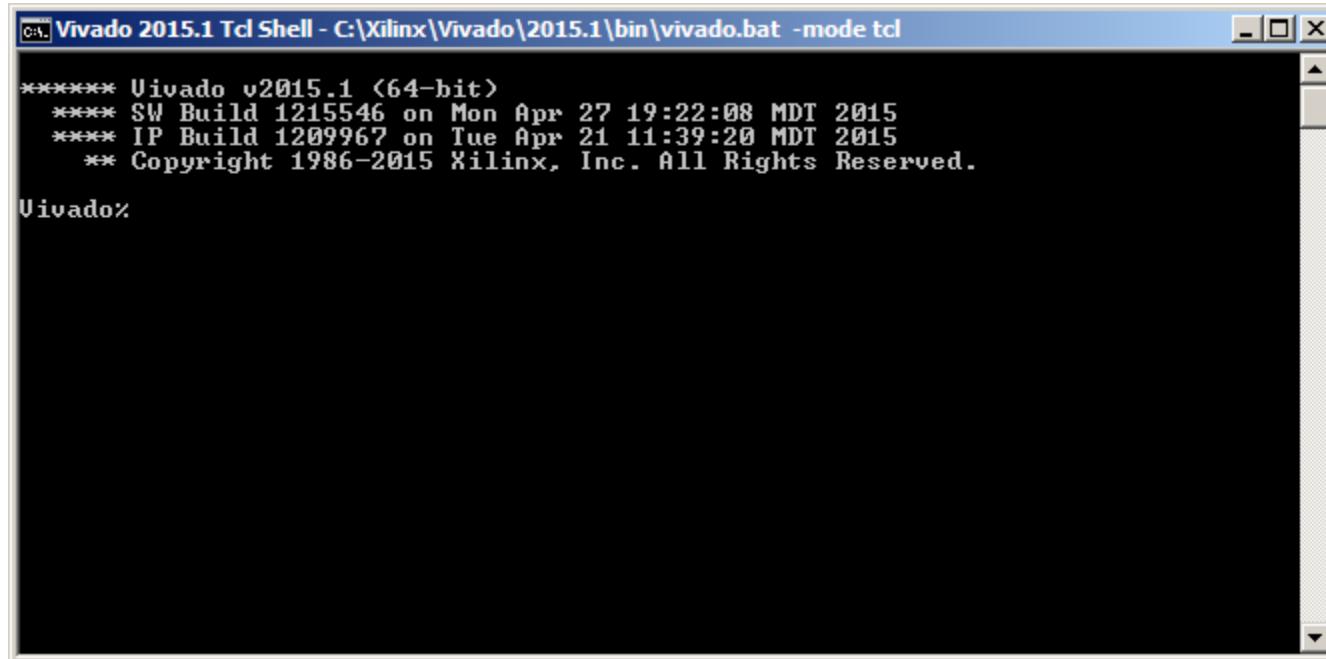
- Available through <http://www.xilinx.com/vc707>



VC707 BIST

► Open a Vivado Tcl Shell:

**Start → All Programs → Xilinx Design Tools → Vivado 2015.1 →
Vivado 2015.1 Tcl Shell**



The screenshot shows a terminal window titled "Vivado 2015.1 Tcl Shell - C:\Xilinx\Vivado\2015.1\bin\vivado.bat -mode tcl". The window displays the following startup message:

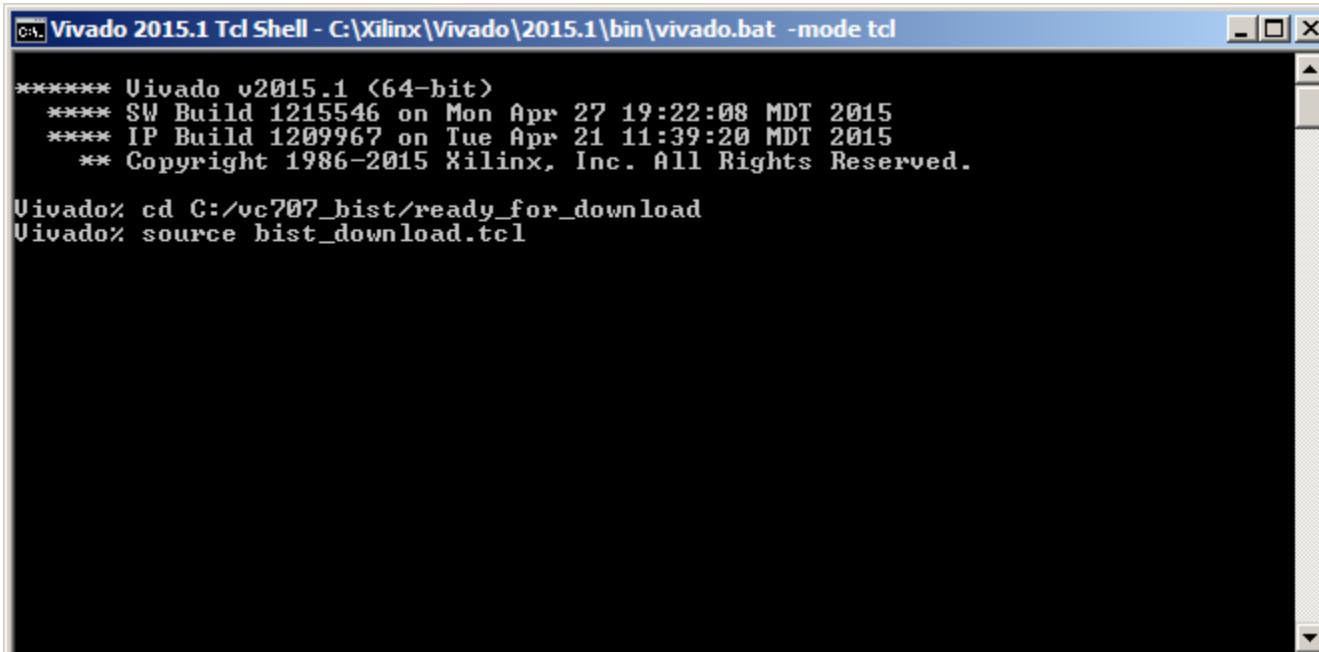
```
***** Vivado v2015.1 (64-bit)
***** SW Build 1215546 on Mon Apr 27 19:22:08 MDT 2015
***** IP Build 1209967 on Tue Apr 21 11:39:20 MDT 2015
** Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.
```

The prompt "Vivado%" is visible at the bottom of the window.

VC707 BIST

- Download the BIST bitstream with Vivado
- In the Vivado Tcl Shell type:

```
cd C:/vc707_bist/ready_for_download  
source bist_download.tcl
```

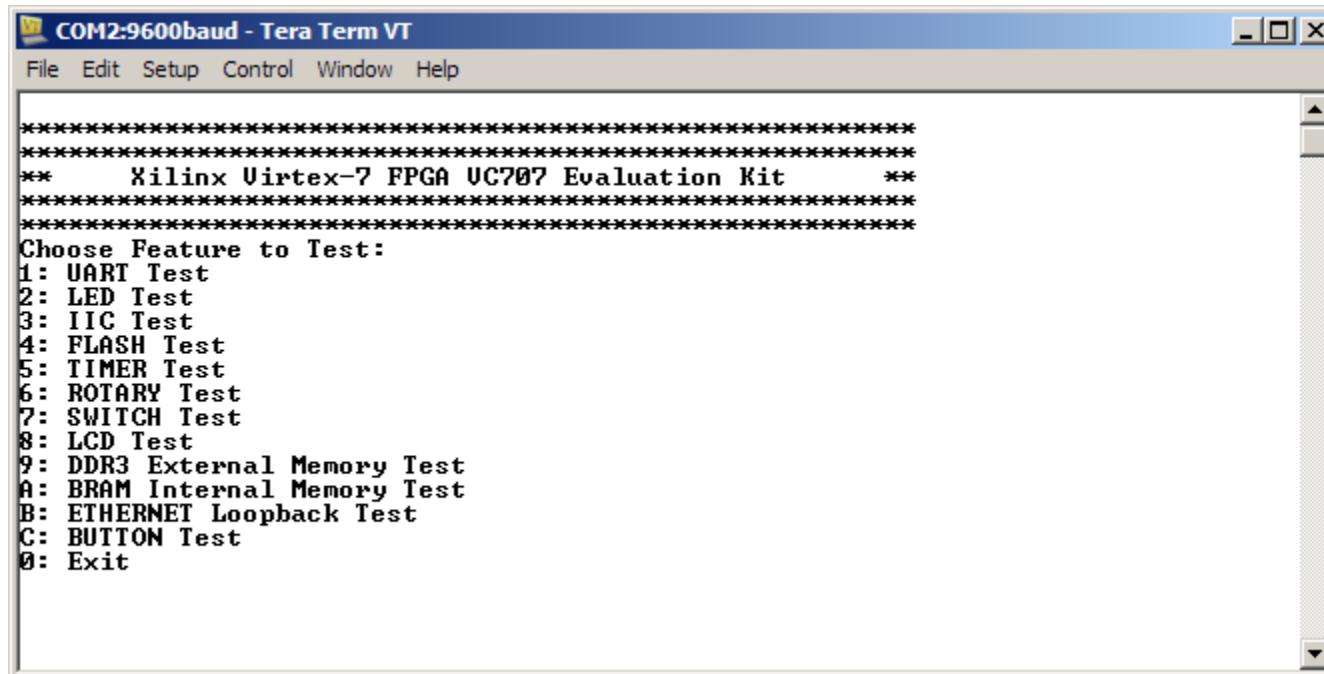


The screenshot shows a Windows command-line interface window titled "Vivado 2015.1 Tcl Shell - C:\Xilinx\Vivado\2015.1\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2015.1 (64-bit)  
***** SW Build 1215546 on Mon Apr 27 19:22:08 MDT 2015  
***** IP Build 1209967 on Tue Apr 21 11:39:20 MDT 2015  
** Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/vc707_bist/ready_for_download  
Vivado> source bist_download.tcl
```

VC707 BIST

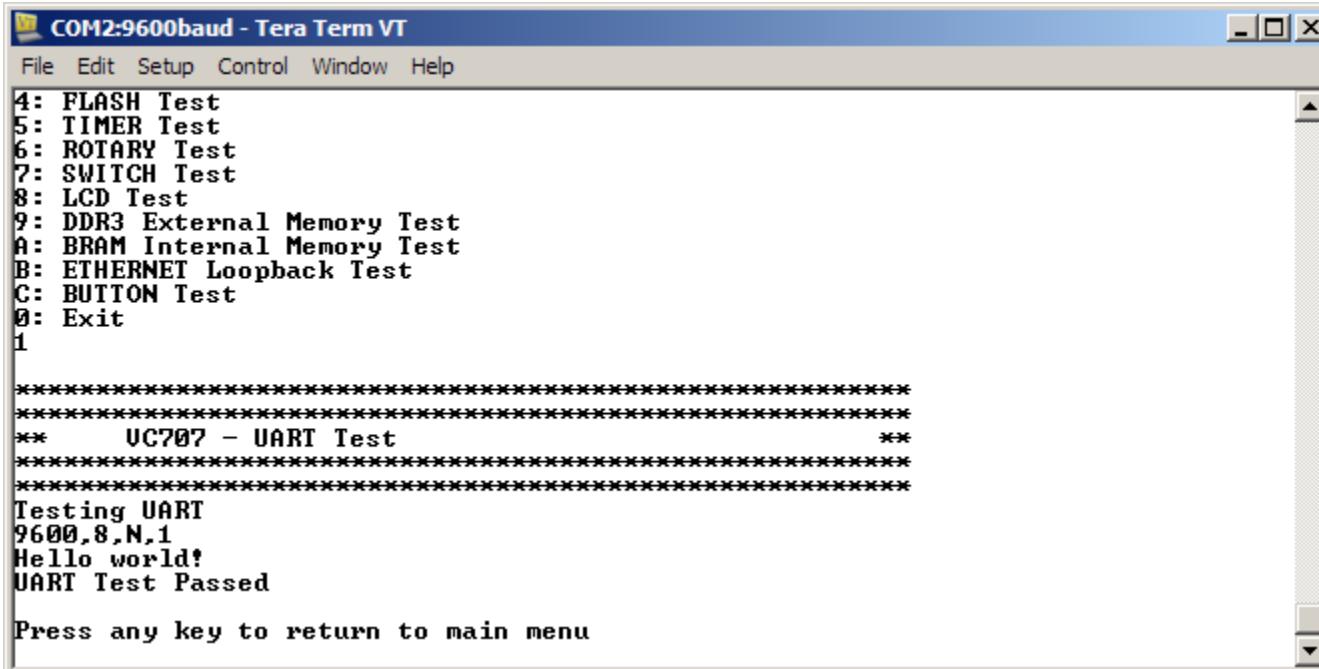
► View initial BIST screen



VC707 BIST

➤ UART Test

- Type “1” to start the UART Test
- After each test, press any key to return to the main menu



The screenshot shows a terminal window titled "COM2:9600baud - Tera Term VT". The menu at the top includes File, Edit, Setup, Control, Window, and Help. The main area displays a test menu:

```
4: FLASH Test
5: TIMER Test
6: ROTARY Test
7: SWITCH Test
8: LCD Test
9: DDR3 External Memory Test
A: BRAM Internal Memory Test
B: ETHERNET Loopback Test
C: BUTTON Test
0: Exit
1
```

Following the menu, the text "*****" appears twice, followed by the title "** UC707 - UART Test **". Below this, the output of the test is shown:

```
Testing UART
9600,8,N,1
Hello world!
UART Test Passed
```

At the bottom, the message "Press any key to return to main menu" is displayed.

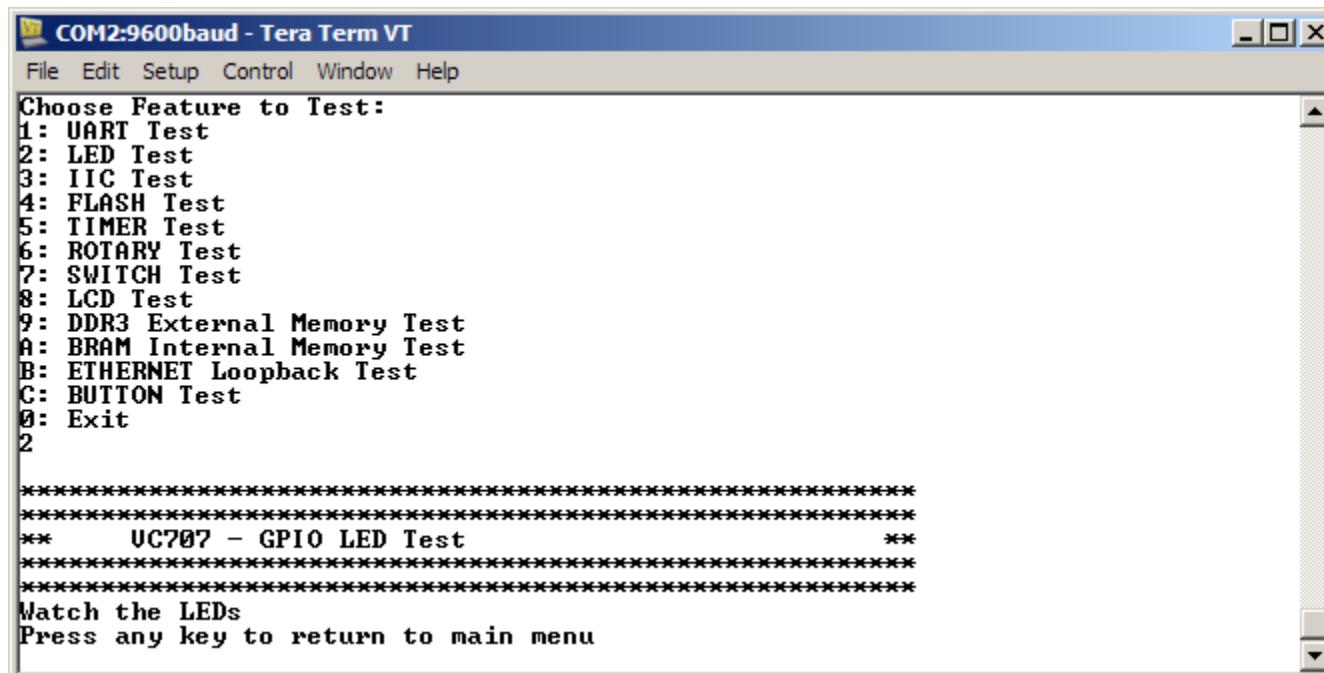
VC707 BIST

➤ LED Test

- Type **2** to begin LED Test

➤ View Walking 1's pattern on GPIO LEDs

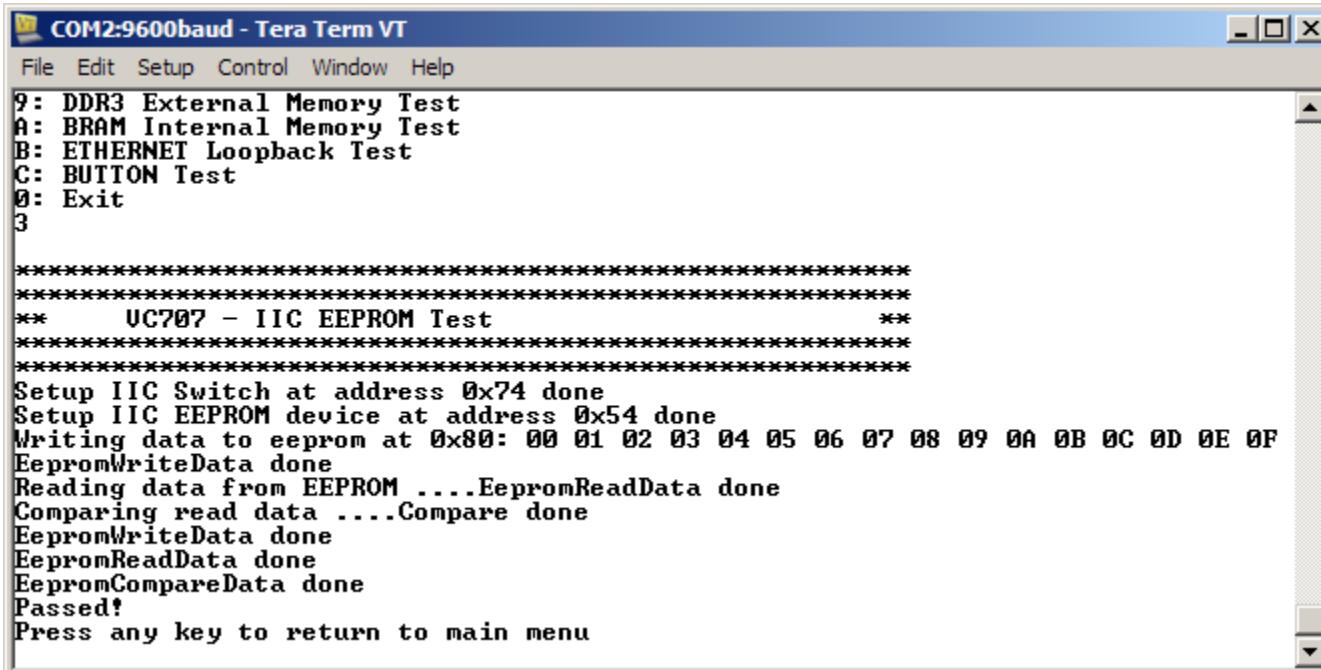
- Sequence repeats twice



VC707 BIST

► IIC Test

- Type 3 to begin IIC Test



The screenshot shows a terminal window titled "COM2:9600baud - Tera Term VT". The menu bar includes File, Edit, Setup, Control, Window, and Help. The main window displays a test menu:

```
9: DDR3 External Memory Test
A: BRAM Internal Memory Test
B: ETHERNET Loopback Test
C: BUTTON Test
0: Exit
3
```

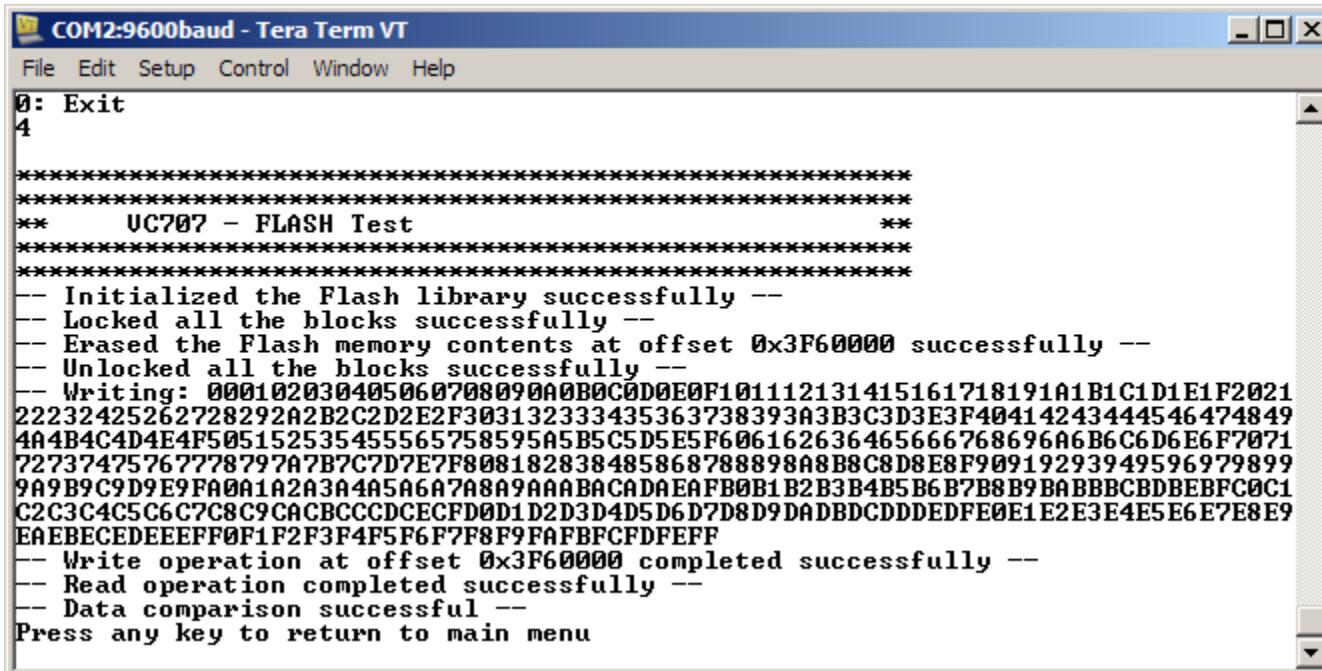
Following the selection of option 3, the window displays the output of the IIC EEPROM Test:

```
*****
**      UC707 - IIC EEPROM Test      **
*****
Setup IIC Switch at address 0x74 done
Setup IIC EEPROM device at address 0x54 done
Writing data to eeprom at 0x80: 00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F
EepromWriteData done
Reading data from EEPROM ....EepromReadData done
Comparing read data ....Compare done
EepromWriteData done
EepromReadData done
EepromCompareData done
Passed!
Press any key to return to main menu
```

VC707 BIST

► Flash Test

- Type 4 to begin Flash test



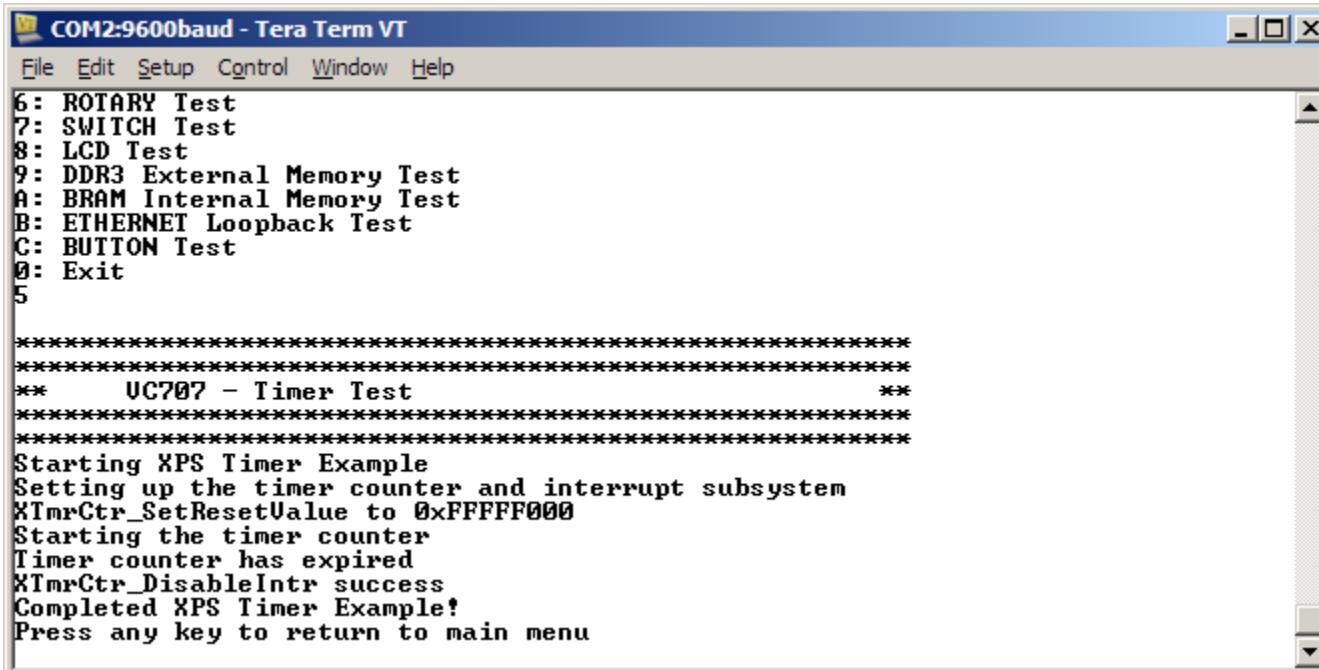
The screenshot shows a terminal window titled "COM2:9600baud - Tera Term VT". The window contains the following text output:

```
0: Exit
4
*****
** UC707 - FLASH Test **
*****
-- Initialized the Flash library successfully --
-- Locked all the blocks successfully --
-- Erased the Flash memory contents at offset 0x3F60000 successfully --
-- Unlocked all the blocks successfully --
-- Writing: 000102030405060708090A0B0C0D0E0F101112131415161718191A1B1C1D1E1F2021
22232425262728292A2B2C2D2E2F303132333435363738393A3B3C3D3E3F40414243444546474849
4A4B4C4D4E4F505152535455565758595A5B5C5D5E5F606162636465666768696A6B6C6D6E6F7071
72737475767778797A7B7C7D7E7F808182838485868788898A8B8C8D8E8F90919293949596979899
9A9B9C9D9E9FA0A1A2A3A4A5A6A7A8A9AAABACADAEAFB0B1B2B3B4B5B6B7B8B9BABBBBCDBEBFC0C1
C2C3C4C5C6C7C8C9CACBCCCCECFD0D1D2D3D4D5D6D7D8D9DADBDCCDDDEDFE0E1E2E3E4E5E6E7E8E9
EAEBECEDEEFF0F1F2F3F4F5F6F7F8F9FAFBFCFDFEFF
-- Write operation at offset 0x3F60000 completed successfully --
-- Read operation completed successfully --
-- Data comparison successful --
Press any key to return to main menu
```

VC707 BIST

► Timer Test

- Type **5** to begin Timer Test



The screenshot shows a terminal window titled "COM2:9600baud - Tera Term VT". The menu bar includes File, Edit, Setup, Control, Window, and Help. The main window displays a list of test options:

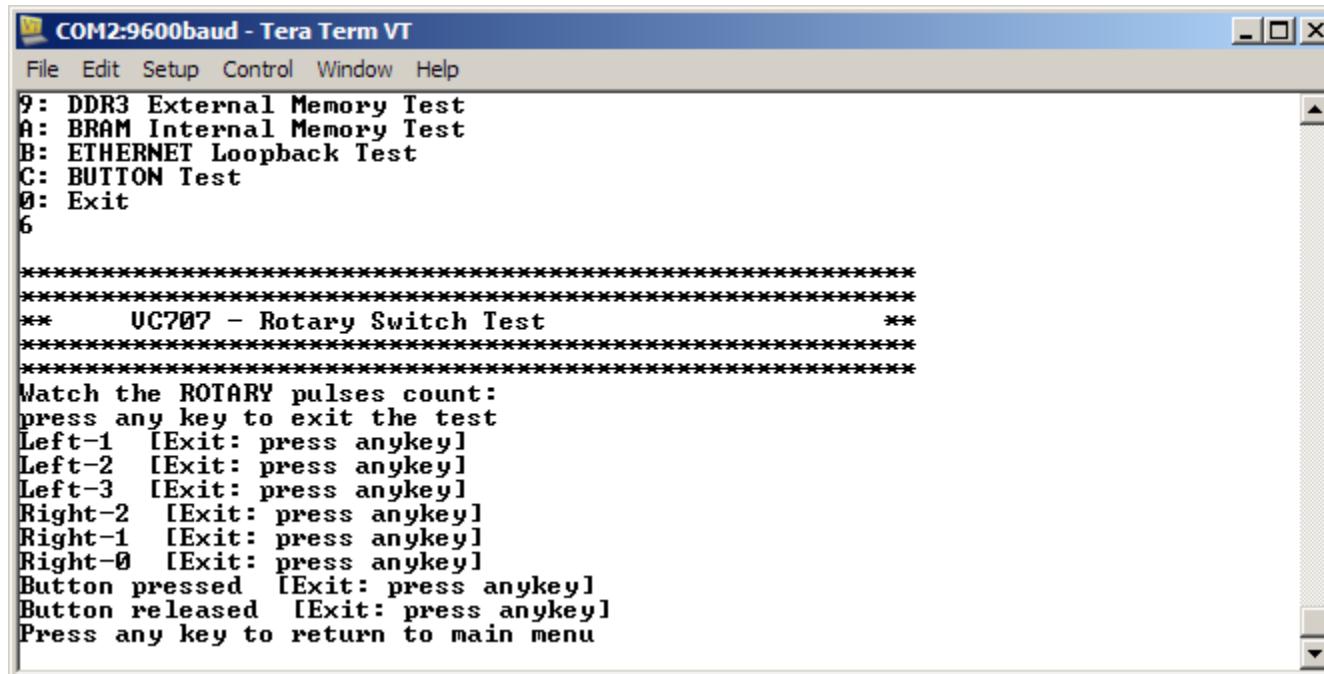
```
File Edit Setup Control Window Help
6: ROTARY Test
7: SWITCH Test
8: LCD Test
9: DDR3 External Memory Test
A: BRAM Internal Memory Test
B: ETHERNET Loopback Test
C: BUTTON Test
0: Exit
5

*****
** UC707 - Timer Test **
*****
Starting XPS Timer Example
Setting up the timer counter and interrupt subsystem
XTmrCtr_SetResetValue to 0xFFFFF000
Starting the timer counter
Timer counter has expired
XTmrCtr_DisableIntr success
Completed XPS Timer Example!
Press any key to return to main menu
```

VC707 BIST

► Rotary Test

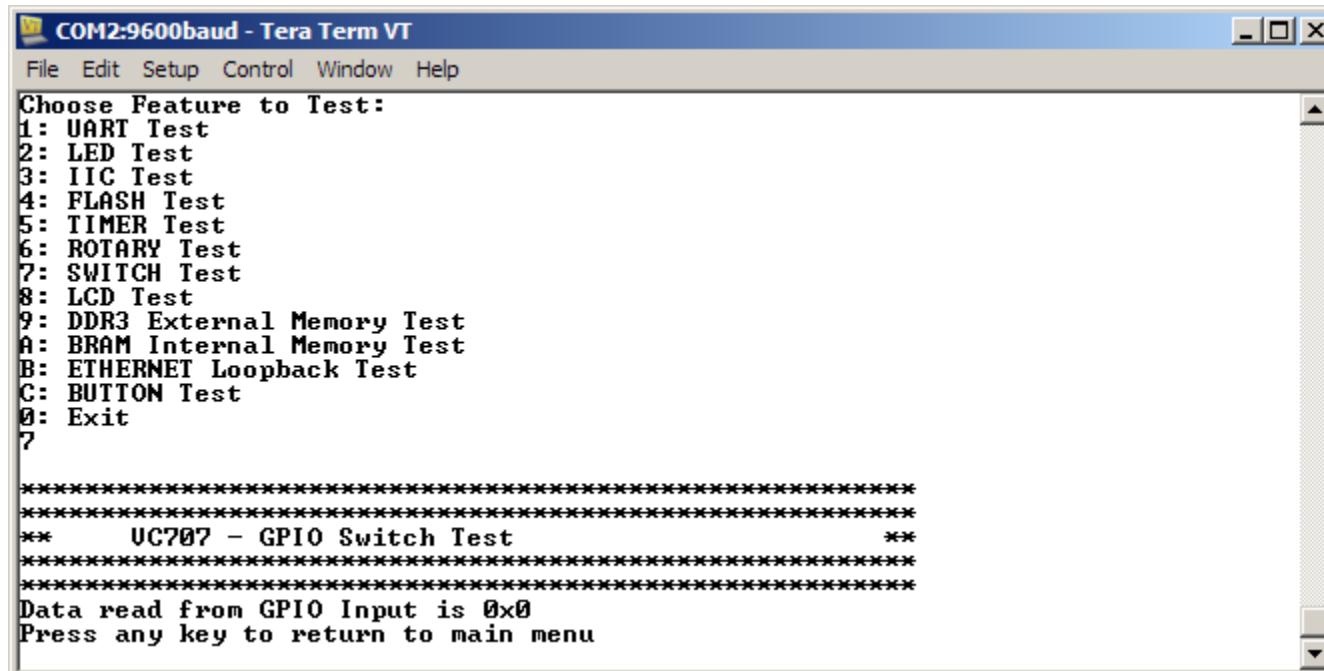
- Type **6** to begin Rotary Test
- Turn the rotary switch (under the LCD) back and forth
- Push the rotary switch inwards to actuate the push button switch



VC707 BIST

► GPIO Switch Test

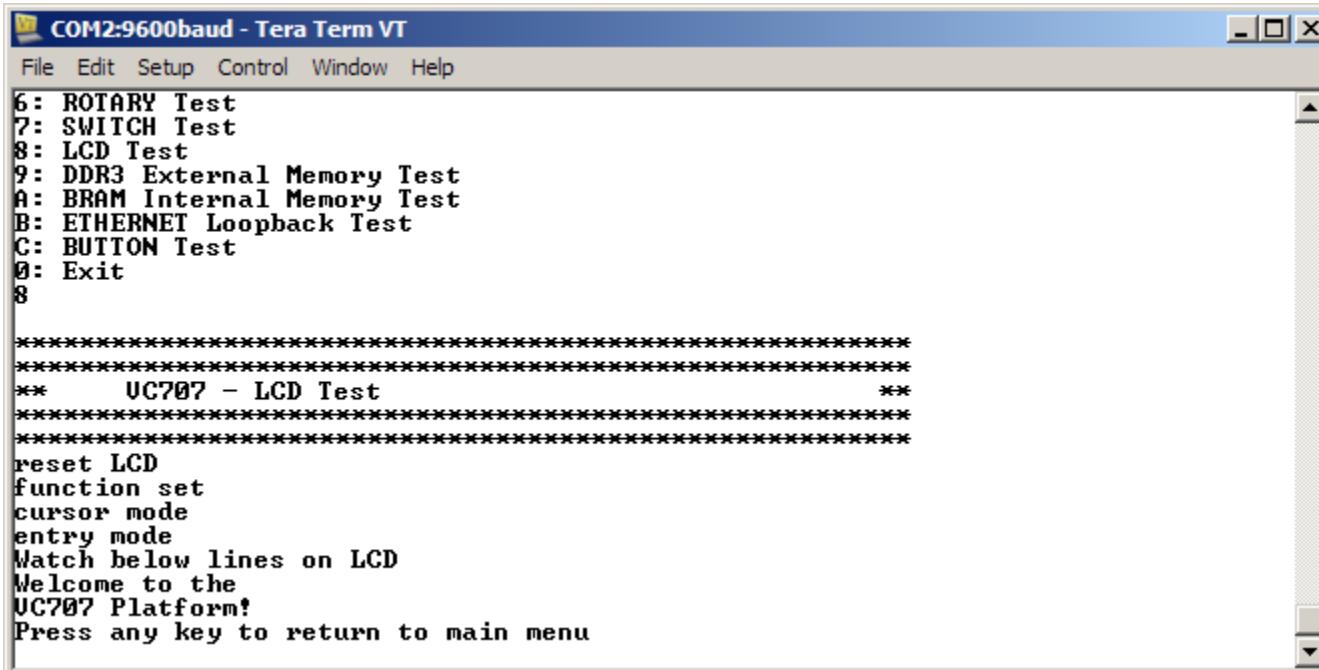
- Set 8-position GPIO DIP Switch (SW2)
- Type 7 to begin GPIO Switch Test
 - Reads switch settings



VC707 BIST

► LCD Test

- Type 8 to begin LCD Test



COM2:9600baud - Tera Term VT

File Edit Setup Control Window Help

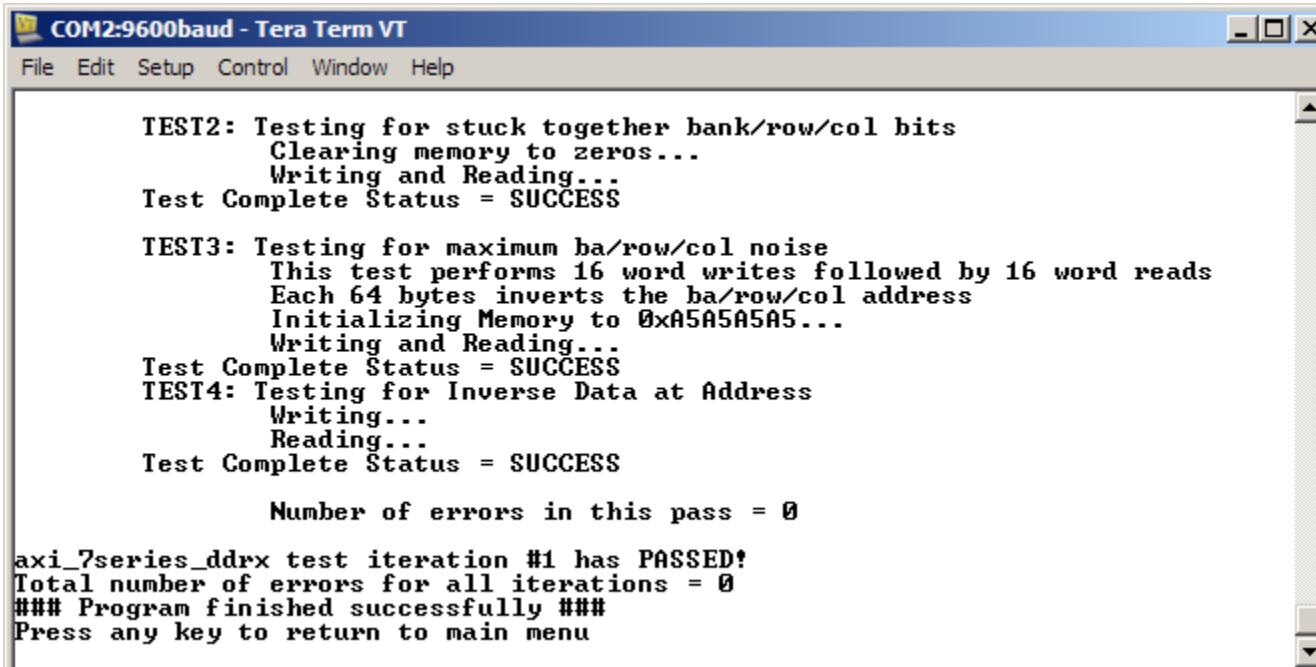
```
6: ROTARY Test
7: SWITCH Test
8: LCD Test
9: DDR3 External Memory Test
A: BRAM Internal Memory Test
B: ETHERNET Loopback Test
C: BUTTON Test
0: Exit
8

*****
**      UC707 - LCD Test      **
*****
reset LCD
function set
cursor mode
entry mode
Watch below lines on LCD
Welcome to the
UC707 Platform!
Press any key to return to main menu
```

VC707 BIST

► External Memory Test

- Type **9** to begin External Memory Test



The screenshot shows a terminal window titled "COM2:9600baud - Tera Term VT". The window contains the following text output from a BIST script:

```
TEST2: Testing for stuck together bank/row/col bits
Clearing memory to zeros...
Writing and Reading...
Test Complete Status = SUCCESS

TEST3: Testing for maximum ba/row/col noise
This test performs 16 word writes followed by 16 word reads
Each 64 bytes inverts the ba/row/col address
Initializing Memory to 0xA5A5A5A5...
Writing and Reading...
Test Complete Status = SUCCESS
TEST4: Testing for Inverse Data at Address
Writing...
Reading...
Test Complete Status = SUCCESS

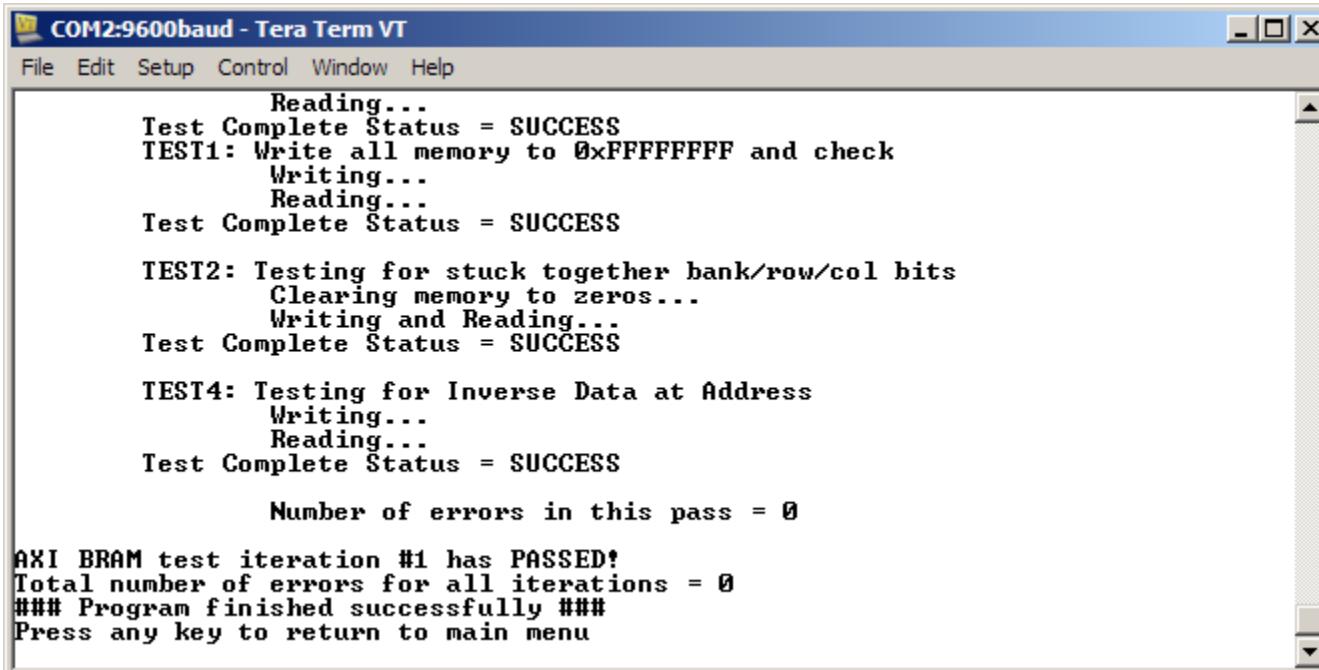
Number of errors in this pass = 0

axi_7series_ddrx test iteration #1 has PASSED!
Total number of errors for all iterations = 0
### Program finished successfully ####
Press any key to return to main menu
```

VC707 BIST

► Internal Memory Test

- Type A to begin BRAM Memory Test



The screenshot shows a terminal window titled "COM2:9600baud - Tera Term VT". The window contains the following text output from an AXI BRAM test:

```
Reading...
Test Complete Status = SUCCESS
TEST1: Write all memory to 0xFFFFFFFF and check
    Writing...
    Reading...
Test Complete Status = SUCCESS

TEST2: Testing for stuck together bank/row/col bits
    Clearing memory to zeros...
    Writing and Reading...
Test Complete Status = SUCCESS

TEST4: Testing for Inverse Data at Address
    Writing...
    Reading...
Test Complete Status = SUCCESS

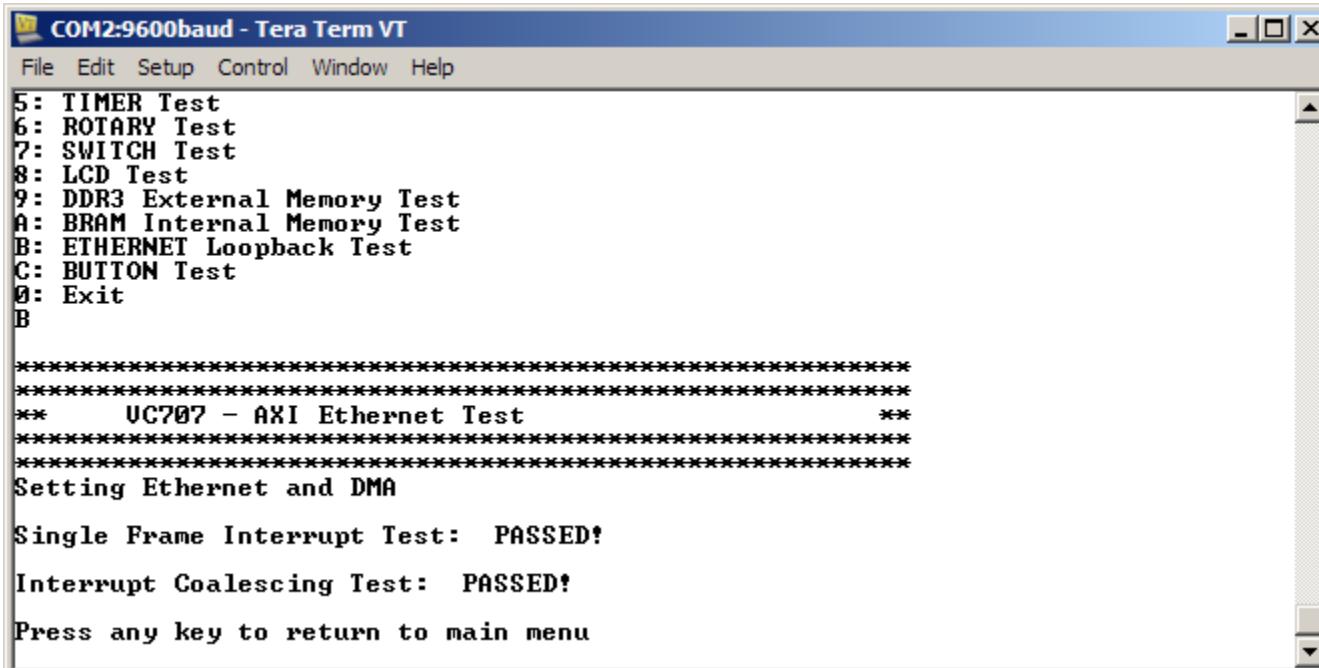
Number of errors in this pass = 0

AXI BRAM test iteration #1 has PASSED!
Total number of errors for all iterations = 0
### Program finished successfully ####
Press any key to return to main menu
```

VC707 BIST

► Ethernet Test

- Type **B** to begin AXI Ethernet Test



COM2:9600baud - Tera Term VT

File Edit Setup Control Window Help

```
5: TIMER Test
6: ROTARY Test
7: SWITCH Test
8: LCD Test
9: DDR3 External Memory Test
A: BRAM Internal Memory Test
B: ETHERNET Loopback Test
C: BUTTON Test
0: Exit
B

*****
**      UC707 - AXI Ethernet Test      **
*****
Setting Ethernet and DMA

Single Frame Interrupt Test: PASSED!
Interrupt Coalescing Test: PASSED!
Press any key to return to main menu
```

VC707 BIST

► Button Test

- Type **B** to begin Button Test



```
COM2:9600baud - Tera Term VT
File Edit Setup Control Window Help
B: ETHERNET Loopback Test
C: BUTTON Test
Q: Exit
C

*****
** UC707 - Button Test **
*****
Press west button
Press south button
Press east button
Press north button
Press center button
Press any button
Press any key to return to main menu
```

Run the USB Design



Caution



► This procedure will format a disk drive

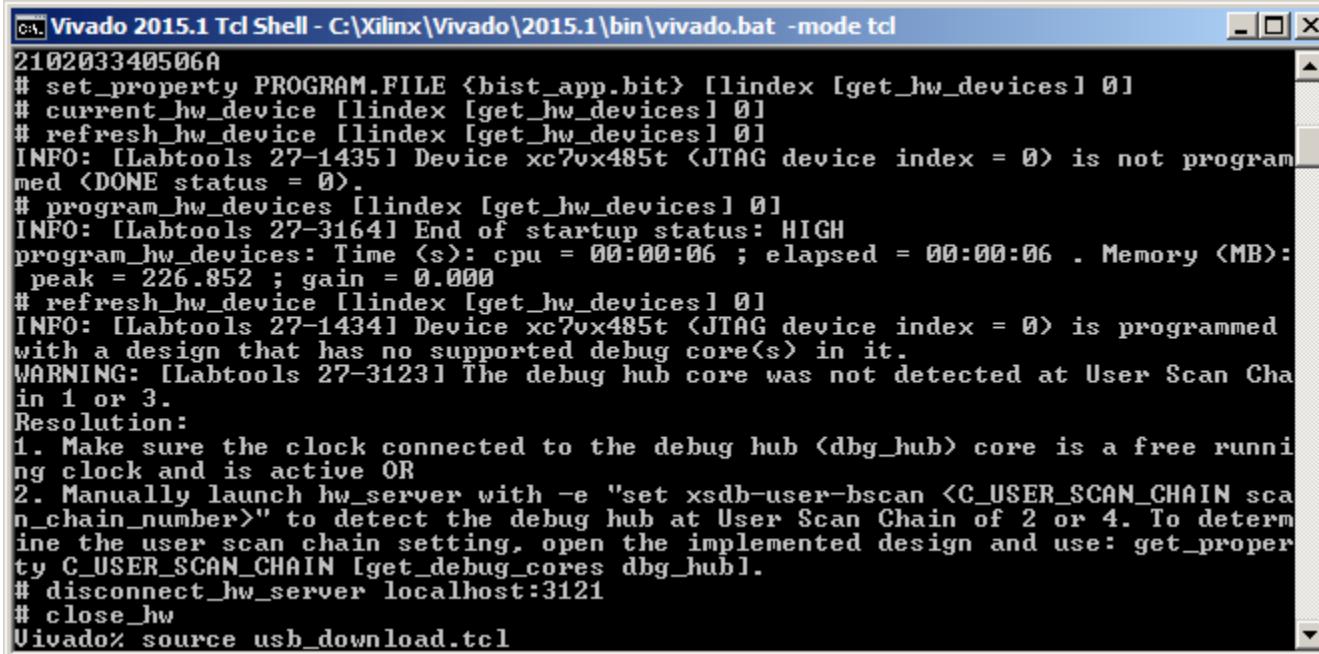
- Make sure you are formatting the VC707 USB Flash and not your PC's hard drive
- Drive letters mentioned in this procedure will vary from PC to PC - **Verify** the drive letter before formatting

► Xilinx cannot take responsibility for lost data or damaged hard drives



Run the USB Design

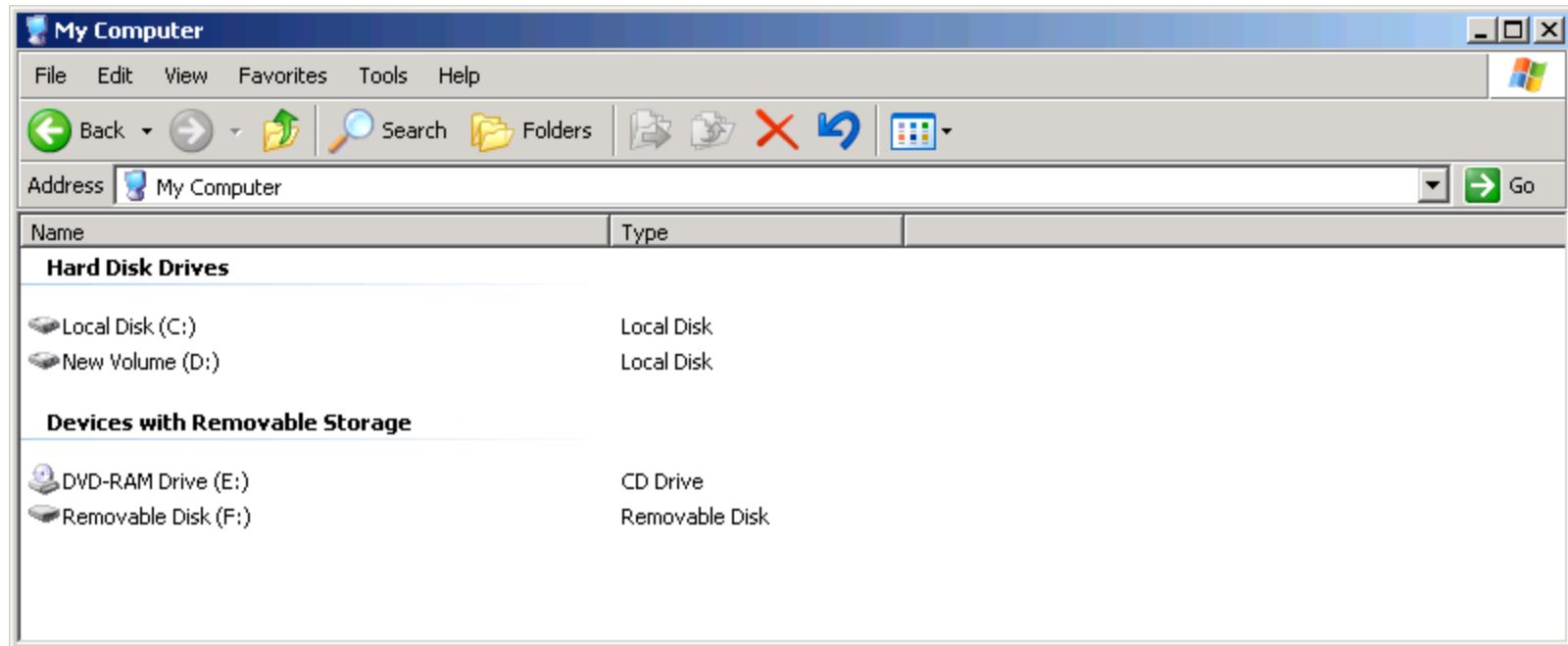
- Download the USB bitstream with Vivado
- In the Vivado Tcl Shell type:
source usb_download.tcl



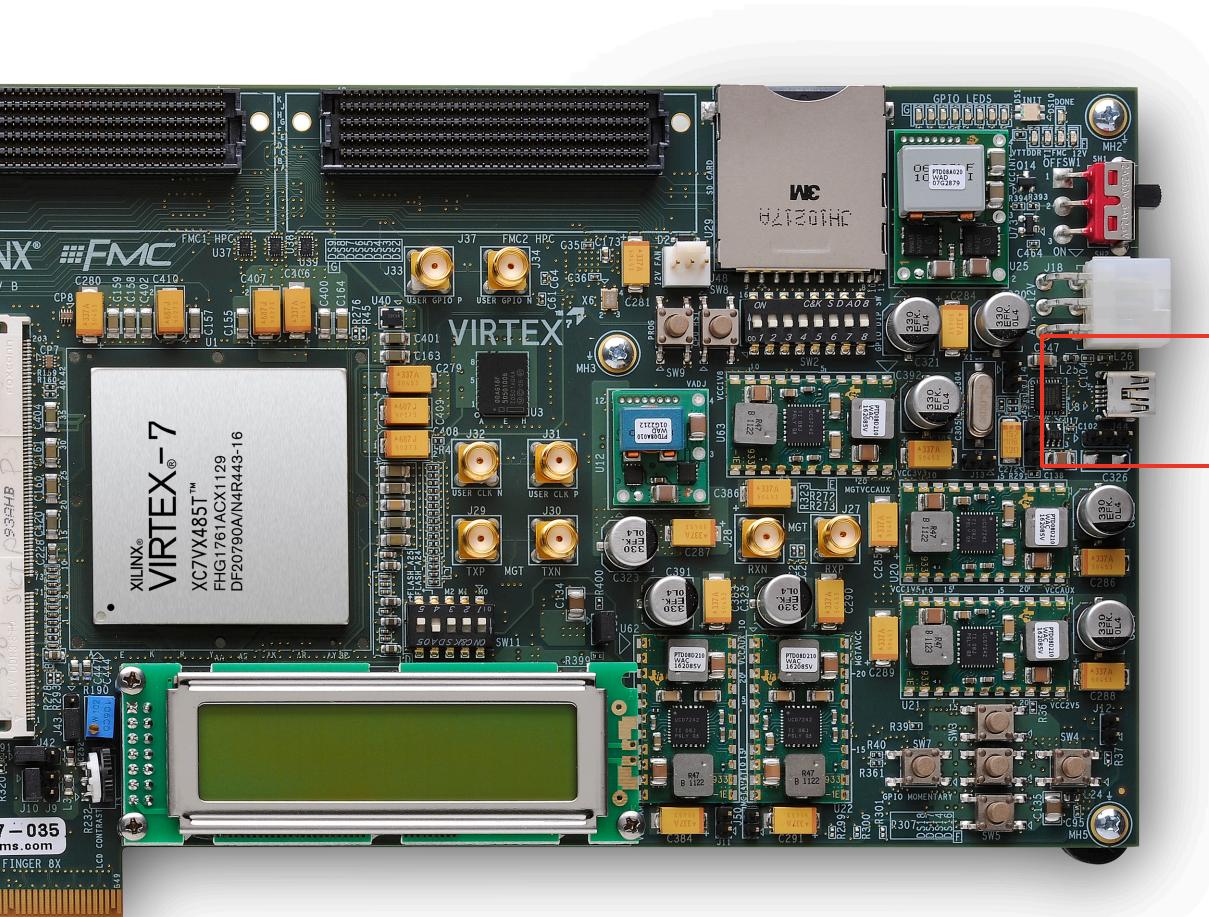
```
210203340506A
# set_property PROGRAM.FILE {bist_app.bit} [lindex [get_hw_devices] 0]
# current_hw_device [lindex [get_hw_devices] 0]
# refresh_hw_device [lindex [get_hw_devices] 0]
INFO: [Labtools 27-1435] Device xc7vx485t (JTAG device index = 0) is not programmed (DONE status = 0).
# program_hw_devices [lindex [get_hw_devices] 0]
INFO: [Labtools 27-3164] End of startup status: HIGH
program_hw_devices: Time <s>: cpu = 00:00:06 ; elapsed = 00:00:06 . Memory <MB>:
peak = 226.852 ; gain = 0.000
# refresh_hw_device [lindex [get_hw_devices] 0]
INFO: [Labtools 27-1434] Device xc7vx485t (JTAG device index = 0) is programmed with a design that has no supported debug core(s) in it.
WARNING: [Labtools 27-3123] The debug hub core was not detected at User Scan Chain 1 or 3.
Resolution:
1. Make sure the clock connected to the debug hub (dbg_hub) core is a free running clock and is active OR
2. Manually launch hw_server with -e "set xsdb-user-bscan <C_USER_SCAN_CHAIN scan_chain_number>" to detect the debug hub at User Scan Chain of 2 or 4. To determine the user scan chain setting, open the implemented design and use: get_property C_USER_SCAN_CHAIN [get_debug_cores dbg_hub].
# disconnect_hw_server localhost:3121
# close_hw
Vivado> source usb_download.tcl
```

Run the USB Design

- ▶ View your current set of disk drives



Run the USB Design



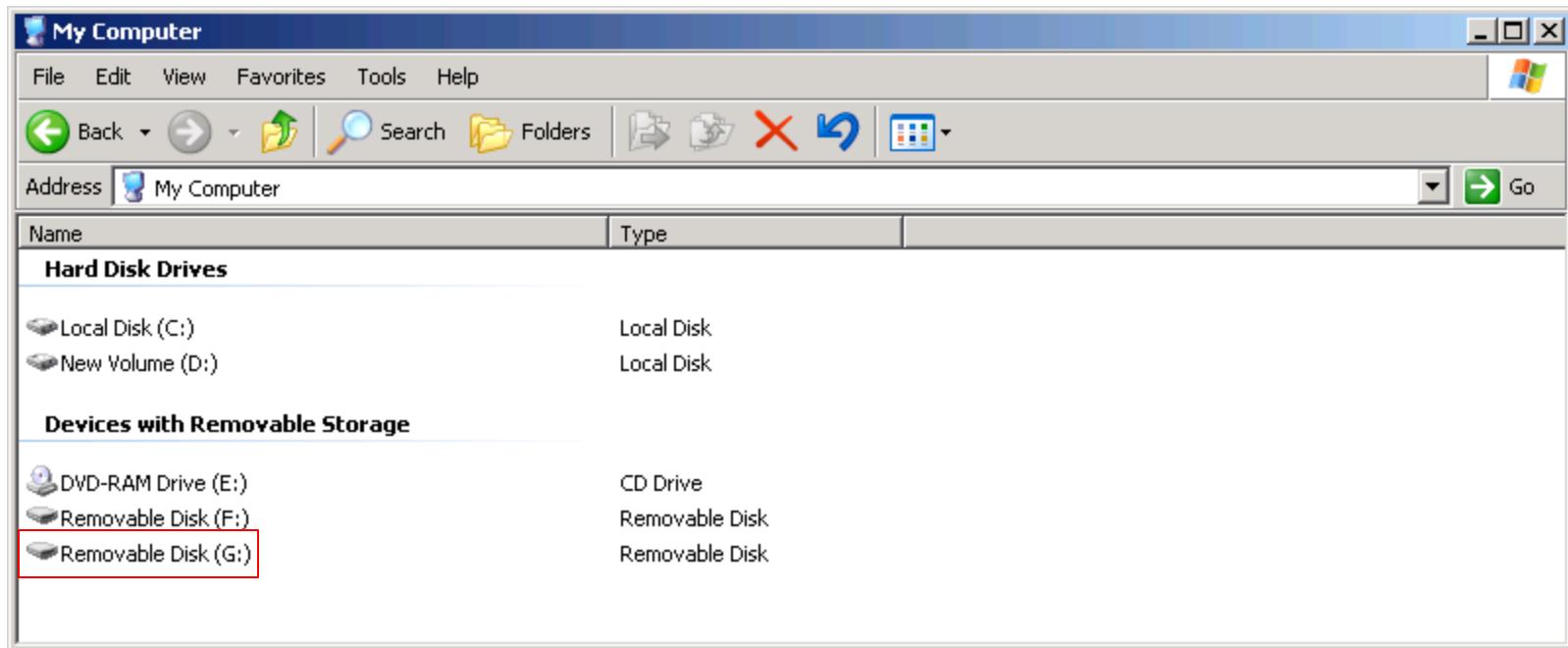
- Connect a USB Type-A to Mini-B cable to the USB PHY connector on the VC707 board
 - Connect this cable to your PC

Note: Presentation applies to the VC707

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Run the USB Design

- An extra removable drive will appear
 - In this case, “G:”



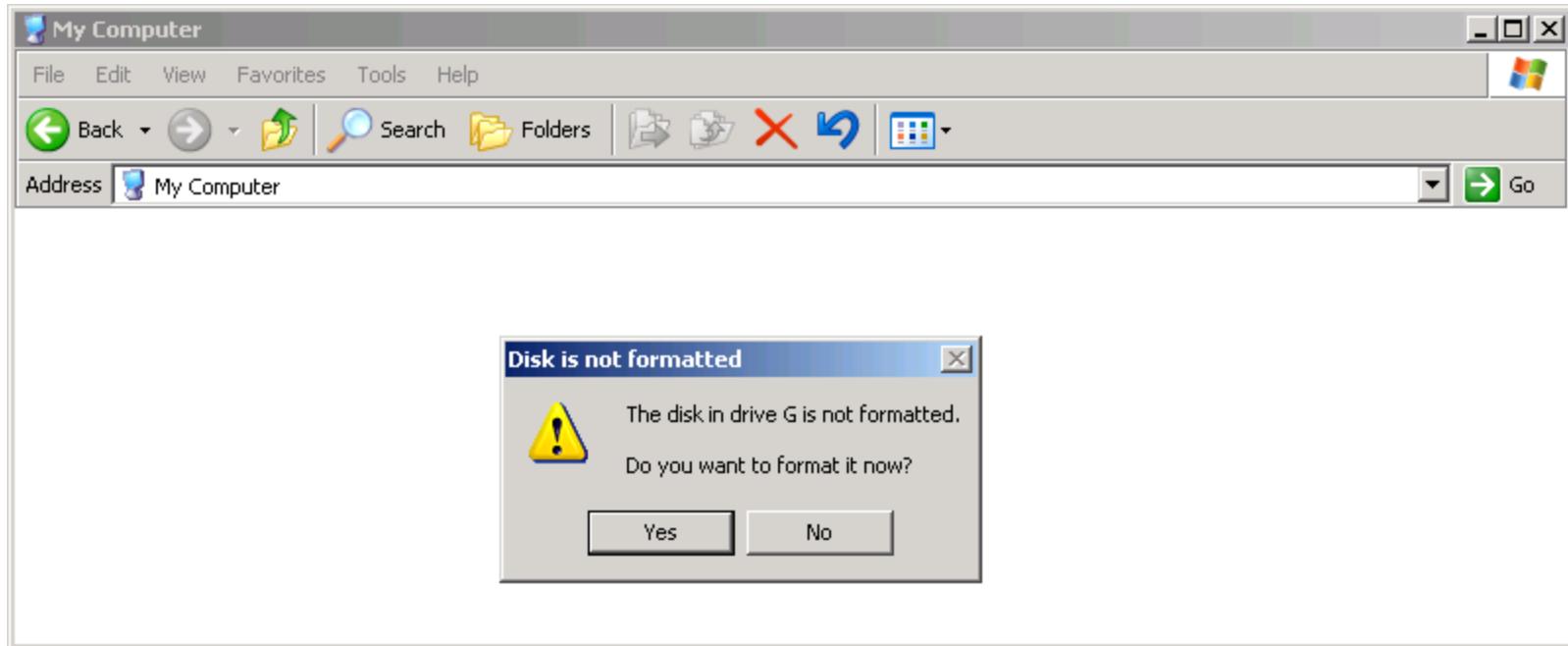
Run the USB Design

► Open the “G:” drive

- A “Disk is not formatted” message will appear



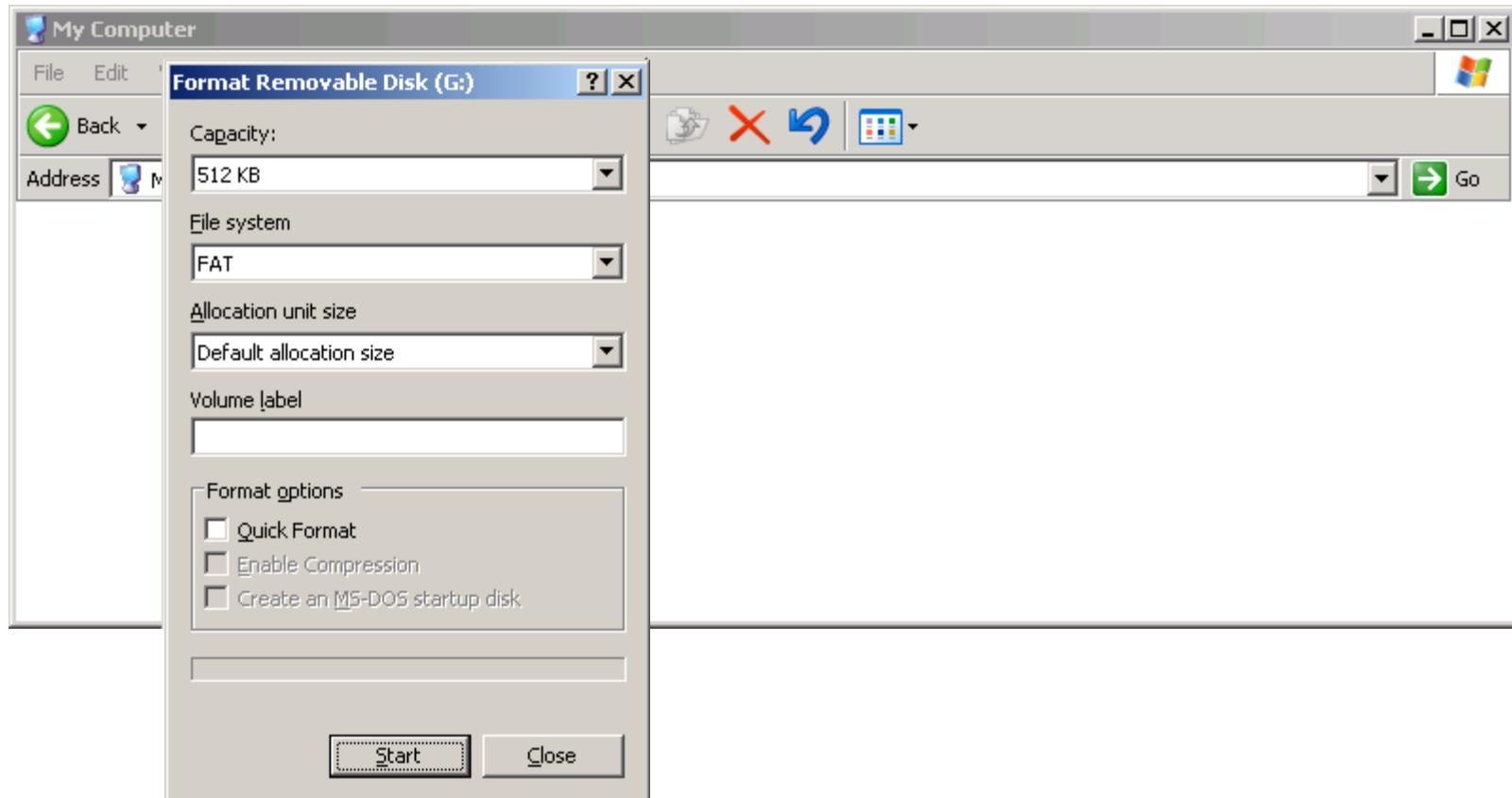
If this is the correct drive, click **Yes**



Run the USB Design

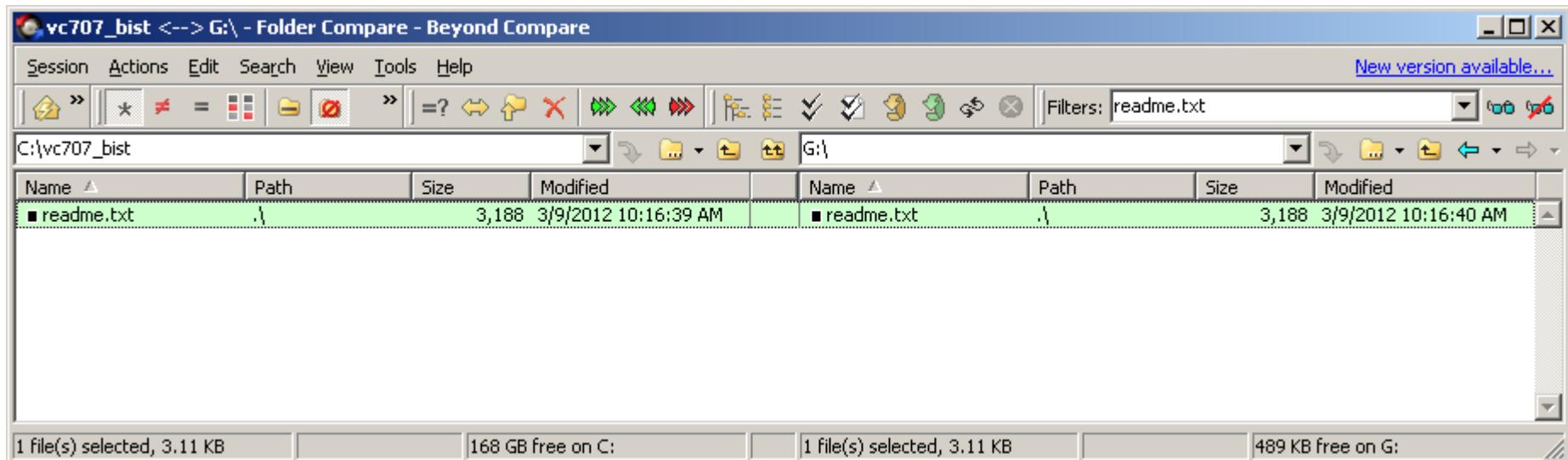
► A format dialog for drive G: will appear

- The size should be 512 KB
- If this is the correct, click **Start**
- Close this dialog when done



Run the USB Design

- At this point, you can copy small files to G: and verify the operation of this drive



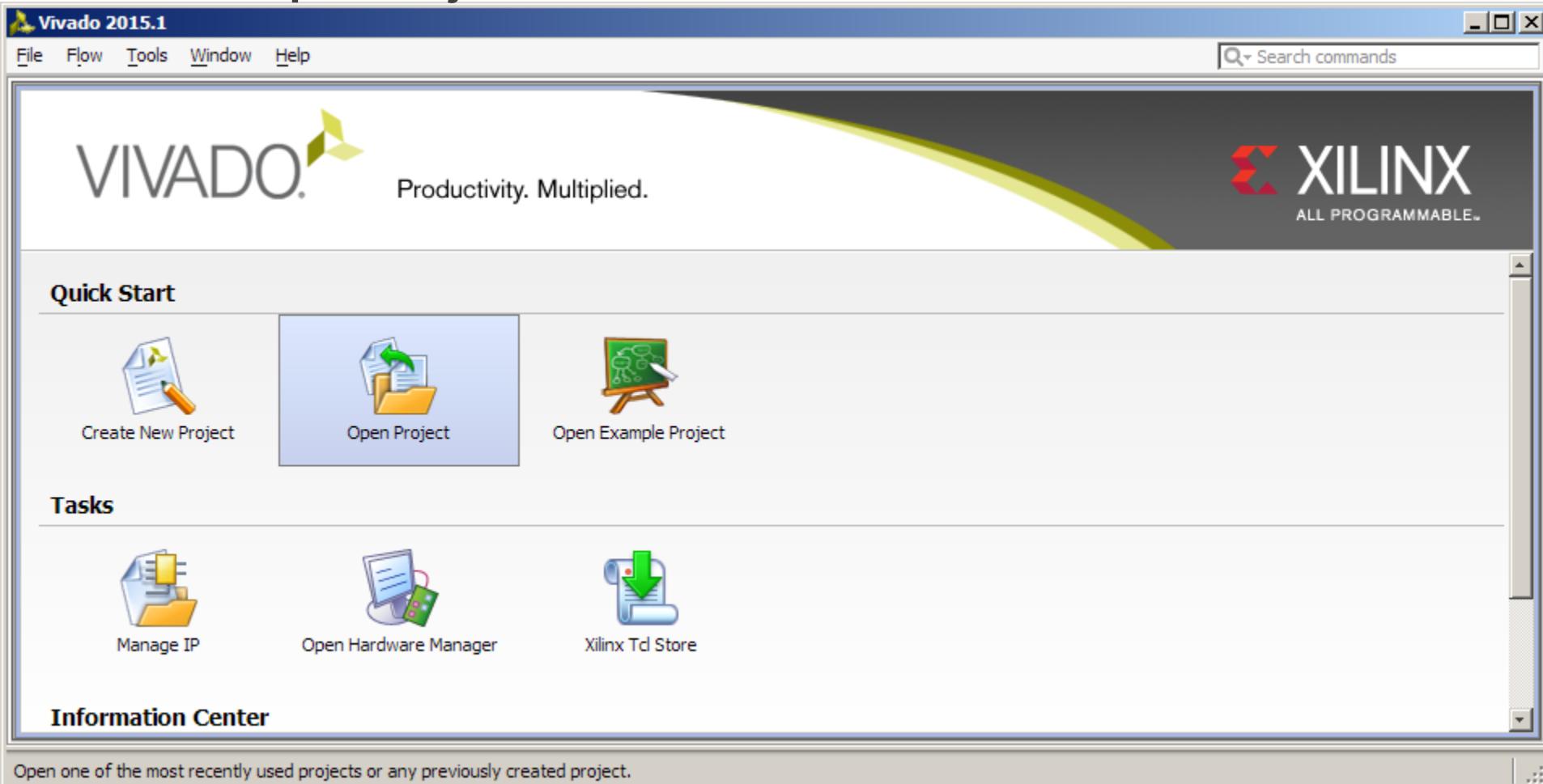
Compile VC707 BIST Design

Compile VC707 BIST Design

► Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2015.1 → Vivado

► Select Open Project



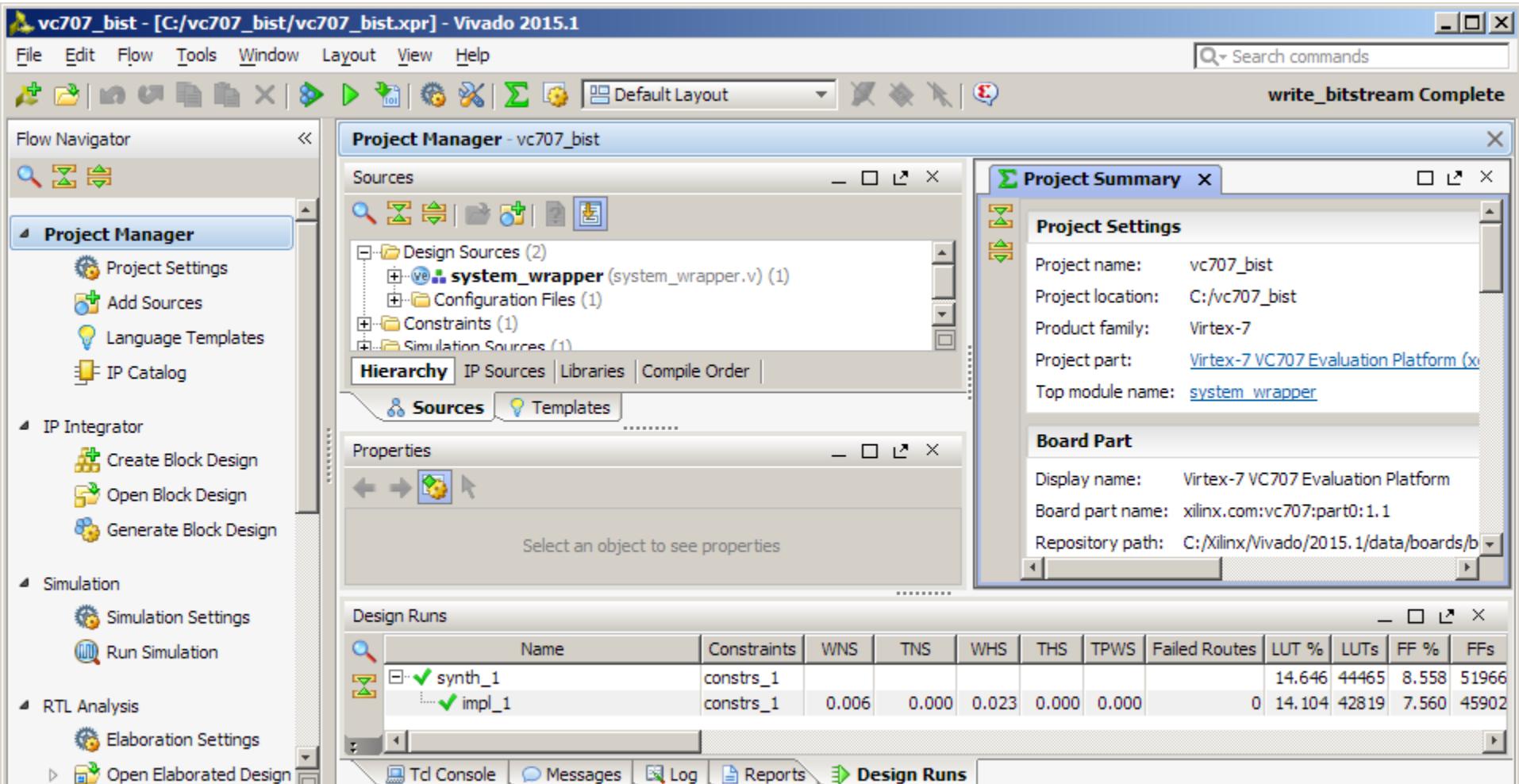
Note: Presentation applies to the VC707

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Compile VC707 BIST Design

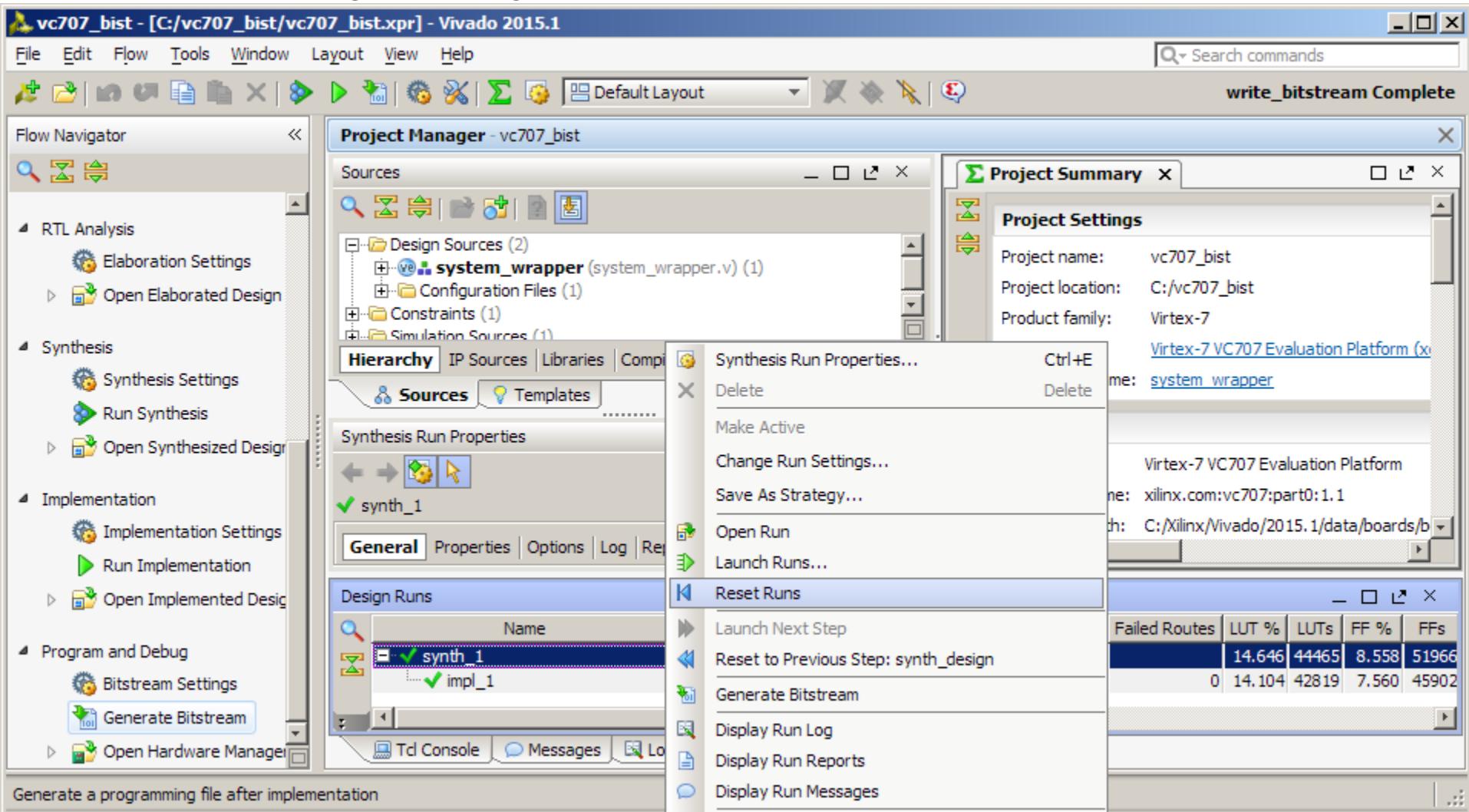
► Open the VC707 Design:

- <Design Name>\vc707_bist\vc707_bist.xpr



Compile VC707 BIST Design

- The design is fully implemented; you can recompile, or export to SDK
 - To recompile, right-click **synth_1**, select **Reset Runs** then **Generate Bitstream**

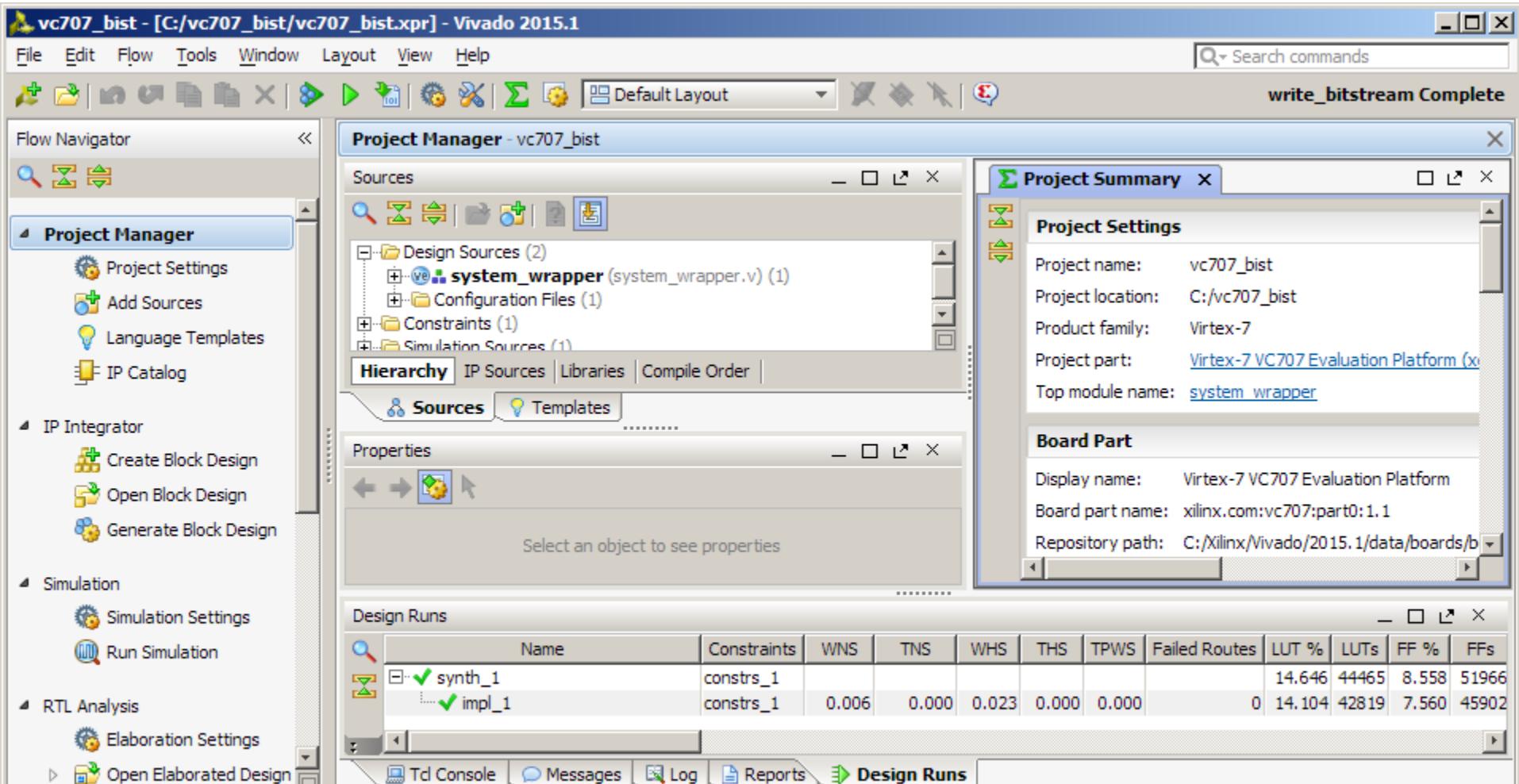


Note: Presentation applies to the VC707

XILINX ➤ ALL PROGRAMMABLE.

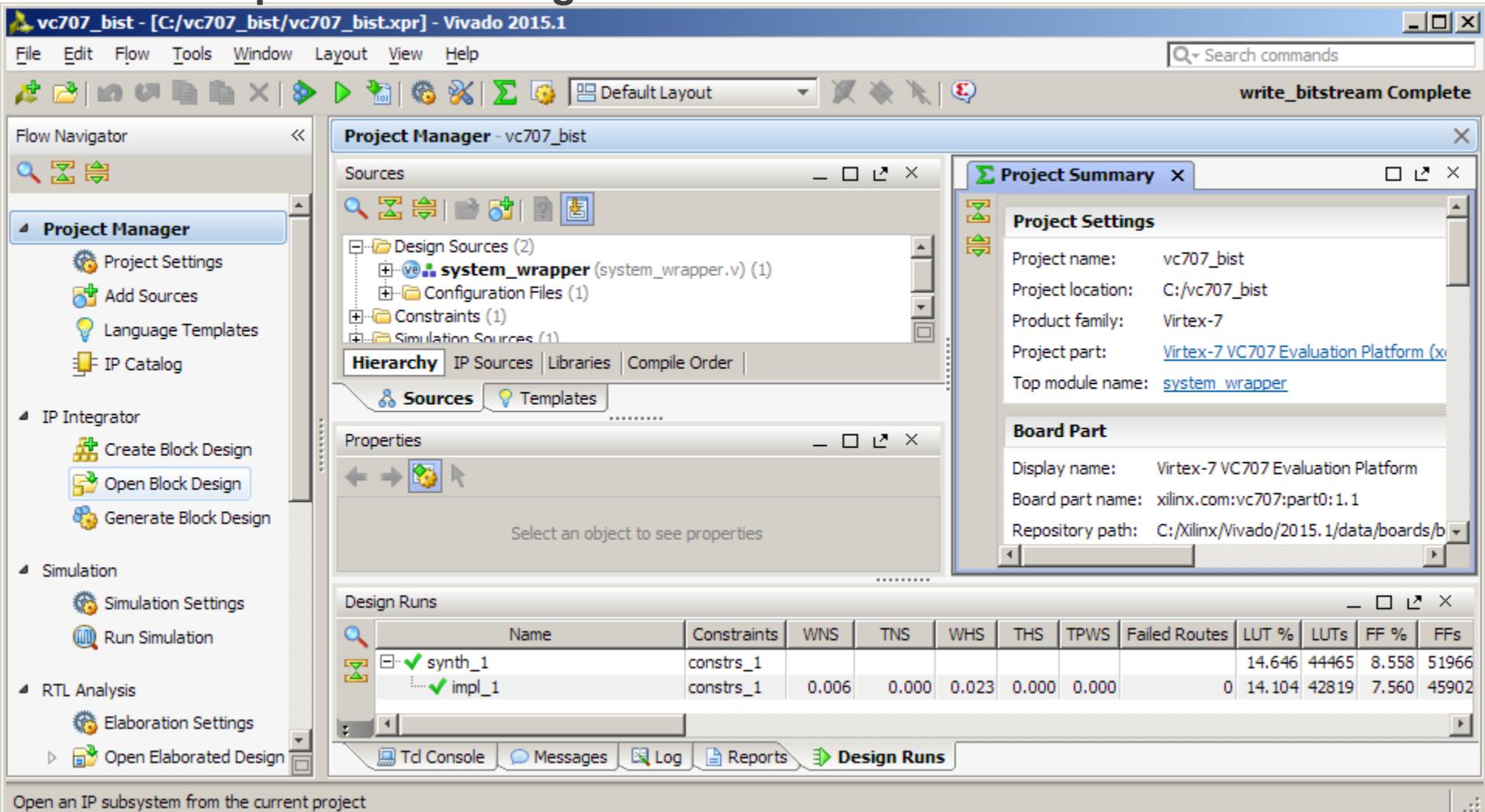
Compile VC707 BIST Design

- Once done, both the Synthesis and Implementation will have green check marks



Compile VC707 BIST Design

- The BIST Design has been implemented with IP Integrator (IPI)
- Click Open Block Design

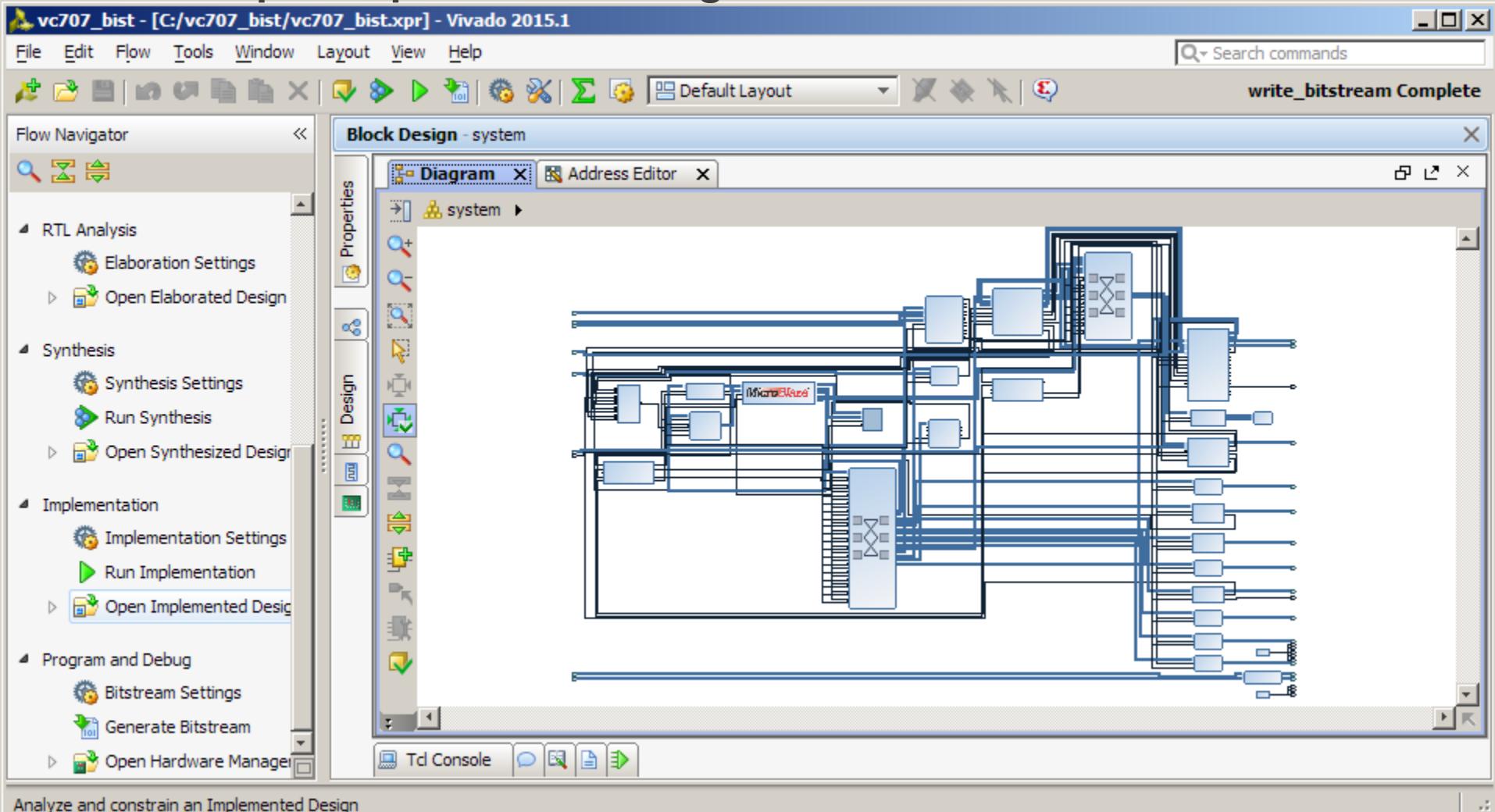


Note: Presentation applies to the VC707

XILINX ➤ ALL PROGRAMMABLE™

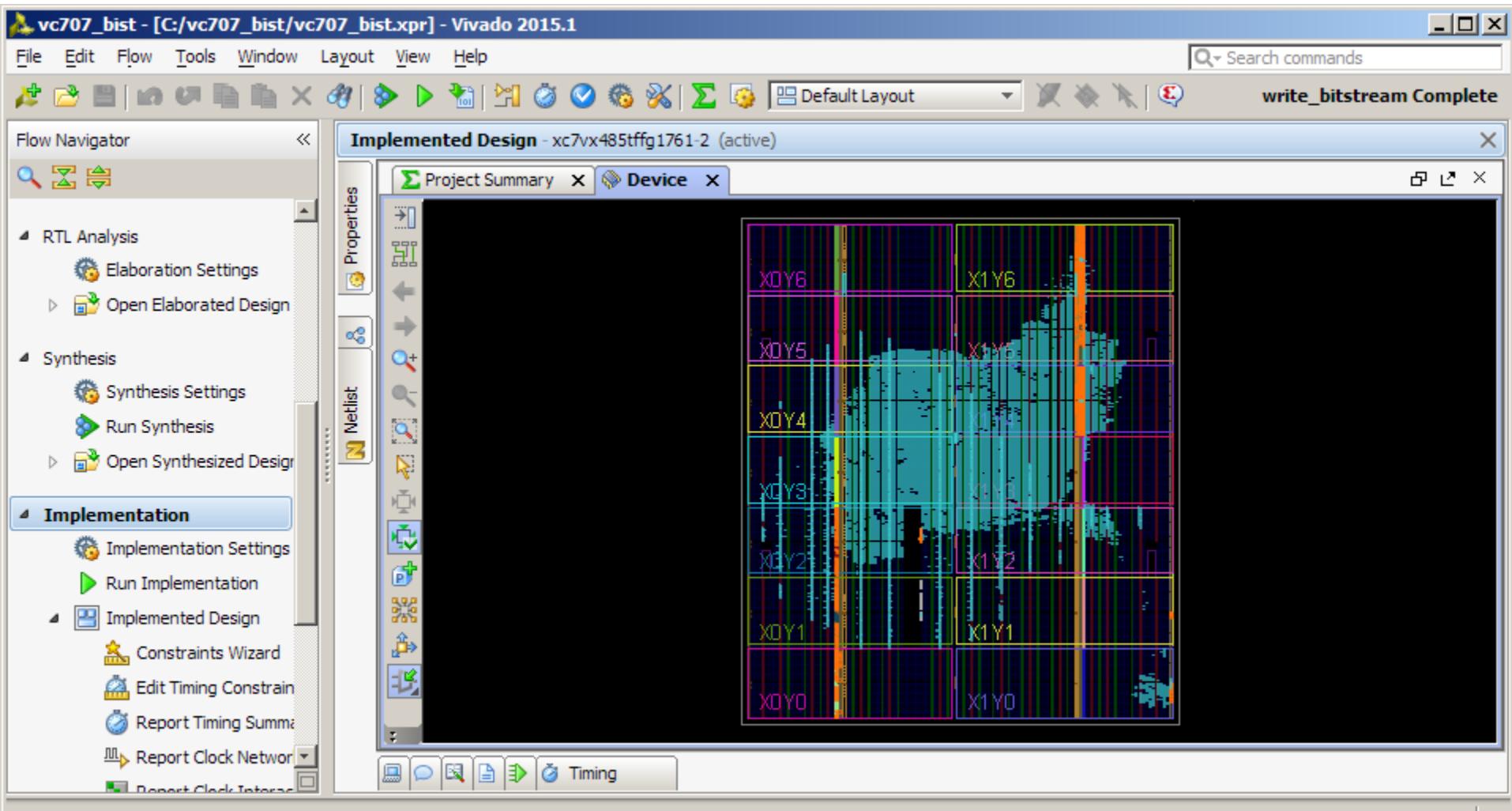
Compile VC707 BIST Design

- All the IP Blocks used in the design can be seen in this view
- Click Open Implemented Design



Compile VC707 BIST Design

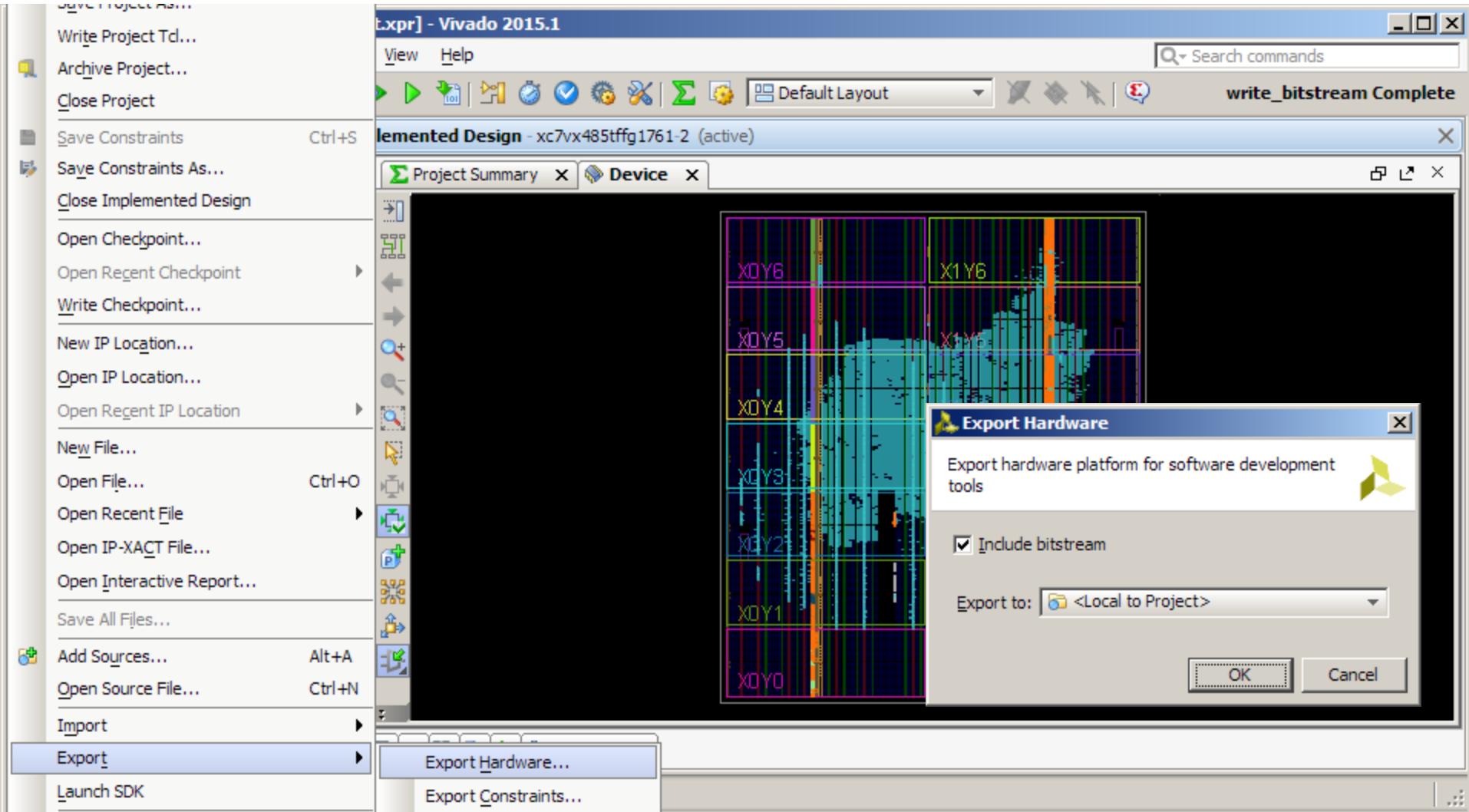
► View Implemented Design



Compile VC707 BIST Design

► Select File → Export → Export Hardware

► Click OK



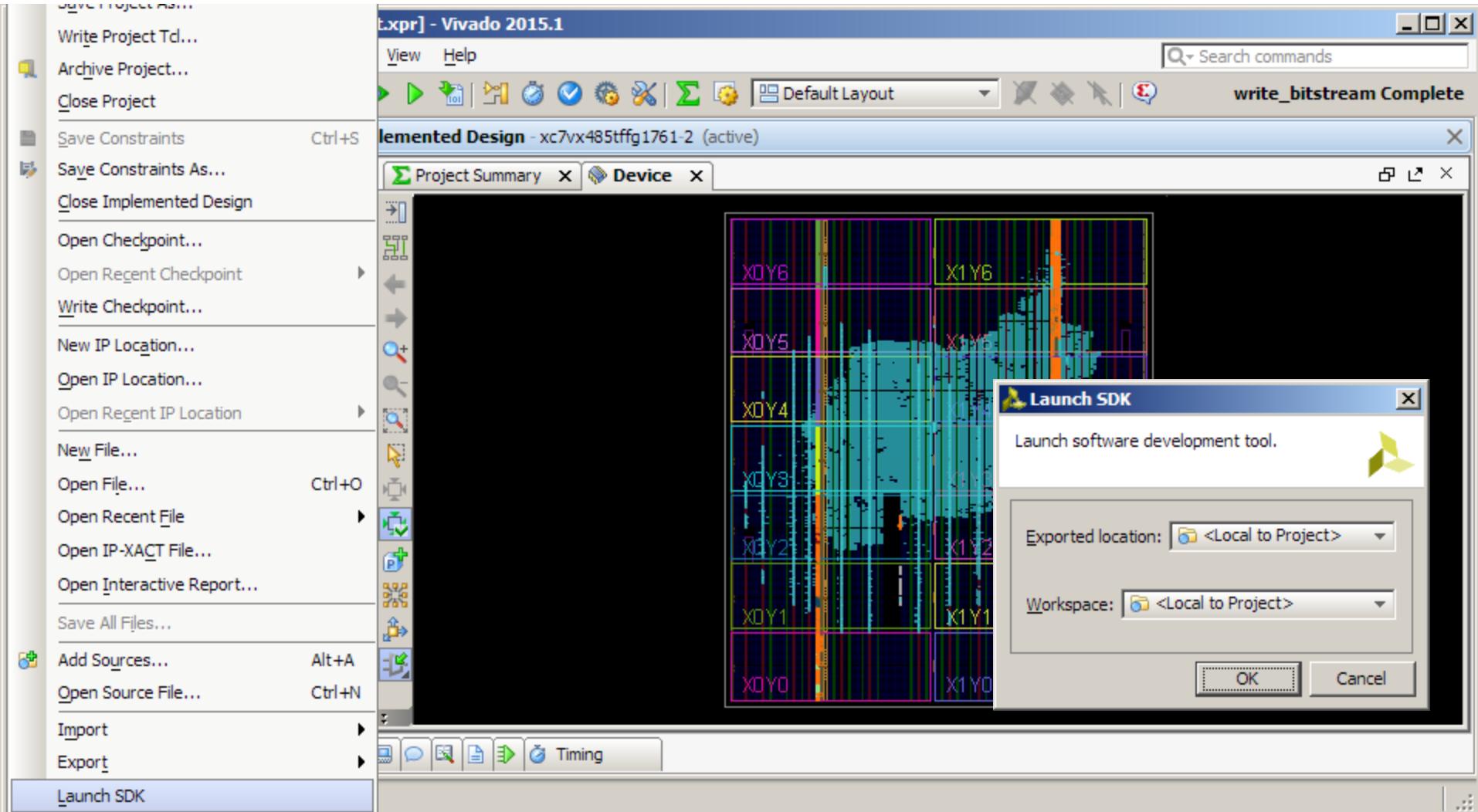
Note: Presentation applies to the VC707

 XILINX ➤ ALL PROGRAMMABLE

Compile VC707 BIST Design

► Select File → Launch SDK

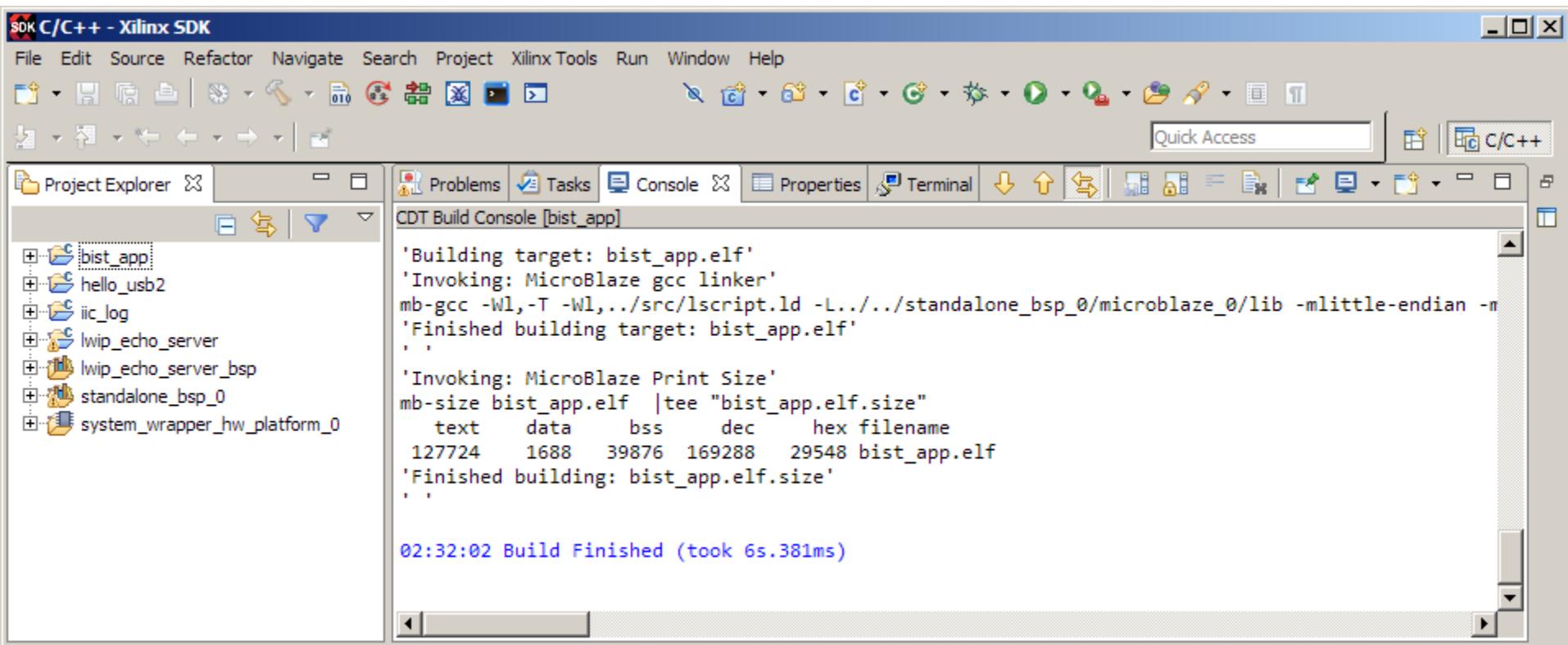
► Click OK



Compile VC707 Software in SDK

➤ SDK Software Compile - Build ELF files in SDK

- Project builds automatically
- When done, close SDK and return to Vivado



The screenshot shows the Xilinx C/C++ - Xilinx SDK interface. The window title is "SDK C/C++ - Xilinx SDK". The menu bar includes File, Edit, Source, Refactor, Navigate, Search, Project, Xilinx Tools, Run, Window, and Help. The toolbar contains various icons for file operations like Open, Save, and Build. The left pane is the "Project Explorer" showing projects: bist_app, hello_usb2, iic_log, lwip_echo_server, lwip_echo_server_bsp, standalone_bsp_0, and system_wrapper_hw_platform_0. The right pane is the "CDT Build Console [bist_app]" which displays the following build log:

```
'Building target: bist_app.elf'
'Invoking: MicroBlaze gcc linker'
mb-gcc -Wl,-T -Wl,../src/lscript.ld -L../../standalone_bsp_0/microblaze_0/lib -mlittle-endian -march=mb
'Finished building target: bist_app.elf'
'

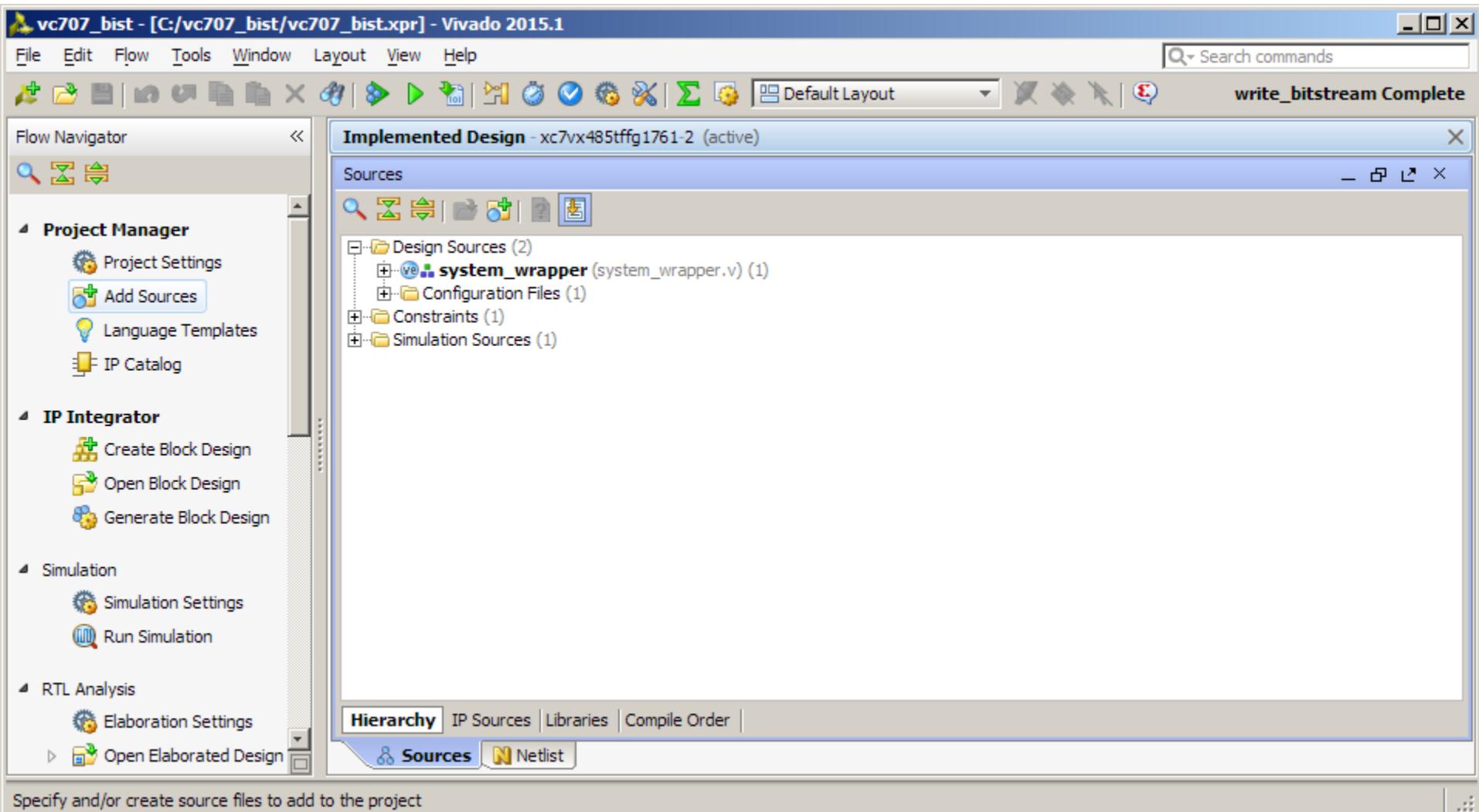
'Invoking: MicroBlaze Print Size'
mb-size bist_app.elf |tee "bist_app.elf.size"
    text      data      bss      dec      hex filename
 127724     1688     39876   169288    29548 bist_app.elf
'Finished building: bist_app.elf.size'
'

02:32:02 Build Finished (took 6s.381ms)
```

Program VC707 with BIST Design

Program VC707 with BIST Design

► Select Add Sources



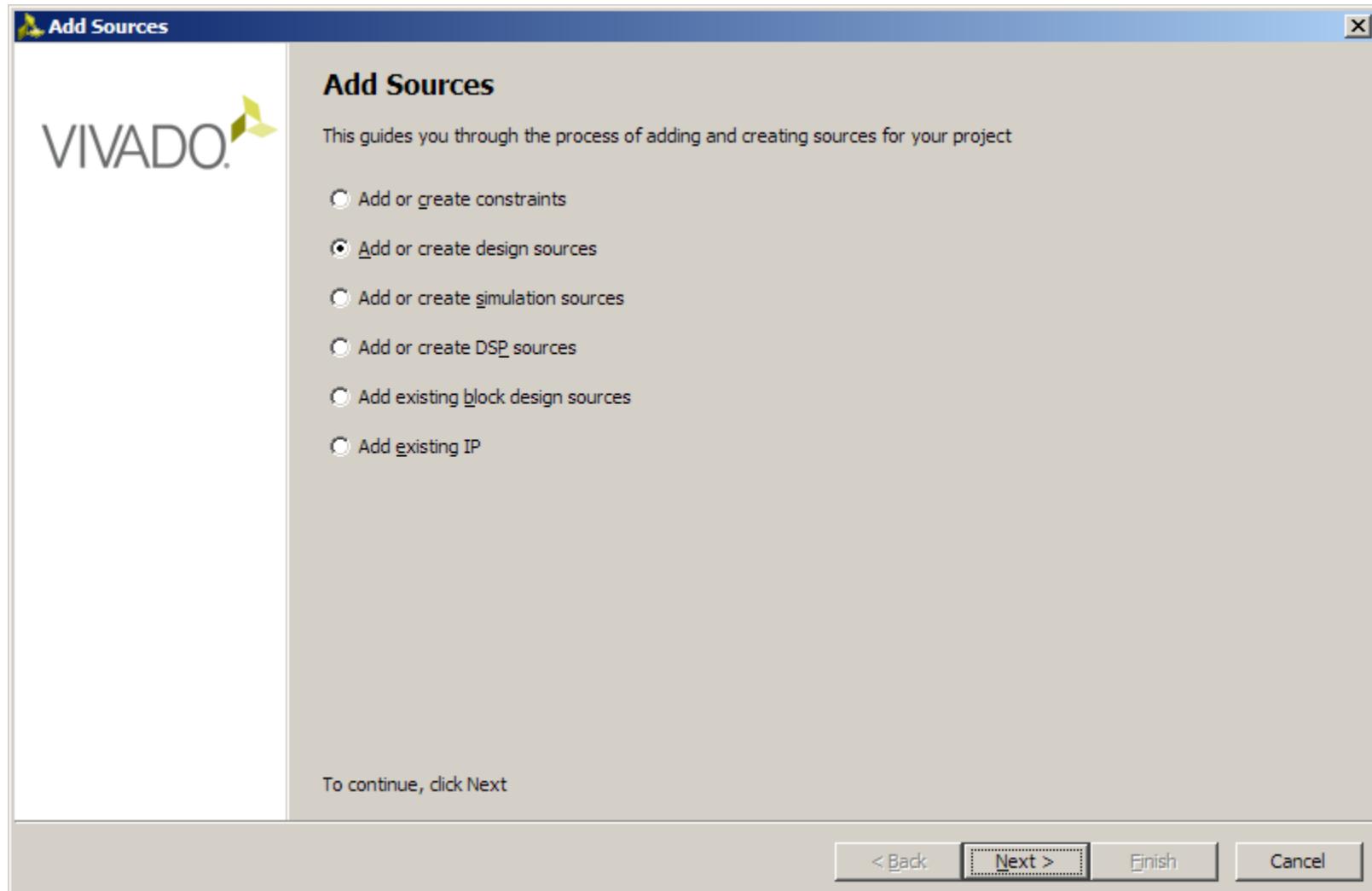
Specify and/or create source files to add to the project

Note: Presentation applies to the VC707

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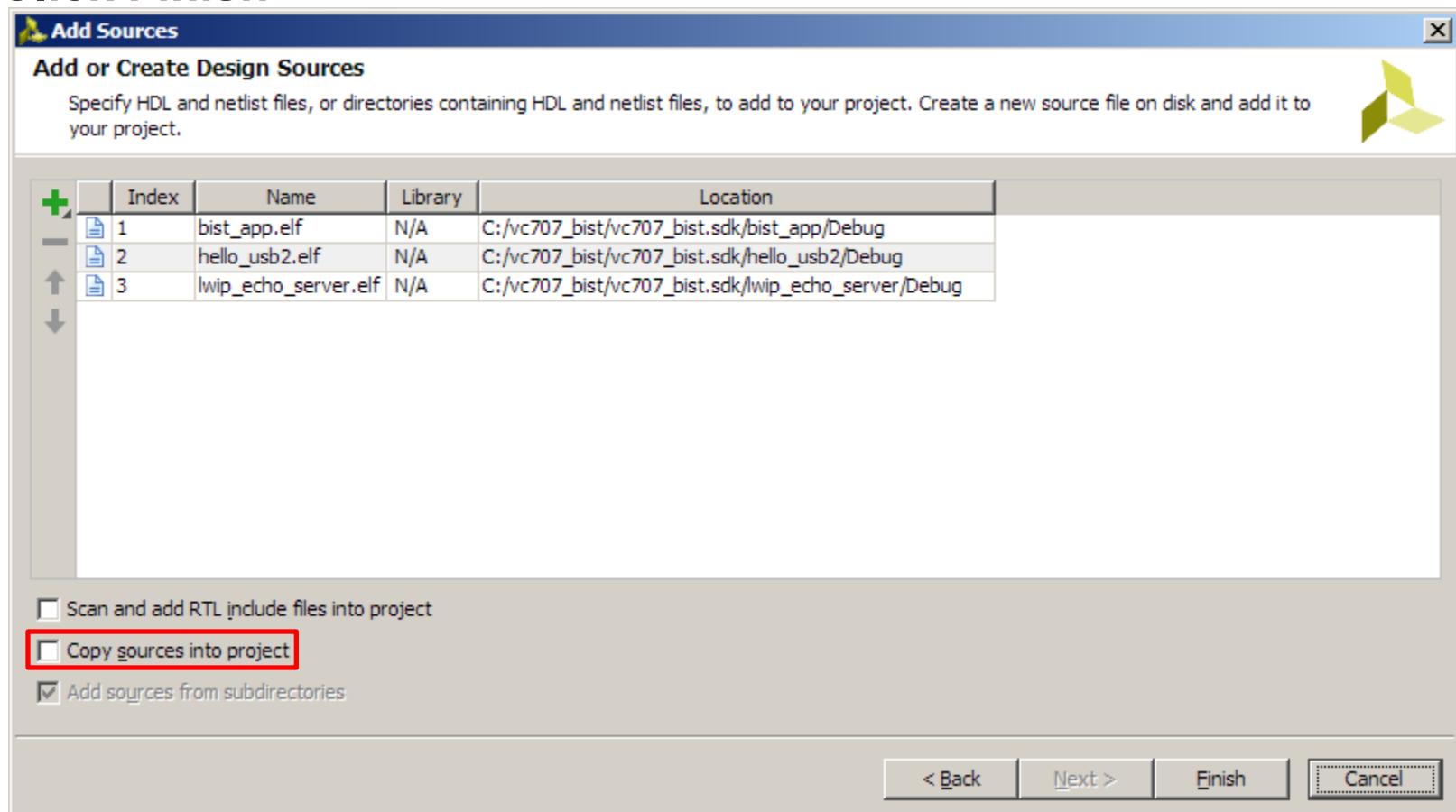
Program VC707 with BIST Design

► Select Add or Create Design Sources



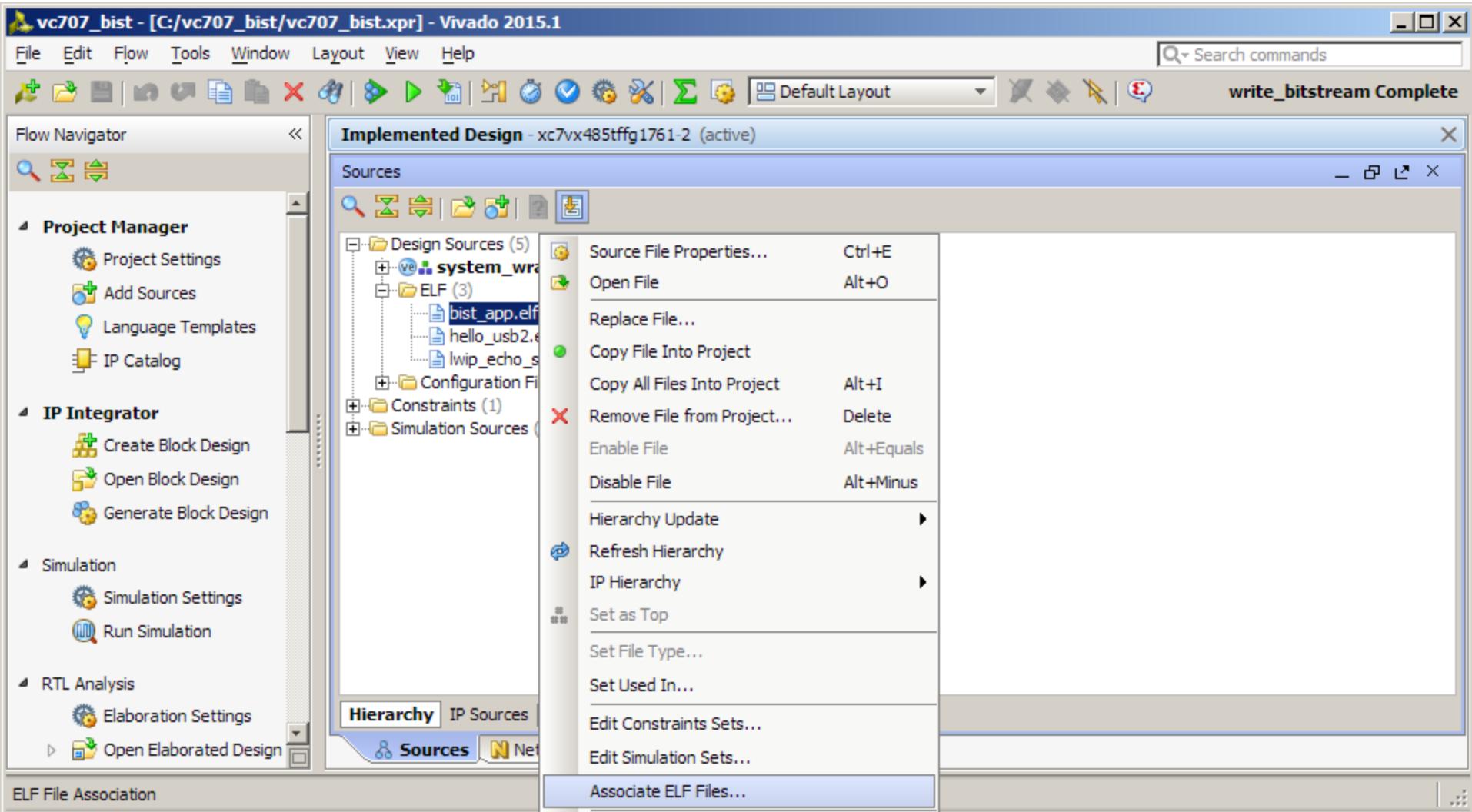
Program VC707 with BIST Design

- Add **bist_app.elf**, **hello_usb2.elf**, and **lwip_echo_server.elf** from the SDK tree
- Make sure **Copy sources into project** is deselected
- Click Finish



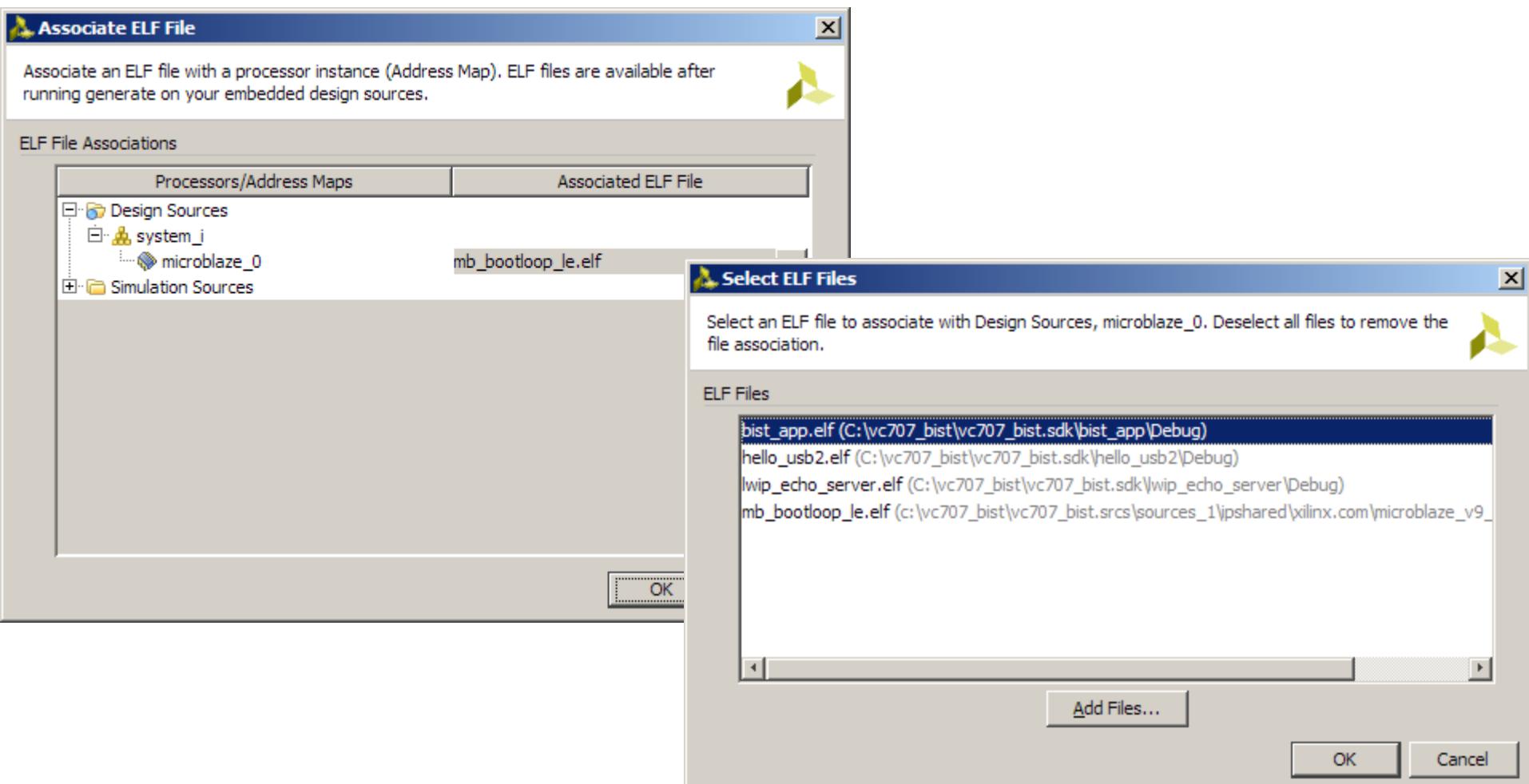
Program VC707 with BIST Design

► Right-click on one of the ELF files and select Associate ELF files



Program VC707 with BIST Design

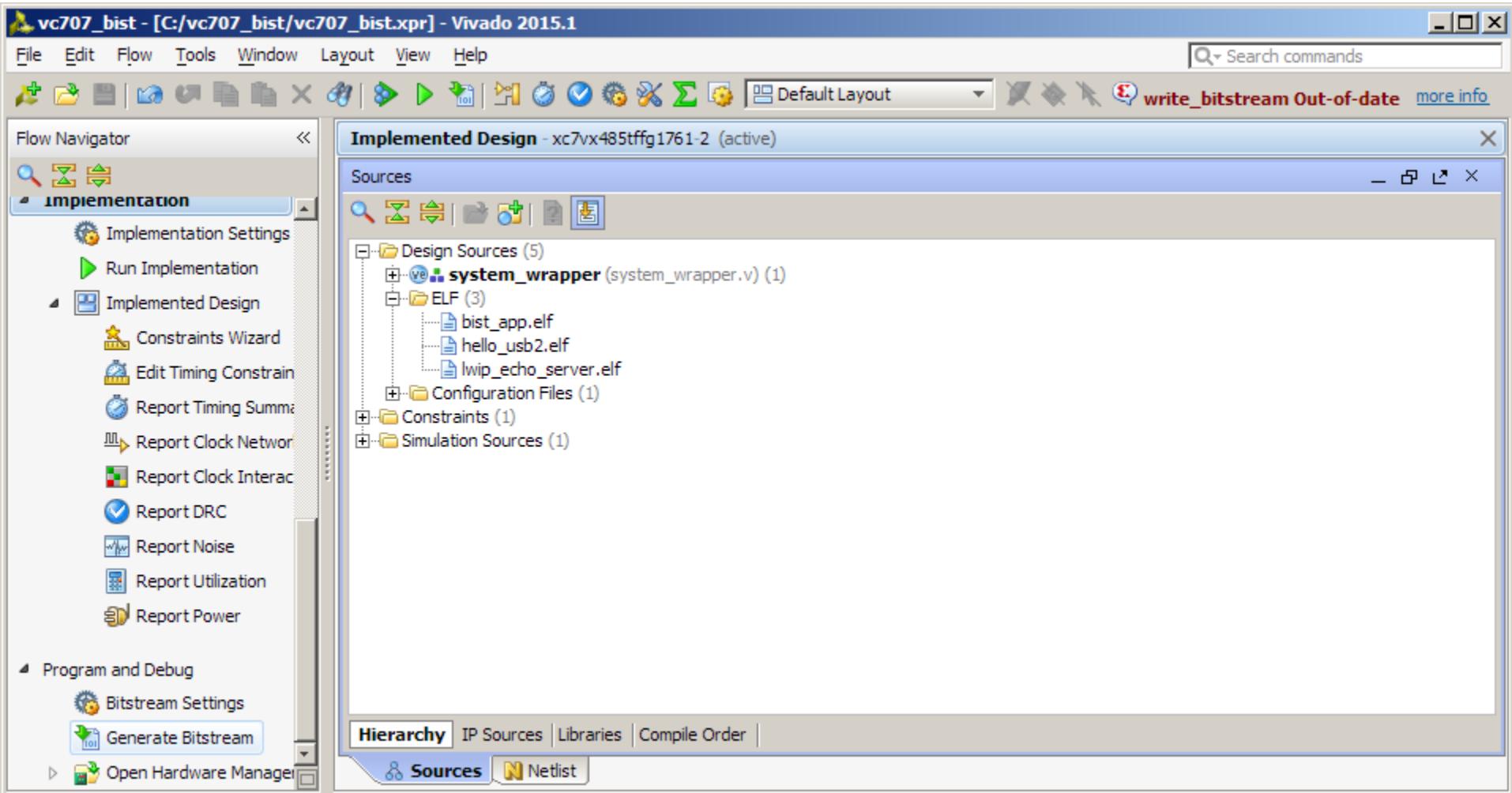
- Click the button to the right; select the `bist_app.elf` then click OK twice



Program VC707 with BIST Design

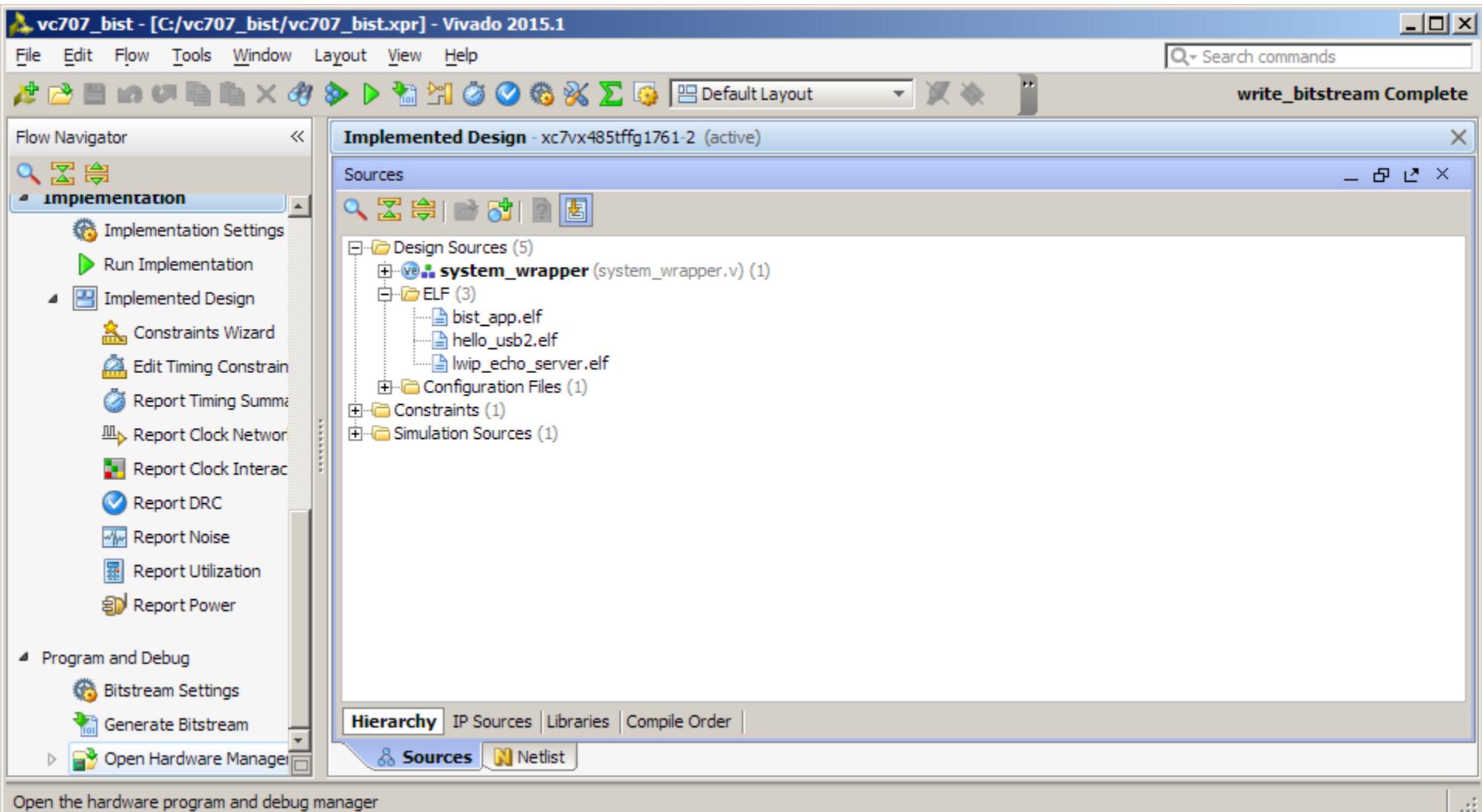
► Select Generate Bitstream

- This creates a bitstream with the BIST ELF file



Program VC707 with BIST Design

► Click Open Hardware Manager



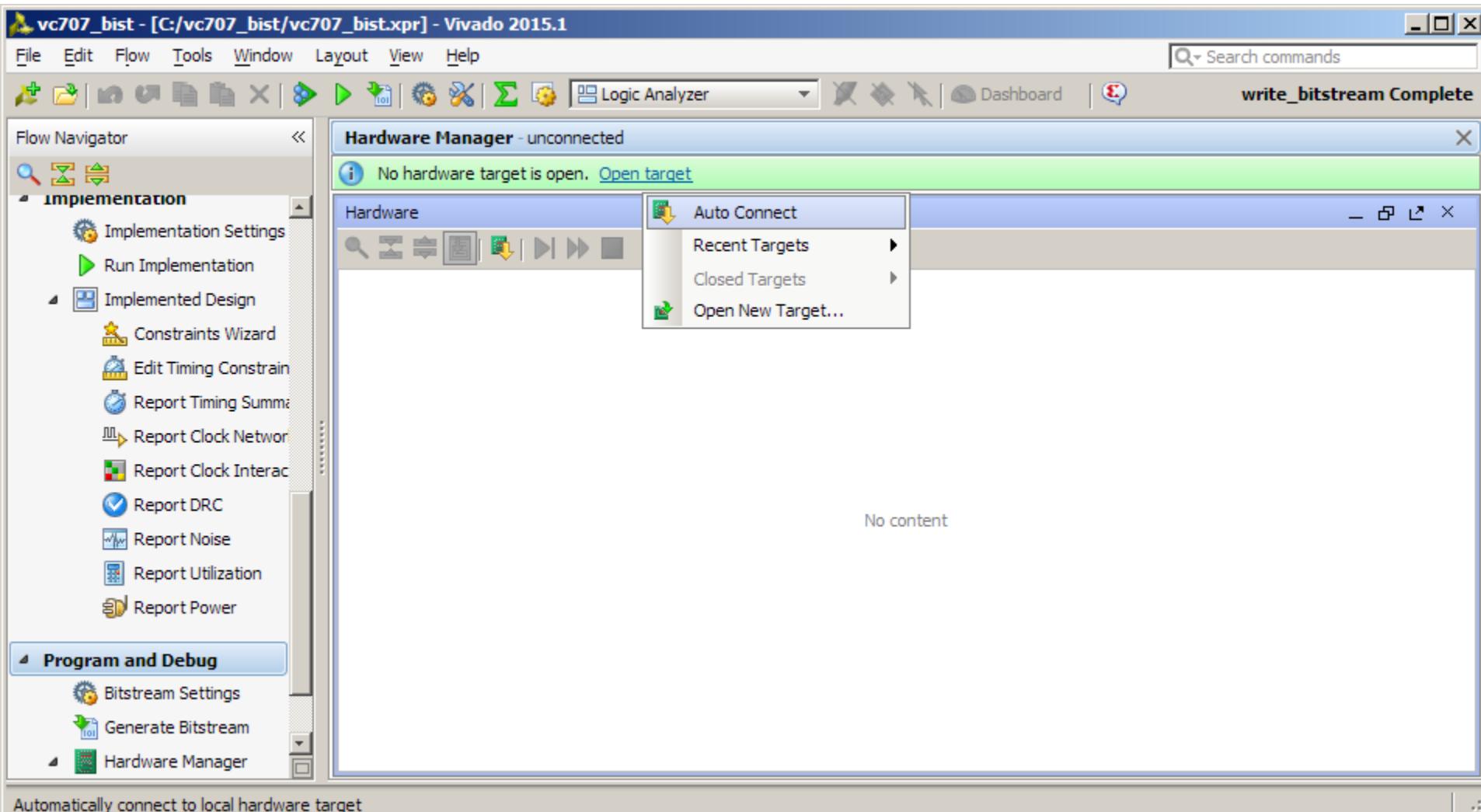
Open the hardware program and debug manager

Note: Presentation applies to the VC707

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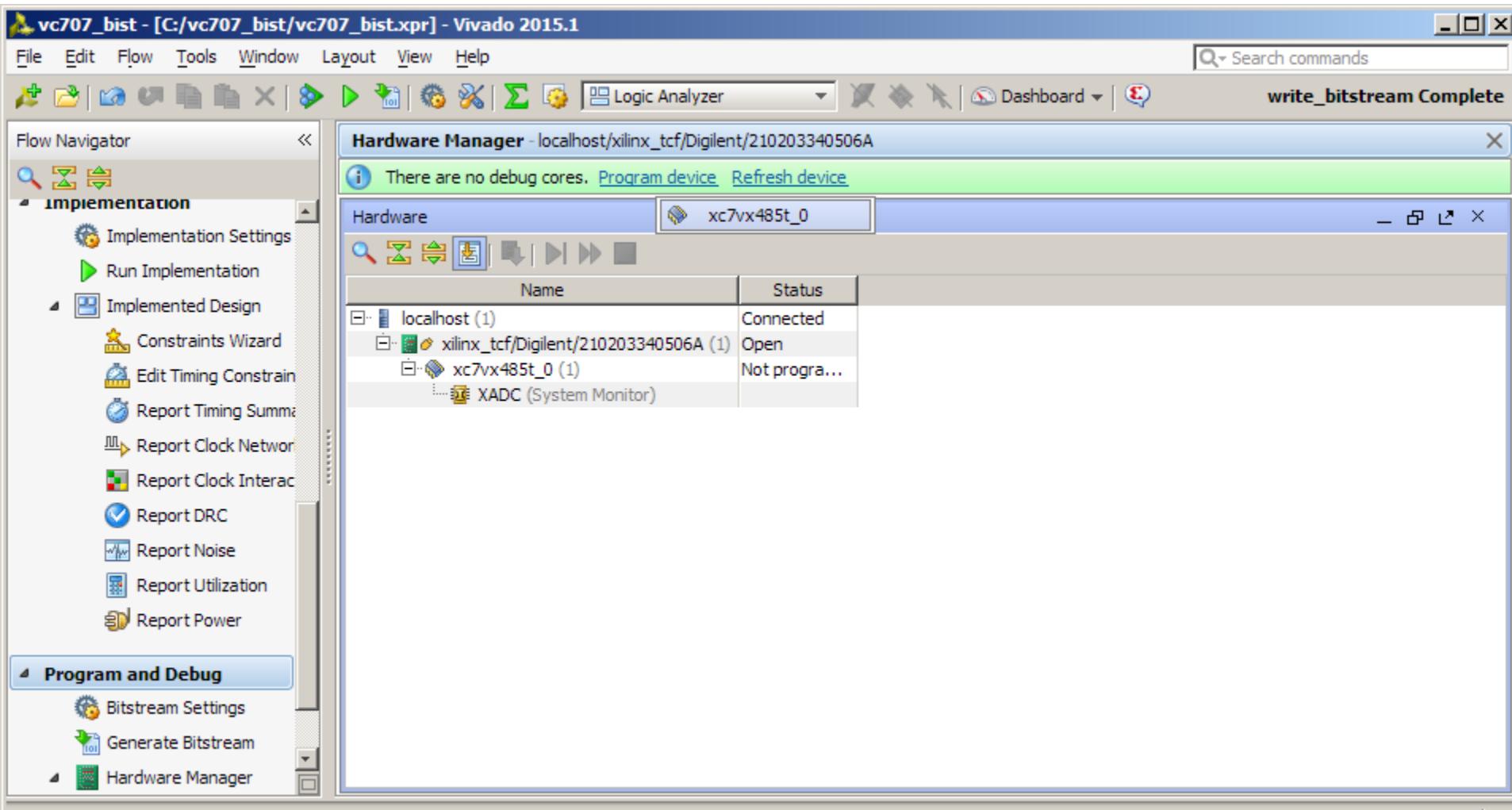
Program VC707 with BIST Design

► Click Open Target and select Auto Connect



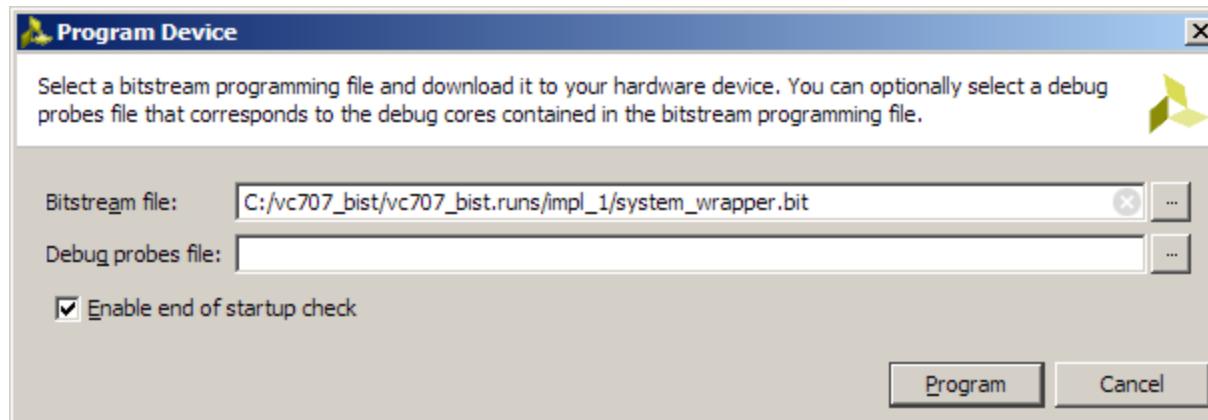
Program VC707 with BIST Design

► Select Program device → xc7vx485t_0



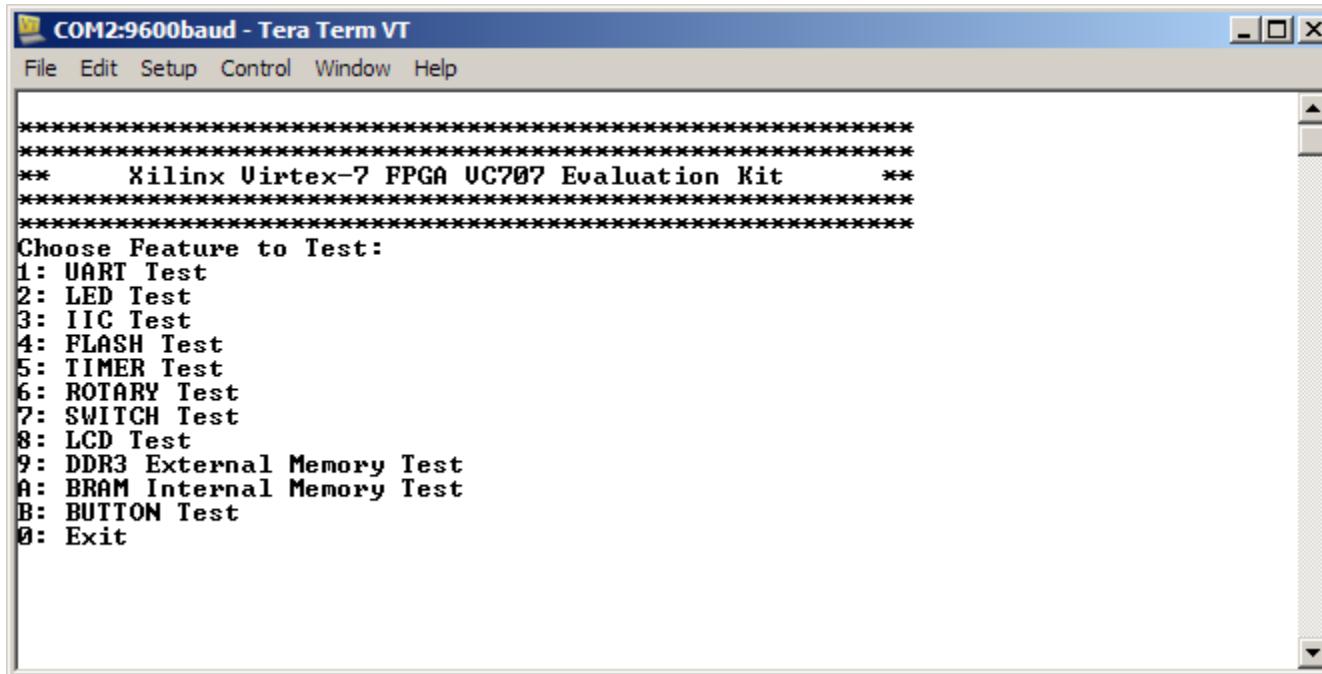
Program VC707 with BIST Design

- The newly created bitstream is default
- Click Program



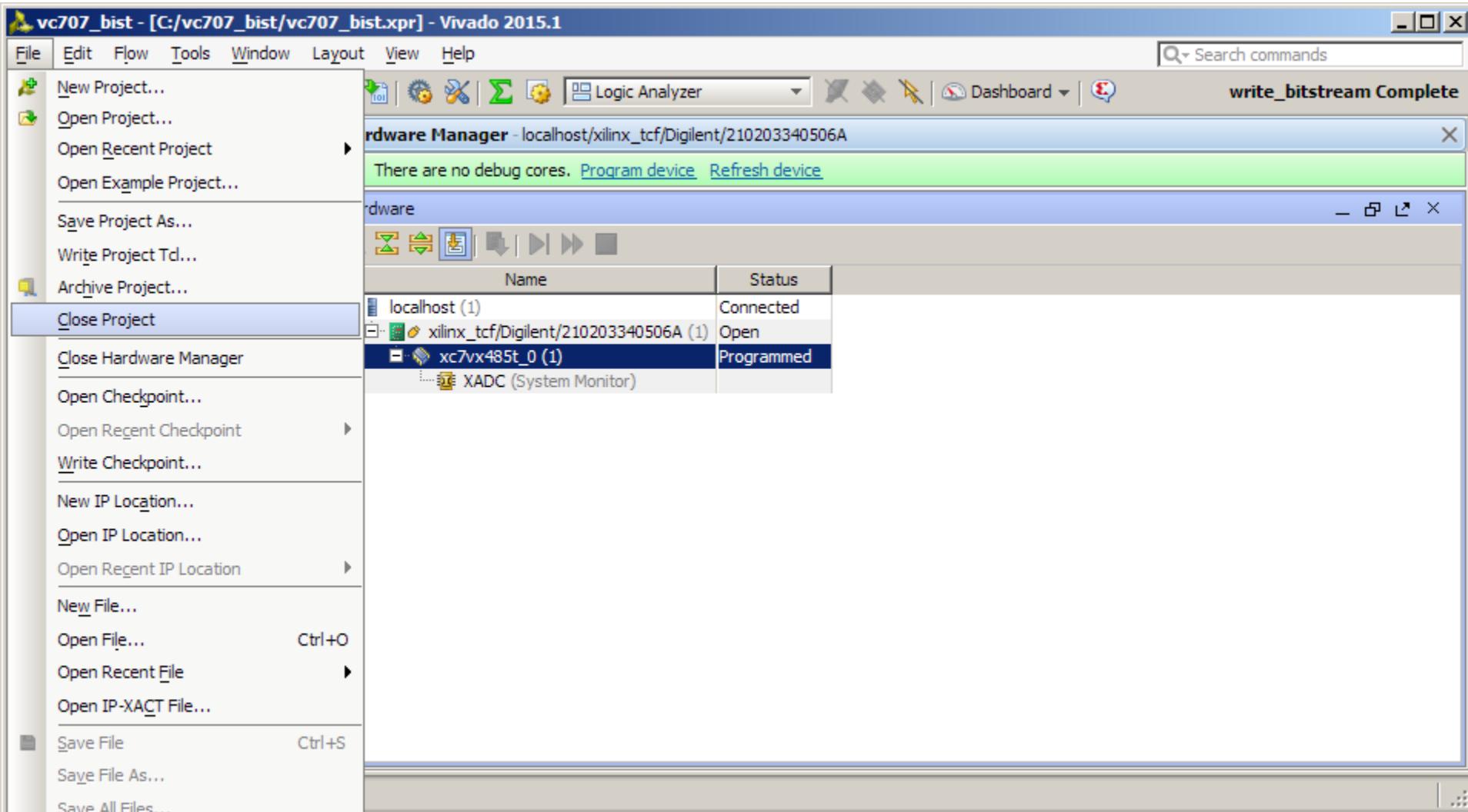
Program VC707 with BIST Design

- BIST Application runs in the terminal window



Program VC707 with BIST Design

► Close the Project



Note: Presentation applies to the VC707

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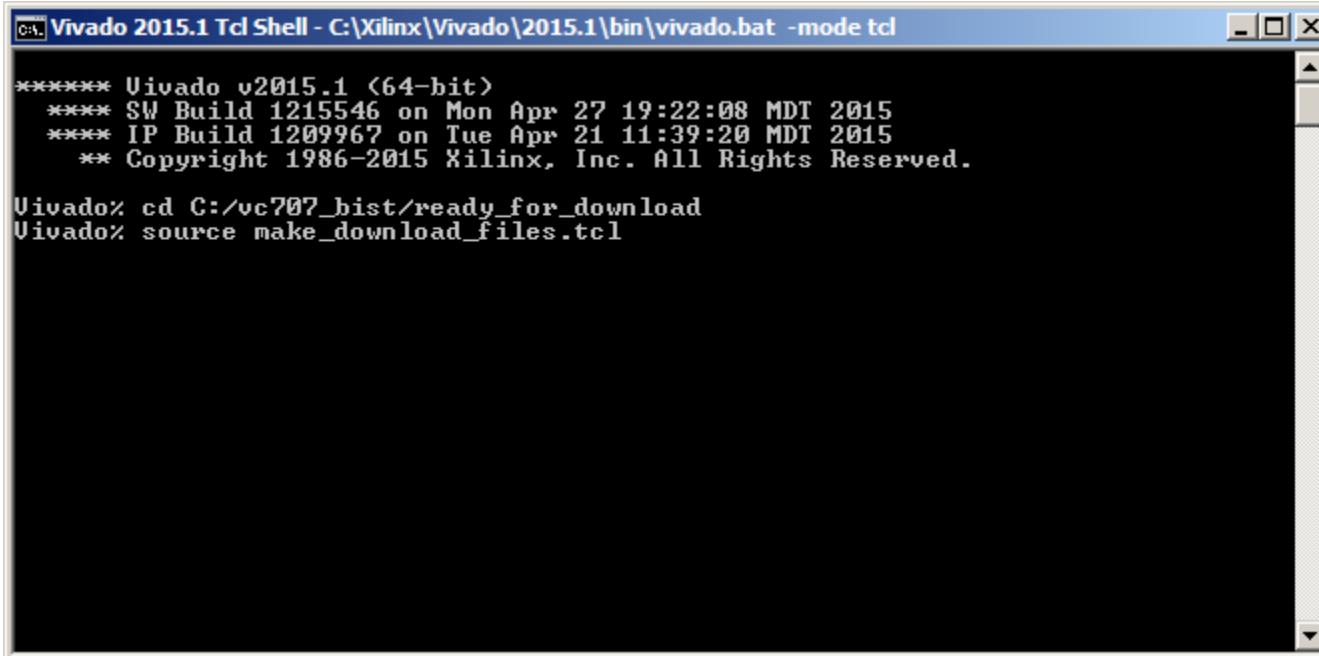
Program VC707 with BIST Design

➤ Repeat this process using Tcl scripts

➤ Open a Vivado Tcl Shell and type:

```
cd C:/vc707_bist/ready_for_download  
source make_download_files.tcl
```

➤ This script uses Tcl commands to add the ELF files to the BIST project , then generate the BIST, USB2, and LwIP bitstreams

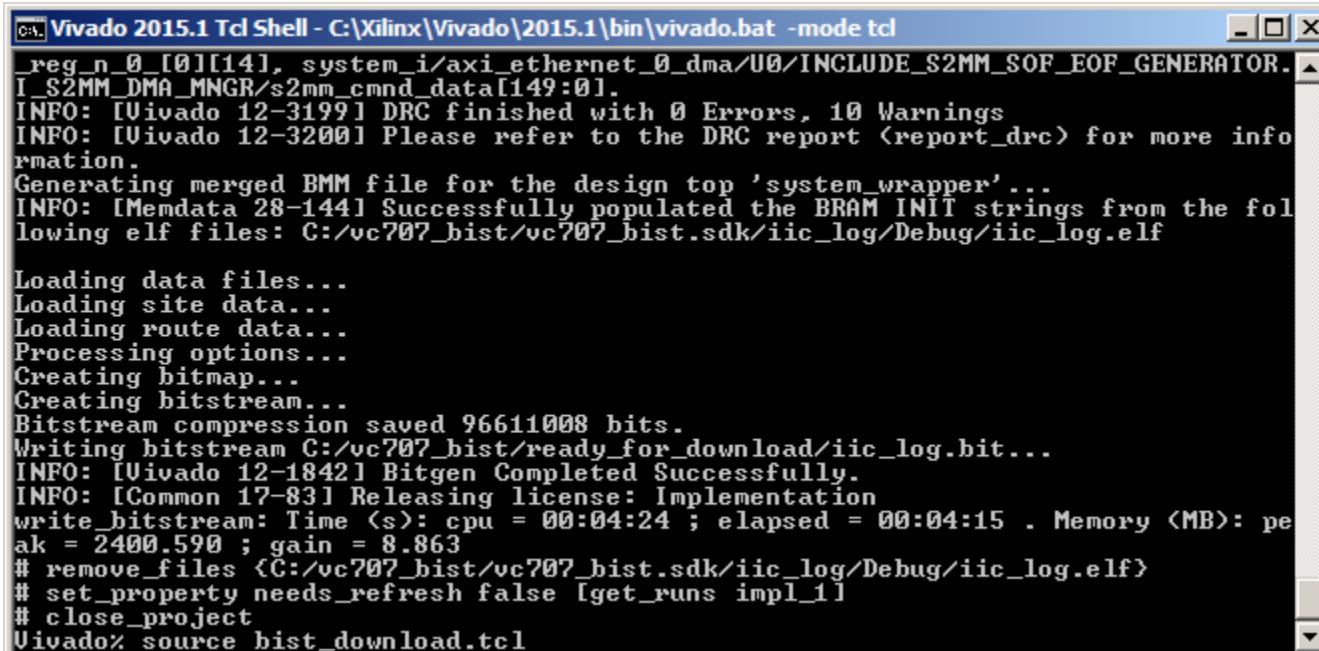


The screenshot shows a Windows command-line interface window titled "Vivado 2015.1 Tcl Shell - C:\Xilinx\Vivado\2015.1\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2015.1 (64-bit)  
**** SW Build 1215546 on Mon Apr 27 19:22:08 MDT 2015  
**** IP Build 1209967 on Tue Apr 21 11:39:20 MDT 2015  
** Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/vc707_bist/ready_for_download  
Vivado> source make_download_files.tcl
```

Program VC707 with BIST Design

- Download the BIST bitstream
- In the Vivado Tcl Shell type:
`source bist_download.tcl`

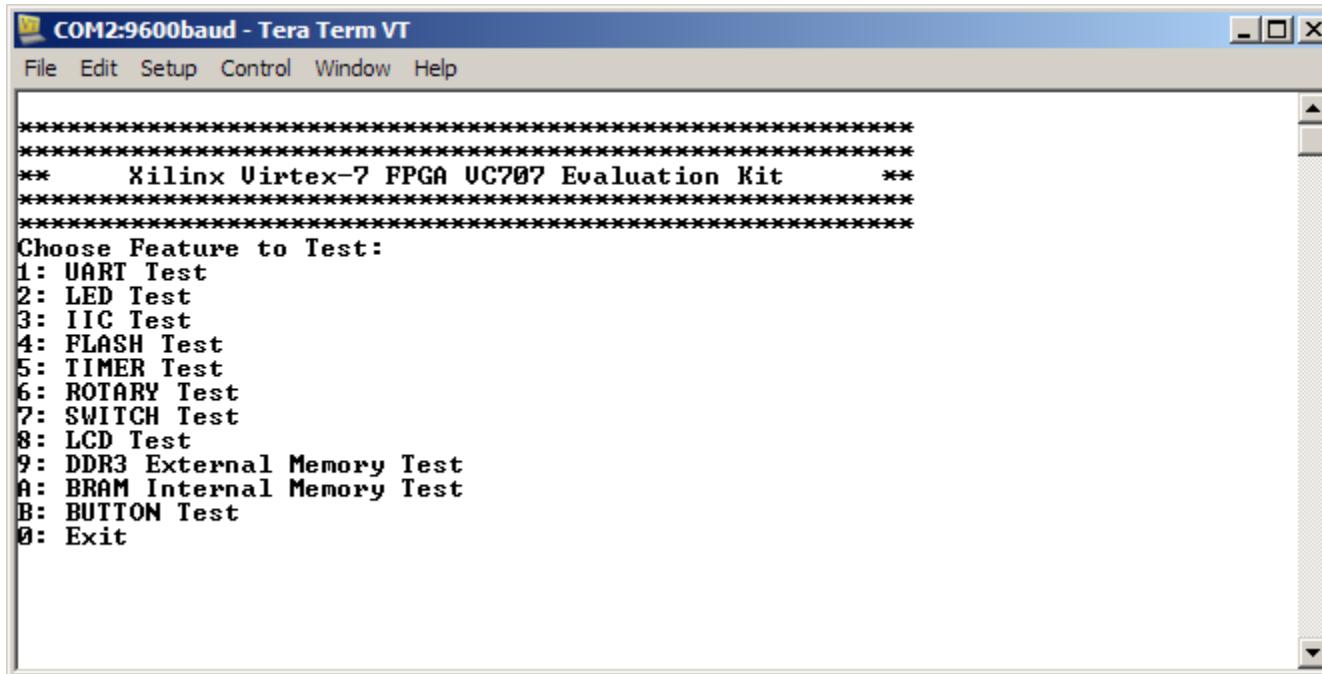


```
cd Vivado 2015.1 Tcl Shell - C:\Xilinx\Vivado\2015.1\bin\vivado.bat -mode tcl
source bist_download.tcl
INFO: [Drc 12-3199] DRC finished with 0 Errors, 10 Warnings
INFO: [Drc 12-3200] Please refer to the DRC report <report_drc> for more information.
Generating merged BMM file for the design top 'system_wrapper'...
INFO: [Memdata 28-144] Successfully populated the BRAM INIT strings from the following elf files: C:/vc707_bist/vc707_bist.sdk/iic_log/Debug/iic_log.elf

Loading data files...
Loading site data...
Loading route data...
Processing options...
Creating bitmap...
Creating bitstream...
Bitstream compression saved 96611008 bits.
Writing bitstream C:/vc707_bist/ready_for_download/iic_log.bit...
INFO: [Vivado 12-1842] Bitgen Completed Successfully.
INFO: [Common 17-83] Releasing license: Implementation
write_bitstream: Time <s>: cpu = 00:04:24 ; elapsed = 00:04:15 . Memory <MB>: peak = 2400.590 ; gain = 8.863
# remove_files {C:/vc707_bist/vc707_bist.sdk/iic_log/Debug/iic_log.elf}
# set_property needs_refresh false [get_runs impl_1]
# close_project
Vivado> source bist_download.tcl
```

Program VC707 with BIST Design

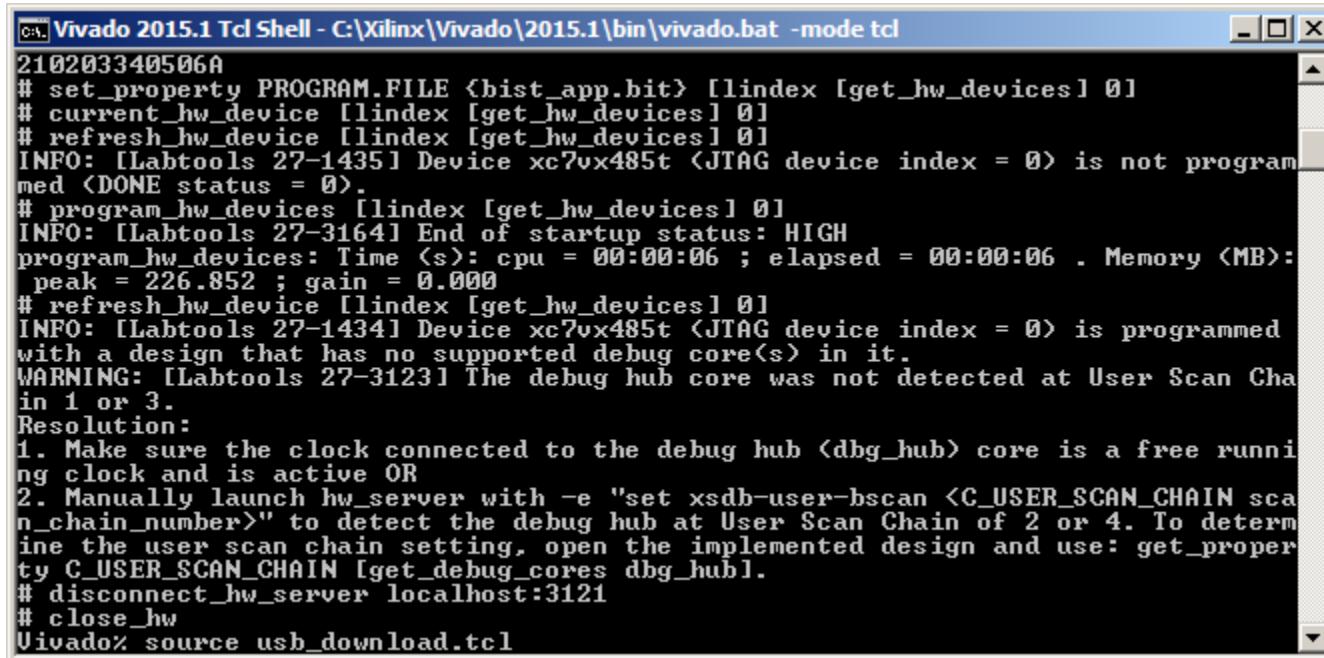
- BIST Application runs in the terminal window



Run the USB2 Design

Run the USB2 Design

- Download the USB2 bitstream
- In the Vivado Tcl Shell type:
source usb_download.tcl

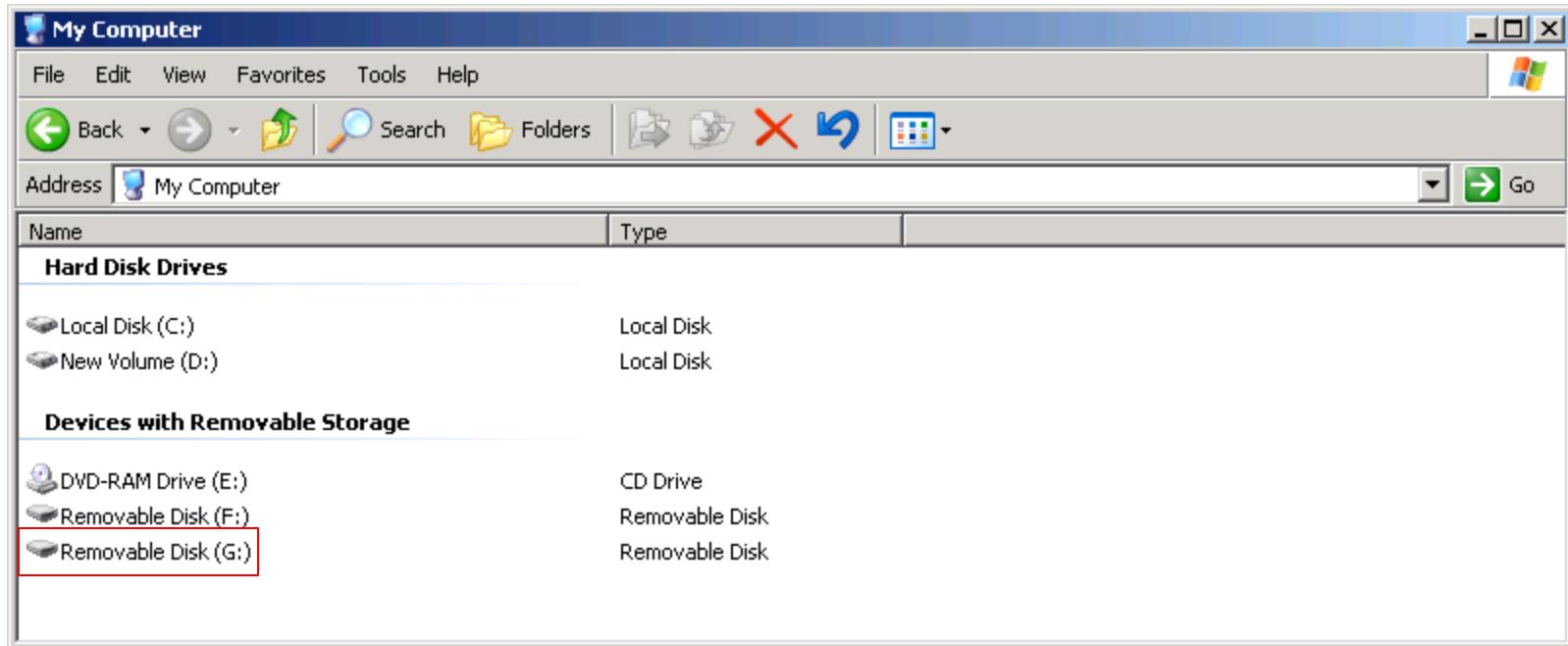


```
04 Vivado 2015.1 Tcl Shell - C:\Xilinx\Vivado\2015.1\bin\vivado.bat -mode tcl
210203340506A
# set_property PROGRAM.FILE {bist_app.bit} [lindex [get_hw_devices] 0]
# current_hw_device [lindex [get_hw_devices] 0]
# refresh_hw_device [lindex [get_hw_devices] 0]
INFO: [Labtools 27-1435] Device xc7vx485t (JTAG device index = 0) is not programmed (DONE status = 0).
# program_hw_devices [lindex [get_hw_devices] 0]
INFO: [Labtools 27-3164] End of startup status: HIGH
program_hw_devices: Time <s>: cpu = 00:00:06 ; elapsed = 00:00:06 . Memory <MB>:
peak = 226.852 ; gain = 0.000
# refresh_hw_device [lindex [get_hw_devices] 0]
INFO: [Labtools 27-1434] Device xc7vx485t (JTAG device index = 0) is programmed with a design that has no supported debug core(s) in it.
WARNING: [Labtools 27-3123] The debug hub core was not detected at User Scan Chain 1 or 3.
Resolution:
1. Make sure the clock connected to the debug hub (dbg_hub) core is a free running clock and is active OR
2. Manually launch hw_server with -e "set xsdb-user-bscan <C_USER_SCAN_CHAIN scan_chain_number>" to detect the debug hub at User Scan Chain of 2 or 4. To determine the user scan chain setting, open the implemented design and use: get_property C_USER_SCAN_CHAIN [get_debug_cores dbg_hub].
# disconnect_hw_server localhost:3121
# close_hw
Vivado> source usb_download.tcl
```

Run the USB2 Design

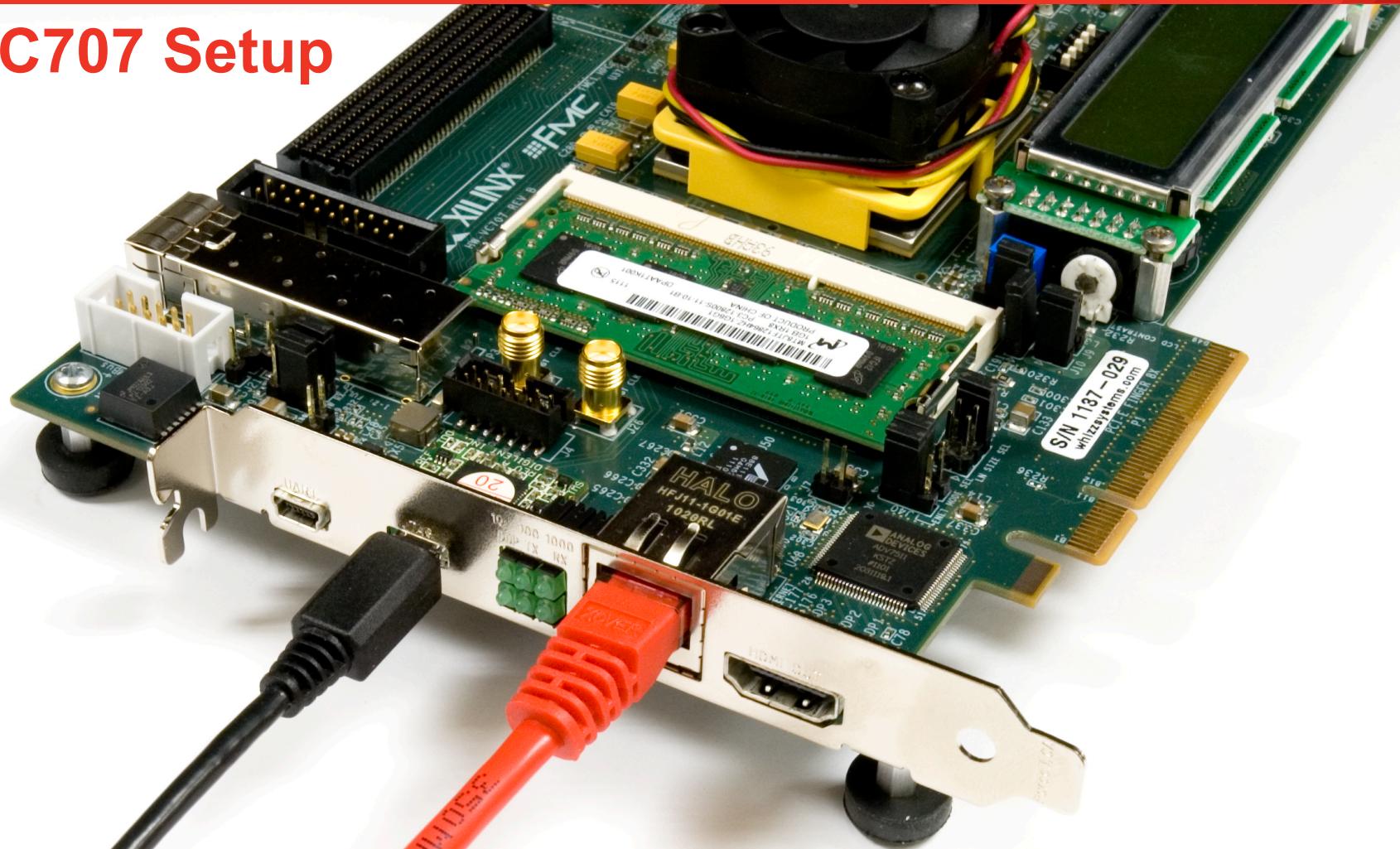
► An extra removable drive will appear

- In this case, “G:”
- As mentioned before, be careful in formatting any drive



Run the LwIP Ethernet Design

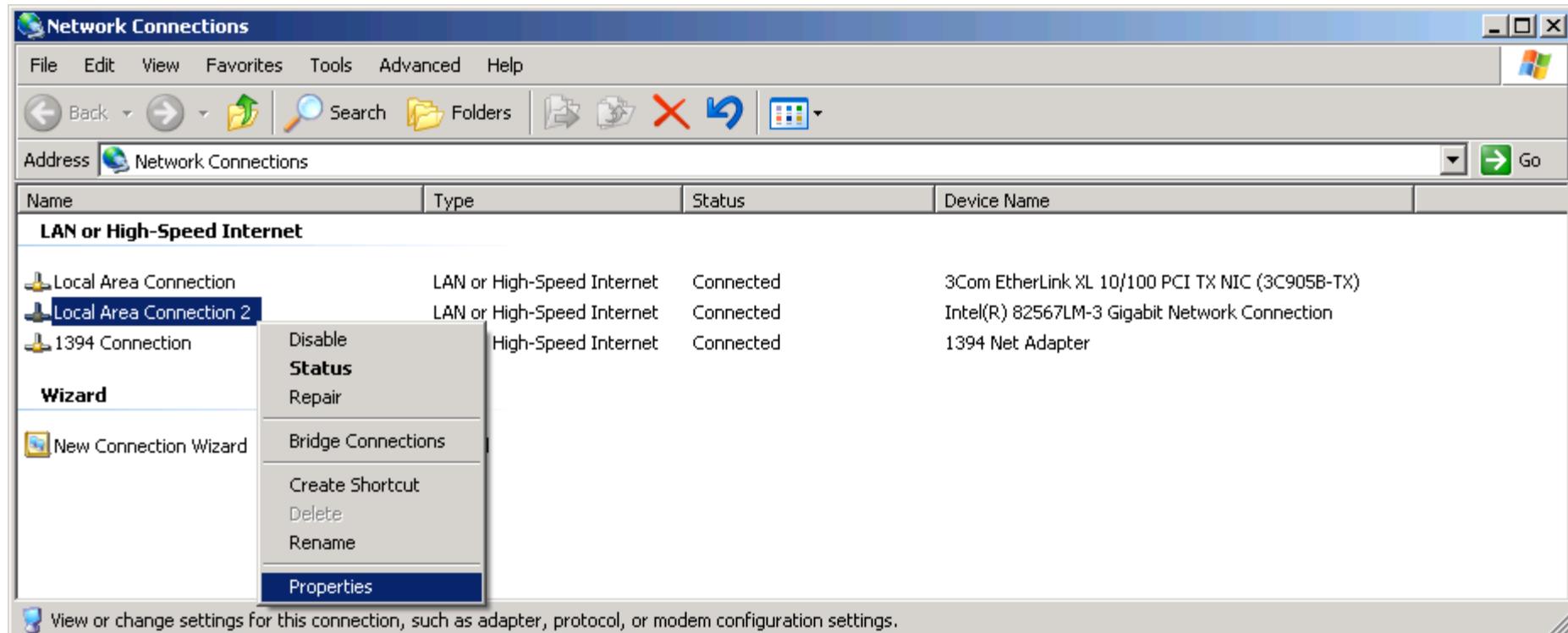
VC707 Setup



- **Connect a Ethernet cable to the VC707**
- Connect this cable to your PC
 - Power on the VC707 board

Run the LwIP Ethernet Design

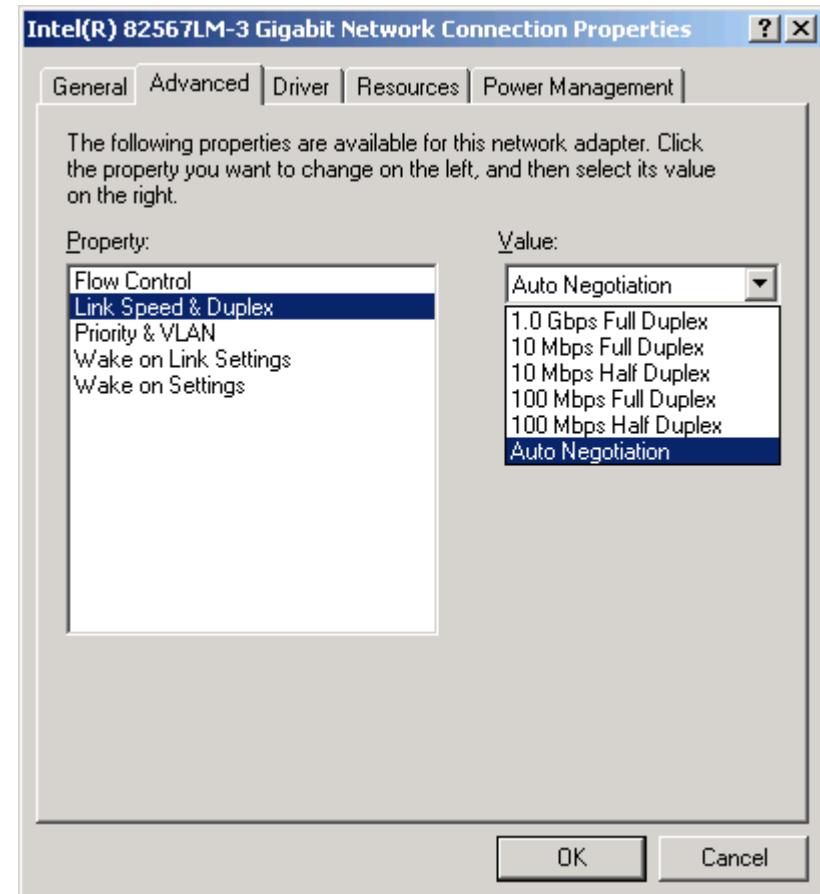
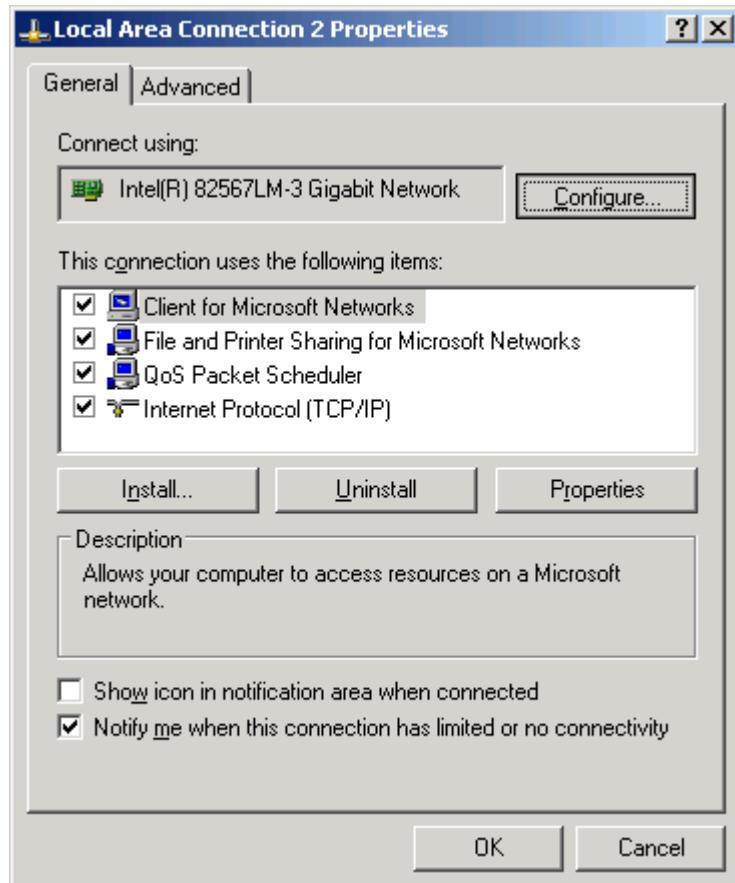
- From the Windows Control Panel, open Network Connections
- Right-click on the Gigabit Ethernet Adapter and select Properties



Run the LwIP Ethernet Design

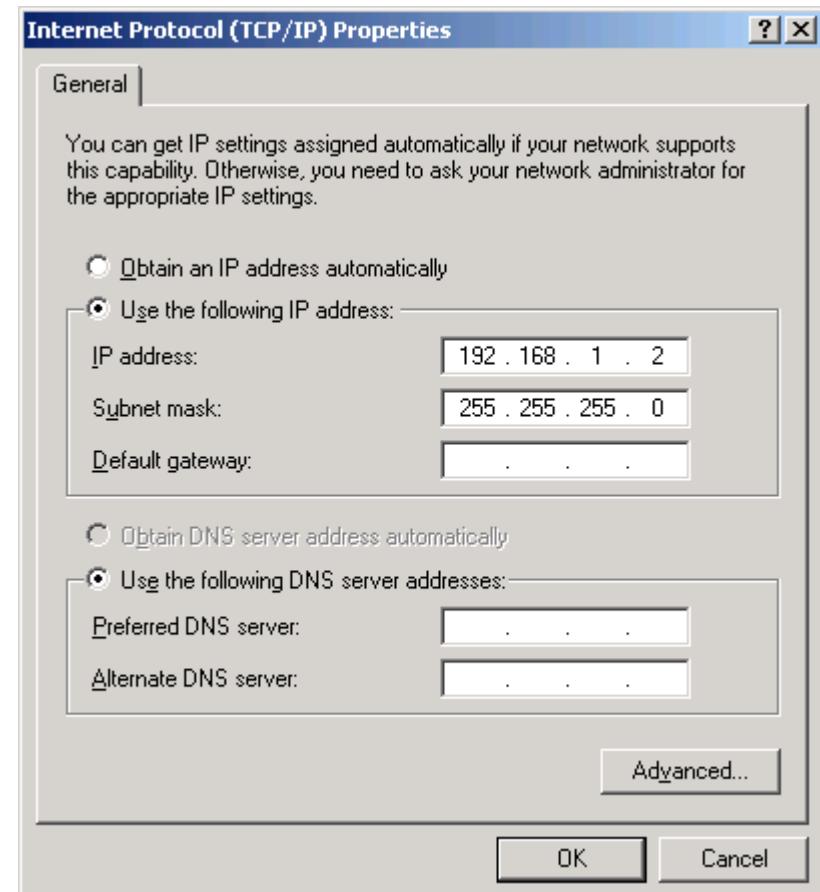
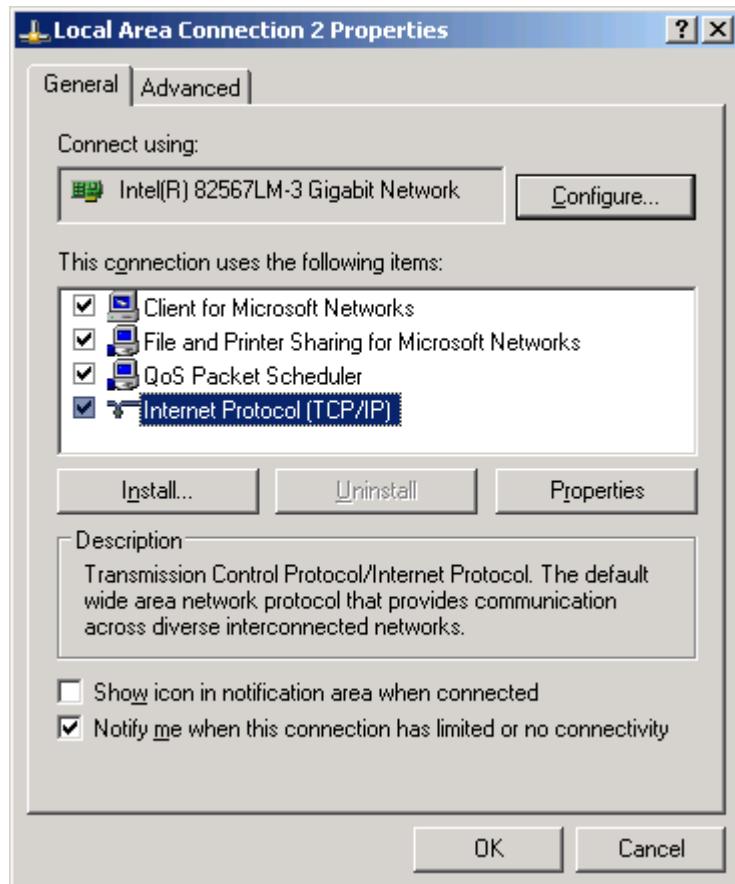
► Click Configure

- Set the Media Type to Auto for 1 Gbps then click OK



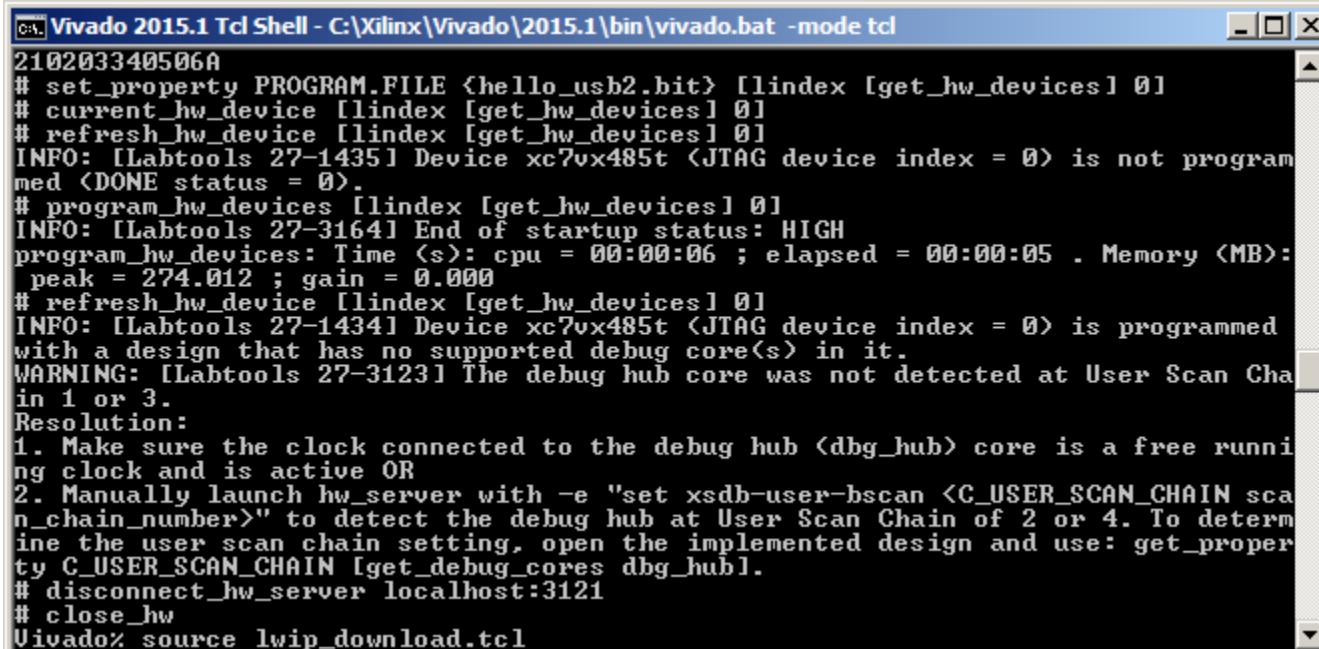
Run the LwIP Ethernet Design

- Reopen the properties after the last step
- Set your host (PC) to this IP Address:



Run the LwIP Ethernet Design

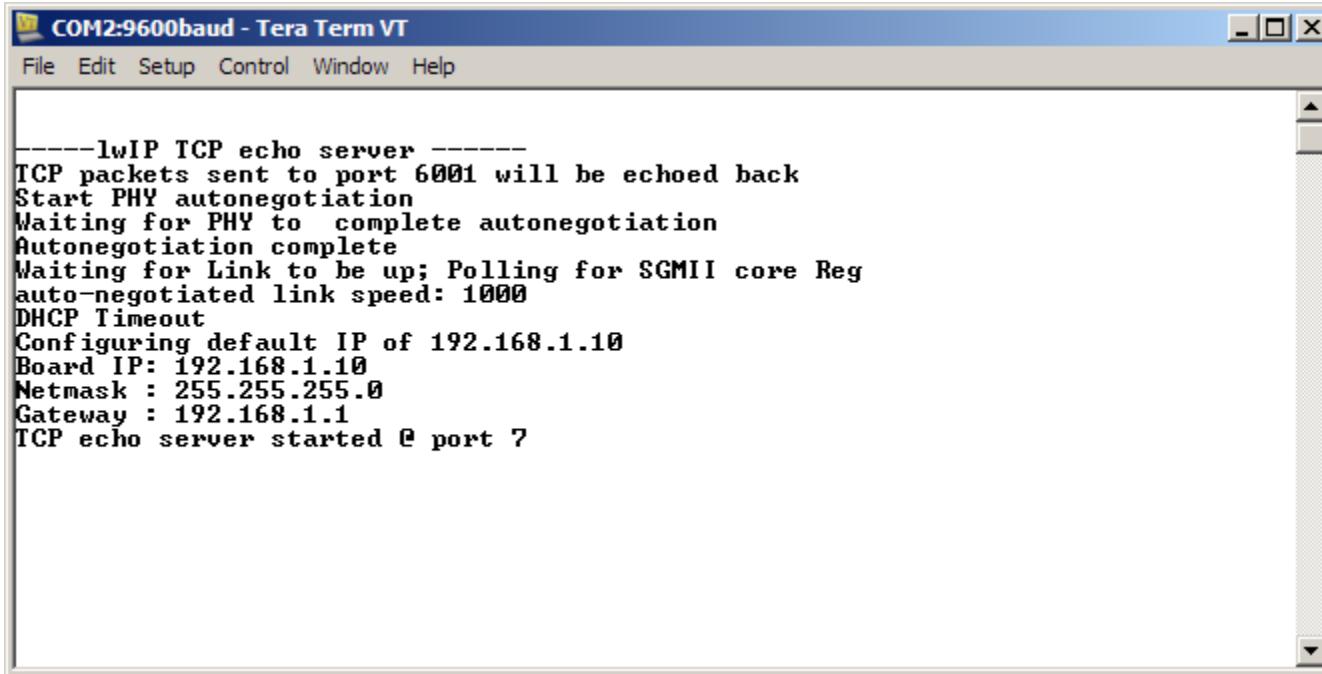
- Download the LwIP bitstream with Vivado
- In the Vivado Tcl Shell type:
source lwip_download.tcl



```
210203340506A
# set_property PROGRAM.FILE {hello_usb2.bit} [lindex [get_hw_devices] 0]
# current_hw_device [lindex [get_hw_devices] 0]
# refresh_hw_device [lindex [get_hw_devices] 0]
INFO: [Labtools 27-1435] Device xc7vx485t (JTAG device index = 0) is not programmed (DONE status = 0).
# program_hw_devices [lindex [get_hw_devices] 0]
INFO: [Labtools 27-3164] End of startup status: HIGH
program_hw_devices: Time <s>: cpu = 00:00:06 ; elapsed = 00:00:05 . Memory <MB>:
peak = 274.012 ; gain = 0.000
# refresh_hw_device [lindex [get_hw_devices] 0]
INFO: [Labtools 27-1434] Device xc7vx485t (JTAG device index = 0) is programmed with a design that has no supported debug core(s) in it.
WARNING: [Labtools 27-3123] The debug hub core was not detected at User Scan Chain 1 or 3.
Resolution:
1. Make sure the clock connected to the debug hub (dbg_hub) core is a free running clock and is active OR
2. Manually launch hw_server with -e "set xsdb-user-bscan <C_USER_SCAN_CHAIN scan_chain_number>" to detect the debug hub at User Scan Chain of 2 or 4. To determine the user scan chain setting, open the implemented design and use: get_property C_USER_SCAN_CHAIN [get_debug_cores dbg_hub].
# disconnect_hw_server localhost:3121
# close_hw
Vivado> source lwip_download.tcl
```

Run the LwIP Ethernet Design

► View LwIP echo server screen



The screenshot shows a window titled "COM2:9600baud - Tera Term VT". The menu bar includes File, Edit, Setup, Control, Window, and Help. The main window displays the following log output from the LwIP TCP echo server:

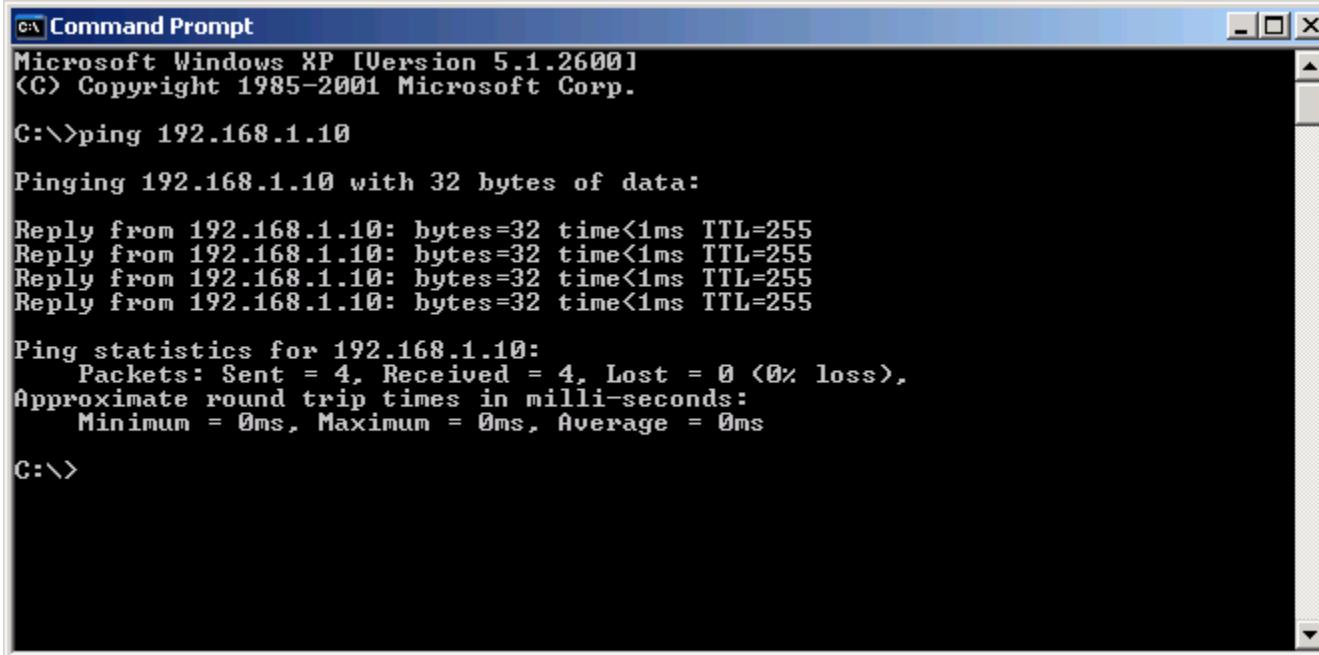
```
----lwIP TCP echo server ----
TCP packets sent to port 6001 will be echoed back
Start PHY autonegotiation
Waiting for PHY to complete autonegotiation
Autonegotiation complete
Waiting for Link to be up; Polling for SGMII core Reg
auto-negotiated link speed: 1000
DHCP Timeout
Configuring default IP of 192.168.1.10
Board IP: 192.168.1.10
Netmask : 255.255.255.0
Gateway : 192.168.1.1
TCP echo server started @ port 7
```

Run the LwIP Ethernet Design

► From a DOS window on the PC Host, enter the command:

ping 192.168.1.10

- Ping from PC host 192.168.1.2 to ZC706 target 192.168.1.10



```
C:\>Command Prompt
Microsoft Windows XP [Version 5.1.2600]
(C) Copyright 1985-2001 Microsoft Corp.

C:\>ping 192.168.1.10

Pinging 192.168.1.10 with 32 bytes of data:
Reply from 192.168.1.10: bytes=32 time<1ms TTL=255

Ping statistics for 192.168.1.10:
    Packets: Sent = 4, Received = 4, Lost = 0 (0% loss),
Approximate round trip times in milli-seconds:
    Minimum = 0ms, Maximum = 0ms, Average = 0ms

C:\>
```

References

References

► IP Integrator Documentation

- Vivado Design Suite Tcl Command Reference Guide – UG835
 - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2015_1/ug835-vivado-tcl-commands.pdf
- Designing IP Subsystems Using IP Integrator – UG994
 - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2015_1/ug994-vivado-ip-subsystems.pdf

► 7 Series Configuration

- 7 Series FPGAs Configuration User Guide
 - http://www.xilinx.com/support/documentation/user_guides/ug470_7Series_Config.pdf

References

► Vivado Release Notes

- Vivado Design Suite User Guide - Release Notes – UG973
 - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2015_1/ug973-vivado-release-notes-install-license.pdf
- Vivado Design Suite 2015.x - Vivado Known Issues
 - <http://www.xilinx.com/support/answers/63538.html>

► Vivado Programming and Debugging

- Vivado Design Suite Programming and Debugging User Guide – UG908
 - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2015_1/ug908-vivado-programming-debugging.pdf

Documentation

Documentation

➤ Virtex-7

- Virtex-7 FPGA Family
 - <http://www.xilinx.com/products/silicon-devices/fpga/virtex-7/index.htm>
- Design Advisory Master Answer Record for Virtex-7 FPGAs
 - <http://www.xilinx.com/support/answers/42944.htm>

➤ VC707 Documentation

- Virtex-7 FPGA VC707 Evaluation Kit
 - <http://www.xilinx.com/products/boards-and-kits/ek-v7-vc707-g.html>
- VC707 Getting Started Guide – UG848
 - http://www.xilinx.com/support/documentation/boards_and_kits/ vc707/ug848-VC707-getting-started-guide.pdf
- VC707 User Guide – UG885
 - http://www.xilinx.com/support/documentation/boards_and_kits/ vc707/ug885_VC707_Eval_Bd.pdf