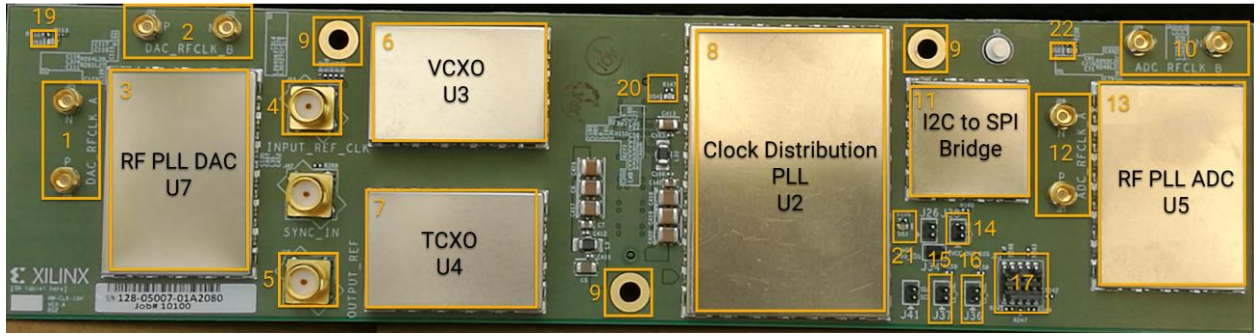
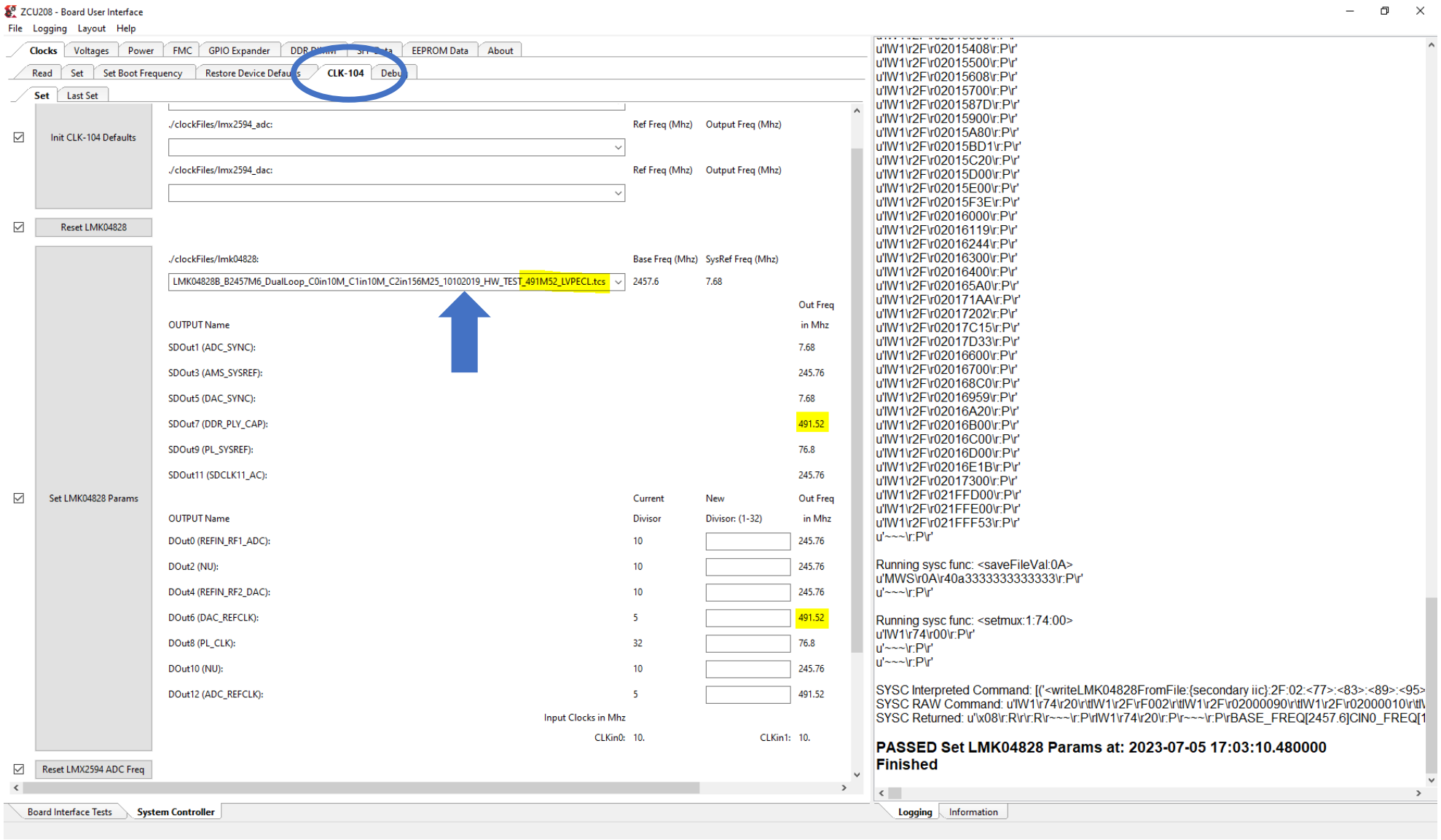
Frequency Folding Tool

CLK104 RF PLL ADC/DAC

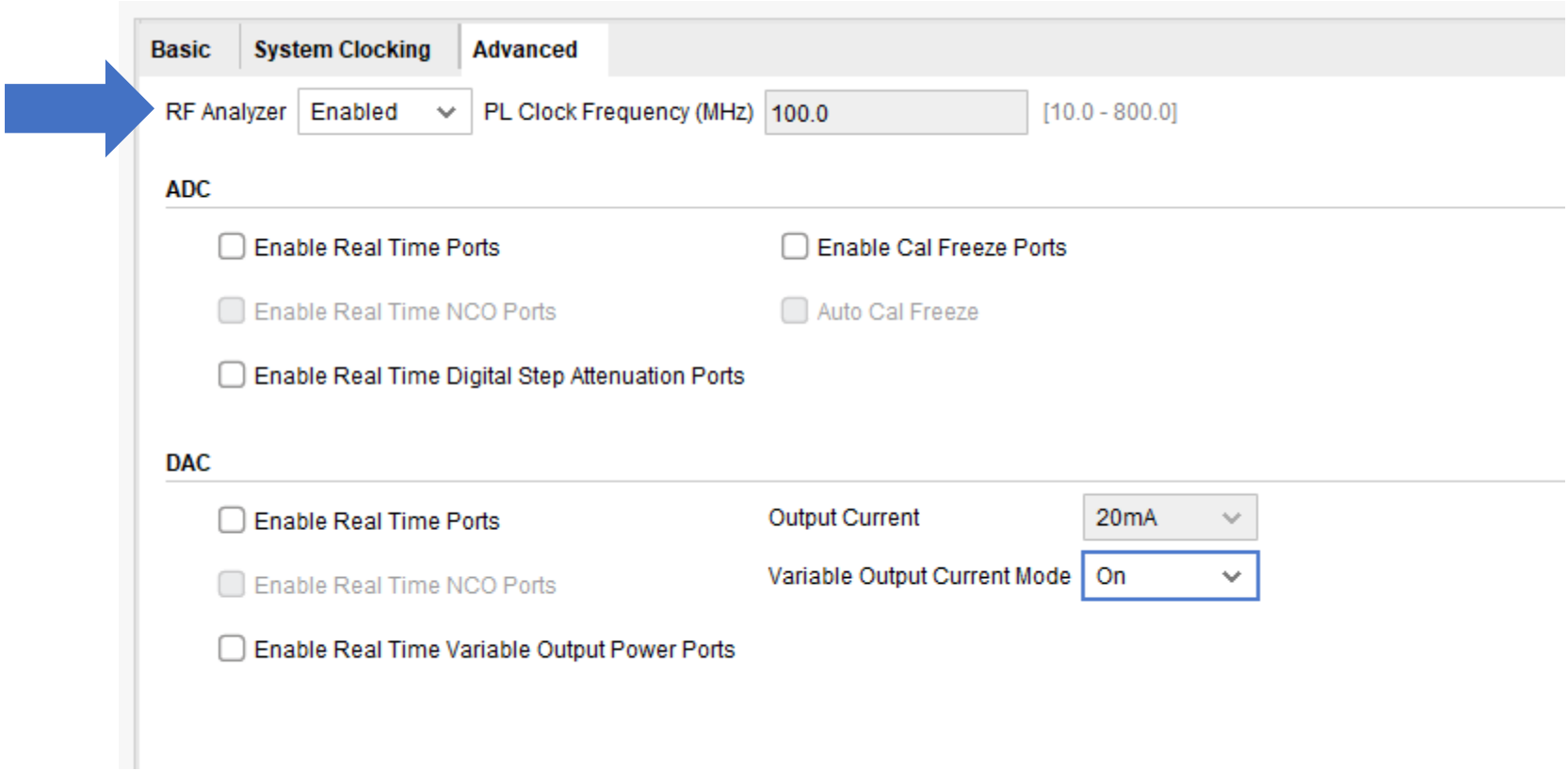


Callout	Reference Designation	Description
1	J20, J21	DAC_RFCLK_A, DAC RF PLL output A
12	J27, J28	ADC_RFCLK_A, ADC RF PLL output A

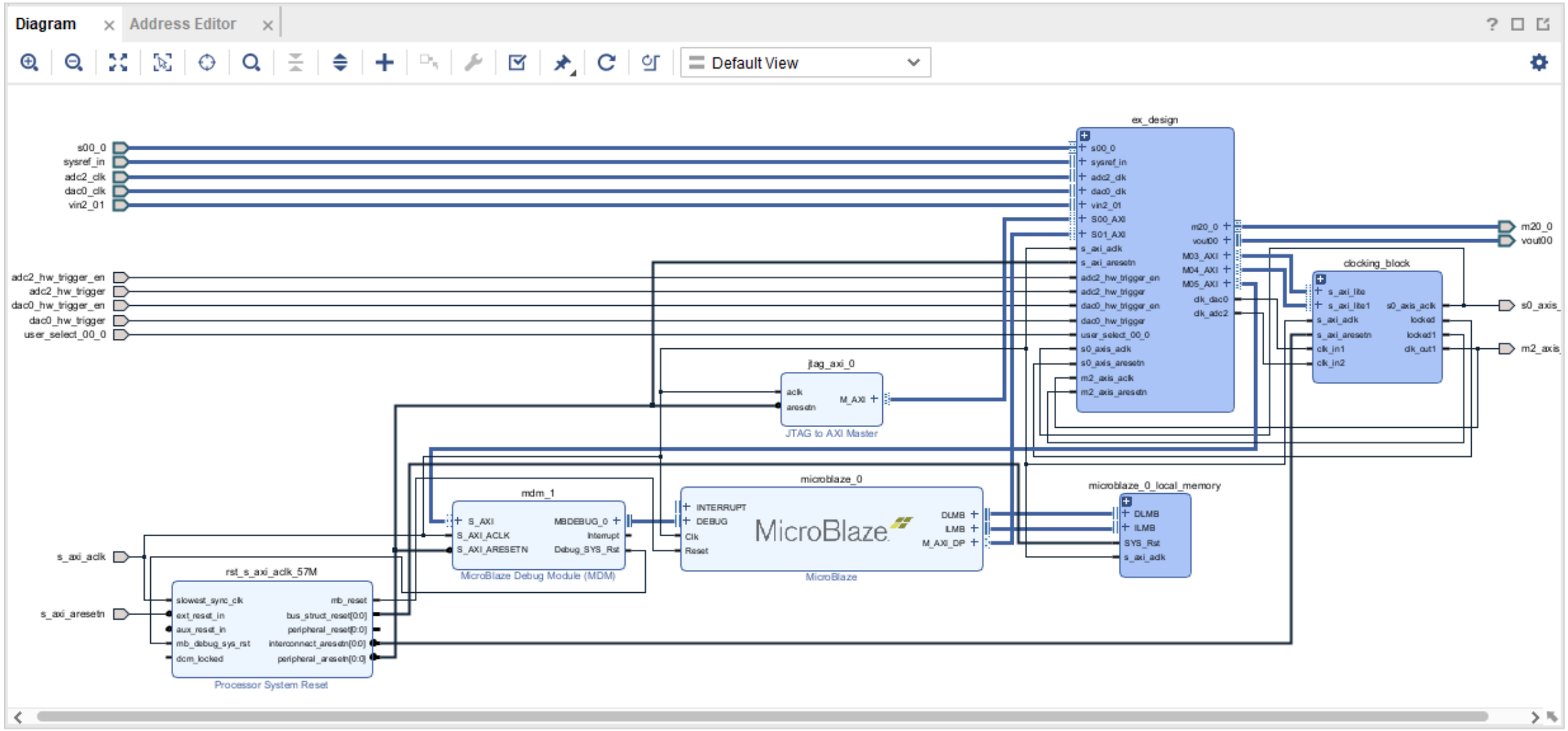
Configuring Clock via System Controller



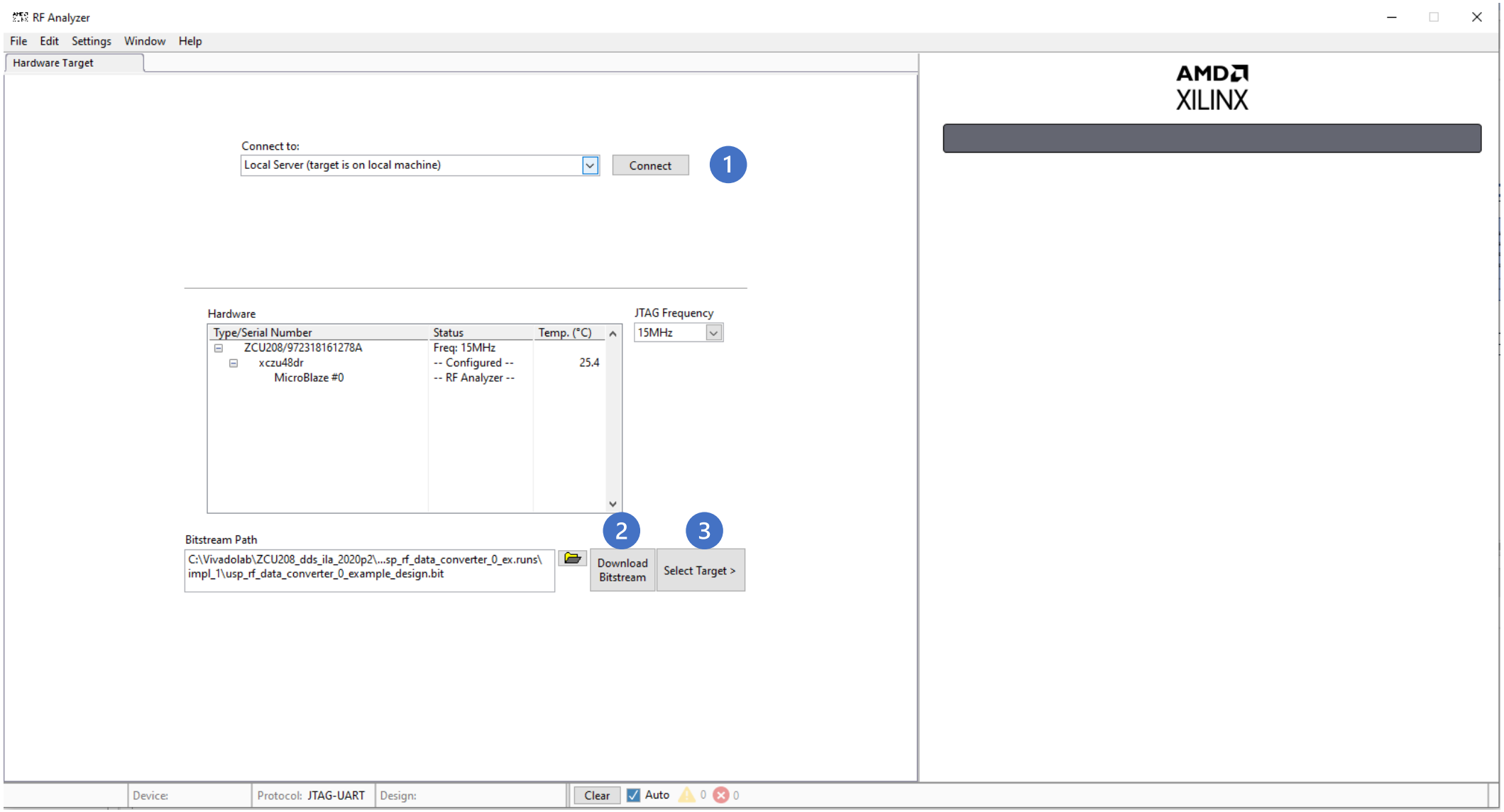
Advanced


Basic
System Clocking
Advanced
RF Analyzer
Enabled
PL Clock Frequency (MHz)
100.0
[10.0 - 800.0]
ADC
Enable Real Time Ports
Enable Cal Freeze Ports
Enable Real Time NCO Ports
Auto Cal Freeze
Enable Real Time Digital Step Attenuation Ports
DAC
Enable Real Time Ports
Output Current
20mA
Enable Real Time NCO Ports
Variable Output Current Mode
On
Enable Real Time Variable Output Power Ports

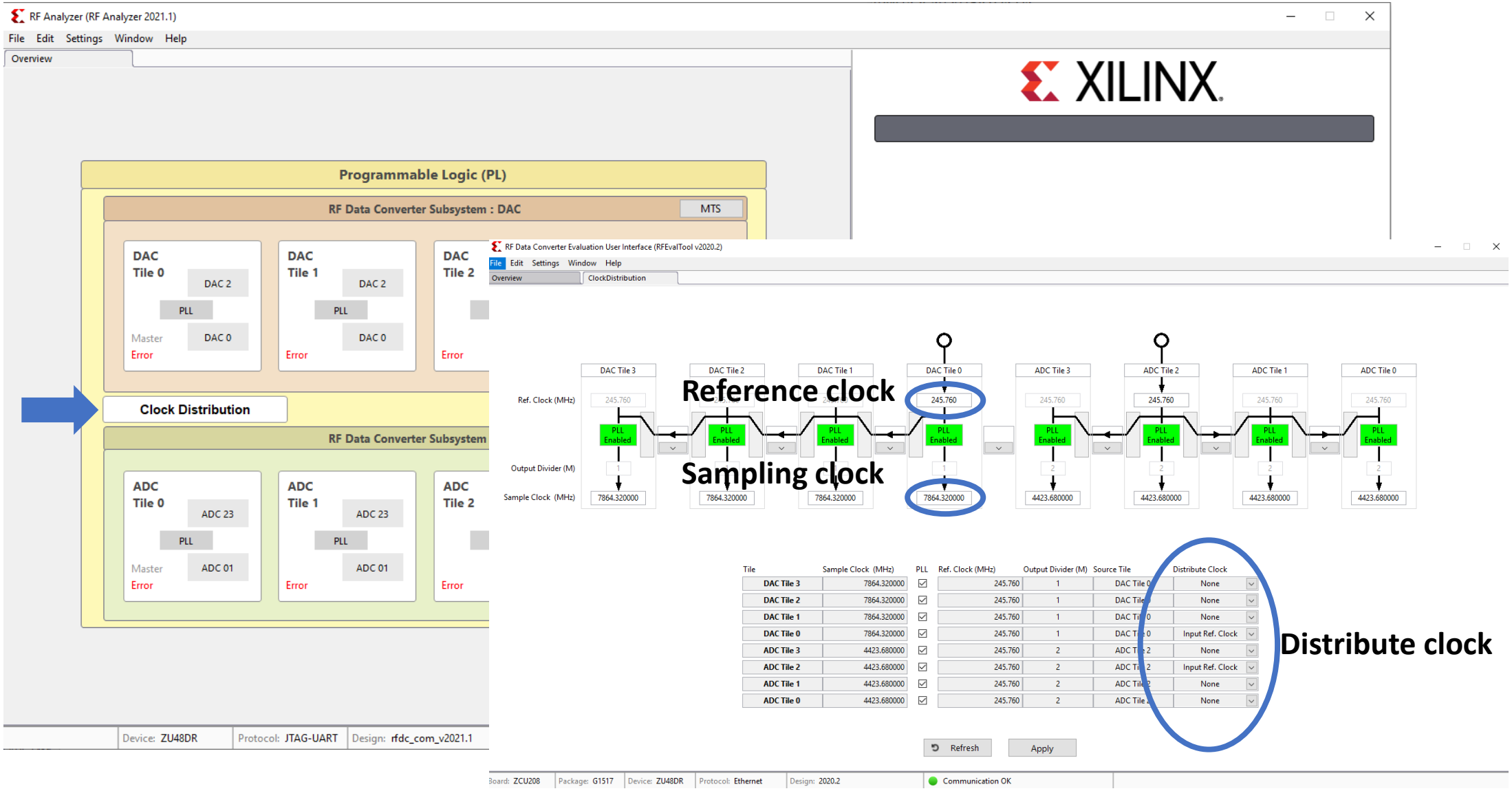
Example Design



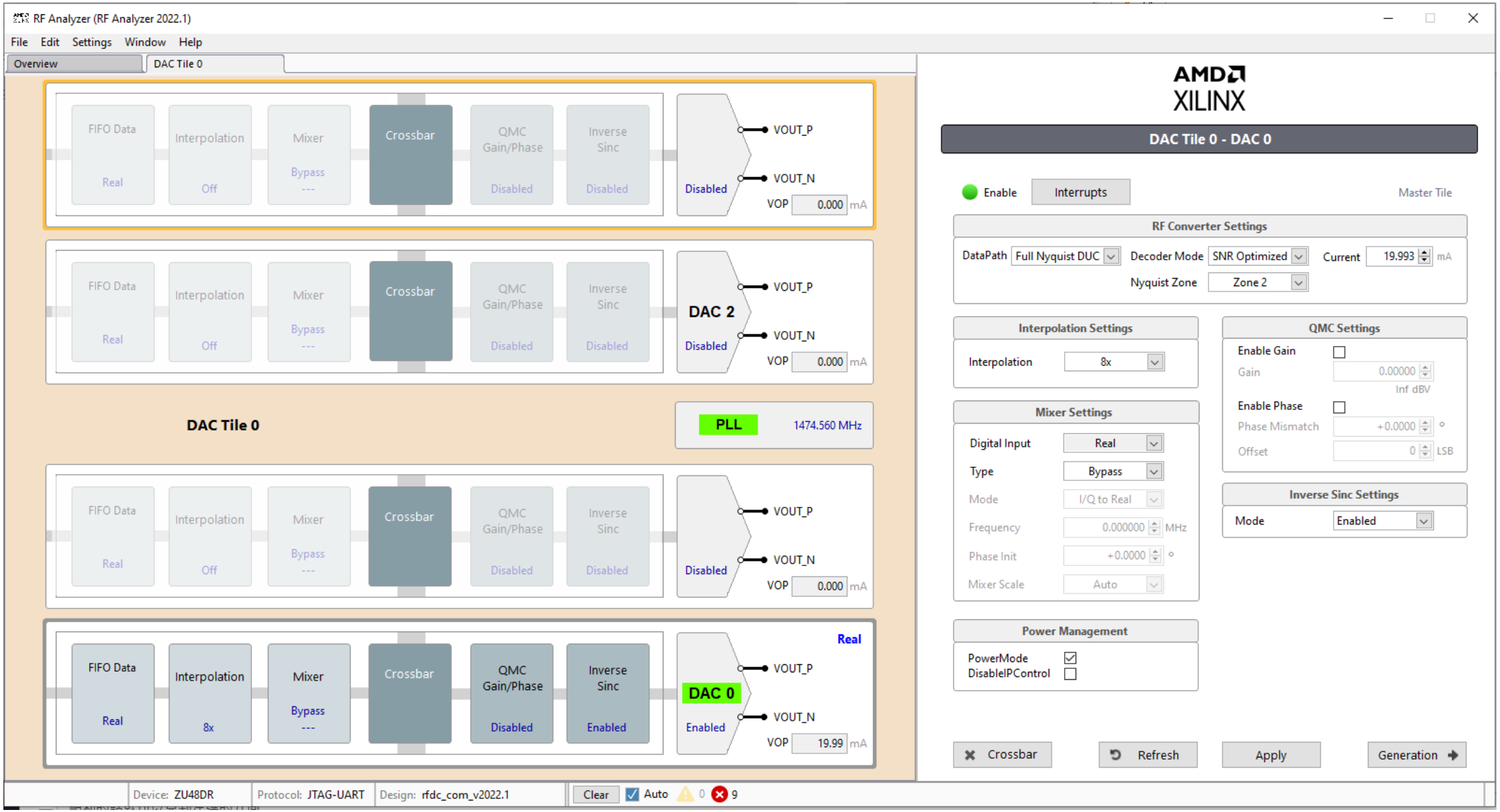
RF Analyzer


RF Analyzer
File Edit Settings Window Help
Hardware Target
AMD
XILINX
Connect to:
Local Server (target is on local machine)
Connect
1
Hardware
Type/Serial Number
Status
Temp. (°C)
ZCU208/972318161278A
Freq: 15MHz
xczu48dr
-- Configured --
25.4
MicroBlaze #0
-- RF Analyzer --
JTAG Frequency
15MHz
2
3
Bitstream Path
C:\Vivadolab\ZCU208_dds_ila_2020p2\...sp_rf_data_converter_0_ex.runs\impl_1\usp_rf_data_converter_0_example_design.bit
Download Bitstream
Select Target >
Device:
Protocol: JTAG-UART
Design:
Clear
Auto
0
0

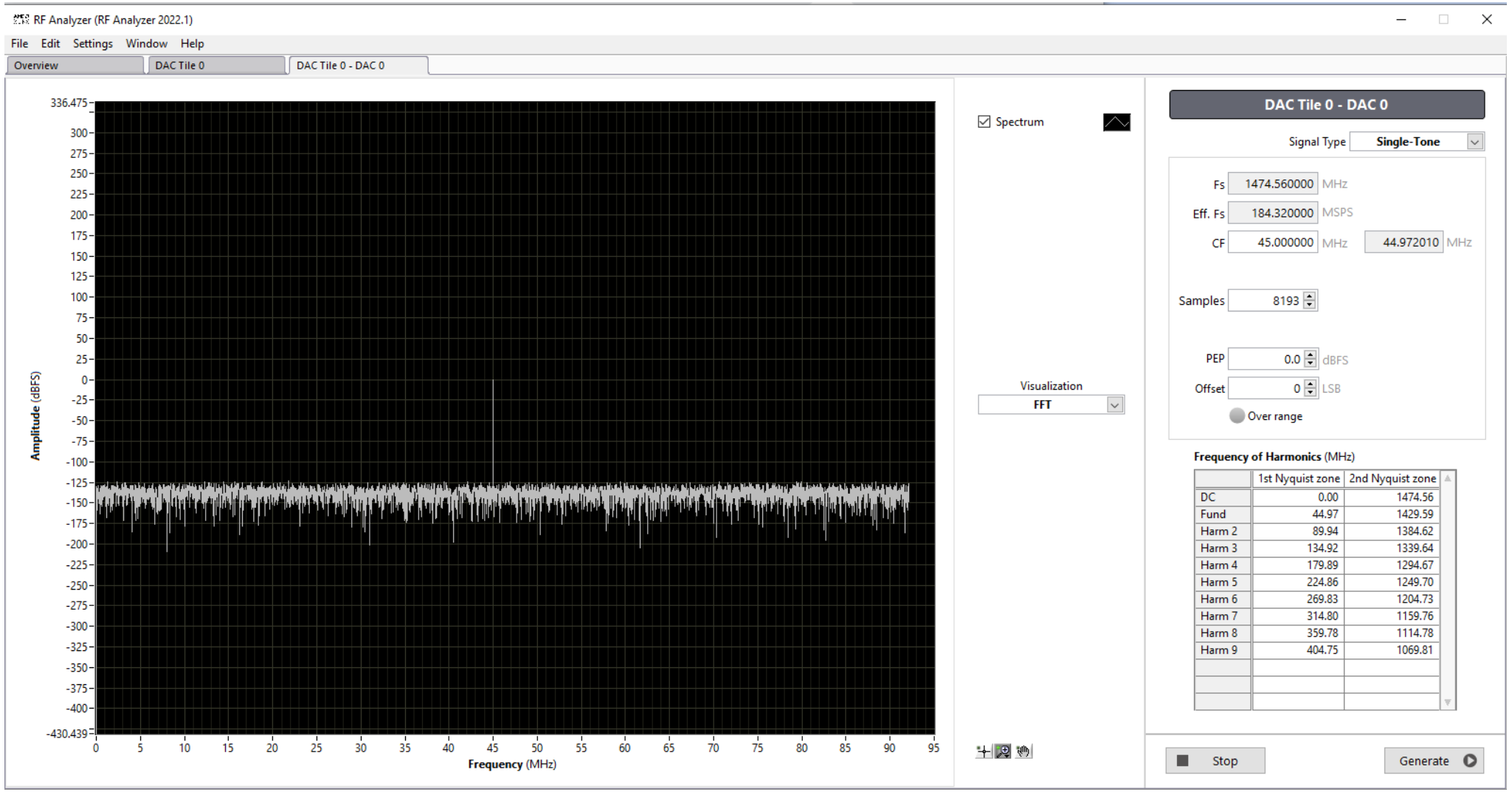
Configuring Clock via RF analyzer



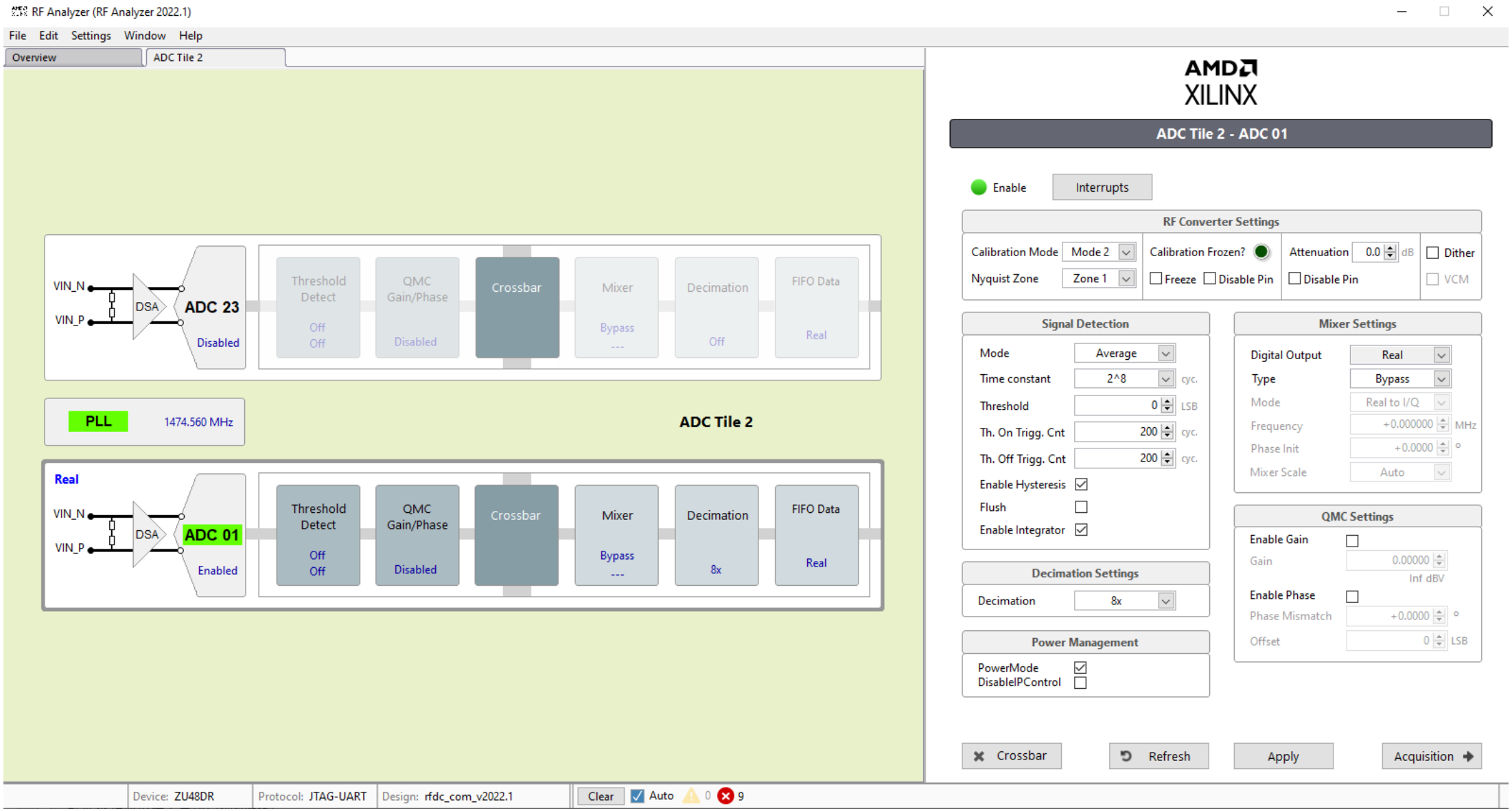
RF Analyzer


RF Analyzer (RF Analyzer 2022.1)
File Edit Settings Window Help
Overview
DAC Tile 0
FIFO Data Real
Interpolation Off
Mixer Bypass ---
Crossbar
QMC Gain/Phase Disabled
Inverse Sinc Disabled
Disabled
VOUT_P
VOUT_N
VOP 0.000 mA
DAC 2
DAC Tile 0
PLL 1474.560 MHz
FIFO Data Real
Interpolation 8x
Mixer Bypass ---
QMC Gain/Phase Disabled
Inverse Sinc Enabled
DAC 0
Enabled
Real
VOP 19.99 mA
AMD XILINX
DAC Tile 0 - DAC 0
Enable
Interrupts
Master Tile
RF Converter Settings
DataPath Full Nyquist DUC
Decoder Mode SNR Optimized
Current 19.993 mA
Nyquist Zone Zone 2
Interpolation Settings
Interpolation 8x
QMC Settings
Enable Gain
Gain 0.00000
Inf dBV
Enable Phase
Phase Mismatch +0.0000
Offset 0 LSB
Mixer Settings
Digital Input Real
Type Bypass
Mode I/Q to Real
Frequency 0.000000 MHz
Phase Init +0.0000
Mixer Scale Auto
Inverse Sinc Settings
Mode Enabled
Power Management
PowerMode
DisableIPControl
Crossbar
Refresh
Apply
Generation
Device: ZU48DR
Protocol: JTAG-UART
Design: rfdc_com_v2022.1
Clear
Auto
0
9

RF Analyzer


RF Analyzer (RF Analyzer 2022.1)
File Edit Settings Window Help
Overview
DAC Tile 0
DAC Tile 0 - DAC 0
Amplitude (dBFS)
Frequency (MHz)
Spectrum
Visualization
FFT
DAC Tile 0 - DAC 0
Signal Type
Single-Tone
Fs 1474.560000 MHz
Eff. Fs 184.320000 MSPS
CF 45.000000 MHz 44.972010 MHz
Samples 8193
PEP 0.0 dBFS
Offset 0 LSB
Over range
Frequency of Harmonics (MHz)
1st Nyquist zone
2nd Nyquist zone
DC 0.00 1474.56
Fund 44.97 1429.59
Harm 2 89.94 1384.62
Harm 3 134.92 1339.64
Harm 4 179.89 1294.67
Harm 5 224.86 1249.70
Harm 6 269.83 1204.73
Harm 7 314.80 1159.76
Harm 8 359.78 1114.78
Harm 9 404.75 1069.81
Stop
Generate

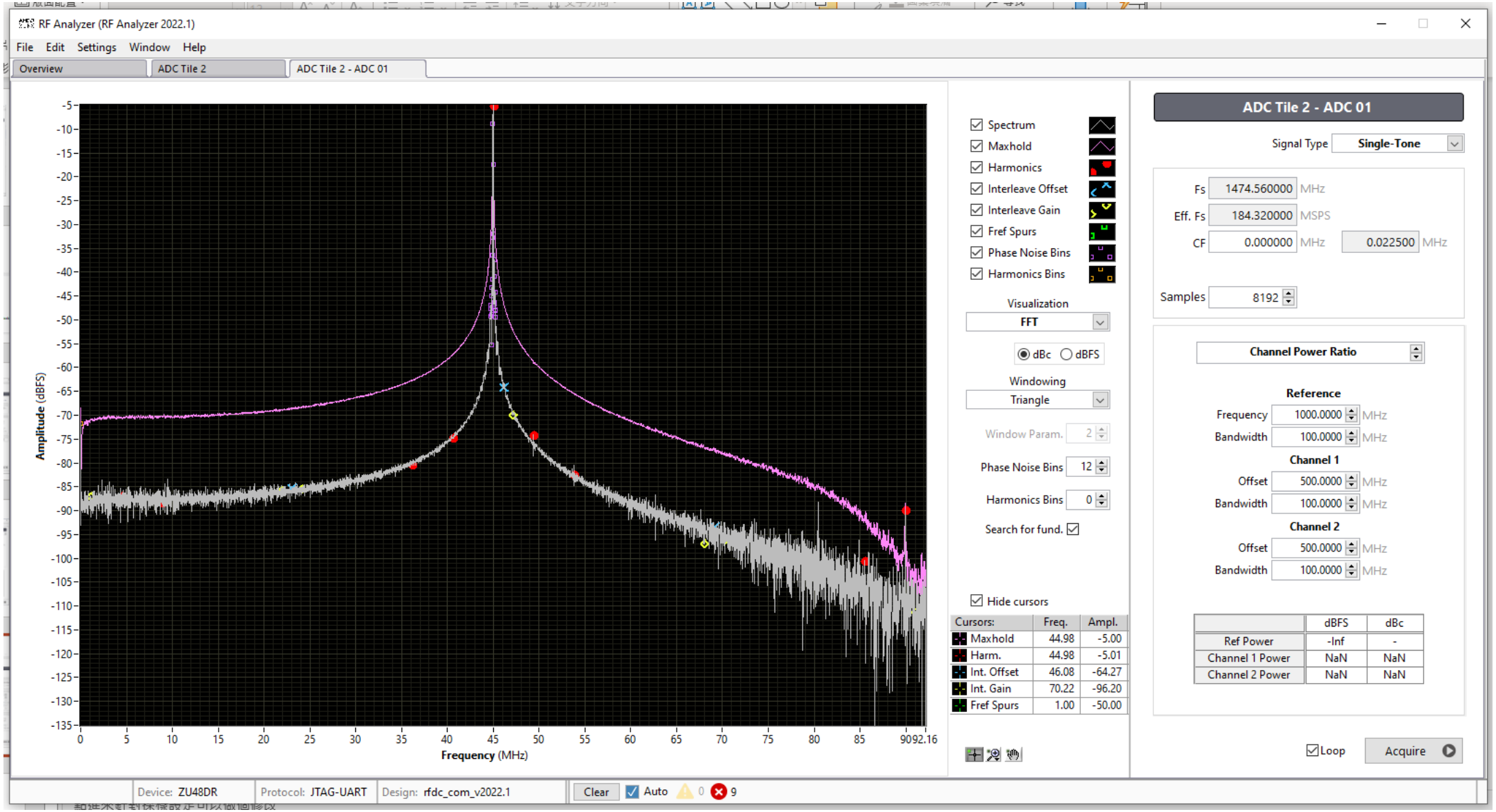
RF Analyzer


RF Analyzer (RF Analyzer 2022.1)
File Edit Settings Window Help
Overview
ADC Tile 2
VIN_N
VIN_P
DSA
ADC 23
Disabled
Threshold Detect
Off
Off
QMC Gain/Phase
Disabled
Crossbar
Mixer
Bypass

Decimation
Off
FIFO Data
Real
PLL
1474.560 MHz
ADC Tile 2
Real
ADC 01
Enabled
Threshold Detect
Off
Off
QMC Gain/Phase
Disabled
Crossbar
Mixer
Bypass

Decimation
8x
FIFO Data
Real
AMD
XILINX
ADC Tile 2 - ADC 01
Enable
Interrupts
RF Converter Settings
Calibration Mode
Mode 2
Calibration Frozen?
Attenuation
0.0
dB
Dither
Nyquist Zone
Zone 1
Freeze
Disable Pin
Disable Pin
VCM
Signal Detection
Mode
Average
Time constant
2^8
cyc.
Threshold
0
LSB
Th. On Trigg. Cnt
200
cyc.
Th. Off Trigg. Cnt
200
cyc.
Enable Hysteresis
Flush
Enable Integrator
Mixer Settings
Digital Output
Real
Type
Bypass
Mode
Real to I/Q
Frequency
+0.000000
MHz
Phase Init
+0.0000
°
Mixer Scale
Auto
QMC Settings
Enable Gain
Gain
0.00000
Inf dBV
Enable Phase
Phase Mismatch
+0.0000
°
Offset
0
LSB
Decimation Settings
Decimation
8x
Power Management
PowerMode
DisableIPControl
Crossbar
Refresh
Apply
Acquisition
Device: ZU48DR
Protocol: JTAG-UART
Design: rfdc_com_v2022.1
Clear
Auto
0
9

RF Analyzer


RF Analyzer (RF Analyzer 2022.1)
File Edit Settings Window Help
Overview
ADC Tile 2
ADC Tile 2 - ADC 01
Amplitude (dBFS)
Frequency (MHz)
Spectrum
Maxhold
Harmonics
Interleave Offset
Interleave Gain
Fref Spurs
Phase Noise Bins
Harmonics Bins
Visualization
FFT
dBc dBFS
Windowing
Triangle
Window Param. 2
Phase Noise Bins 12
Harmonics Bins 0
Search for fund.
Hide cursors
Cursors: Freq. Ampl.
Maxhold 44.98 -5.00
Harm. 44.98 -5.01
Int. Offset 46.08 -64.27
Int. Gain 70.22 -96.20
Fref Spurs 1.00 -50.00
ADC Tile 2 - ADC 01
Signal Type Single-Tone
Fs 1474.560000 MHz
Eff. Fs 184.320000 MSPS
CF 0.000000 MHz 0.022500 MHz
Samples 8192
Channel Power Ratio
Reference
Frequency 1000.0000 MHz
Bandwidth 100.0000 MHz
Channel 1
Offset 500.0000 MHz
Bandwidth 100.0000 MHz
Channel 2
Offset 500.0000 MHz
Bandwidth 100.0000 MHz
dBFS dBc
Ref Power -Inf -
Channel 1 Power NaN NaN
Channel 2 Power NaN NaN
Loop
Acquire
Device: ZU48DR
Protocol: JTAG-UART
Design: rfdc_com_v2022.1
Clear
Auto

Reference

ZCU208 Evaluation Board User Guide (UG1410)

RF Data Converter Interface User Guide (UG1309)

DDS Compiler v6.0 Product Guide (PG141)

Zynq UltraScale+ RFSoC RF Data Converter v2.5 Gen 1/2/3 Product Guide (PG269)

Thank You