HDMI_ZC702

AMD
together we advance_

Vivado IP Integrator

1. Generating image patterns by PL.

2. Transferring Data to PS via VDMA.

3. Using DDR as buffer , and returning control signals and image data to PL via VDMA.

4. Image formatting.(AXIS)

5. Generate timing information.

6. Merge the image data with the timing information to output the video data. (AXIS > Video)

7. Output Interface.

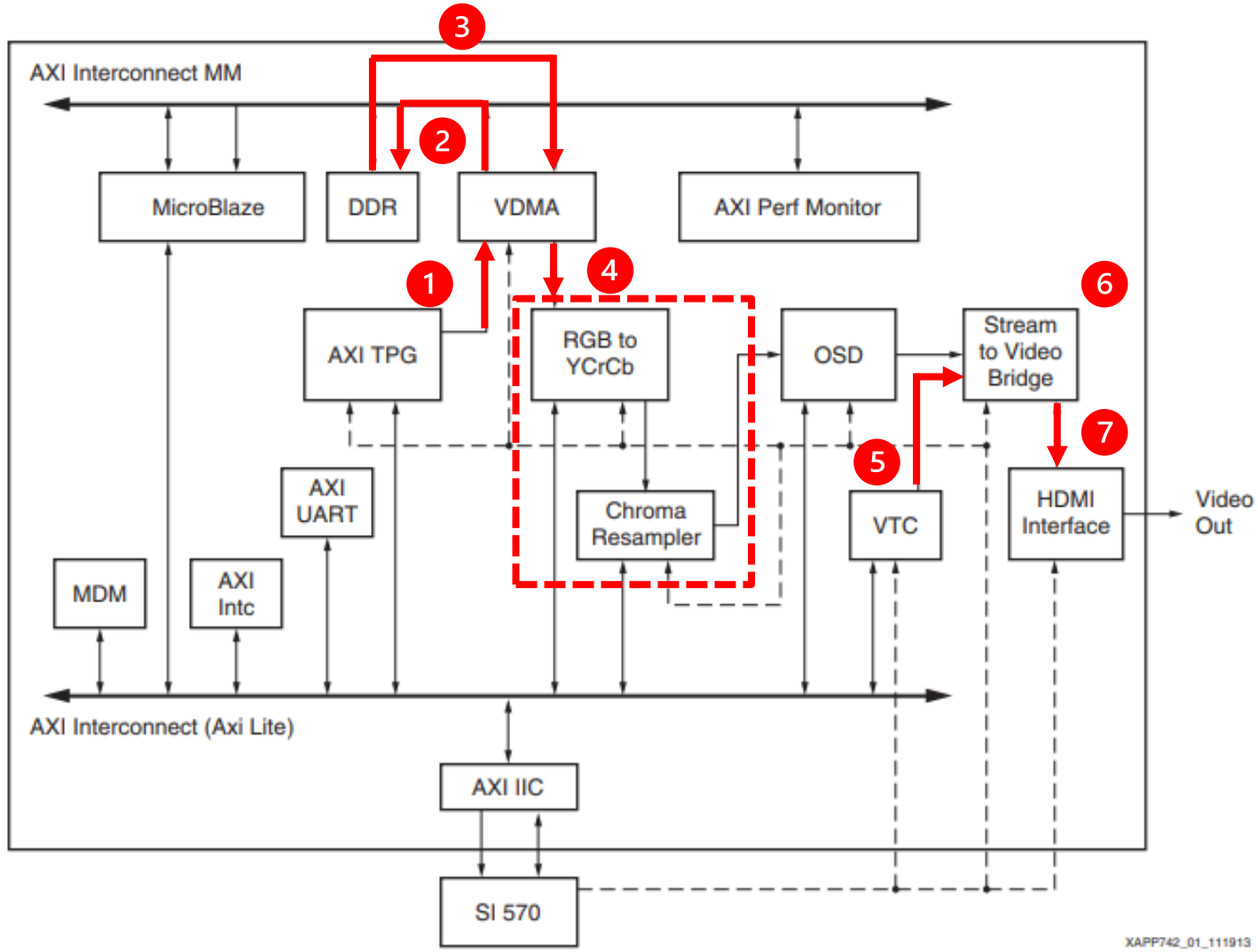


Figure 1: **Reference System Block Diagram**

Block Diagram

AXI VDMA

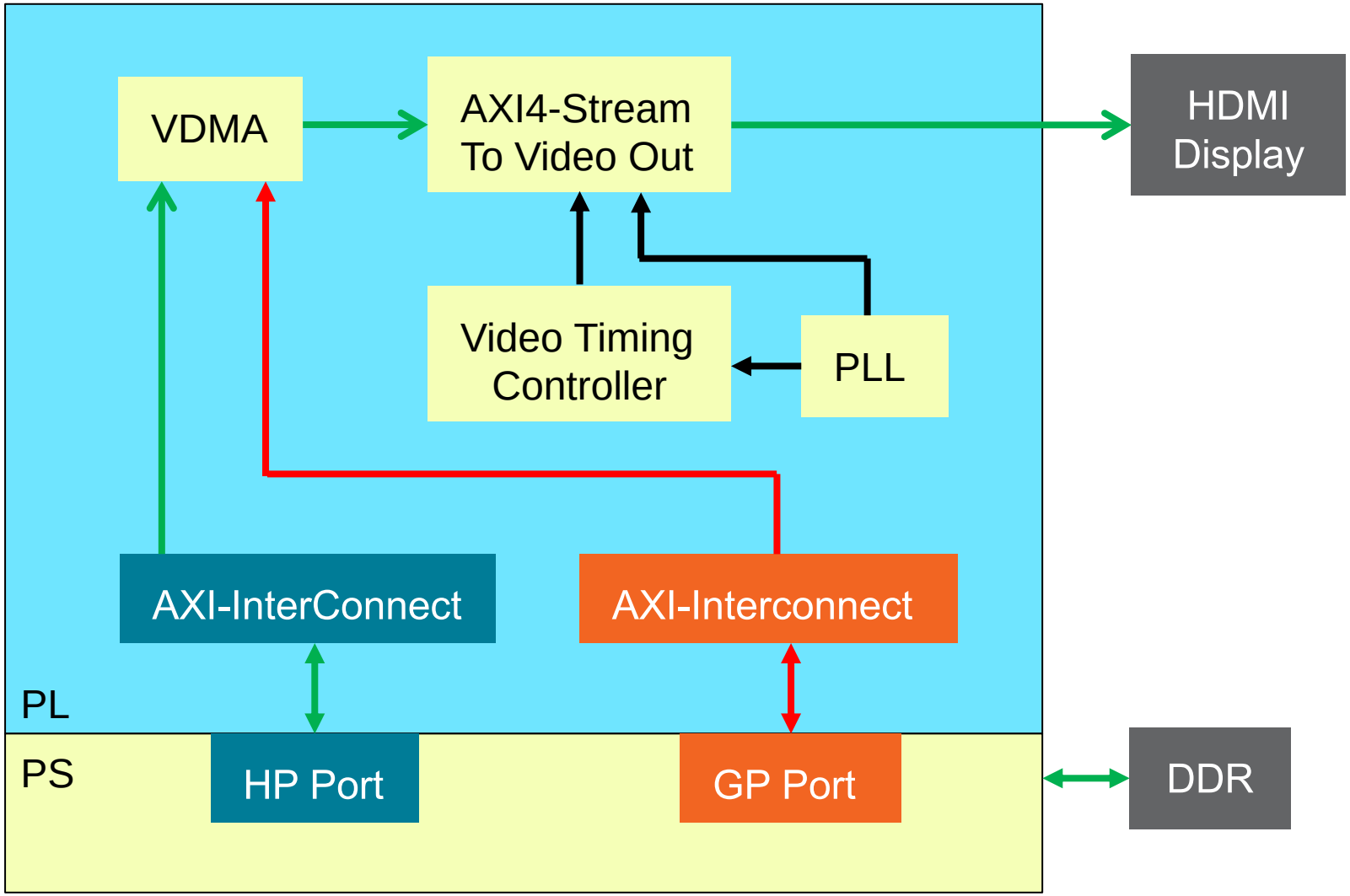
provide video read/write transfer capabilities from the AXI4 memory-mapped domain to the AXI4-Stream domain.

Video Timing Controller

The VTC LogiCORE™ IP is a general-purpose video timing generator and detector.
The output side of the core generates the horizontal and vertical blanking and synchronization pulses used in a standard video system and includes support for programmable pulse polarity.

Video Timing Controller

The TPG block can generate several video test patterns that are commonly used in the video industry for verification and testing.
In the reference design, the TPG is used as a replacement to a video source because only the amount of traffic generated to demonstrate the performance of the system is of interest



Block Diagram

AXI VDMA

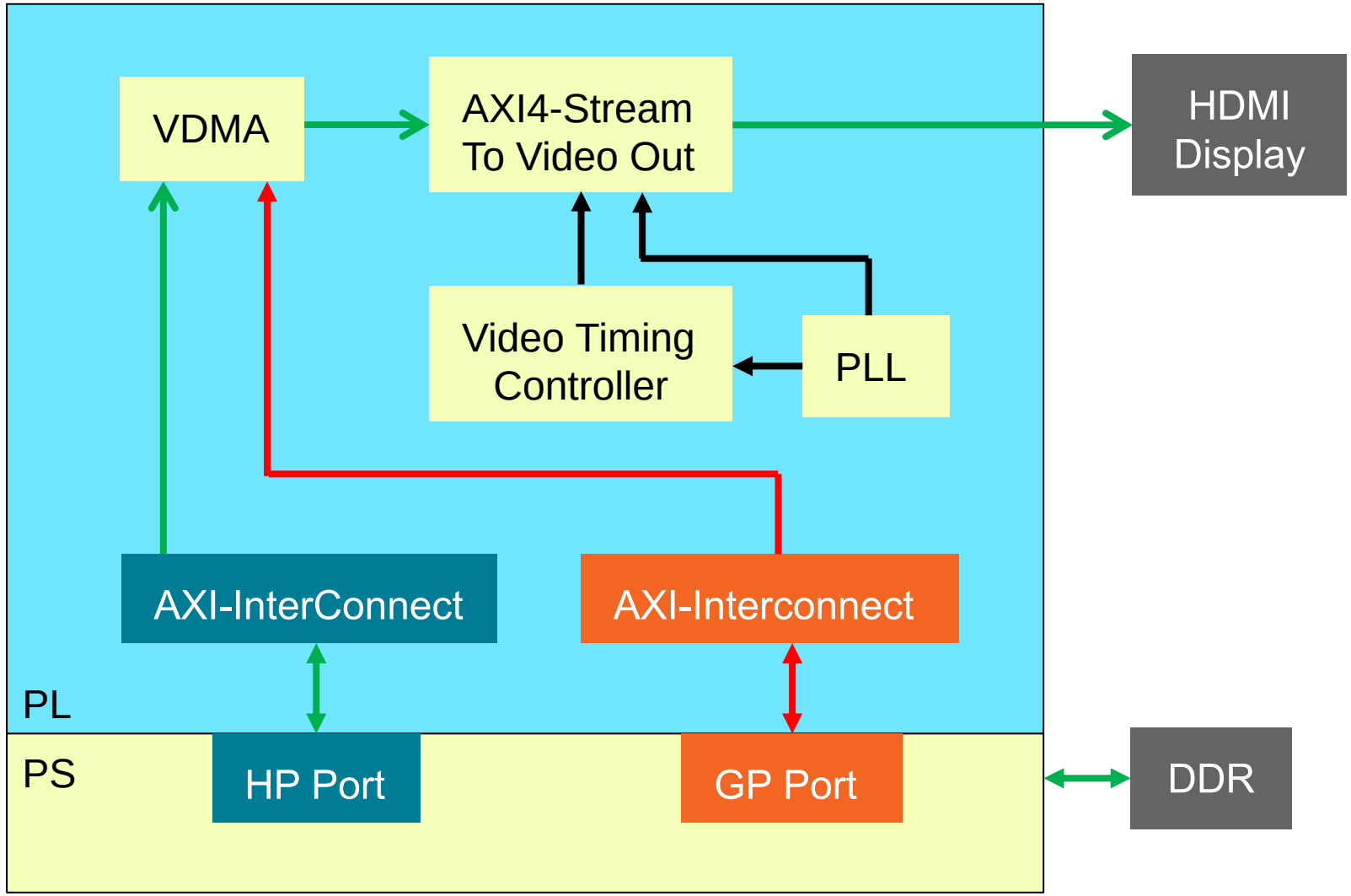
provide video read/write transfer capabilities from the AXI4 memory-mapped domain to the AXI4-Stream domain.

Video Timing Controller

The VTC LogiCORE™ IP is a general-purpose video timing generator and detector.
The output side of the core generates the horizontal and vertical blanking and synchronization pulses used in a standard video system and includes support for programmable pulse polarity.

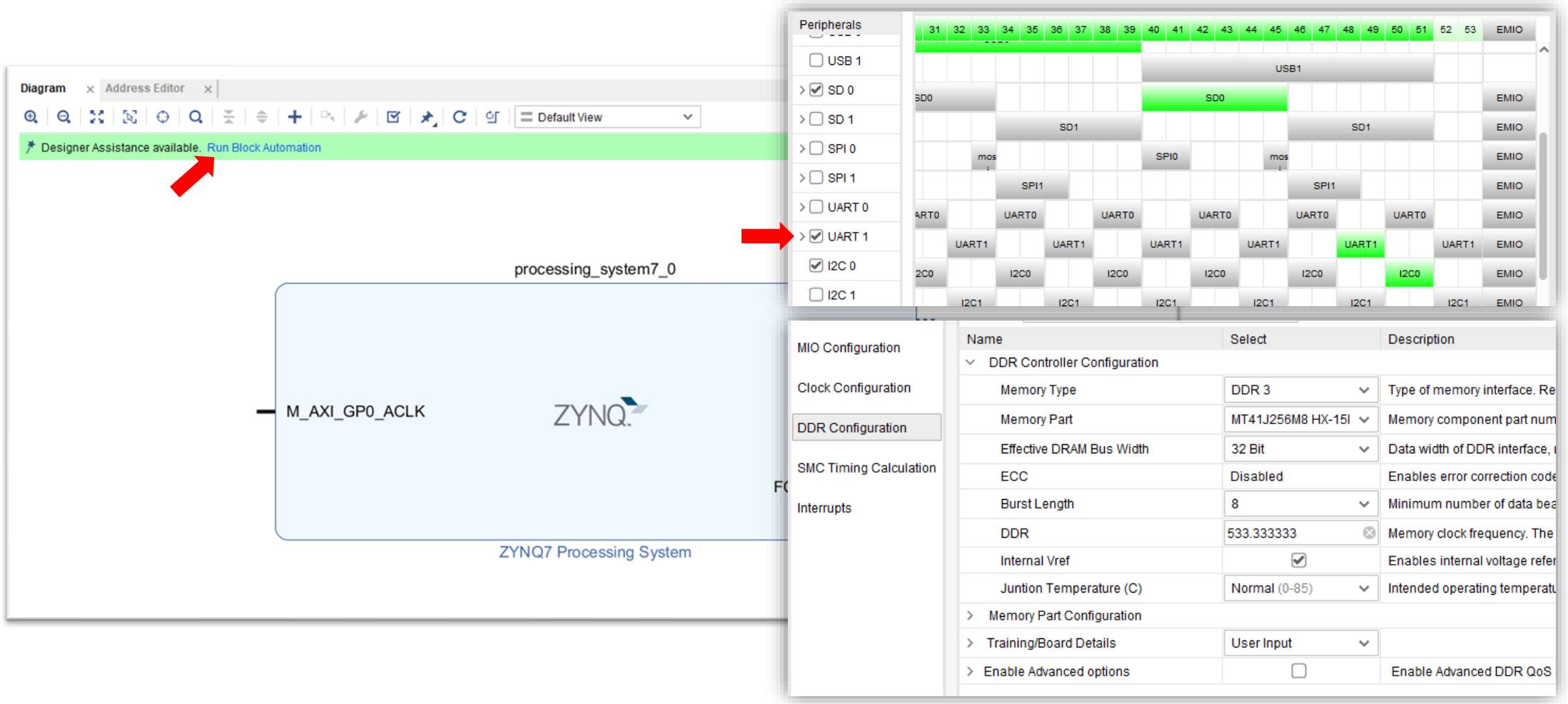
Video Timing Controller

The TPG block can generate several video test patterns that are commonly used in the video industry for verification and testing.
In the reference design, the TPG is used as a replacement to a video source because only the amount of traffic generated to demonstrate the performance of the system is of interest



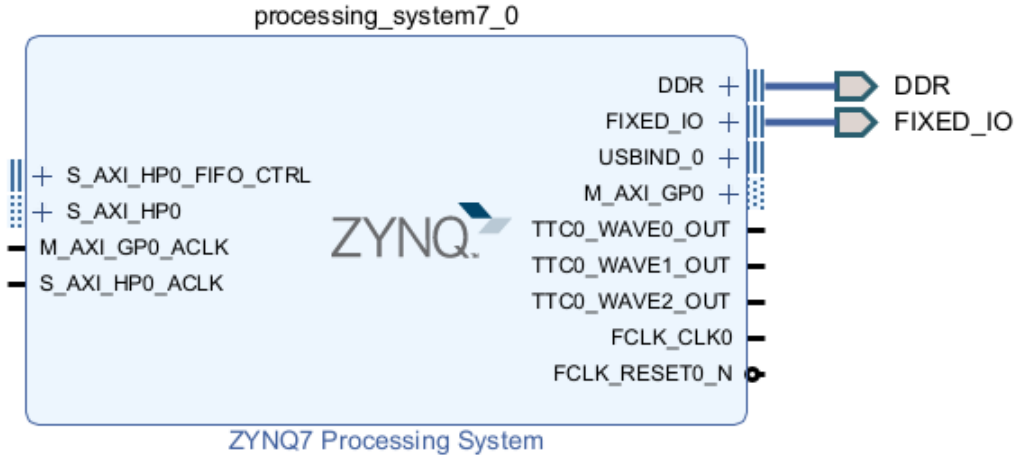
Zynq

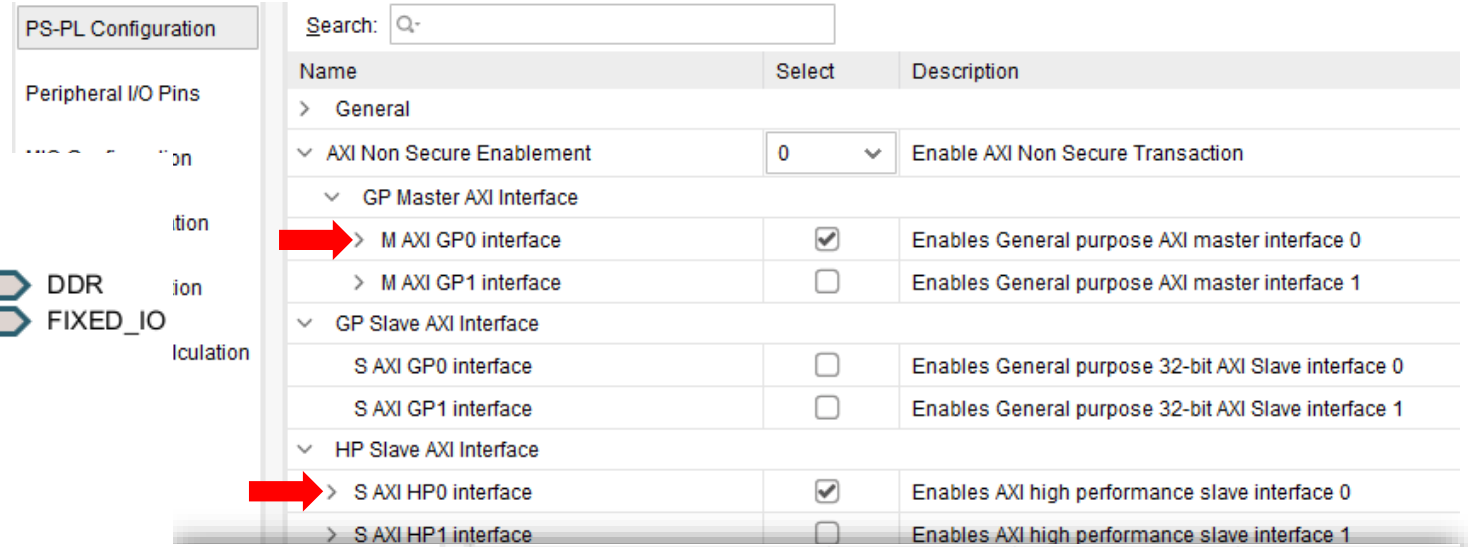
Click Run Block Automation to configure the settings for DDR and IO.
(Ensure that the UART interface is enabled.)

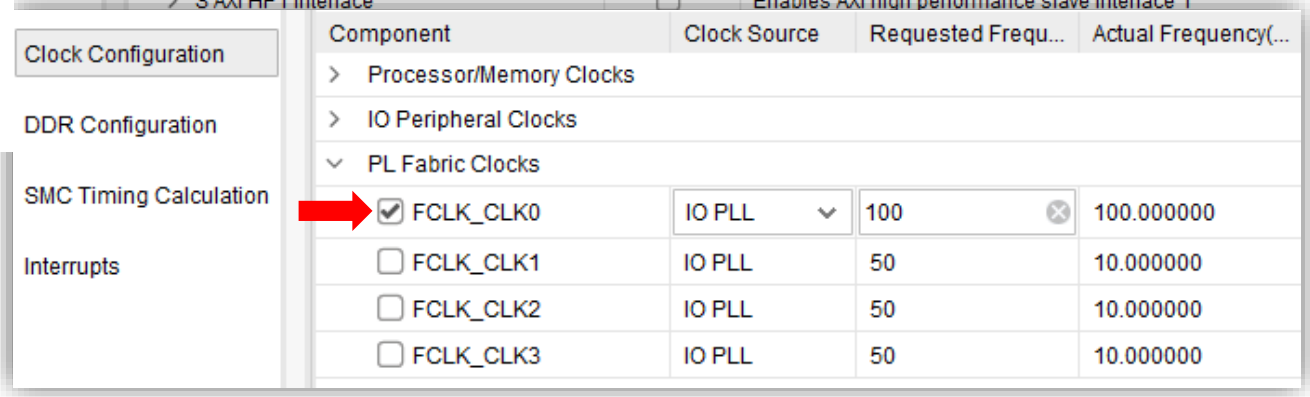


Zynq

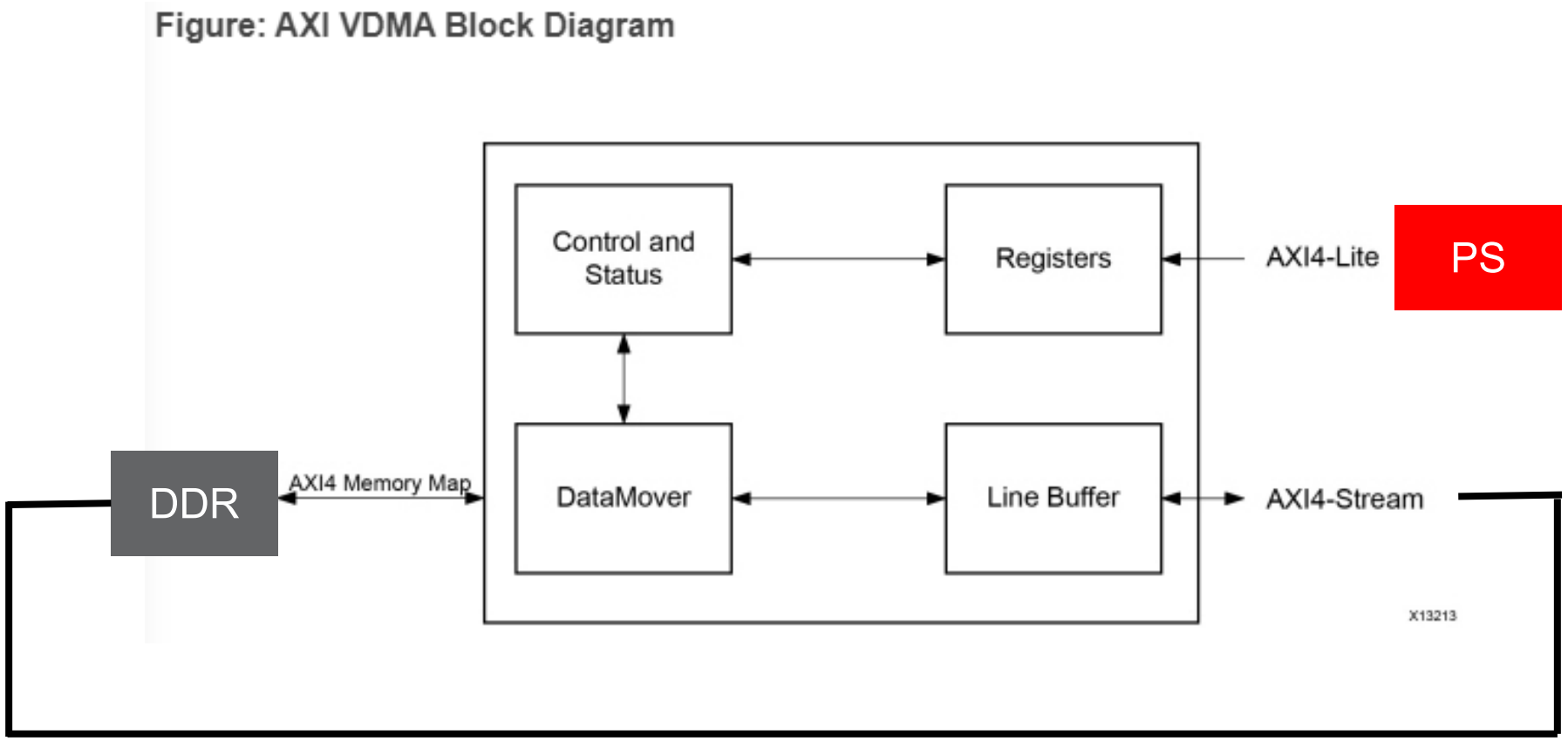
- Enable M AXI GP0 port for communication control on the PS side.
- Enable S AXI HP0 port for high-speed data transmission.
- Change the PL Fabric Clocks to 100MHz.



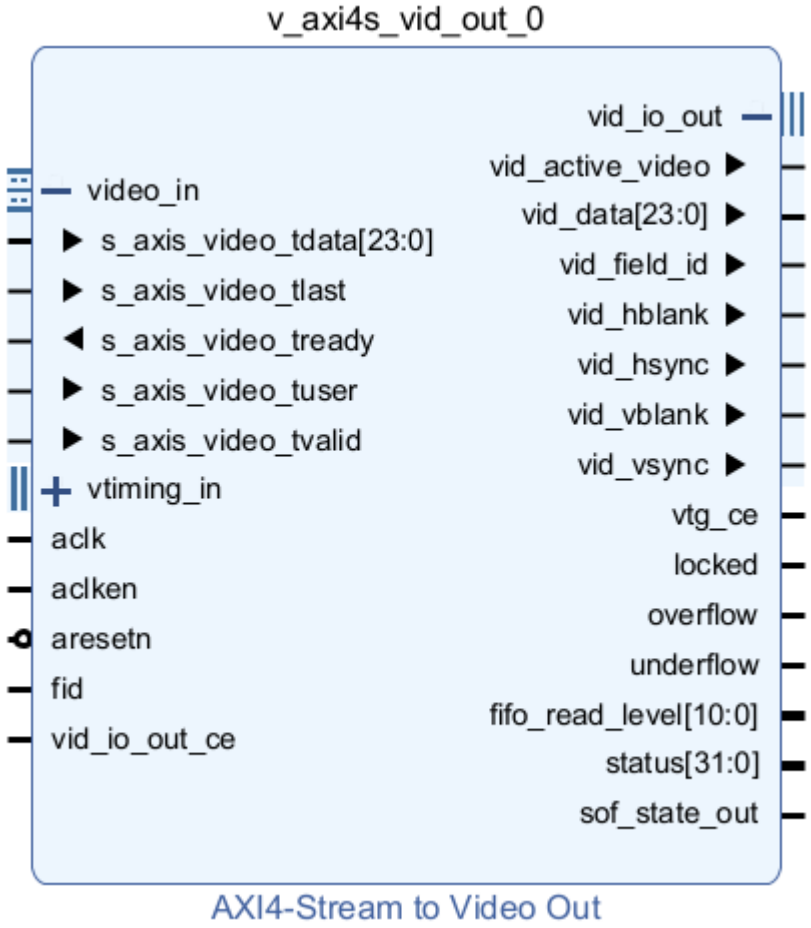


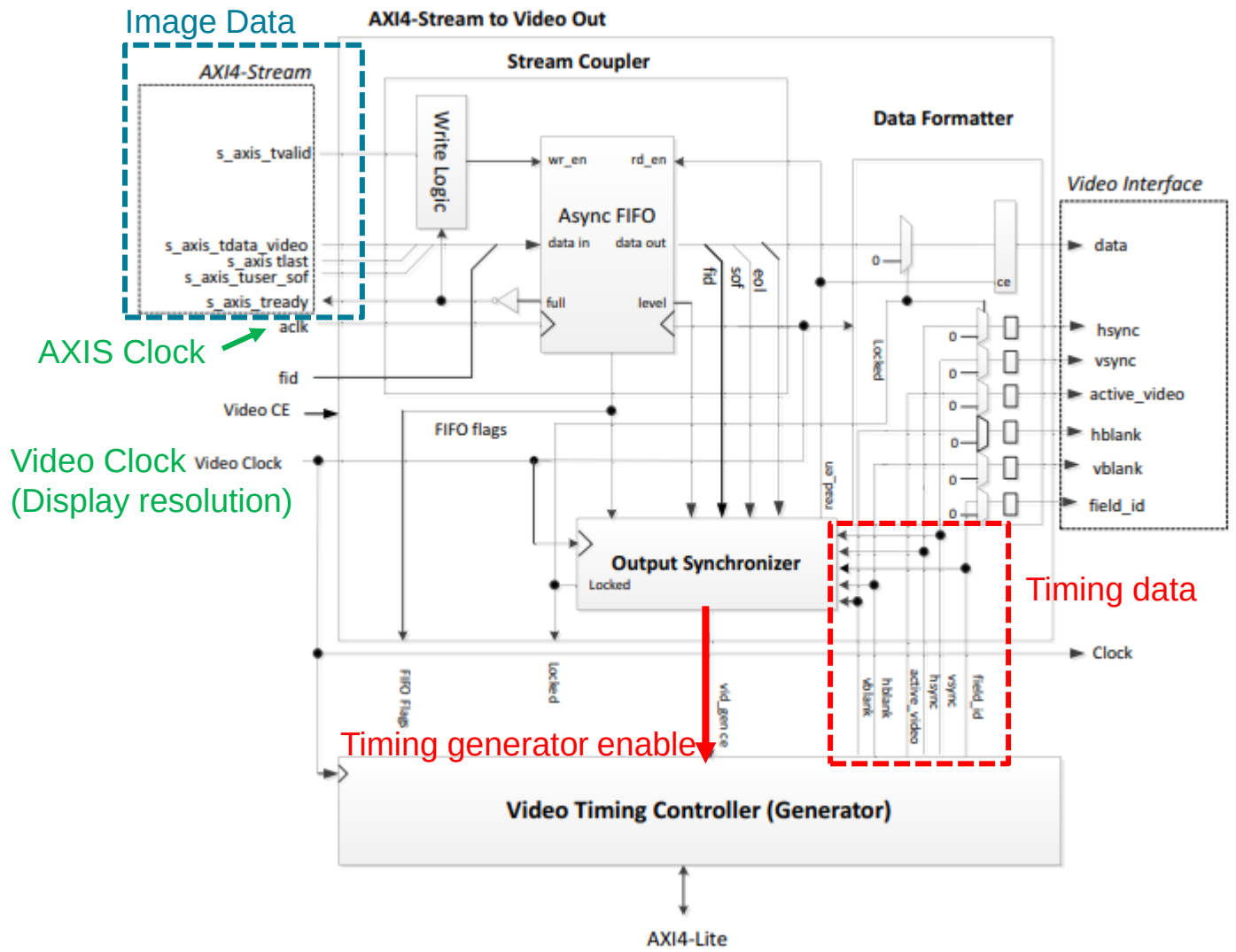


AXI Video Direct Memory Access(VDMA)

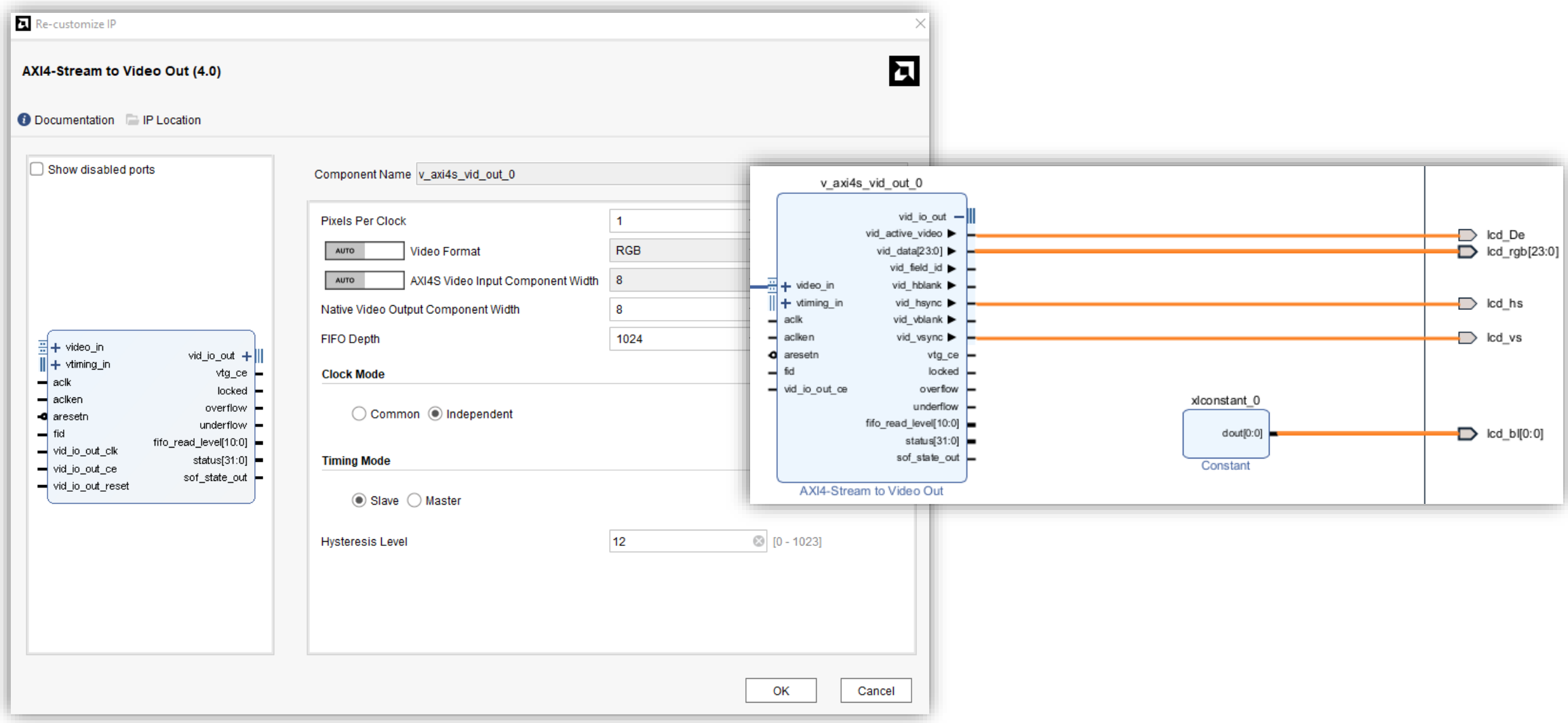


AXI Stream to Video





AXI Stream to Video



Video Timing Controller

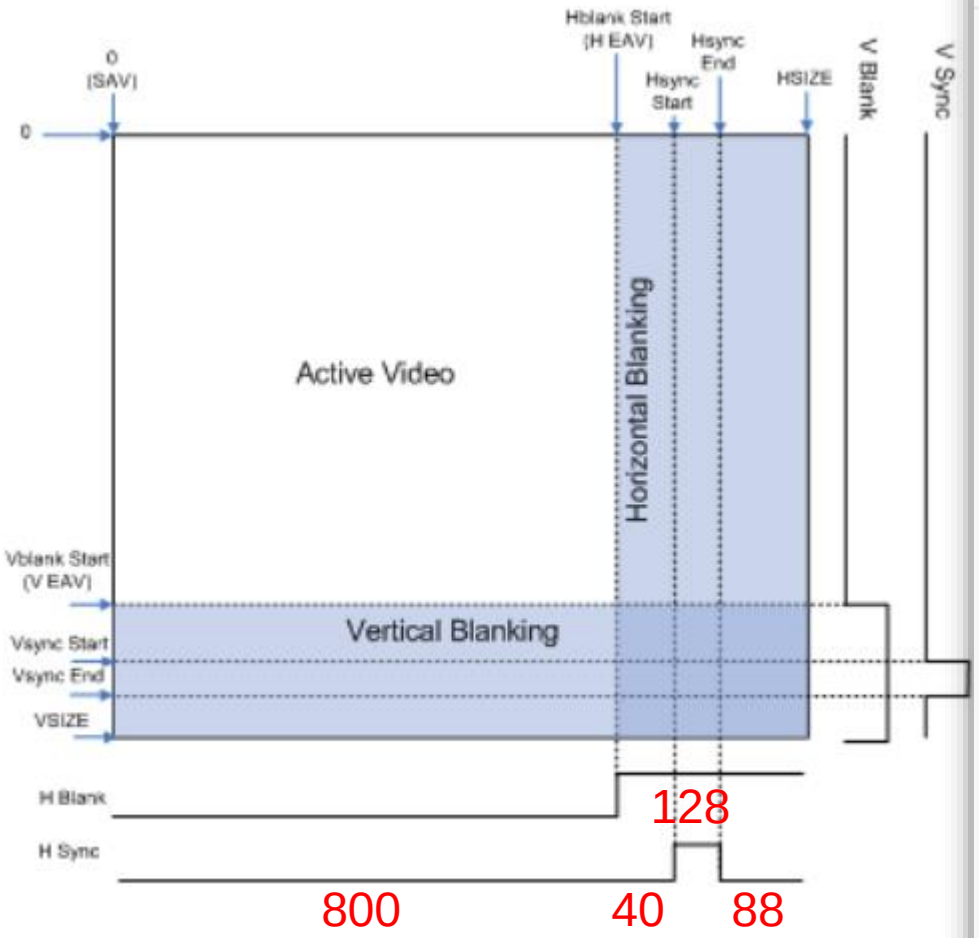
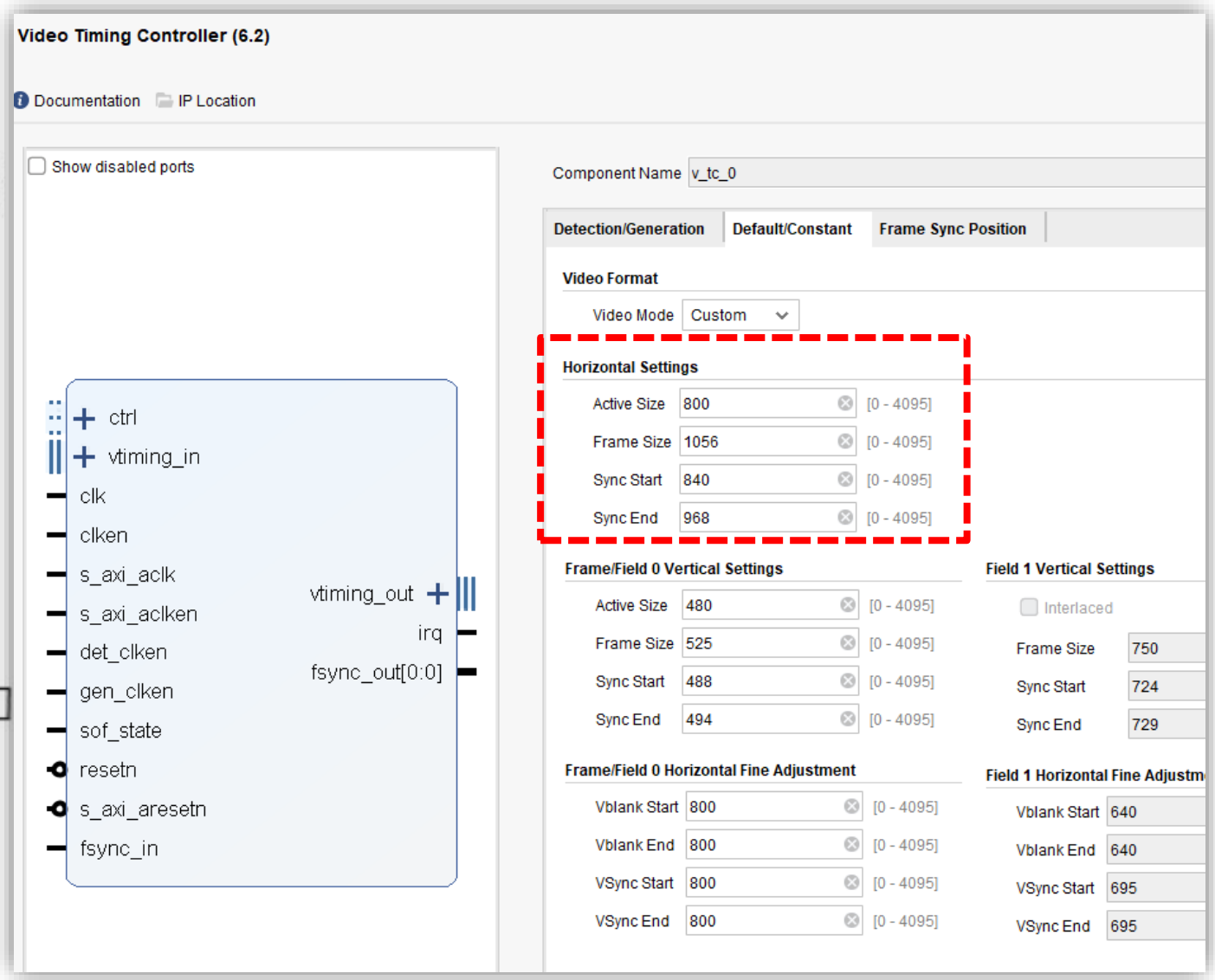
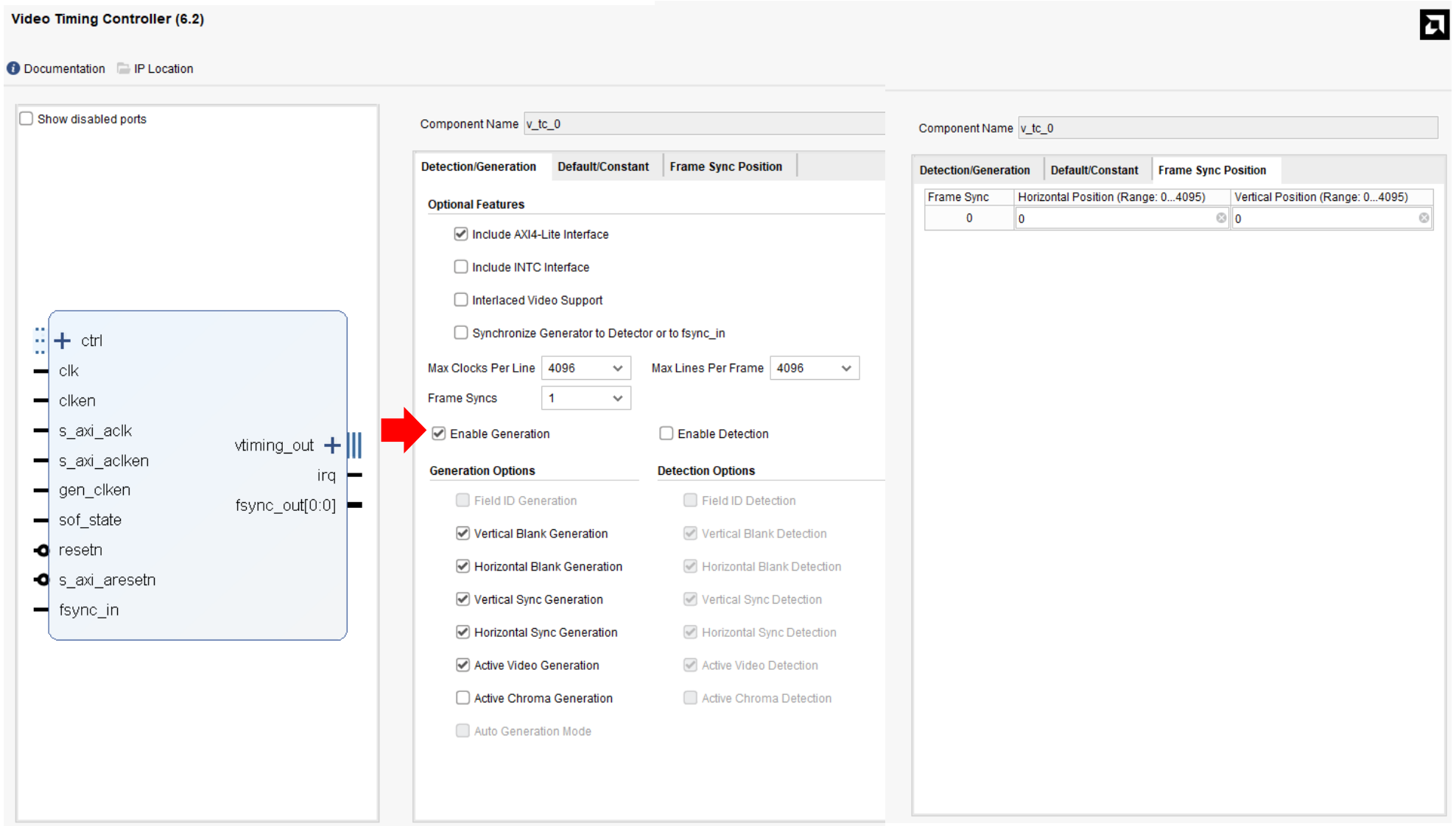


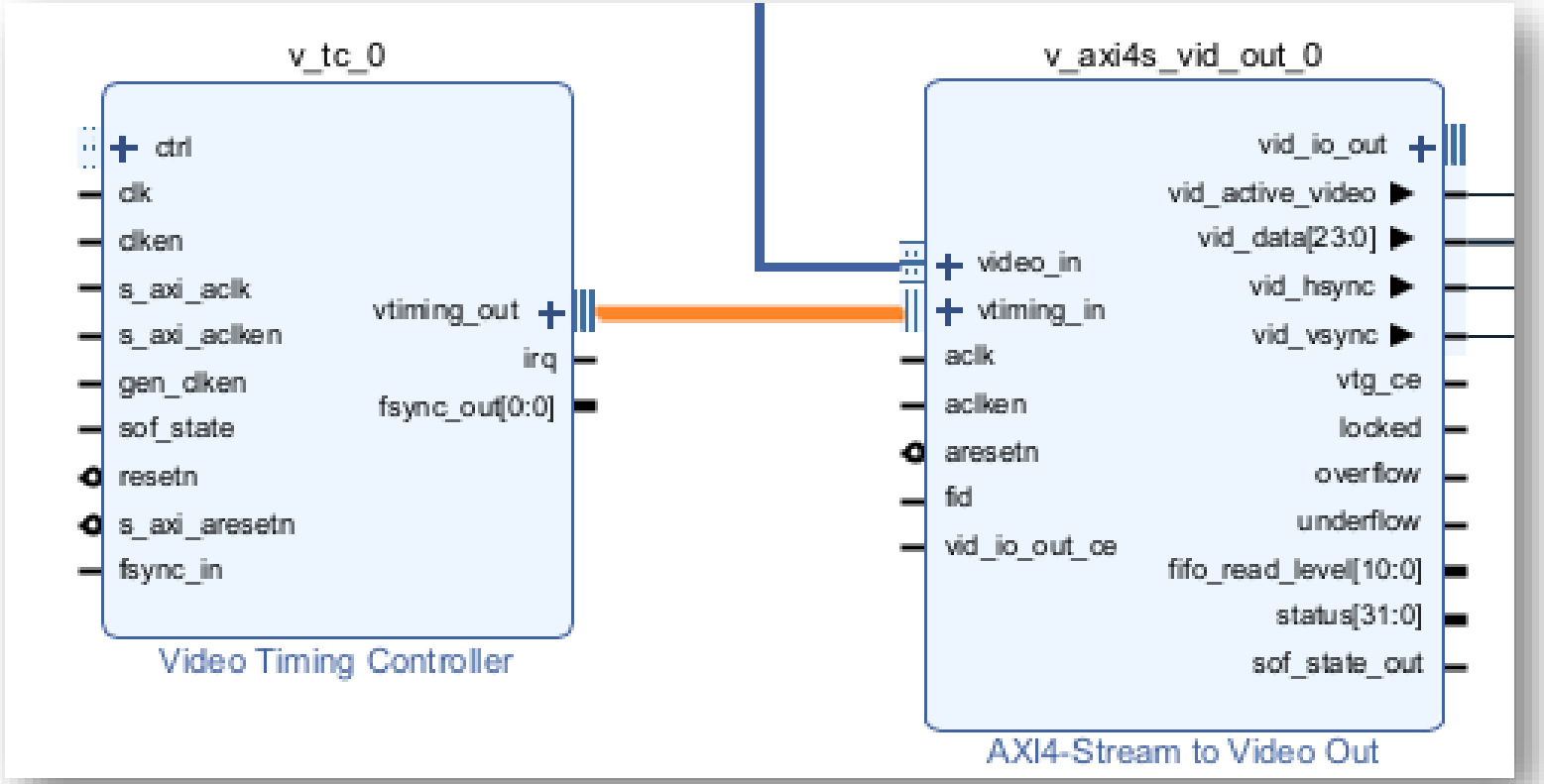
Figure 1-1: **Example Video Frame and Timing Signals**



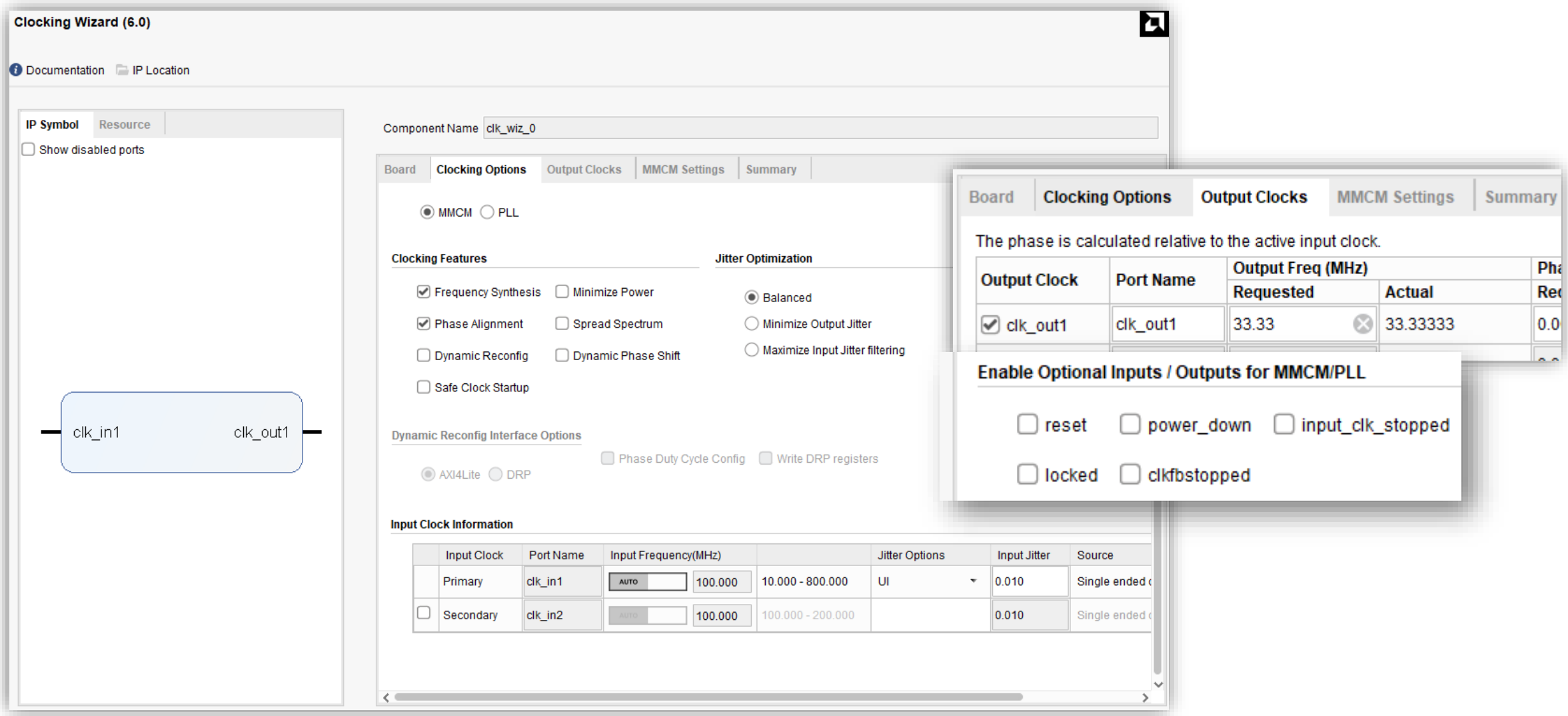
Video Timing Controller



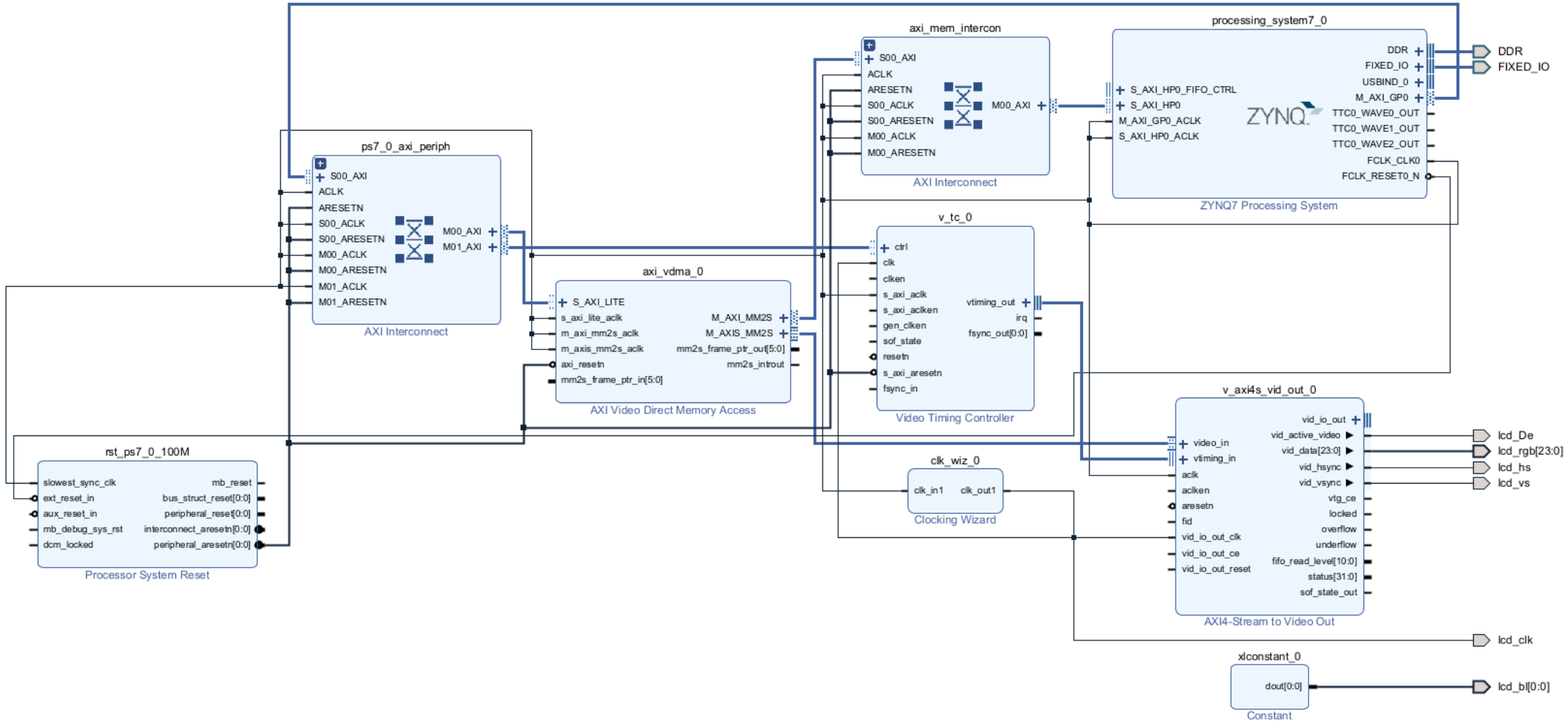
Video Timing Controller



Clocking Wizard



Final Block Design



Final Block Design