



Zynq® UltraScale+™ RFSoC Example Design: ZCU208

DDS Compiler for DAC and
System ILA for ADC Capture



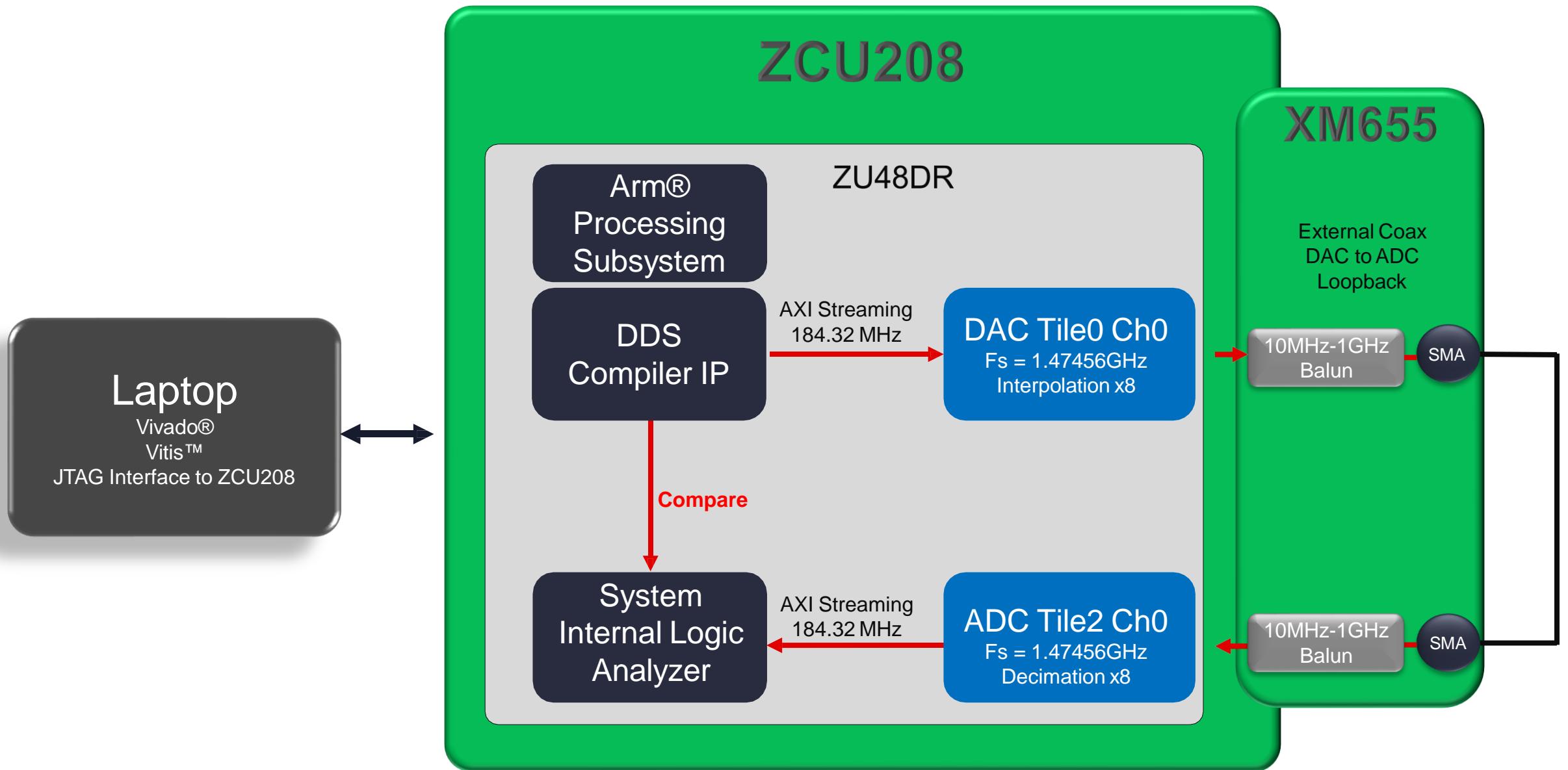
Agenda

- ▶ This is an example starter design for the RFSoC.
- ▶ Demo Block Diagram
- ▶ Implement
- ▶ Run Design
- ▶ DDS Compiler
- ▶ Data Converter
- ▶ Addition



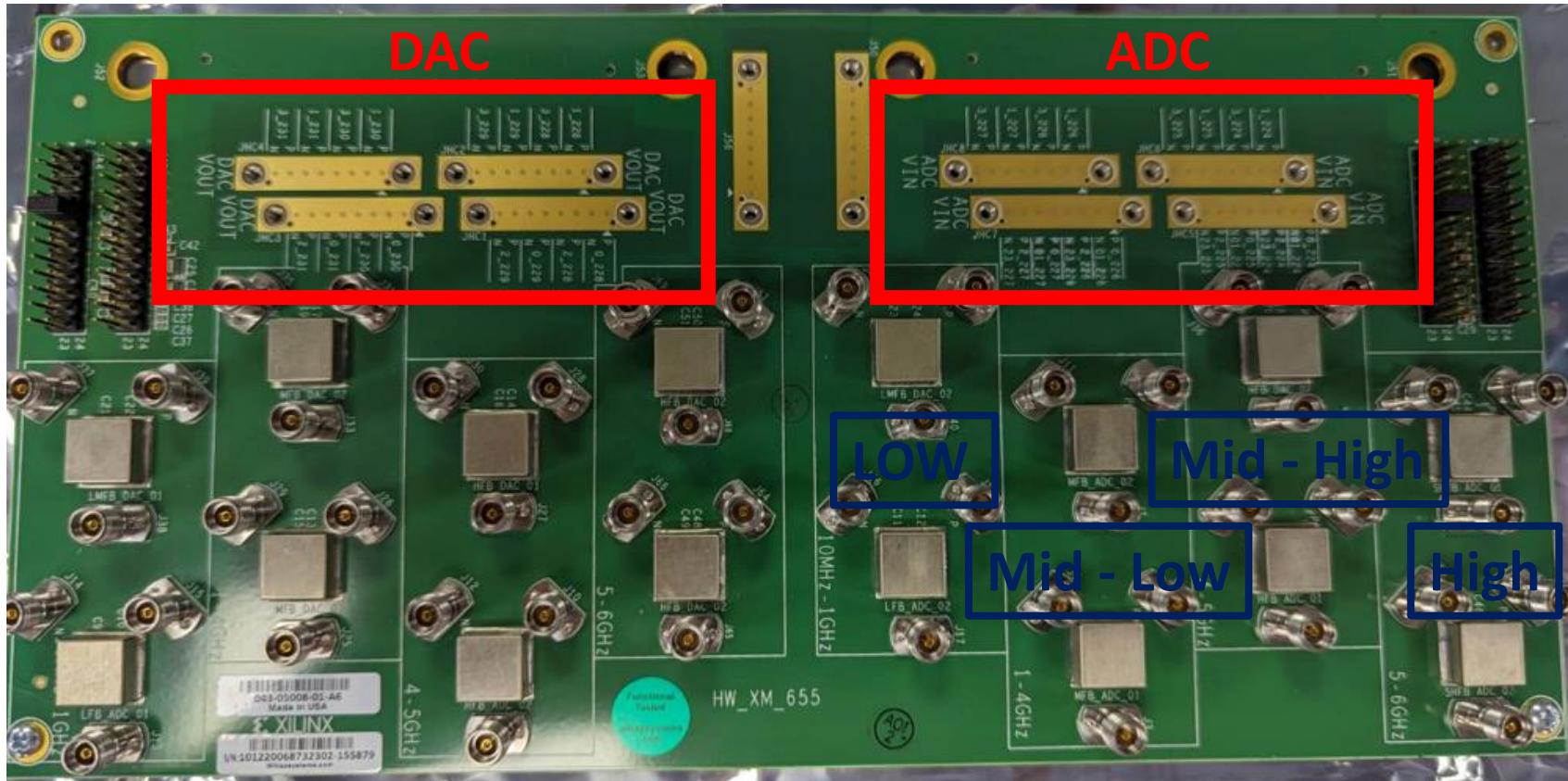
Demo Block Diagram

Demo Block Diagram



XM655

KEY



LOW

10MHz – 1GHz

Mid-Low

1GHz – 4GHz

Mid-High

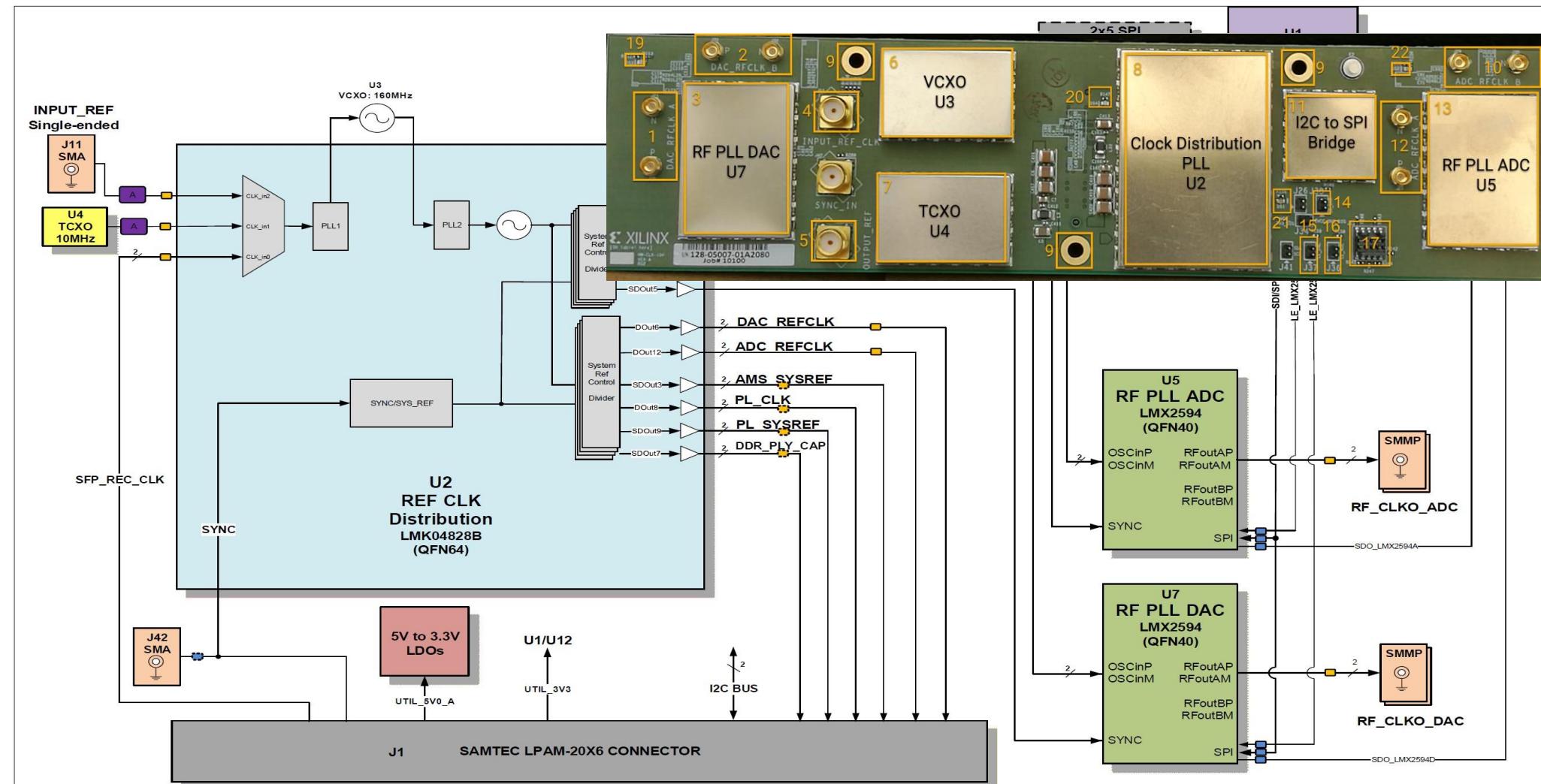
4GHz – 5GHz

High

5GHz – 6GHz

CLK104 RF Clock Block Diagram

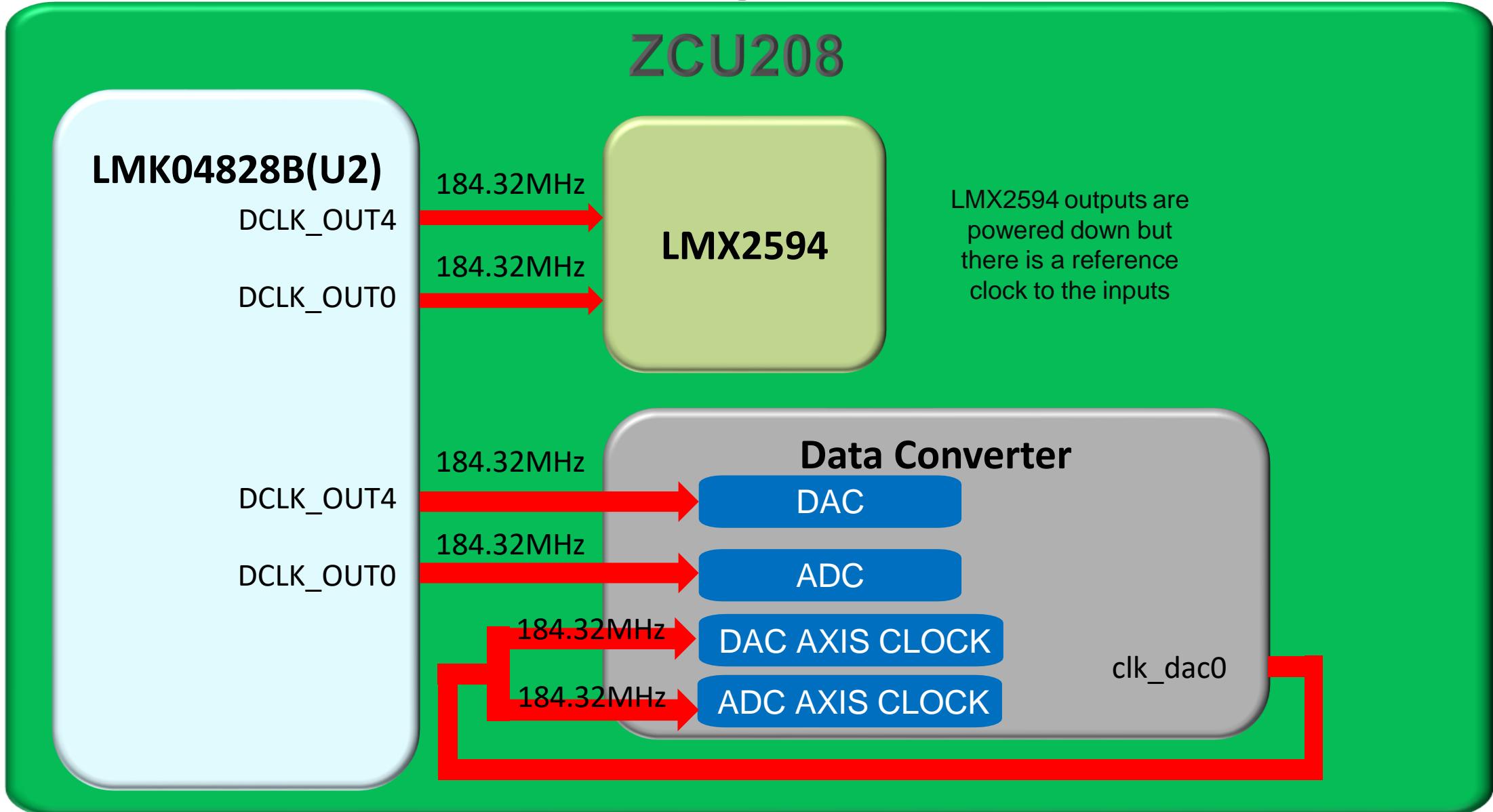
Block Diagram



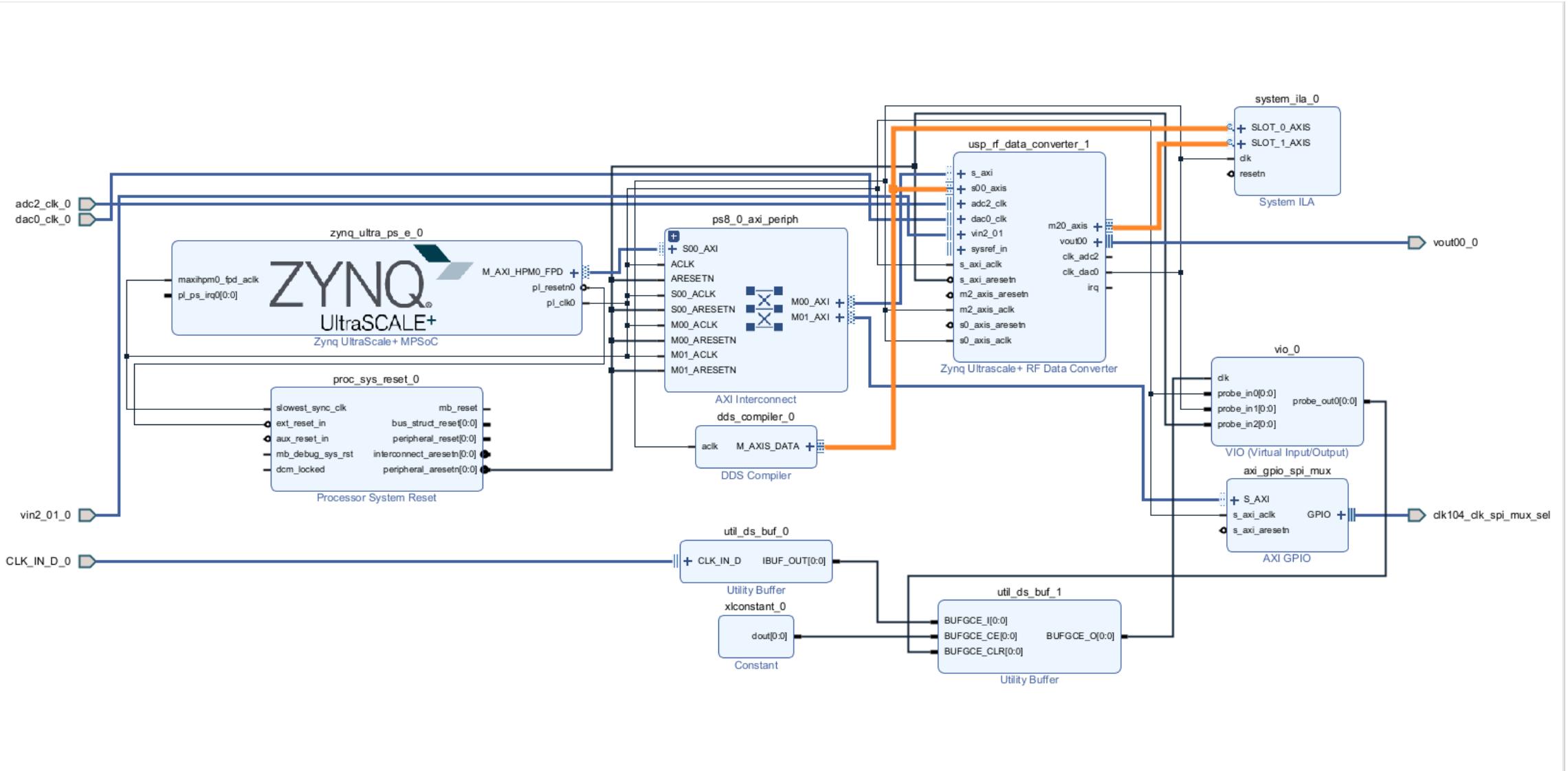
Only the LMK04828B is used for this design; the LMX2594 outputs are powered down.

Clocking is configured via an I2C to SPI bridge.

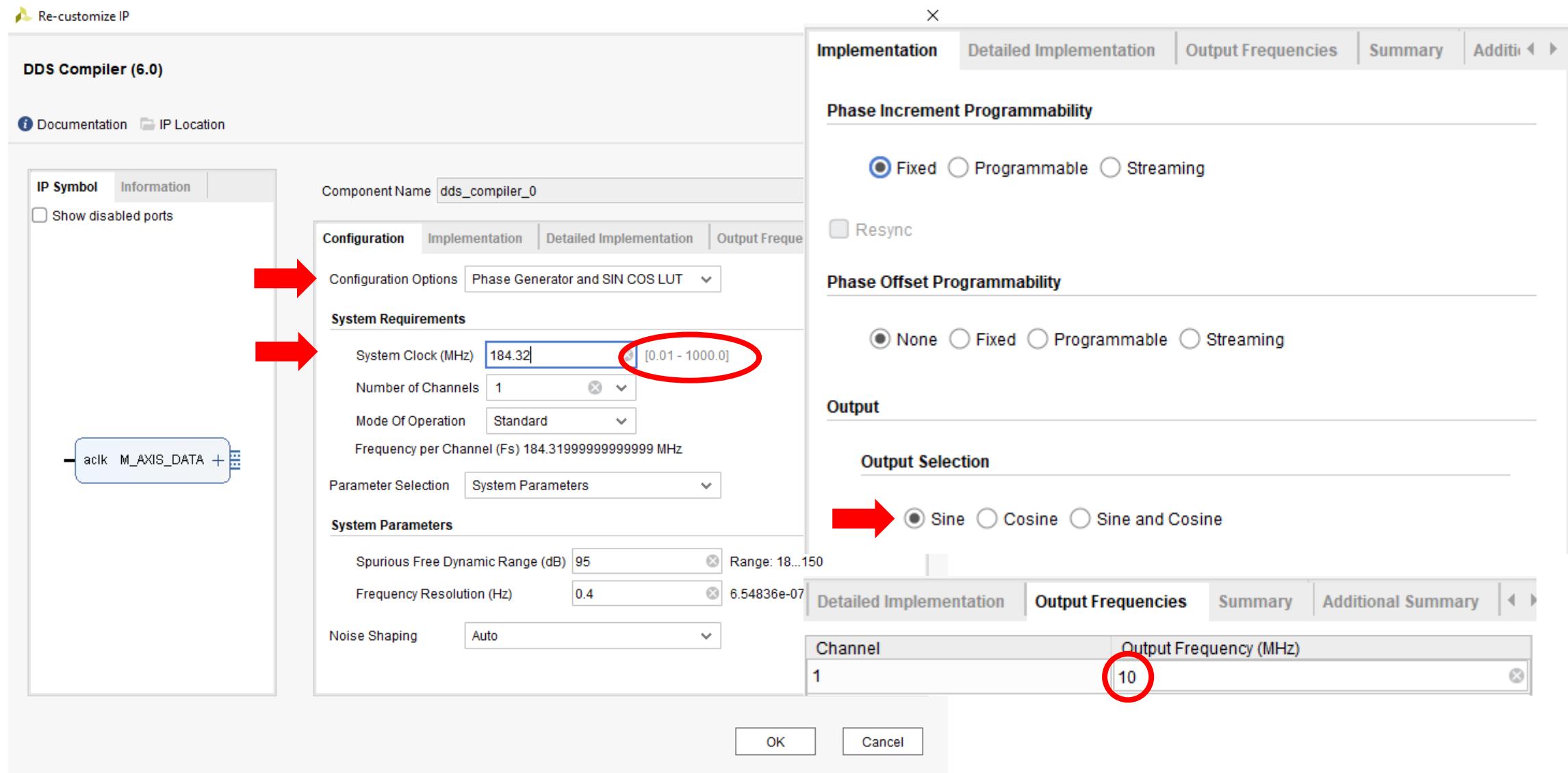
CLK104 RF Clock Block Diagram



Block Design



DDS Compiler Setting



Data Converter Setting

Basic System Clocking Advanced

RF-ADC RF-DAC

DAC Tile 228 DAC Tile 229 DAC Tile 230 DAC Tile 231

Multi Tile Sync Coupling Mode

Enable Multi Tile Sync Link Coupling: AC

Converter Band Mode Variable Output Current

Band: Single Output Power: 20.0

Converter Configuration

DAC 0 DAC 1

Enable DAC

DUC Configuration

DUC 0

Invert Q Output Inverse Sinc Filter

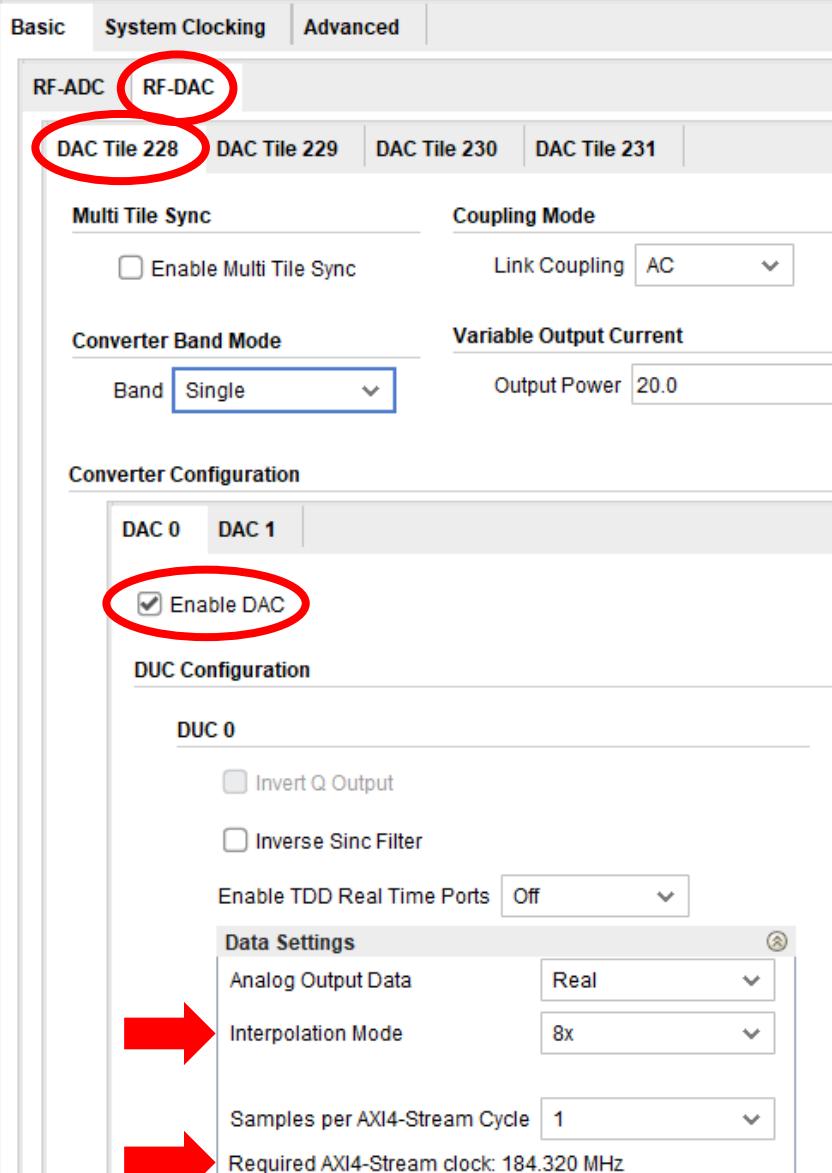
Enable TDD Real Time Ports: Off

Data Settings

Analog Output Data: Real Interpolation Mode: 8x

Samples per AXI4-Stream Cycle: 1

Required AXI4-Stream clock: 184.320 MHz



Basic System Clocking Advanced

RF-ADC RF-DAC

ADC Tile 224 ADC Tile 225 ADC Tile 226 ADC Tile 227

Multi Tile Sync Converter Band Mode

Enable Multi Tile Sync Band: Single

Converter Configuration

ADC 0

Enable ADC Invert Q Output

Dither

Enable TDD Real Time Ports: Off

Data Settings

Digital Output Data: Real Decimation Mode: 8x

Samples per AXI4-Stream Cycle: 1

Required AXI4-Stream clock: 184.320 MHz

Observation Channel

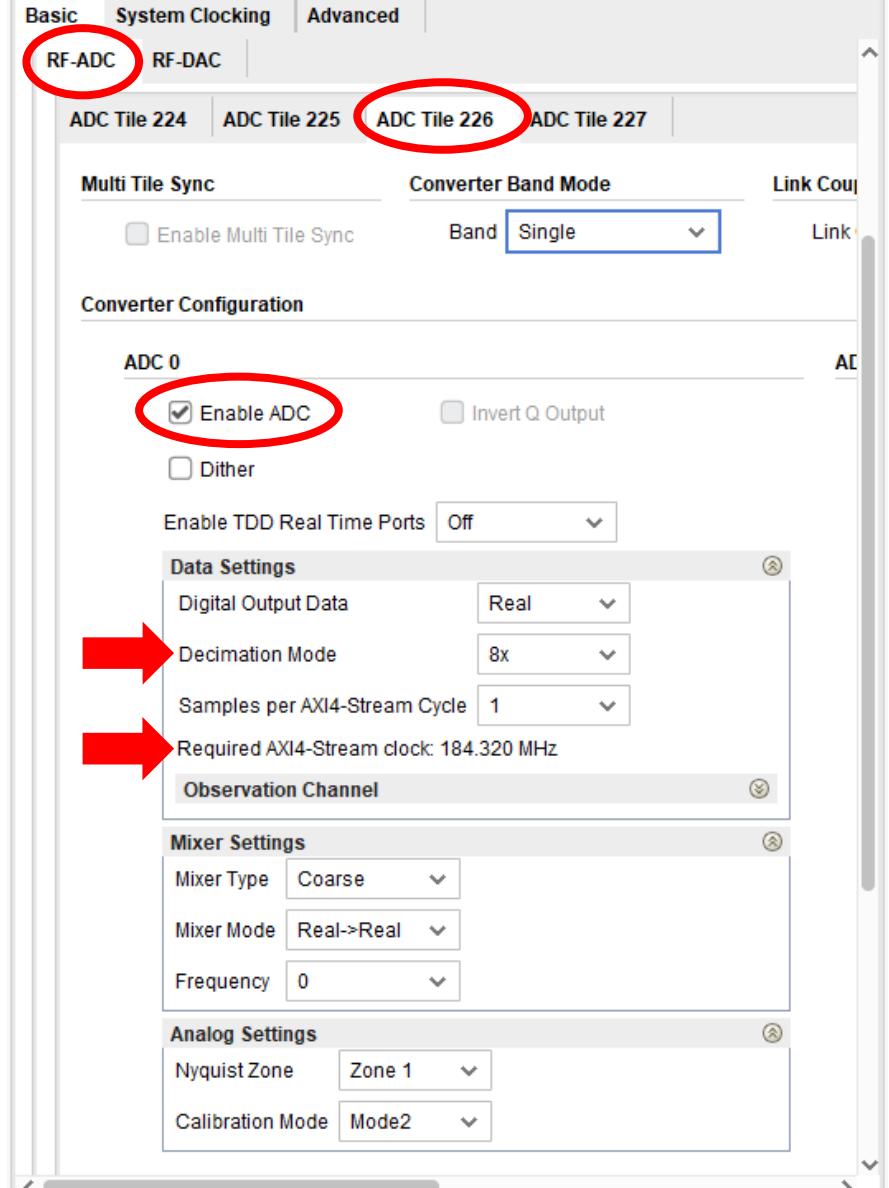
Mixer Settings

Mixer Type: Coarse Mixer Mode: Real->Real

Frequency: 0

Analog Settings

Nyquist Zone: Zone 1 Calibration Mode: Mode2



Data Converter Setting

Basic System Clocking Advanced

AXI4-Lite Interface Configuration

AXI4-Lite Clock (MHz) 

Tile Clocking Settings

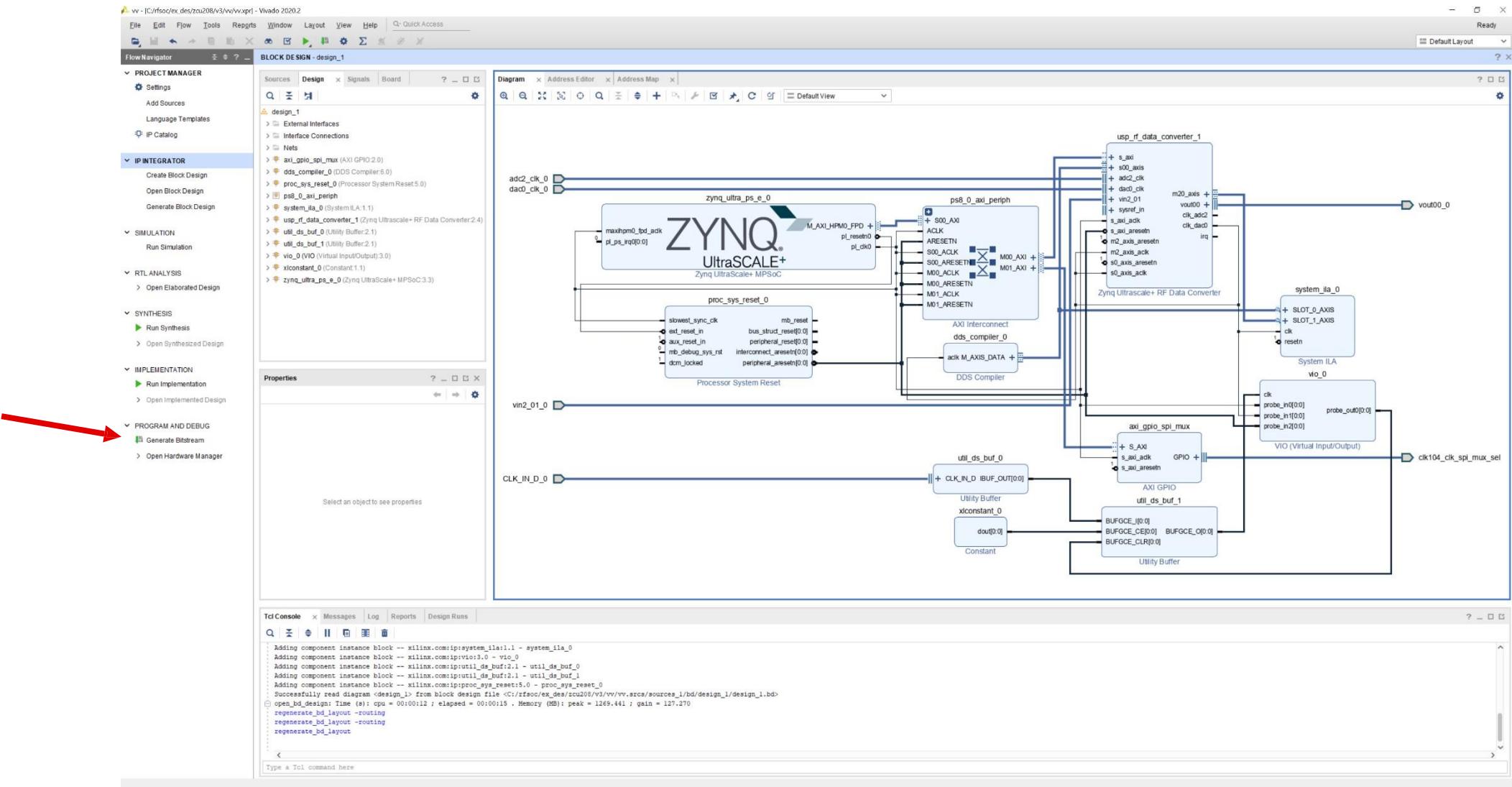
Tile	Sampling Rate (GSPS)	Max Fs (GSPS)	PLL	Reference Clock (MHz)	PLL Ref Clock (MHz)	Ref Clock Divider	Fabric Clock (MHz)	Clock Out (MHz)	Clock Source	Distribute Clock
ADC 224	2.0	5.000	<input type="checkbox"/>	2000.000	-	1	0.0	15.625	Tile224	Off
ADC 225	2.0	5.000	<input type="checkbox"/>	2000.000	-	1	0.0	15.625	Tile225	Off
ADC 226	1.47456 	5.000	<input checked="" type="checkbox"/>	184.320	184.32	1	184.320	11.520	Tile226	Off
ADC 227	2.0	5.000	<input type="checkbox"/>	2000.000	-	1	0.0	15.625	Tile227	Off
DAC 228	1.47456 	7.000	<input checked="" type="checkbox"/>	184.320	184.32	1	184.320	184.320	Tile228	Off
DAC 229	6.4	10.000	<input type="checkbox"/>	6400.000	-	1	0.0	50.000	Tile229	Off
DAC 230	6.4	10.000	<input type="checkbox"/>	6400.000	-	1	0.0	50.000	Tile230	Off
DAC 231	6.4	10.000	<input type="checkbox"/>	6400.000	-	1	0.0	50.000	Tile231	Off



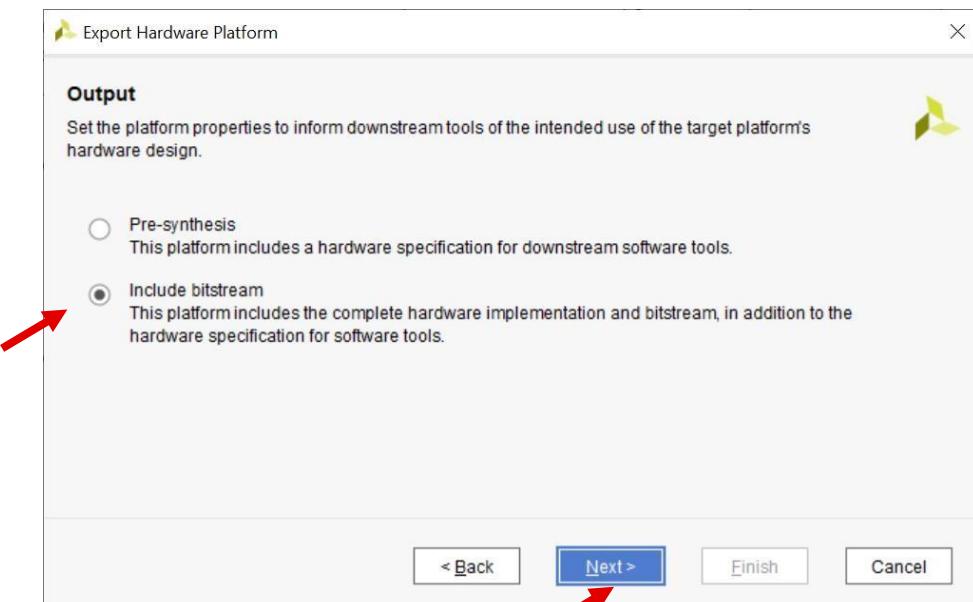
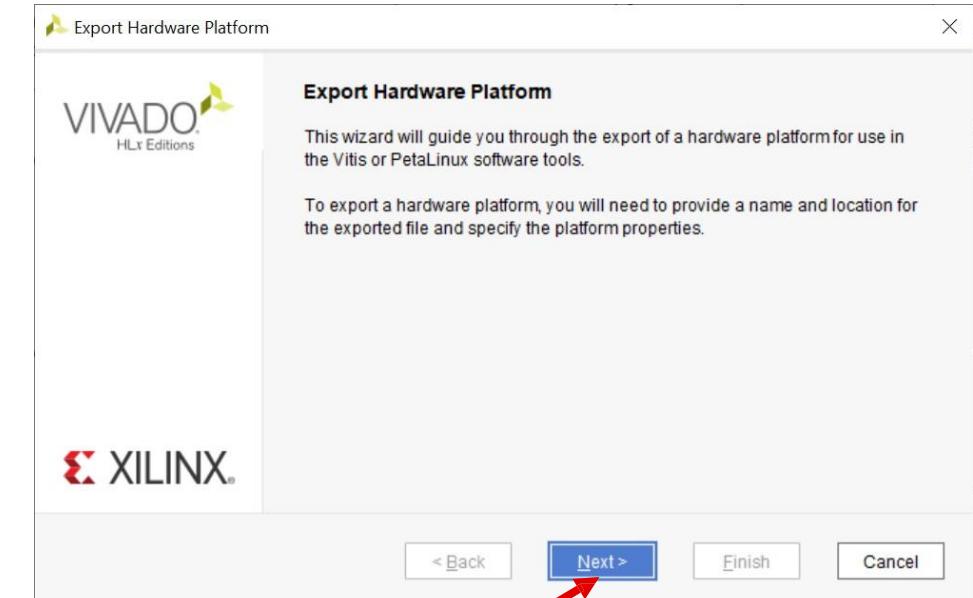
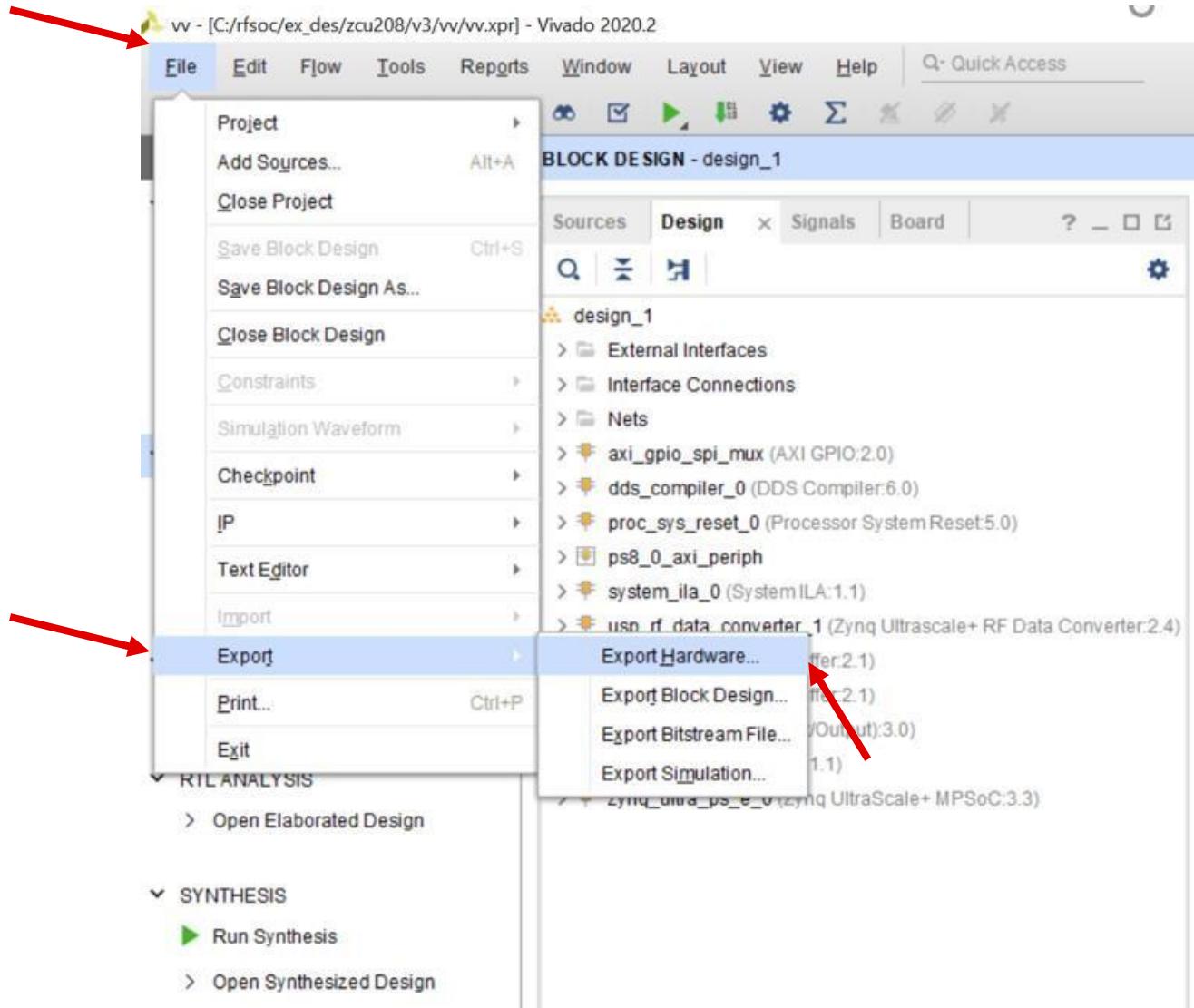


Implement

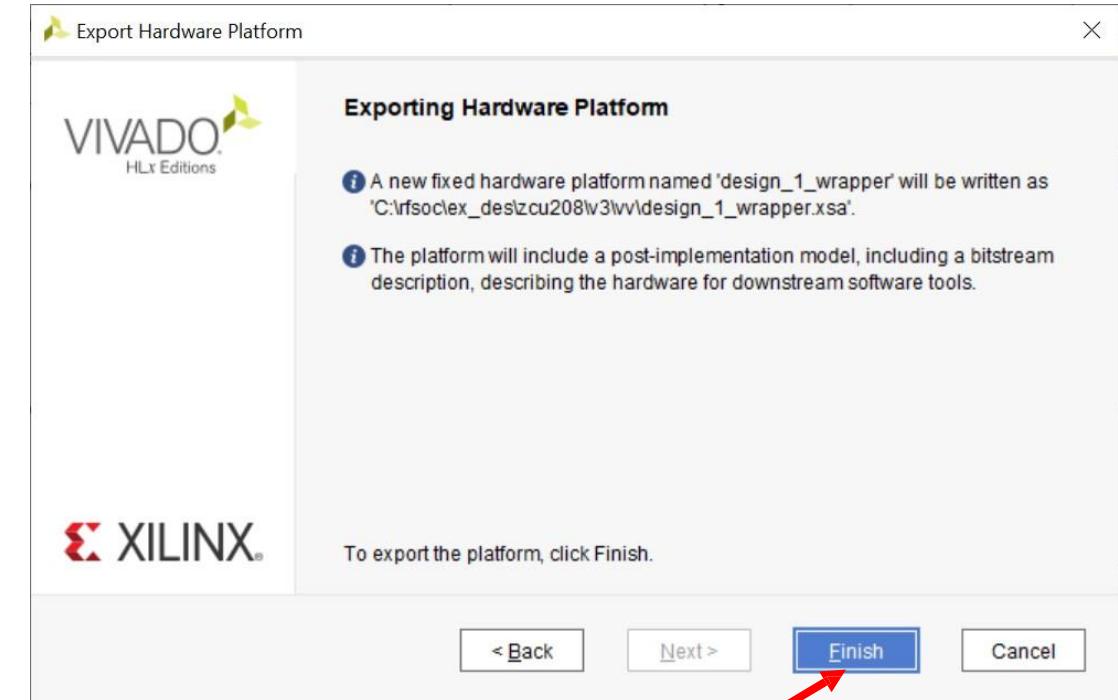
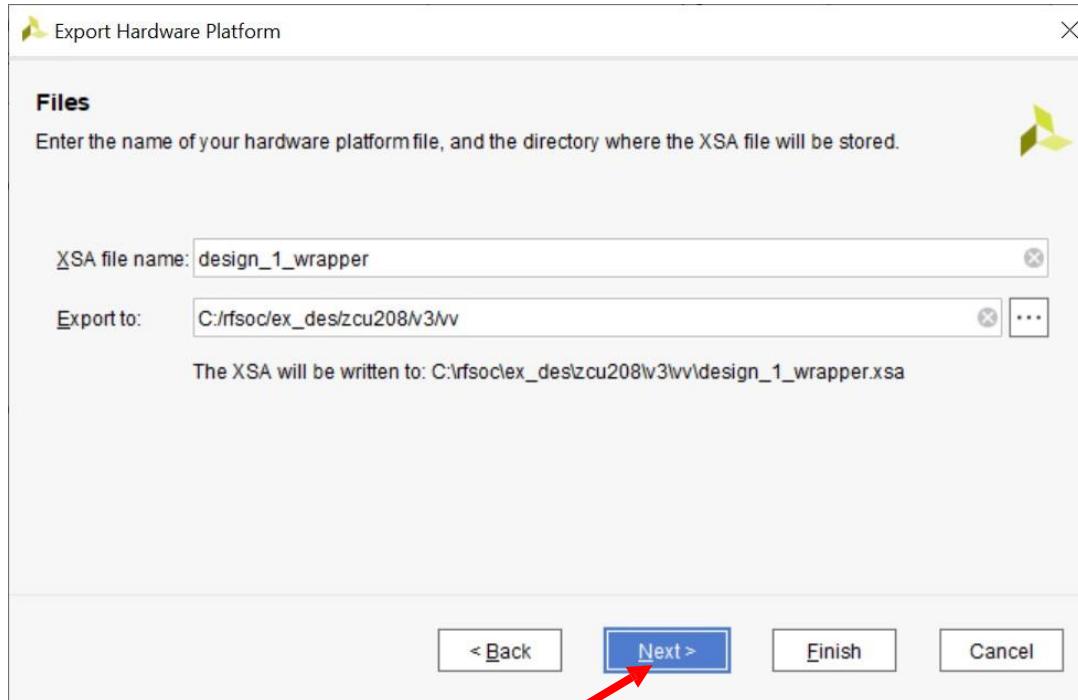
Open Hardware Design and Generate the Bitstream



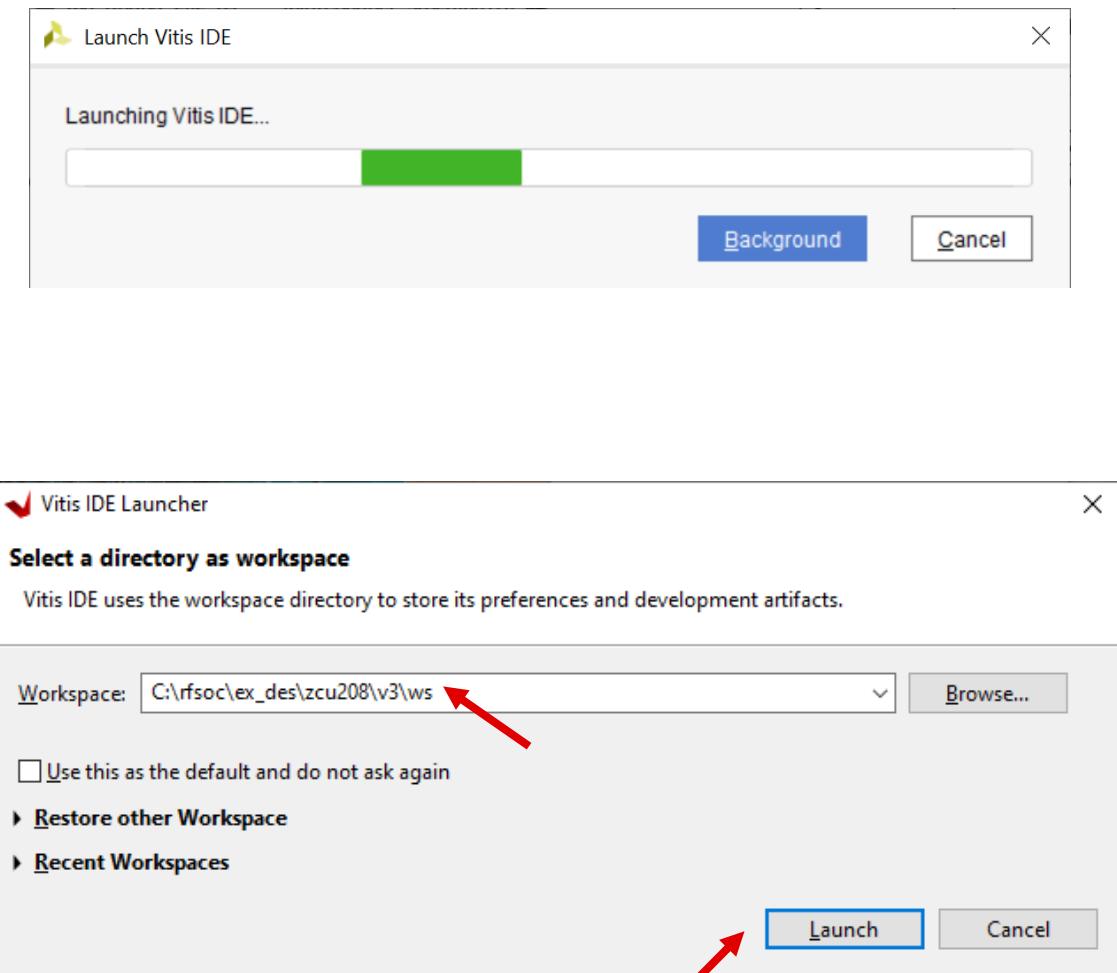
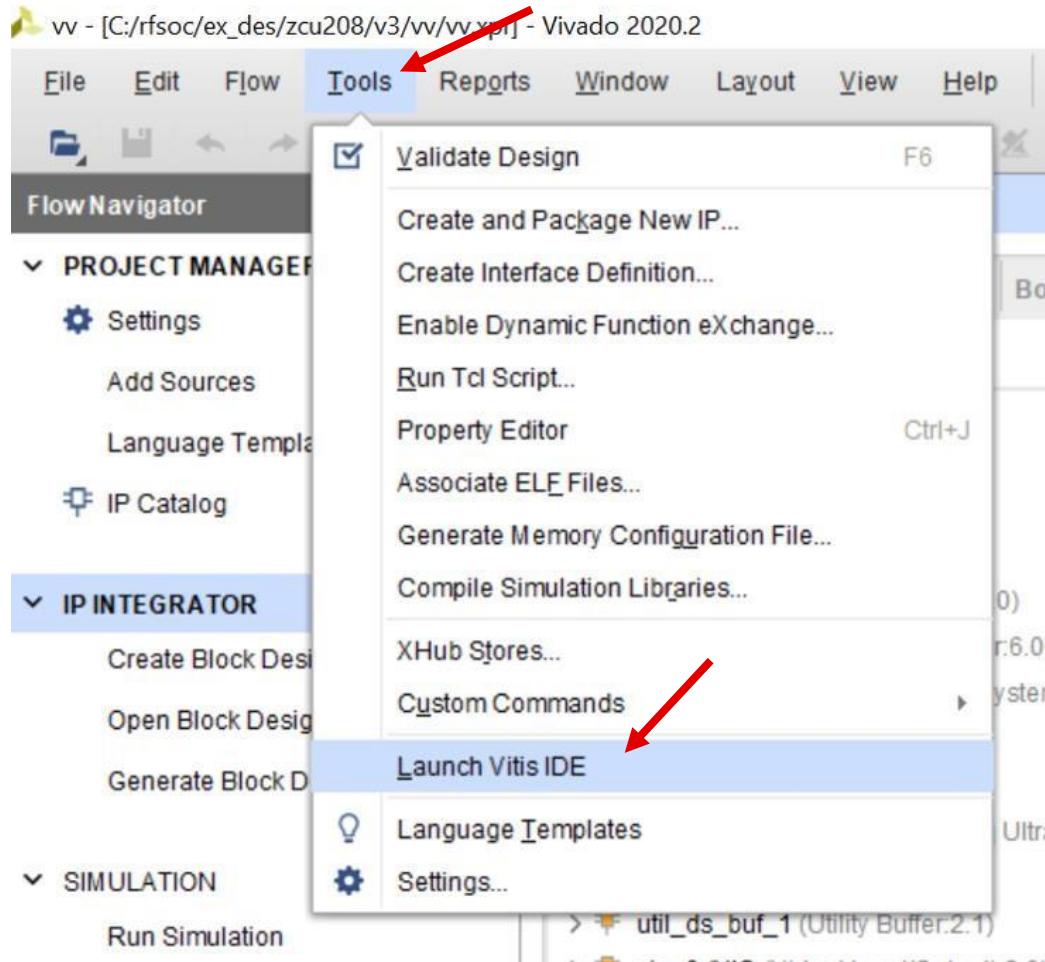
Export Hardware



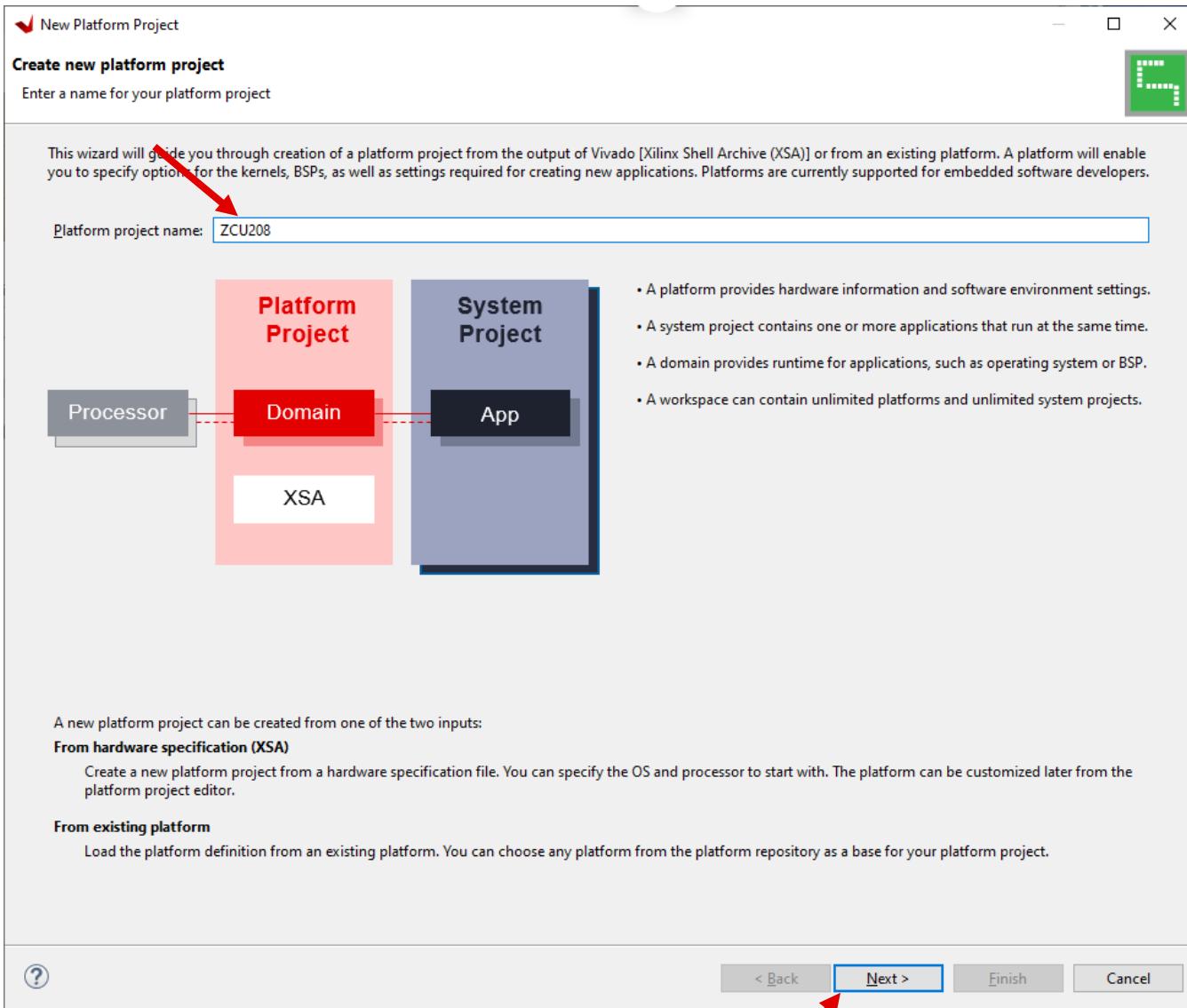
Export Hardware



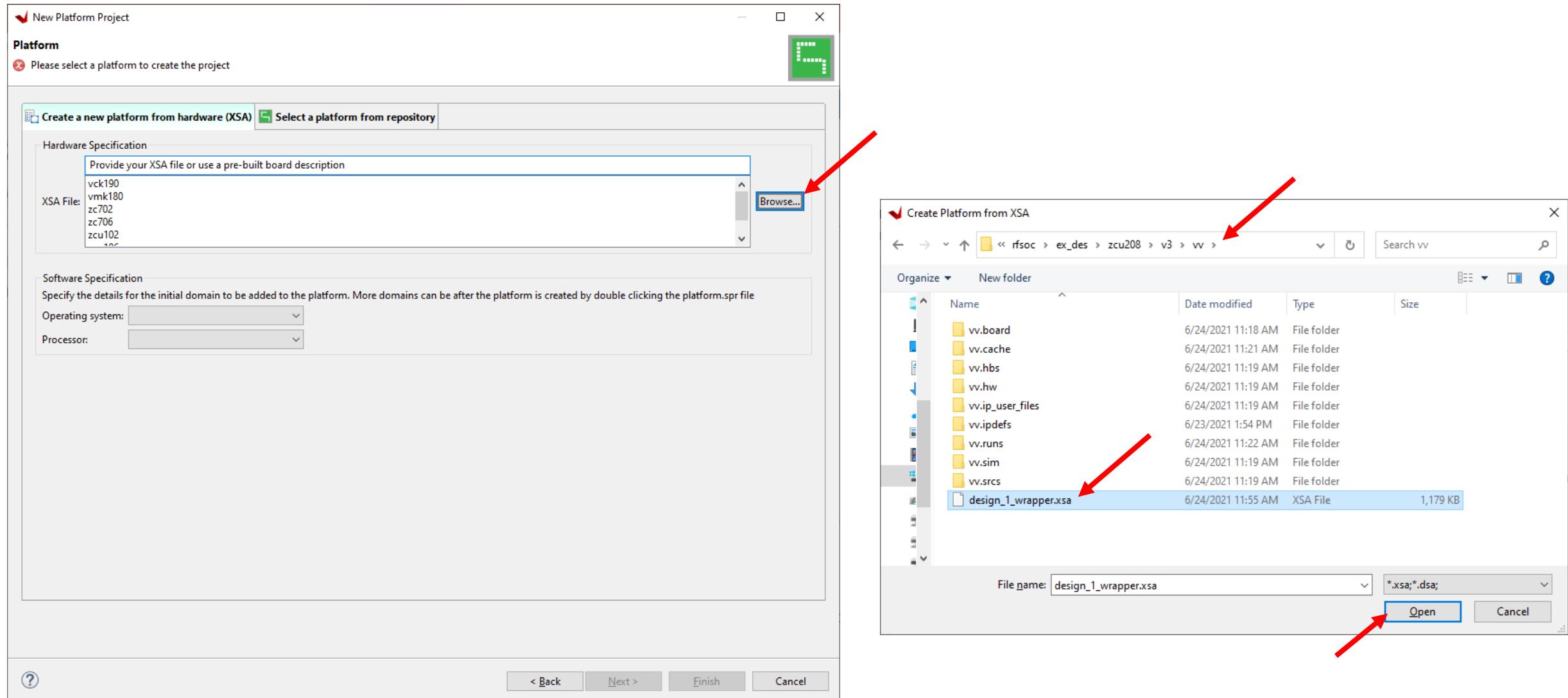
Open Vitis™ Software Platform



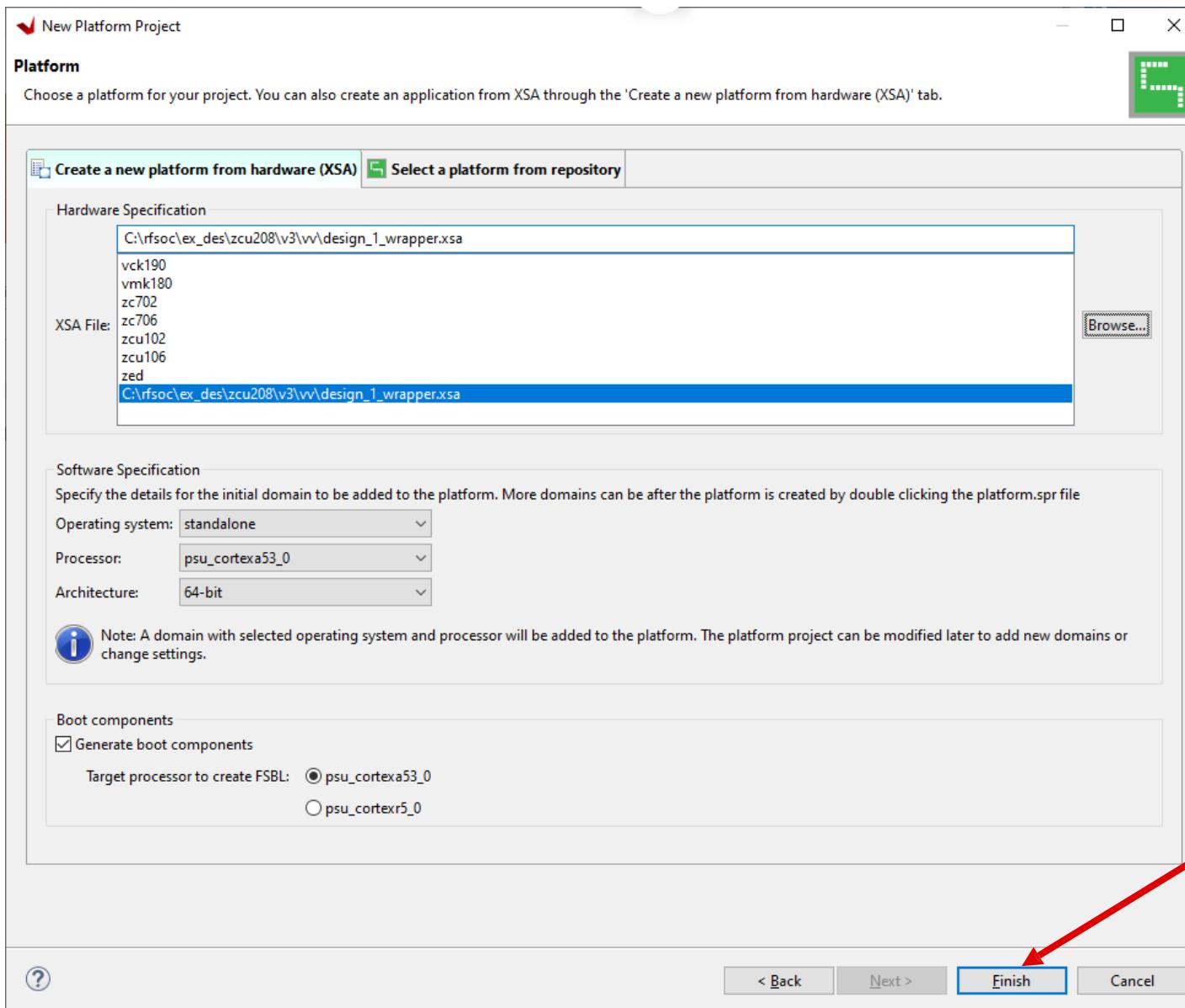
Create Platform Project Cont'd



Create Platform Project

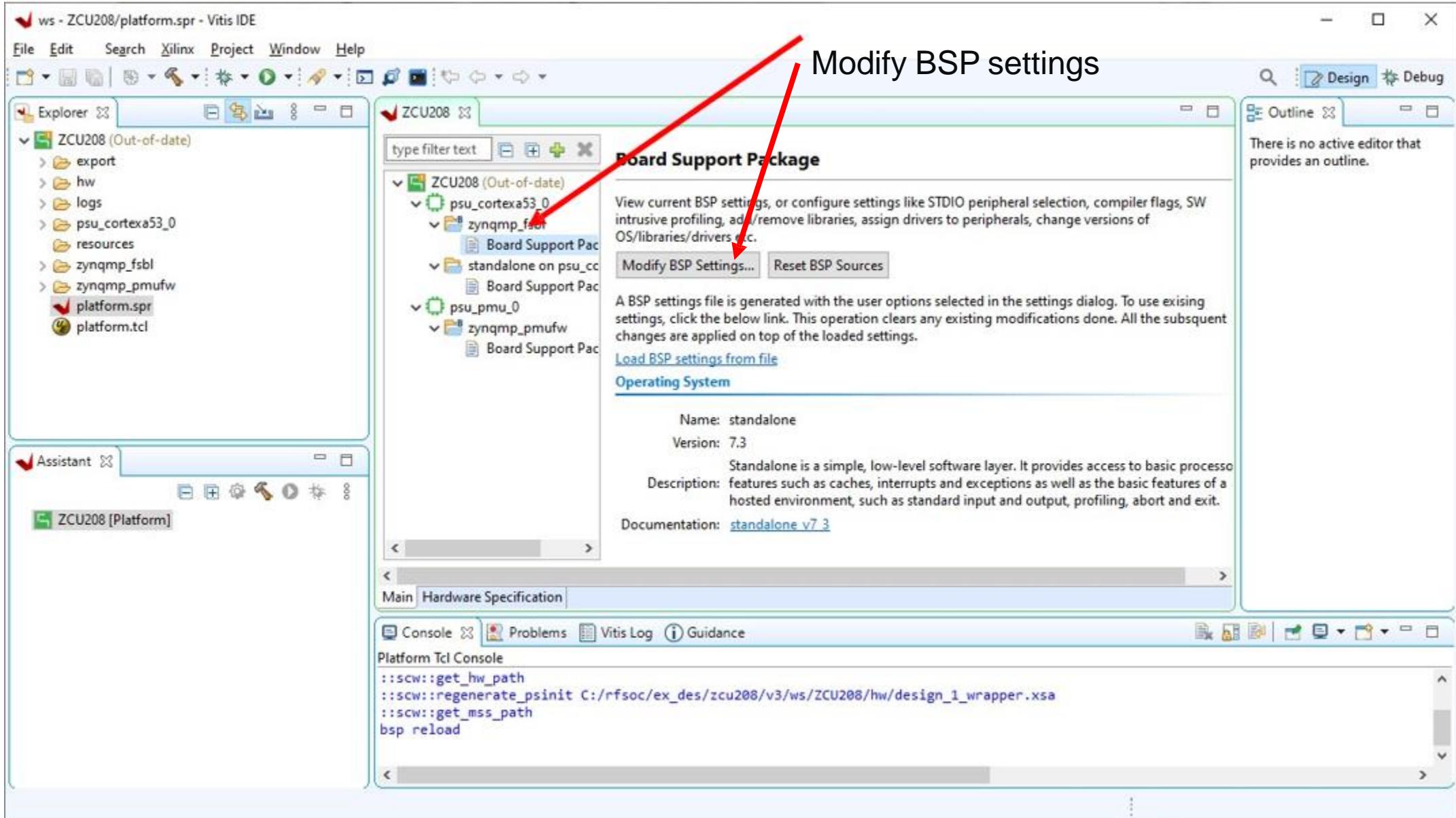


Create Platform Project Cont'd

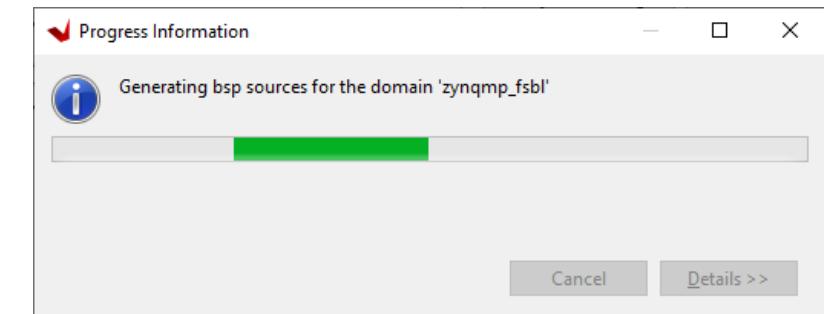
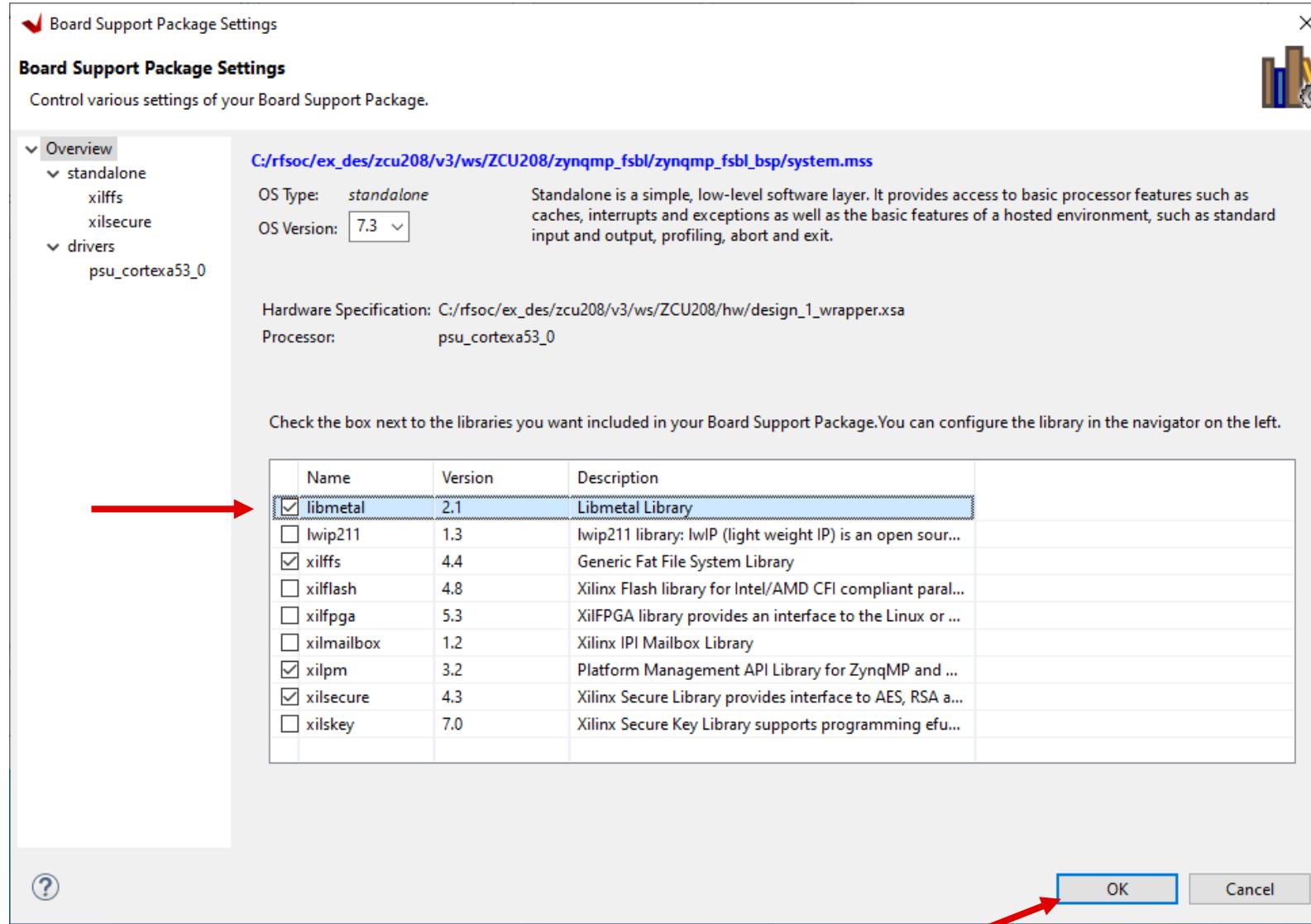


This may take
a few minutes.

Modify BSP settings

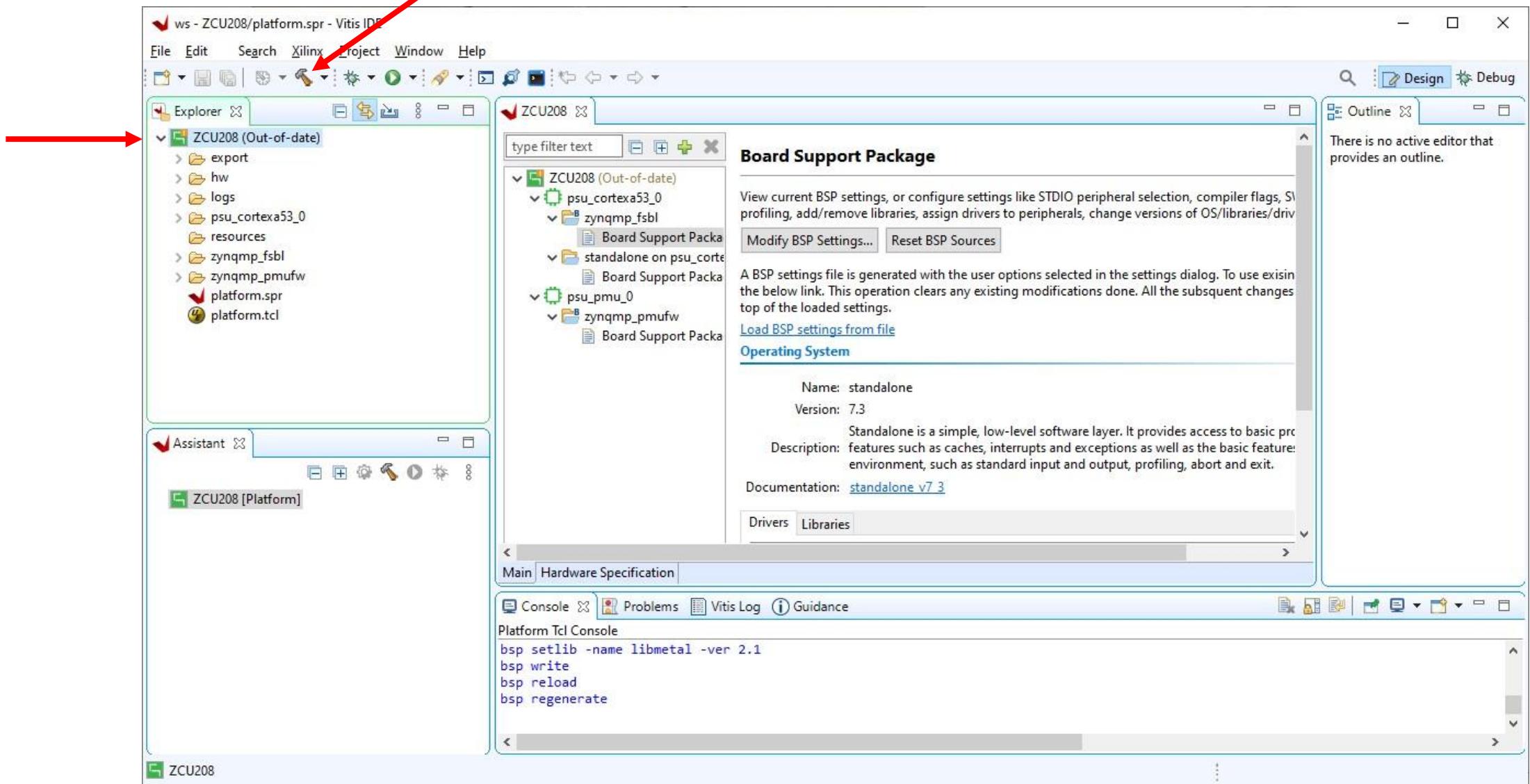


Enable libmetal

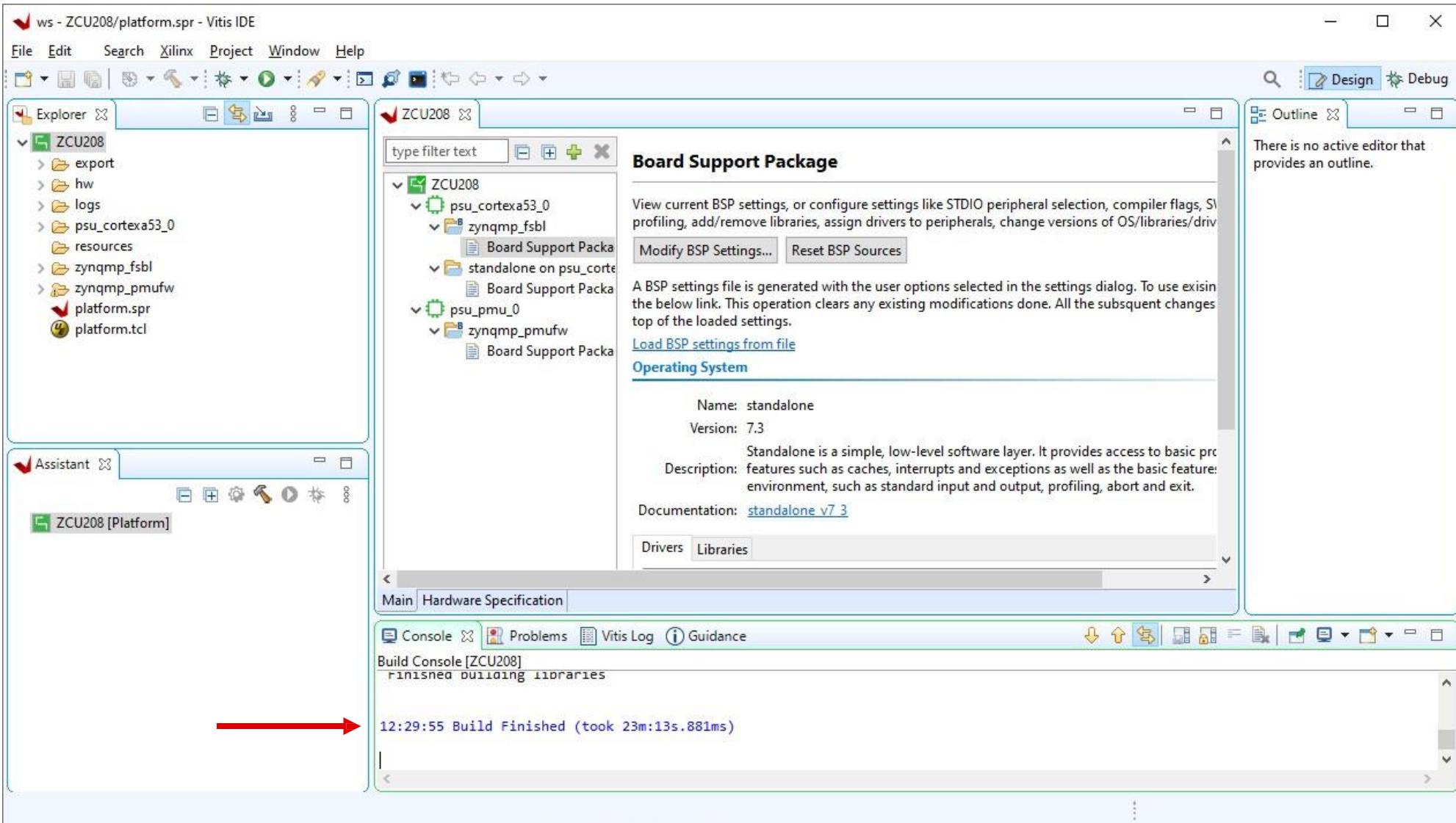


Build Project

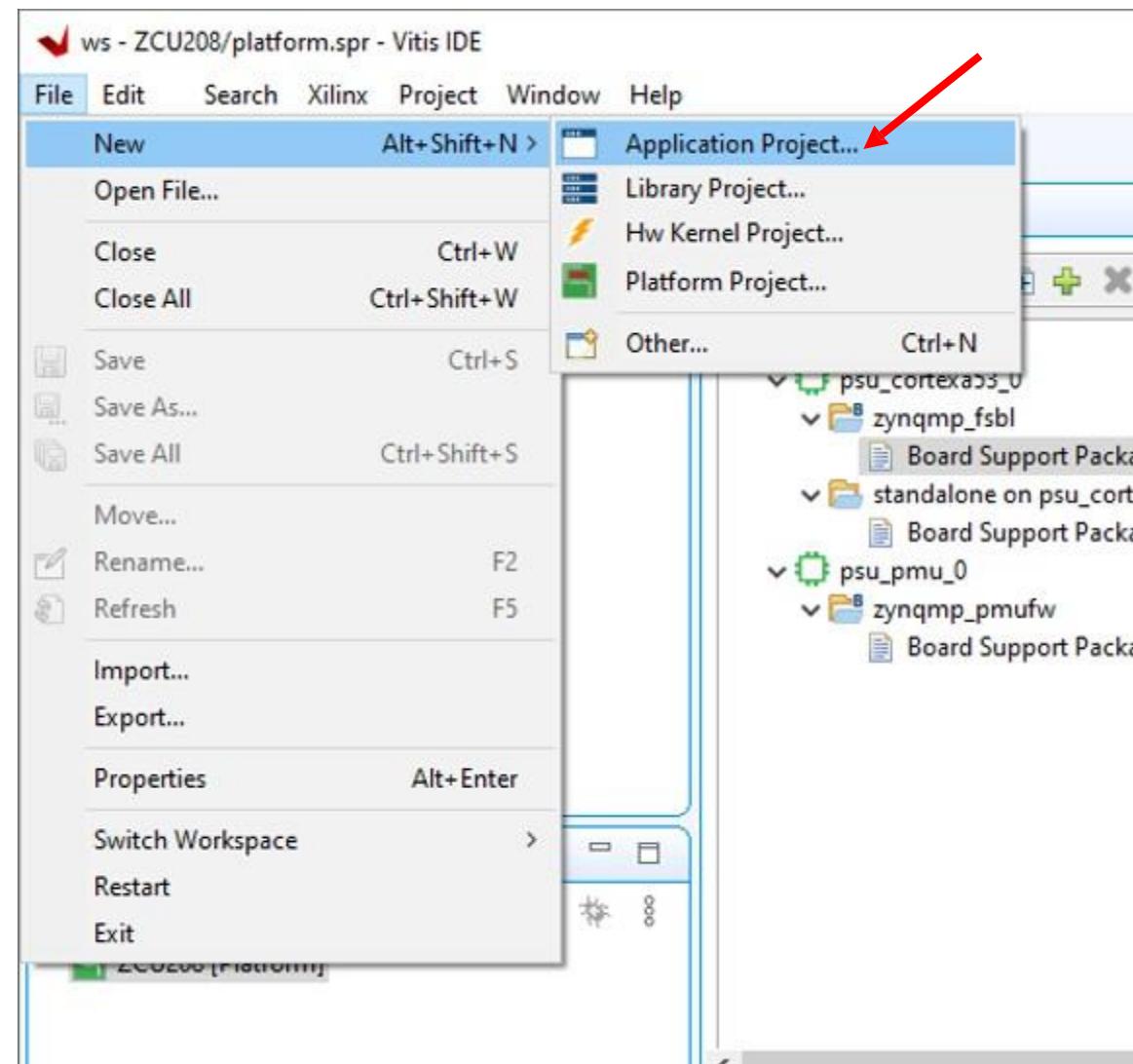
This may take
a few minutes.



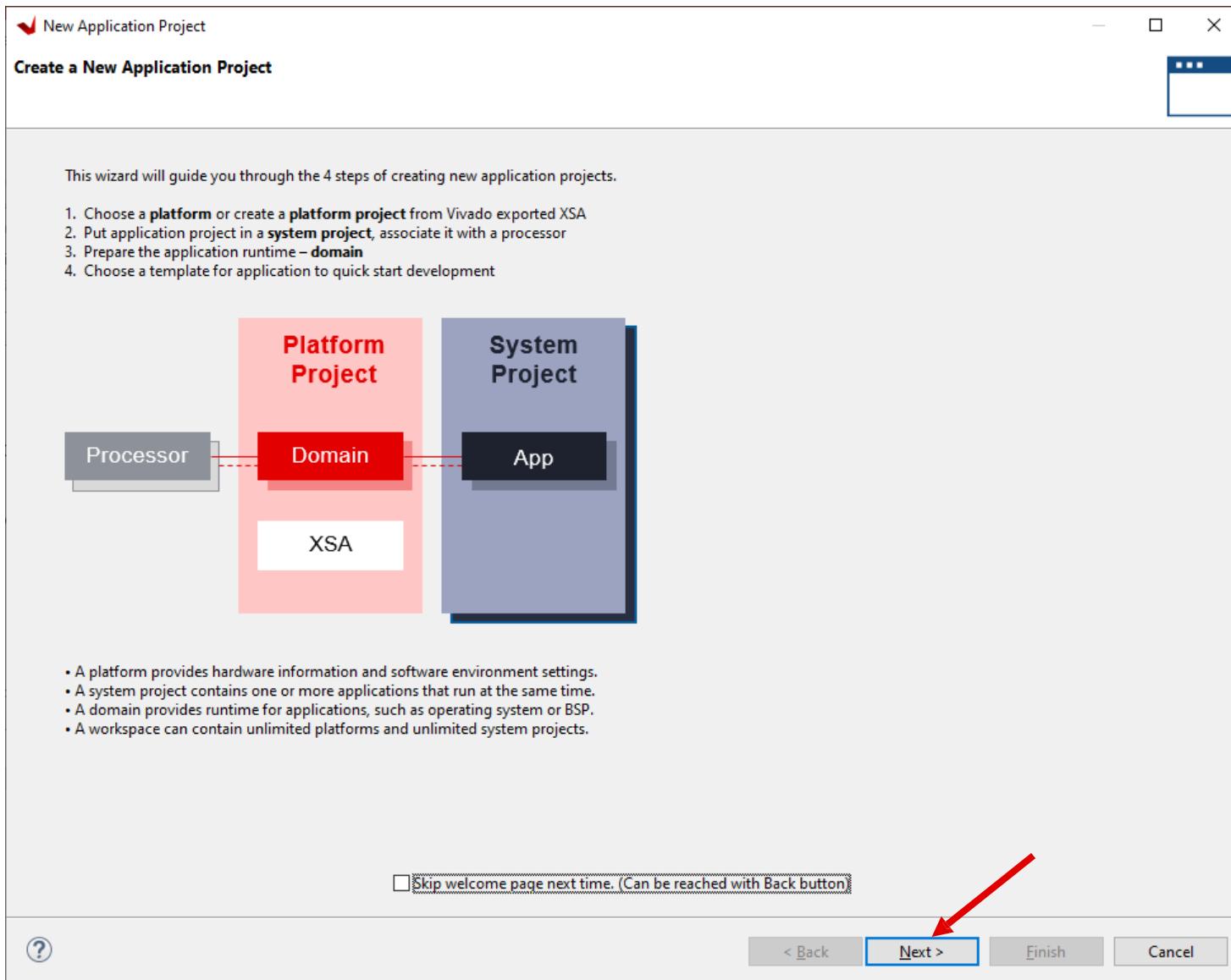
Build Complete



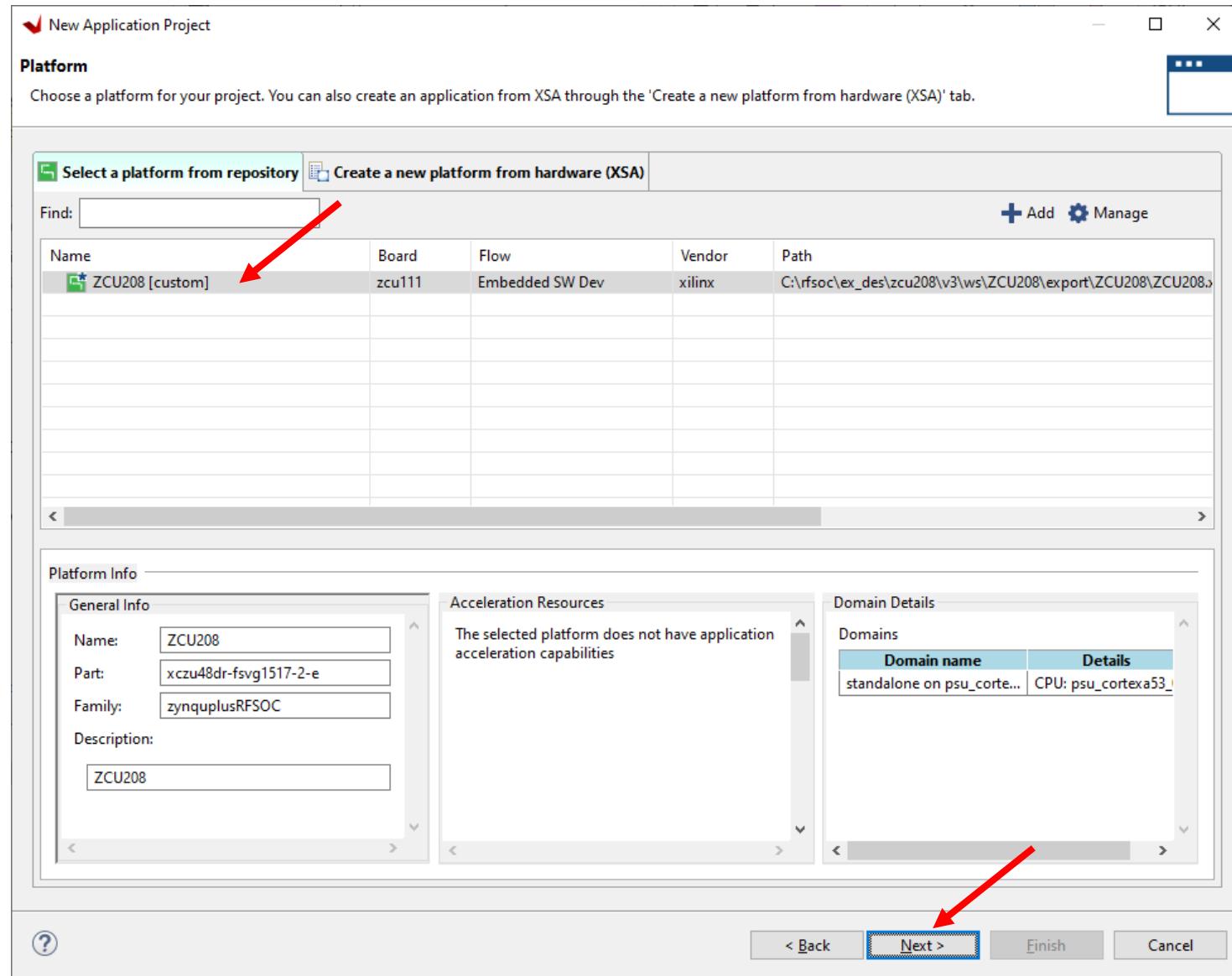
Create Application



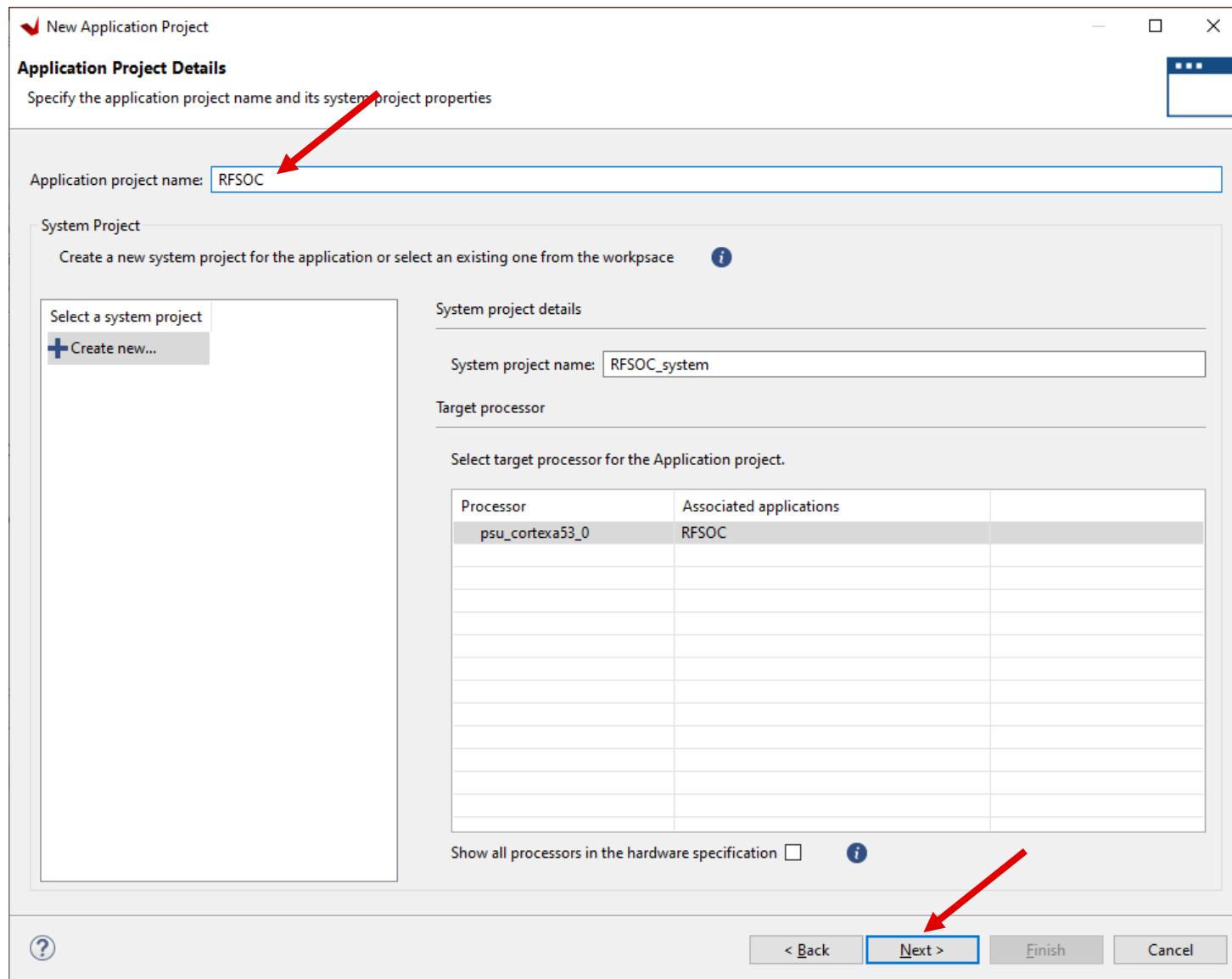
Create Application Cont'd



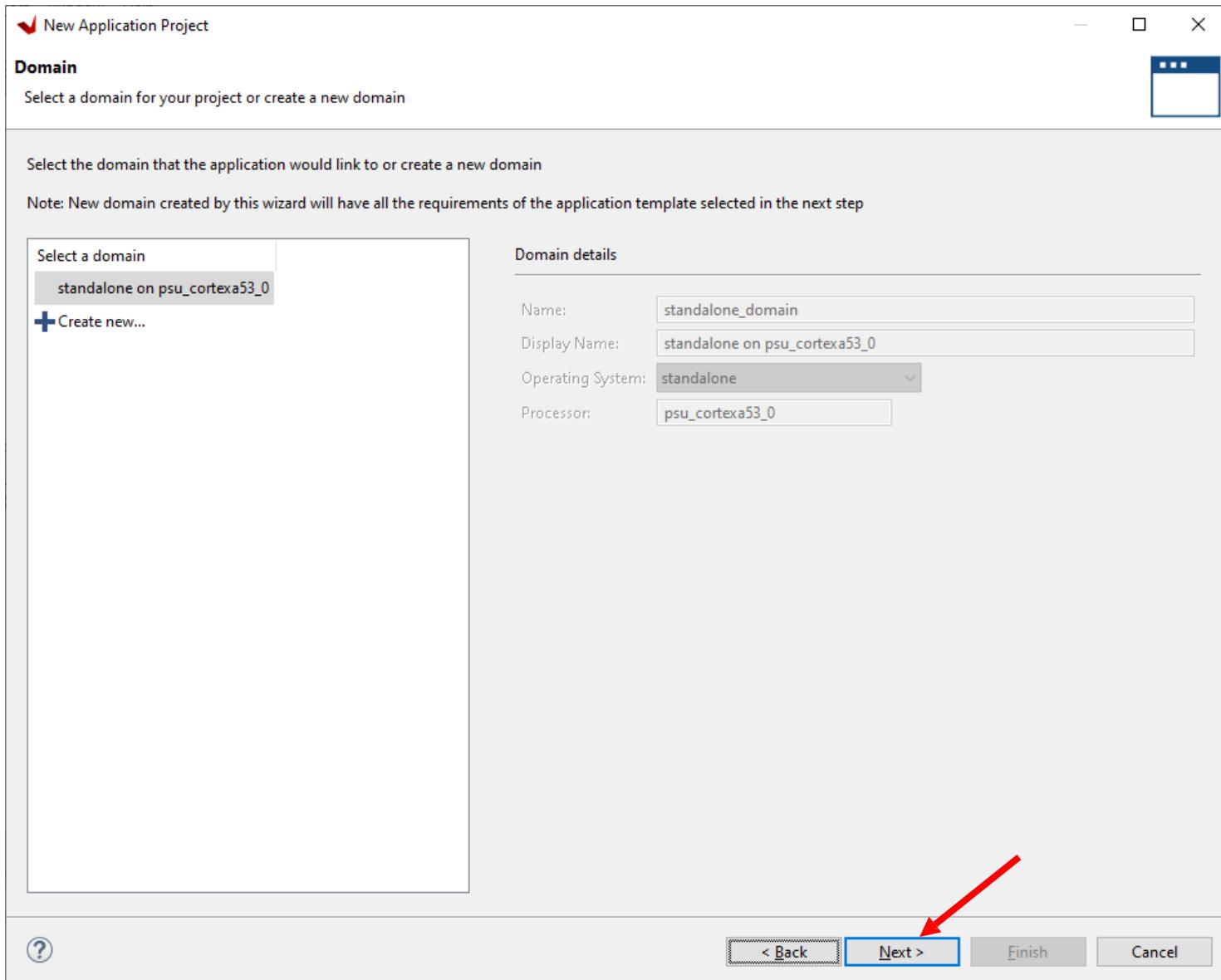
Create Application Cont'd



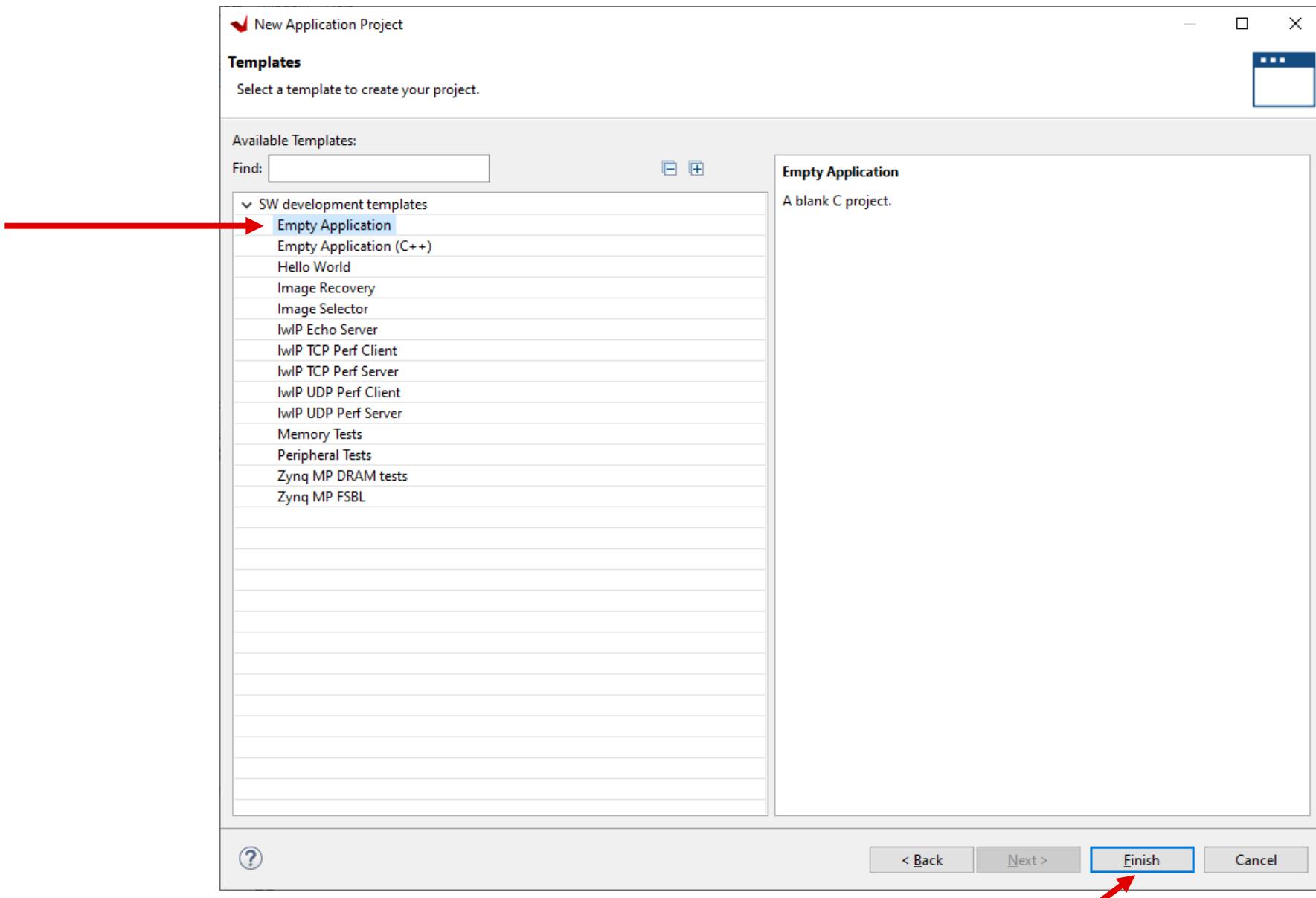
Create Application Cont'd



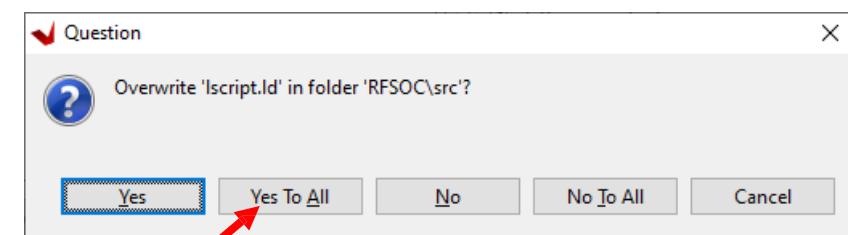
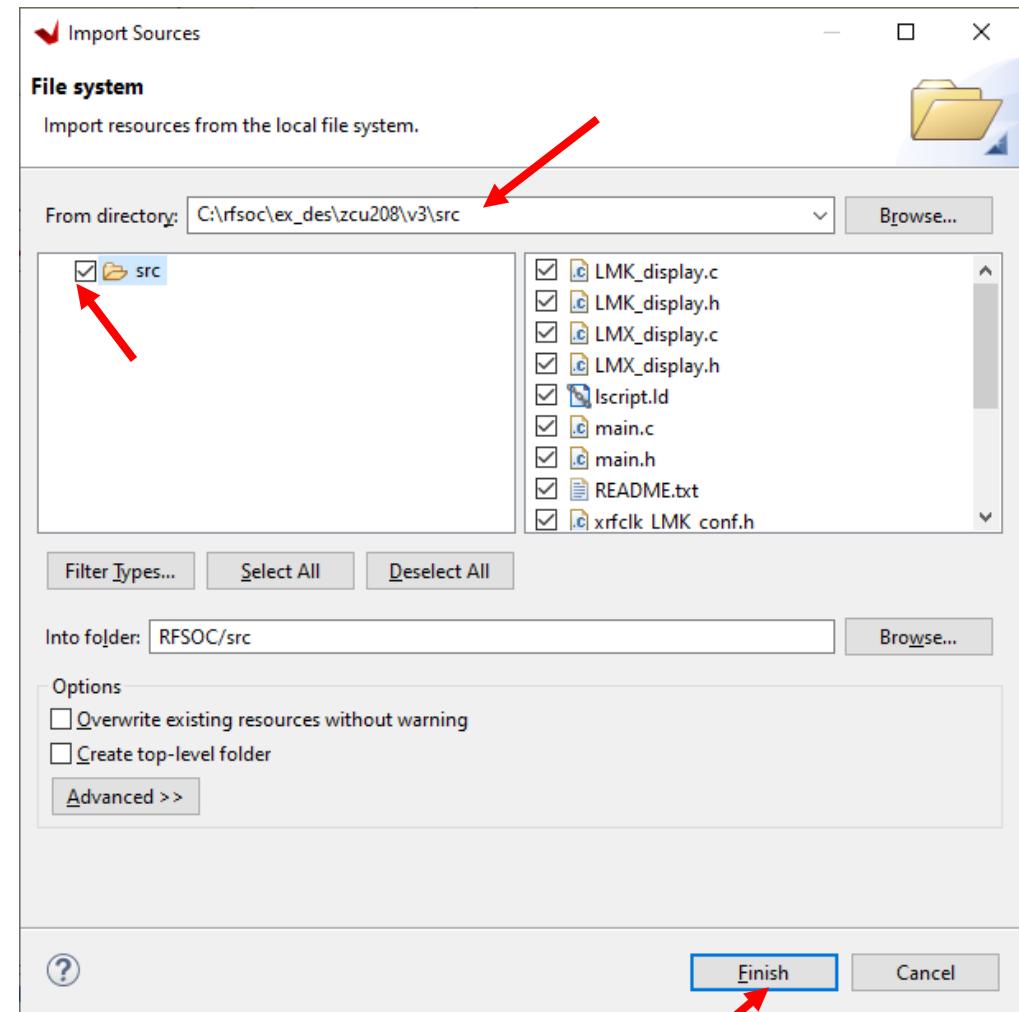
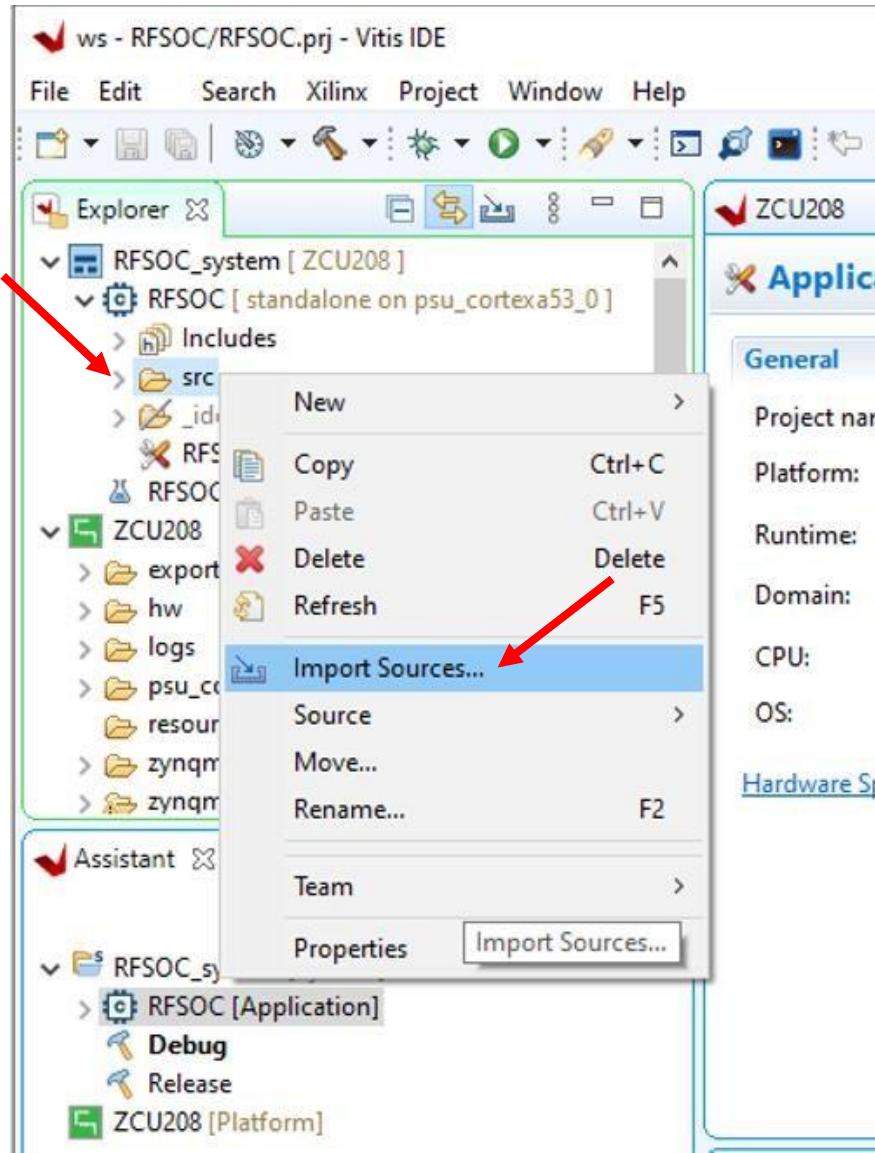
Create Application Cont'd



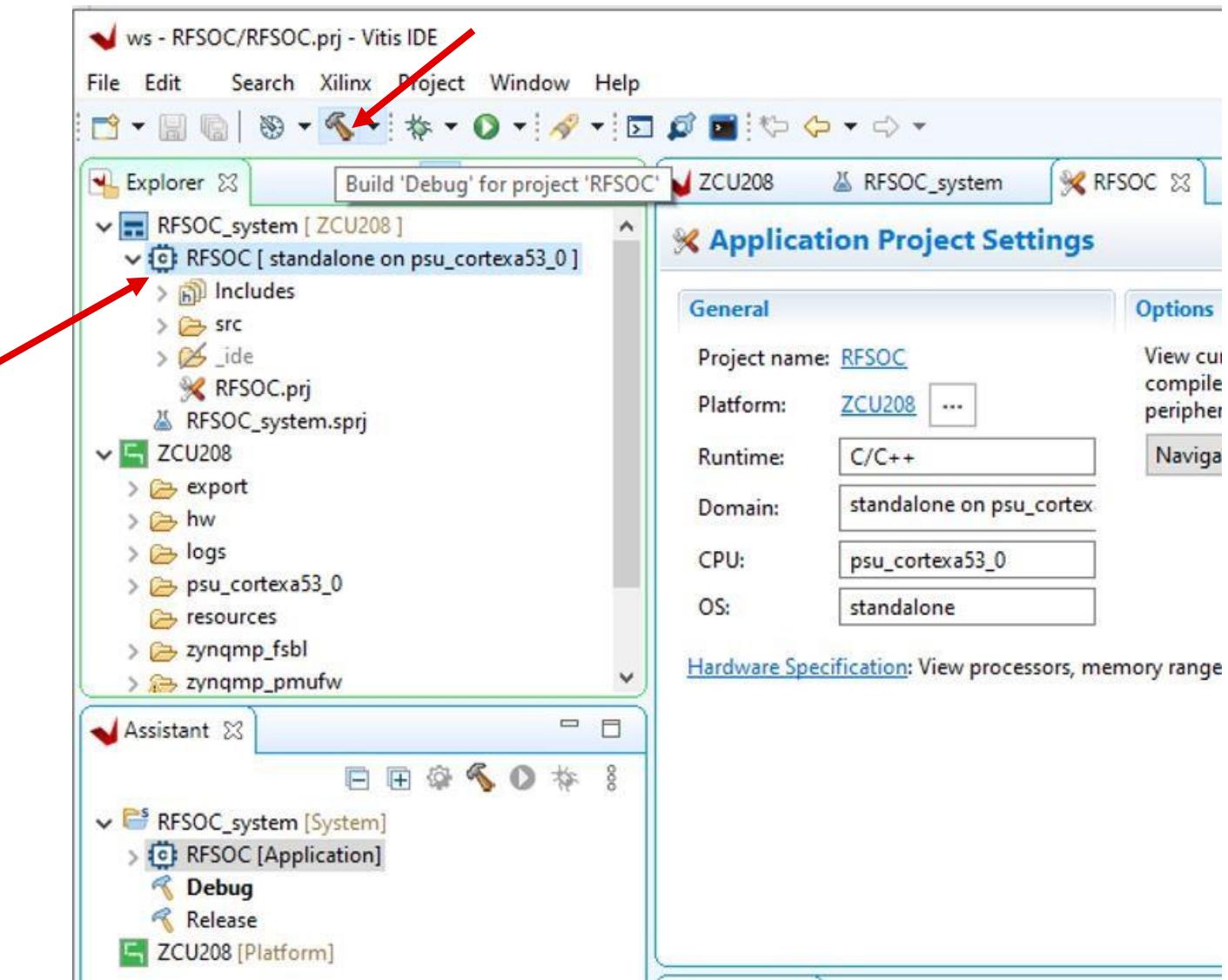
Create Application Cont'd



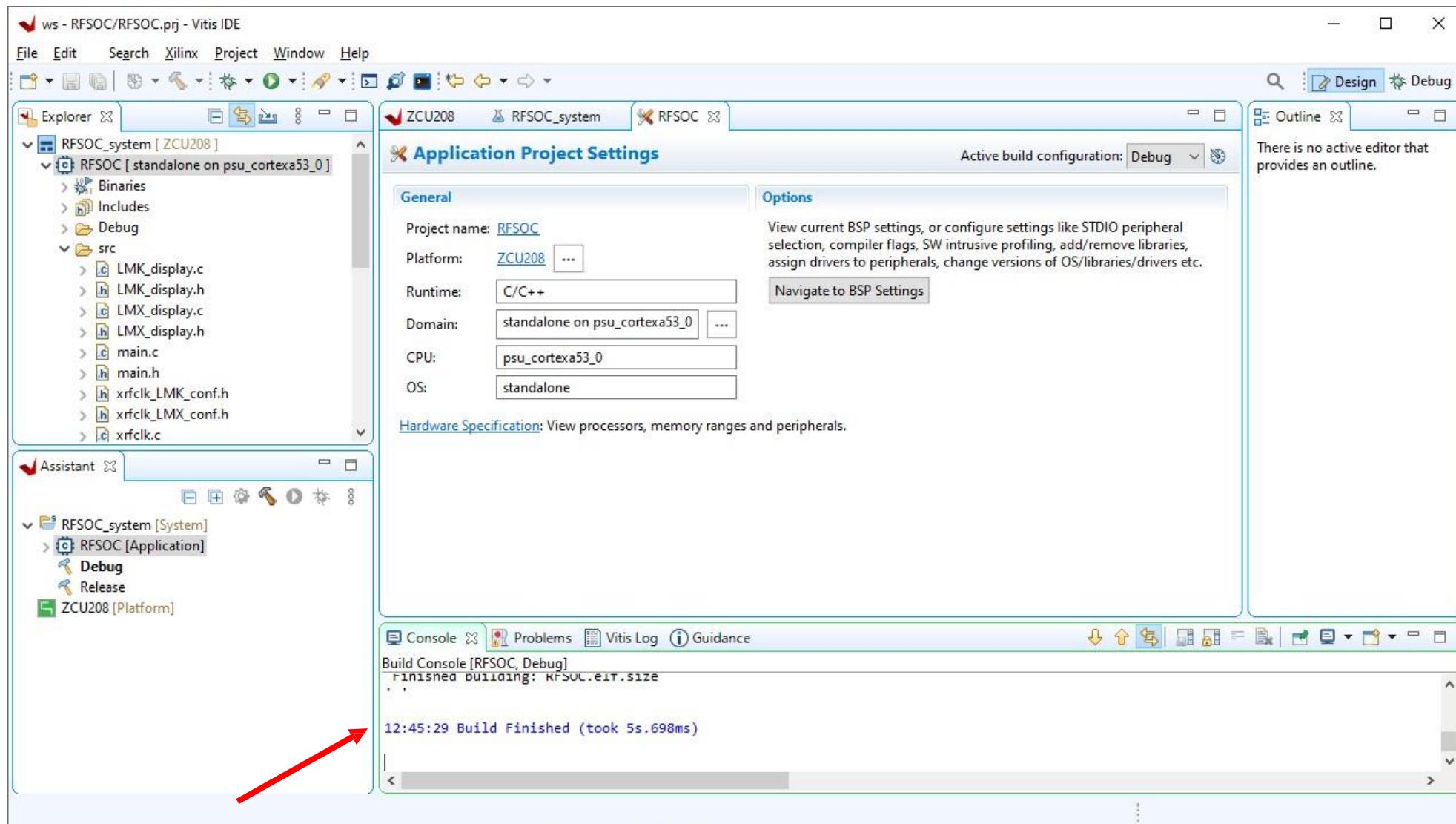
Import Sources



Build Application



Build Complete

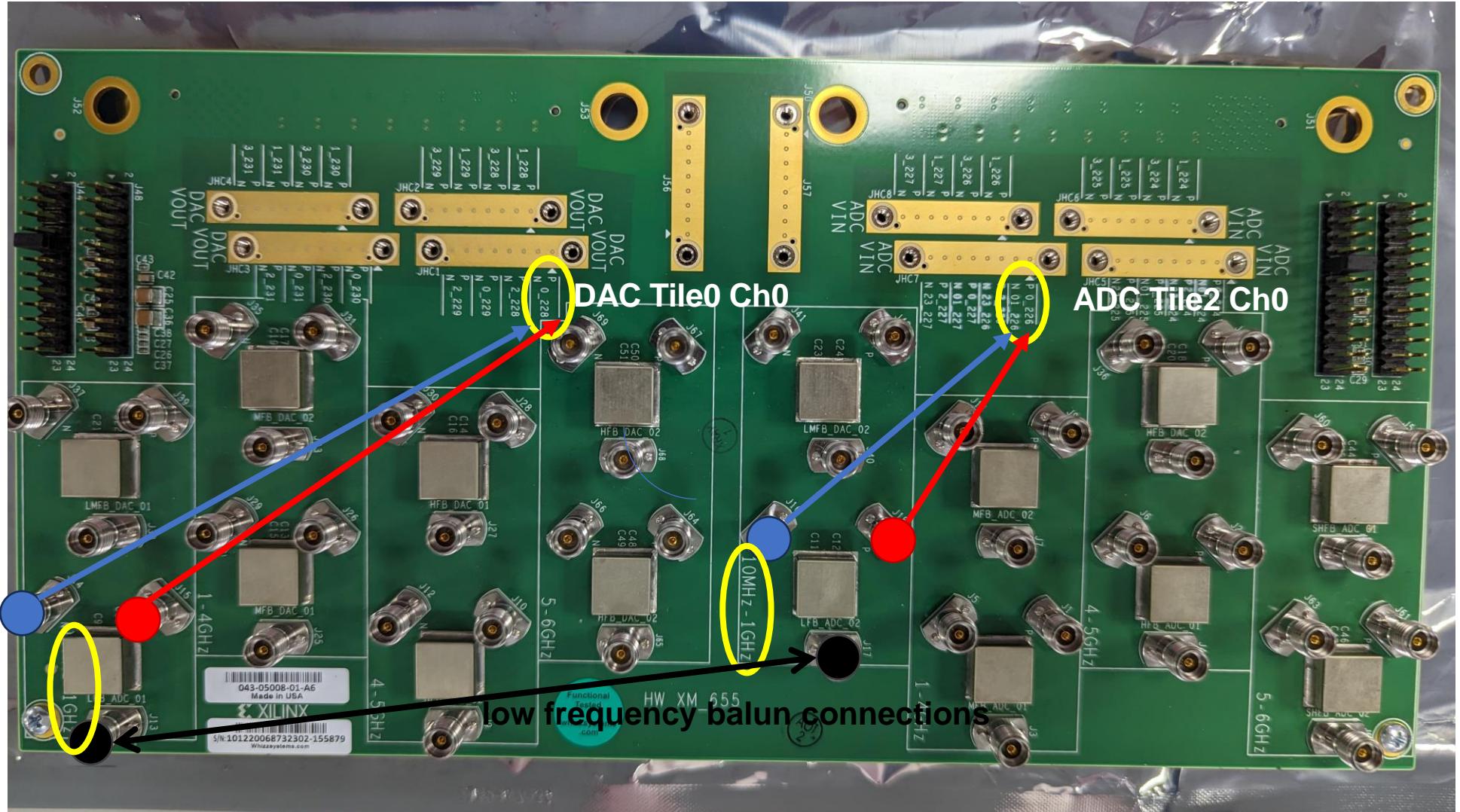




Run Design

Board Setup for the Upcoming Designs

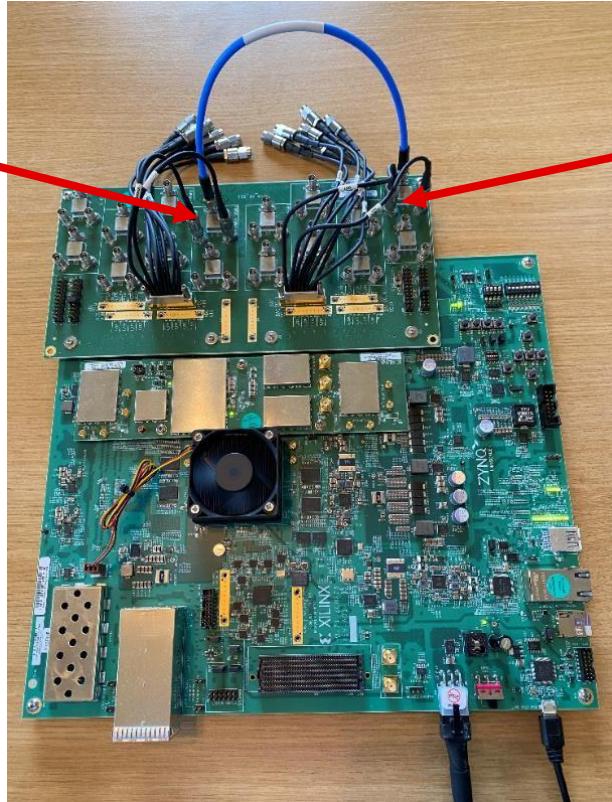
- ▶ Connect DAC Tile 228 Ch0 output to ADC Tile 226 Ch0 input on XM655 (low frequency balun connections).



Board Setup for the Upcoming Designs

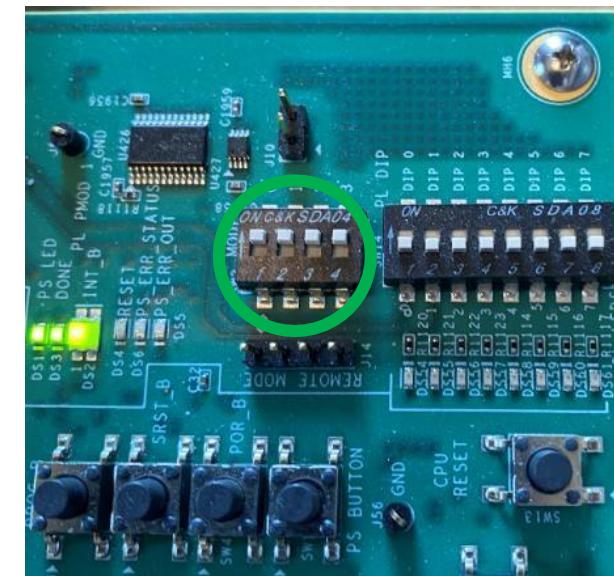
- ▶ Connect DAC Tile 228 Ch0 output to ADC Tile 226 Ch0 input on XM655 (low frequency balun connections).
- ▶ Set SW2 to on,on,on,on (JTAG boot mode).
- ▶ Connect USB to host for JTAG, PS UART, and System Controller UART access.

ADC Tile2 Ch0



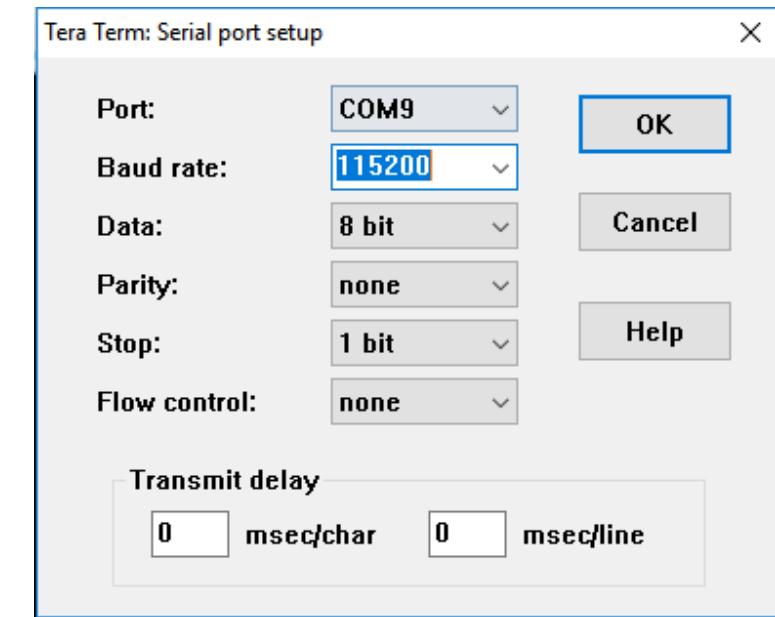
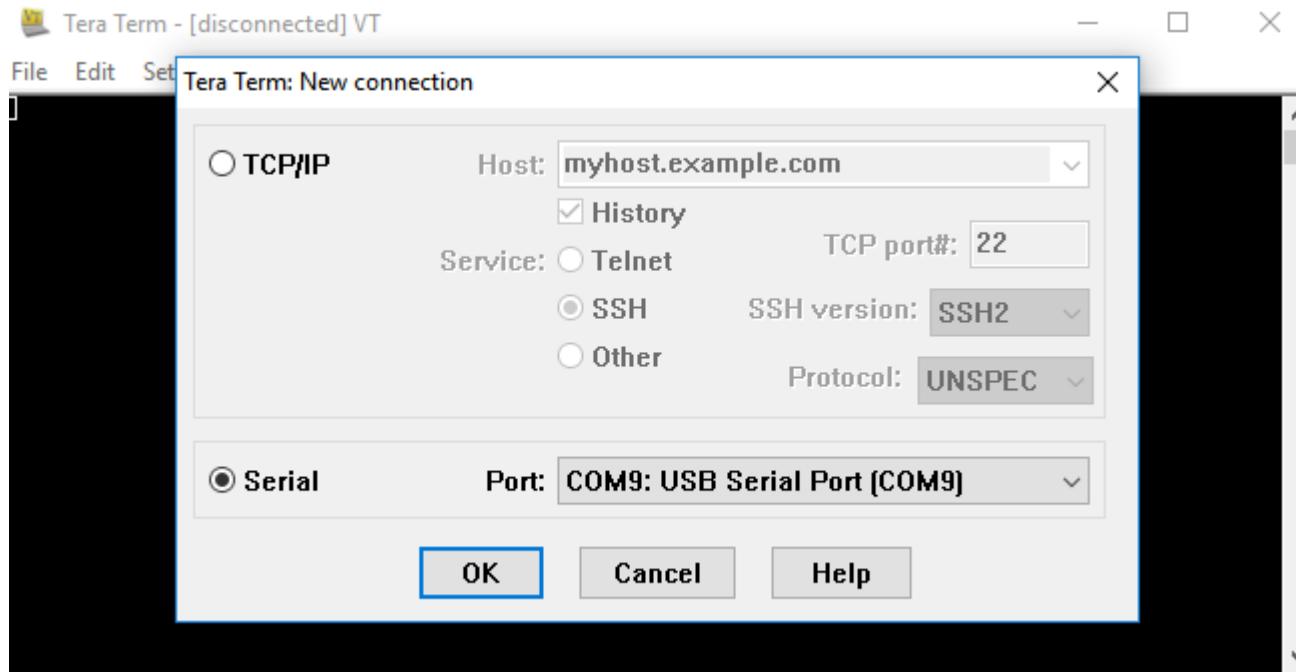
DAC Tile0 Ch0

SW2

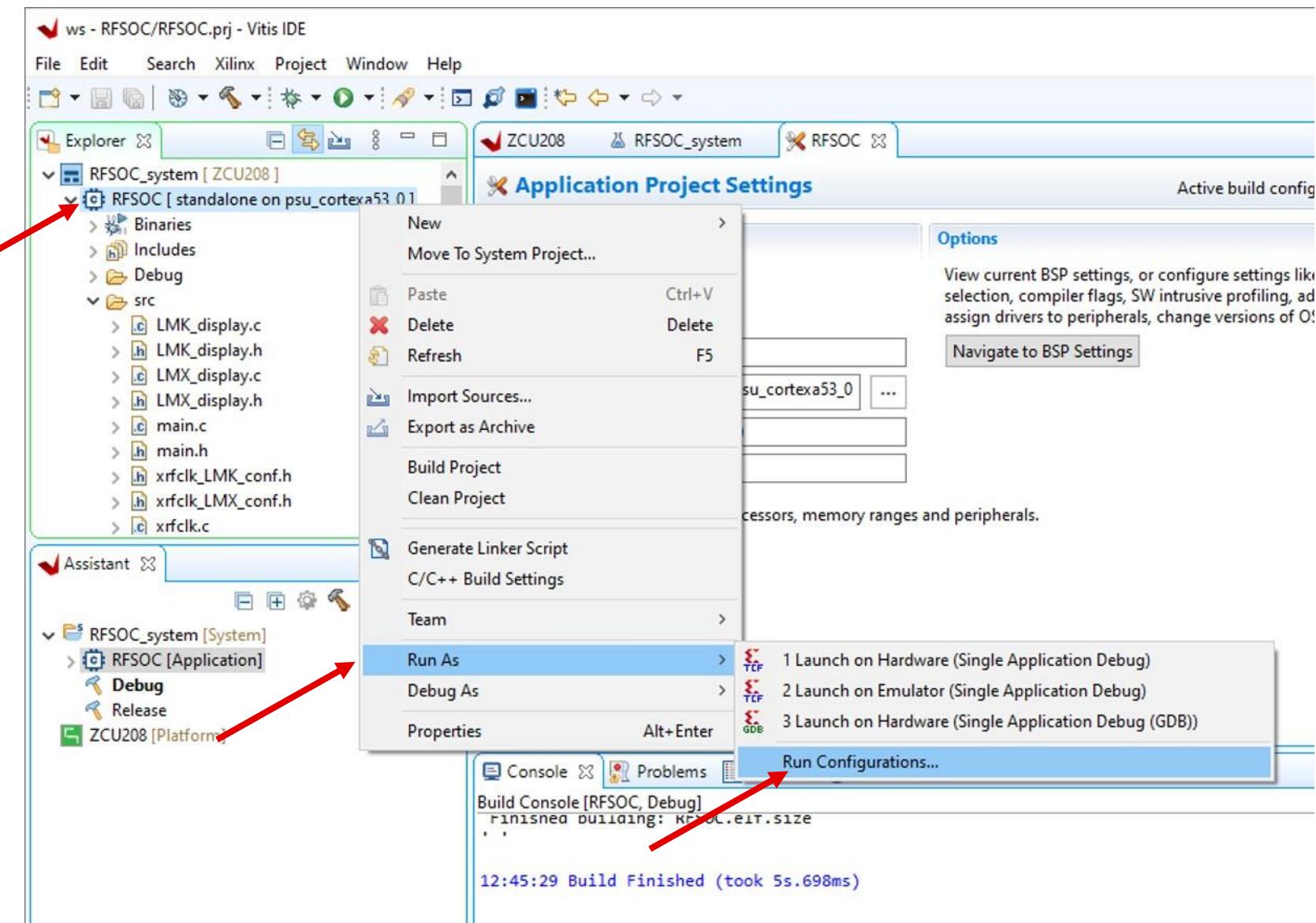


Open a Terminal Window

Open the COM port on the compute and set the rate to 115200.

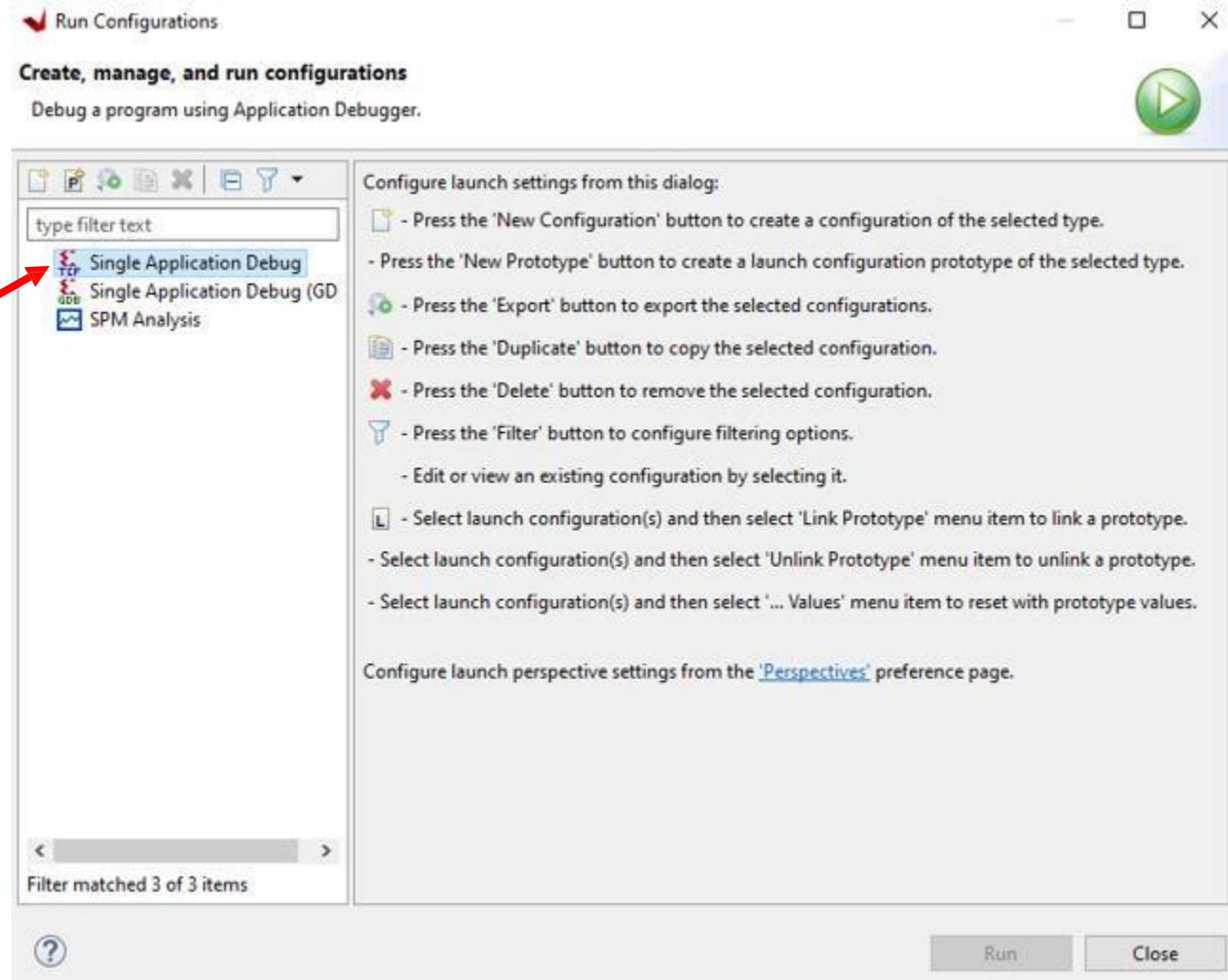


Setup Run Configuration

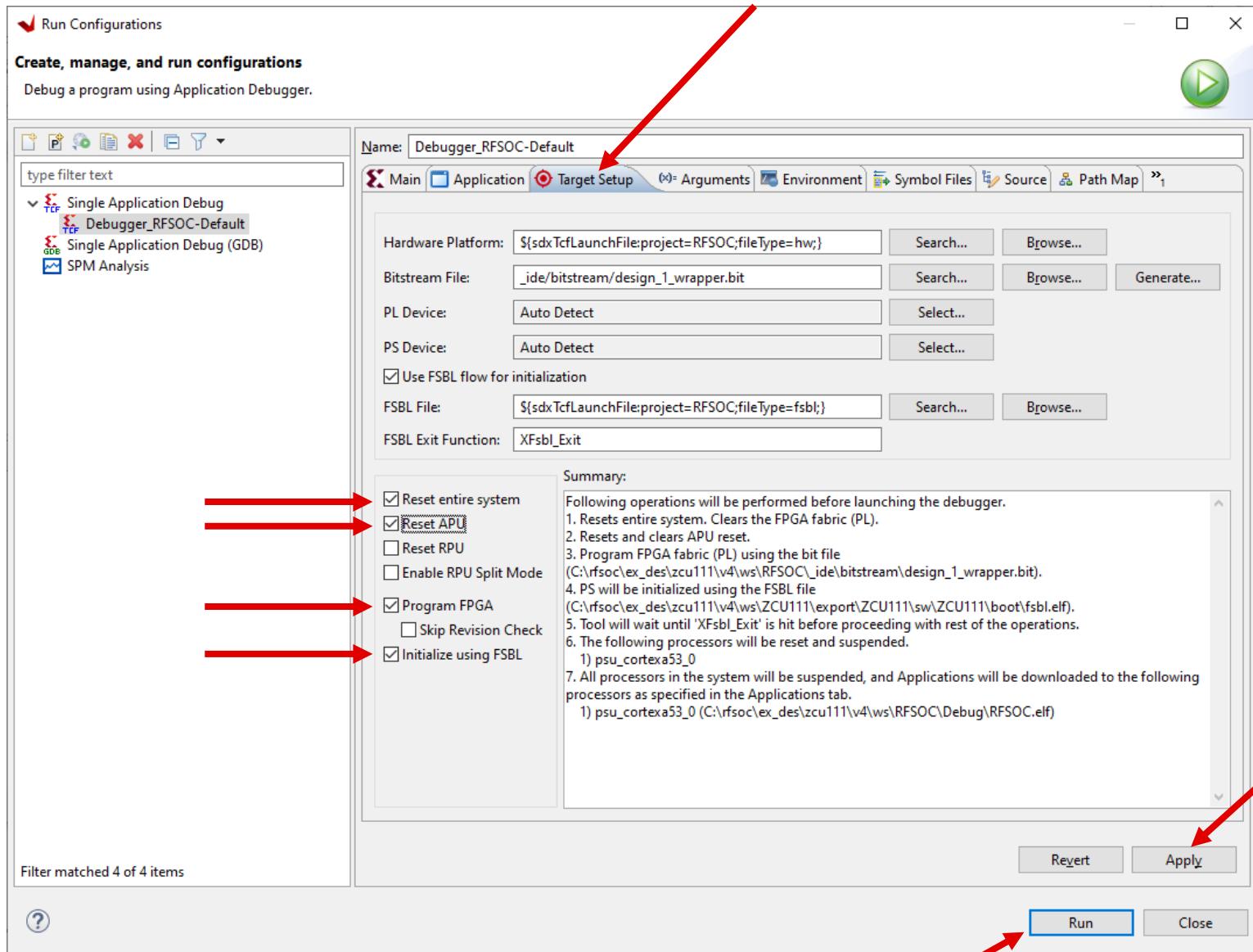


Run Configuration Cont'd

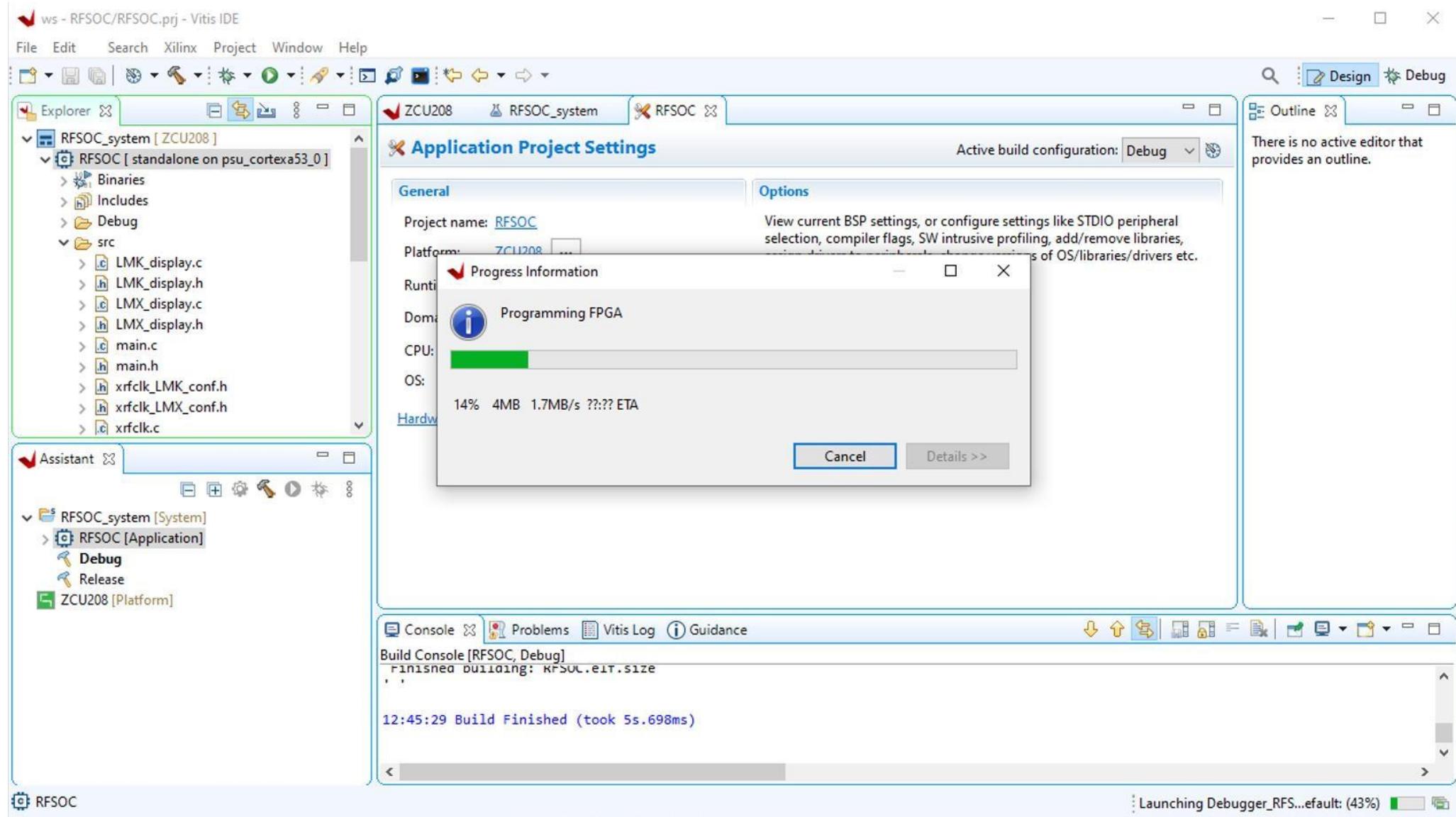
Double Click



Run Configuration Cont'd



Run Design



Application Startup

The application...

1. Programs the clocks.
2. Issues the data converters master reset.
3. Displays the Power-on Sequence Step of the data converters.

```
COM41:115200baud - Tera Term VT
File Edit Setup Control Window Help

Xilinx Zynq MP First Stage Boot Loader
Release 2020.2 Jun 24 2021 - 12:14:38
PMU-FW is not running, certain applications may not be supported.

#####
Hello RFSoC World!

RFDC IP Version: 2.4

Configuring the data converter clocks...
Configuring CLK104 LMK and LMX devices
Clk settings read from LMK -----
CLKin1_freq: 10000KHz
DCLKout00(RFIN_RF1) : 184320KHz SDCLKout01(RF1_ADC_SYNC ) : -----
DCLKout02(NC) : ----- SDCLKout03(AMS_SYSREF ) : -----
DCLKout04(RFIN_RF2) : 184320KHz SDCLKout05(RF2_DAC_SYNC ) : -----
DCLKout06(DAC_REFCLK) : 184320KHz SDCLKout07(DDR_PL_CAP_SYNC): -----
DCLKout08(PL_CLK) : ----- SDCLKout09(PL_SYSREF ) : -----
DCLKout10(NC) : ----- SDCLKout11(J10_SINGLE_END ) : -----
DCLKout12(ADC_REFCLK) : 184320KHz SDCLKout13(NC ) : -----


Clk settings read from LMX_RF1 -----
CLKin_freq: 184320KHz
RFoutA Freq: -----
RFoutB Freq: -----


Clk settings read from LMX_RF2 -----
CLKin_freq: 184320KHz
RFoutA Freq: -----
RFoutB Freq: -----

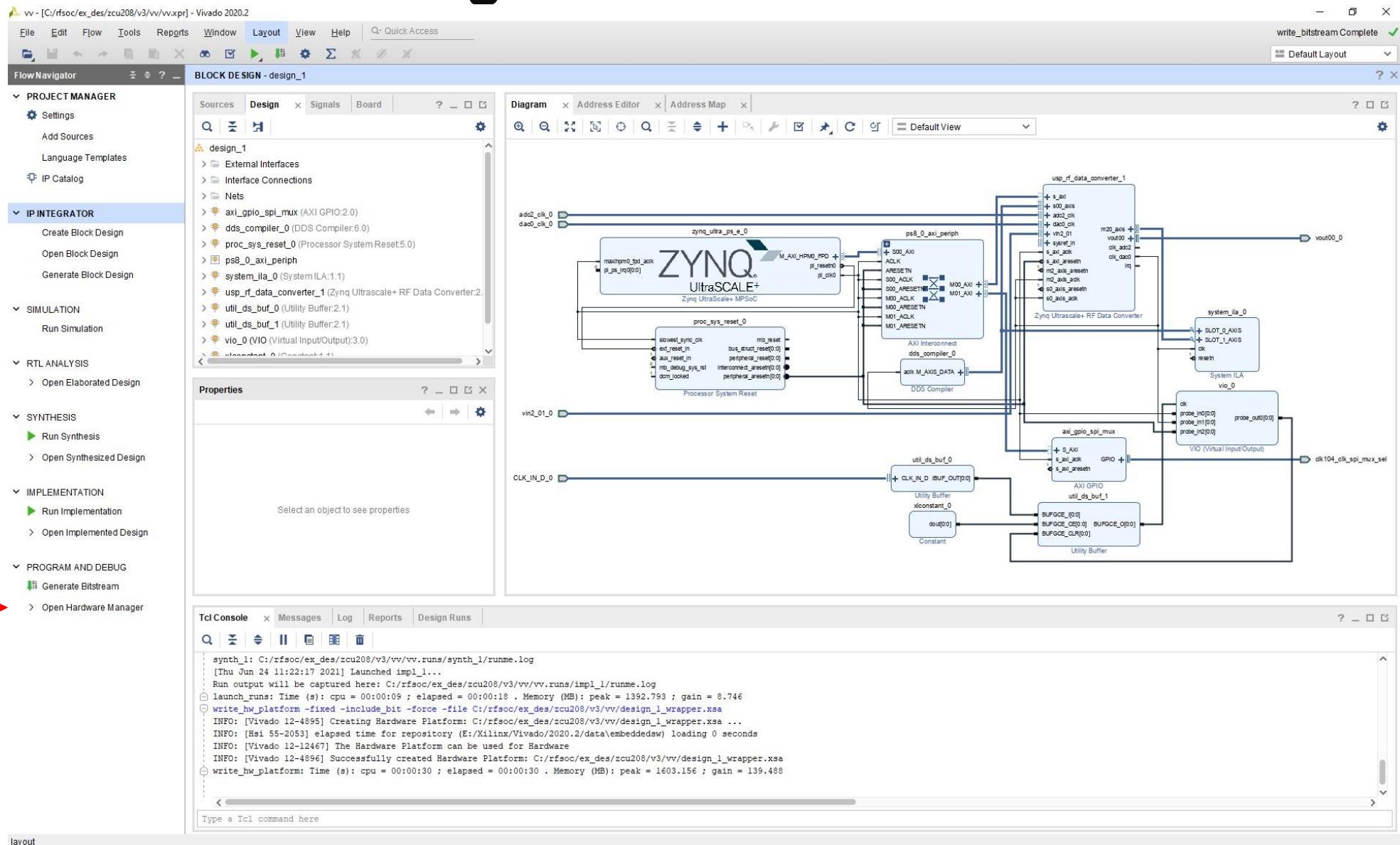

==== Metal log enabled ====
metal: debug: registered generic bus

DeviceID: 0
Silicon Revision: 1
The RFDC controller is initialized.
Data Converter startup up is in progress...

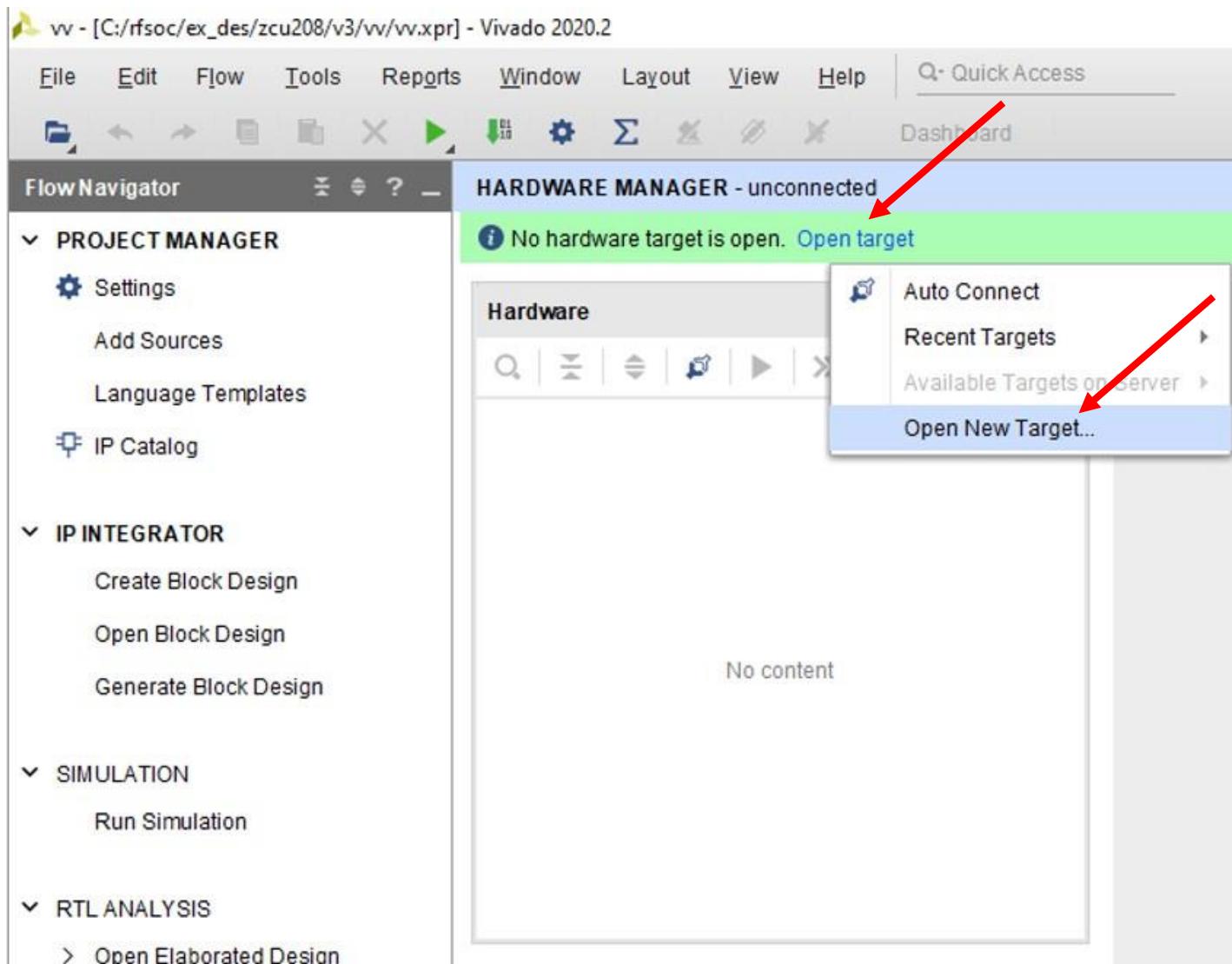
The Power-on sequence step. 0xF is complete.
  DAC Tile0 Power-on Sequence Step: 0x0000000F
  ADC Tile2 Power-on Sequence Step: 0x0000000F

Data Converter start up is complete!
----- Startup Complete -----
```

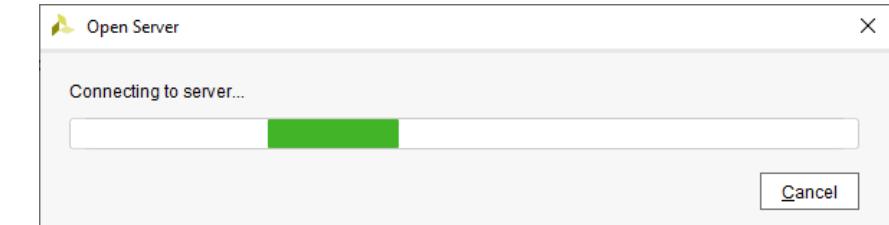
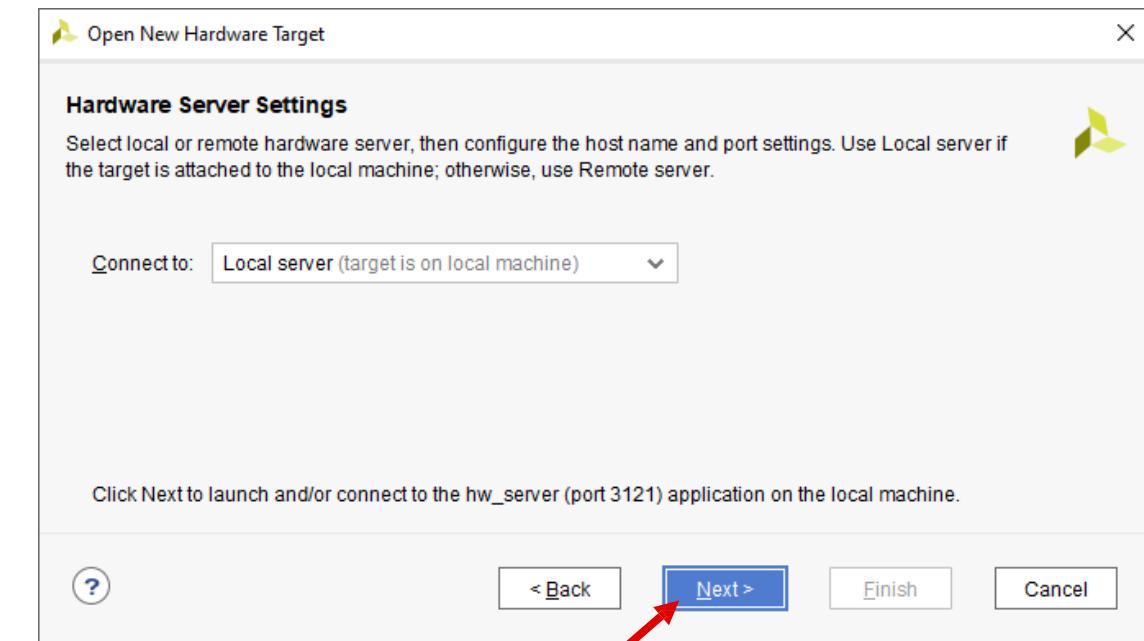
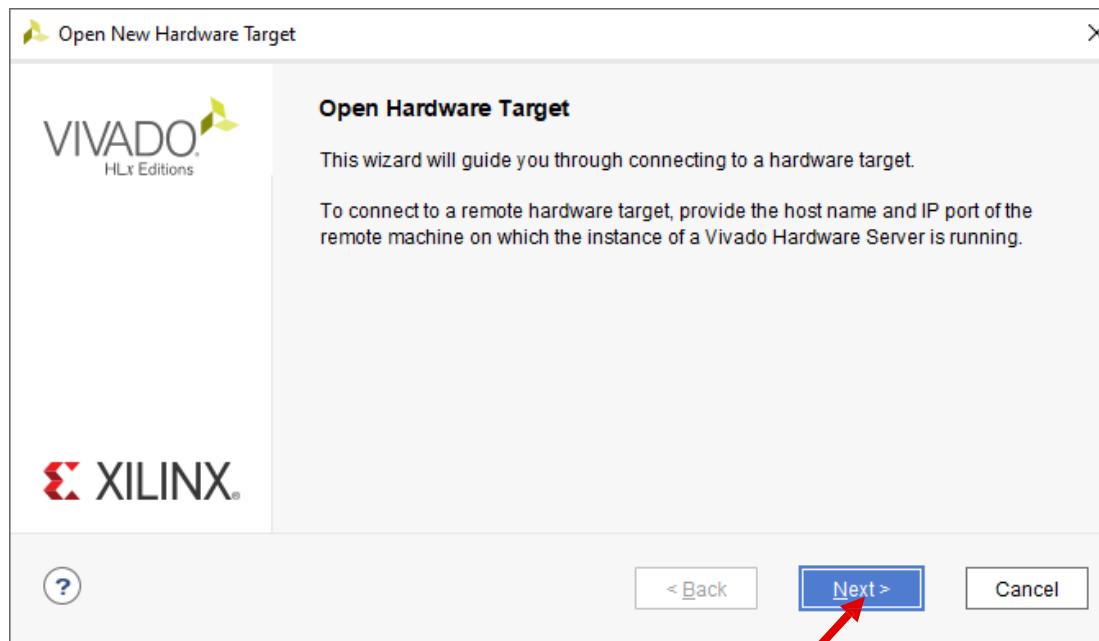
Open Hardware Manager



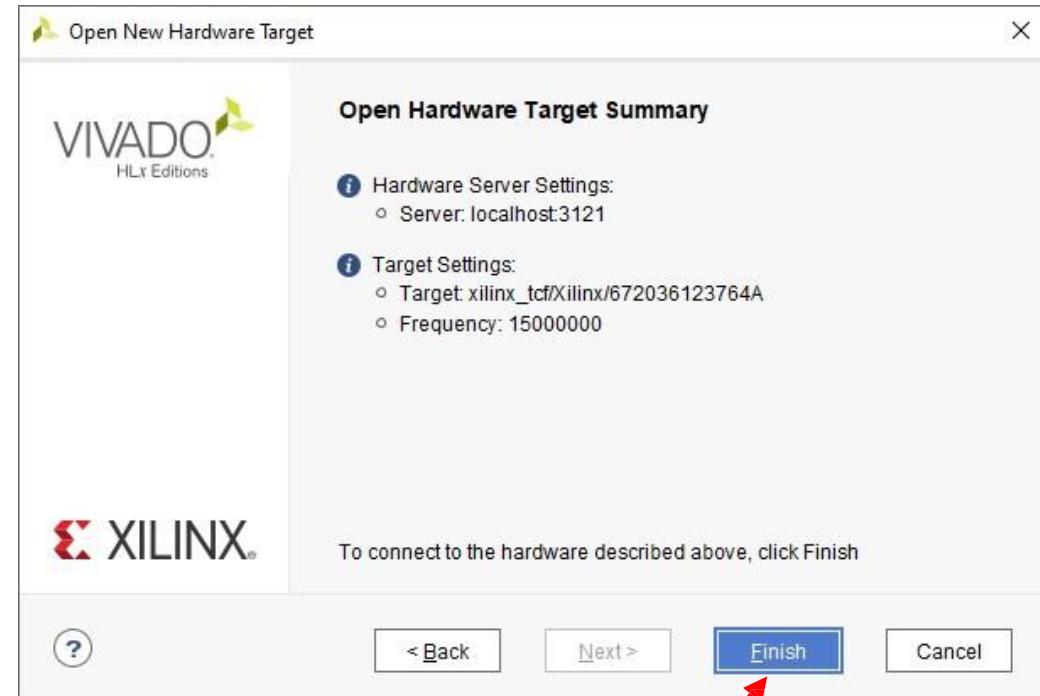
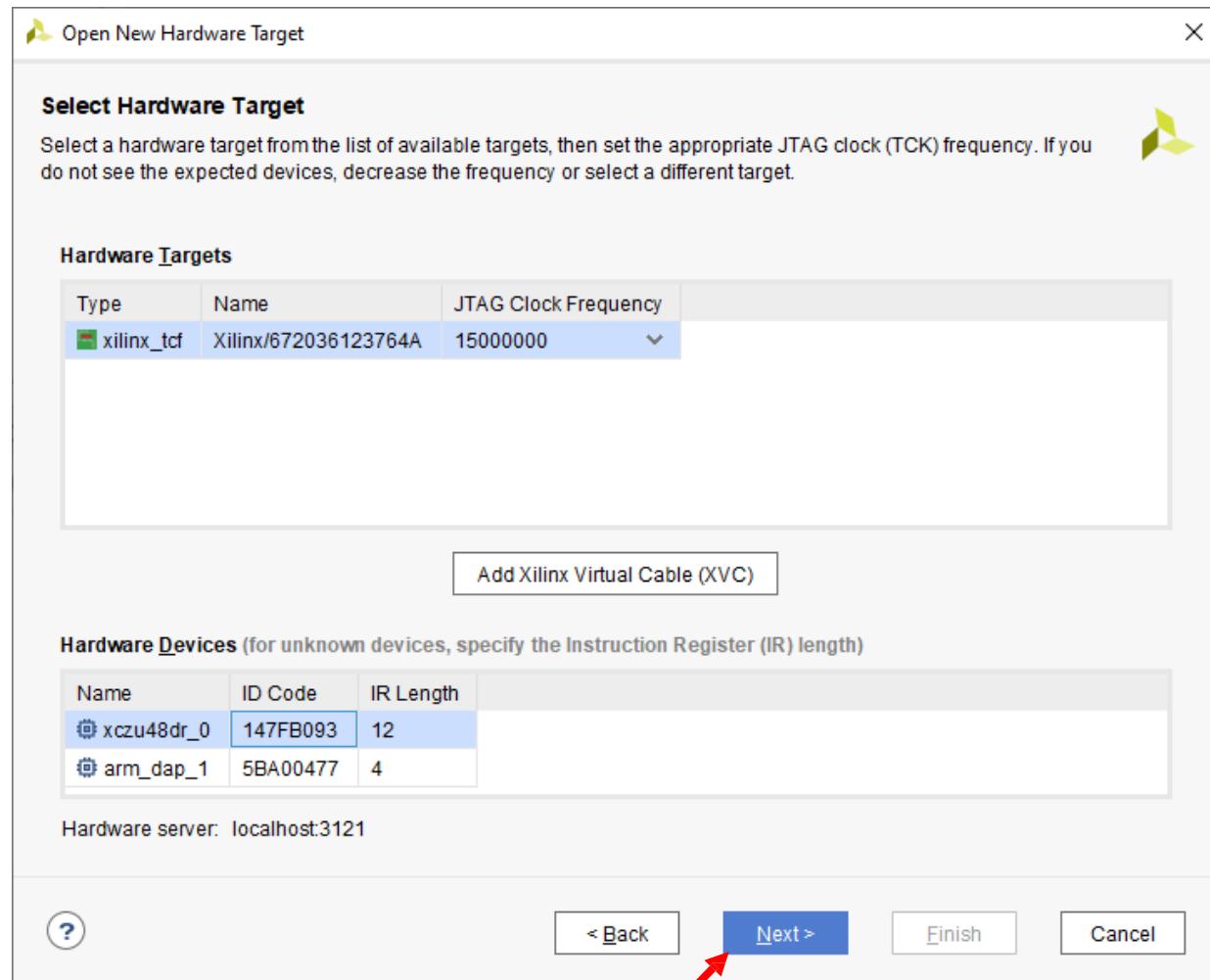
Open New Target



Open Hardware Target



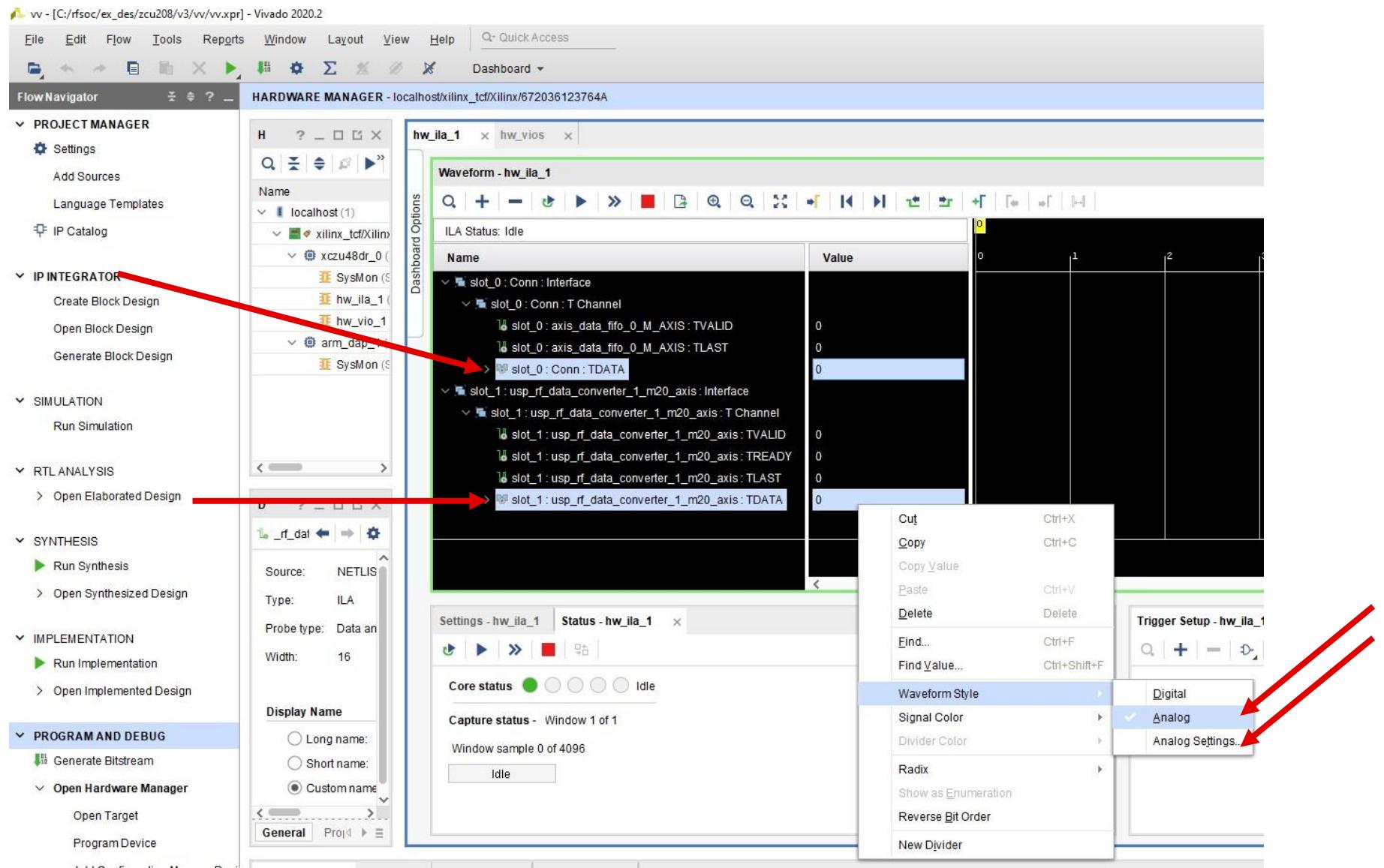
Open Hardware Target Cont'd



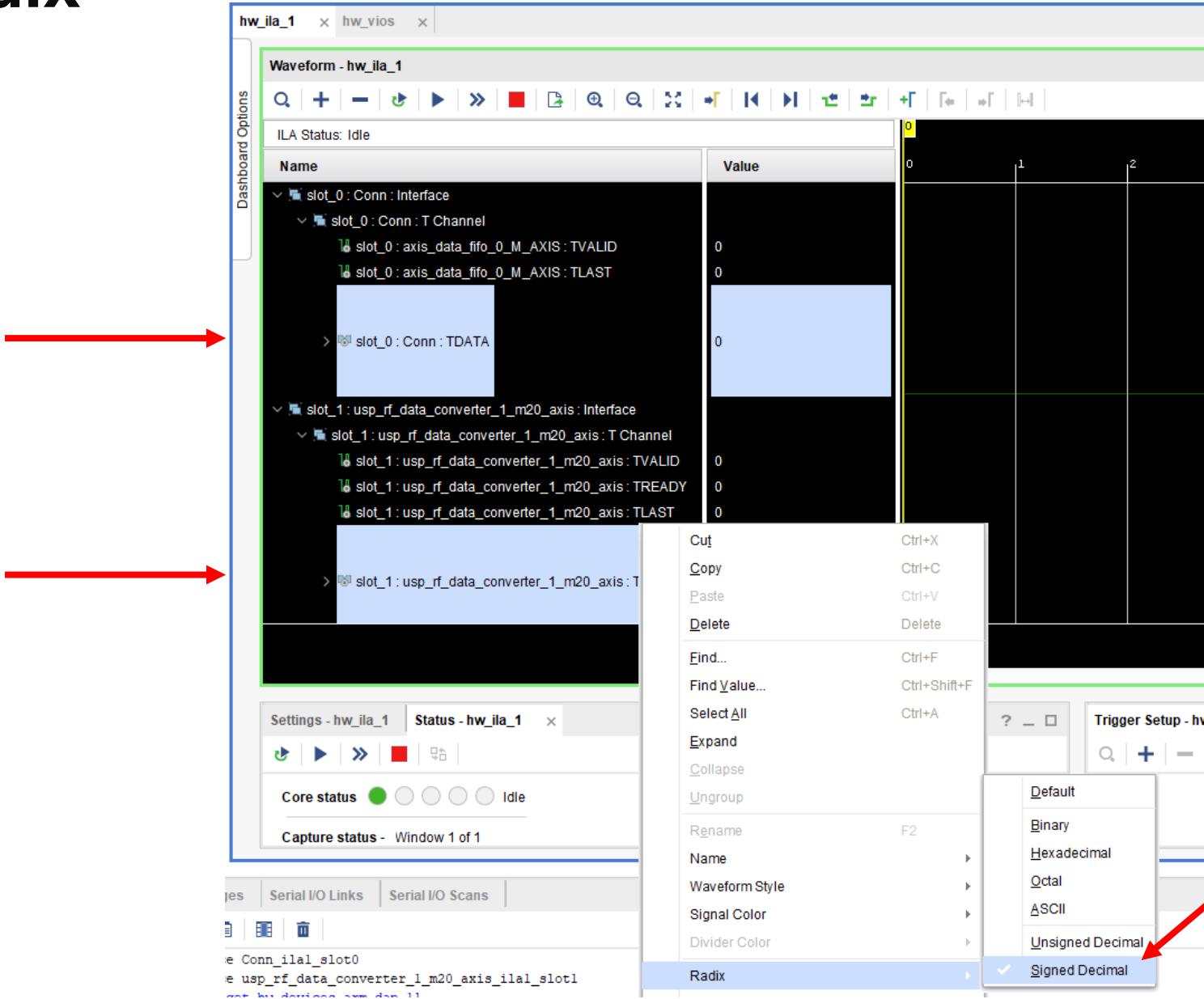
Convert Data to the Analog Waveform Style

10MHz sine wave
going from the DDS
compiler to the DAC.

ADC capture to the
System ILA.



Radix

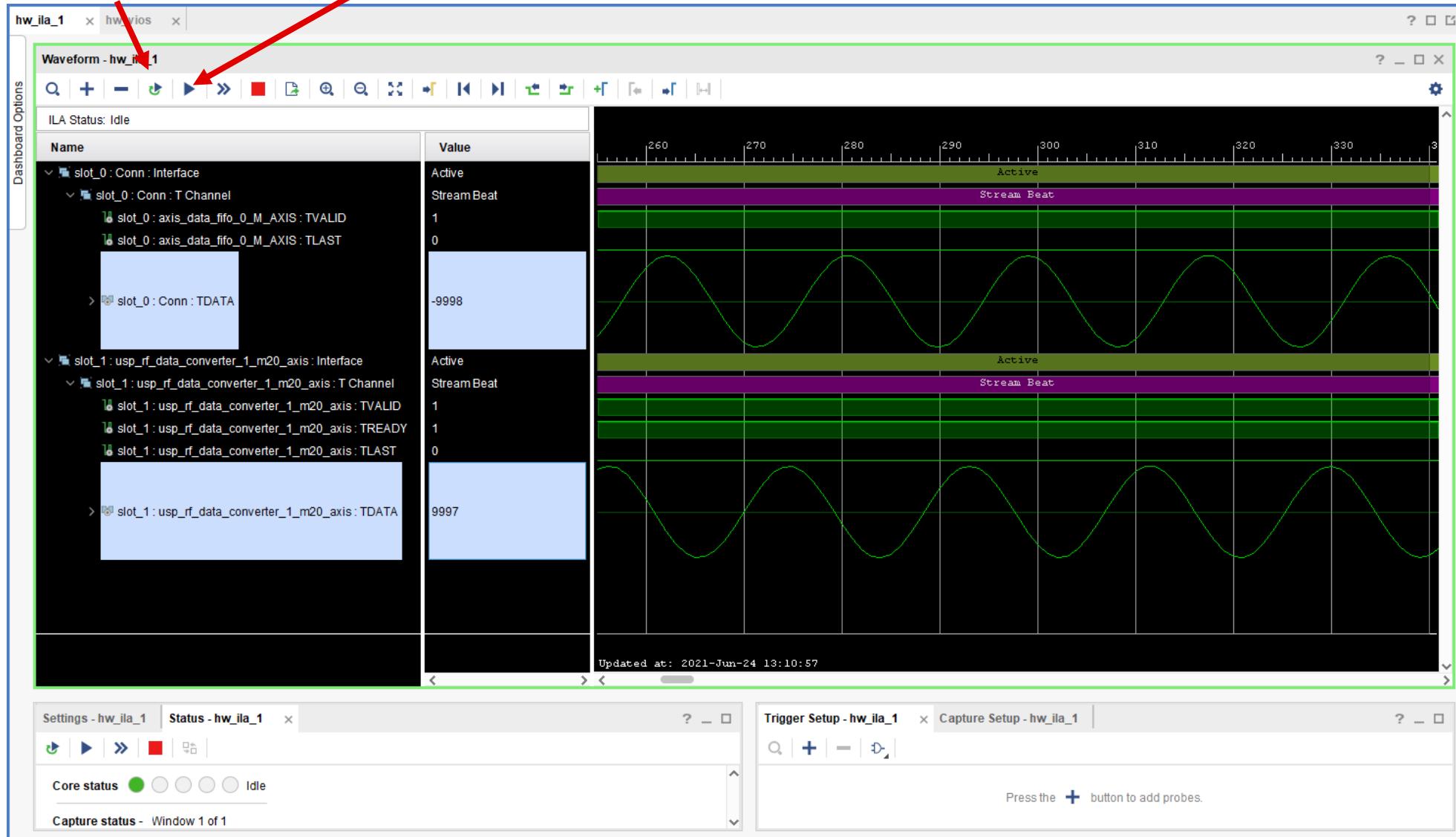


Use Radix of Signed Decimal.

System ILA Capture

Automatically retrigger

Trigger ILA capture





DDS Compiler

DDS Overview

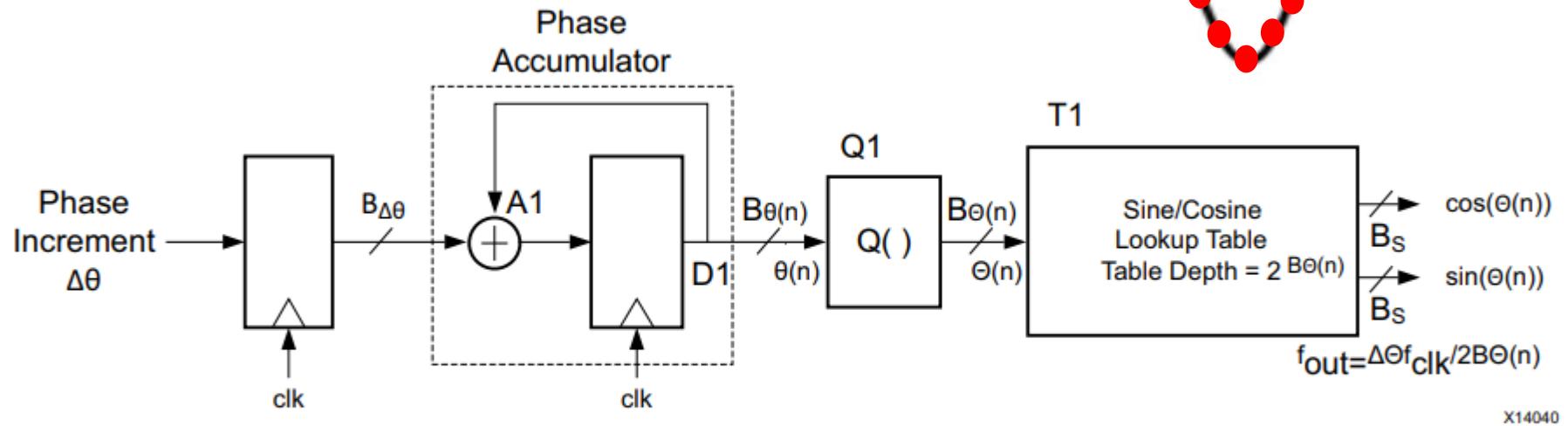
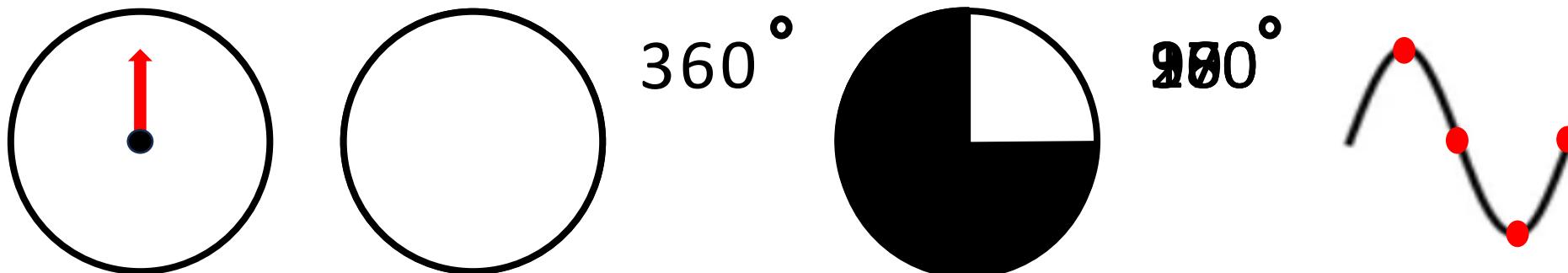
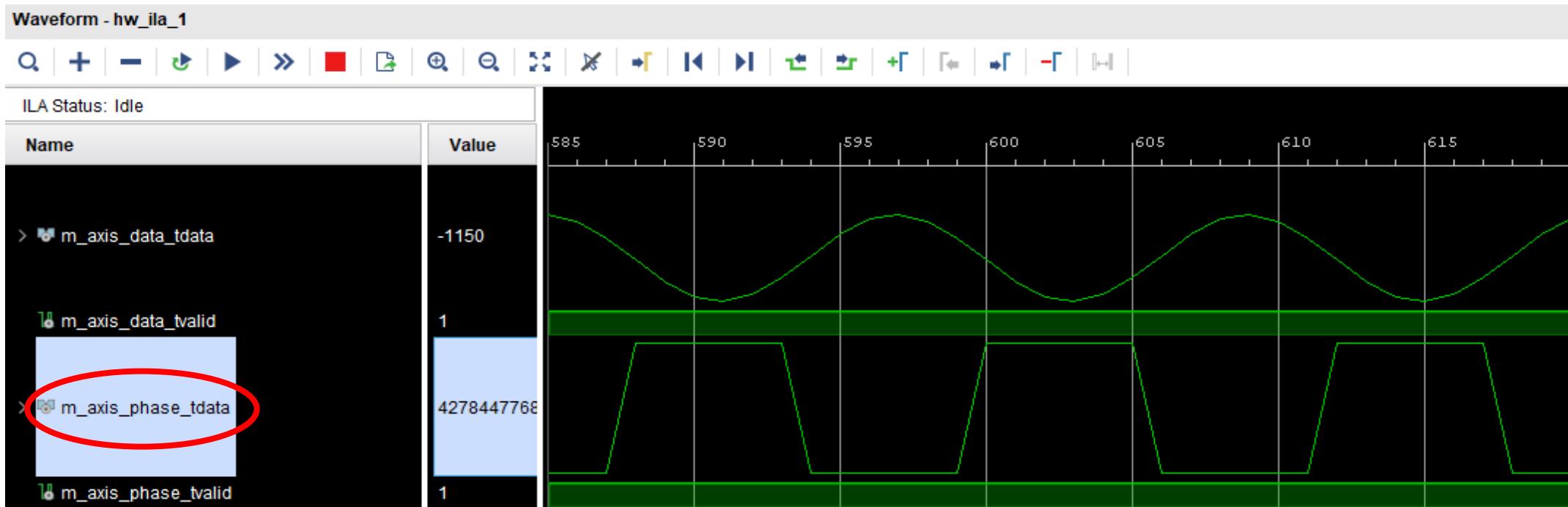
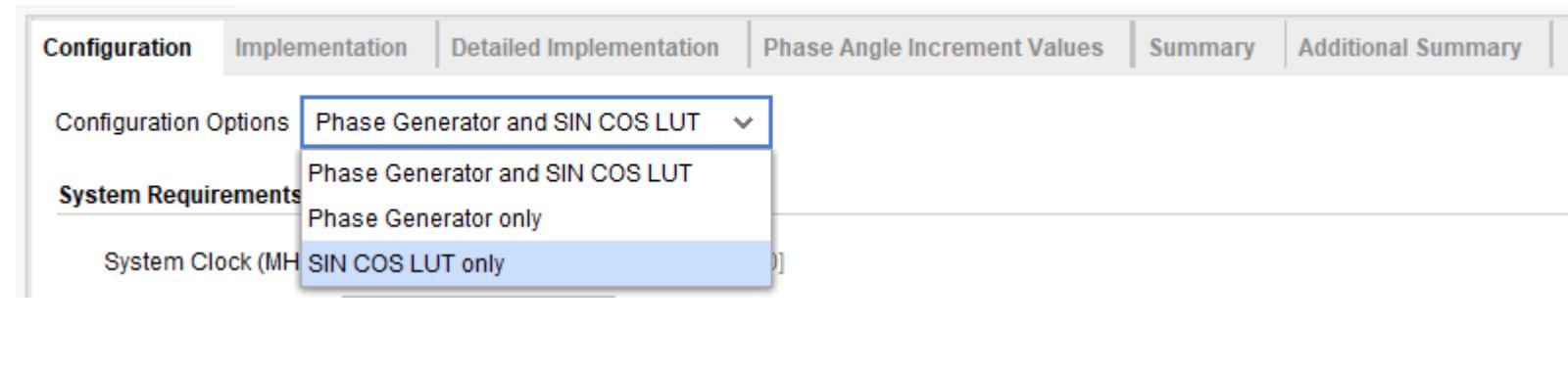
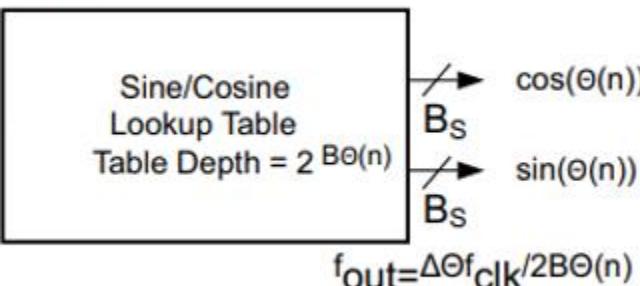


Figure 3-1: Phase Truncation DDS (Simplified View of the DDS Core)



Generated Phase and SIN COS LUT

T1



Mode of Operation

Mode Of Operation

Standard

Frequency per Channel (Fs) 12.0 MHz

Configuration	Implementation	Detailed Implementation	Output Frequencies	Summary
Channel				Output Frequency (MHz)
1				1

Configuration	Implementation	Detailed Implementation	Output Frequencies	Summary	Additional Summary
Channels		Phase Increment		Phase Offset	
1	1	HEX Value	Actual MHz	HEX Value	Actual Cycles

(0.75000000000000000000)
0
(0.00000000000000000000)

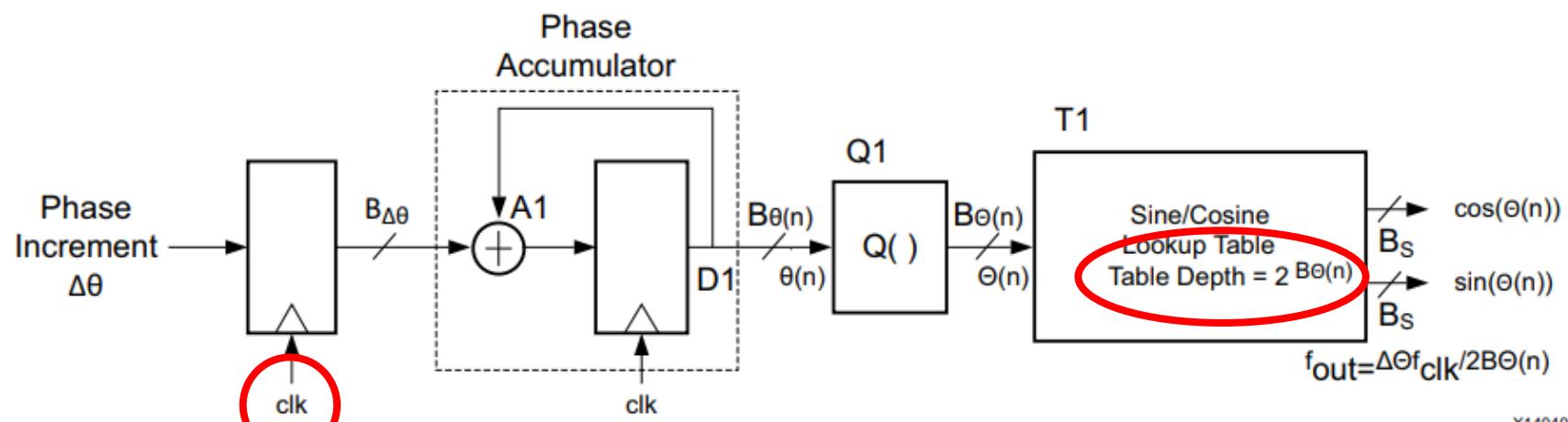


Figure 3-1: Phase Truncation DDS (Simplified View of the DDS Core)

Rasterized

Standard Mode

$$f_{out} = \frac{f_{clk}\Delta\theta}{2^{B_{\theta(n)}}}$$

Mode Of Operation

Modulus

 [9 - 16384]

Frequency per Channel (Fs) 12.0 MHz

Rasterized Mode

$$f_{out} = \frac{f_{clk}\Delta\theta}{M}$$



Configuration		Implementation		Detailed Implementation		Output Frequencies		Summary		Additional Summary	
Channels	Phase Increment				Phase Offset						
	HEX Value	Actual MHz		HEX Value	Actual Cycles						
1	14	(1.00000000000000000000)		0	(0.00000000000000000000)						

Parameter Selection

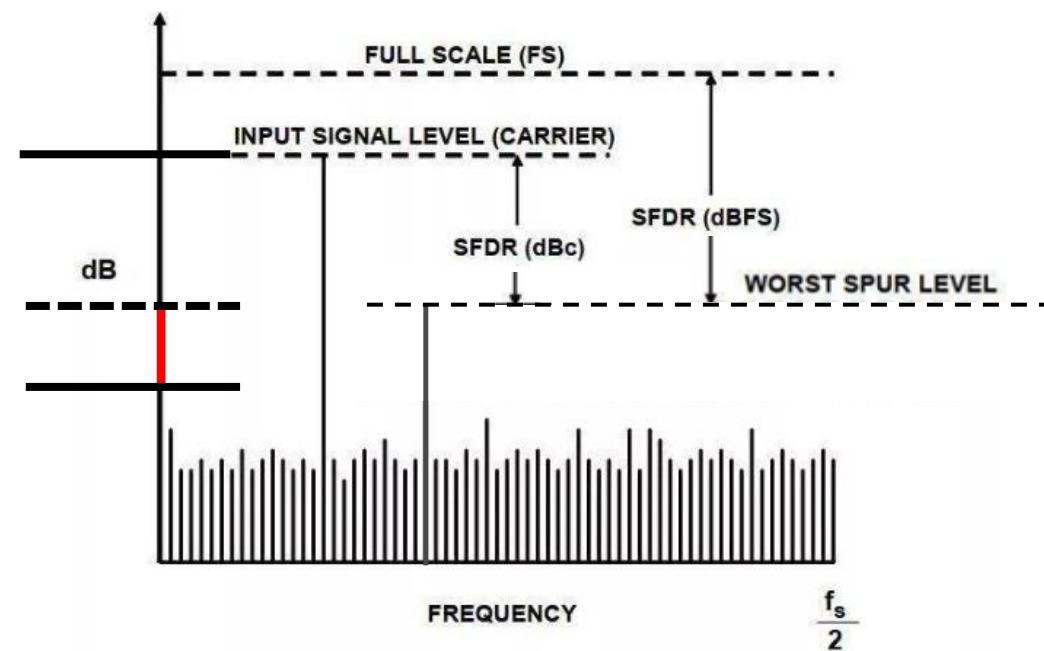
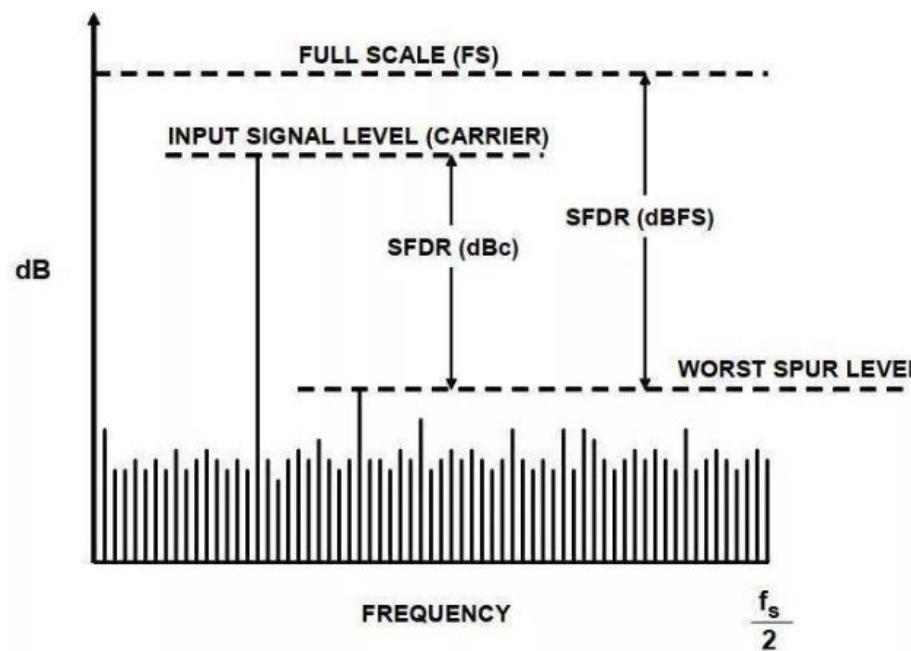
Parameter Selection System Parameters

System Parameters

Spurious Free Dynamic Range (dB) Range: 18...150

Frequency Resolution (Hz) 2.13163e-08...750000

Channel	Output Frequency (MHz)
1	0



Parameter Selection

Parameter Selection Hardware Parameters

Noise Shaping None

Hardware Parameters

Phase Width [3 - 48] →

Output Width [3 - 26] →

Phase Angle Increment Values

Channel Phase Angle Increment Values (Binary)

1	0	X
2	0	
3	0	
4	0	

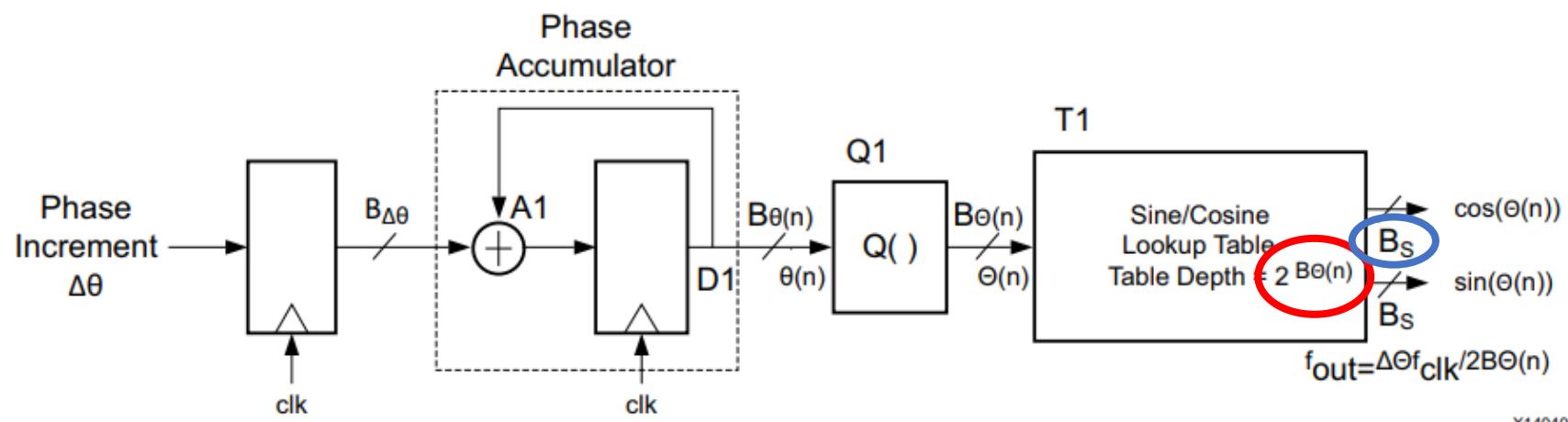
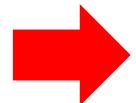


Figure 3-1: Phase Truncation DDS (Simplified View of the DDS Core)

Noise Shaping



\$17



Input Signal



\$23



15



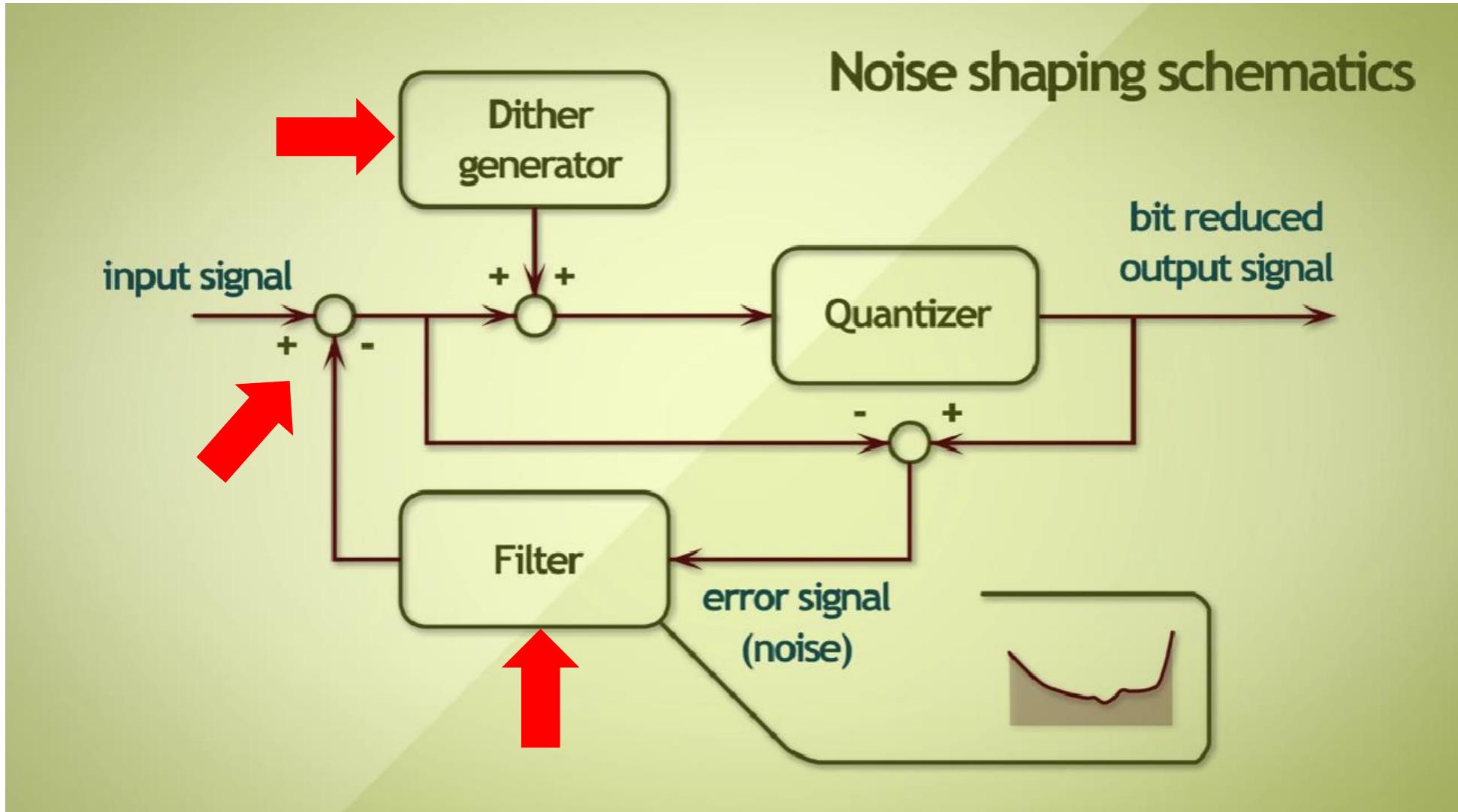
25



Output Signal

Noise

Noise Shaping



Noise Shaping



\$17



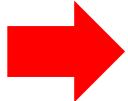
\$23



\$17



\$23



Noise Shaping



\$17



\$23



\$17



\$23



Noise Shaping

Parameter Selection

System Parameters

Spurious Free Dynamic Range (dB)

Frequency Resolution (Hz)

Noise Shaping

- Auto
- None
- Phase Dithering
- Taylor Series Corrected

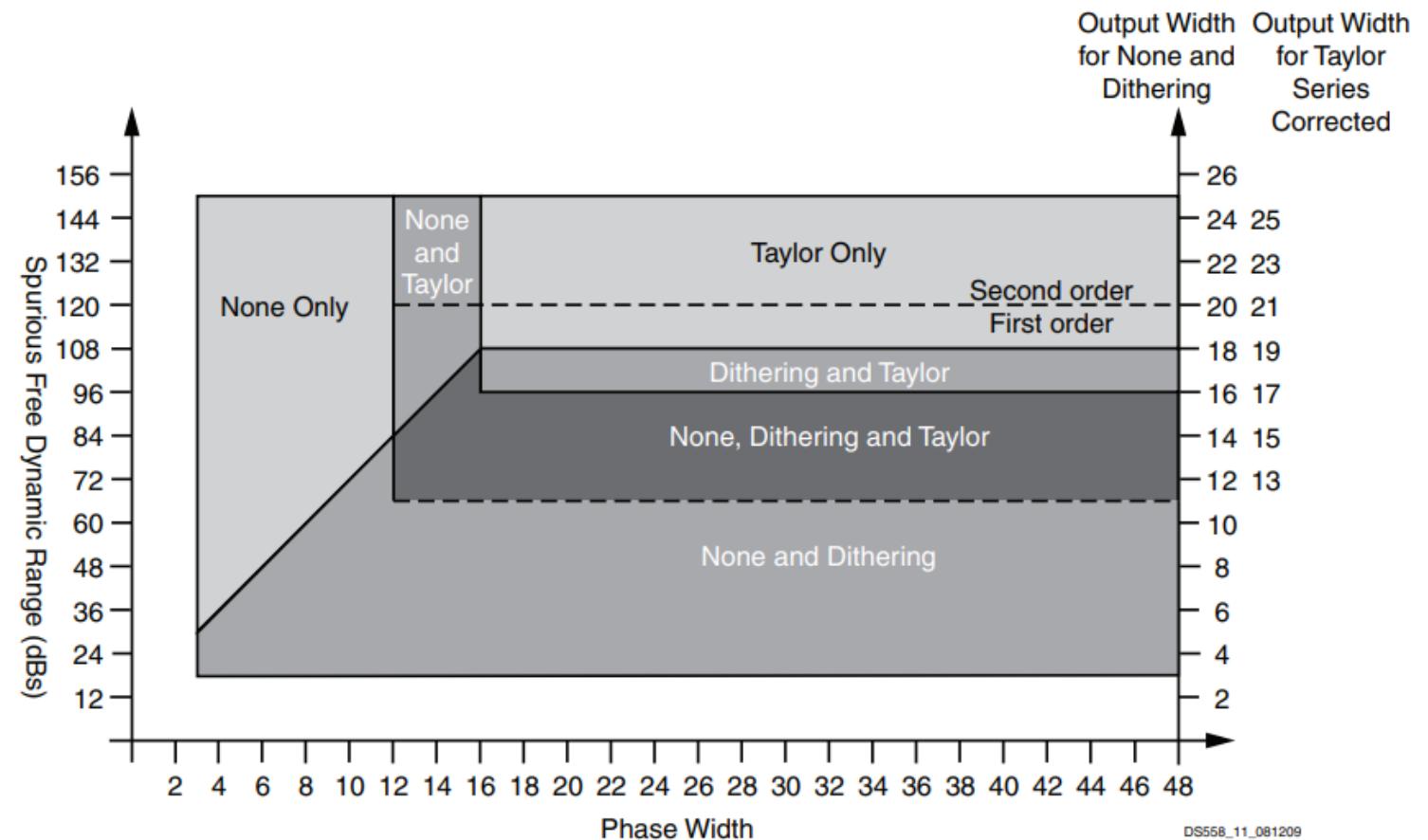


Figure 4-1: Noise Shaping Regions

Phase Increment and Offset Programmability

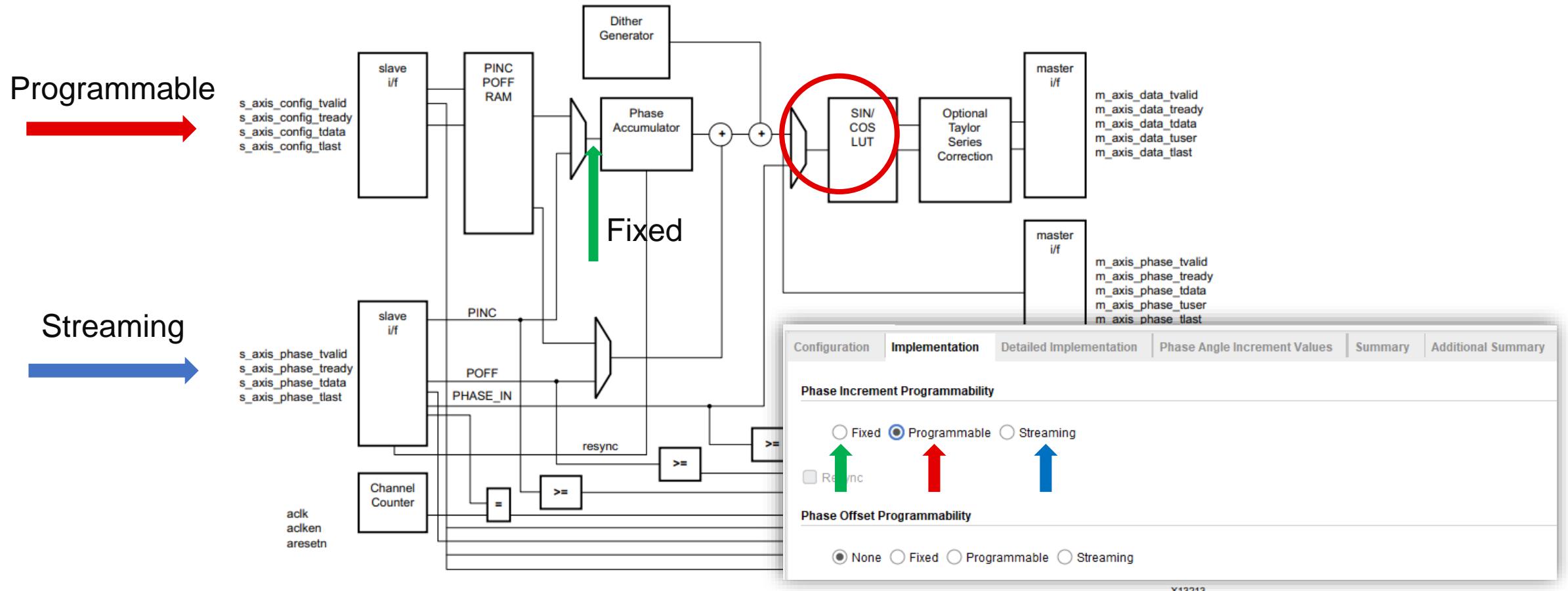


Figure 2-1: DDS Core Architecture

Config Channel Programming

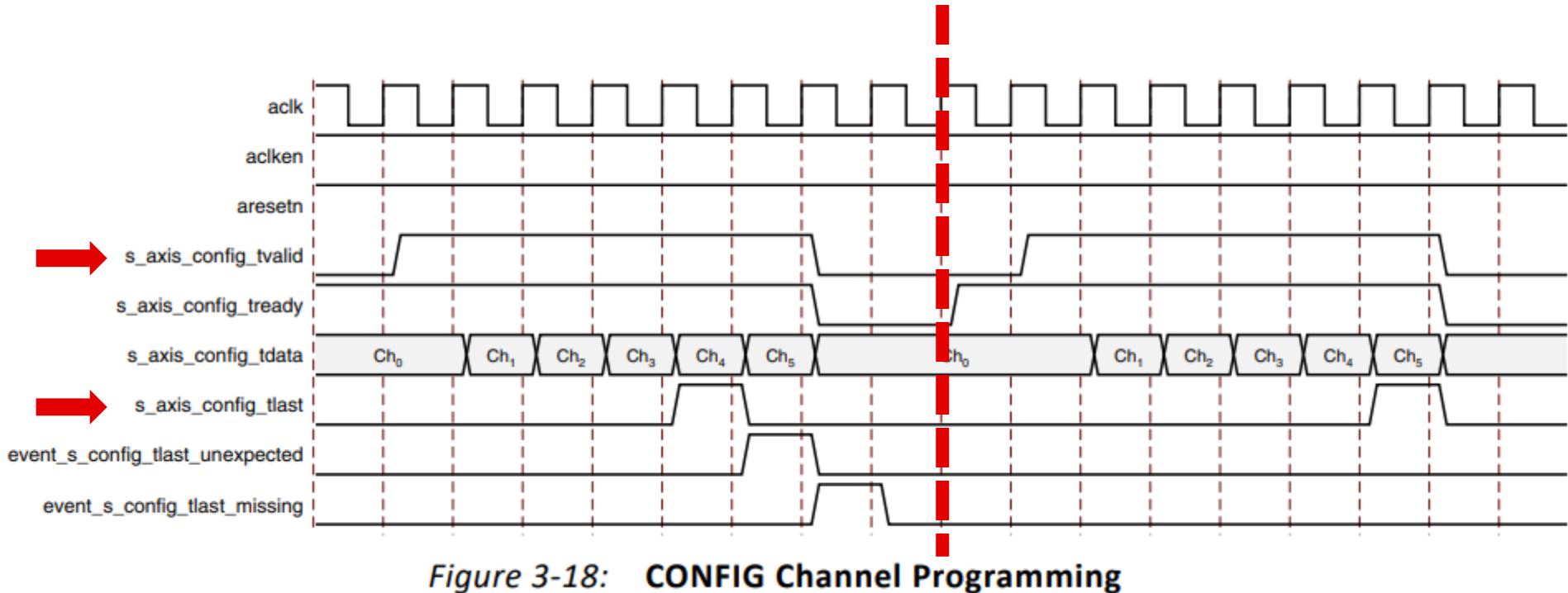


Figure 3-18: CONFIG Channel Programming

Summary

Configuration	Implementation	Detailed Implementation	Output Frequencies	Summary	Additional Summary
Output Width				8 Bits	
Channels				1	
System Clock				12 MHz	
Frequency per Channel (Fs)				12.0 MHz	
Noise Shaping				None (Auto)	
Memory Type				Block ROM (Auto)	
Optimization Goal				Area (Auto)	
Phase Width				25 Bits	
Frequency Resolution				0.4 Hz	
Phase Angle Width				8 Bits	
Spurious Free Dynamic Range				45 dB	
Latency				3	
DSP48 slice				0	
BRAM (18k) count				1	

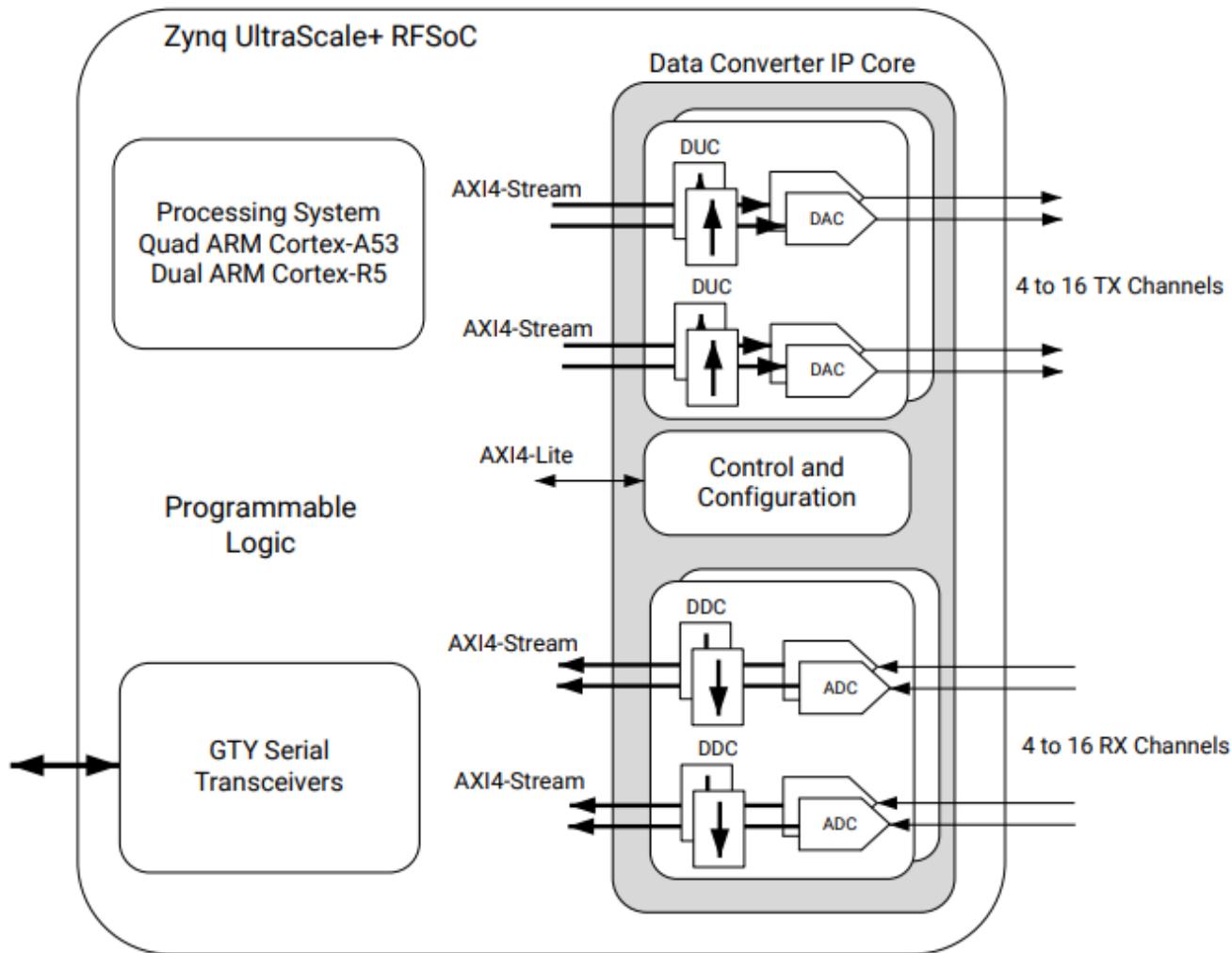
Configuration	Implementation	Detailed Implementation	Output Frequencies	Summary	Additional Summary
Phase Increment		Phase Offset			
Channels	HEX Value	Actual MHz	HEX Value	Actual Cycles	
	1	(1.00000000000000000000000000000000)	0	(0.00000000000000000000000000000000)	
2	0	(0.00000000000000000000000000000000)	0	(0.00000000000000000000000000000000)	



Data Converter

RF Data Converter Overview

Figure 1: Zynq® UltraScale+™ RFSoC RF Data Converter IP Core in Zynq UltraScale+ RFSoC (Gen 1/Gen 2/Gen 3)



X19532-062819

RF Data Converter Overview

Figure 2: RF-ADC Tile Structure

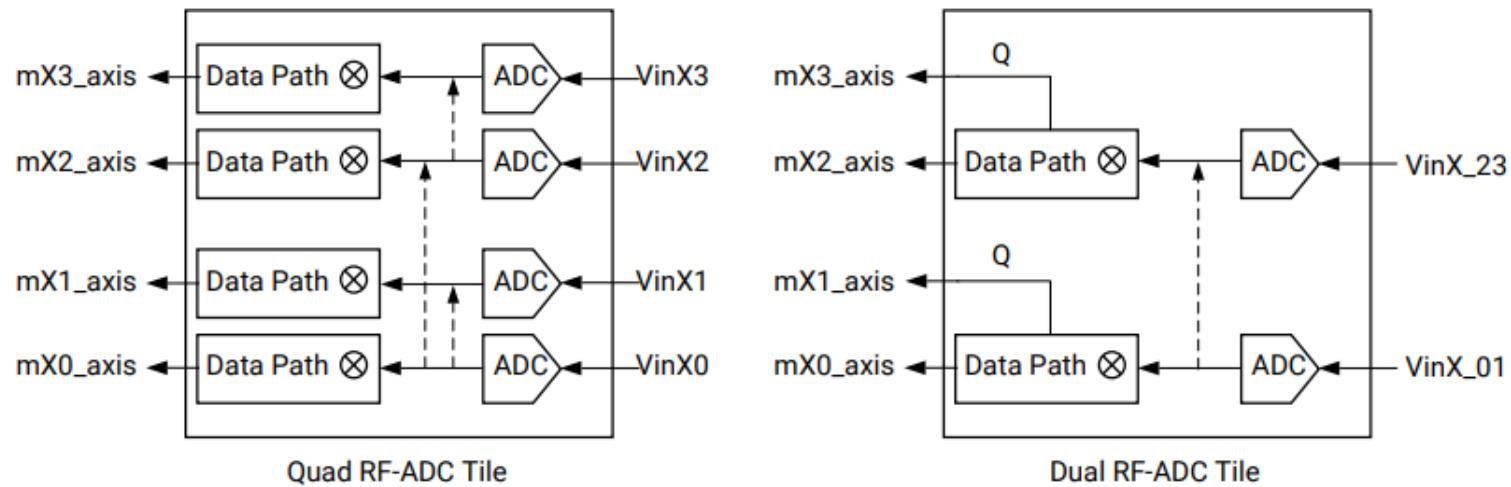
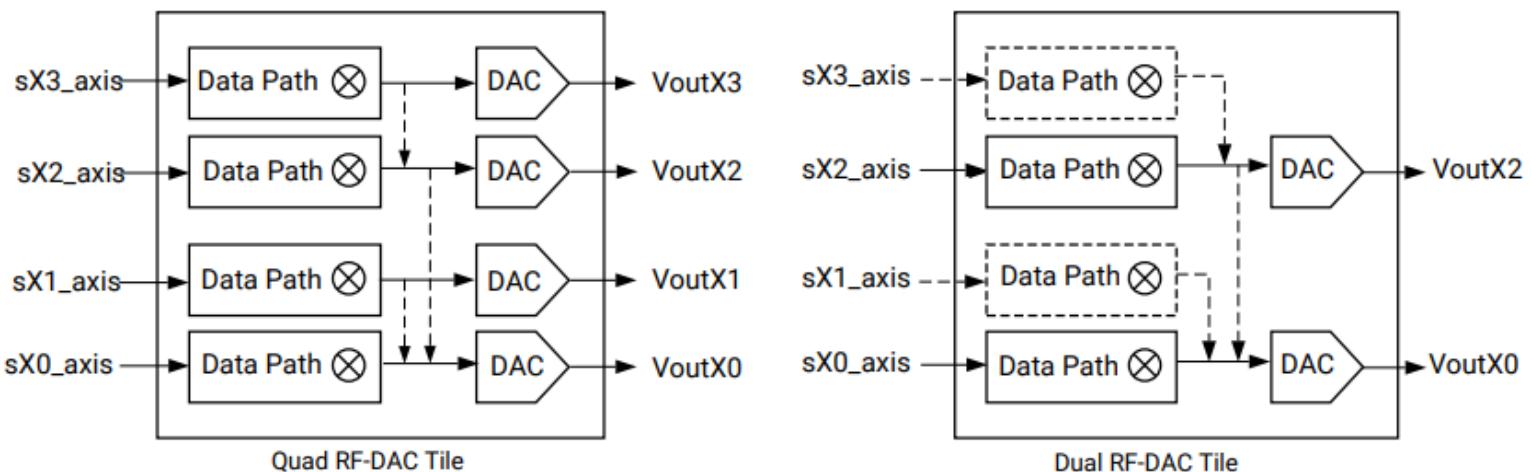
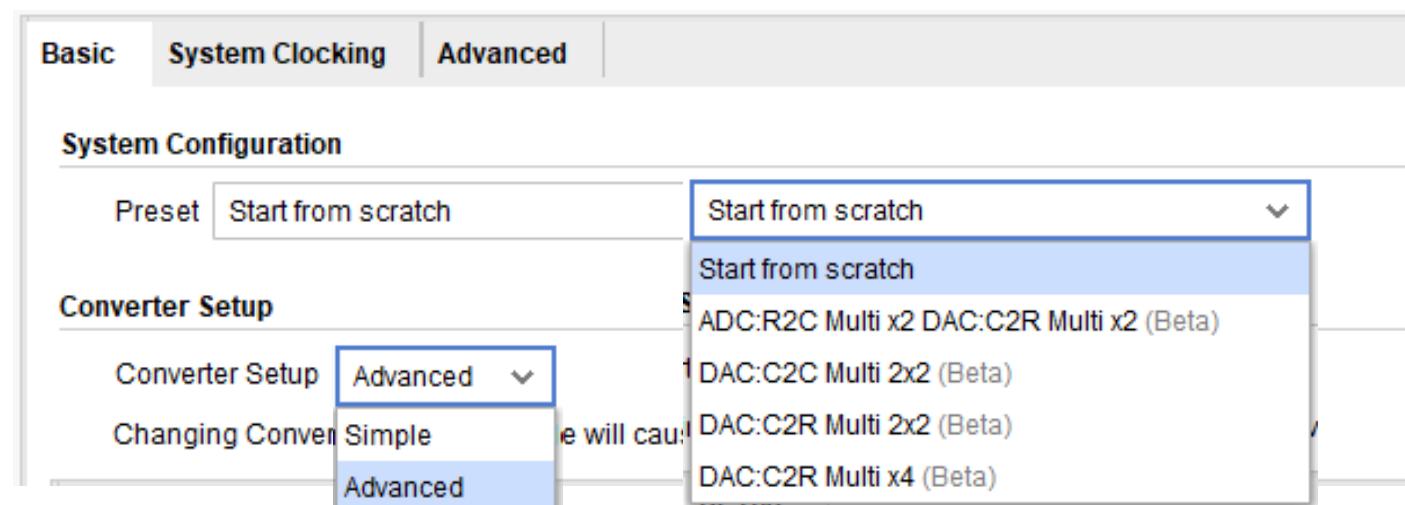
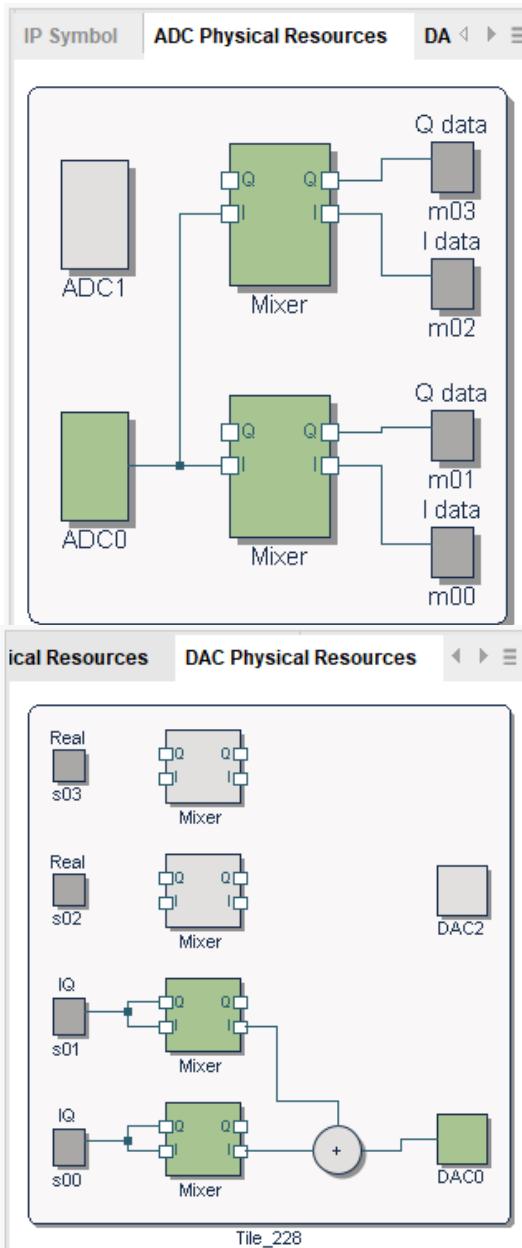


Figure 3: RF-DAC Tile Structure



RF Data Converter Overview



Converter Configuration

Multi Tile Sync

Enable Multi Tile Sync

Converter Band Mode

Band **Single**

Single
Multi x2(pair 01)

Link Coupling

Link Coupling **AC**

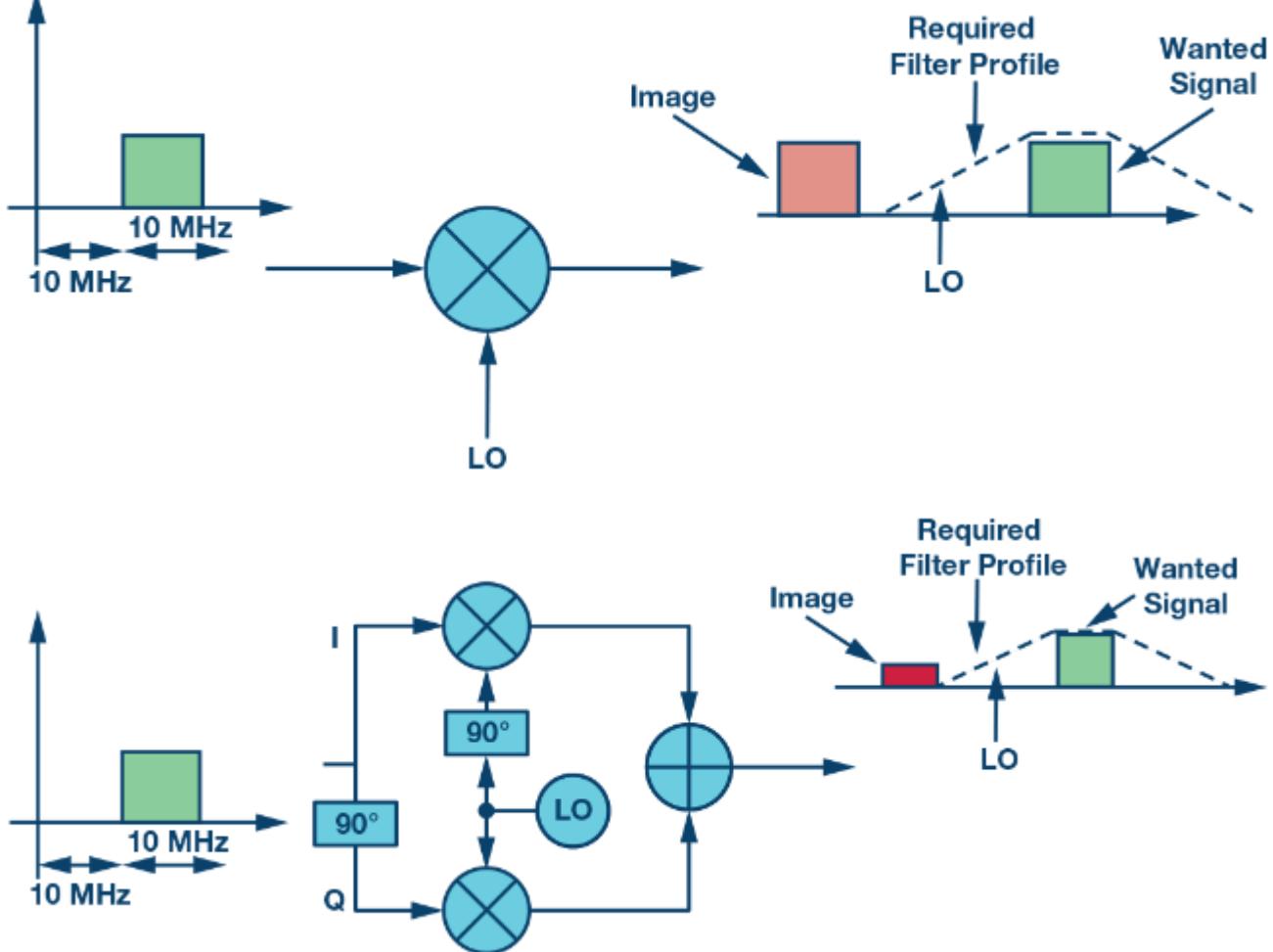
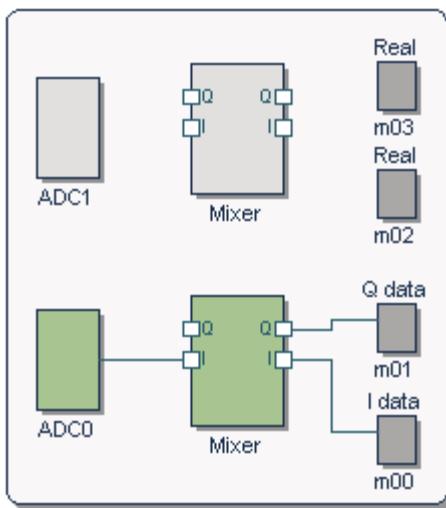
AC
DC

Converter Configuration

In-Phase (0°)

Quadrature(90°)

I/Q Mixer



Link Coupling

Multi Tile Sync

Enable Multi Tile Sync

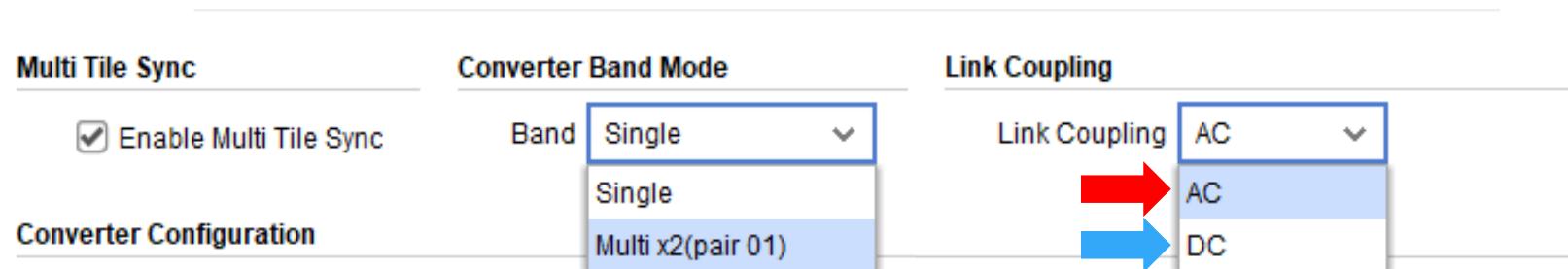
Converter Configuration

Band Single ▾

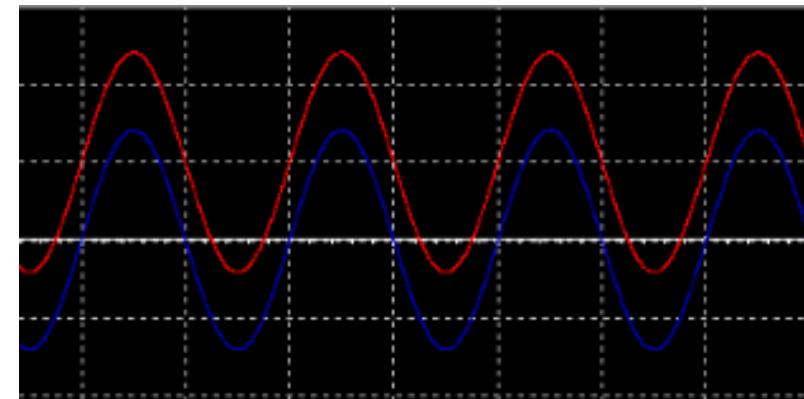
- Single
- Multi x2(pair 01)

Link Coupling AC ▾

- AC
- DC



$$v(t) = \underline{V \sin(wt + \varphi)} + 5$$



Converter Configuration

Converter Configuration

ADC 0

Enable ADC Invert Q Output

Dither

Enable TDD Real Time Ports: Off

Data Settings

Digital Output Data: Real
Decimation Mode: 1x
Samples per AXI4-Stream Cycle: 8

Required AXI4-Stream clock: 250.000 MHz

Observation Channel

Mixer Settings

Mixer Type: Coarse
Mixer Mode: Real->Real
Frequency: 0

Analog Settings

Nyquist Zone: Zone 1
Calibration Mode: Mode2

IF

RF difference

RF sum

LO

TRx Slot: RX | TX | RX | TX

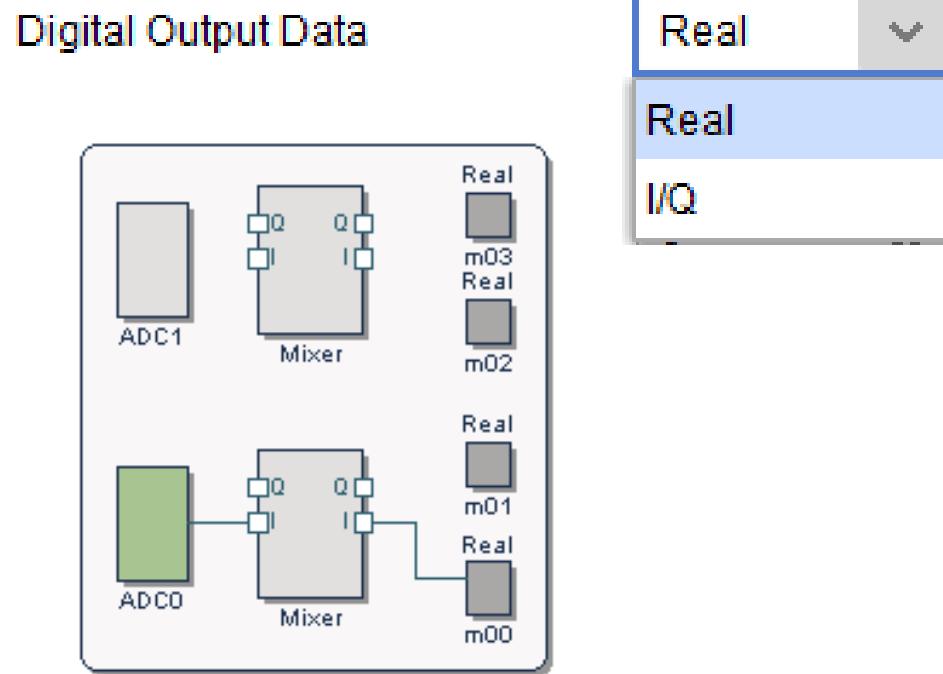
RF-DAC (Power Saving): Power Down | TX | Power Down | TX
Data=0 | Data=0

RF-ADC (Power Saving): RX | Power Down | RX | Power Down
Data=0 | Data=0

Data Settings

Data Settings

Digital Output Data	Real
Decimation Mode	1x
Samples per AXI4-Stream Cycle	8
Required AXI4-Stream clock	250.000 MHz



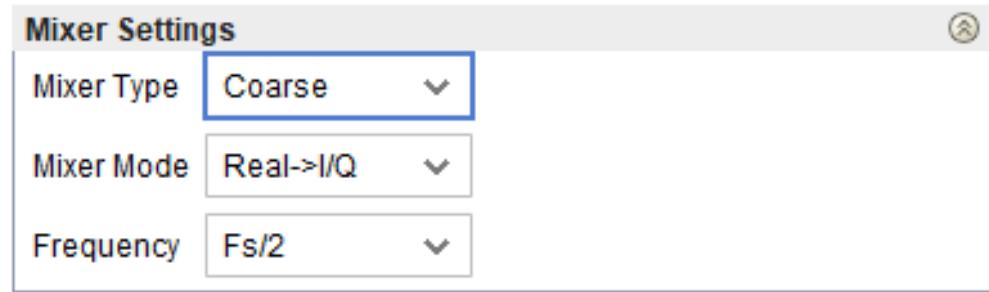
Decimation Mode

1x
4x
5x
6x
8x
10x
12x
16x
20x
24x
40x

Samples per AXI4-Stream Cycle

8
4
5
6
7
8
9
10
11
12

Mixer Settings



Mixer Type	Coarse	Mixer Type	Fine
Frequency	Fs/2	NCO Frequency (GHz)	-10~10
	<ul style="list-style-type: none">Fs/2Fs/4-Fs/4	NCO Phase	180 -180

Analog Settings



DAC Converter Configuration

DAC Tile 228 DAC Tile 229 DAC Tile 230 DAC Tile 231

Multi Tile Sync

Enable Multi Tile Sync

Coupling Mode

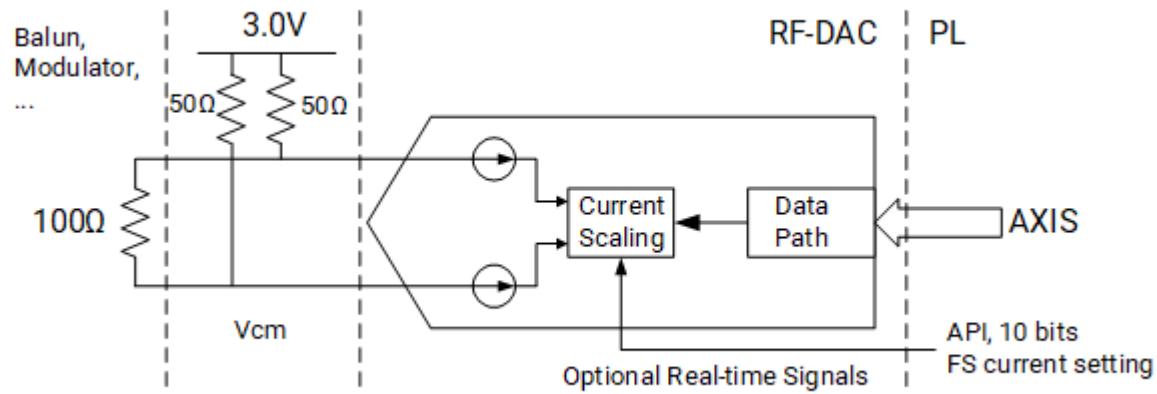
Link Coupling

Converter Band Mode

Band

Variable Output Current

Output Power [2.25 - 40.5]



X23175042120

DAC Converter Configuration

DUC Configuration

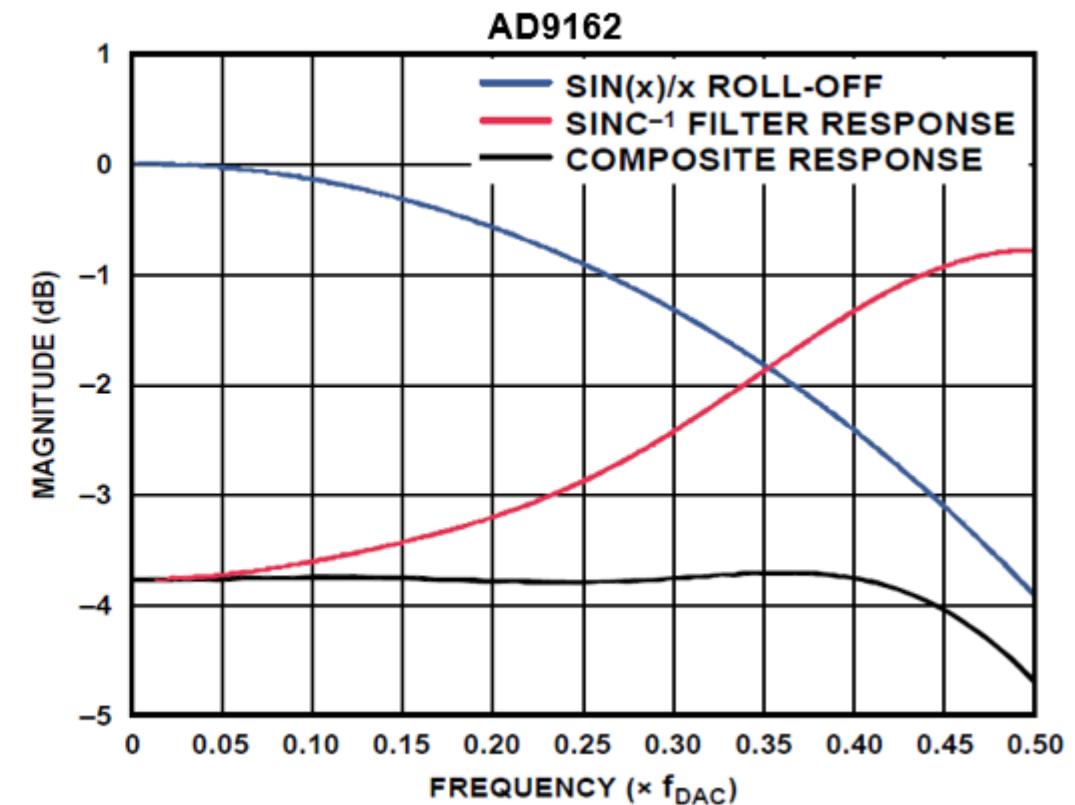
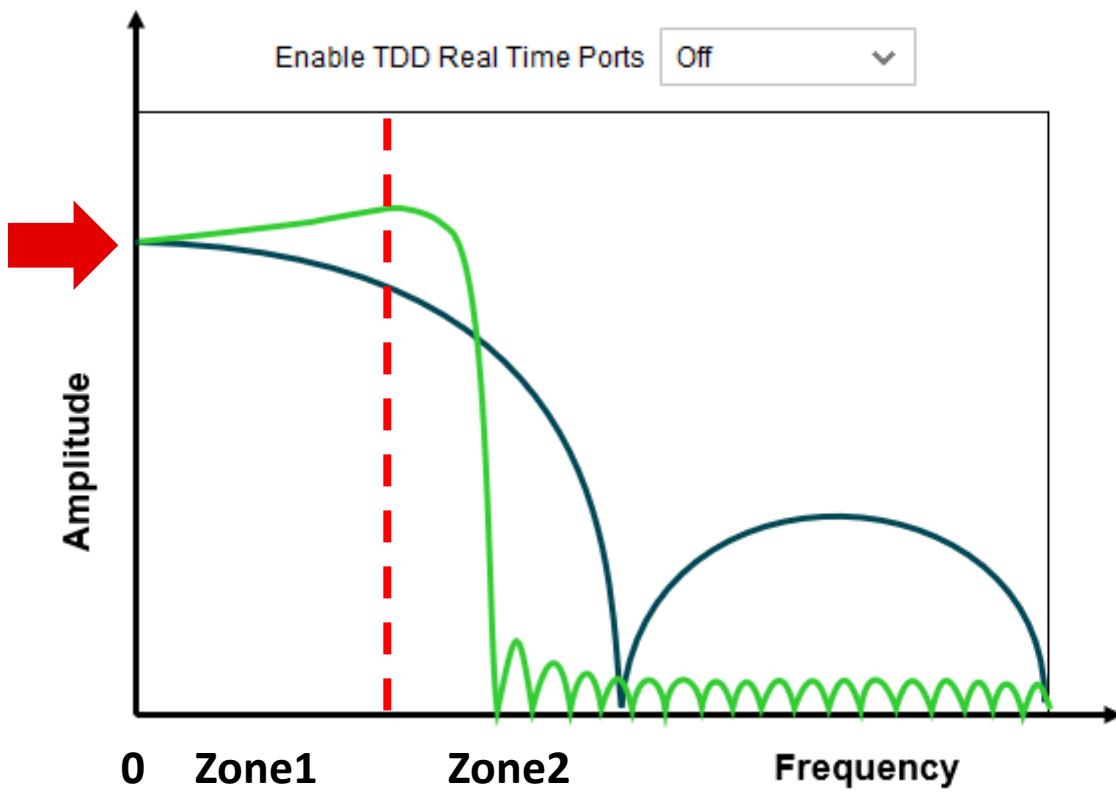
DUC 0

Invert Q Output

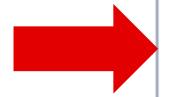
Inverse Sinc Filter

Enable TDD Real Time Ports

Off



Interpolation



Data Settings

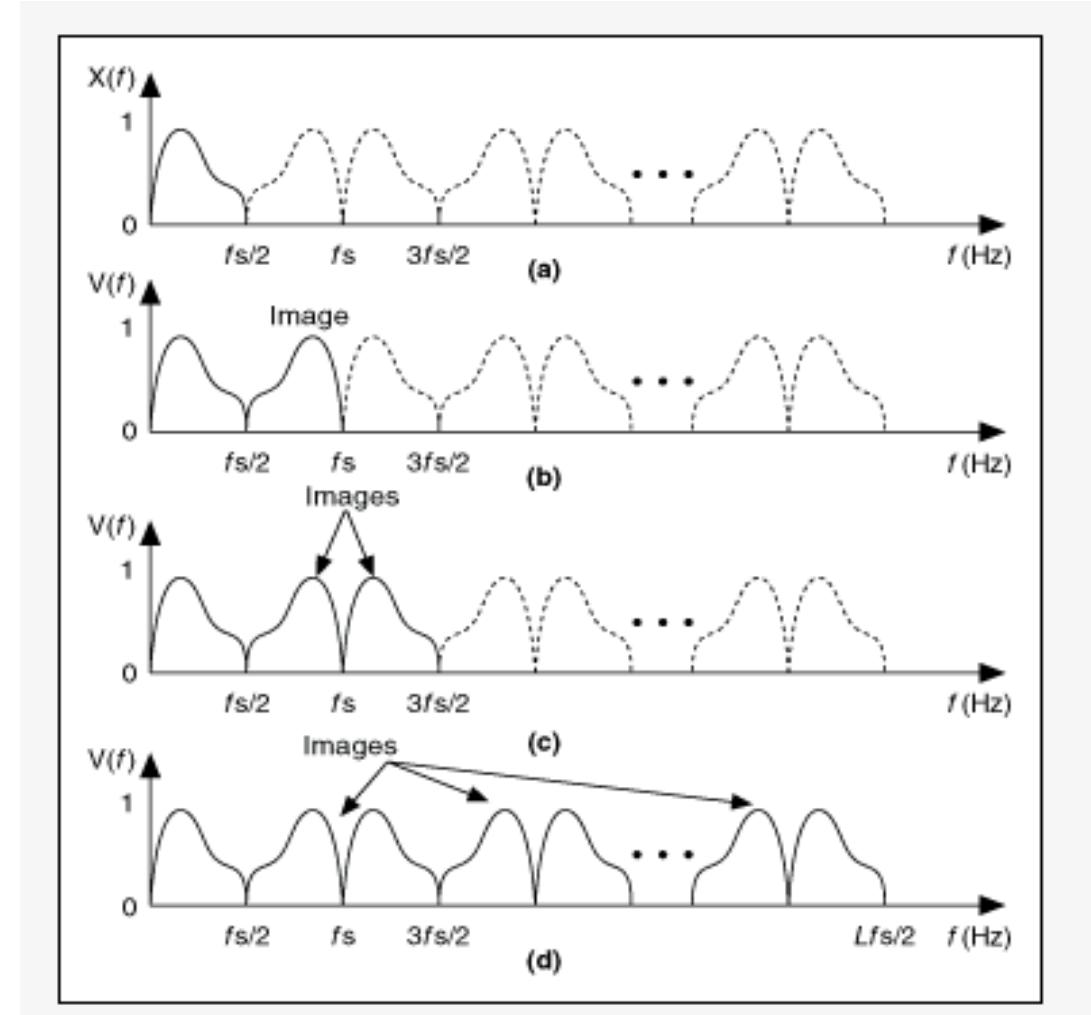
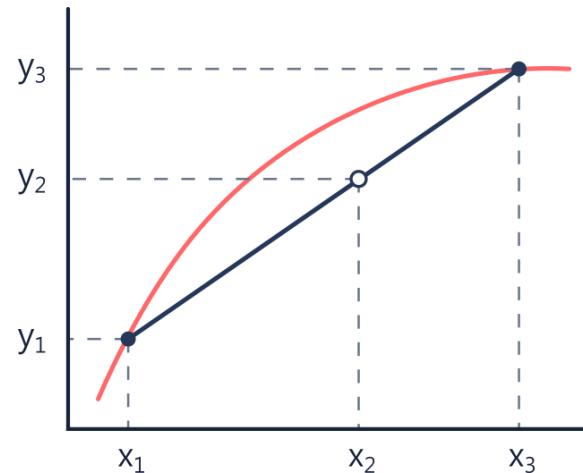
Analog Output Data: Real

Interpolation Mode: 8x

Samples per AXI4-Stream Cycle: 1

Required AXI4-Stream clock: 184.320 MHz

Datapath Mode: DUC 0 to Fs/2



DAC Converter Configuration

Data Settings

Analog Output Data: Real

Interpolation Mode: 8x

Samples per AXI4-Stream Cycle: 1

Required AXI4-Stream clock: 184.320 MHz

Datapath Mode: **DUC 0 to Fs/2**

Datapath Mode

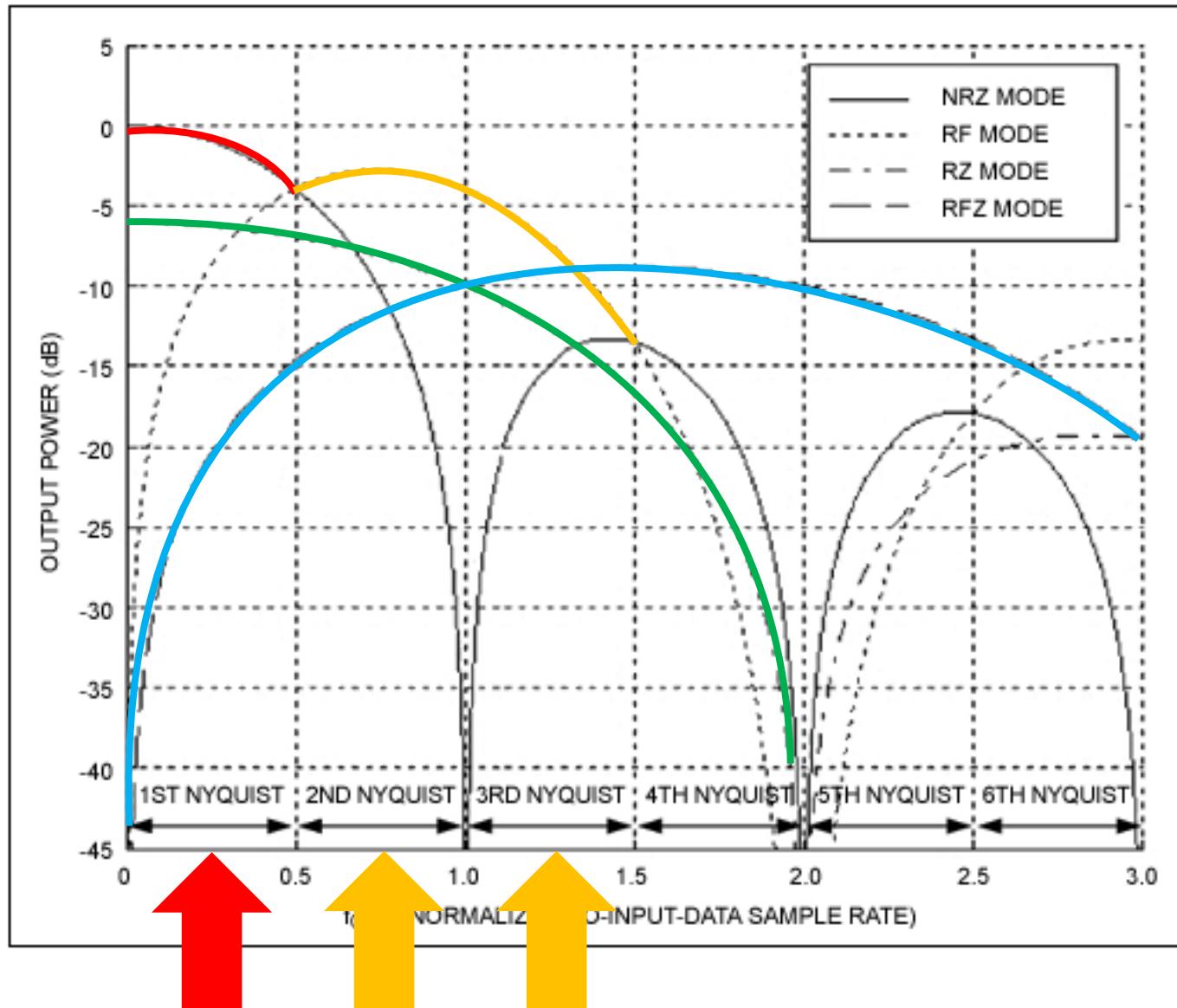
- DUC 0 to Fs/2
- DUC 0 to Fs/2**
- DUC 0 to Fs/4
- DUC Fs/4 to Fs/2
- No DUC 0 to Fs/2



Mode ¹	Mode 1		Mode 2		Mode 3		Mode 4	
Short Name	Full Nyquist DUC		IMR Low-pass		IMR High-pass		DUC-Bypass	
IMR x2	OFF		ON		ON		OFF	
Mix-Mode	OFF	ON	OFF	ON	OFF	ON	OFF	ON
Usable Bandwidth (F_s)	0-0.45	0.55-0.95	0-0.2	0.8-0.95	0.3-0.45	0.55-0.7	0-0.45	0.55-0.95
Reconstruction Filter	Low-pass	Band-pass	Low-pass	Band-pass	Low-pass	Band-pass	Low-pass	Band-pass

The maximum sample rate changes depending on modes; the Mode 1 supports lower maximum sample rate than others. See *Zynq UltraScale+ RFSoC Data Sheet: DC and AC Switching Characteristics* (DS926).

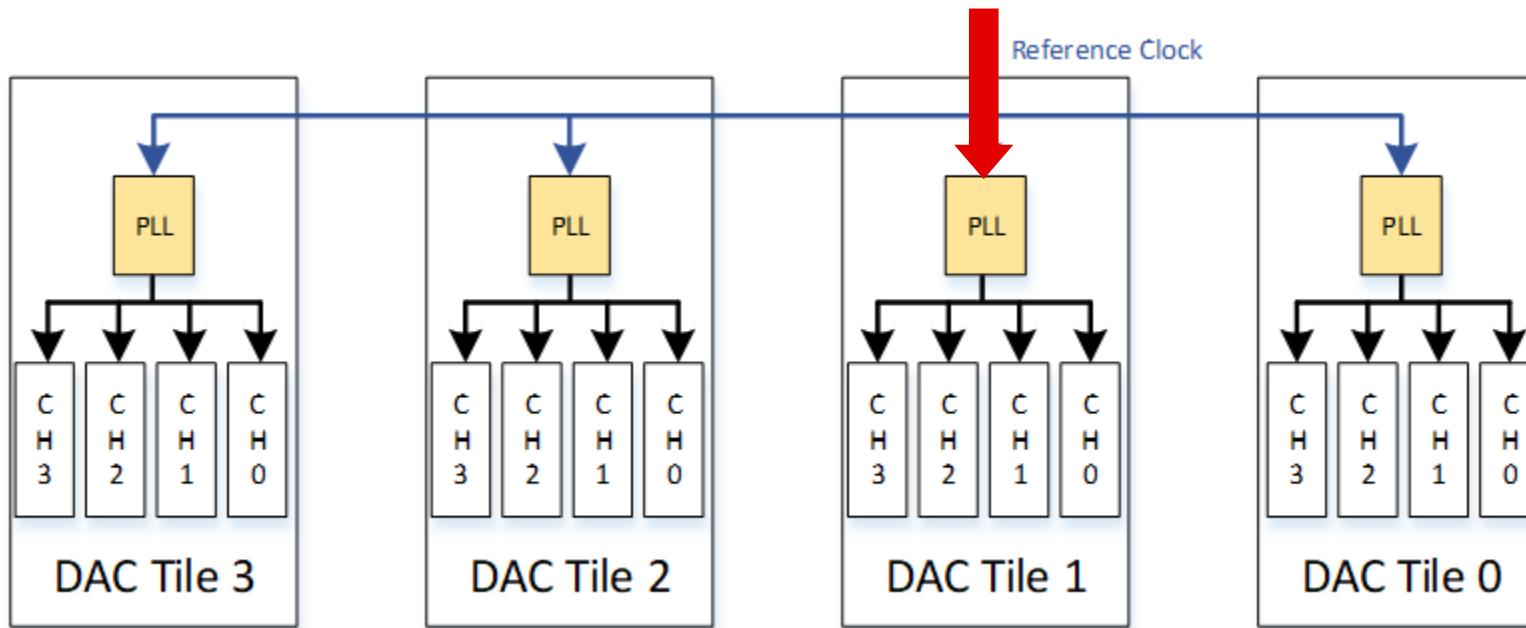
Interpolation



System Clocking

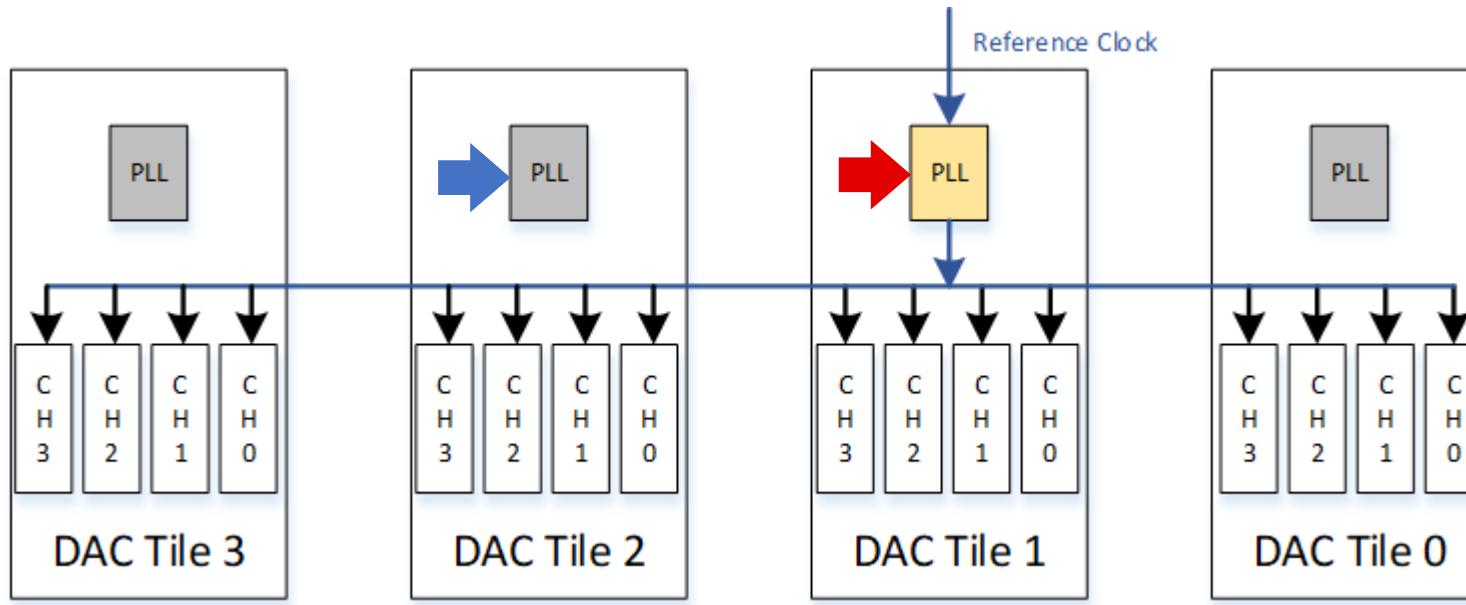
AXI4-Lite Interface Configuration									
Tile Clocking Settings									
Tile	Sampling Rate (GSPS)	Max Fs (GSPS)	PLL	Reference Clock (MHz)	PLL Ref Clock (MHz)	Ref Clock Divider	Fabric Clock (MHz)	Clock Out (MHz)	
ADC 224	2.0	5.000	<input type="checkbox"/>	2000.000	-	1	0.0	15.625	
ADC 225	2.0	5.000	<input type="checkbox"/>	2000.000	-	1	0.0	15.625	
ADC 226	1.47456 <input checked="" type="checkbox"/>	5.000	<input checked="" type="checkbox"/>	184.320	184.32	1	184.320	11.520	
ADC 227	2.0	5.000	<input type="checkbox"/>	2000.000	-	1	0.0	15.625	
DAC 228	1.47456 <input checked="" type="checkbox"/>	7.000	<input checked="" type="checkbox"/>	184.320	184.32	1	184.320	184.320	
DAC 229	6.4	10.000	<input type="checkbox"/>	6400.000	-	1	0.0	50.000	
DAC 230	6.4	10.000	<input type="checkbox"/>	6400.000	-	1	0.0	50.000	
DAC 231	6.4	10.000	<input type="checkbox"/>	6400.000	-	1	0.0	50.000	

Distribute Clock Mode (Input Refclk)



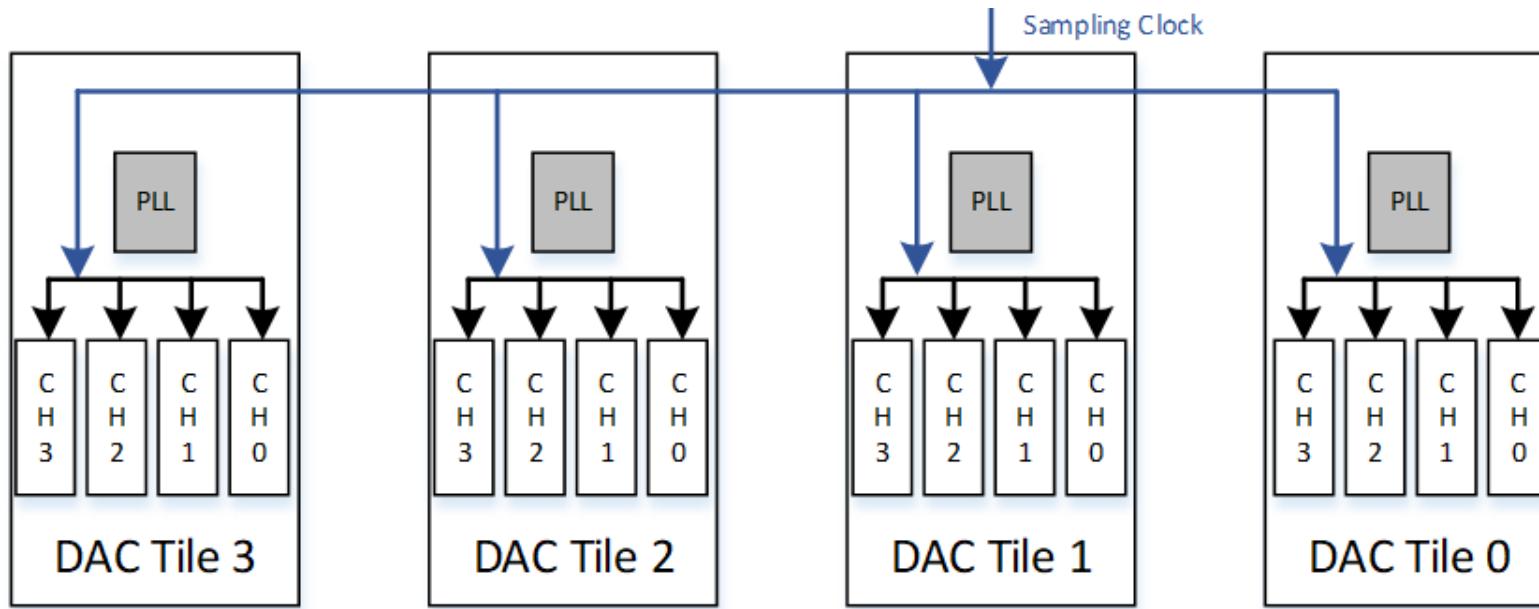
DAC 228	1.47456	<input checked="" type="checkbox"/>	7.000	<input checked="" type="checkbox"/>	149.955	<input type="button" value="▼"/>	149.955	<input type="button" value="▼"/>	1	<input type="button" value="▼"/>	184.320	<input type="button" value="▼"/>	11.520	<input type="button" value="▼"/>	Tile228	<input type="button" value="▼"/>	Input Refclk	<input type="button" value="▼"/>
DAC 229	1.47456	<input checked="" type="checkbox"/>	7.000	<input checked="" type="checkbox"/>	149.955	<input type="button" value="▼"/>	149.955	<input type="button" value="▼"/>	1	<input type="button" value="▼"/>	184.320	<input type="button" value="▼"/>	11.520	<input type="button" value="▼"/>	Tile228	<input type="button" value="▼"/>	Off	<input type="button" value="▼"/>
DAC 230	1.47456	<input checked="" type="checkbox"/>	7.000	<input checked="" type="checkbox"/>	149.955	<input type="button" value="▼"/>	149.955	<input type="button" value="▼"/>	1	<input type="button" value="▼"/>	184.320	<input type="button" value="▼"/>	11.520	<input type="button" value="▼"/>	Tile228	<input type="button" value="▼"/>	Off	<input type="button" value="▼"/>
DAC 231	1.47456	<input checked="" type="checkbox"/>	7.000	<input checked="" type="checkbox"/>	149.955	<input type="button" value="▼"/>	149.955	<input type="button" value="▼"/>	1	<input type="button" value="▼"/>	184.320	<input type="button" value="▼"/>	11.520	<input type="button" value="▼"/>	Tile228	<input type="button" value="▼"/>	Off	<input type="button" value="▼"/>

Distribute Clock Mode (PLL output)



DAC 228	1.47456	<input checked="" type="checkbox"/>	7.000	<input checked="" type="checkbox"/>	102.876	-	102.876	1	-	184.320	11.520	-	Tile228	-	PLL output	-
DAC 229	1.47456	<input checked="" type="checkbox"/>	7.000	<input type="checkbox"/>	1474.560	-	-	1	-	491.520	11.520	-	Tile228	-	Off	-
DAC 230	1.47456	<input checked="" type="checkbox"/>	7.000	<input checked="" type="checkbox"/>	102.876	-	102.876	1	-	184.320	11.520	-	Tile230	-	PLL output	-
DAC 231	1.47456	<input checked="" type="checkbox"/>	7.000	<input type="checkbox"/>	1474.560	-	-	1	-	491.520	11.520	-	Tile230	-	Off	-

Distribute Clock Mode (off)



DAC 228	1.47456	<input checked="" type="checkbox"/>	7.000	<input type="checkbox"/>	1474.560	<input type="button" value="▼"/>	-	<input type="checkbox"/>	1	<input type="button" value="▼"/>	184.320	<input type="button" value="▼"/>	11.520	<input type="button" value="▼"/>	Tile228	<input type="button" value="▼"/>	Off	<input type="button" value="▼"/>
DAC 229	1.47456	<input type="checkbox"/>	10.000	<input type="checkbox"/>	1474.560	<input type="button" value="▼"/>	-	<input type="checkbox"/>	1	<input type="button" value="▼"/>	0.0	<input type="button" value="▼"/>	11.520	<input type="button" value="▼"/>	Tile229	<input type="button" value="▼"/>	Off	<input type="button" value="▼"/>
DAC 230	1.47456	<input checked="" type="checkbox"/>	7.000	<input type="checkbox"/>	1474.560	<input type="button" value="▼"/>	-	<input type="checkbox"/>	1	<input type="button" value="▼"/>	184.320	<input type="button" value="▼"/>	11.520	<input type="button" value="▼"/>	Tile230	<input type="button" value="▼"/>	Off	<input type="button" value="▼"/>
DAC 231	1.47456	<input type="checkbox"/>	10.000	<input type="checkbox"/>	1474.560	<input type="button" value="▼"/>	-	<input type="checkbox"/>	1	<input type="button" value="▼"/>	0.0	<input type="button" value="▼"/>	11.520	<input type="button" value="▼"/>	Tile231	<input type="button" value="▼"/>	Off	<input type="button" value="▼"/>



Thank You

