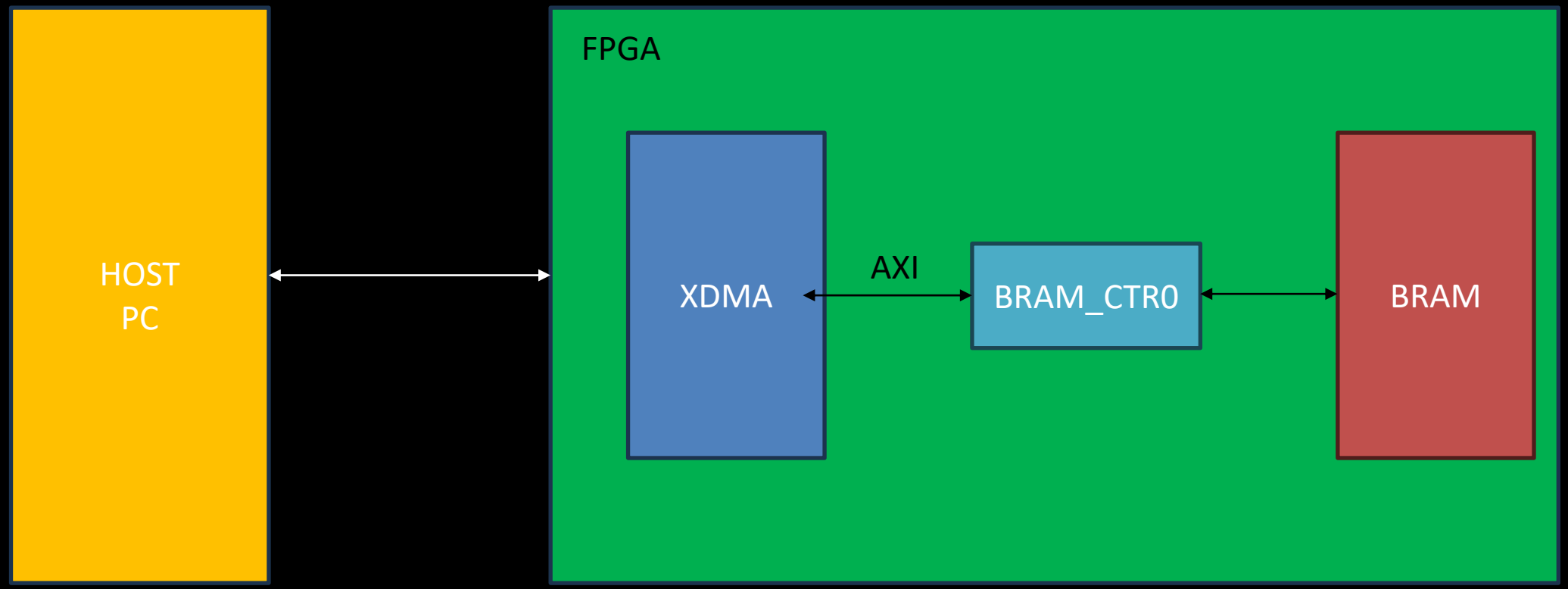
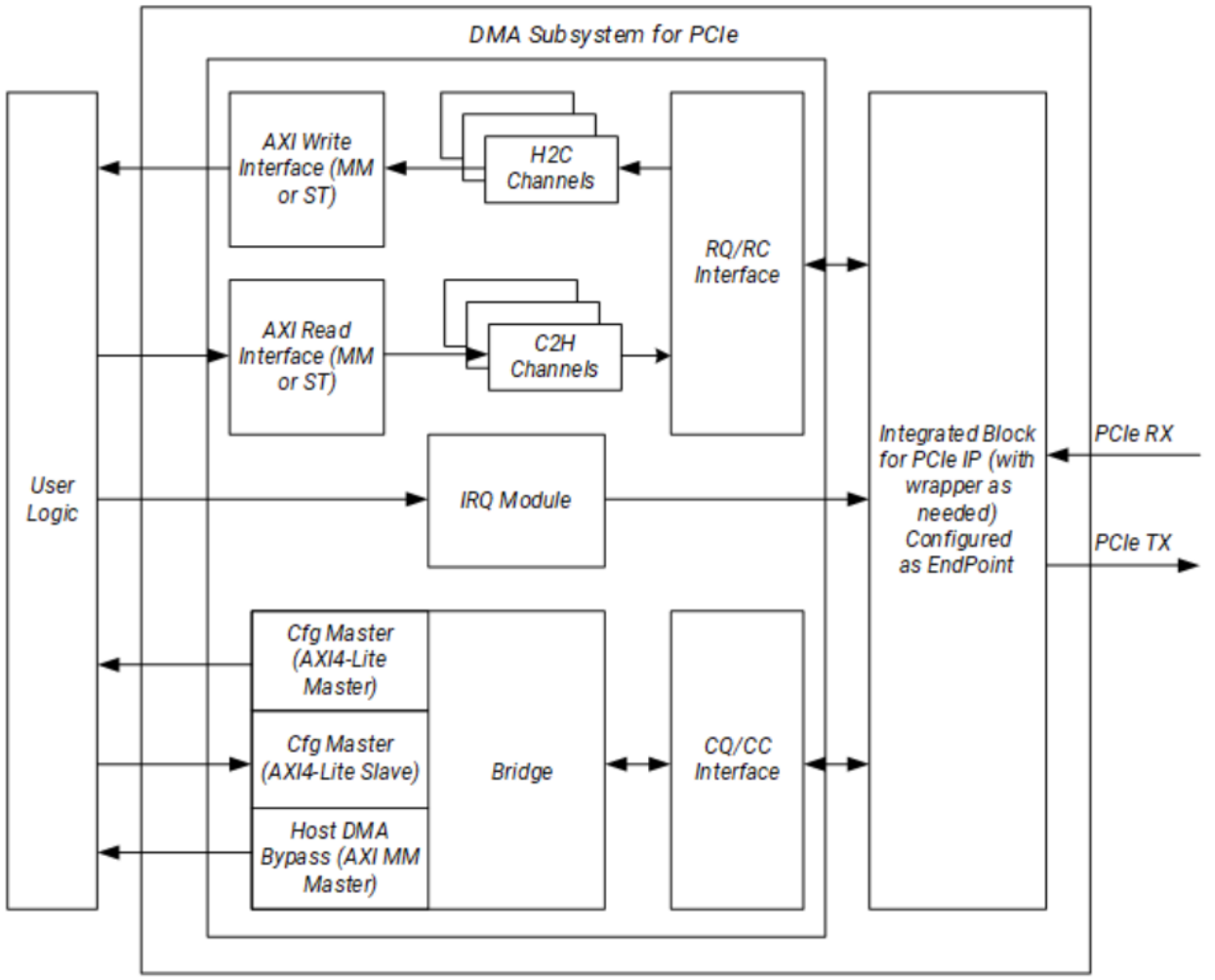
Peripheral Component Interconnect Express(Pcie) with Xilinx DMA

Block Diagram



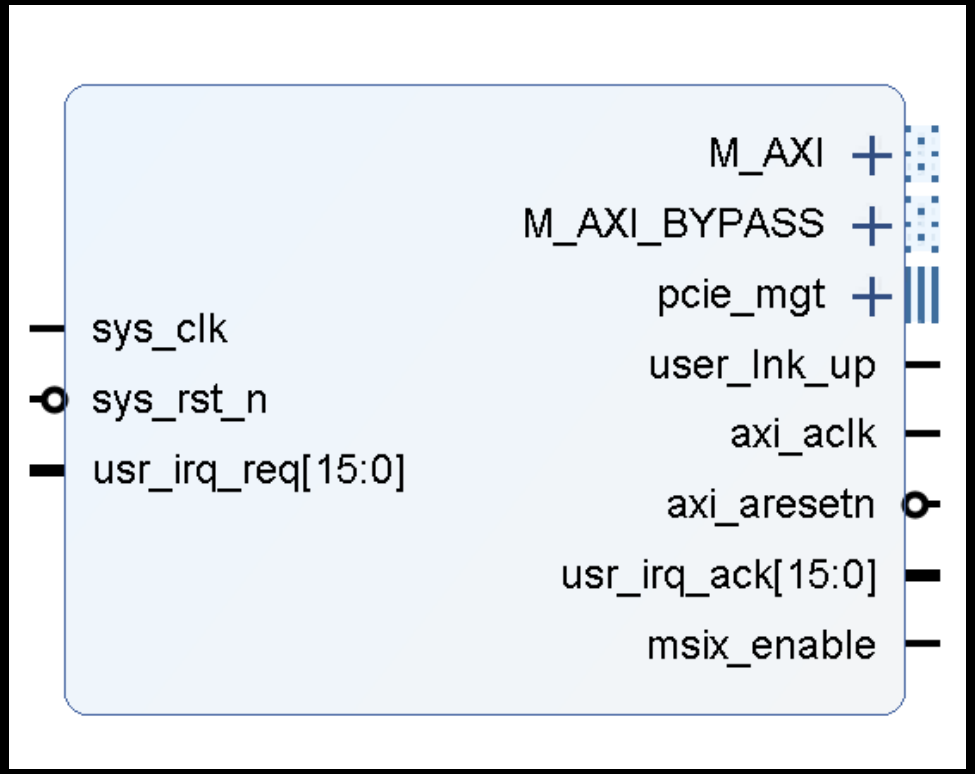
XDMA IP CORE

Figure: DMA/Bridge Subsystem for PCI Express® Overview



XDMA IP Setting

IP Port



與FPGA的User Logic走axi通信

PCIE總線

驅動PCie通信的clk&Reset

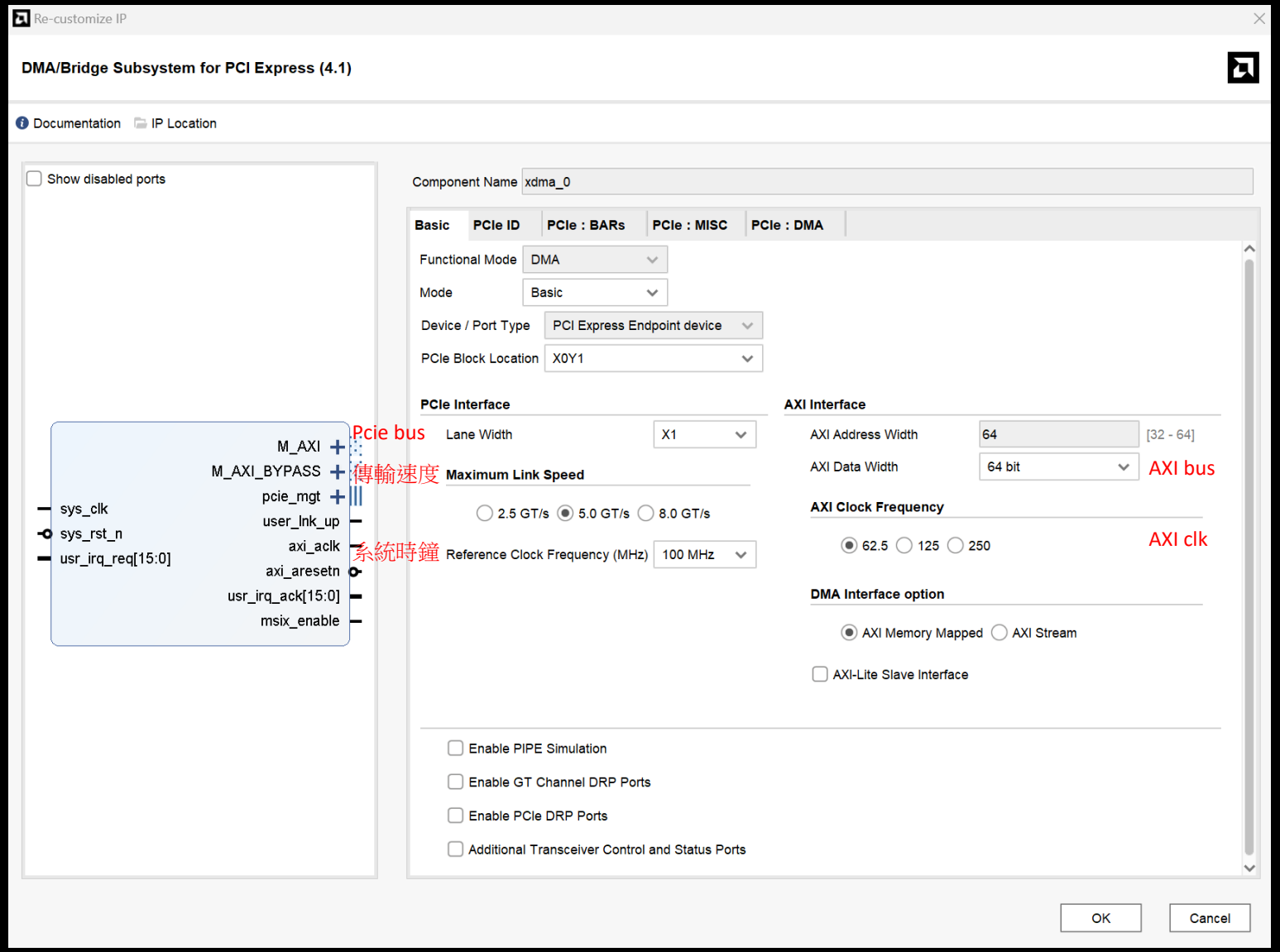
通信完成信號線

中斷請求

驅動AXI傳輸的CLK&Reset

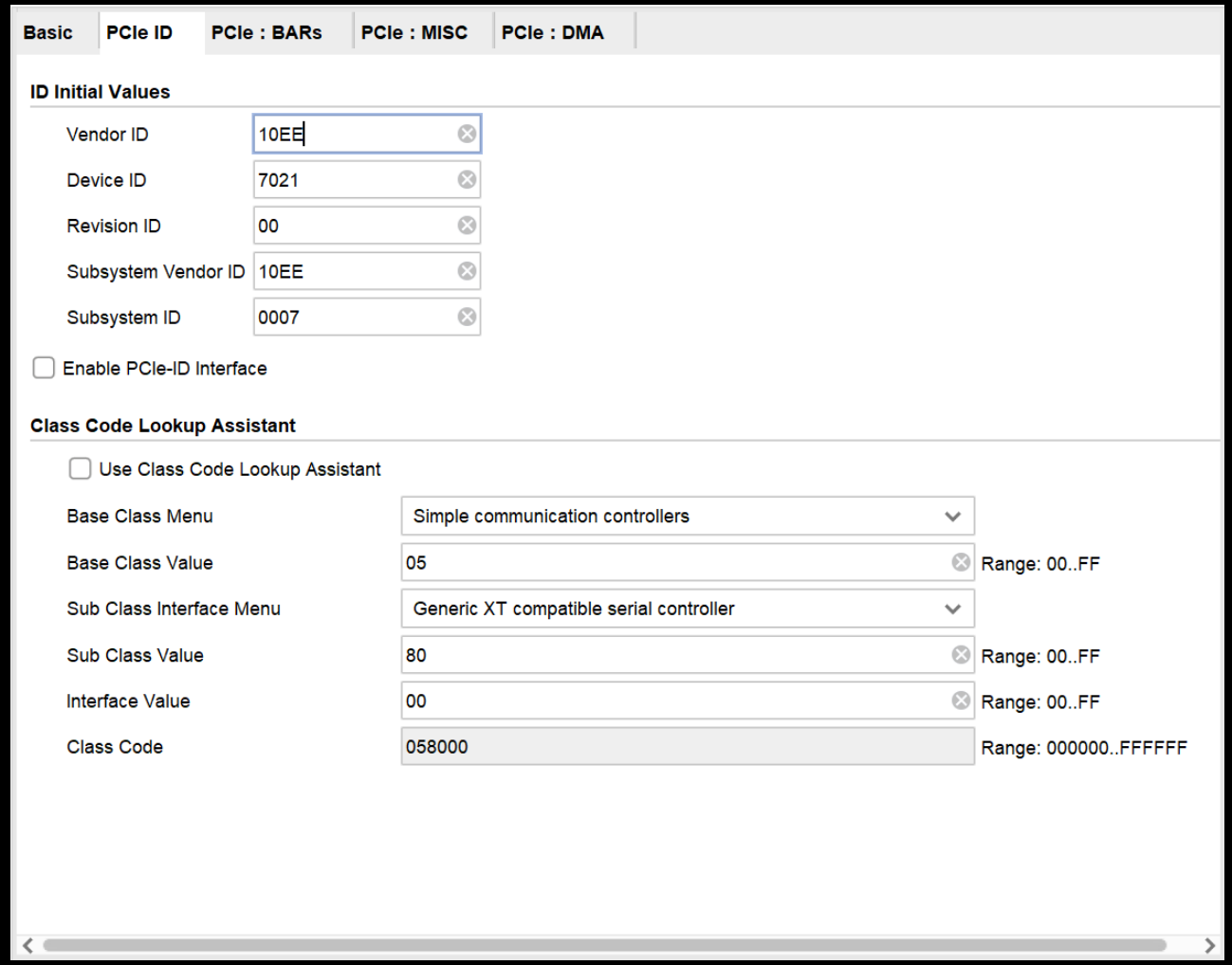
中斷響應

XDMA IP Setting



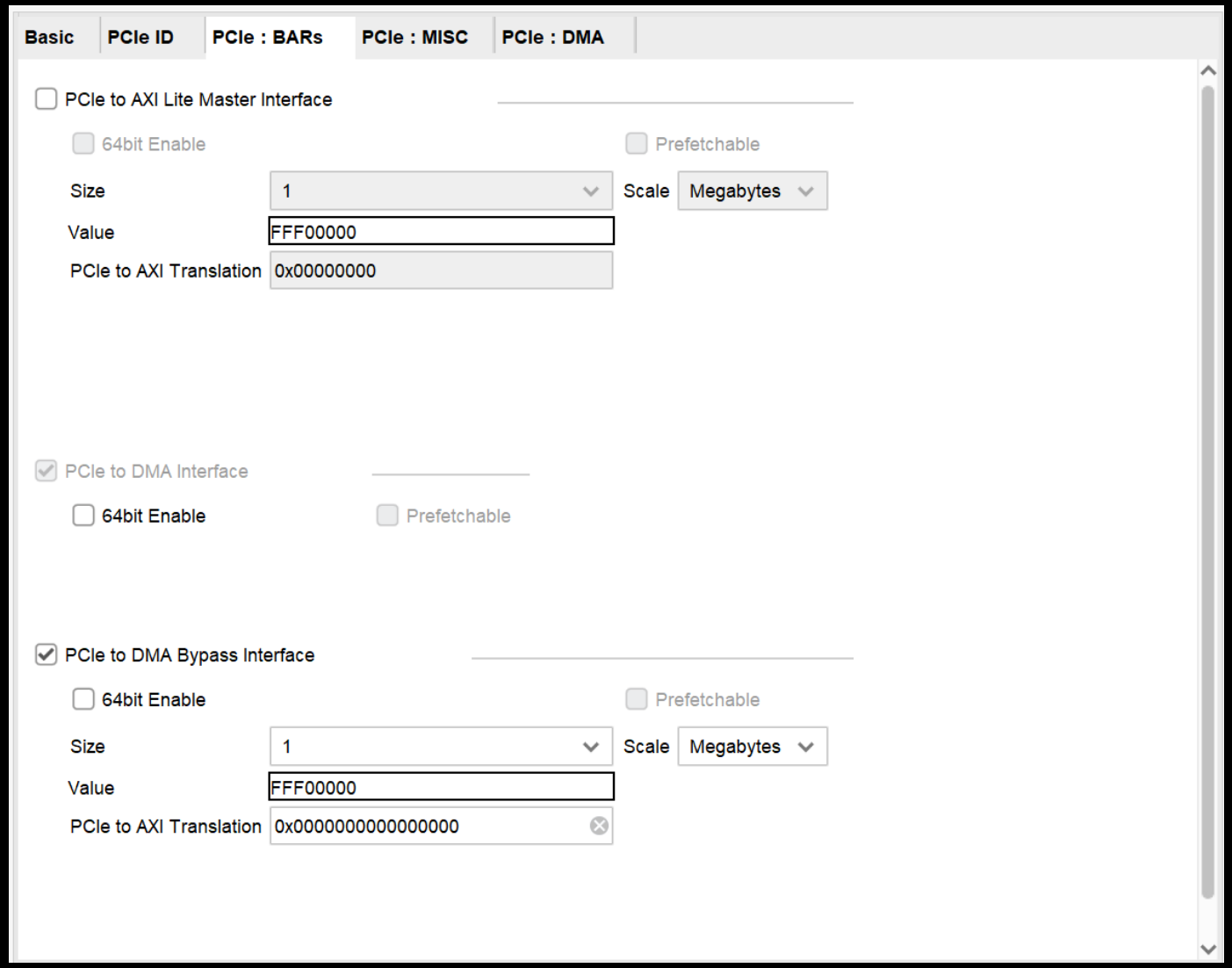
XDMA IP Setting

Pcie ID辨識 依據Device修改



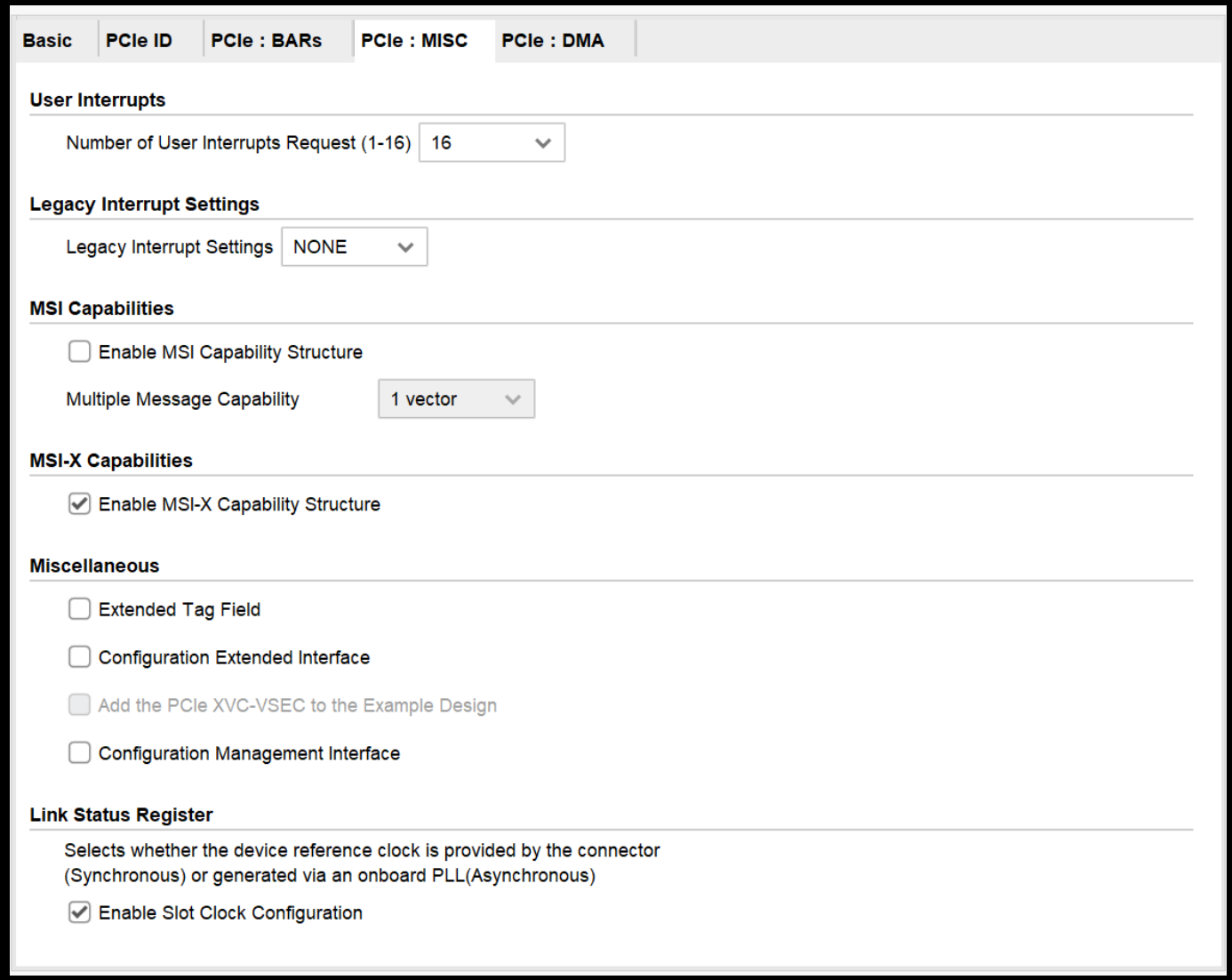
XDMA IP Setting

PCIE Address分配



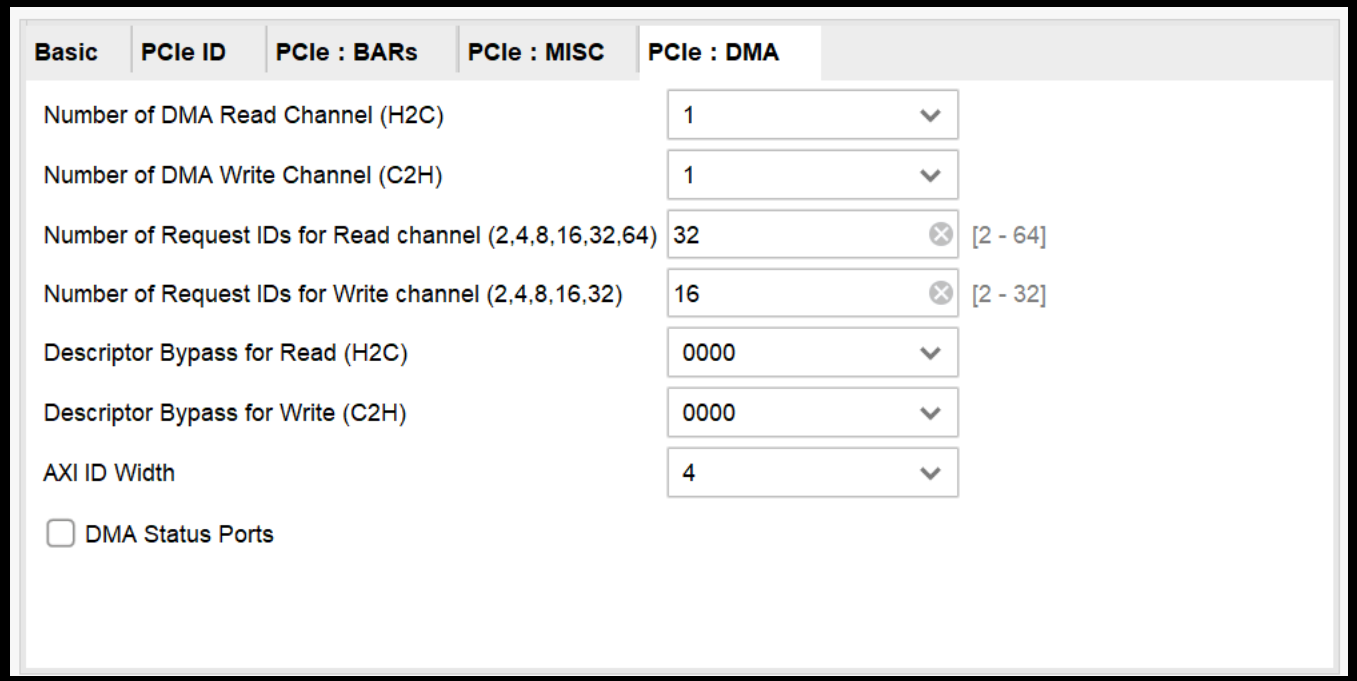
XDMA IP Setting

PCIE 中斷設置 最高16bit



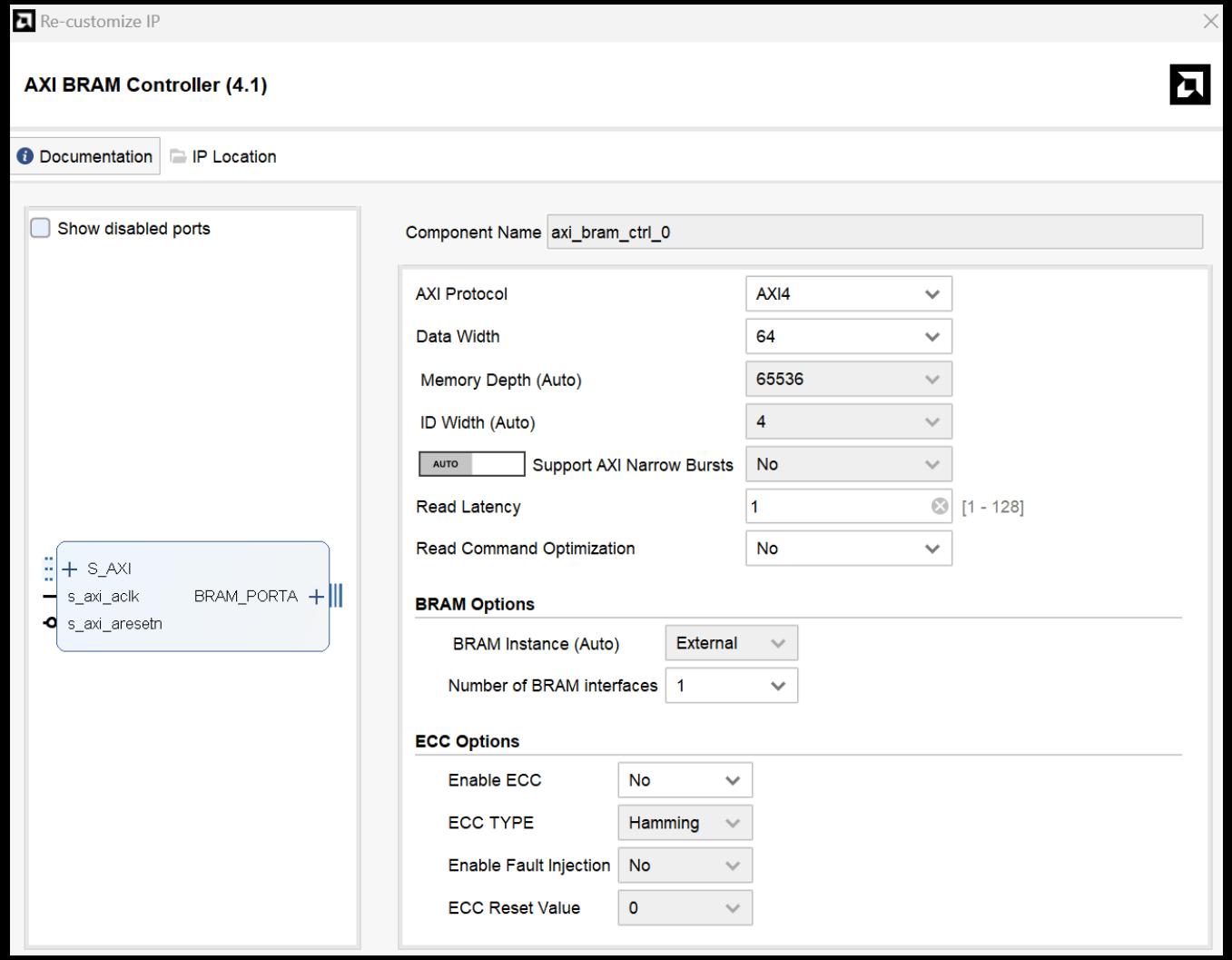
XDMA IP Setting

DMA設置 主要修改通道數量 以GEN3來說最高兩讀兩寫



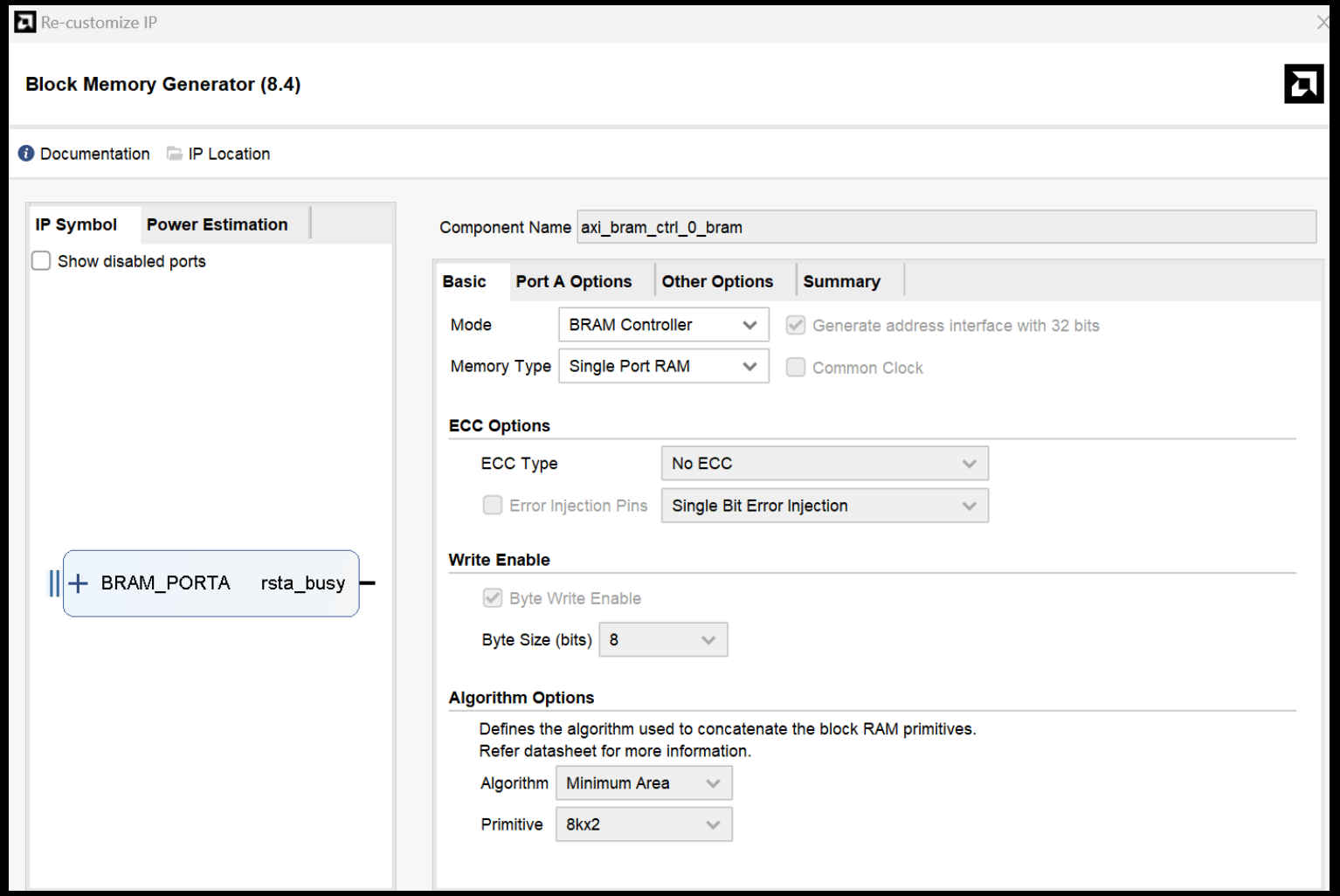
Bram_ctrl

接收xdma的axi data並轉給bram



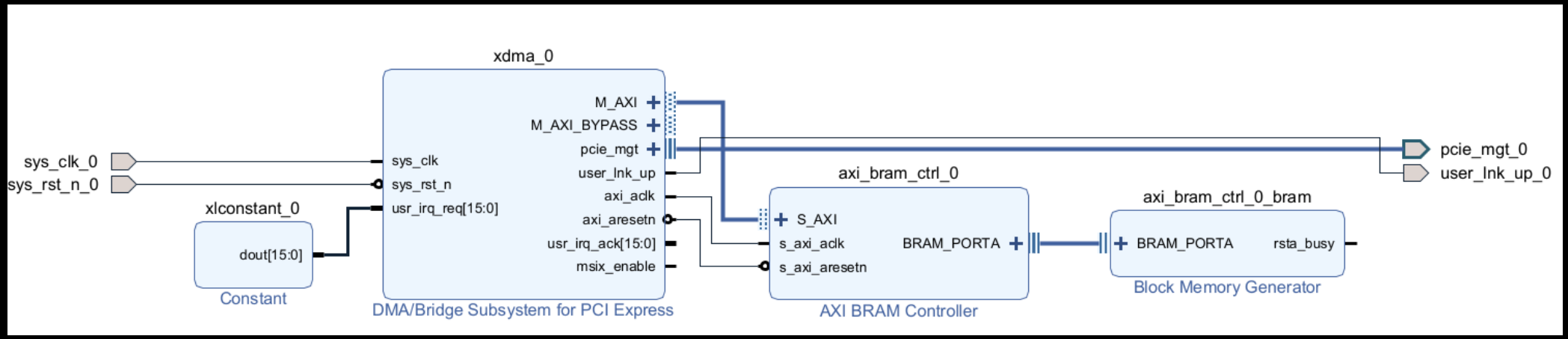
Bram inst

FPGA的bram例化



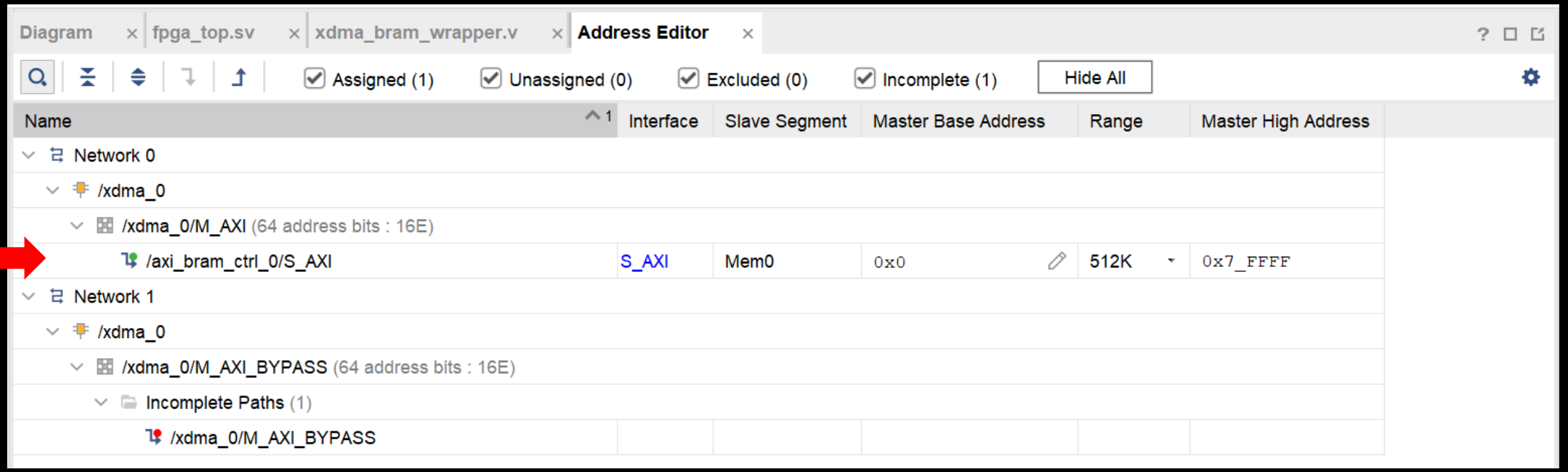
AMD

Block Design



AMD

Address assign



FPGA_Top

除了bd以外還需添加io & clock buffer，所以另外編寫一個頂層文件

```
module fpga_top (
    output wire       o_led0,
    input  wire       i_pcie_rstn,
    input  wire       i_pcie_refclkp, i_pcie_refclkn,
    input  wire [0:0] i_pcie_rxp, i_pcie_rxn,
    output wire [0:0] o_pcie_txp, o_pcie_txn
);
wire  pcie_rstn;
wire  pcie_refclk;
```

AMD

FPGA_Top

使用xilinx提供的原語

```
//////////////////////////////////////////////////////////////////
// Ref clock input buffer
//////////////////////////////////////////////////////////////////
IBUFDS_GTE2 refclk_ibuf (
    .CEB             ( 1'b0             ),
    .I               ( i_pcie_refclkp   ),
    .IB              ( i_pcie_refclkn   ),
    .O               ( pcie_refclk      ),
    .ODIV2           (                  )
);
//////////////////////////////////////////////////////////////////
// Reset input buffer
//////////////////////////////////////////////////////////////////
IBUF   sys_reset_n_ibuf (
    .I               ( i_pcie_rstn      ),
    .O               ( pcie_rstn        )
);
```

AMD

FPGA_Top

Block design inst

```
//////////////////////////////////////////////////////////////////
// block design
//////////////////////////////////////////////////////////////////
xdma_bram_wrapper xdma_bram_wrapper_i (
    .pcie_mgt_0_rxn  ( i_pcie_rxn        ),
    .pcie_mgt_0_rxp  ( i_pcie_rxp        ),
    .pcie_mgt_0_txn  ( o_pcie_txn        ),
    .pcie_mgt_0_txp  ( o_pcie_txp        ),
    .sys_clk_0       ( pcie_refclk       ),
    .sys_rst_n_0     ( pcie_rstn         ),
    .user_lnk_up_0   ( o_led0            )
);


endmodule
```

AMD

FPGA_Top

Constraints

```
set_property -dict { PACKAGE_PIN AR22  IOSTANDARD LVCMOS15 } [get_ports { o_led0 }];
#set_property -dict { PACKAGE_PIN AR23  IOSTANDARD LVCMOS15 } [get_ports { o_led1 }];

set_property -dict { PACKAGE_PIN AY35  IOSTANDARD LVCMOS18  PULLUP true } [get_ports i_pcie_rstn]
set_property PACKAGE_PIN AB8  [get_ports { i_pcie_refclkp }];
create_clock -name sys_clk -period 10 [get_ports i_pcie_refclkp]

set_property PACKAGE_PIN W2   [get_ports { o_pcie_txp[0] }];
#set_property PACKAGE_PIN AA2  [get_ports { o_pcie_txp[1] }];
#set_property PACKAGE_PIN AC2  [get_ports { o_pcie_txp[2] }];
#set_property PACKAGE_PIN AE2  [get_ports { o_pcie_txp[3] }];
#set_property PACKAGE_PIN AG2  [get_ports { o_pcie_txp[4] }];
#set_property PACKAGE_PIN AH4  [get_ports { o_pcie_txp[5] }];
#set_property PACKAGE_PIN AJ2  [get_ports { o_pcie_txp[6] }];
#set_property PACKAGE_PIN AK4  [get_ports { o_pcie_txp[7] }];

set_property PACKAGE_PIN Y4   [get_ports { i_pcie_rxp[0] }];
#set_property PACKAGE_PIN AA6  [get_ports { i_pcie_rxp[1] }];
#set_property PACKAGE_PIN AB4  [get_ports { i_pcie_rxp[2] }];
#set_property PACKAGE_PIN AC6  [get_ports { i_pcie_rxp[3] }];
#set_property PACKAGE_PIN AD4  [get_ports { i_pcie_rxp[4] }];
#set_property PACKAGE_PIN AE6  [get_ports { i_pcie_rxp[5] }];
#set_property PACKAGE_PIN AF4  [get_ports { i_pcie_rxp[6] }];
#set_property PACKAGE_PIN AG6  [get_ports { i_pcie_rxp[7] }];
```

AMD

Host PC Driver

上電燒錄後，須確保FPGA不斷電的情況下重啟Ubuntu主機

重啟後先尋找是否有辨識到Xilinx PCie Device

```
$ lspci
...                                                     # Other PCI Device
01:00.0 Memory controller: Xilinx Corporation Device 7021       # Xilinx PCIe-XDMA Device
...                                                     # Other PCI Device
```

下載Xilinx提供的dma driver

https://github.com/Xilinx/dma_ip_drivers

cd至以下目錄中，並編譯xdma driver

```
$ cd xdma
$ sudo make install
$ cd tools
$ sudo mak
```

Load Kernal Driver

```
$ sudo modprobe xdma
```

使用xilinx提供的測試app來讀寫

```
$ ./load_driver.sh
$ ./run_test.sh
```

AMD


AMD