



DisplayPort 1.4 via VCK190 VMK180 Zcu102

Course Agenda
2022.2

測試流程參考文件

DisplayPort 1.4 RX Subsystem Product Guide (PG300)

VCK190 Evaluation Board User Guide (UG1366)

ZCU102 Evaluation Board User Guide

VMK180 Evaluation Board User Guide (UG1411)

VCK190/VMK180 - What board should I select in Vivado - with or without the new SD level shifter?



VCK190

Course Agenda
2022.2

New Project
 ✕

Default Part

Choose a default Xilinx part or board for your project.

開發版依照板子上的貼紙選擇(Click)

Parts | **Boards**

To fetch the latest available boards from git repository, click on 'Refresh' button. [Dismiss](#)

[Reset All Filters](#)

Vendor: Name: Board Rev:

Search: (2 matches)

| Display Name | Preview | Status | Vendor | File Version | Part |
|-----------------------------------------------------------------------------|---------|-----------|------------|--------------|---------------------------|
| Versal VCK190 Evaluation Platform | | Installed | xilinx.com | 3.0 | xcvc1902-vsua2197-2MP-e-S |
| Versal VCK190 Evaluation Platform with New SD Level Shifter | | Installed | xilinx.com | 1.0 | xcvc1902-vsua2197-2MP-e-S |

?

SOLUTION

On the board, there is a sticker that has a number starting with 043. All 043-05005-01-**101**-xxxx (VCK190) and 043-05005-02-**101**-xxxx (VMK180) and later serials have the latest level shifter.

The 101 variant is the first series of boards to ship with the latest level shifter captured in the BOM/Schematics. Select the "New SD Level Shifter" selection for these newer boards.

Boards prior to those serial numbers and serials that are 4 digits have the old IP4856CX25/CZ. Select the "Versal VCK190 Evaluation Platform" for these boards. If there you have any questions please open a case or post your question in the community.

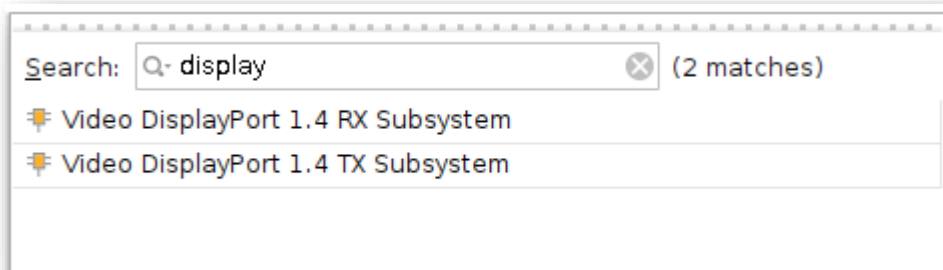
4

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依據開發版以及要進行的測試選擇對應的IP



Right-click **BD** and click **Add IP**. Search for DisplayPort 1.4 and select either the DisplayPort 1.4 Receiver Subsystem IP (for RX only (ZCU102, VCU118), Pass-through (KCU105, ZCU102, and VCK190) designs) or the DisplayPort 1.4 Transmitter Subsystem IP (for TX only (ZCU102, VCU118, and VCK190), or Pass-through (KCU105) designs).

Re-customize IP@anstek-Z490-GAMING-X

Video DisplayPort 1.4 RX Subsystem (3.0)

Documentation
IP Location

☐ Show disabled ports

| | | |
|---------------------------|--------------------------|------------|
| + s_axi | m_axis_phy_rx_sb_control | + edid_iic |
| + s_axis_phy_rx_sb_status | m_axis_video_stream1 | + ext_iic |
| + s_axis_inkl_rx_lane0 | aux_rx_io_p | |
| + s_axis_inkl_rx_lane1 | aux_rx_io_n | |
| + s_axis_inkl_rx_lane2 | rx_hpd | |
| + s_axis_inkl_rx_lane3 | dprxss_dp_irq | |
| s_axi_aclk | rx_gt_ctrl_out[31:0] | |
| s_axi_aresetn | rx_misc0_str1[7:0] | |
| rx_vid_clk | rx_misc1_str1[7:0] | |
| rx_vid_rst | adaptive_sdp_out[31:0] | |
| m_axis_aclk_stream1 | adaptive_sdp_vld | |
| rx_dec_clk | ext_rst[0:0] | |
| rx_inl_clk | dprxss_iic_irq | |

Component Name v_dp_rxss1_0

Main Page
Application Example Design

Application Example Design
FB Passthrough without HDCP

Application Example Design Overview

SST Pass-through without HDCP Architecture

- Example uses a Video Frame Buffer to capture received frame and plays it back using transmit path.
- I2S Transmitter along with Audio clock recovery unit is used with DisplayPort RX to transmit the received audio to external audio receiver.
- I2S Receiver is used with DisplayPort TX to transmit audio through DP
- Configuration: SST Mode, MAX_BPC=10, GT Data Width=2 Bytes, HDCP=False

Note: To generate the Application Example Design, right click the subsystem in the IPI canvas and select 'Open IP Example Design'

```

graph LR
    I2S_Tx[I2S Transmitter / Audio Clock Recovery] --> DP_Receive[DisplayPort Receive Subsystem]
    DP_Receive --> VFB[Video Frame Buffer]
    VFB --> SPG[Stream Pattern Generator]
    SPG --> DP_Transmit[DisplayPort Transmit Subsystem]
    I2S_Rx[I2S Receiver] --> DP_Transmit
    DP_Transmit --> VPHY[Video PHY Controller]
    VPHY -- DP Mainlink --> DP_Mainlink_Out[DP Mainlink]
    DP_Mainlink_In[DP Mainlink] --> VPHY
    
```

Bought IP license available

OK

Cancel

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IP Setting確認無誤後就打開Example Design 直接生成bit or image即可(不須其餘操作)

Available Example Designs

The following table shows the example designs available for the TX and RX DisplayPort 1.4 subsystems.

Table: Available Example Designs

| GT Type | Topology | Video PHY Config ¹ | | Hardware | BPC | Processor |
|---------|------------------------------------------------------------|-------------------------------|---------|-----------------------------------|-----|-------------|
| | | (TXPLL) | (RXPLL) | | | |
| GTHE3 | Pass-through without HDCP1.3 | QPLL | CPLL | KCU105 + Inrevium TB-FMCH-VFMC-DP | 8 | MicroBlaze™ |
| GTHE4 | RX only | - | CPLL | ZCU102 + Inrevium TB-FMCH-VFMC-DP | 10 | A53 |
| | TX only | QPLL | - | ZCU102 + Inrevium TB-FMCH-VFMC-DP | 10 | A53 |
| | FB Pass-through without HDCP1.3/HDCP2.2/2.3 ^{2,3} | QPLL | CPLL | ZCU102 + Inrevium TB-FMCH-VFMC-DP | 10 | A53 |
| | FB Pass-through with HDCP1.3 and HDCP2.2/2.3 ⁴ | QPLL | CPLL | ZCU102 + Inrevium TB-FMCH-VFMC-DP | 10 | A53 |
| | MST FB Pass-through without HDCP1.3 and TX only | QPLL | CPLL | ZCU102+ Inrevium TB-FMCH-VFMC-DP | 10 | A53 |
| GTYE4 | RX only | - | CPLL | VCU118 + Inrevium TB-FMCH-VFMC-DP | 10 | MicroBlaze |
| | TX only | QPLL | - | VCU118 + Inrevium TB-FMCH-VFMC-DP | 10 | MicroBlaze |
| GTYE5 | TX Only | RPLL | - | VCK190 + Inrevium TBFMCH-VFMC-DP | 10 | A72 |
| | FB Pass-through without HDCP1.3/HDCP2.2/2.3 ² | RPLL | LCPLL | VCK190 + Inrevium TBFMCH-VFMC-DP | 10 | A72 |

Vitis

type filter text

▼ vck190dp

▼ processor_hier_0_versal_cips_0_pspmc_0_p

▼ standalone on processor_hier_0_versal_

Board Support Package

▼ processor_hier_0_versal_cips_0_pspmc_0_p

▼ another

Board Support Package

Board Support Package

View current BSP settings, or configure settings like STDIO peripheral selection, compiler flags, SW intrusive profiling, add/remove libraries, assign drivers to peripherals, change versions of OS/libraries/drivers etc.

[Modify BSP Settings...](#) [Reset BSP Sources](#)

A BSP settings file is generated with the user options selected in the settings dialog. To use existing settings, click the below link. This operation clears any existing modifications done. All the subsequent changes are applied on top of the loaded settings.

[Load BSP settings from file](#)

Operating System

Name: standalone

Version: 8.0

Description: Standalone is a simple, low-level software layer. It provides access to basic processor features such as caches, interrupts and exceptions as well as the basic features of a hosted environment, such as standard input and output, profiling, abort and exit.

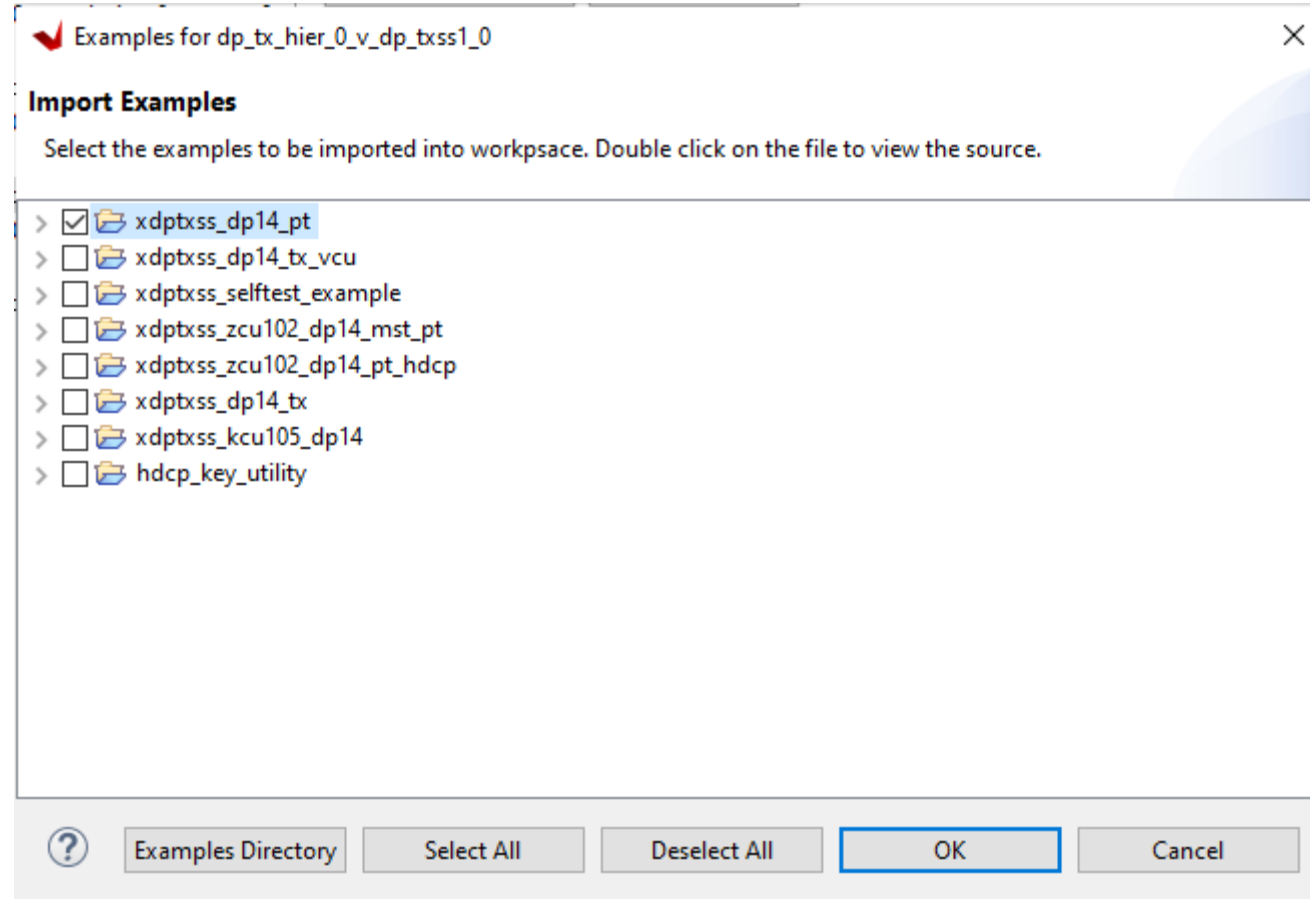
Documentation: -

Drivers

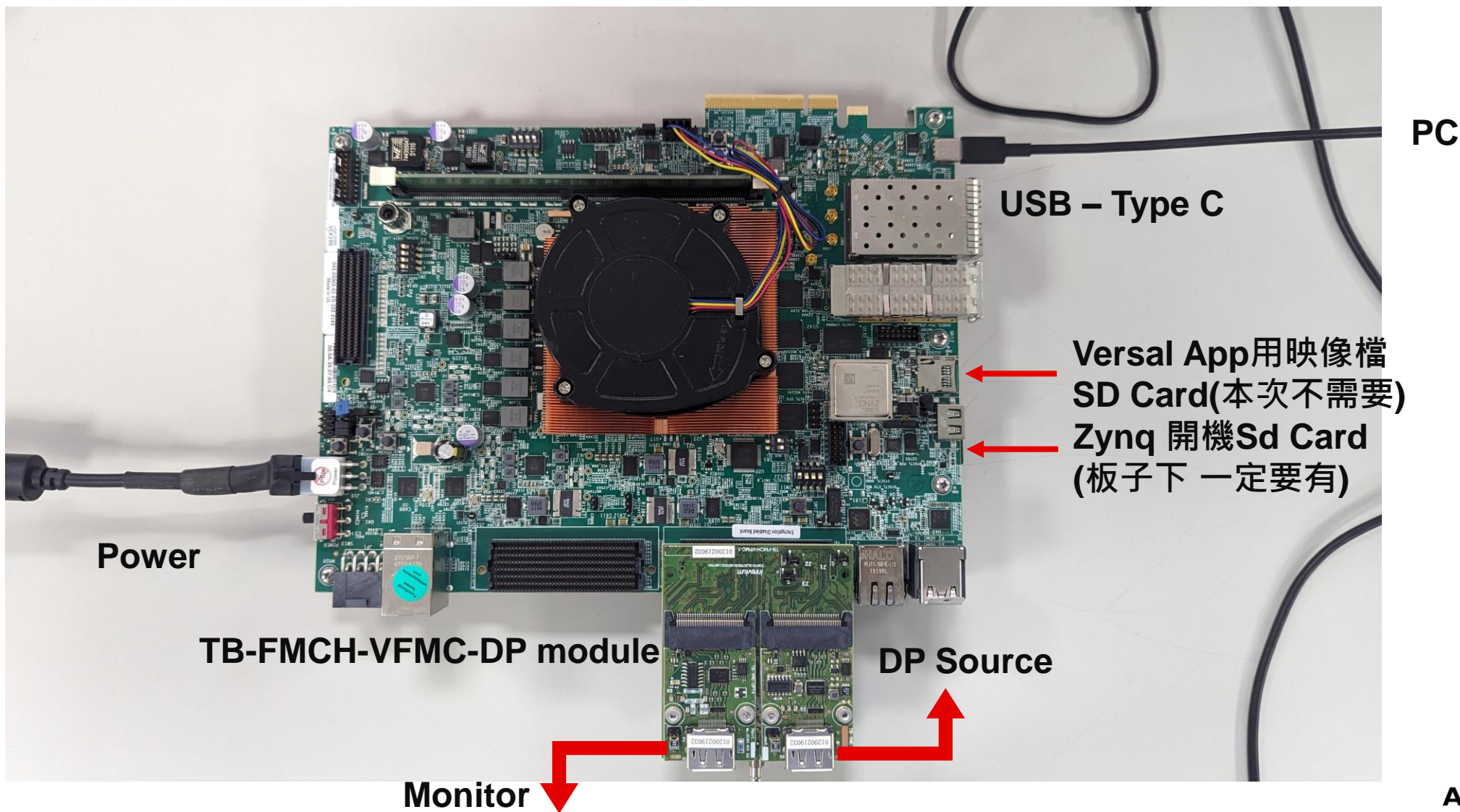
Libraries

| Name | Driver | Documentation | Examples |
|---------------------------------|-------------|------------------------------------|---------------------------------|
| dp_rx_hier_0_rx_acr | generic | - | - |
| dp_rx_hier_0_v_dp_rxss1_0 | dp14rxss | Documentation Link | Import Examples |
| dp_rx_hier_0_v_frmbuf_wr_0 | v_frmbuf_wr | Documentation Link | Import Examples |
| dp_rx_hier_0_vid_edid_0 | generic | - | - |
| dp_rx_hier_0_video_frame_crc_0 | generic | - | - |
| dp_tx_hier_0_axis_switch_0 | axis_switch | Documentation Link | Import Examples |
| dp_tx_hier_0_clk_wizard_2 | clk_wiz | Documentation Link | - |
| dp_tx_hier_0_i2s_receiver_0 | i2srx | Documentation Link | Import Examples |
| dp_tx_hier_0_tx_clk_rst | gpio | Documentation Link | Import Examples |
| dp_tx_hier_0_v_dp_txss1_0 | dp14txss | Documentation Link | Import Examples |
| dp_tx_hier_0_v_frmbuf_rd_0 | v_frmbuf_rd | Documentation Link | Import Examples |
| dp_tx_hier_0_video_frame_crc_tx | generic | - | - |
| gt_quad_gt_quad_base | generic | - | - |

Vitis(也是會分板子跟測試方式 如果是190的pass-through 選擇第一項)



VCK190 Board Setup (生成的同時可以準備設置開發版)



VCK190 Board Setup (要求有REFCLK 所以要裝在2上)

VCK190 Evaluation Board User Guide (UG1366)

UG1366

2023-03-17

1.1 English

FMCP1 Connector J51

[Figure 1, callout 20]

The HSPC connector J51 implements a subset of the full FMCP connectivity:

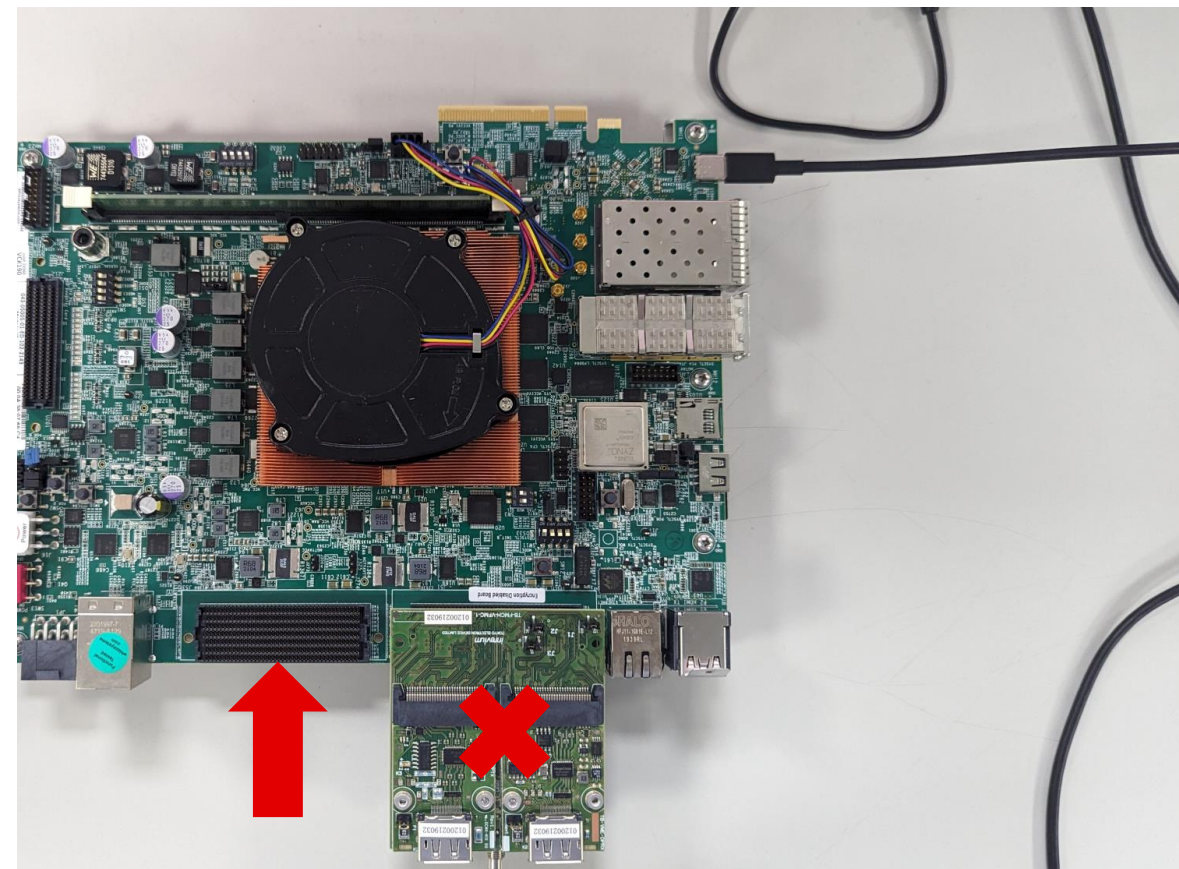
- 68 single-ended or 34 differential user-defined pairs (34 LA pairs: LA[00:33])
- 12 transceiver differential pairs
- 3 transceiver differential clocks
- 2 differential clocks
- 239 ground and 15 power connections

FMCP2 Connector J53

[Figure 1, callout 20]

The HSPC connector J53 implements a subset of the full FMCP connectivity:

- 68 single-ended or 34 differential user-defined pairs (34 LA pairs: LA[00:33])
- 12 transceiver differential pairs
- 3 transceiver differential clocks
- 2 differential clocks
- 1 differential (REFCLK) clock C2M pair
- 1 differential (SYNC) clock C2M pair
- 239 ground and 15 power connections



Setting the FMC Voltage to 1.5V

<https://www.xilinx.com/products/boards-and-kits/vck190.html#resources>

使用System Controller調整電壓



 [XTP618 - VCK190 System Controller GUI Tutorial \(v1.5\)](#)

Nov 18, 2021

Document Type: Example Designs

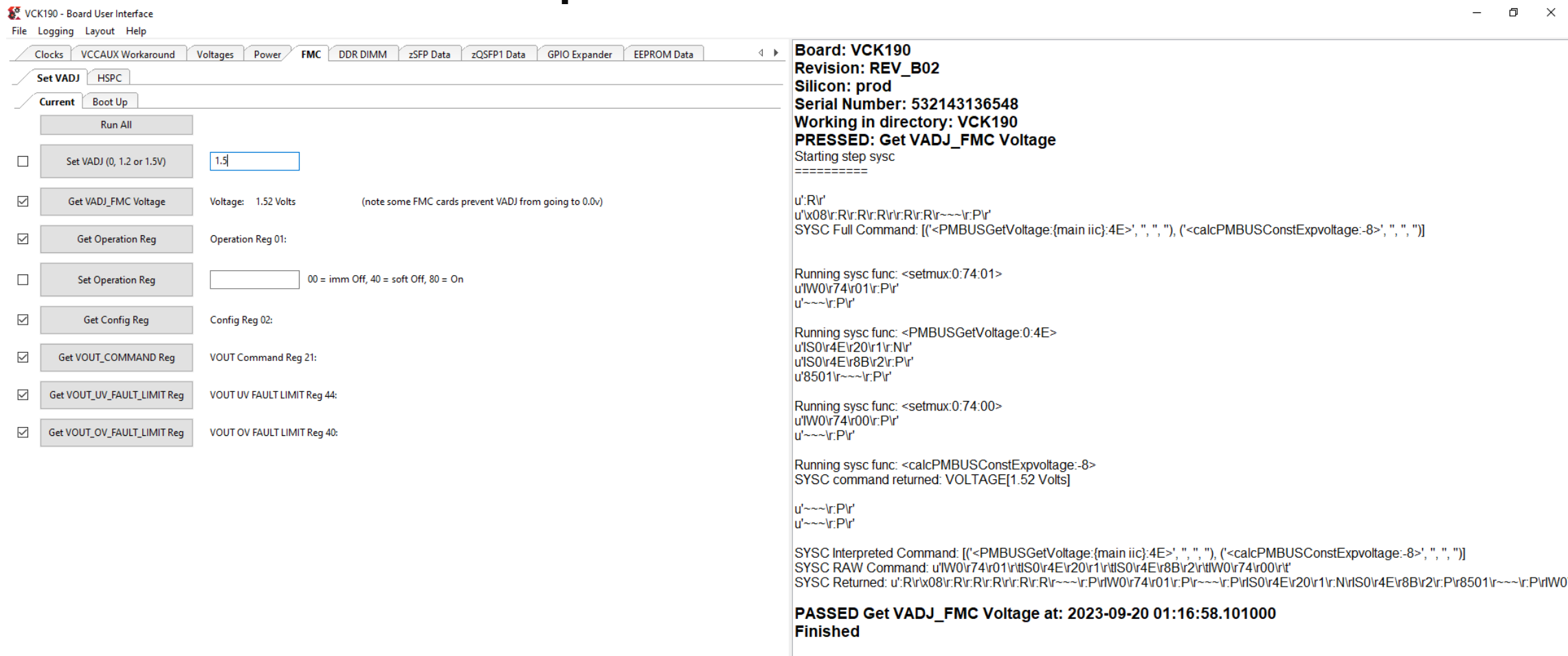
Using the System Controller GUI with the VCK190

 [See All Versions](#)

Design File(s):

[↓ rdf0574-vck190-bit-c-2021-2.zip](#)

底部切到**System controller** 上方切到**FMC**
選擇**Set VADJ** 讀取當前電壓或更改
若要開機同時更改 到**Boot Up**來改



燒錄成功 應該就會在螢幕上看到畫面 且UART出現以下畫面

```
*****
PlatformInit
VPMC: Setting IO Expanders...
Platform initialization done.
INFO:DPRXSS is SST enabled. DPRXSS works only in SST mode.
INFO:DPTXSS is SST enabled. DPTXSS works only in SST mode.

*****
This system is purely a PassThrough system designed to
display the video that is received on the RX.
The TX is non functional in absence of active RX link
Do not change the Monitor once the application is in run mode
This system can be used for DisplayPort Sink Compliance
*****

-----
--                               Menu                               --
-----

Select option
p - Pass-through design
UserInput: p
Reading EDID contents of the DP Monitor..
DP RX enabled for Adaptive Sync

-----
--                               DisplayPort RX-TX Demo Menu          --
-----

Select option
1 = Change Lane and Link capabilities
2 = Link, MSA and Error Status
3 = Toggle HPD to ask for Retraining
4 = Restart TX path
c = Check SUM on Rx and Tx
d = Quad selection ONLY FOR 8K --> 4K demo
w = Sink register write
r = Sink register read
n = Clone EDID from Monitor
m = Display MCDP6000 status
u = Read from MCDP6000
o = Write to MCDP6000
z = Display this menu again
x = Return to Main menu

-----
> Rx Training done !!! (BW: 0x1E, Lanes: 0x2, Status: 0x9977;0x0).
*** Resolution: 3840 x 2160 @ 30Hz, BPC = 10, PPC = 2, Color = RGB (0) ***

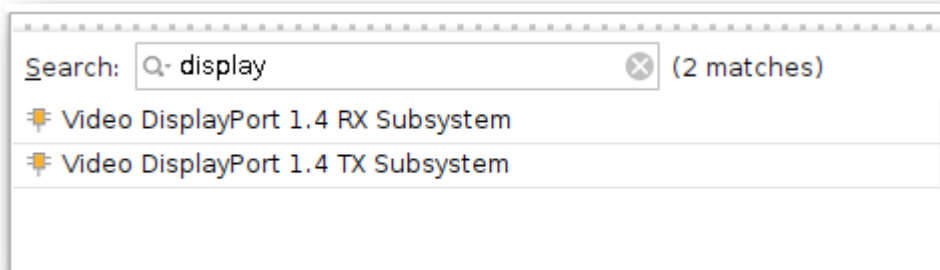
Training TX with: Link rate 14, Lane 4, BPC 10, (0)
.....^^..done !
**
```



ZCU102

Course Agenda
2022.2

依據開發版以及要進行的測試選擇對應的IP



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Application Example Design(此次選擇不帶HDCP的Passthrough)

Re-customize IP@anstek-Z490-GAMING-X

Video DisplayPort 1.4 RX Subsystem (3.0)

Documentation IP Location

Show disabled ports

Component Name v_dp_rxss1_0

Main Page Application Example Design

Application Example Design FB Passthrough with HDCP1.3 and HDCP2.2

Application Example Receive Only

FB Passthrough without HDCP

FB Passthrough with HDCP1.3 and HDCP2.2

MST FB Passthrough without HDCP

Pass-through with HDCP

- Example uses a Video

- Configuration: SST Mod

Note: To generate the Application Example Design, right click the subsystem in the IPI canvas and select 'Open IP Example Design'

Bought IP license available

OK Cancel

```
graph LR
    VFB[Video Frame Buffer] --> DPRS[DisplayPort Receive Subsystem]
    DPRS --> VPHYC[Video PHY Controller]
    VPHYC --> DPTS[DisplayPort Transmit Subsystem]
    DPTS --> SPG[Stream Pattern Generator]
    DPTS --> HK2[HDCP Key Block]
    HK1[HDCP Key Block] --> DPRS
    VPHYC -- DP Mainlink --> Out[DP Mainlink]
```

IP Setting確認無誤後就打開Example Design 直接生成bit or image即可(不須其餘操作)

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| GTHE4 | RX only | - | CPLL | ZCU102 + Inrevium TB-FMCH-VFMC-DP | 10 | A53 |
| | TX only | QPLL | - | ZCU102 + Inrevium TB-FMCH-VFMC-DP | 10 | A53 |
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| | FB Pass-through with HDCP1.3 and HDCP2.2/2.3 ⁴ | QPLL | CPLL | ZCU102 + Inrevium TB-FMCH-VFMC-DP | 10 | A53 |
| | MST FB Pass-through without HDCP1.3 and TX only | QPLL | CPLL | ZCU102+ Inrevium TB-FMCH-VFMC-DP | 10 | A53 |
| GTYE4 | RX only | - | CPLL | VCU118 + Inrevium TB-FMCH-VFMC-DP | 10 | MicroBlaze |
| | TX only | QPLL | - | VCU118 + Inrevium TB-FMCH-VFMC-DP | 10 | MicroBlaze |
| GTYE5 | TX Only | RPLL | - | VCK190 + Inrevium TBFMCH-VFMC-DP | 10 | A72 |
| | FB Pass-through without HDCP1.3/HDCP2.2/2.3 ² | RPLL | LCPLL | VCK190 + Inrevium TBFMCH-VFMC-DP | 10 | A72 |

Board setup

Figure: ZCU102 Board Setup



Setting the FMC Voltage to 1.8V

<https://www.xilinx.com/products/boards-and-kits/ek-u1-zcu102-g.html#resources>

使用System Controller調整電壓



[XTP433 - ZCU102 System Controller GUI Tutorial \(v11.1\)](#)

Jul 26, 2019

Document Type: Example Designs

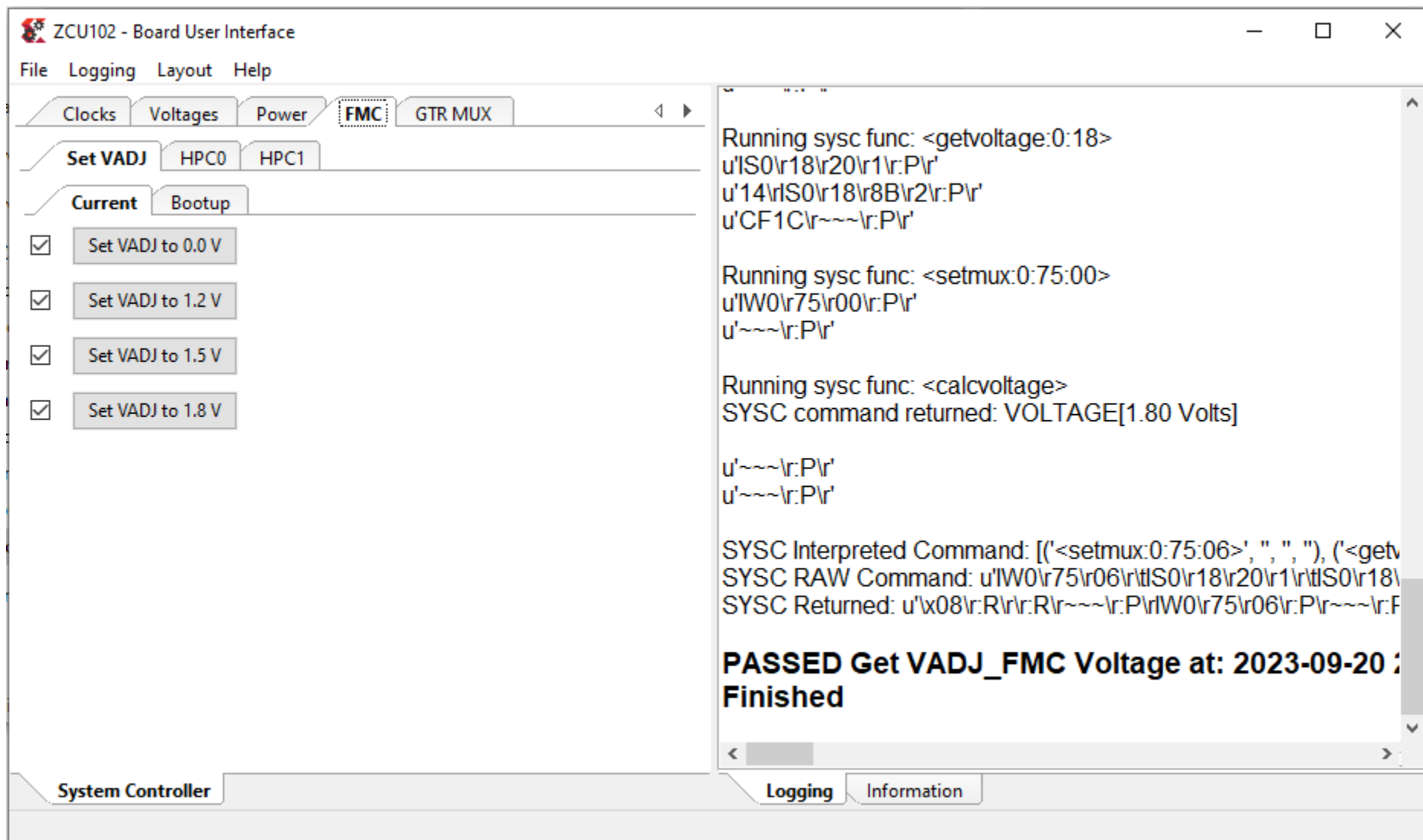
Using the System Controller GUI for the ZCU102

[See All Versions](#)

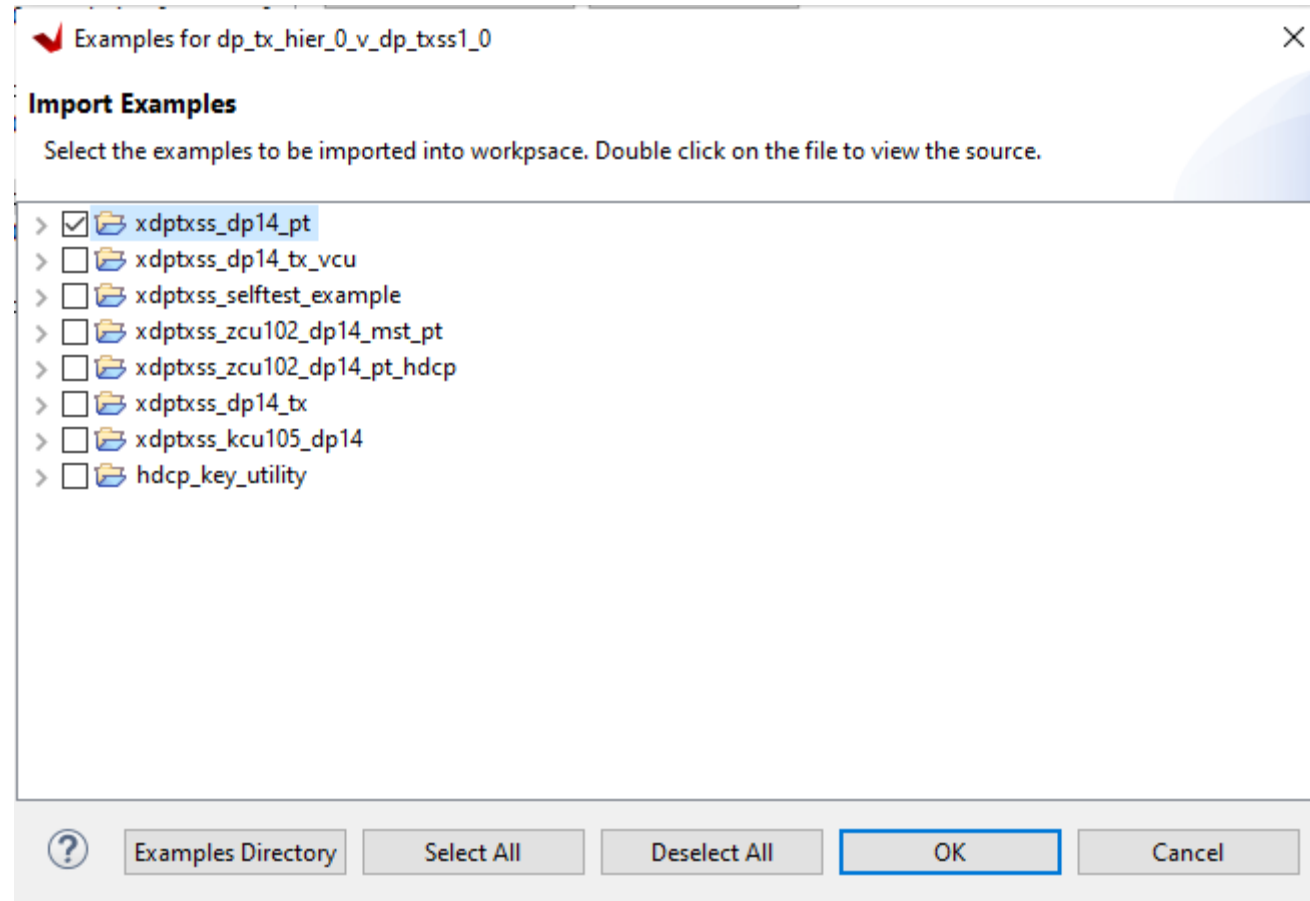
Design File(s):

[rdf0382-zcu102-system-controller-c-2019-1.zip](#)

Setting the FMC Voltage to 1.8V



Vitis(也是會分板子跟測試方式 我們選單純的PT測試 就選第一項)





可能遇到的問題

Course Agenda
2022.2

可能出現的問題

UART顯示Platform init階段失敗

確認FMC電壓是否符合要求

無法讀取更改電壓 檢查是否全英文路徑 以及其他設備干擾(螢幕,藍芽耳機等)

The screenshot shows the VCK190 Board User Interface. The 'FMC' tab is selected, and the 'Boot Up' sub-tab is active. The 'Set VADJ' section is expanded, showing several checkboxes and input fields for configuring FMC voltage settings. The console window on the right displays the board information and a traceback of an exception.

Board: VCK190
Revision: REV_B02
Silicon: prod
Serial Number: 532143136548
Working in directory: VCK190
PRESSED: Get VADJ_FMC Voltage (1.5v)
Starting step sysc
=====

Exception in thread Thread-2:
Traceback (most recent call last):
File "threading.py", line 801, in __bootstrap_inner
File "testthread.py", line 87, in run
File "testthread.py", line 173, in runbutton
File "testthread.py", line 577, in sysc
UnicodeEncodeError: 'ascii' codec can't encode characters in position 0-10: ordinal not in range(128)

可能出現的問題

Not enabled for Adaptive Sync

```

-----
--                               Menu                               --
-----

Select option
p - Pass-through design
UserInput: p
Reading EDID contents of the DP Monitor..
DP RX not enabled for Adaptive Sync
DP RX enabled for VSC Colorimetry support
-----

--                               DisplayPort RX-TX Demo Menu       --
-----

Select option
1 = Change Lane and Link capabilities
2 = Link, MSA and Error Status
3 = Toggle HPD to ask for Retraining
4 = Restart TX path
c = Check SUM on Rx and Tx
d = Quad selection ONLY FOR 8K --> 4K demo
w = Sink register write
r = Sink register read
n = Clone EDID from Monitor
m = Display MCDP6000 status
u = Read from MCDP6000
o = Write to MCDP6000
z = Display this menu again
x = Return to Main menu
-----

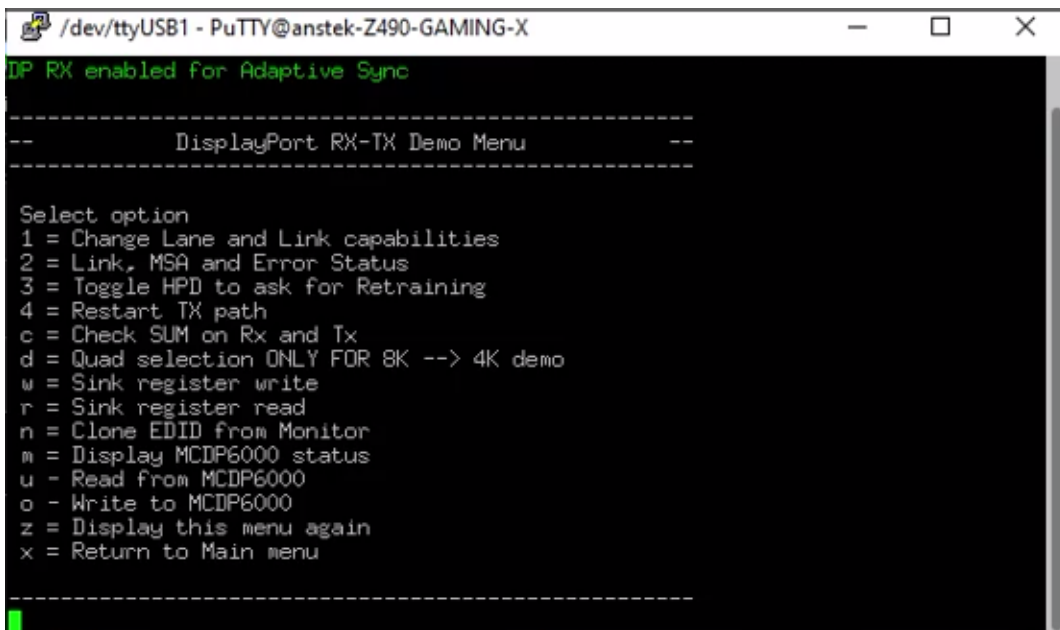
```

請確認DP源及顯示器是否至少DP1.2以上 且已開啟AdaptiveSync功能

可能出現的問題

2021.2會遇到只有單一顆處理器可以training的bug 但2022.2測試正常

其中一顆會卡在這畫面



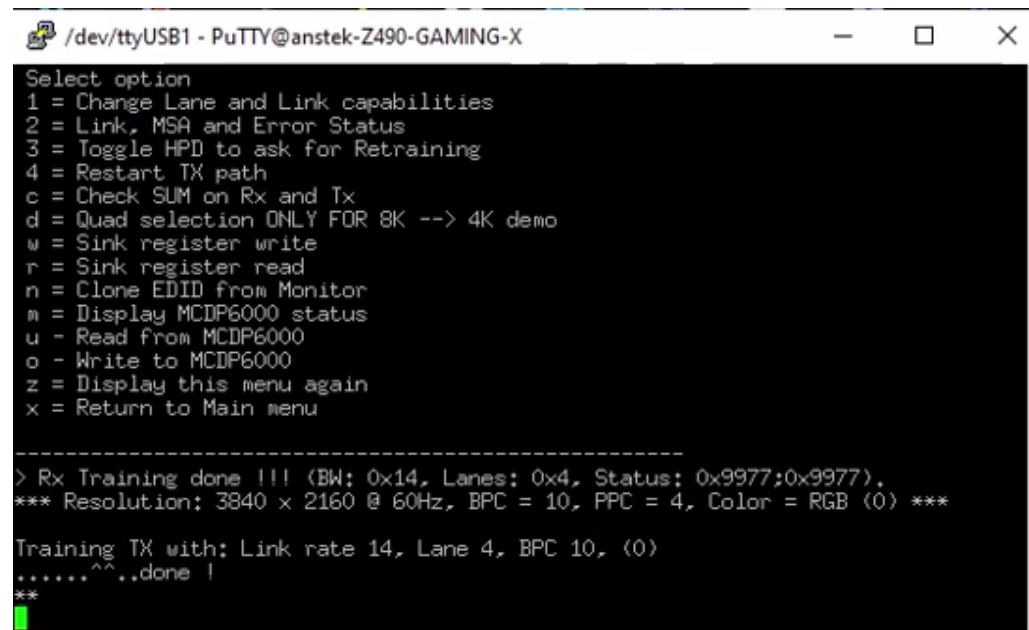
```
/dev/ttyUSB1 - PuTTY@anstek-Z490-GAMING-X
DP RX enabled for Adaptive Sync

-----
--          DisplayPort RX-TX Demo Menu          --
-----

Select option
1 = Change Lane and Link capabilities
2 = Link, MSA and Error Status
3 = Toggle HPD to ask for Retraining
4 = Restart TX path
c = Check SUM on Rx and Tx
d = Quad selection ONLY FOR 8K --> 4K demo
w = Sink register write
r = Sink register read
n = Clone EDID from Monitor
m = Display MCDP6000 status
u = Read from MCDP6000
o = Write to MCDP6000
z = Display this menu again
x = Return to Main menu

-----
```

另一顆會正常training



```
/dev/ttyUSB1 - PuTTY@anstek-Z490-GAMING-X

Select option
1 = Change Lane and Link capabilities
2 = Link, MSA and Error Status
3 = Toggle HPD to ask for Retraining
4 = Restart TX path
c = Check SUM on Rx and Tx
d = Quad selection ONLY FOR 8K --> 4K demo
w = Sink register write
r = Sink register read
n = Clone EDID from Monitor
m = Display MCDP6000 status
u = Read from MCDP6000
o = Write to MCDP6000
z = Display this menu again
x = Return to Main menu

-----
> Rx Training done !!! (BW: 0x14, Lanes: 0x4, Status: 0x9977;0x9977).
*** Resolution: 3840 x 2160 @ 60Hz, BPC = 10, PPC = 4, Color = RGB (0) ***

Training TX with: Link rate 14, Lane 4, BPC 10, (0)
.....^^..done !
**
```

哪一顆會有問題不一定

可能出現的問題

Platform init成功 無法成功training

