FPGA Configuration

AMD
together we advance_

7 Series FPGAs Configuration (UG 470)

依據Xilinx文件UG470 了解FPGA來配置結構與流程，我們會搭配7系列的公版來了解實際的PCB運用情況。
因為FPGA為SRAM，所以需要搭配FLASH或是透過電腦接JTAG來做上電時的配置。
下圖是FPGA可接受的配置模式一覽。(不論是哪個模式，Xilinx FPGA皆支援JTAG模式)

Table 2-1: **7 Series FPGA Configuration Modes**

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	x1	Output
Master SPI	001	x1, x2, x4	Output
Master BPI	010	x8, x16	Output
Master SelectMAP	100	x8, x16	Output
JTAG	101	x1	Not Applicable
Slave SelectMAP	110	x8, x16, x32(1)	Input
Slave Serial(2)	111	x1	Input

Notes:

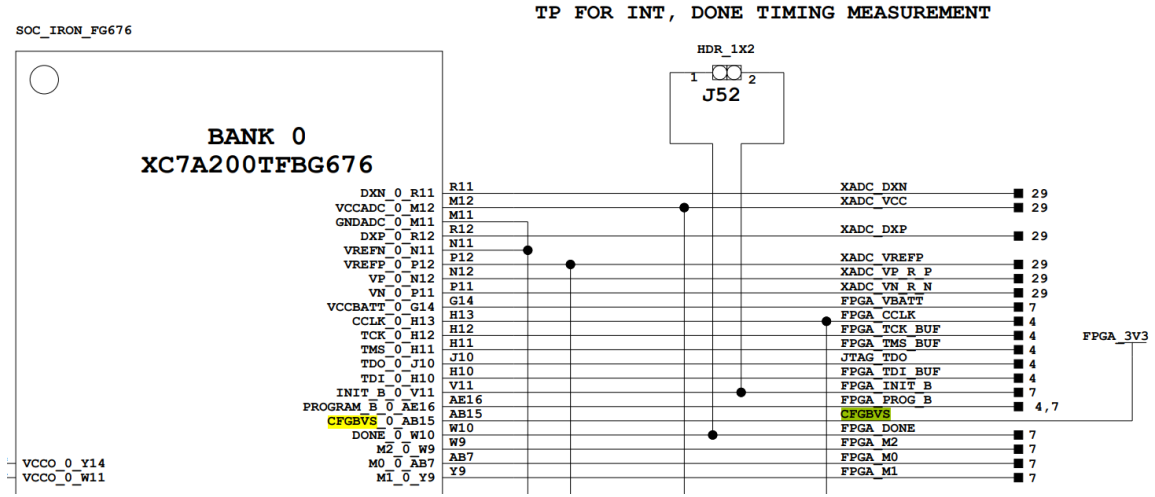
1. The Slave SelectMAP x16 and x32 bus widths do not support AES-encrypted bitstreams.
2. This is the default setting due to internal pull-up resistors on the Mode pins.

Configuration Pin Definitions

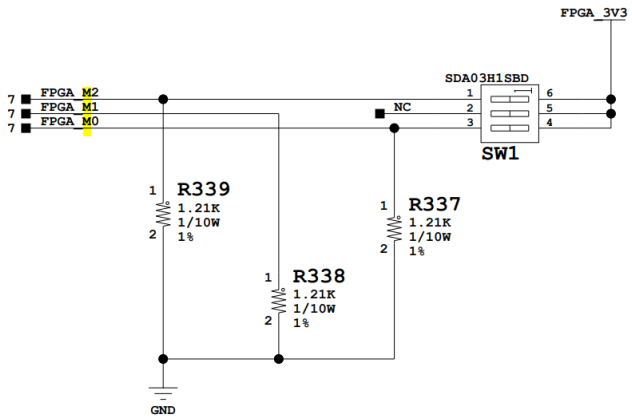
Table 2-4: **Configuration Pin Definitions**

Pin Name	Bank[1]	Type	Direction	Description
CFGBVS	0	Dedicated	Input	Configuration Banks Voltage Select CFGBVS determines the I/O voltage operating range and voltage tolerance for the dedicated configuration bank 0 and for the multi-function configuration pins in banks 14 and 15 in the AMD Spartan™-7, AMD Artix™-7 and AMD Kintex™-7 families. CFGBVS selects the operating voltage for the dedicated bank 0 at all times in all 7 series devices. CFGBVS selects the operating voltage for the multi-function configuration banks 14 and 15 only during configuration. Connect CFGBVS High or Low per the bank voltage requirements. If the V_{CCO_0} supply for bank 0 is supplied with 2.5V or 3.3V, then the CFGBVS pin must be tied High (i.e. connected to V_{CCO_0}). Tie CFGBVS to Low (i.e. connected to GND), only if the V_{CCO_0} for bank 0 is less than or equal to 1.8V. If used during configuration, banks 14 and 15 should match the VCCO level applied to bank 0. ***Caution!*** To avoid device damage, CFGBVS must be connected correctly to either V_{CCO_0} or GND. See Configuration Banks Voltage Select, page 28 for more information. ***Note:*** The CFGBVS pin is not available on AMD Virtex™-7 HT devices. Virtex 7 HT devices support only 1.8V operation for bank 0.
M[2:0]	0	Dedicated	Input	Configuration Mode M[2:0] determine the configuration mode. See Table 2-3, page 19 for the configuration mode settings. Connect each mode pin either directly, or via a ≤ 1 kΩ resistor, to V_{CCO_0} or GND.

CFGBVS：開機電壓選擇Pin



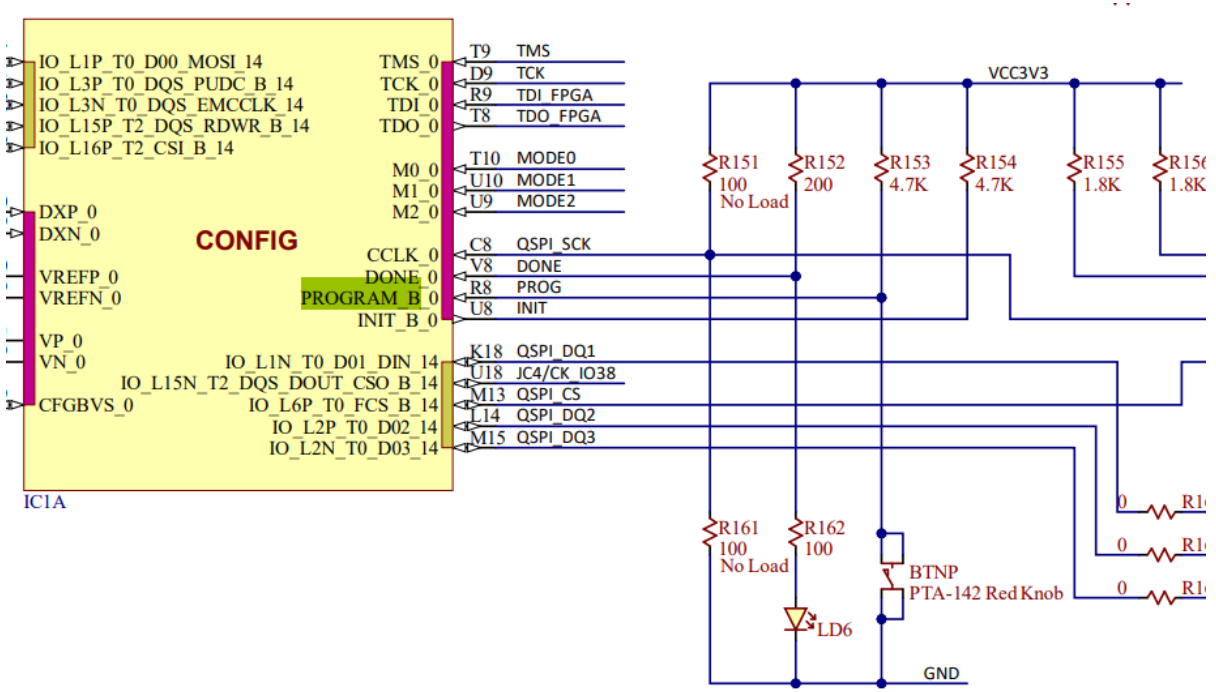
M[2:0]：配置模式



Configuration Pin Definitions

PROGRAM_B：下降沿reset，上升沿program
INT_B：檢測配置狀態(配置中或是發生錯誤)

PROGRAM_B	0	Dedicated	Input	Program (bar) Active-Low reset to configuration logic. When PROGRAM_B is pulsed Low, the FPGA configuration is cleared and a new configuration sequence is initiated. Configuration reset initiated upon falling edge, and configuration (i.e. programming) sequence begins upon the following rising edge. Connect PROGRAM_B to an external ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure a stable High input, and recommend push-button to GND to enable manual configuration reset. ***Note:*** Holding PROGRAM_B Low from power-on does not keep the FPGA configuration in reset. Instead, use INIT_B to delay the power-on configuration sequence.
INIT_B	0	Dedicated	Bidirectional (open-drain)	Initialization (bar) Active-Low FPGA initialization pin or configuration error signal. The FPGA drives this pin Low when the FPGA is in a configuration reset state, when the FPGA is initializing (clearing) its configuration memory, or when the FPGA has detected a configuration error. Upon completing the FPGA initialization process, INIT_B is released to high-Z at which time an external resistor is expected to pull INIT_B High. INIT_B can externally be held Low during power-up to stall the power-on configuration sequence at the end of the initialization process. When a High is detected at the INIT_B input after the initialization process, the FPGA proceeds with the remainder of the configuration sequence dictated by the M[2:0] pin settings. Connect INIT_B to a ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure clean Low-to-High transitions.



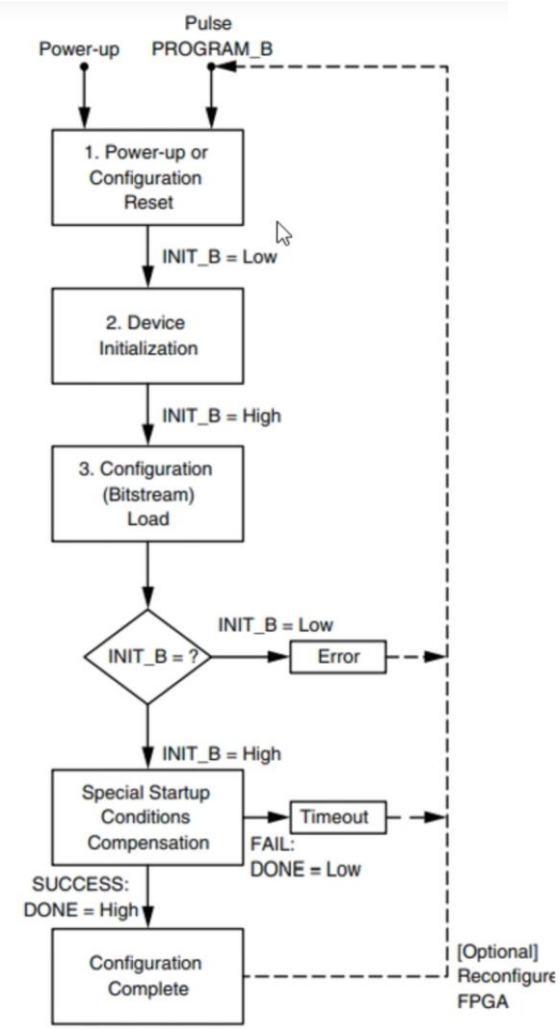
Configuration Pin Definitions

DONE：當燒錄完成拉高
PUDC_B :在配置完成前決定電阻是否上拉

Table 2-4: **Configuration Pin Definitions *(Cont'd)***

Pin Name	Bank(1)	Type	Direction	Description
DONE	0	Dedicated	Bidirectional	Done A High signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default. ***Note:*** DONE has an internal pull-up resistor of approximately 10 kΩ. There is no setup/hold requirement for the DONE register. These changes, along with the DonePipe register software default, eliminate the need for the DriveDONE driver-option. External 330Ω resistor circuits are not required but can be used as they have been in previous generations.
PUDC_B	14	Multi-function	Input	Pull-Up During Configuration (bar) Active-Low PUDC_B input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration. • When PUDC_B is Low, internal pull-up resistors are enabled on each SelectIO pin. • When PUDC_B is High, internal pull-up resistors are disabled on each SelectIO pin. PUDC_B must be tied either directly, or via a ≤ 1 kΩ to V_{CCO_14} or GND. When PUDC_B is tied to GND, the activation of internal pull-ups during power-on depends on the power sequence because the PUDC_B control signal is forwarded through an input buffer in bank 14 and internal paths to the enables of internal pull-ups at applicable pins in their respective I/O banks. An external pull-up resistor is recommended between a pin and the pin's V_{CCO} power supply when it is critical for the pin to be pulled High immediately as the pin's V_{CCO} power ramps up. ***Caution!*** Do not allow this pin to float before and during configuration.

Serial Configuration Mode



Clocking Serial Configuration Data

Figure 2-3 shows how configuration data is clocked into 7 series devices in Slave Serial and Master Serial modes.

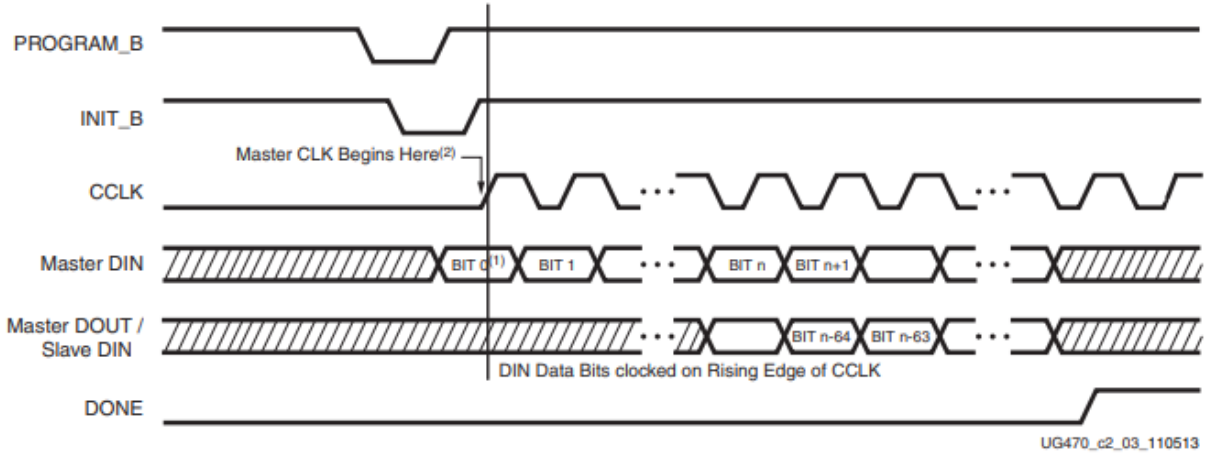


Figure 2-3: **Serial Configuration Clocking Sequence**

Notes relevant to Figure 2-3:

1. Bit 0 represents the MSB of the first byte. For example, if the first byte is `0xAA` (`1010_1010`), bit 0 = `1`, bit 1 = `0`, bit 2 = `1`, etc.
2. For Master configuration mode, CCLK is driven only after INIT_B goes High to shortly after DONE goes High. Otherwise CCLK is in a high-Z state. Data sheet timing is relative to the CCLK pin.
3. CCLK can be free-running in Slave Serial mode.

Slave Serial Mode Configuration Example

Slave Serial Configuration

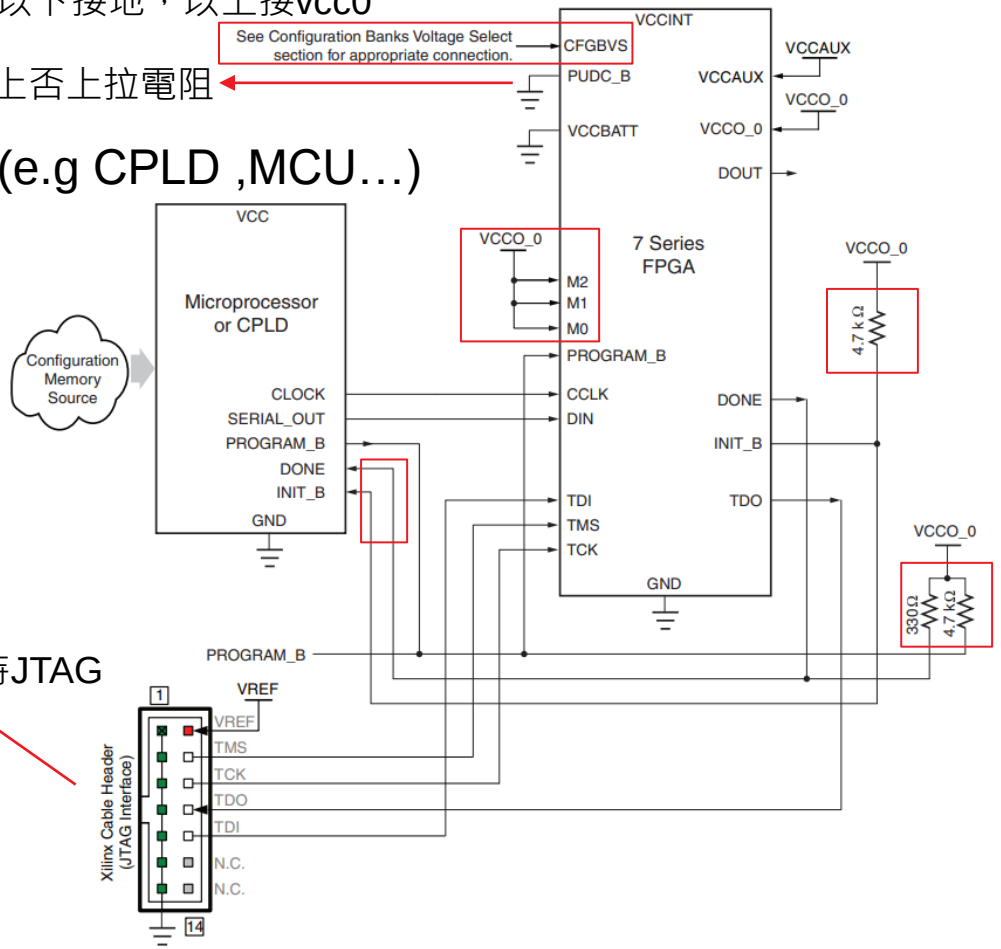
Slave Serial configuration is typically used for devices in a serial daisy chain or when configuring a single device from an external microprocessor or CPLD (see Figure 2-2). Design considerations are similar to Master Serial configuration except for the direction of CCLK. CCLK must be driven from an external clock source, which also provides data (see Clocking Serial Configuration Data, page 35). For daisy chain information, see Chapter 9, Multiple FPGA Configuration.

1.8v以下接地，以上接vcc0

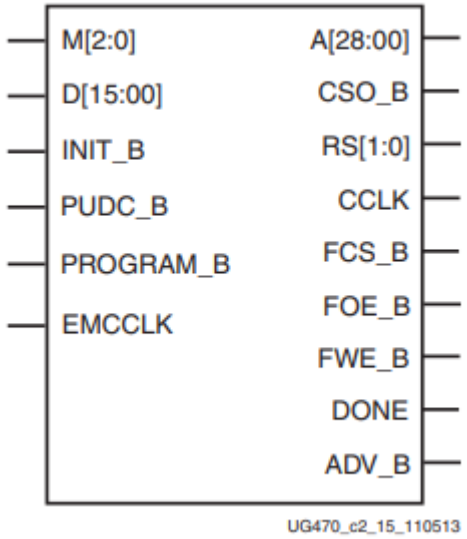
配置完成前，決定上否上拉電阻

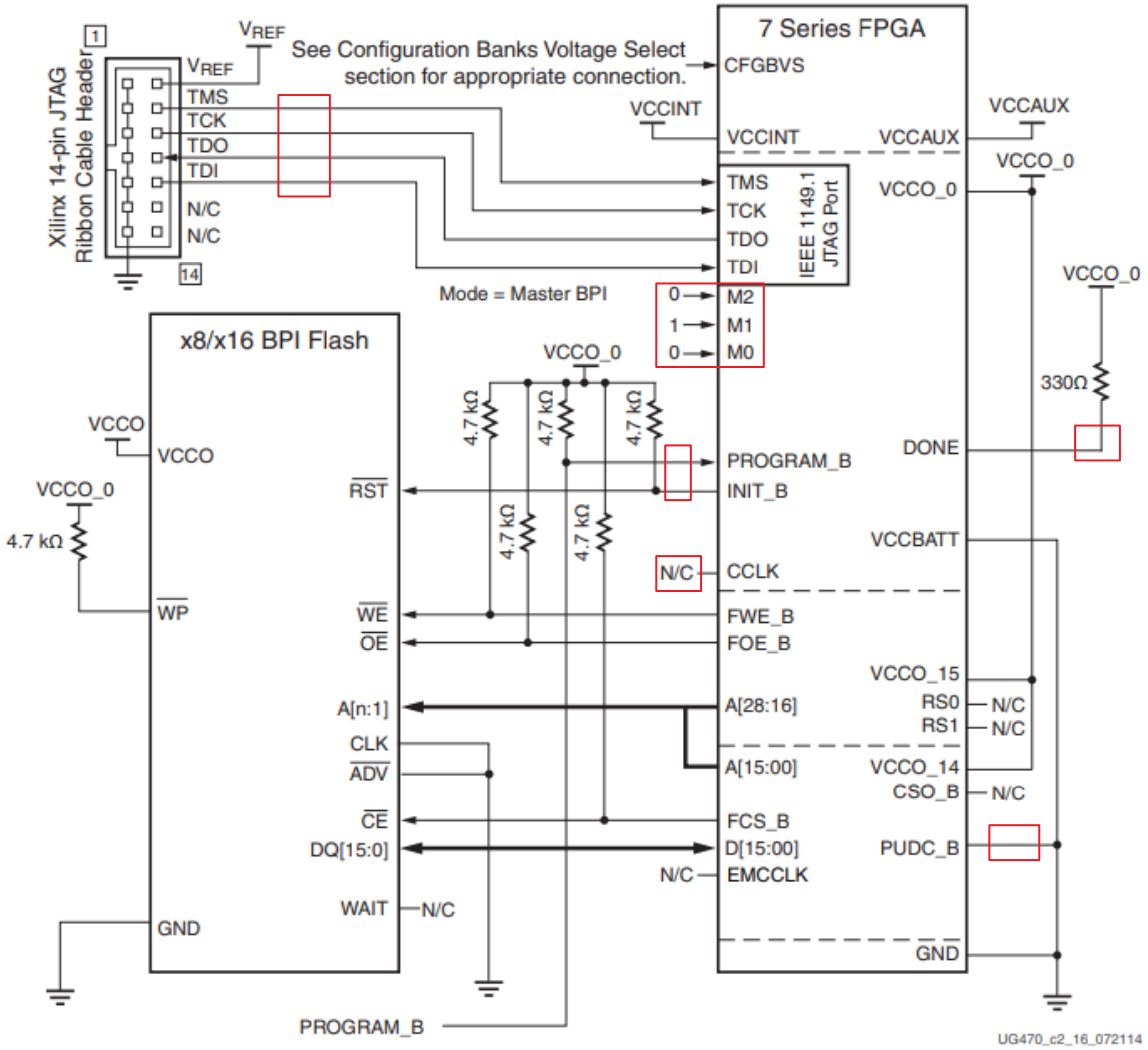
Master(e.g CPLD ,MCU…)

任何模式都可以支持JTAG



Master BPI Configuration





Master SPI Configuration

因為是Master，所以時鐘由FPGA提供

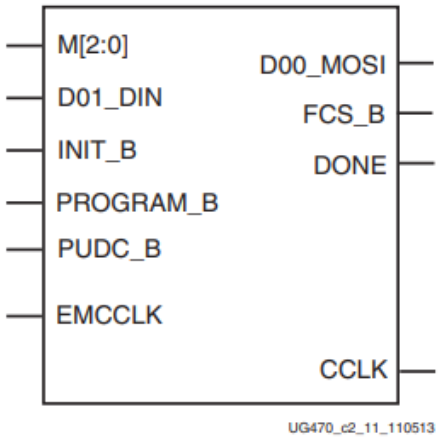


Figure 2-11: **7 Series FPGA SPI Configuration Interface**

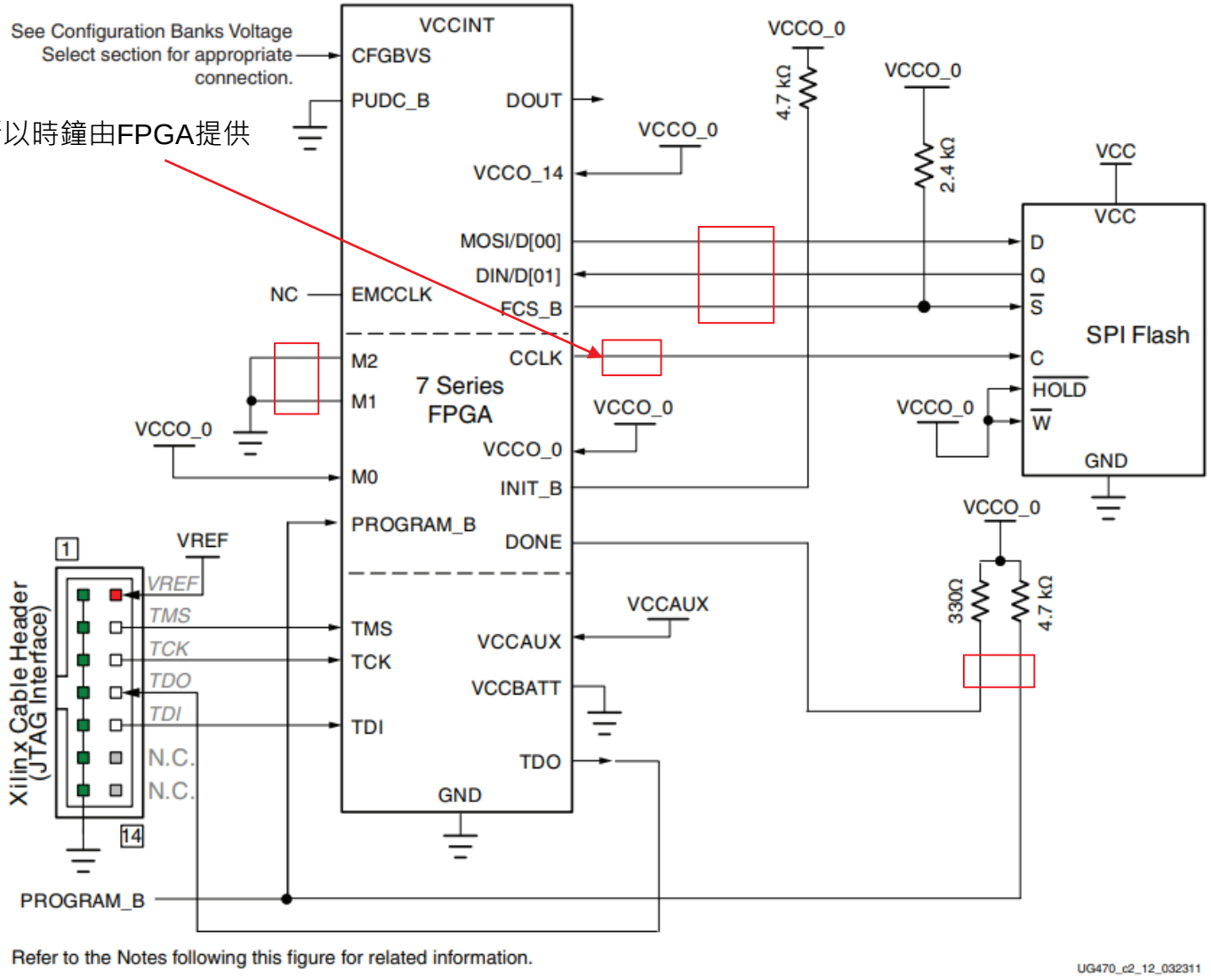
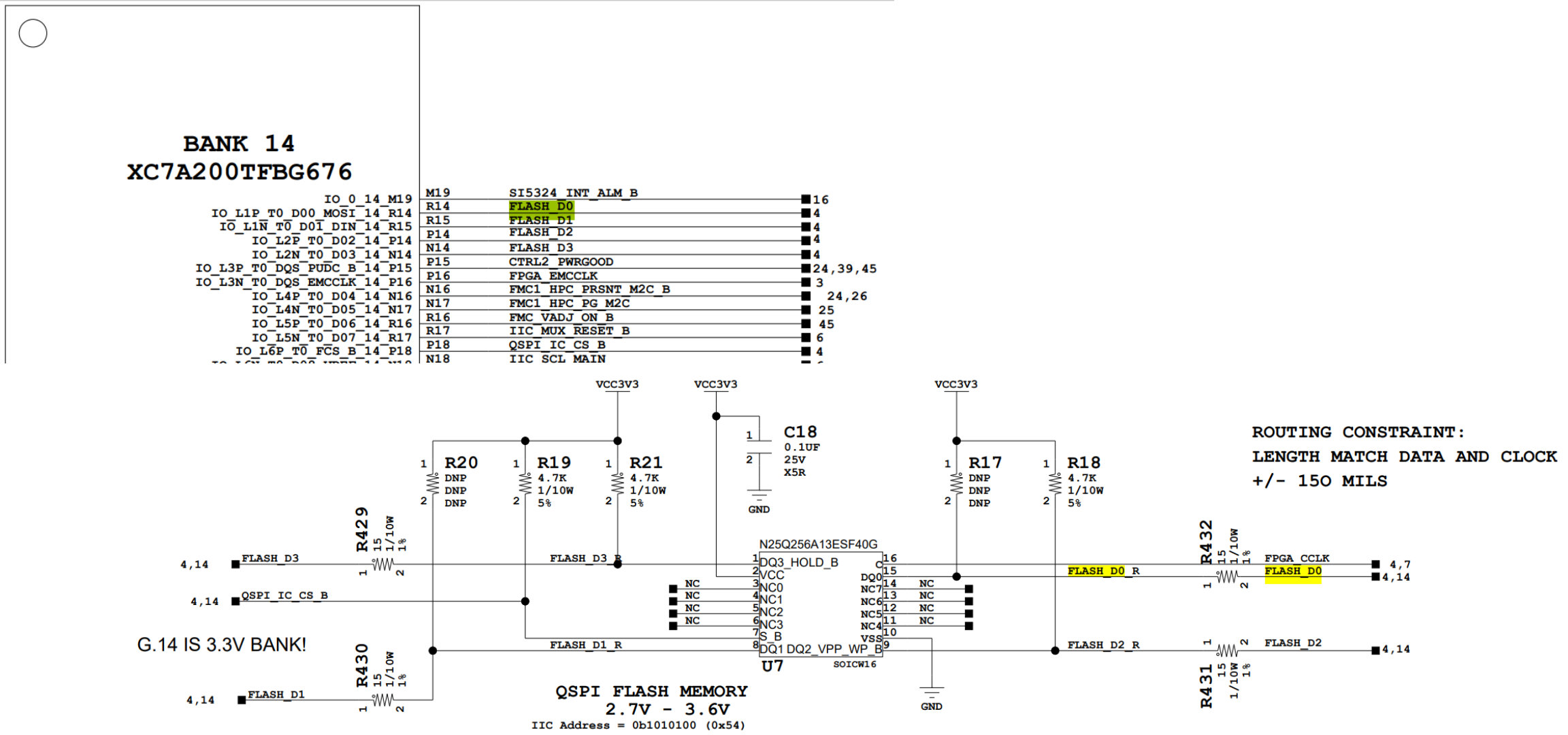
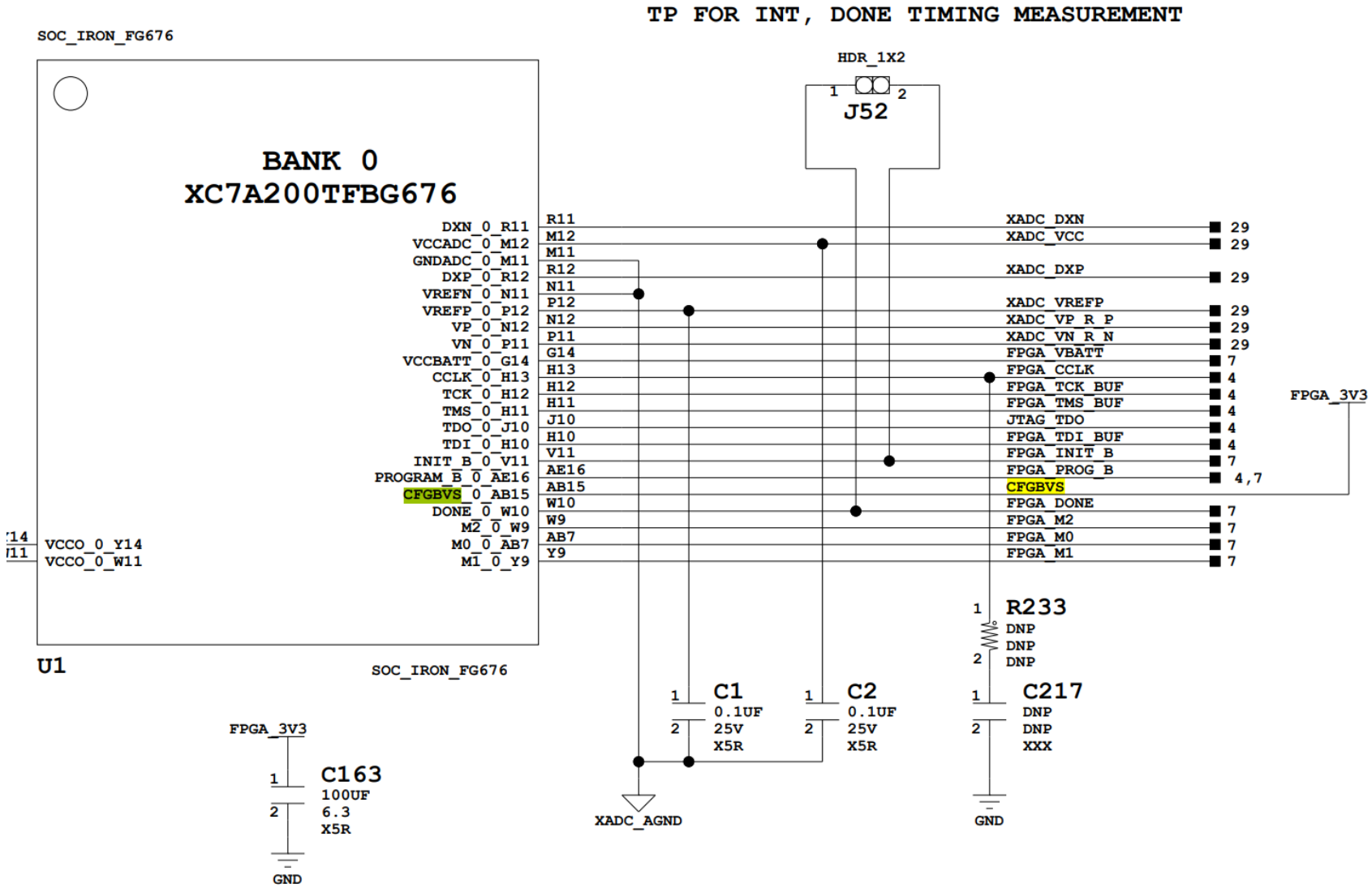


Figure 2-12: **7 Series FPGA SPI x1/x2 Configuration Interface**

AC701 Schematic

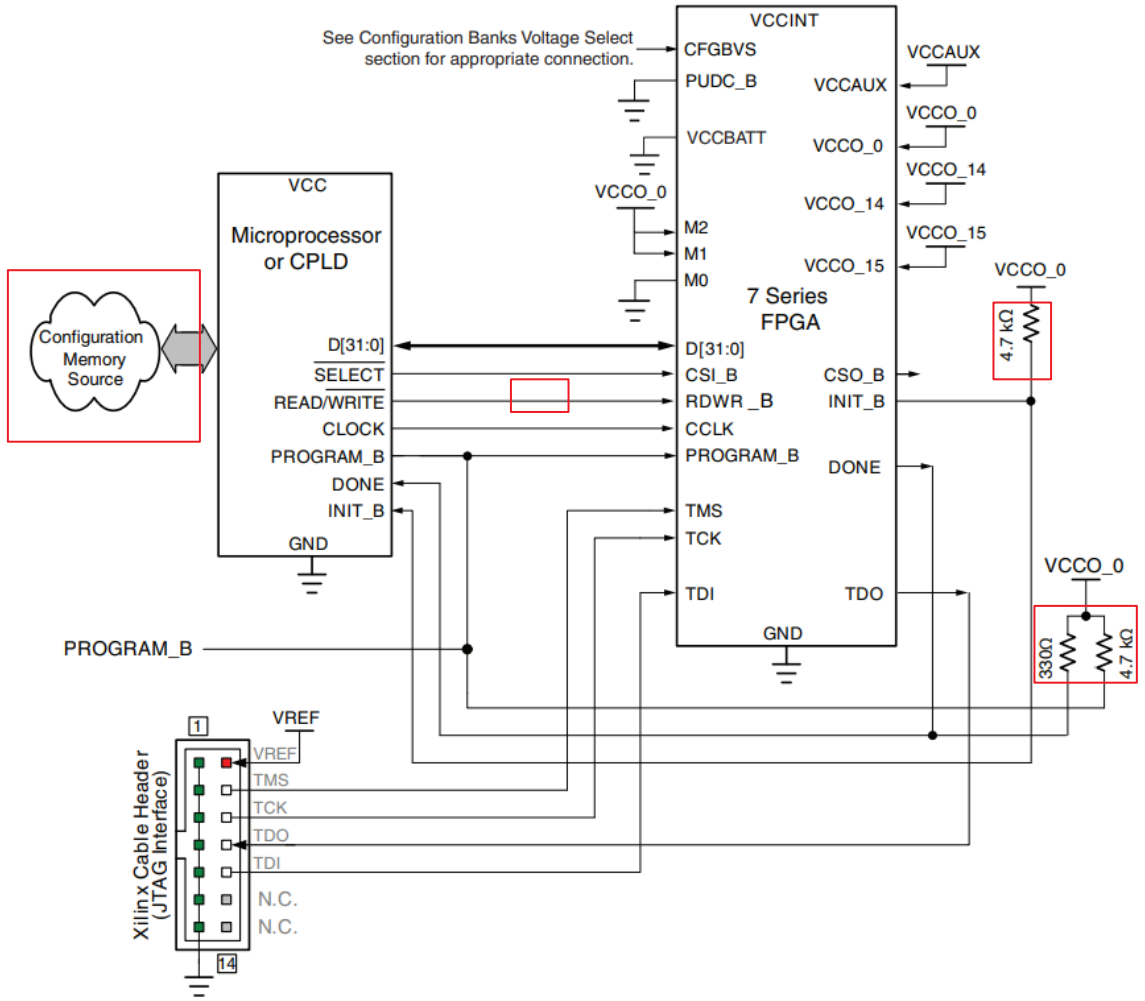


AC701 Schematic



SelectMAP Configuration

當FPGA要做功能的升級或遠端加載時(動態加載)，會需要一個能對外的接口，就會使用SelectMAP或是JTAG。



SelectMAP Configuration

RDWR_B	14	Multi-function	Input	Read/Write (bar) RDWR_B determines the direction of the SelectMAP data bus. When RDWR_B is High, the FPGA outputs read data onto the SelectMAP data bus. When RDWR_B is Low, an external controller can write data to the FPGA through the SelectMAP data bus. • For master SelectMAP mode: Connect RDWR_B directly, or via a ≤ 1 kΩ resistor, to GND. • For slave SelectMAP mode: An external device controls the RDWR_B signal to control the direction of the SelectMAP data bus for read/write from/to the SelectMAP interface. • In all other modes: RDWR_B is ignored and can be left unconnected.

Figure 2-6 summarizes the timing of SelectMAP configuration with continuous data loading.

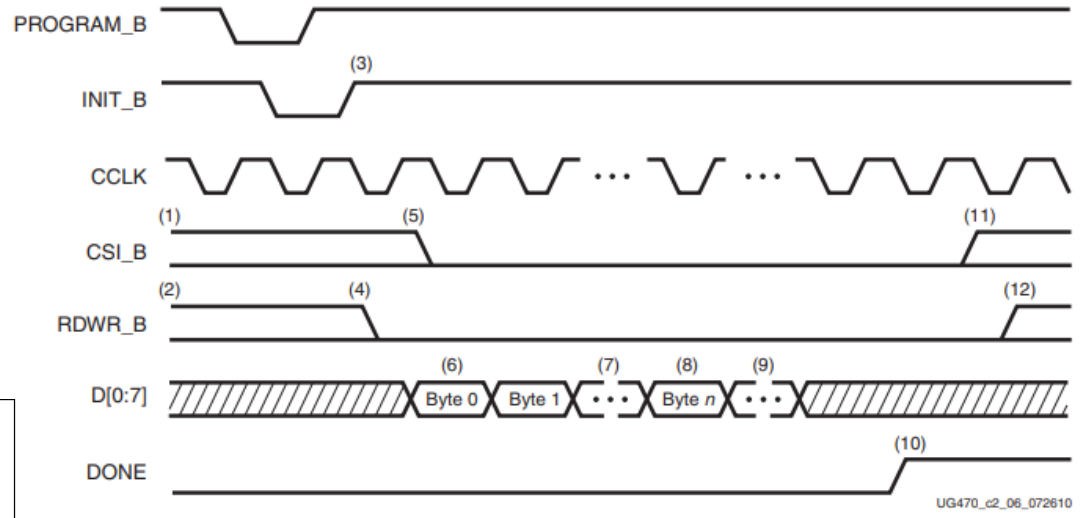


Figure 2-6: **Continuous x8 SelectMAP Data Loading**

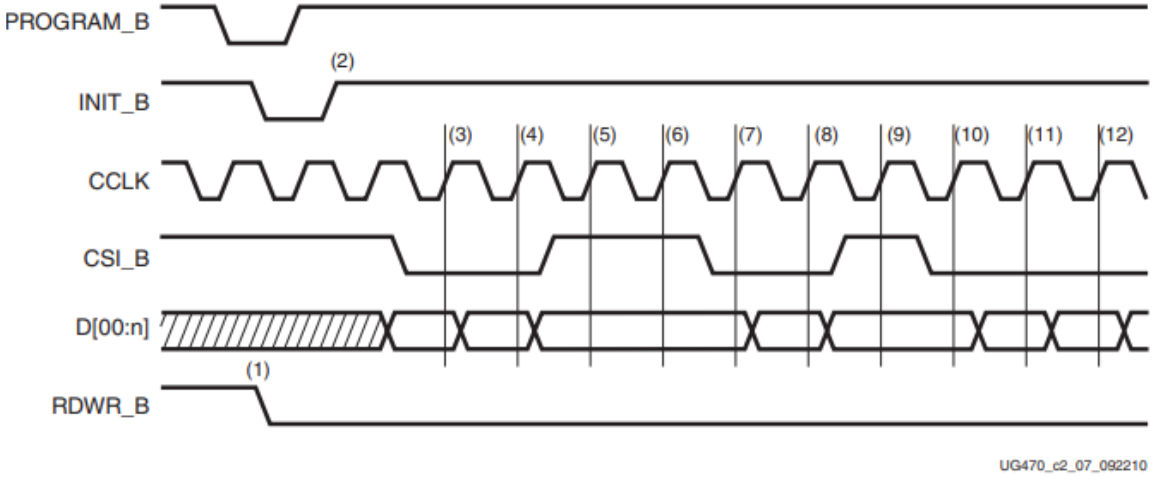


Figure 2-7: **Non-Continuous SelectMAP Data Loading with Free-Running CCLK**

JTAG Controller Pins

Table 3-1: **7 Series FPGA TAP Controller Pins**(1)

Pin	Direction	Pre-Configuration Internal Pull Resistor	Description
TDI	In	Pull-up	**Test Data In**. This pin is the serial input to all JTAG instruction and data registers. The state of the TAP controller and the current instruction determine the register that is fed by the TDI pin for a specific operation. TDI has an internal resistive pull-up to provide a logic High to the system if the pin is not driven. TDI is applied into the JTAG registers on the rising edge of TCK.
TDO	Out	Pull-up	**Test Data Out**. This pin is the serial output for all JTAG instruction and data registers. The state of the TAP controller and the current instruction determine the register (instruction or data) that feeds TDO for a specific operation. TDO changes state on the falling edge of TCK and is only active during the shifting of instructions or data through the device. TDO is an active driver output. TDO has an internal resistive pull-up to provide a logic High if the pin is not active.
TMS	In	Pull-up	**Test Mode Select**. This pin determines the sequence of states through the TAP controller on the rising edge of TCK. TMS has an internal resistive pull-up to provide a logic High if the pin is not driven.
TCK	In	Pull-up	**Test Clock**. This pin is the JTAG Test Clock. TCK sequences the TAP controller and the JTAG registers. TCK has an internal resistive pull-up to provide a logic High if the pin is not driven.

Notes:

1. TMS and TDI have internal pull-up resistors, as specified by IEEE Std 1149.1, as do TDO and TCK. These internal pull-up resistors are active, regardless of the mode selected. Refer to the respective 7 series FPGAs data sheet for internal pull-up values. Bitstream options can be used to enable the pull-up or pull-down resistor after configuration for all four mandatory pins. See UG628, *Command Line Tools User Guide* for more information.

Boundary-Scan Timing Parameters

Characterization data for some of the most commonly requested timing parameters, shown in Figure 3-1, are listed in the respective 7 series FPGAs data sheet in the Configuration Switching Characteristics table.

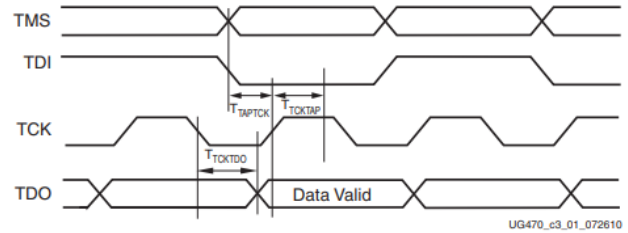


Figure 3-1: **7 Series FPGA Boundary-Scan Port Timing Waveforms**

TCK (clock): 上升沿輸入 ，下降沿輸出
TMS (狀態選擇):上升沿待測晶片，下降沿模擬器
TDI(data input):上升沿待測晶片，下降沿模擬器
TDO(data output):上升沿模擬器，下降沿待測晶片