AMD
XILINX

Vivado Debug Tools

Course Agenda
2023

Agenda

- Integrated Logic Analyzer (ILA)
- Virtual Input/Output(VIO)
- Integrated Bit Error Ratio Tester (IBERT)

AMD
XILINX

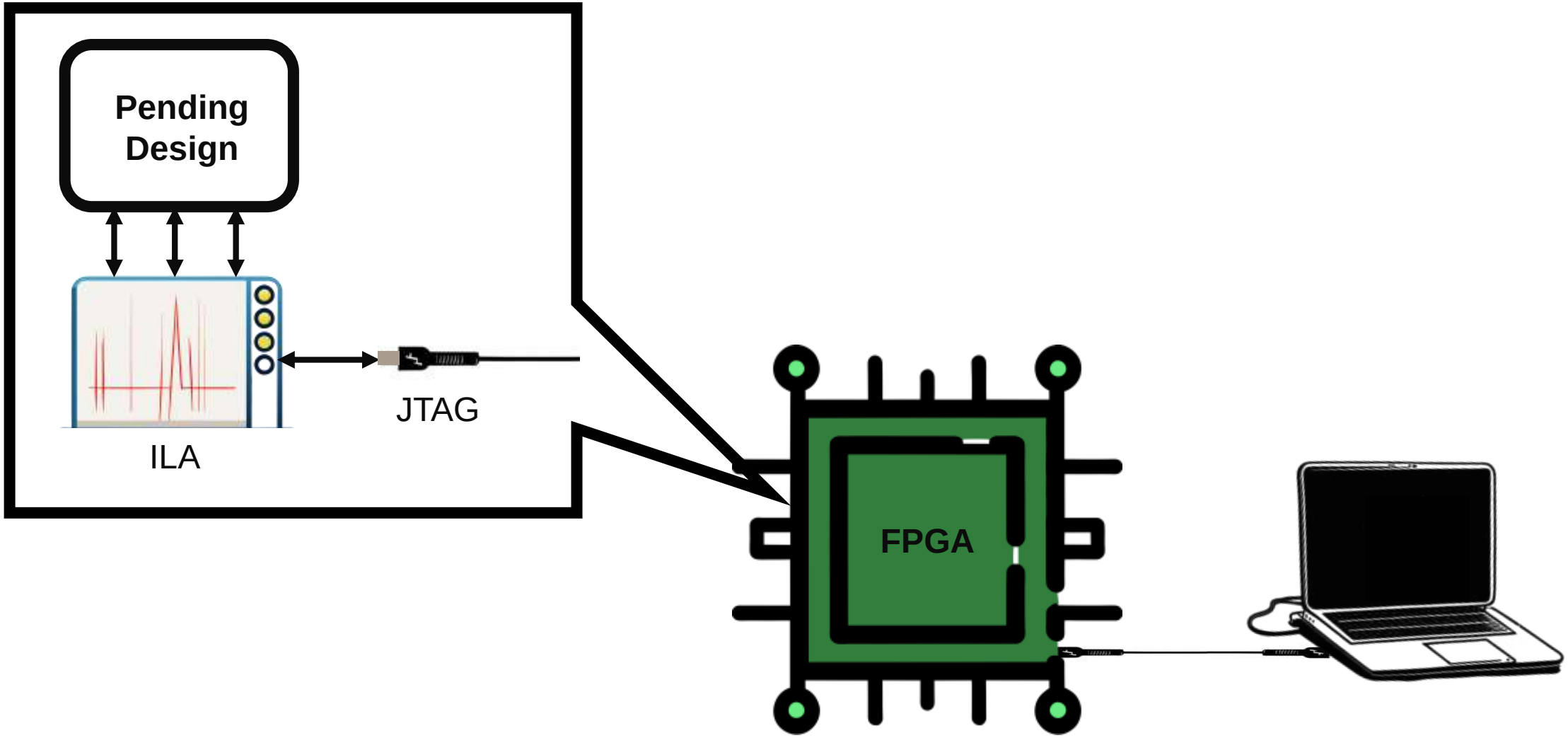
Integrated Logic Analyzer

Course Agenda
2023

Integrated Logic Analyzer

- Several ways to add ILA
- ILA debugging
- ILA IP Setting

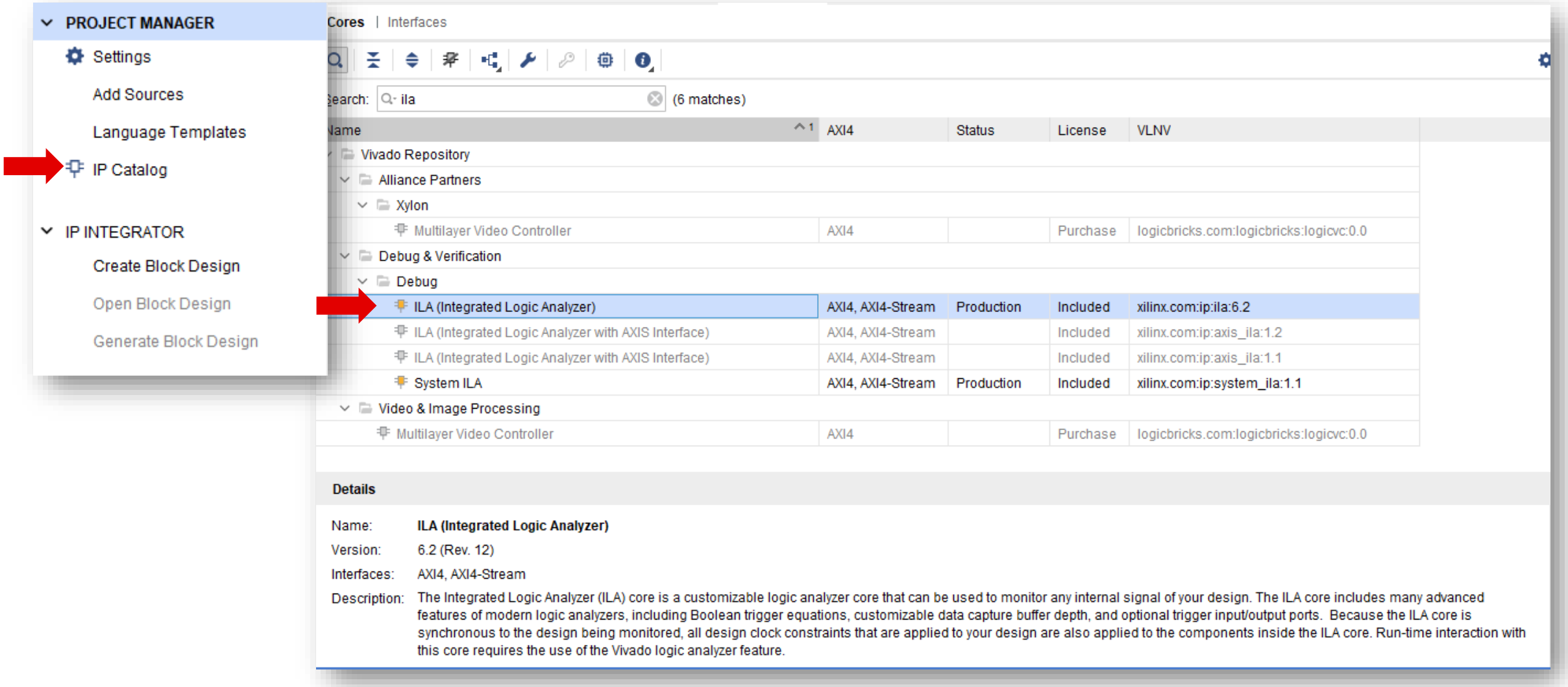
Integrated Logic Analyzer



Several ways to add ILA

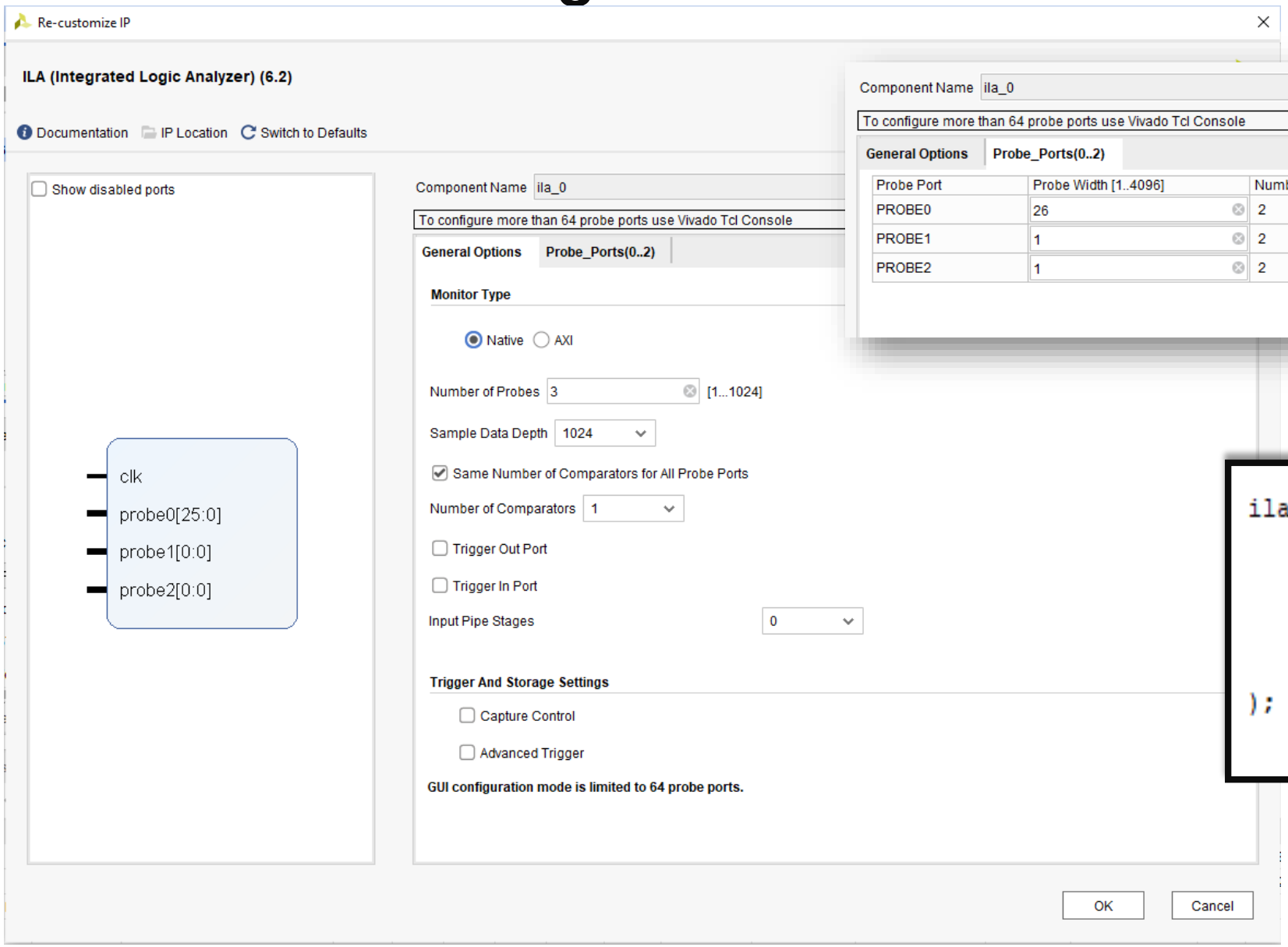
1. Add ILA core through HDL code
2. Add debug mark in the netlist
3. Add ILA core in the block design

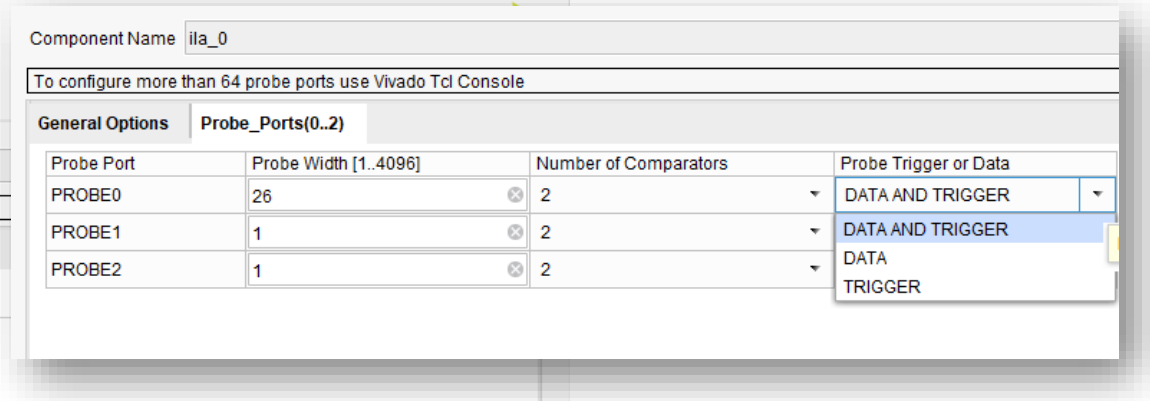
Add ILA core through HDL code



AMD XILINX

Add ILA core through HDL code





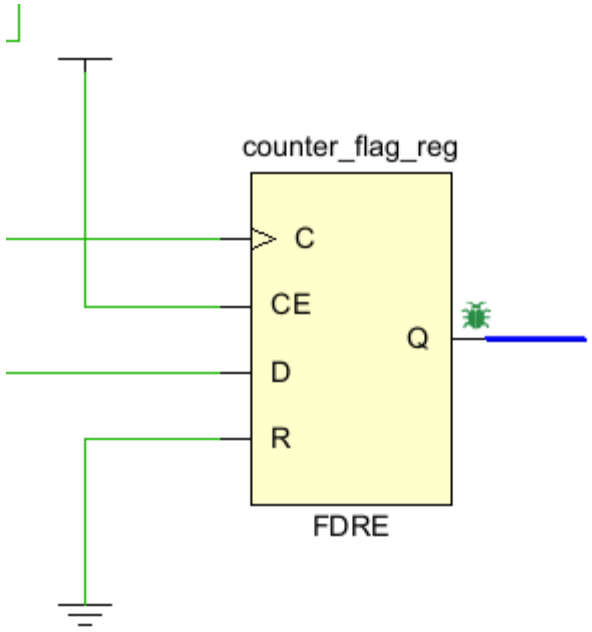

```
ila_0 ila(
    .clk(sys_clk),
    .probe0(counter),
    .probe1(counter_flag),
    .probe2(led_out)
);
```


AMD XILINX

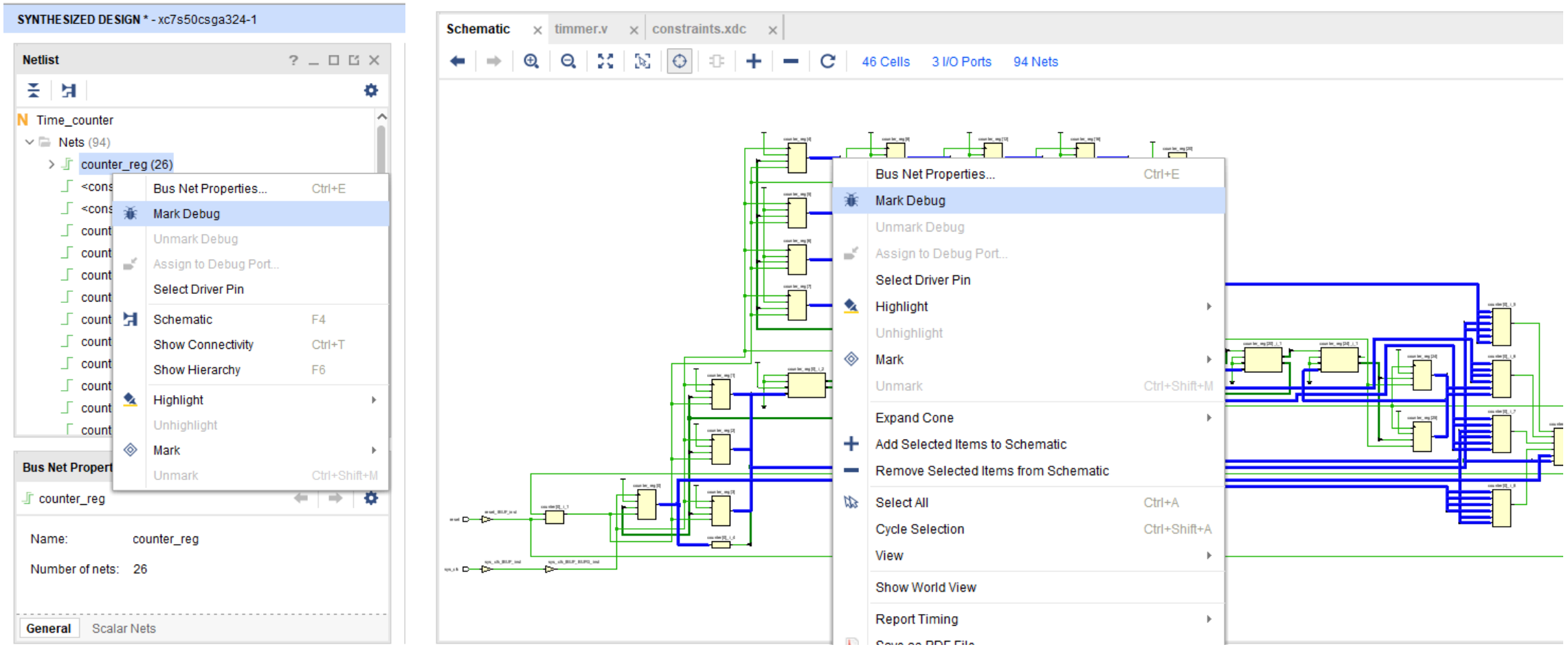
Add debug mark in the netlist

(* mark_debug = “true” *) reg / wire

```
(* mark_debug = "true" *)reg counter_flag;
```

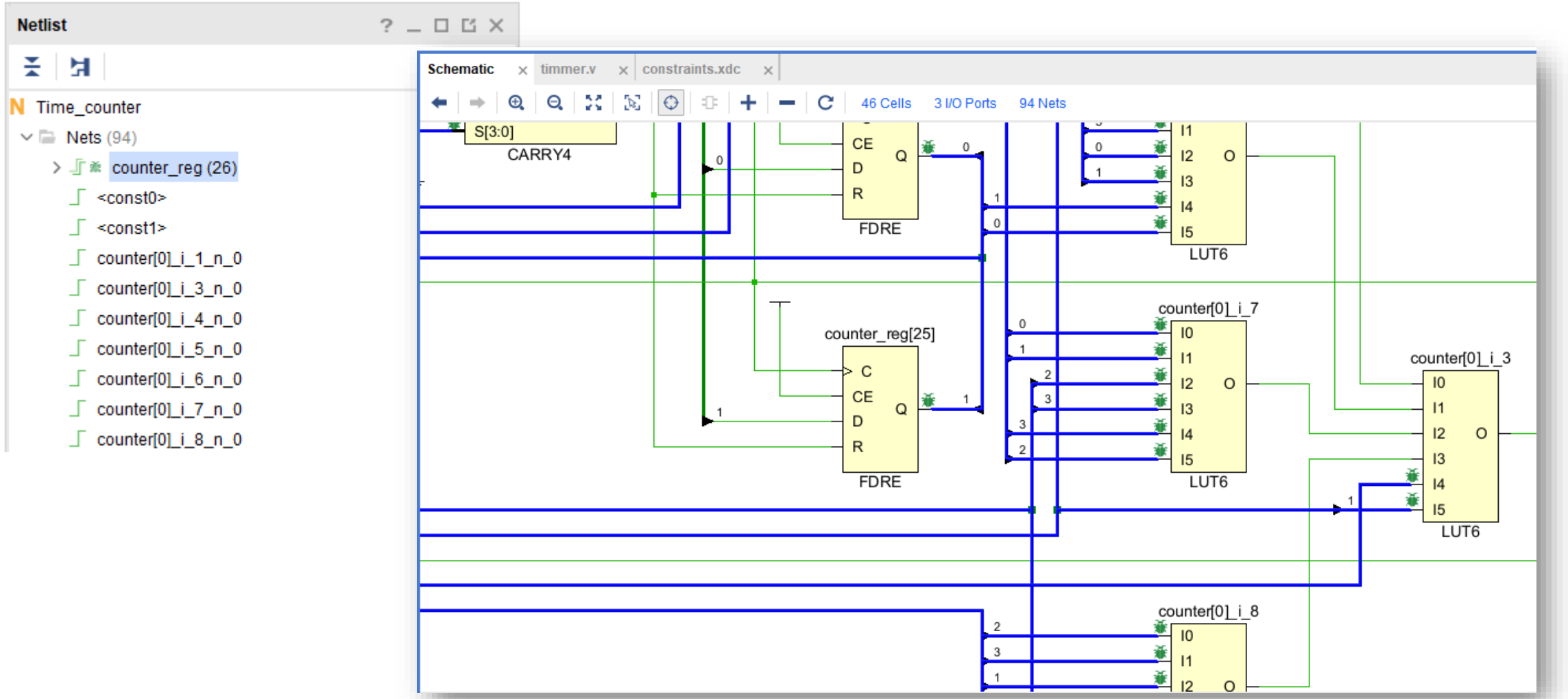


Add debug mark in the netlist

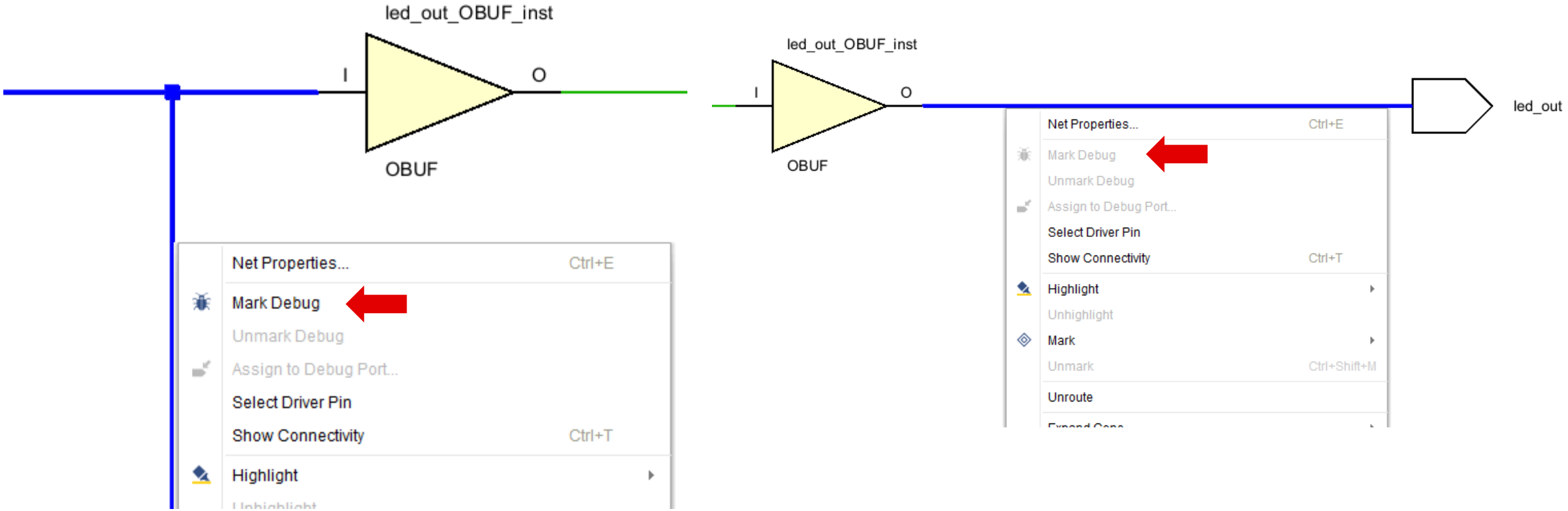


AMD XILINX

Add debug mark in the netlist

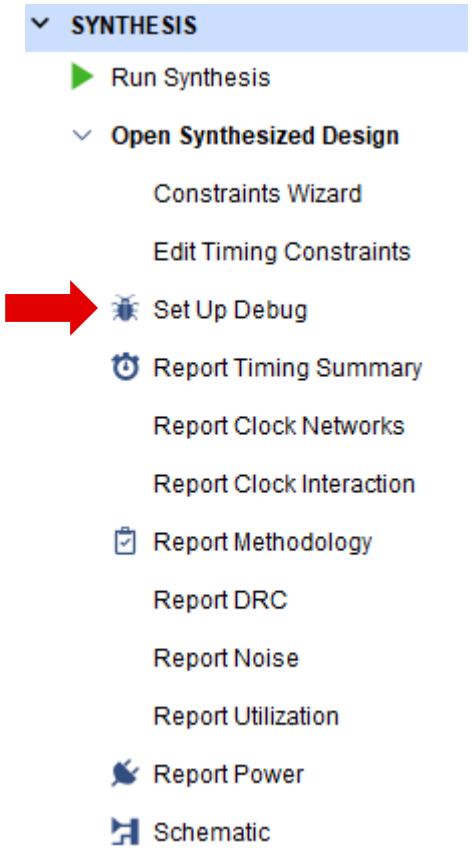


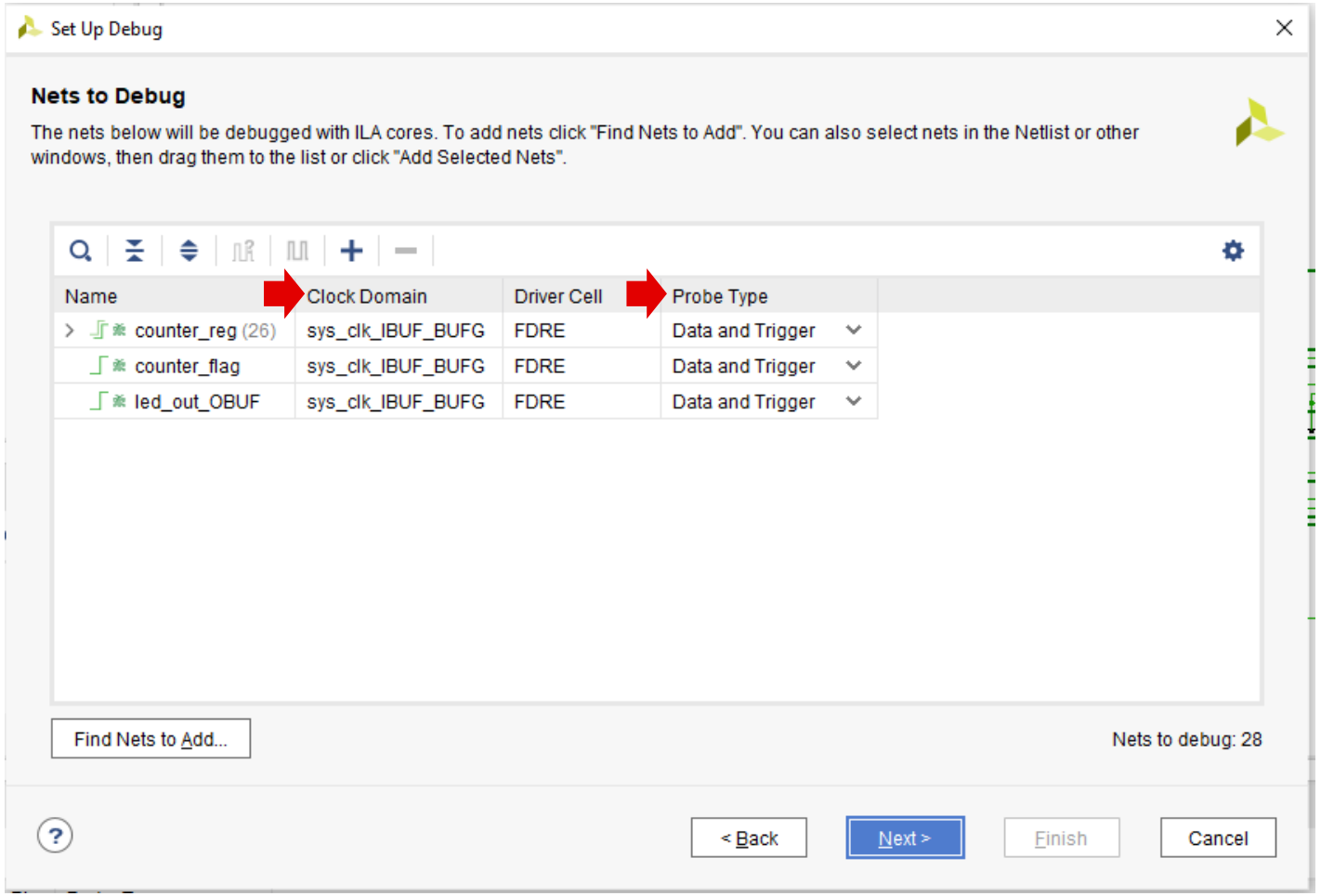
Add debug mark in the netlist



AMD XILINX

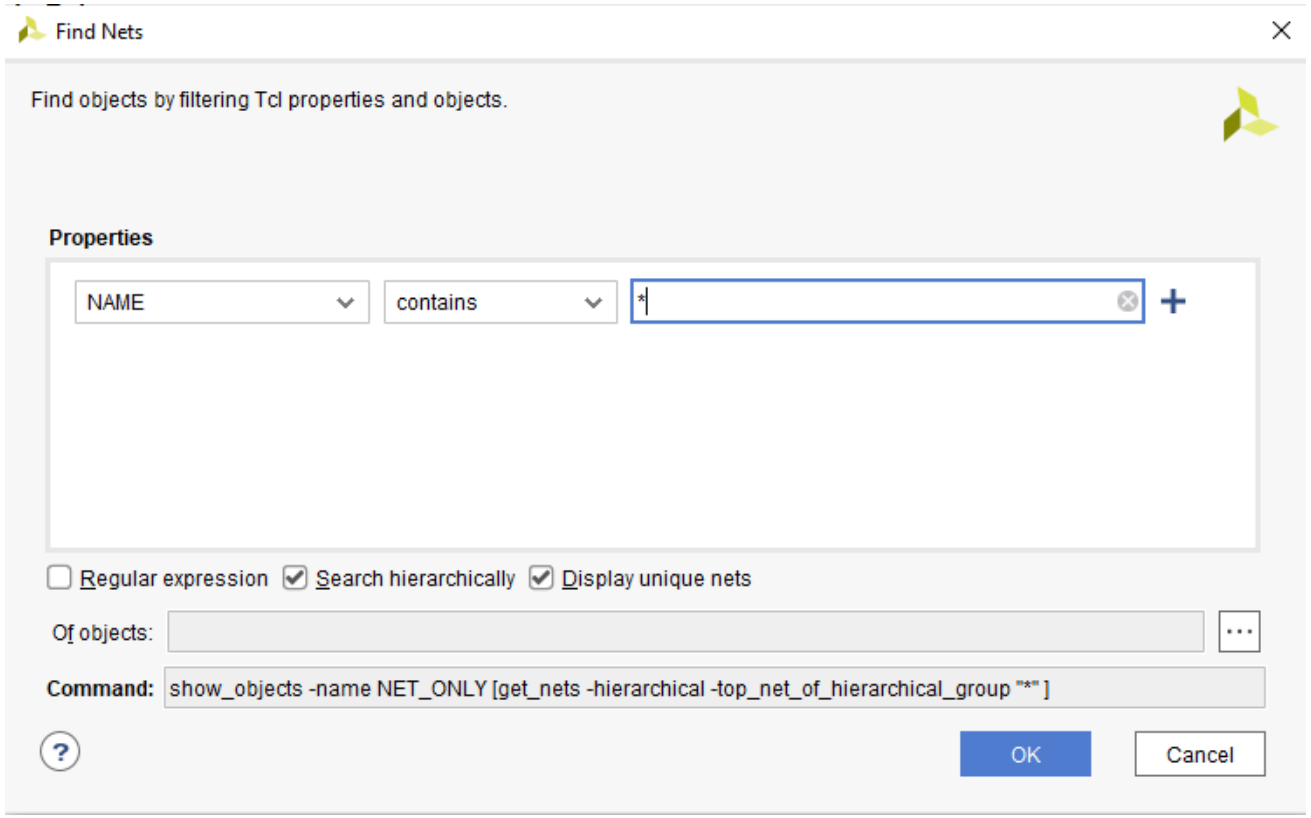
Add debug mark in the netlist

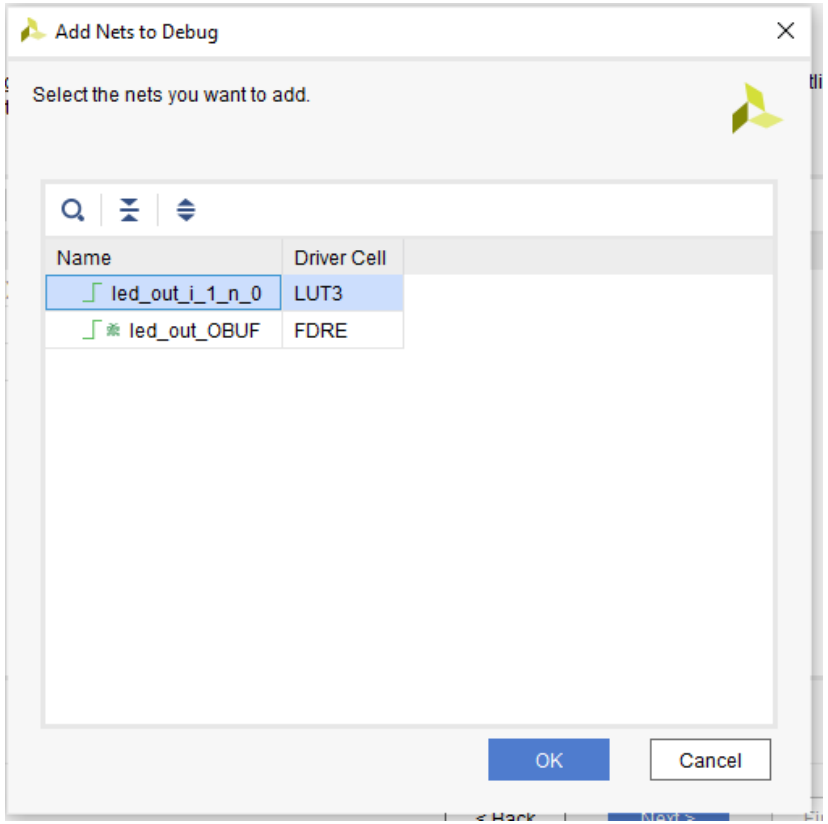




AMD XILINX

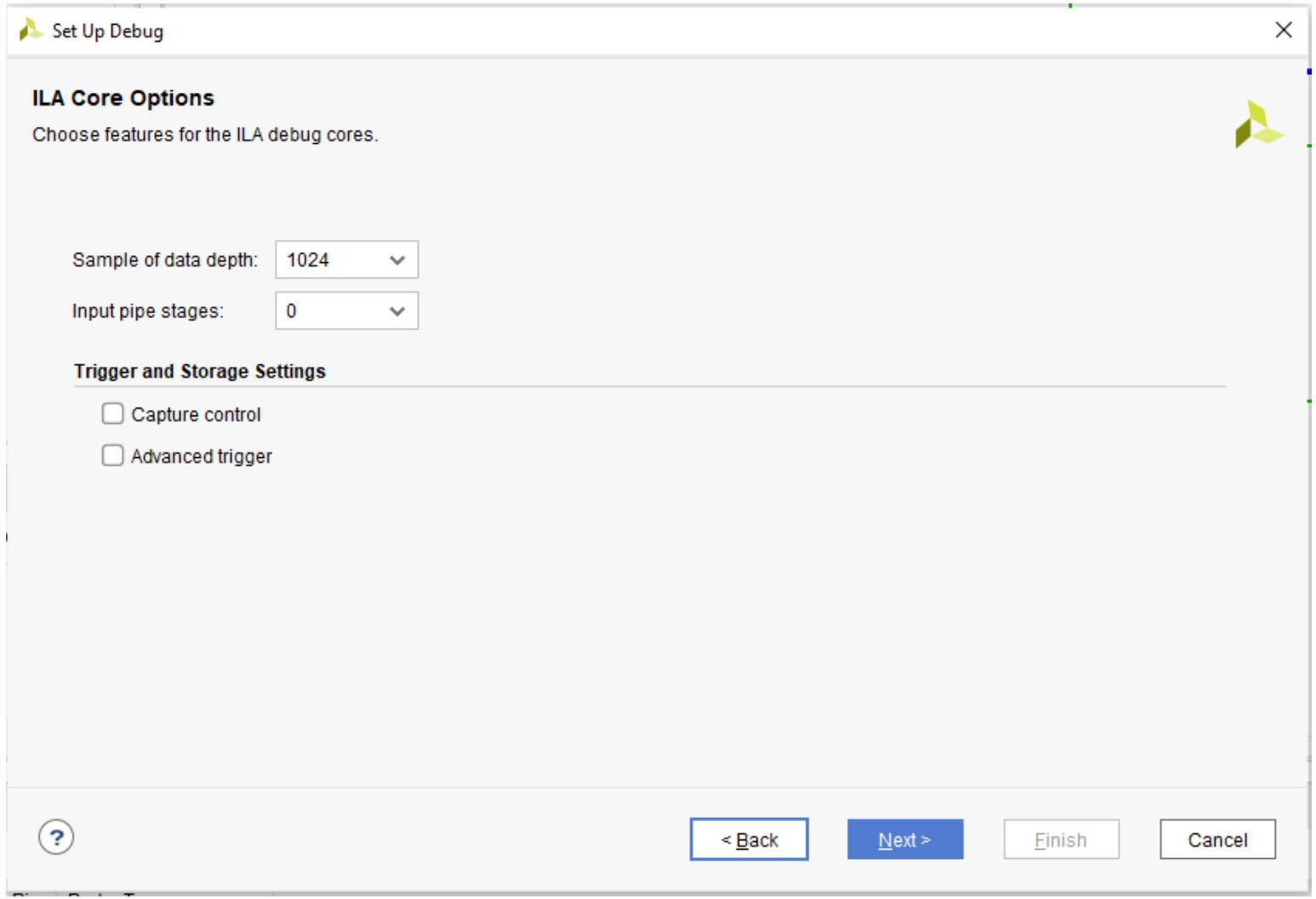
Add debug mark in the netlist





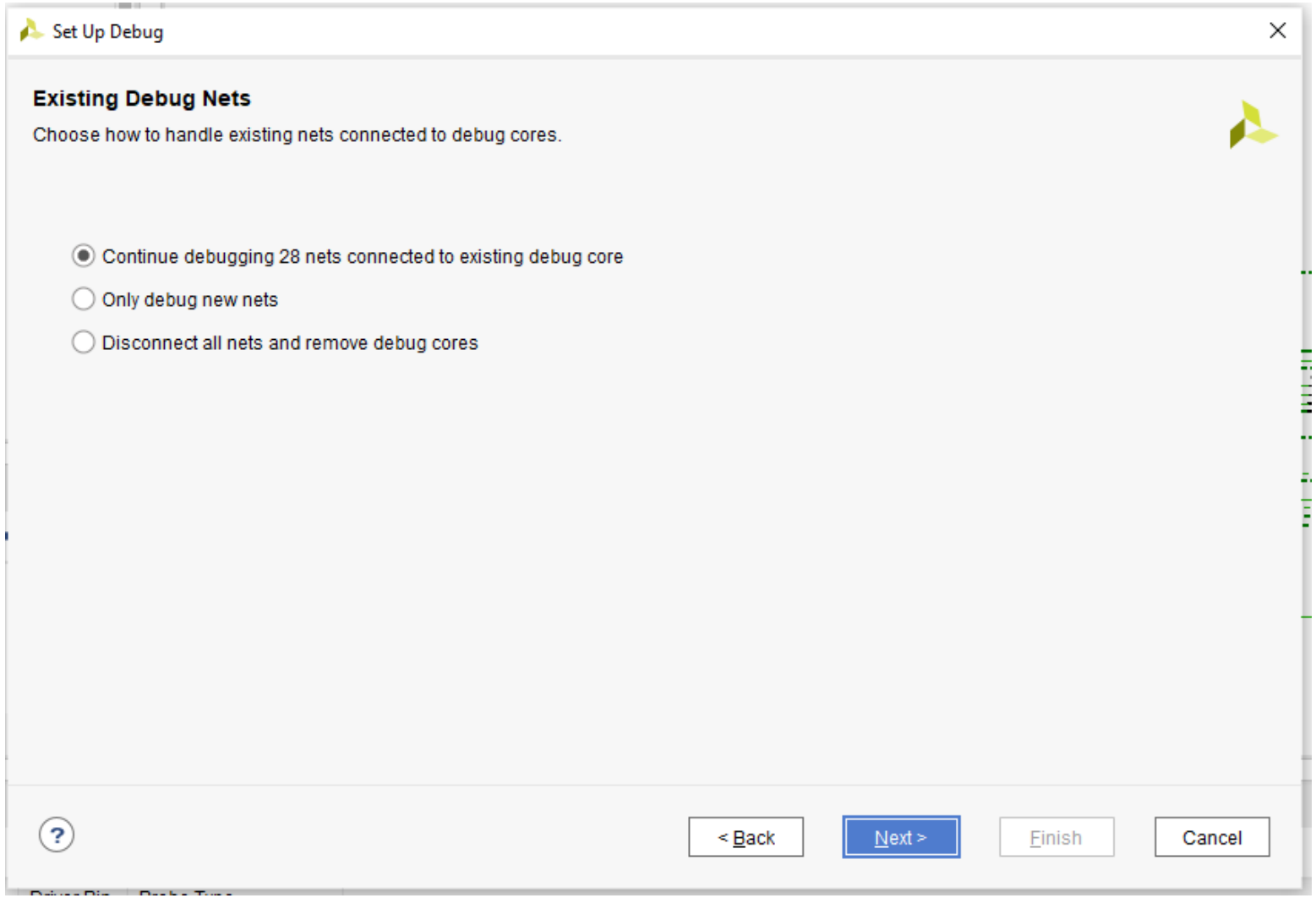
AMD XILINX

Add debug mark in the netlist



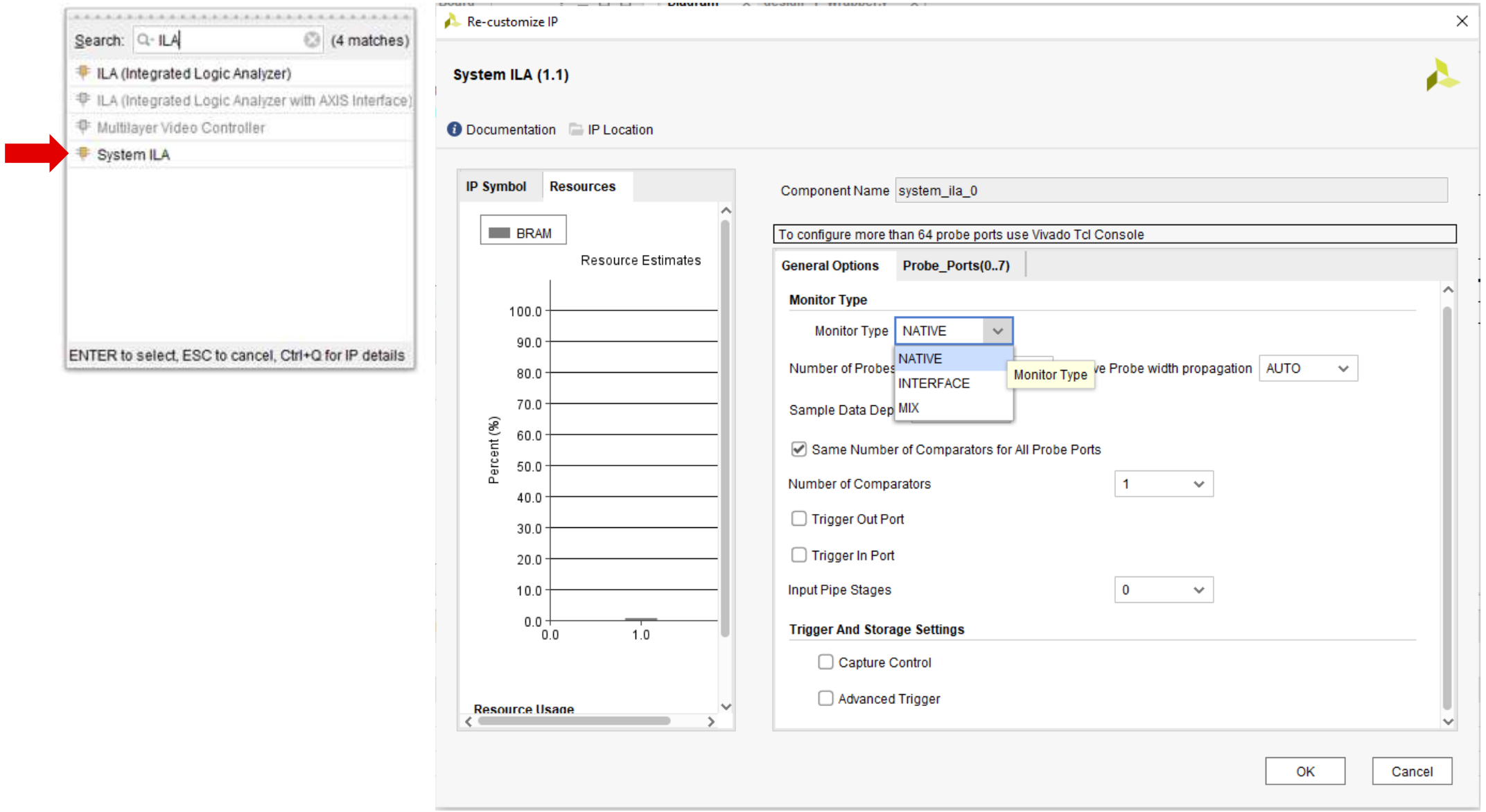
AMD XILINX

Add debug mark in the netlist



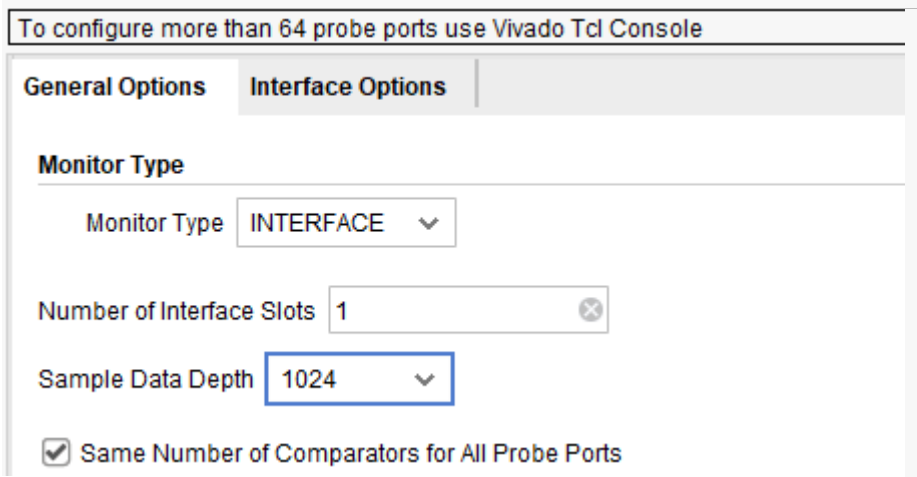
AMD XILINX

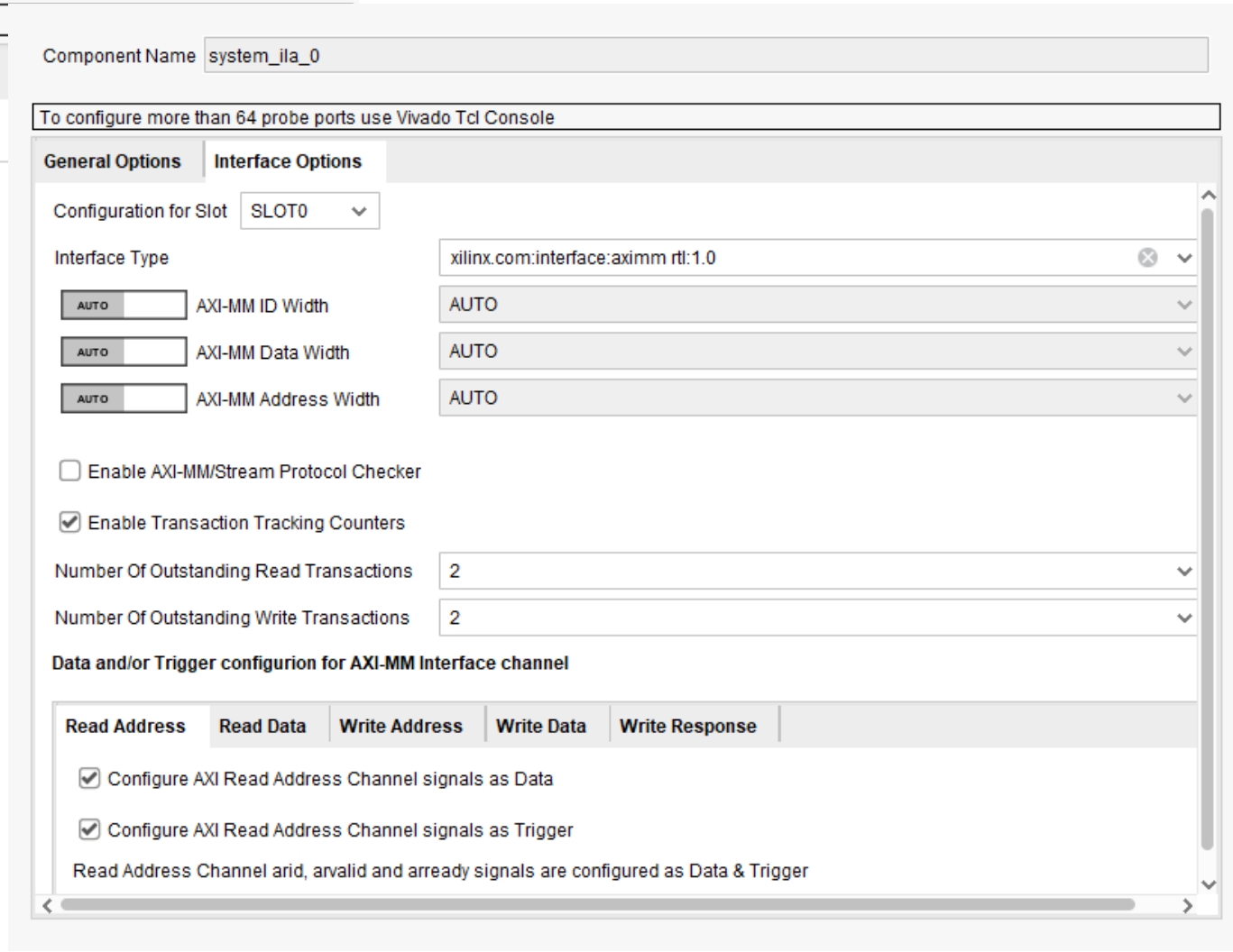
Add ILA core in the block design



AMD XILINX

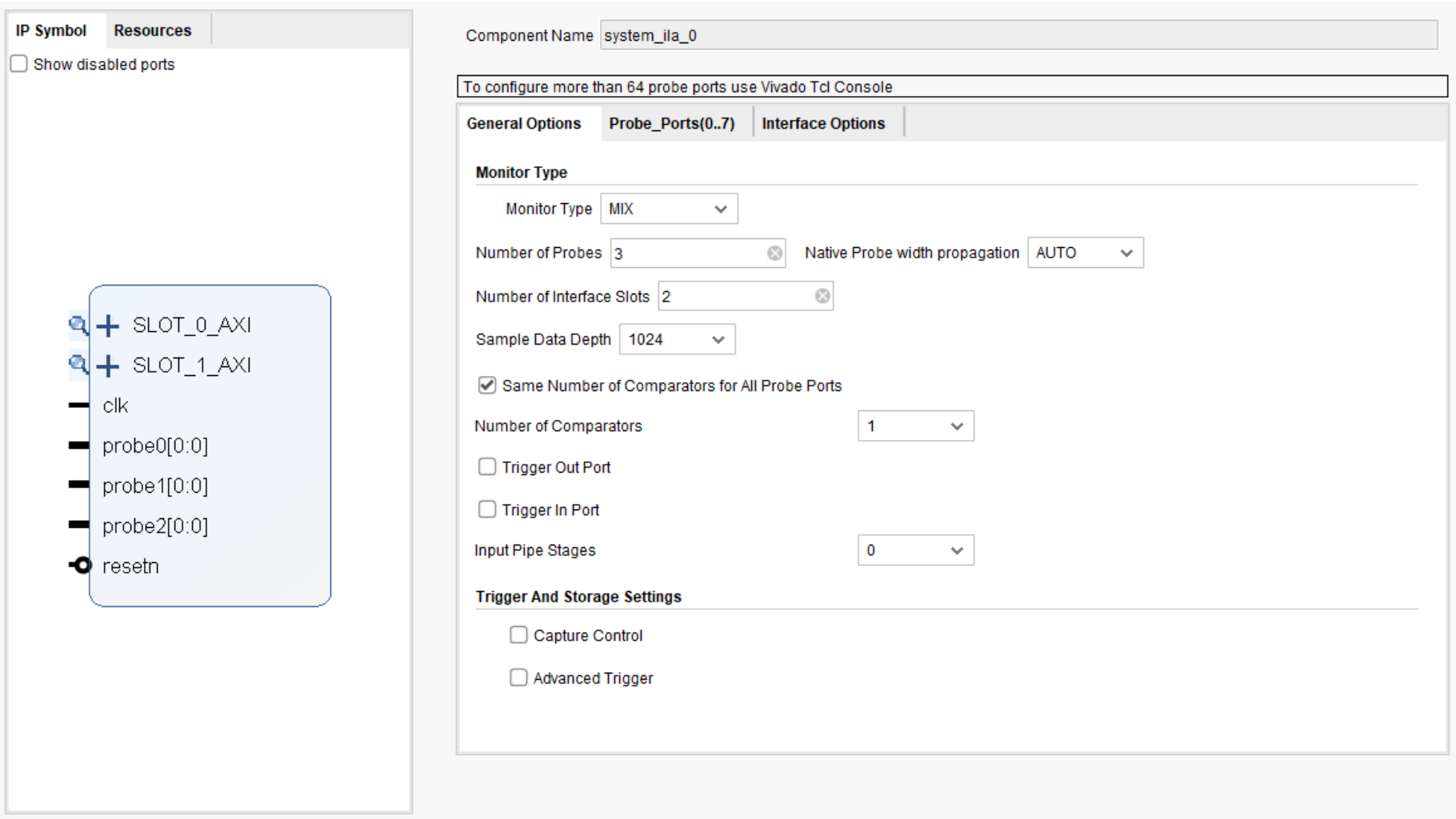
Add ILA core in the block design





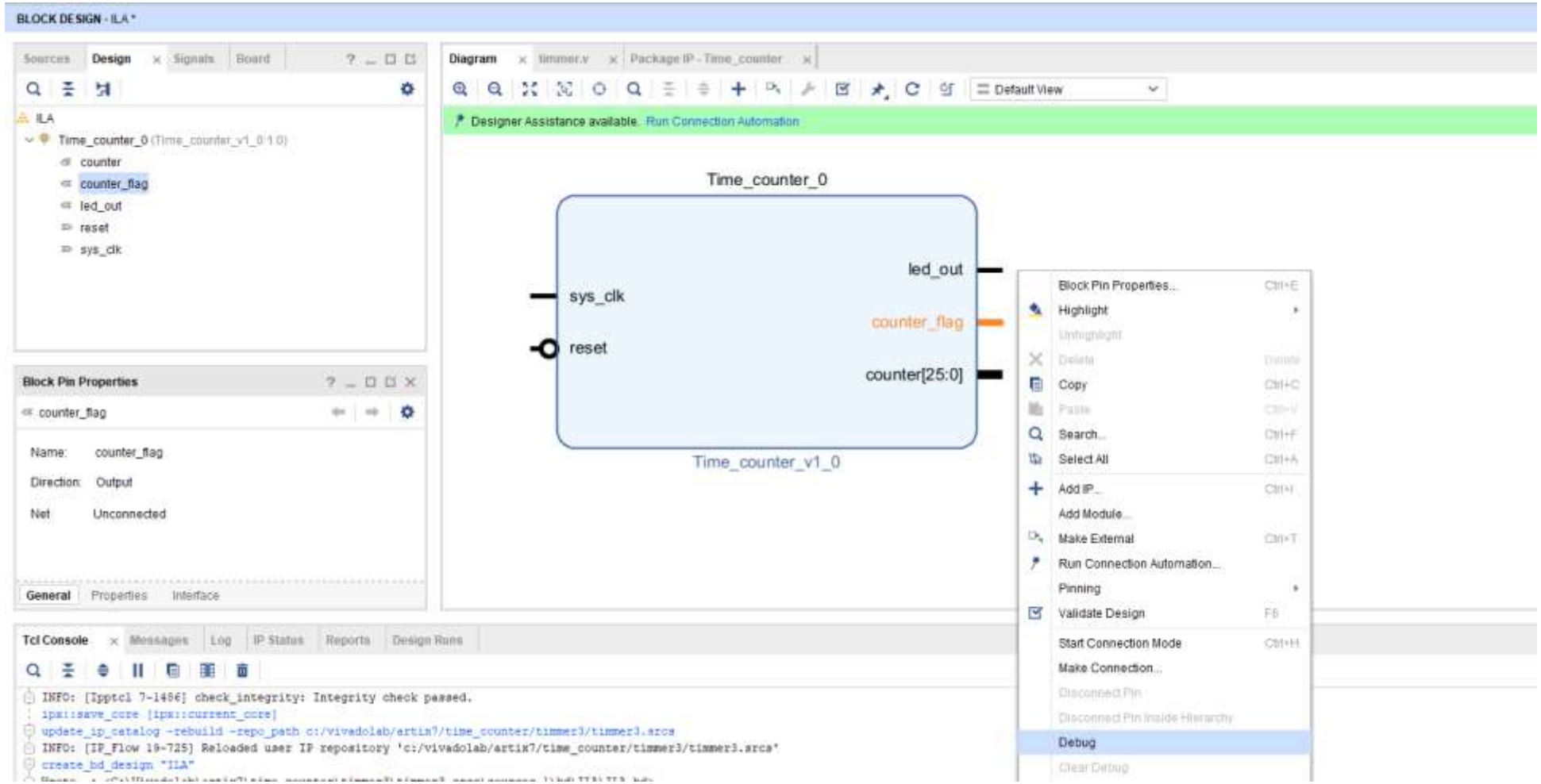
AMD XILINX

Add ILA core in the block design



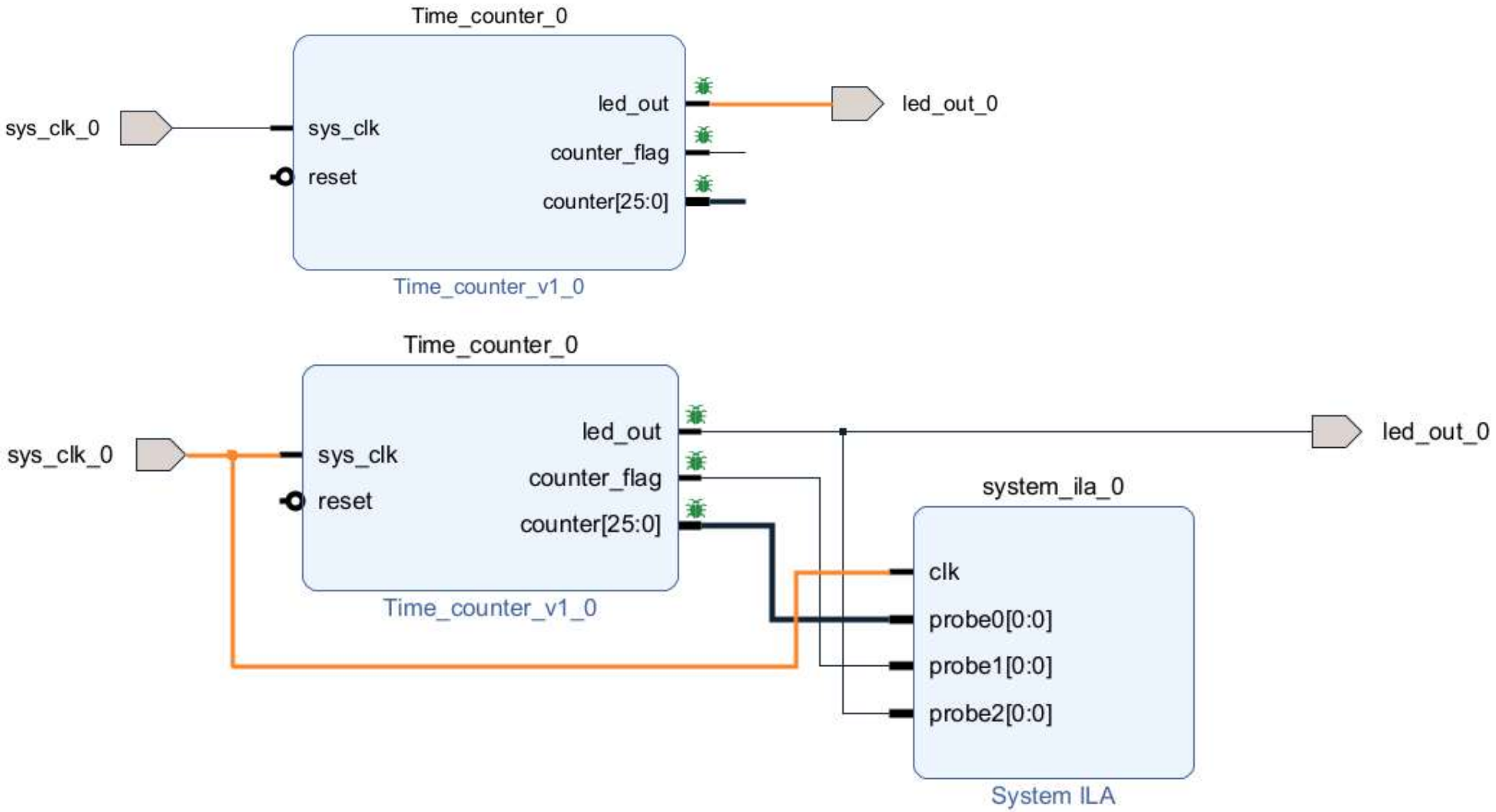
AMD XILINX

Add ILA core in the block design



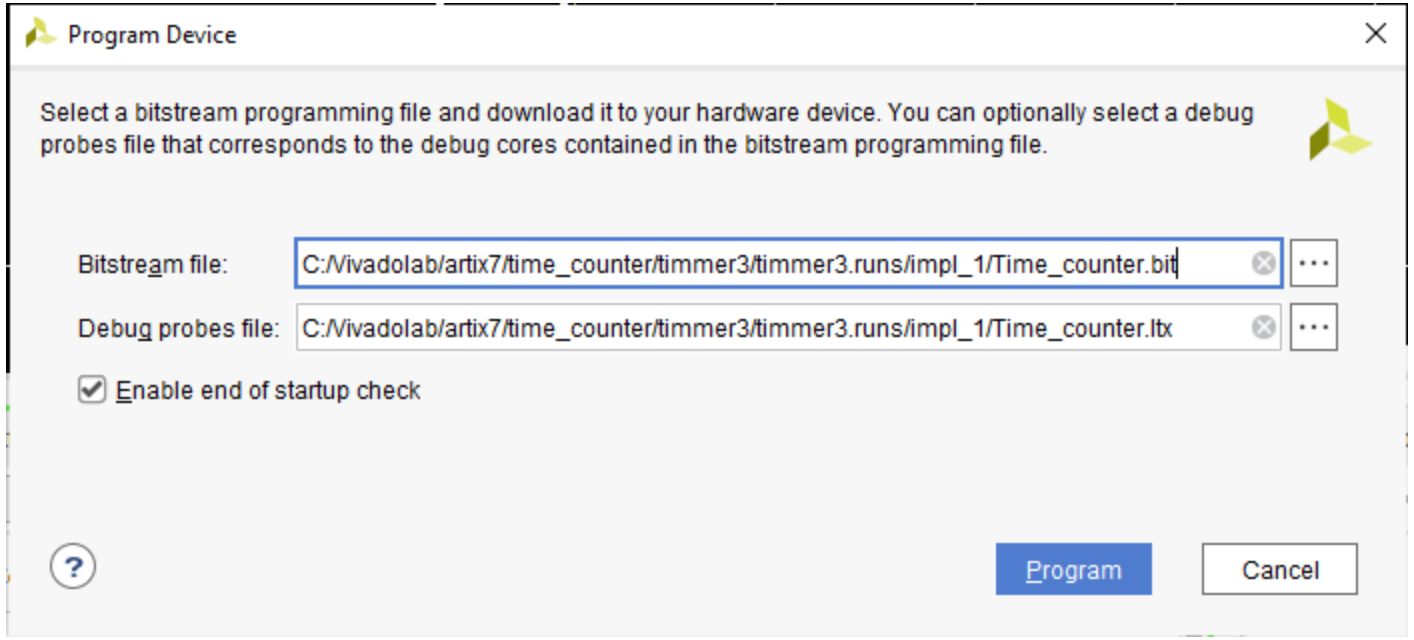
AMD XILINX

Add ILA core in the block design

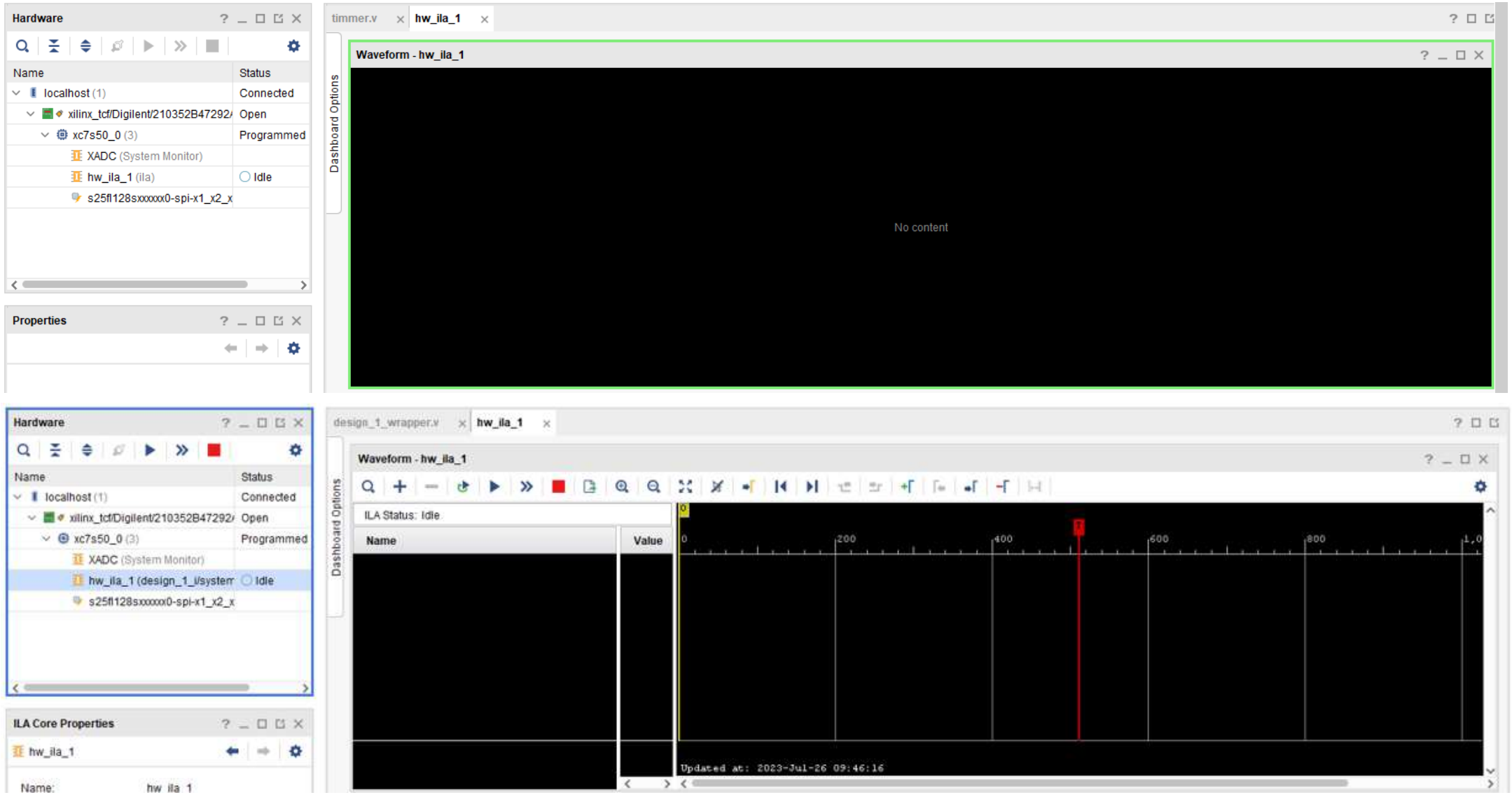


AMD XILINX

ILA debugging

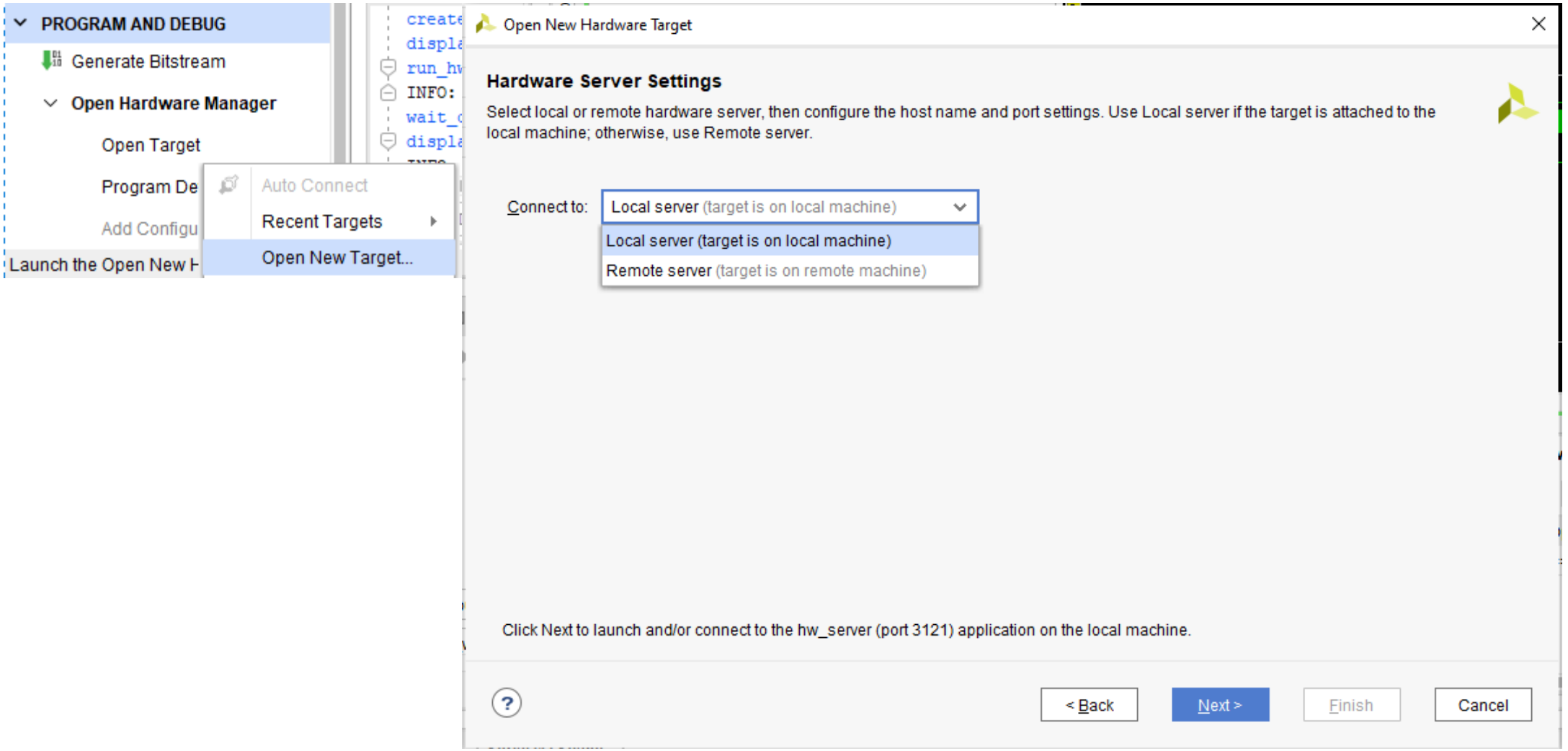


ILA debugging



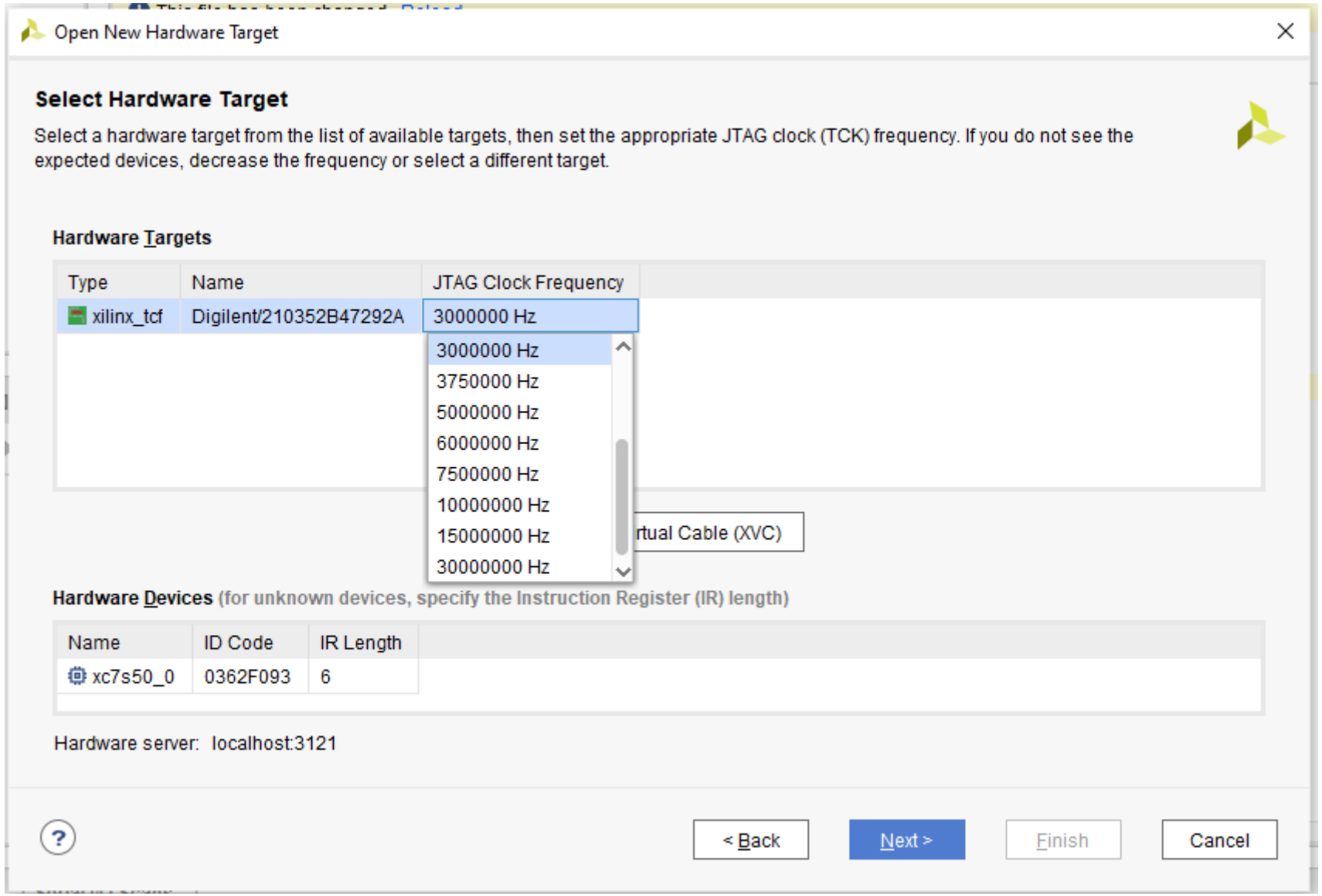
AMD XILINX

ILA debugging



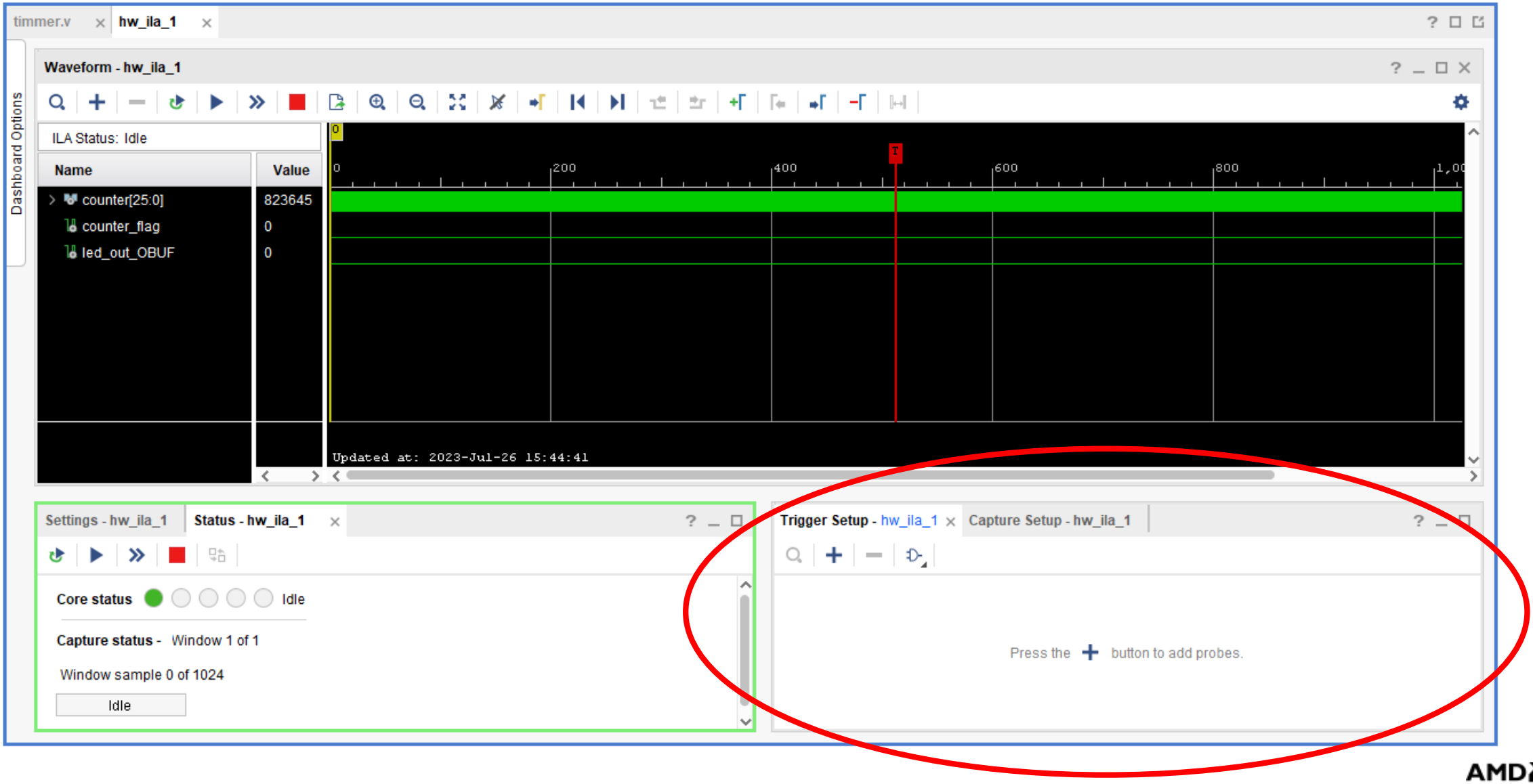
AMD XILINX

ILA debugging



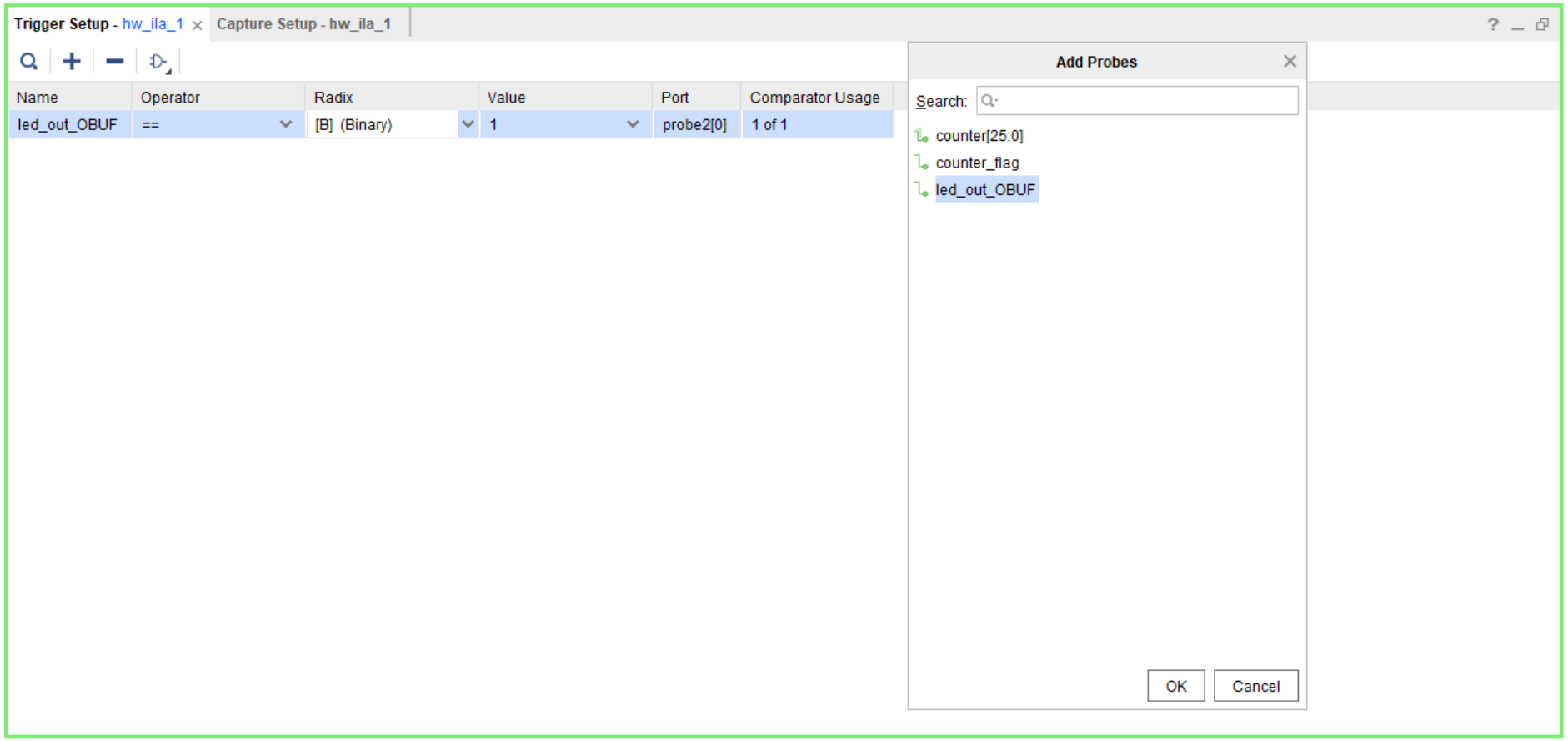
AMD XILINX

ILA debugging



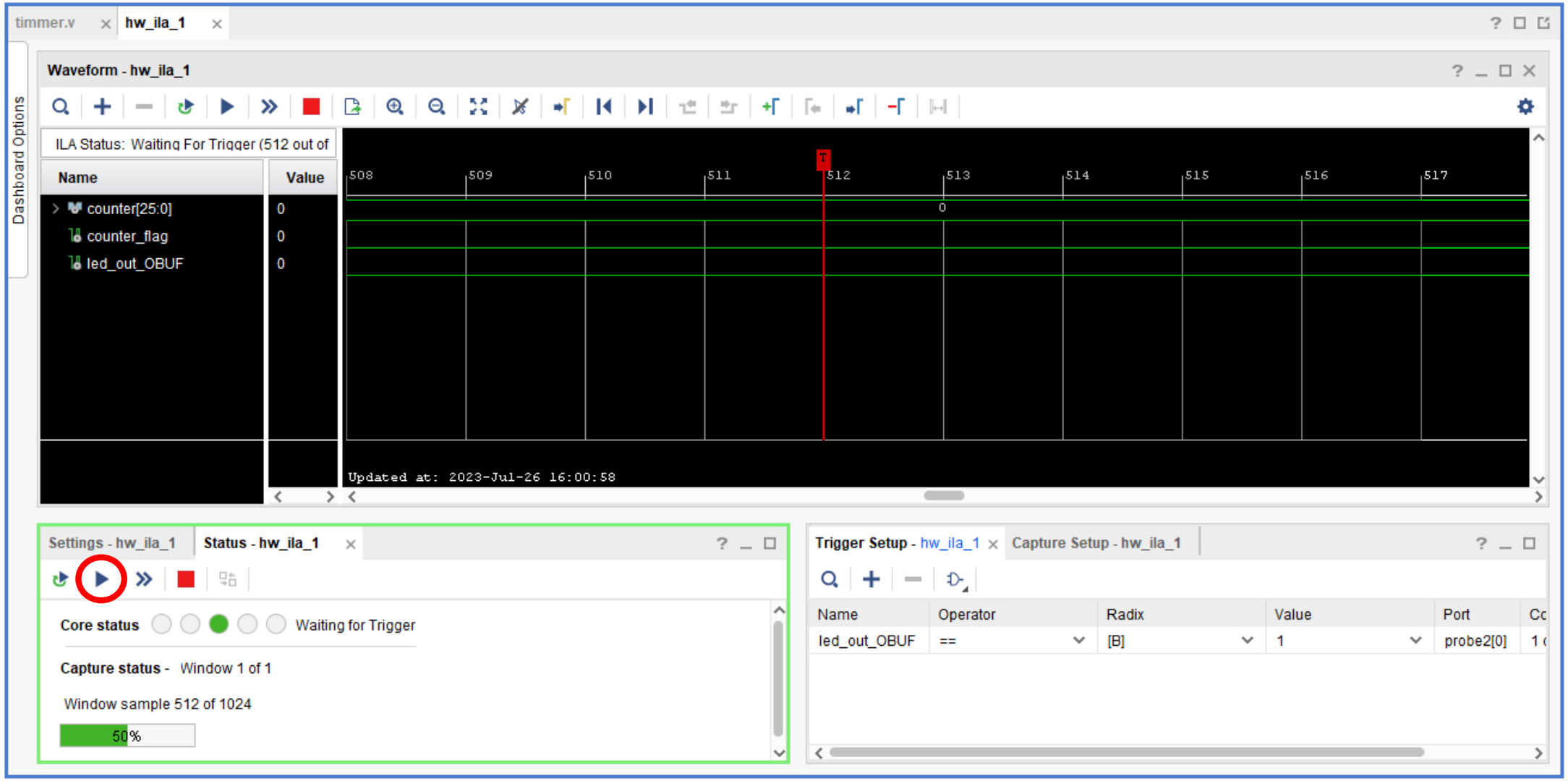
AMD XILINX

ILA debugging



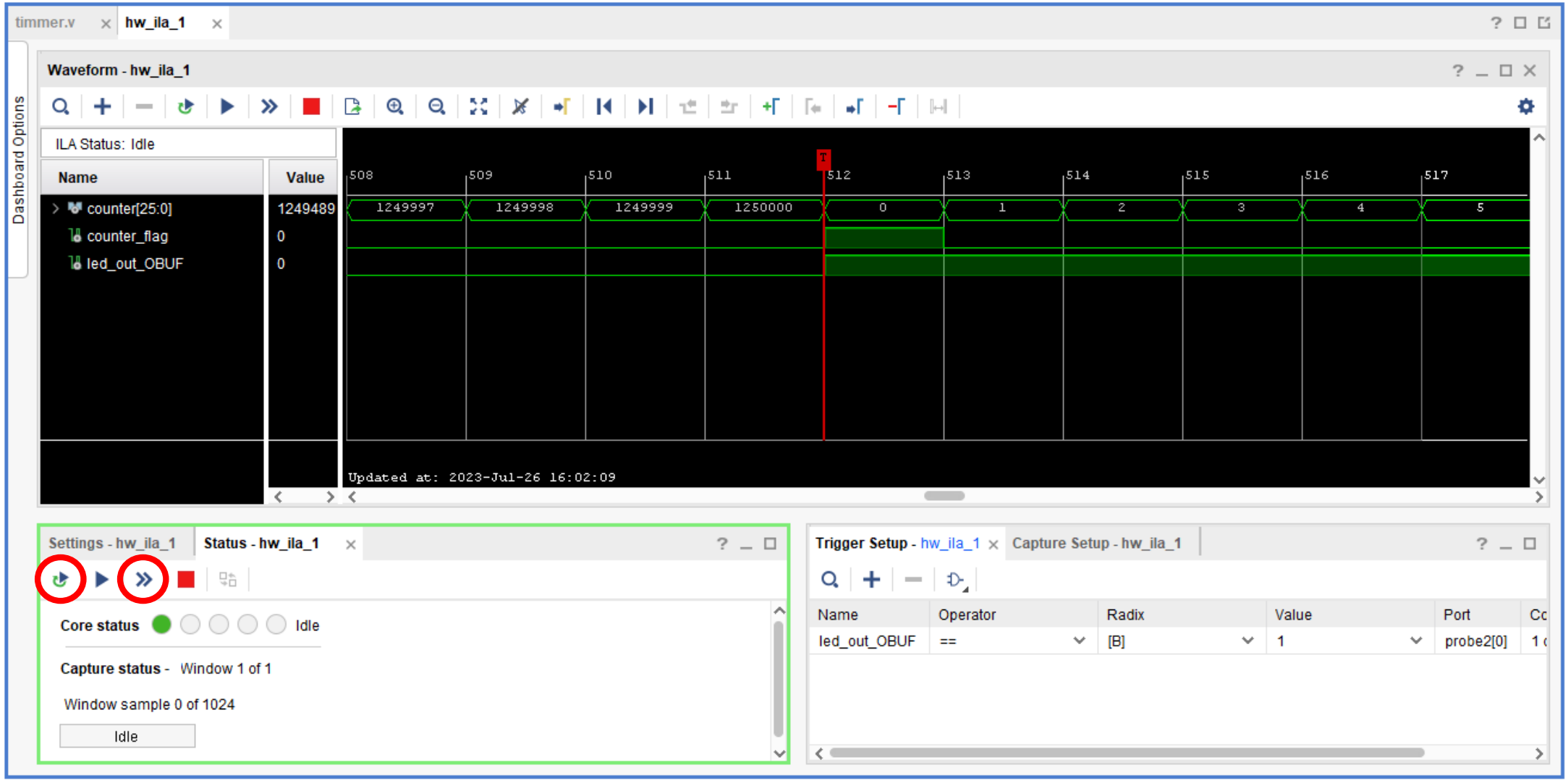
AMD XILINX

ILA debugging



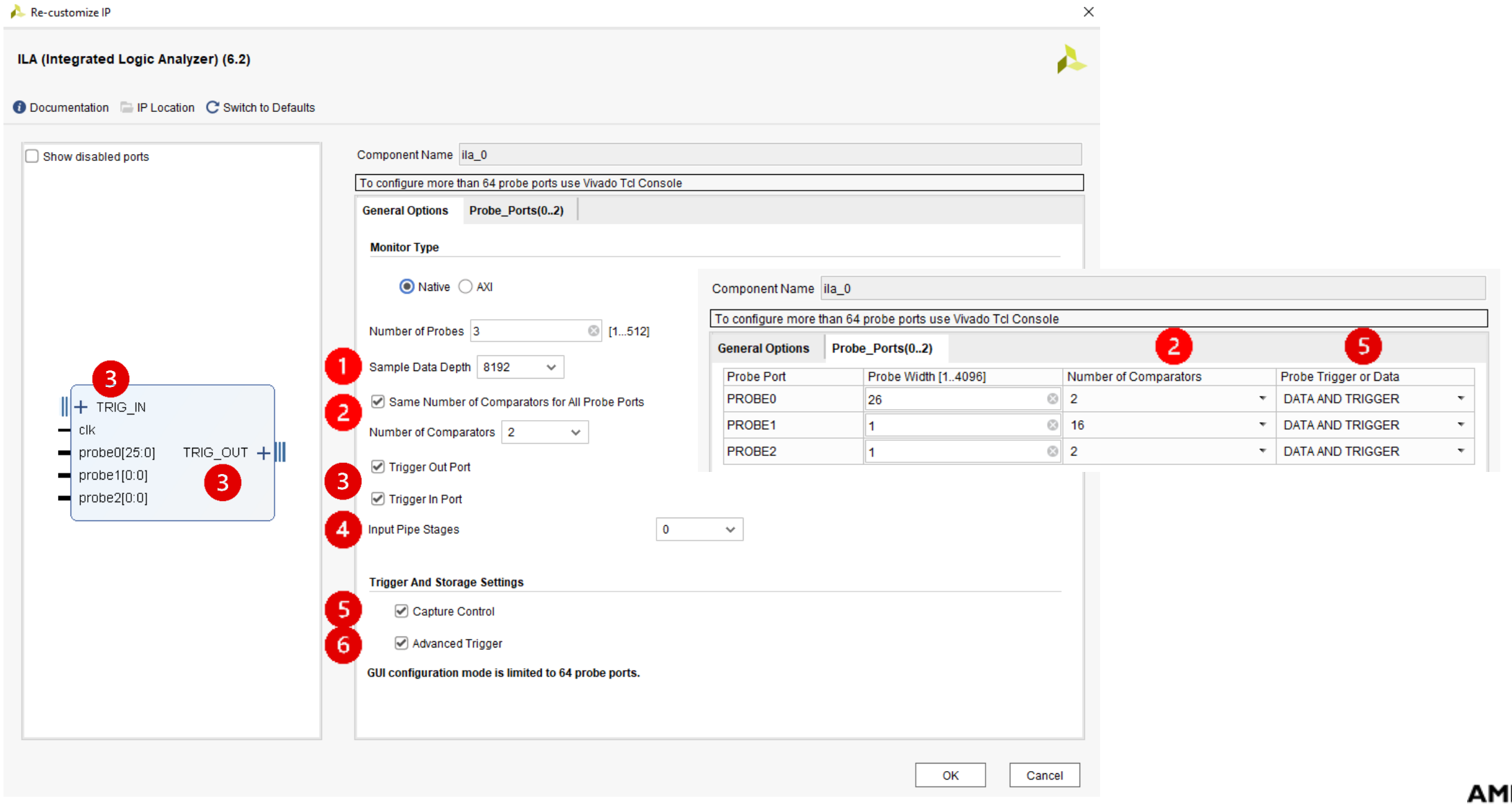
AMD XILINX

ILA debugging



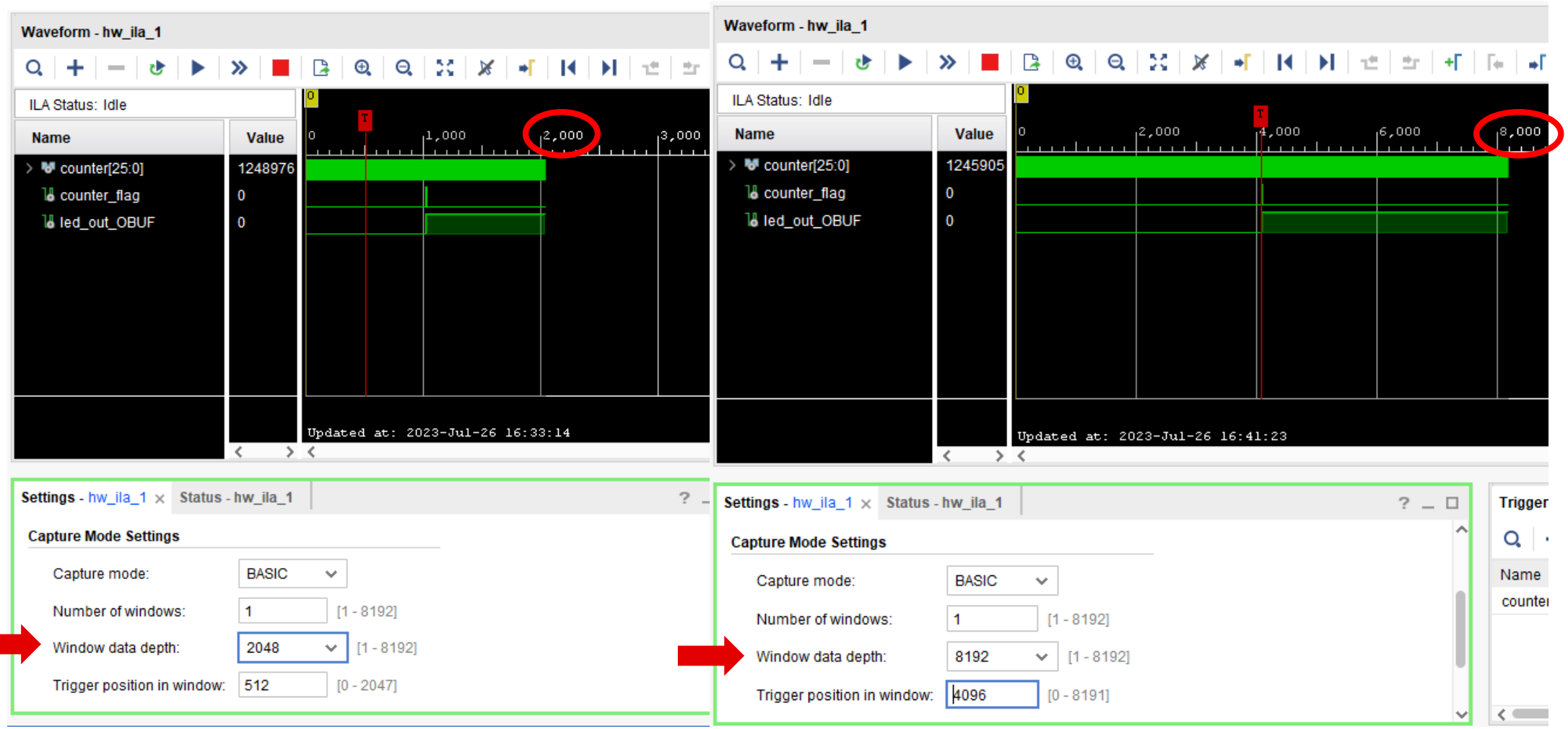
AMD XILINX

ILA IP Setting

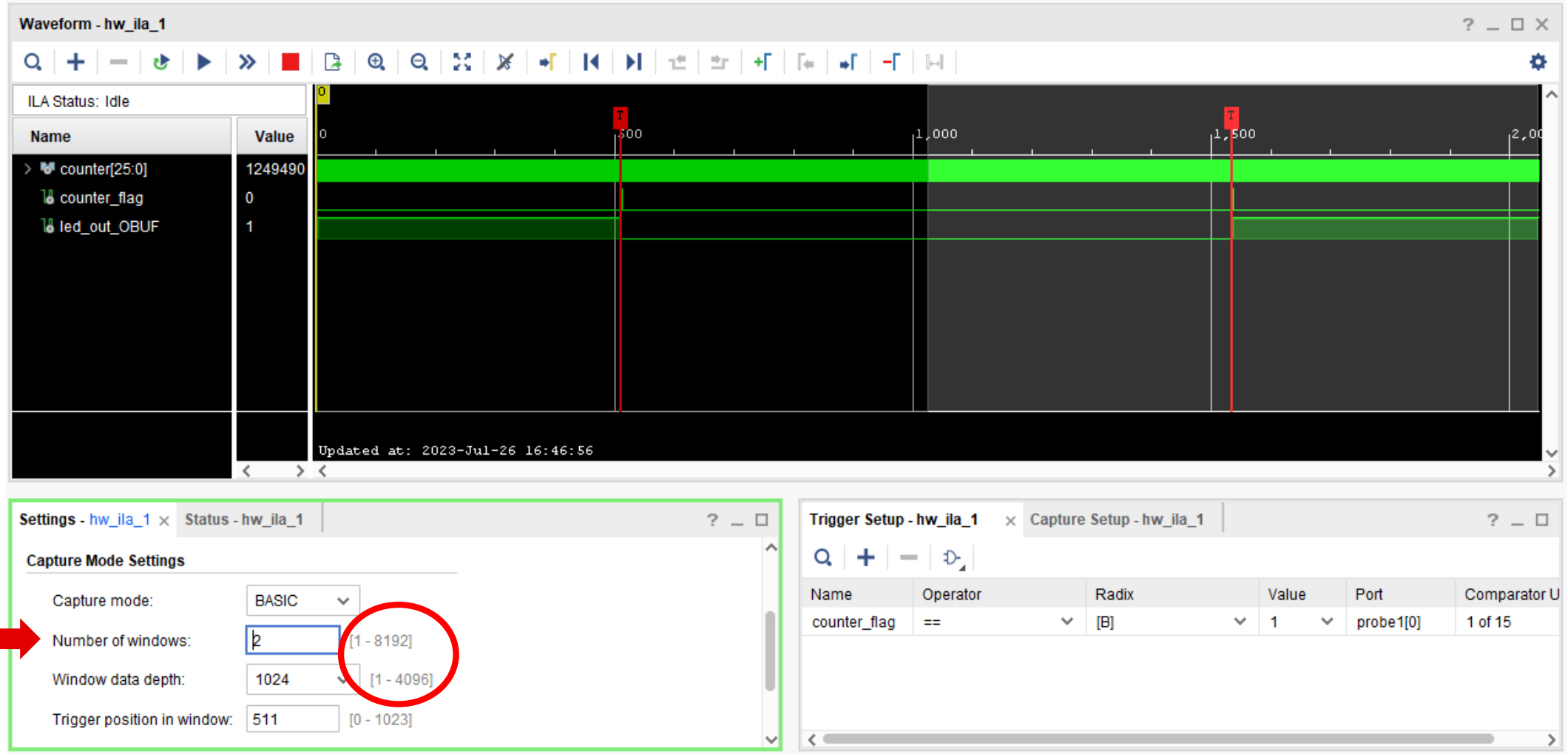


AMD XILINX

ILA IP Setting

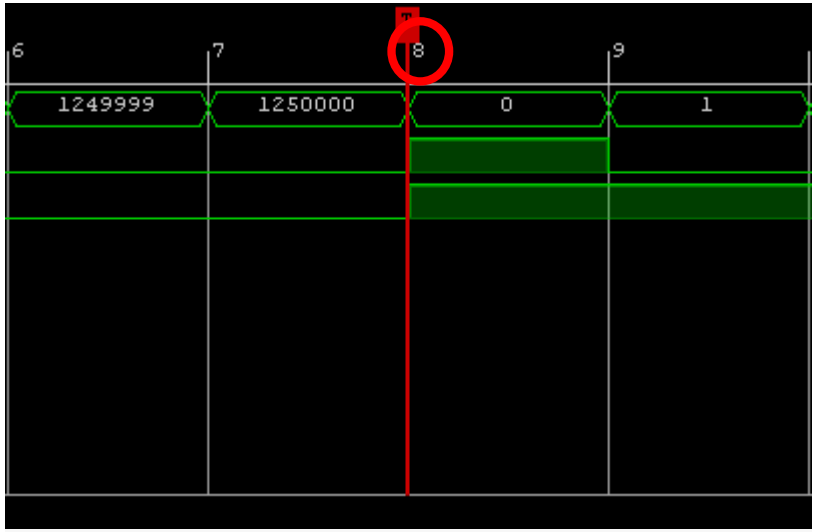


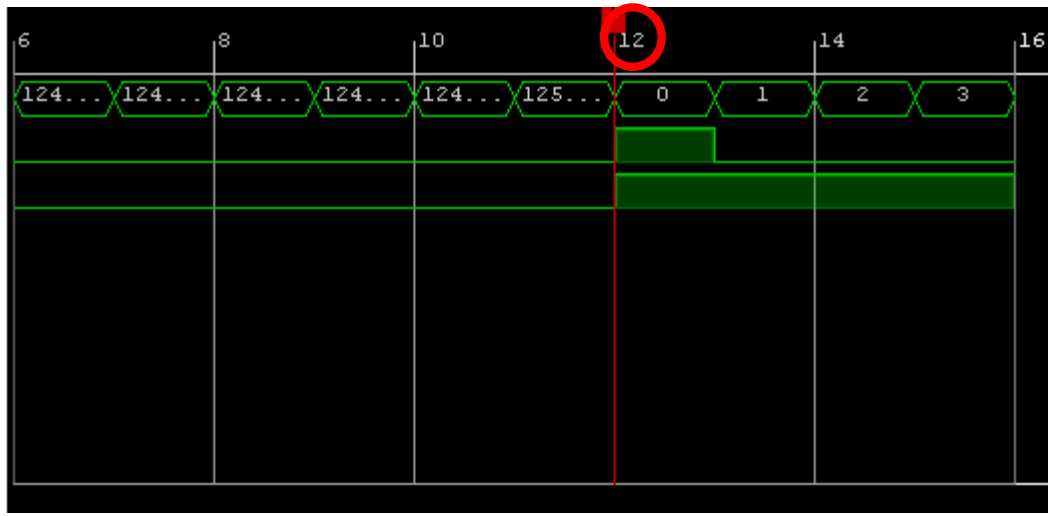
ILA IP Setting

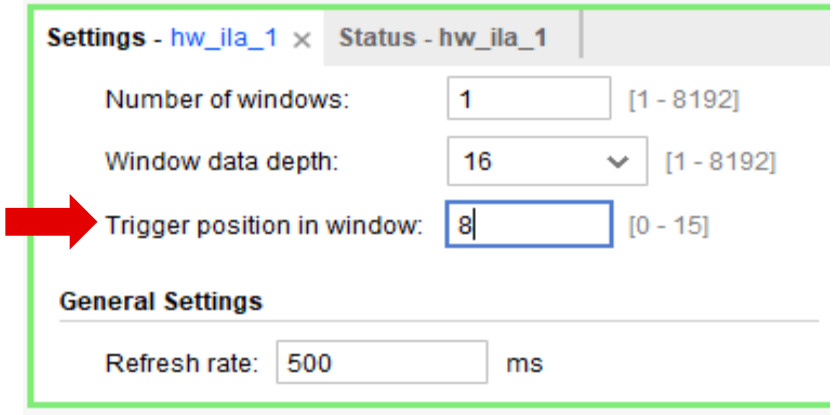


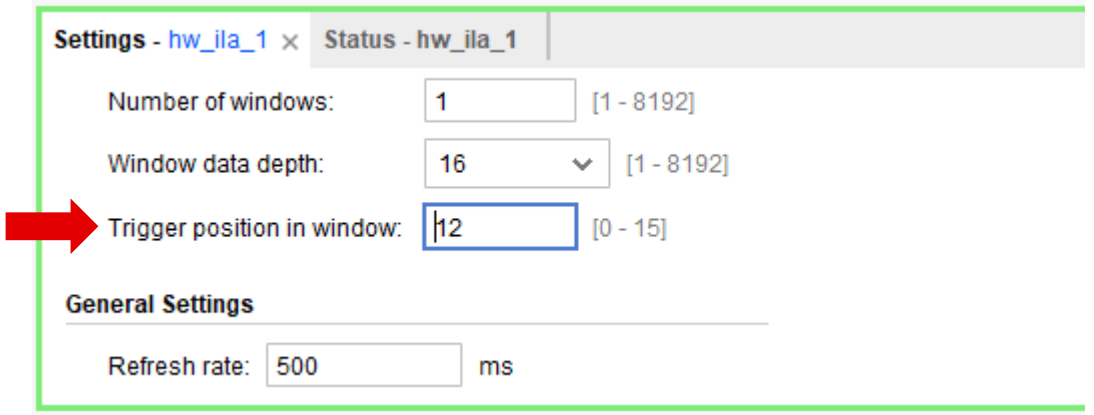
AMD XILINX

ILA IP Setting



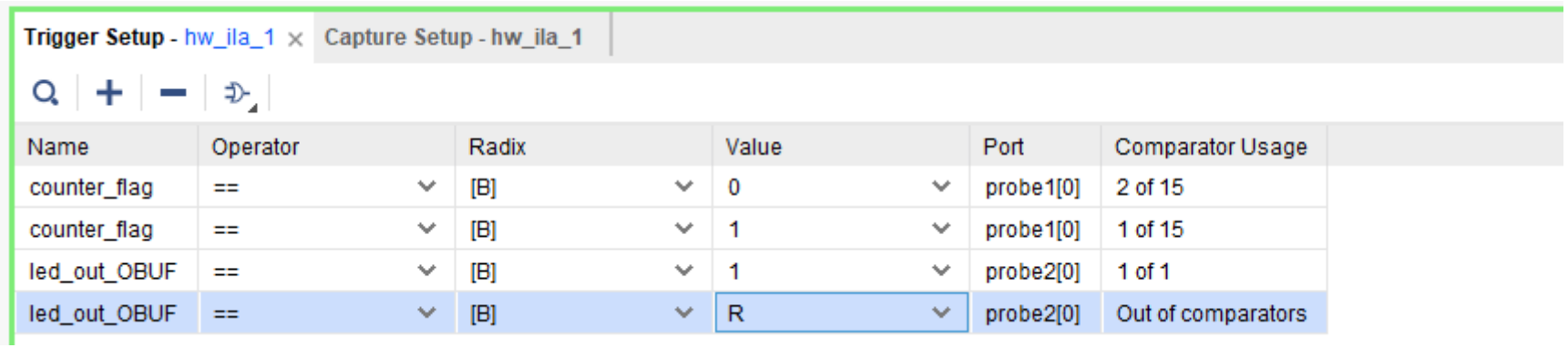


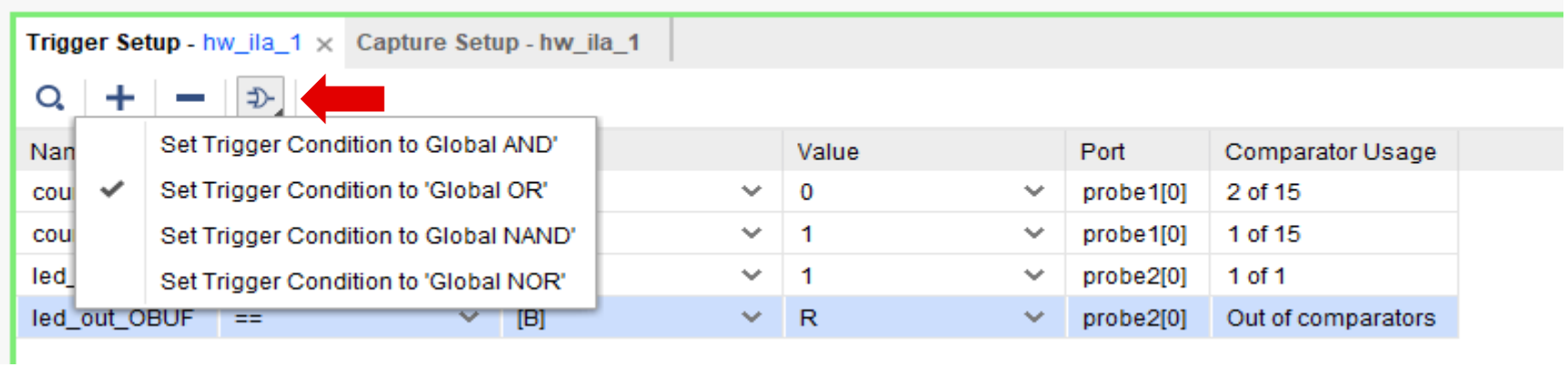




AMD XILINX

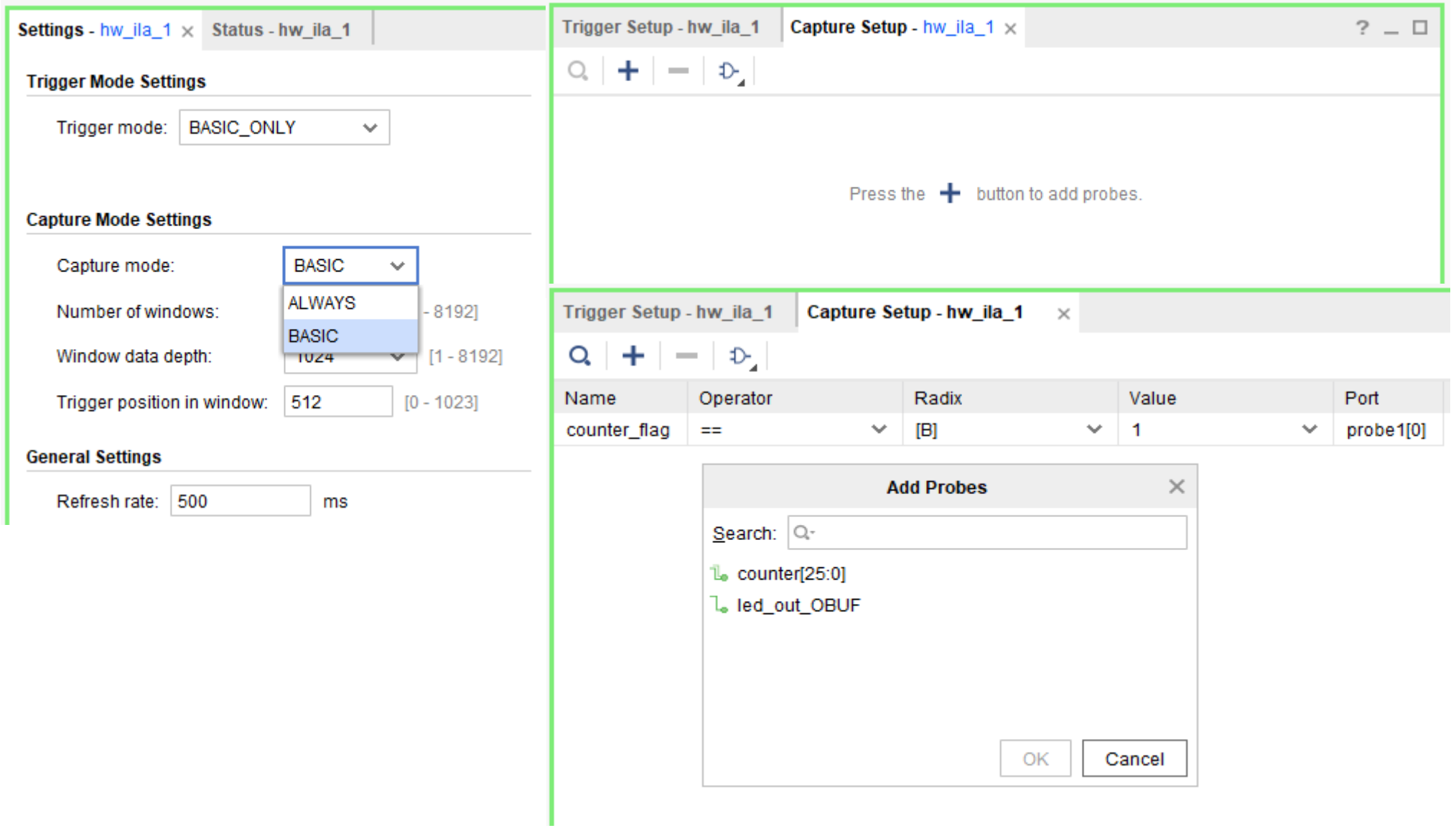
ILA IP Setting





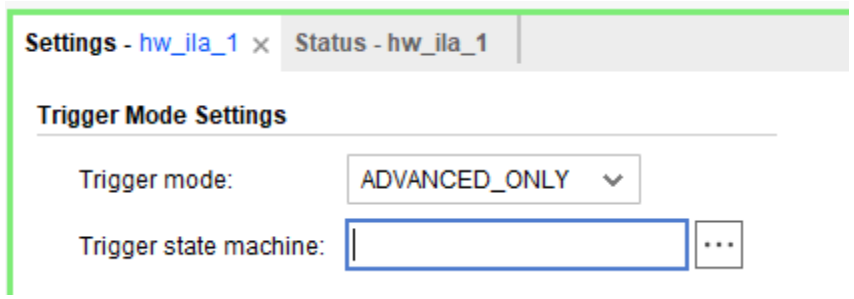
AMD XILINX

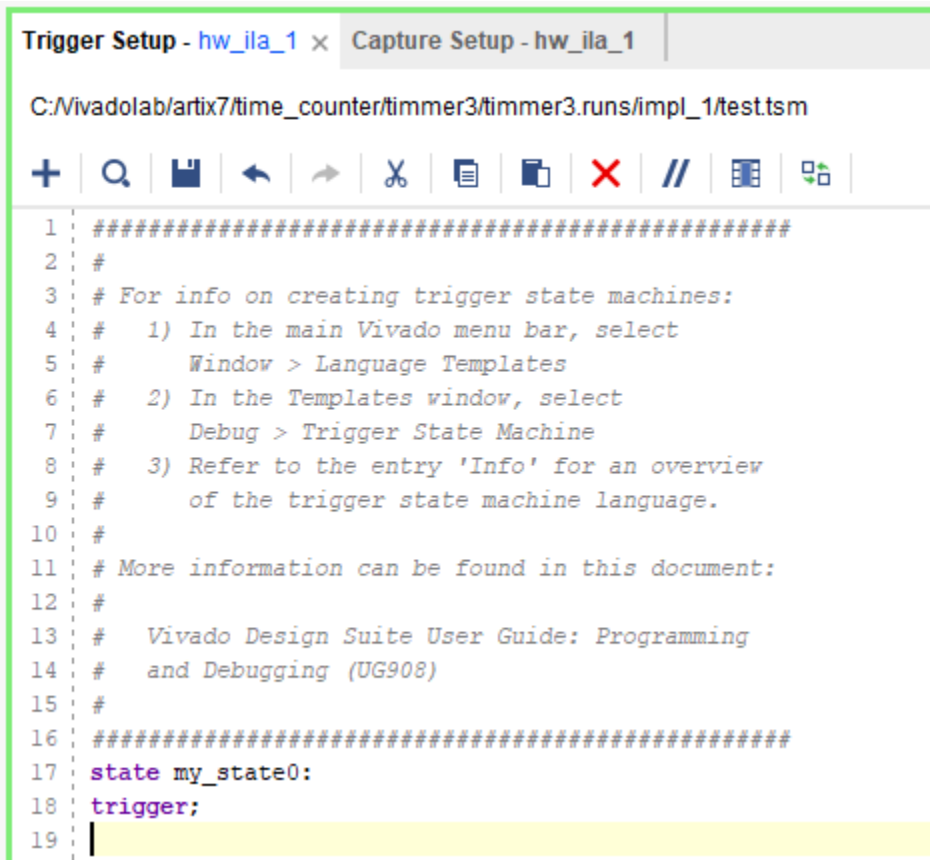
ILA IP Setting



AMD XILINX

ILA IP Setting





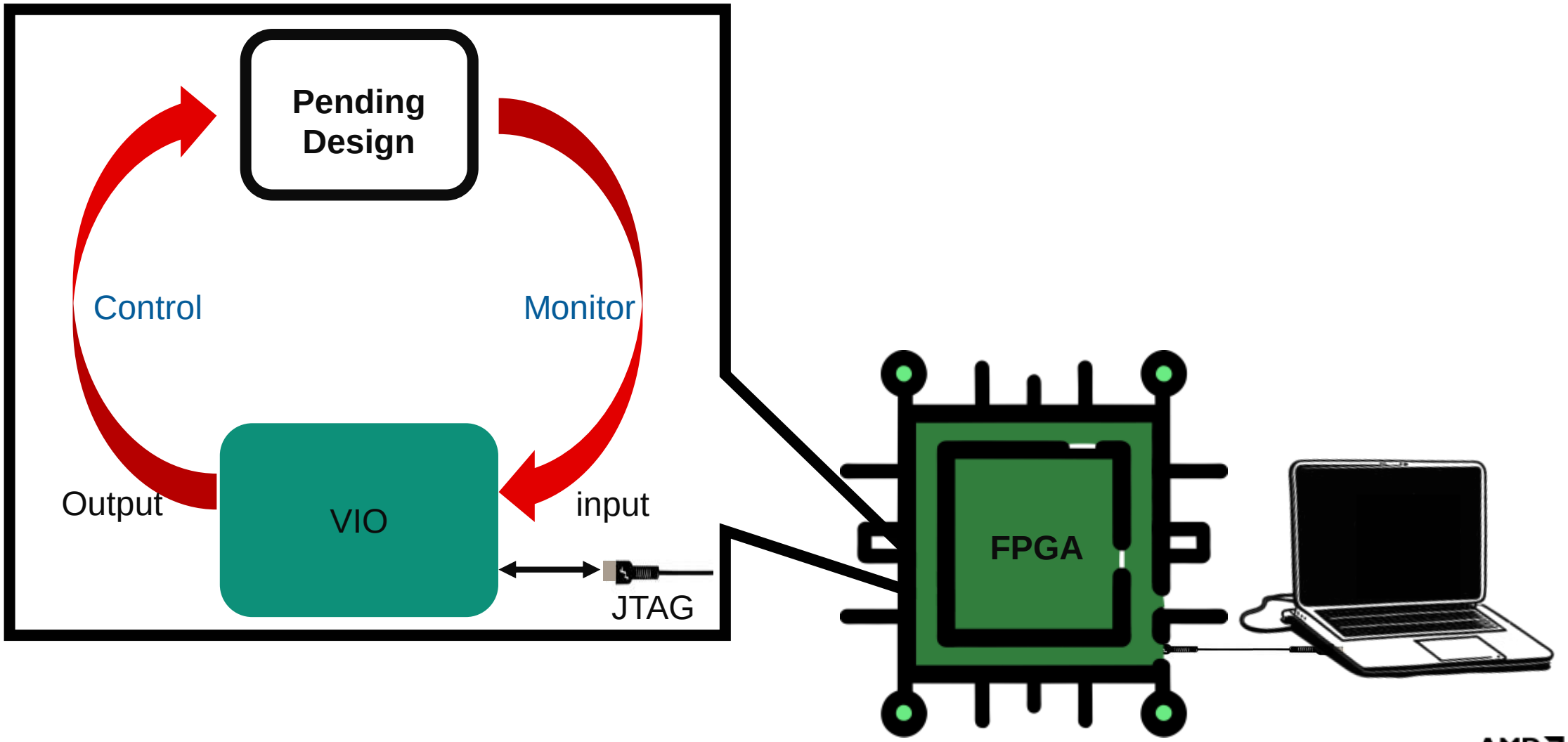
AMD XILINX

AMD
XILINX

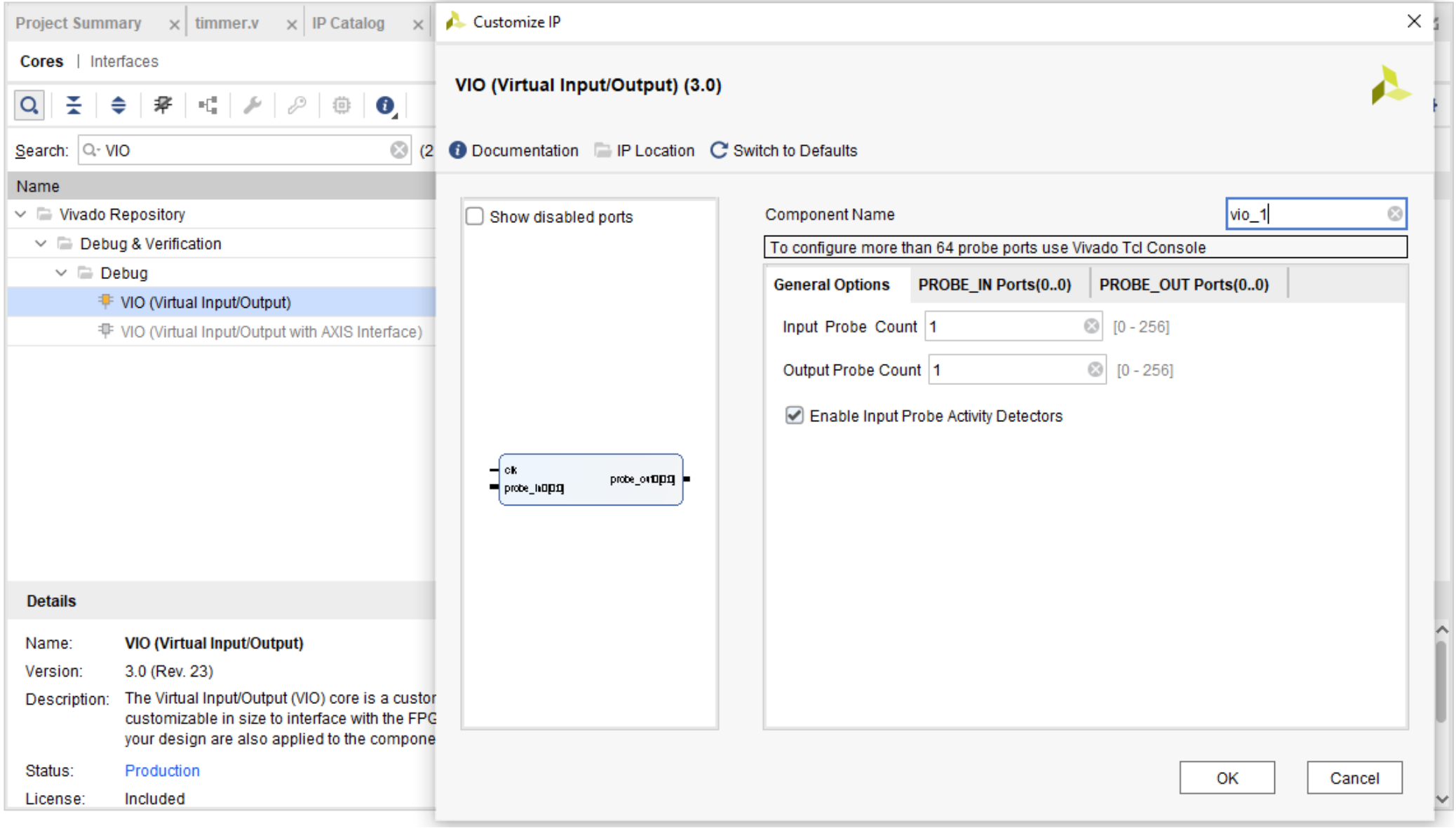
Virtual Input/Output

Course Agenda
2023

Virtual Input/Output

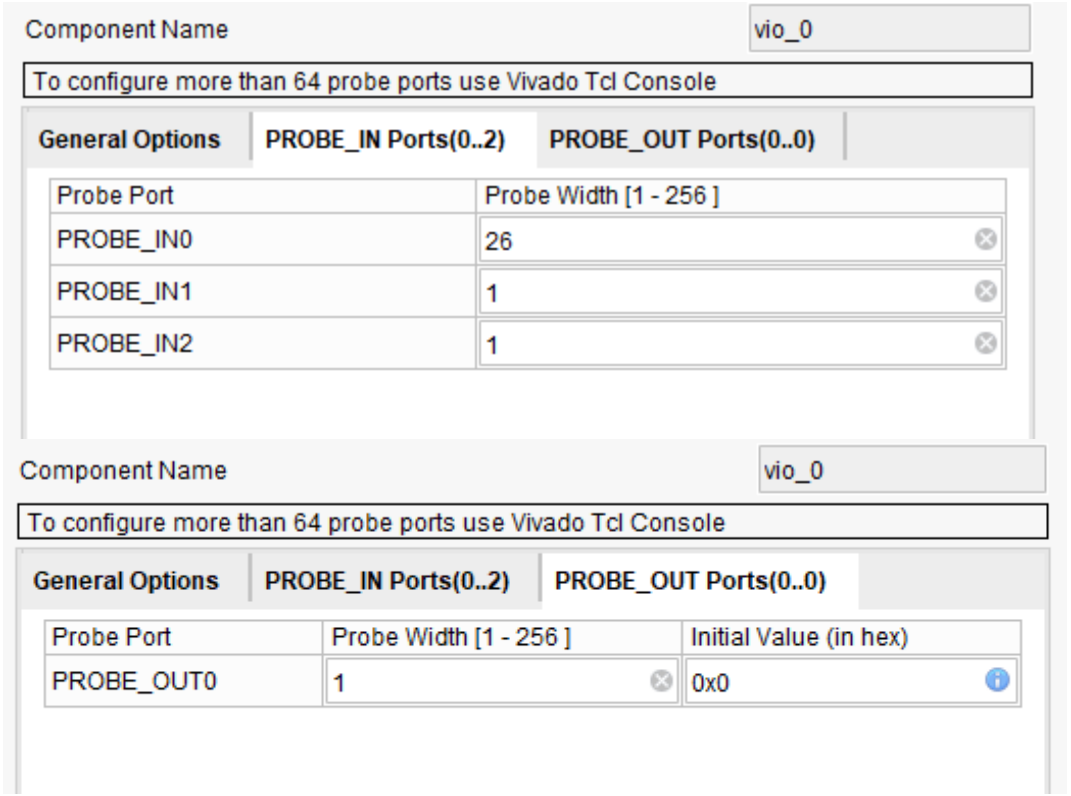


Add VIO IP Core



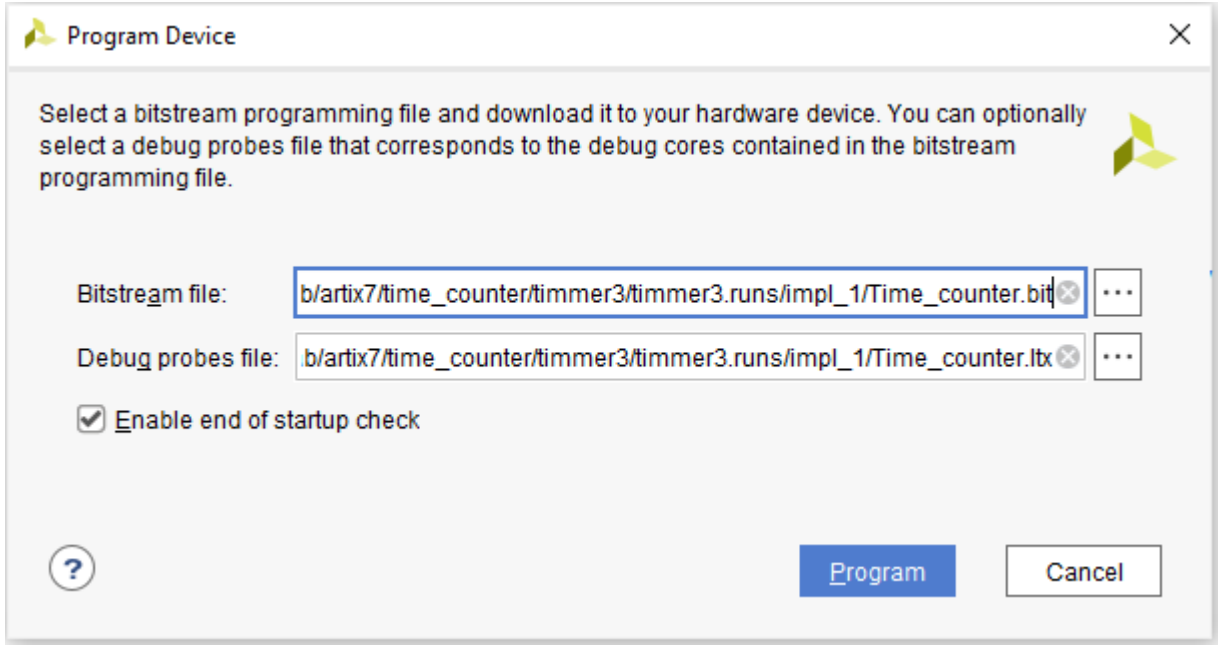
AMD XILINX

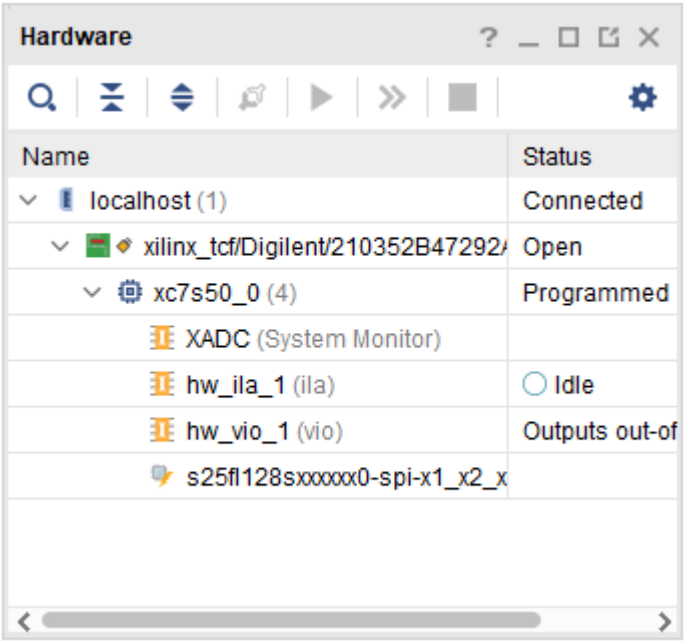
Add VIO IP Core




```
vio_0 vio(
    .clk(sys_clk),
    .probe_out0(vbtn),
    .probe_in0(counter),
    .probe_in1(counter_flag),
    .probe_in2(led_out)
);
```

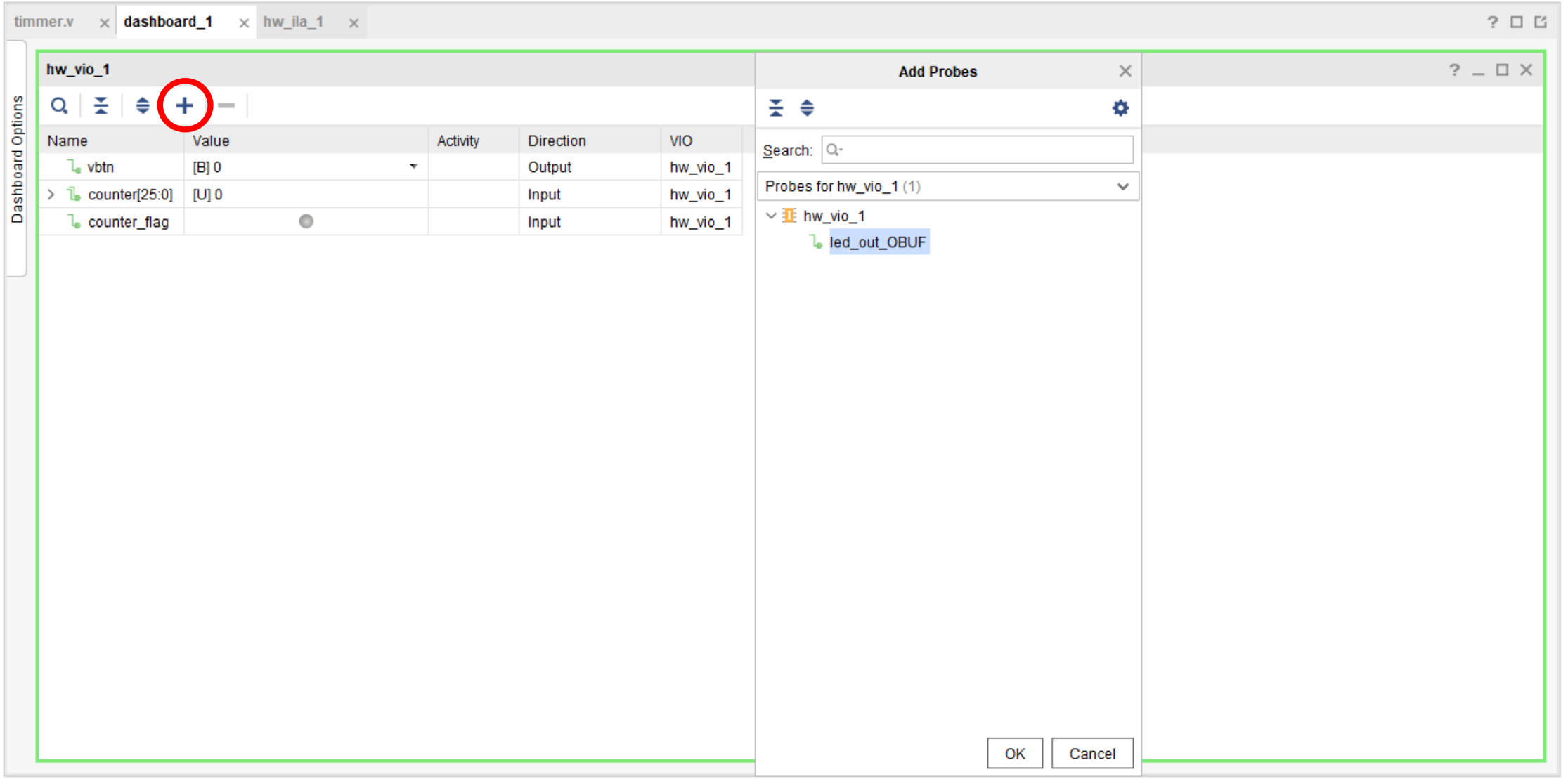
VIO Debugging





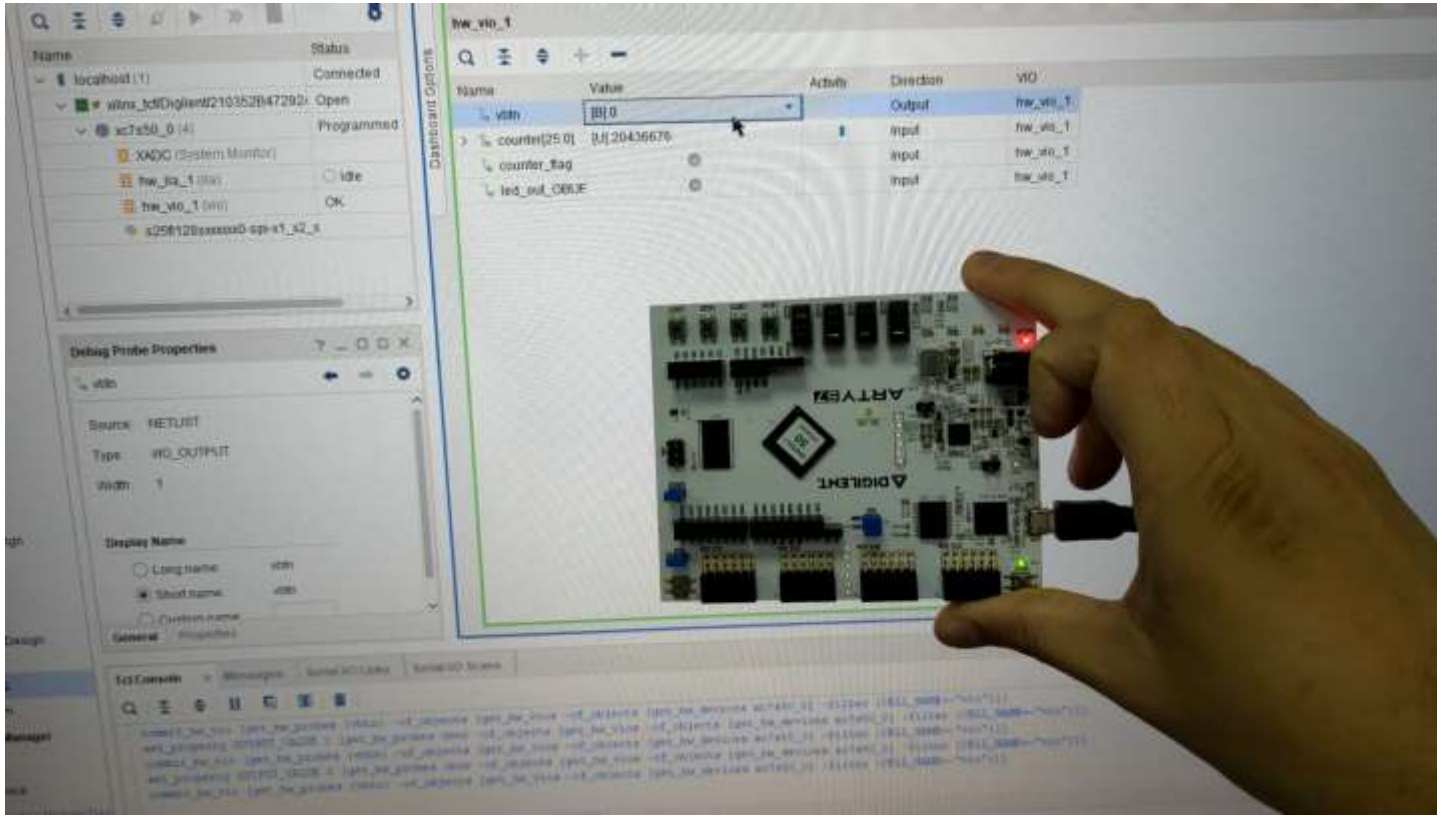
AMD XILINX

VIO Debugging



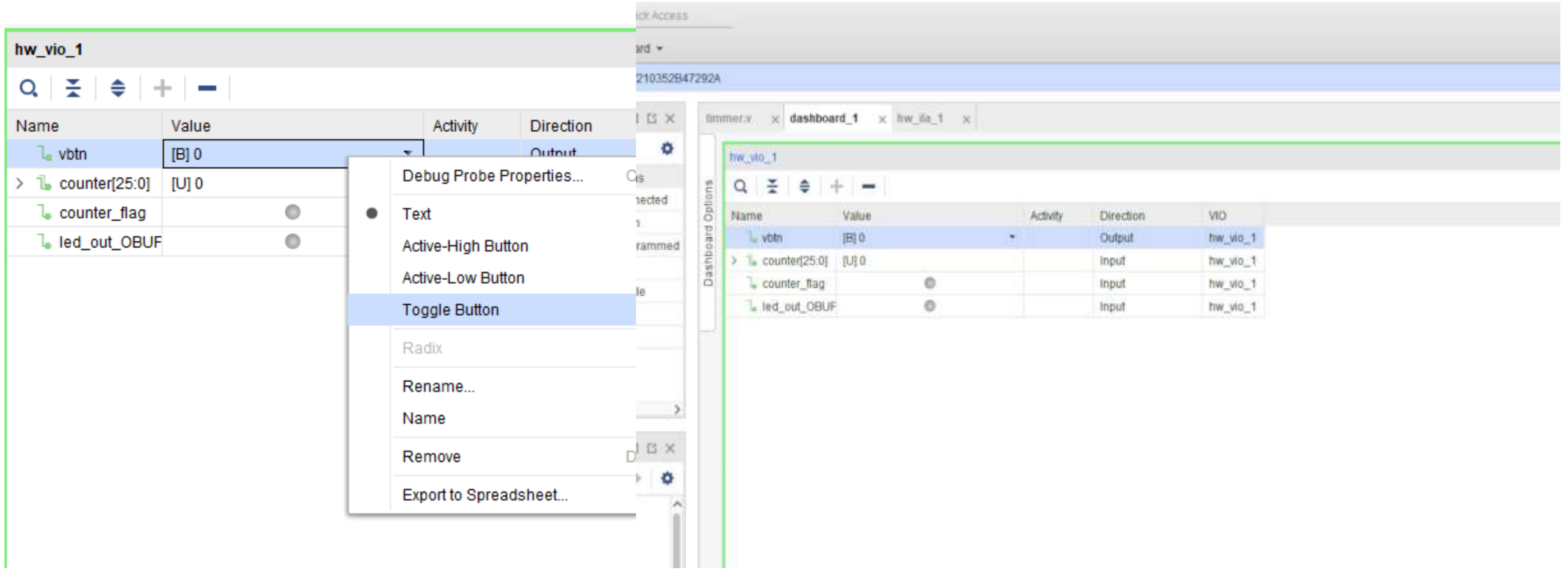
AMD
XILINX

VIO Debugging



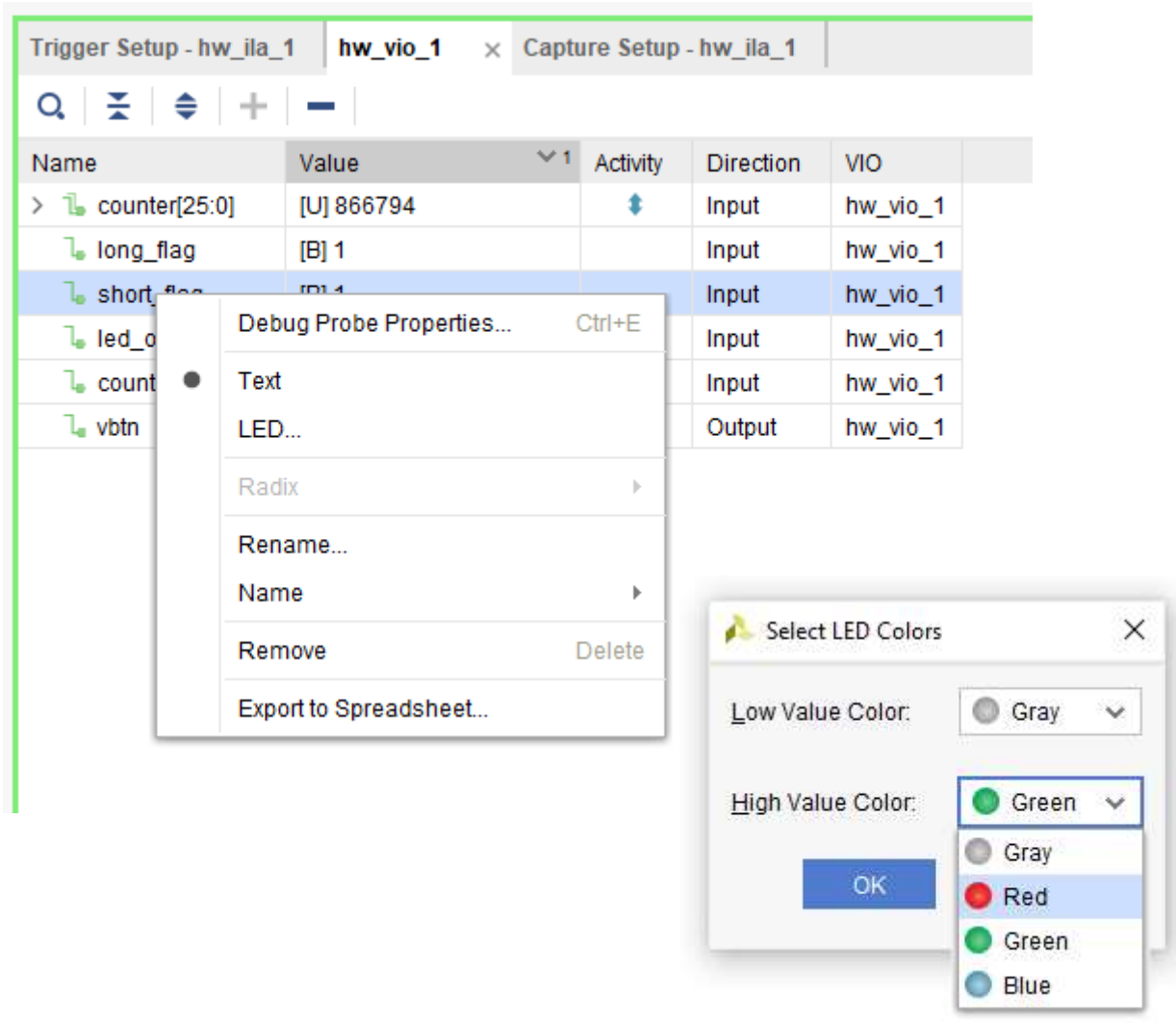
AMD XILINX

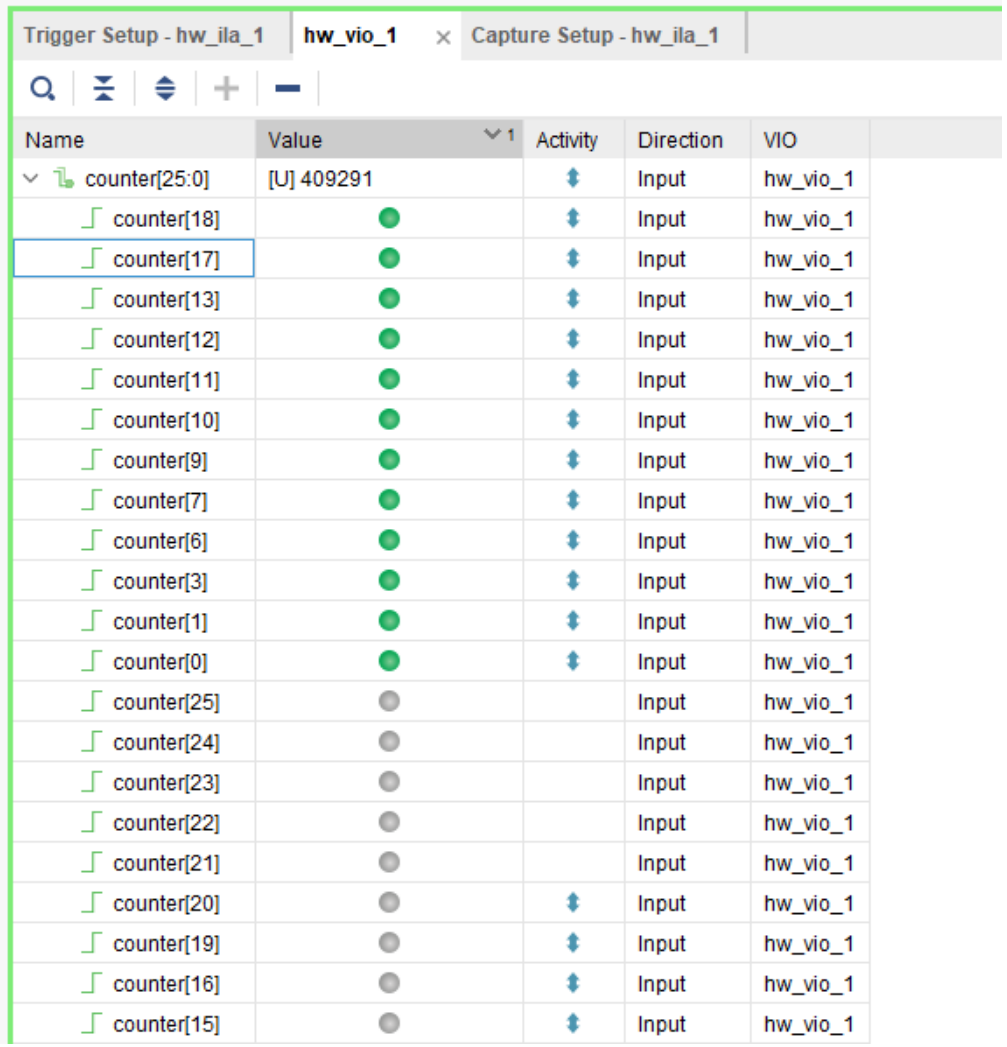
VIO Debugging



AMD XILINX

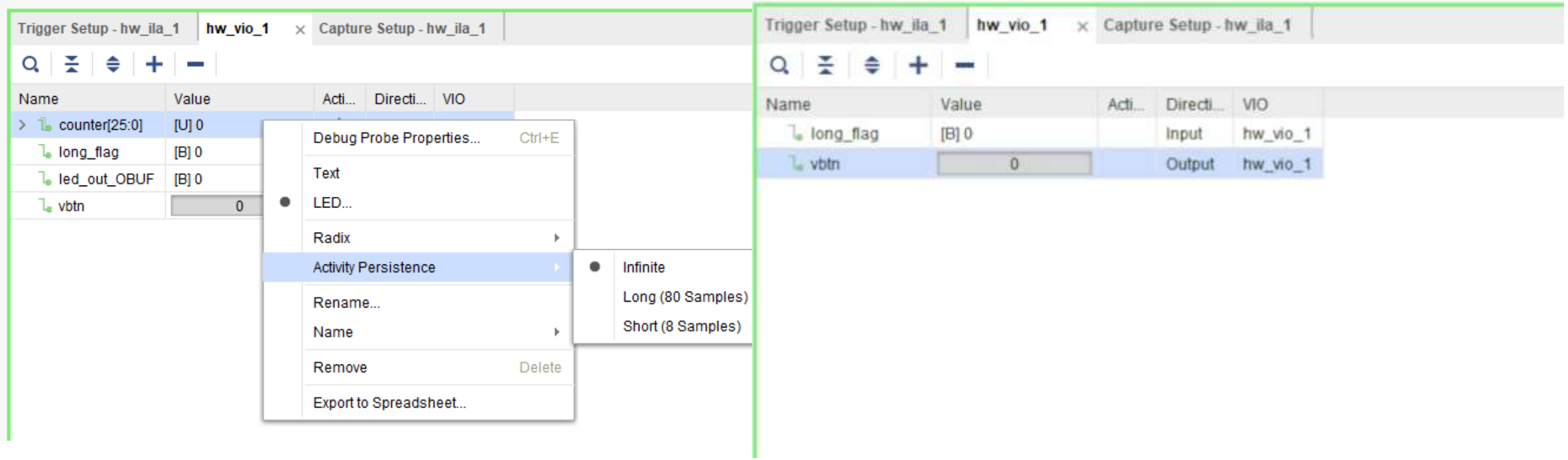
VIO Debugging





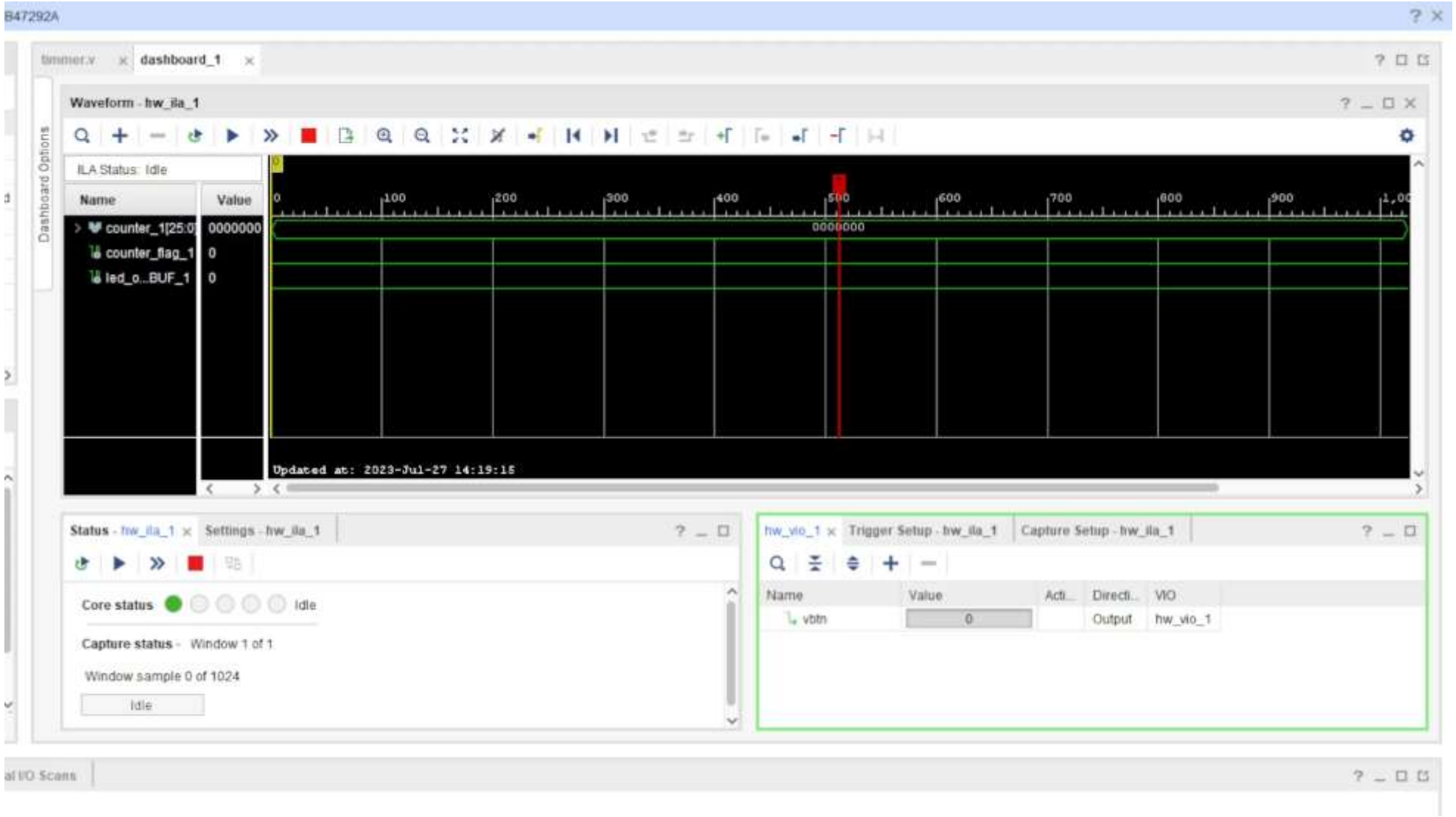
AMD XILINX

VIO Debugging



AMD XILINX

VIO Debugging



AMD XILINX

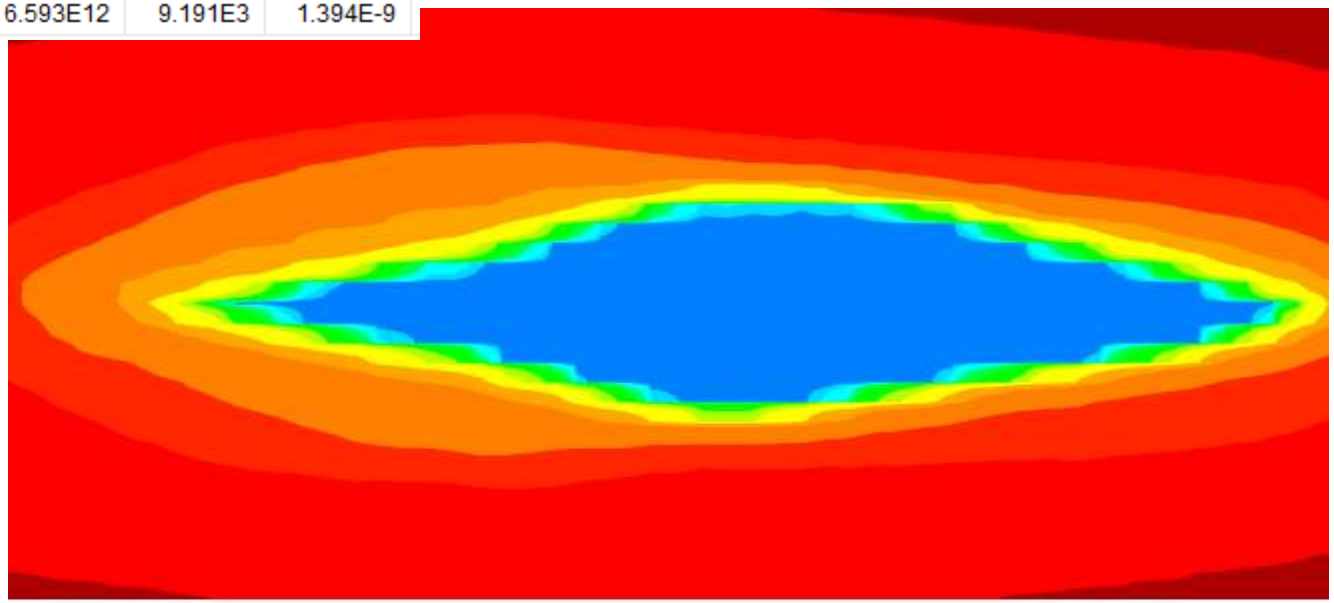
AMD
XILINX

Integrated Bit Error Ratio Tester

Course Agenda
2023

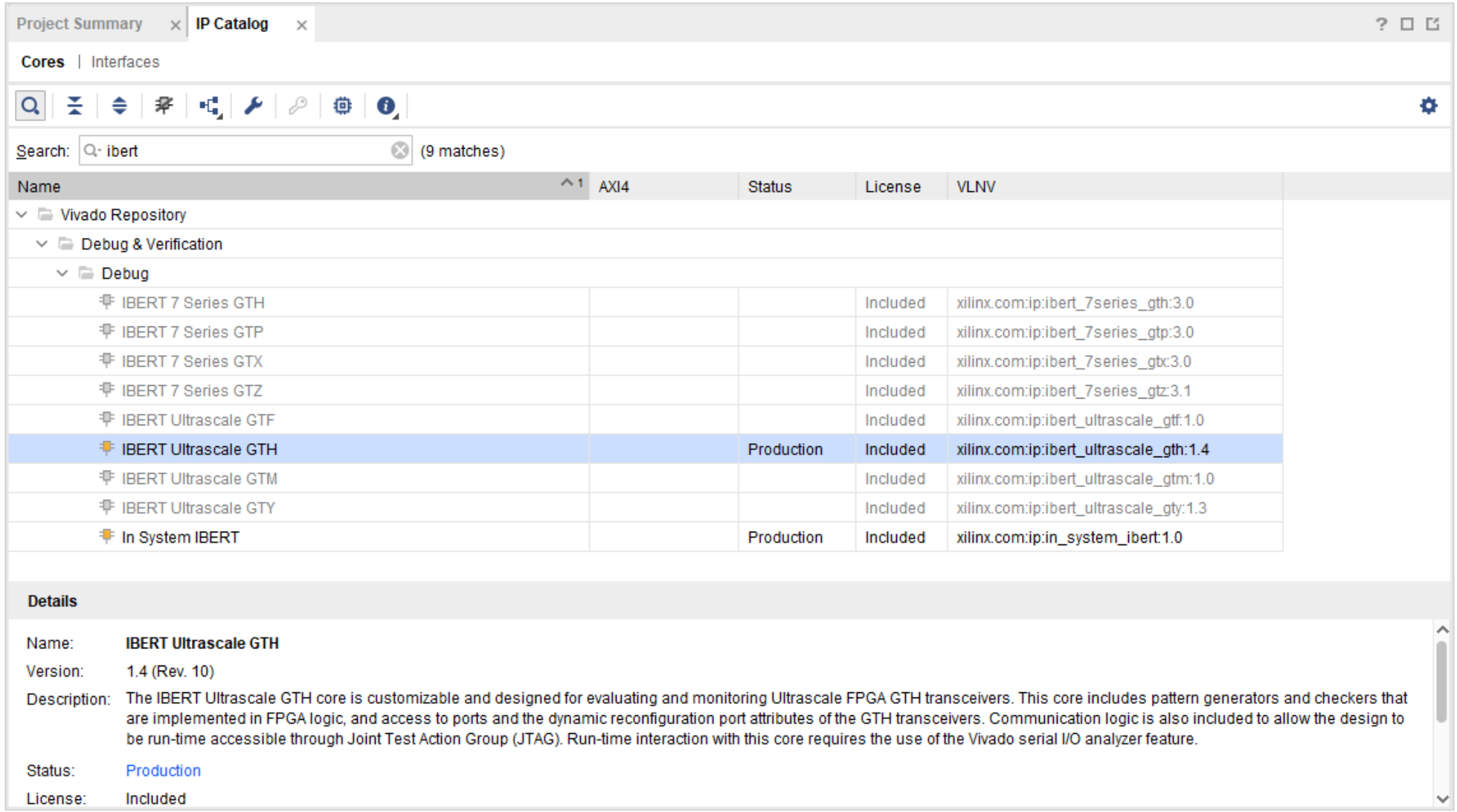
IBERT

Name	TX	RX	Status	Bits	Errors	BER
Link 12	MGT_X0Y12/TX	MGT_X0Y12/RX	15.625 Gbps	6.592E12	1.78E2	2.7E-11
Link 13	MGT_X0Y13/TX	MGT_X0Y13/RX	15.599 Gbps	6.592E12	2.595E4	3.936E-9
Link 14	MGT_X0Y14/TX	MGT_X0Y14/RX	15.625 Gbps	6.592E12	3.717E3	5.638E-10
Link 15	MGT_X0Y15/TX	MGT_X0Y15/RX	15.625 Gbps	6.592E12	3E4	4.551E-9
Link 16	MGT_X0Y16/TX	MGT_X0Y16/RX	15.646 Gbps	6.592E12	1.595E6	2.42E-7
Link 17	MGT_X0Y17/TX	MGT_X0Y17/RX	15.633 Gbps	3.681E12	3.007E11	8.168E-2
Link 18	MGT_X0Y18/TX	MGT_X0Y18/RX	15.625 Gbps	6.593E12	6.4E1	9.708E-12
Link 19	MGT_X0Y19/TX	MGT_X0Y19/RX	15.643 Gbps	6.593E12	9.191E3	1.394E-9



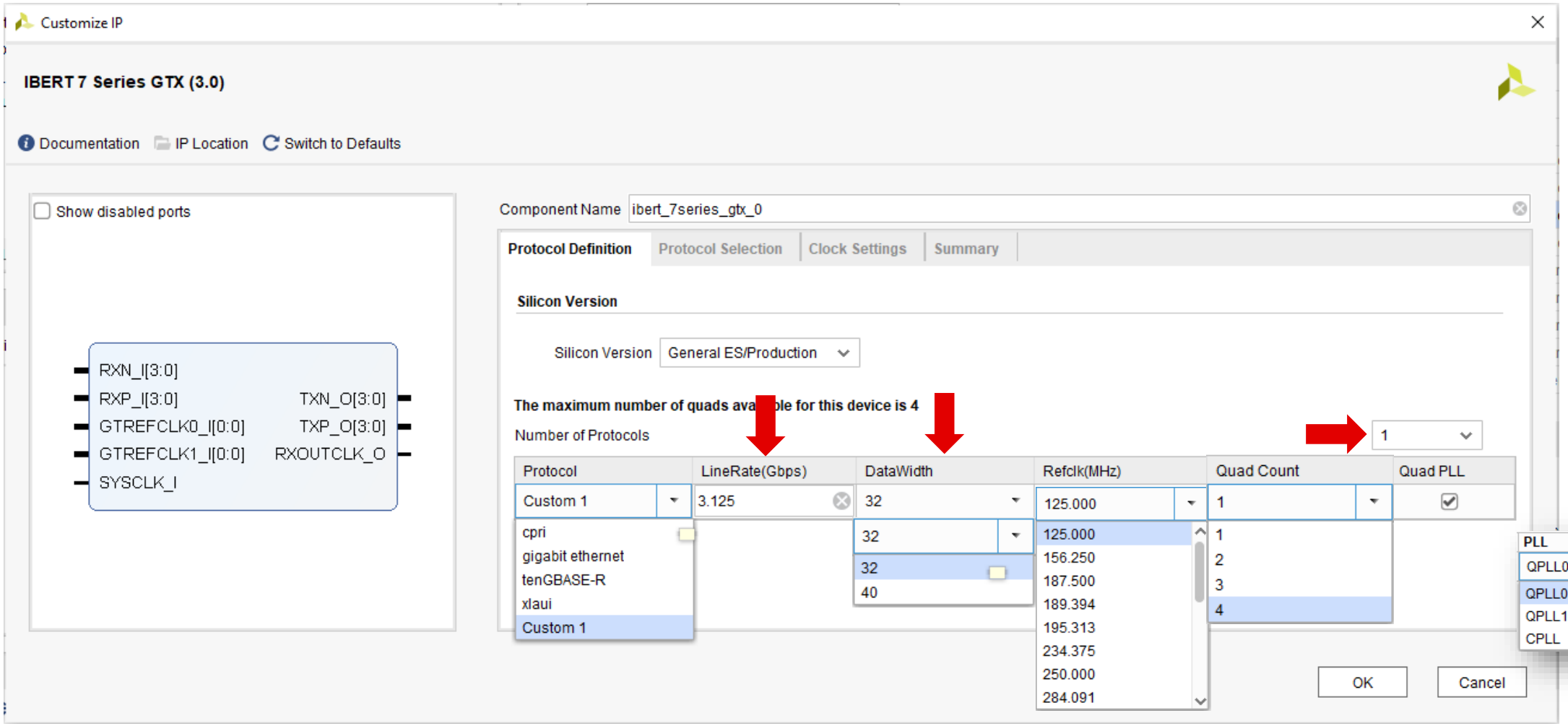
AMD
XILINX

IBERT IP Setting

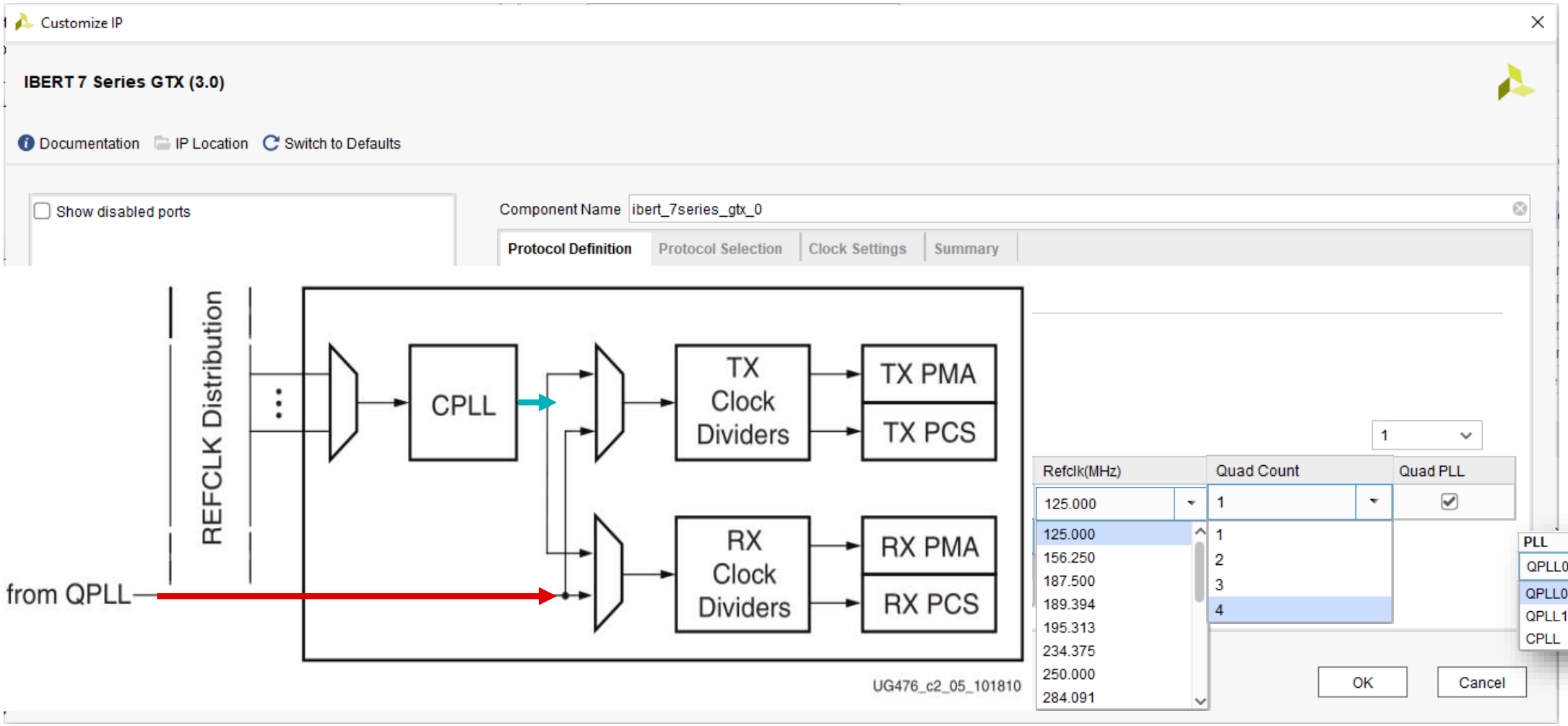


AMD XILINX

IBERT IP Setting

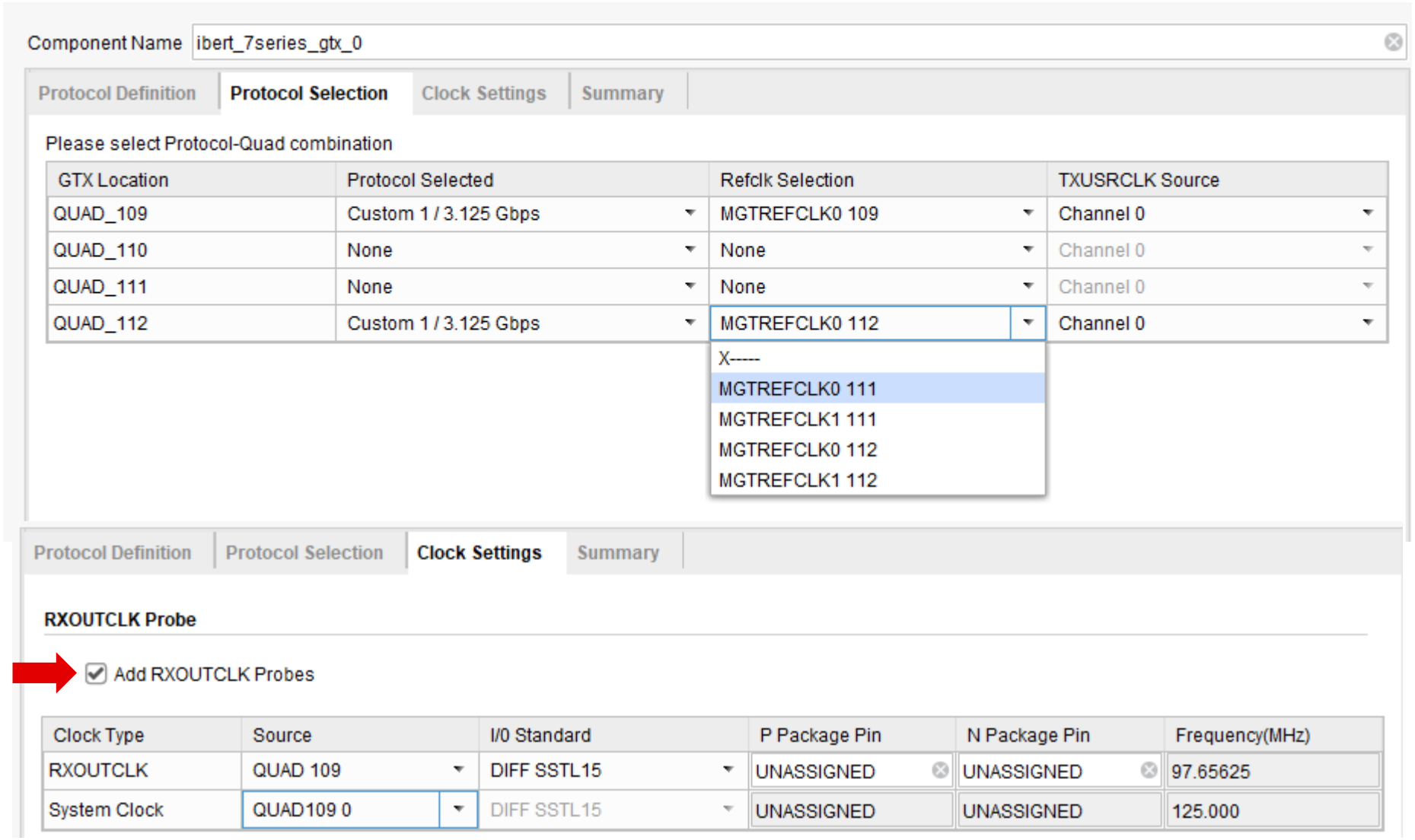


IBERT IP Setting



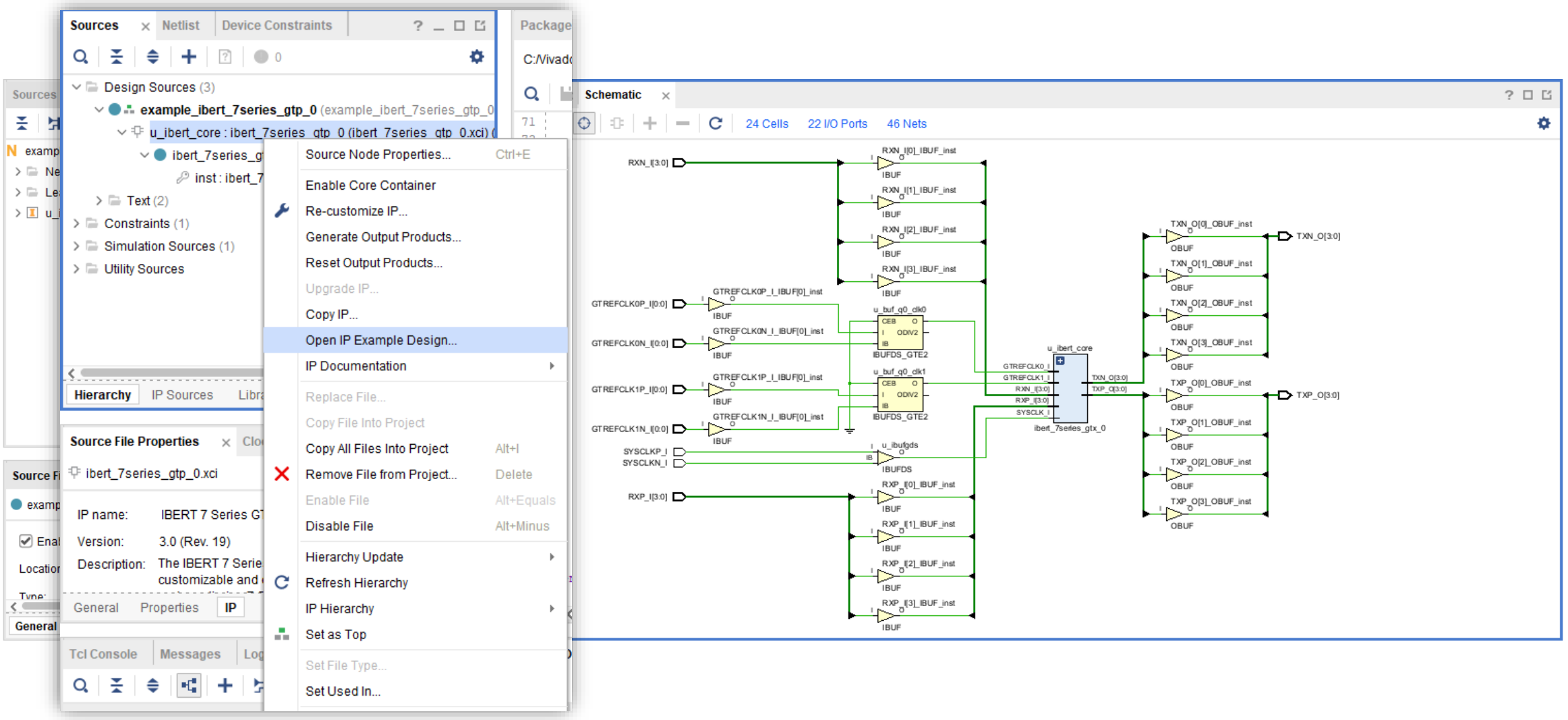
AMD XILINX

IBERT IP Setting



AMD XILINX

IBERT Example Design



AMD XILINX

IBERT Example Design

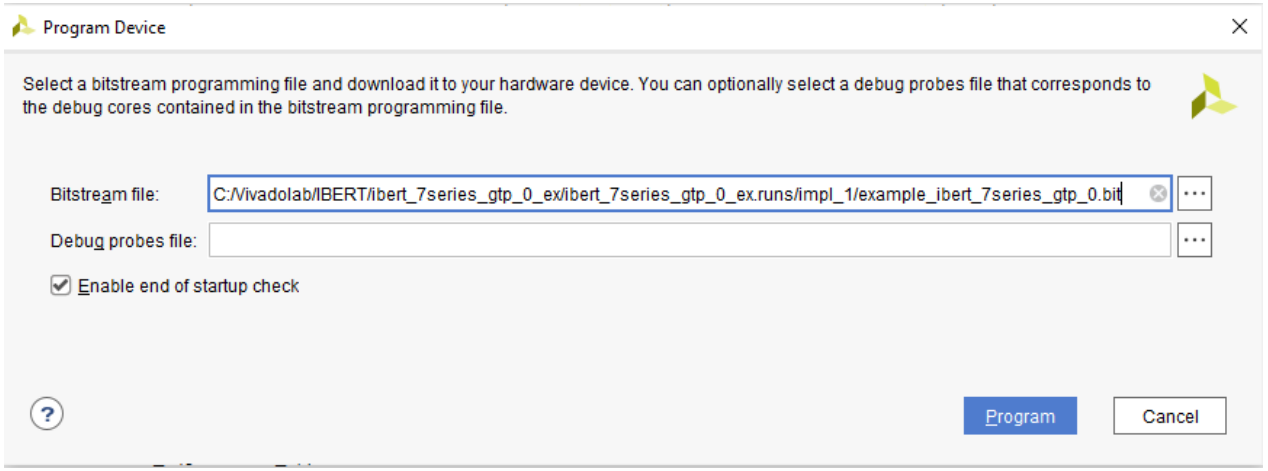
Port Descriptions

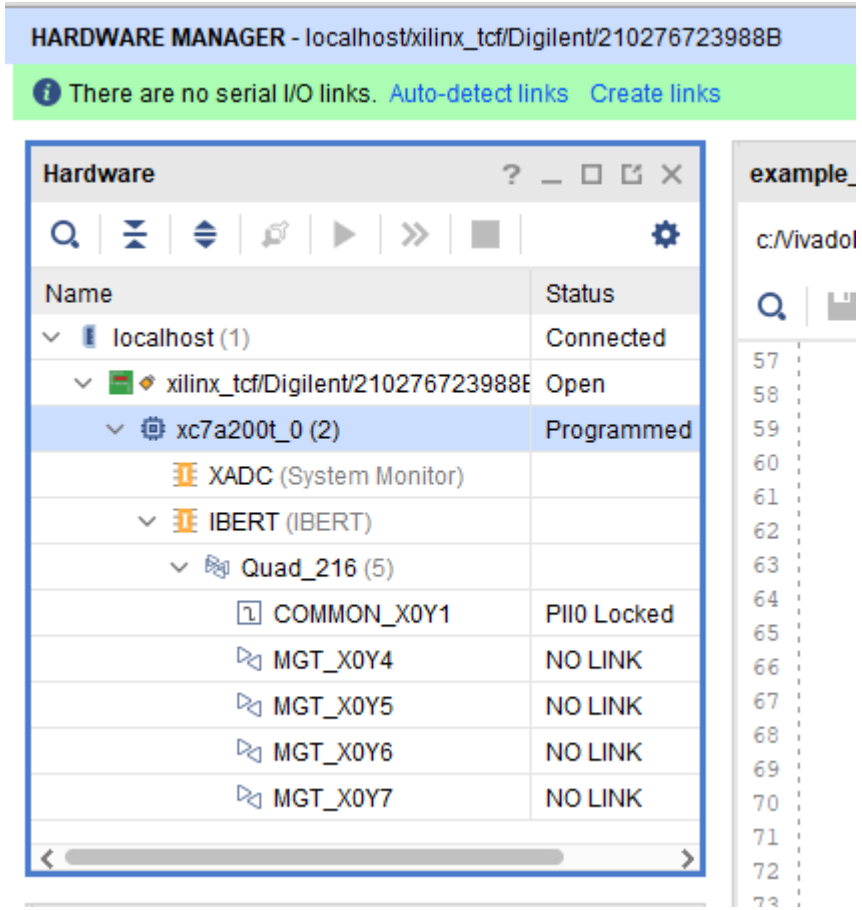
The core ports are shown in Table 2-1.

Table 2-1: **Core Ports**

Signal Name	I/O	Description
SYSCLOCK_I	I	Clock that clocks all communication logic. This port is present only when an external clock is selected in the generator.
TXN_O[7:0] TXP_O[7:0]	O	Transmit differential pairs for each of the n GTP transceivers used.
RXN_O[7:0] RXN_O[7:0]	I	Receive differential pairs for each of the n GTP transceivers used.
GTREFCLK0_I[1:0] GTREFCLK1_I[1:0]	I	GTP transceiver reference clocks used. The number of MGTREFCLK ports can be equal to or less than the number of transmit and receive ports because some GTP transceivers can share clock inputs.
RXOUTCLK_O	O	Quad based RX output clock.

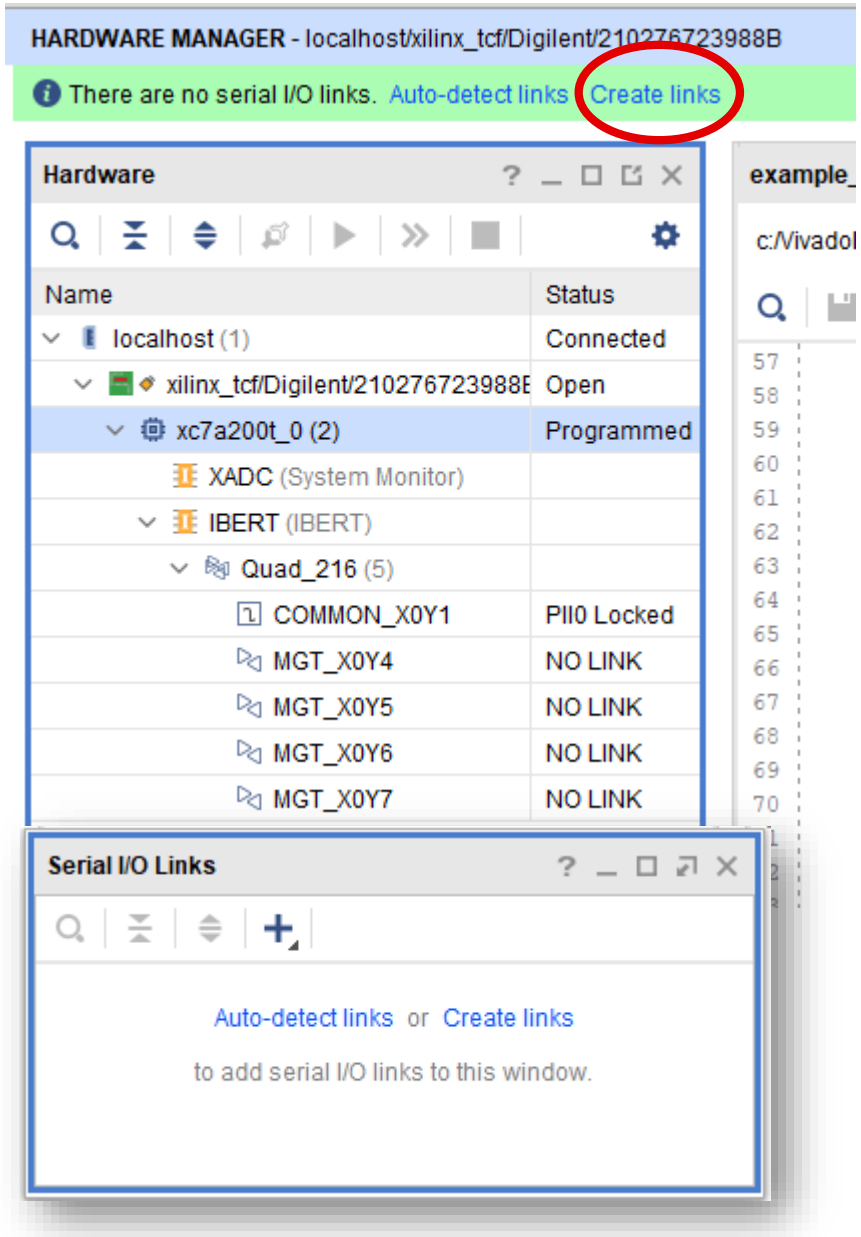
IBERT Debugging

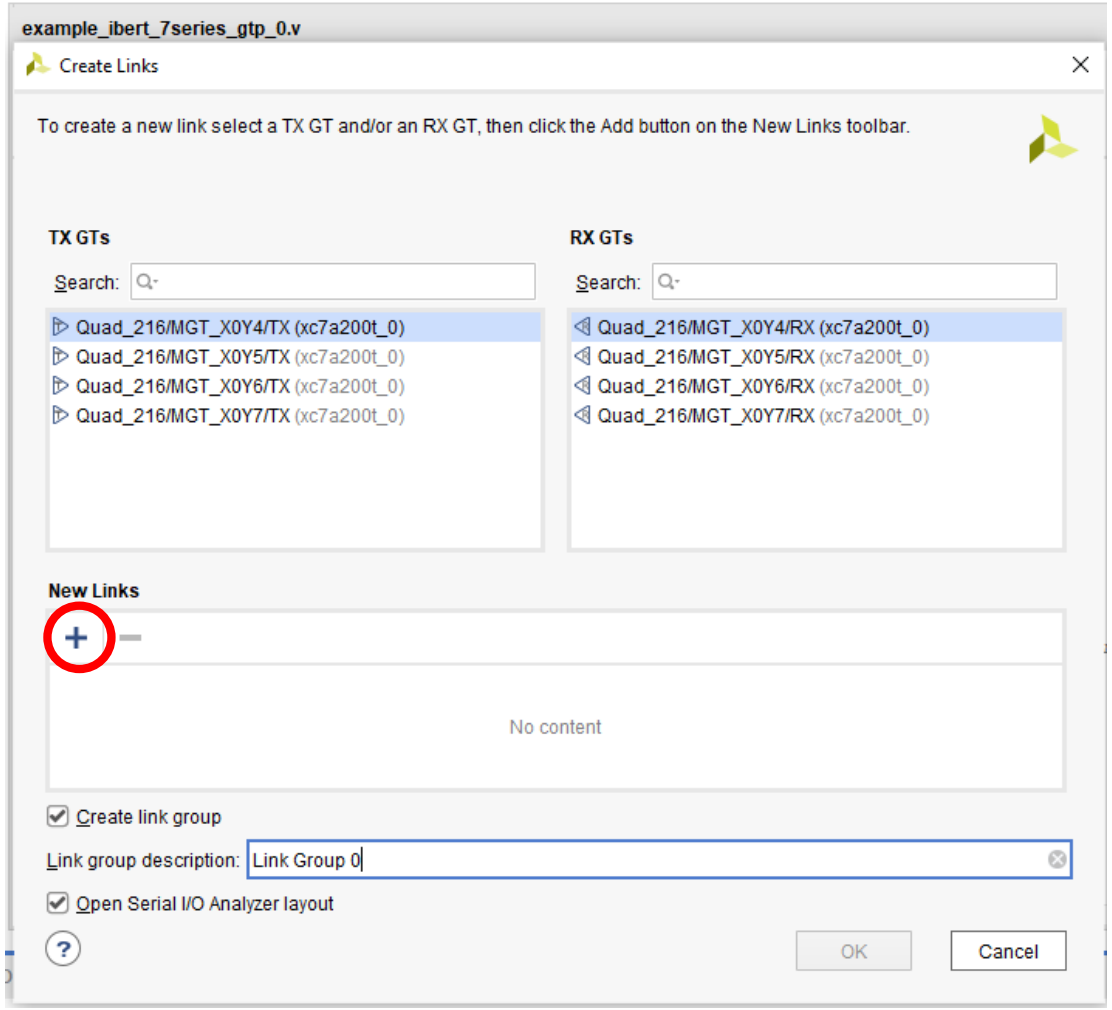




AMD XILINX

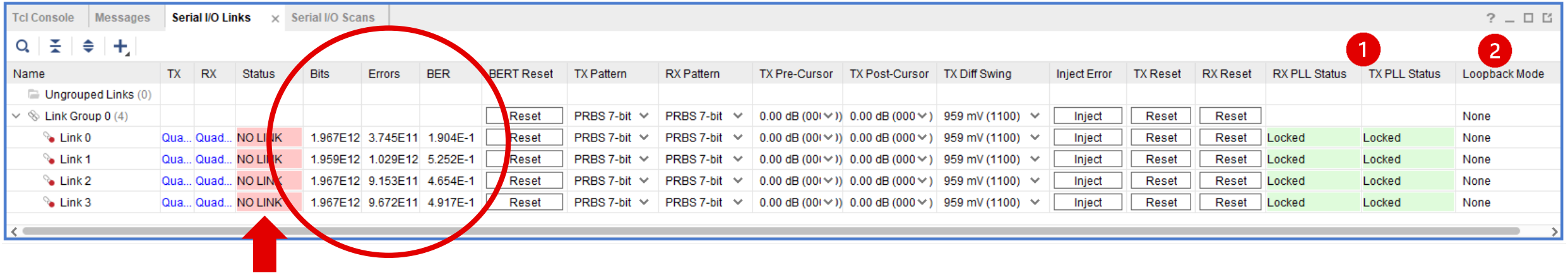
IBERT Debugging





AMD XILINX

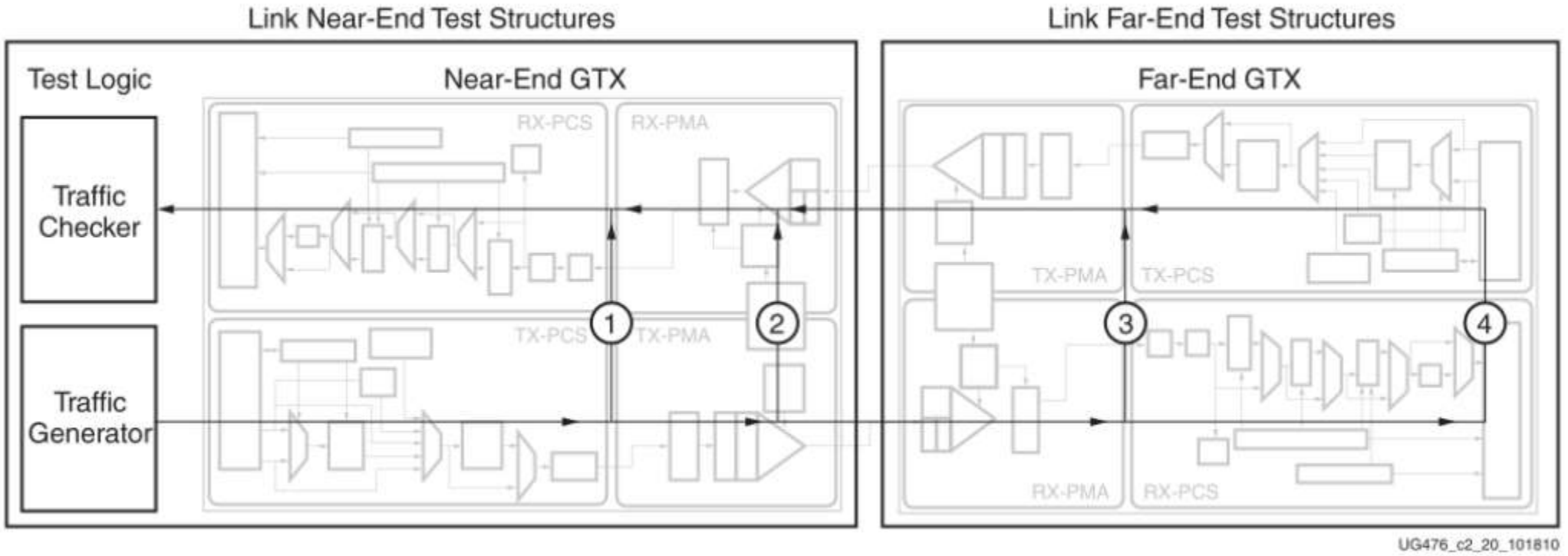
IBERT Debugging



Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status	Loopback Mode
Ungrouped Links (0)																		
Link Group 0 (4)							Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00	0.00 dB (000	959 mV (1100)	Inject	Reset	Reset			None
Link 0	Qua...	Quad...	NO LINK	1.967E12	3.745E11	1.904E-1	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00	0.00 dB (000	959 mV (1100)	Inject	Reset	Reset	Locked	Locked	None
Link 1	Qua...	Quad...	NO LINK	1.959E12	1.029E12	5.252E-1	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00	0.00 dB (000	959 mV (1100)	Inject	Reset	Reset	Locked	Locked	None
Link 2	Qua...	Quad...	NO LINK	1.967E12	9.153E11	4.654E-1	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00	0.00 dB (000	959 mV (1100)	Inject	Reset	Reset	Locked	Locked	None
Link 3	Qua...	Quad...	NO LINK	1.967E12	9.672E11	4.917E-1	Reset	PRBS 7-bit	PRBS 7-bit	0.00 dB (00	0.00 dB (000	959 mV (1100)	Inject	Reset	Reset	Locked	Locked	None

AMD XILINX

IBERT Debugging



AMD XILINX

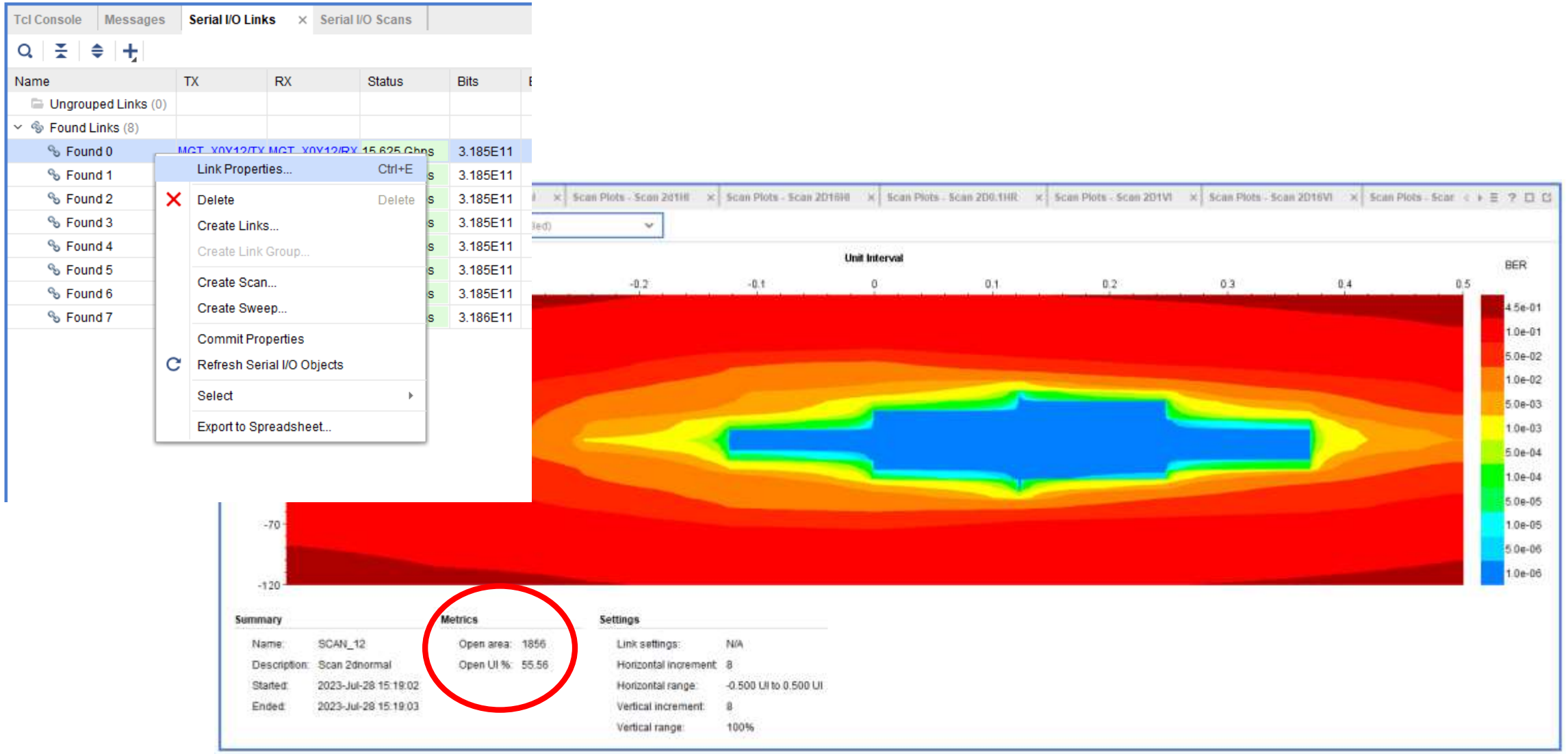
IBERT Debugging

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	...	...	...	...	...	...	...	...	RX PLL Status	TX PLL Status	Loopback Mode
Ungrouped Links (0)																		
Found Links (2)							Reset											Near-End PCS
Auto detected link 0	Quad_216...	Quad_216...	3.131 Gbps	1.574E12	1.241E10	7.881E-3	Reset									Locked	Locked	Near-End PCS
Auto detected link 1	Quad_216...	Quad_216...	3.118 Gbps	1.568E12	1.264E10	8.064E-3	Reset									Locked	Locked	Near-End PCS

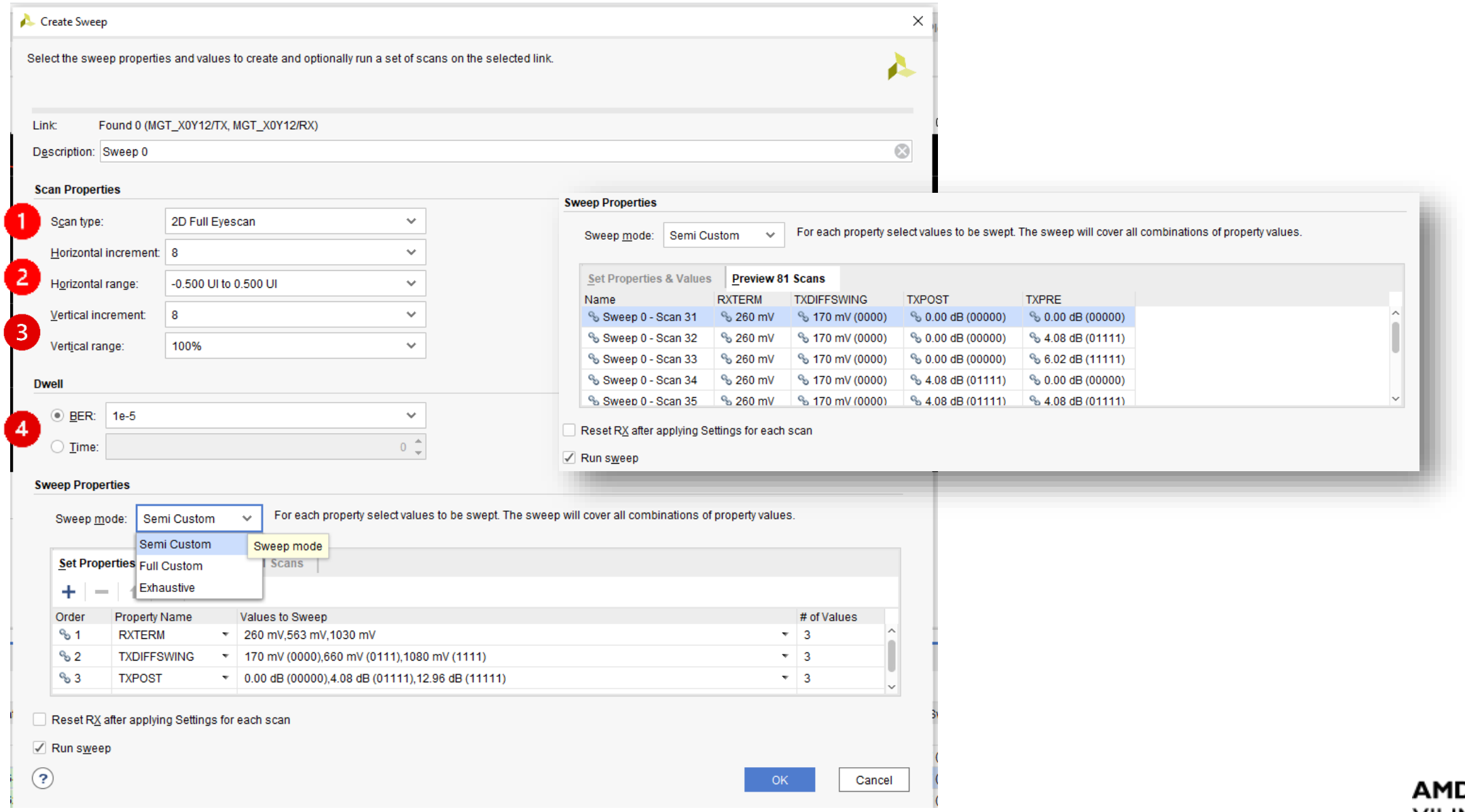
TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	Inject Error	TX Reset	RX Reset
PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	959 mV (1100)	Inject	Reset	Reset
PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	959 mV (1100)	Inject	Reset	Reset
PRBS 7-bit	PRBS 7-bit	0.00 dB (00000)	0.00 dB (00000)	959 mV (1100)	Inject	Reset	Reset

PRBS 7-bit
PRBS 15-bit
PRBS 23-bit
PRBS 31-bit
Fast Clk
Slow Clk

Eye Pattern

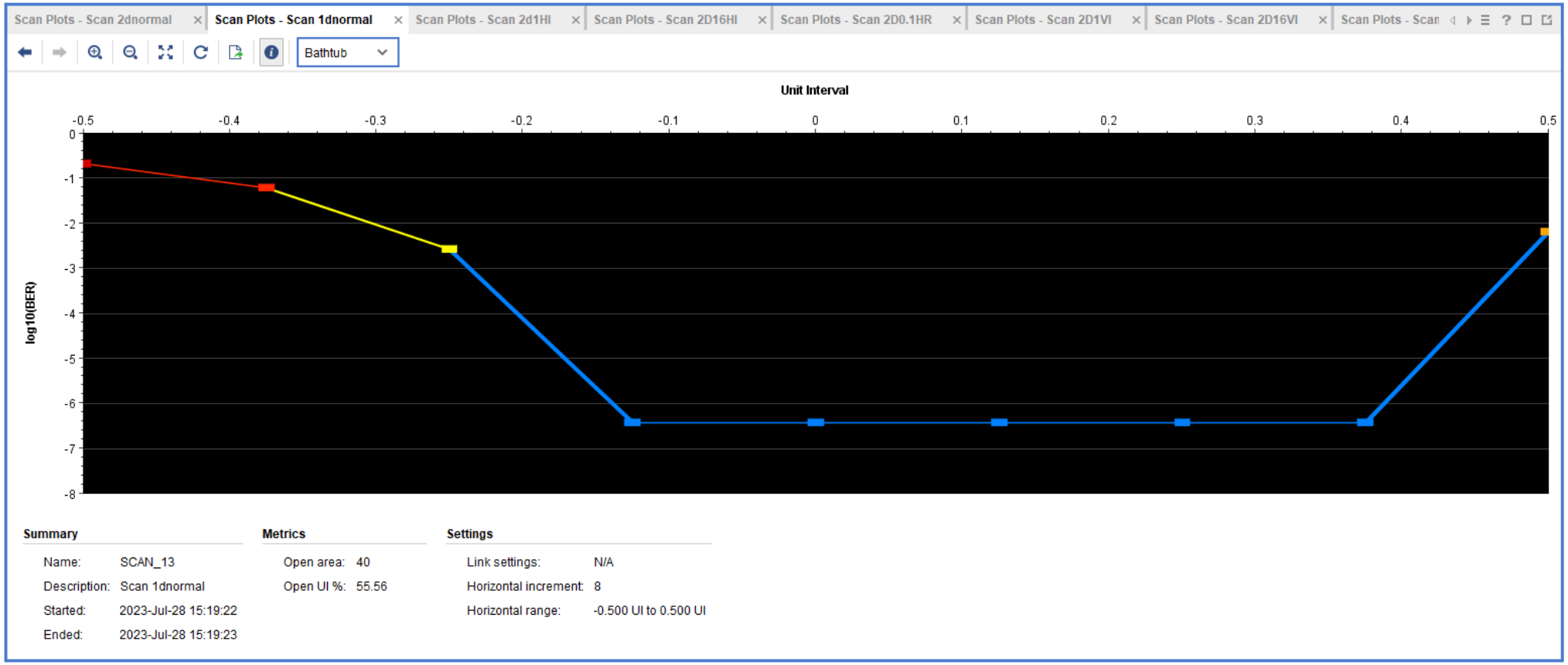


Eye Pattern



AMD XILINX

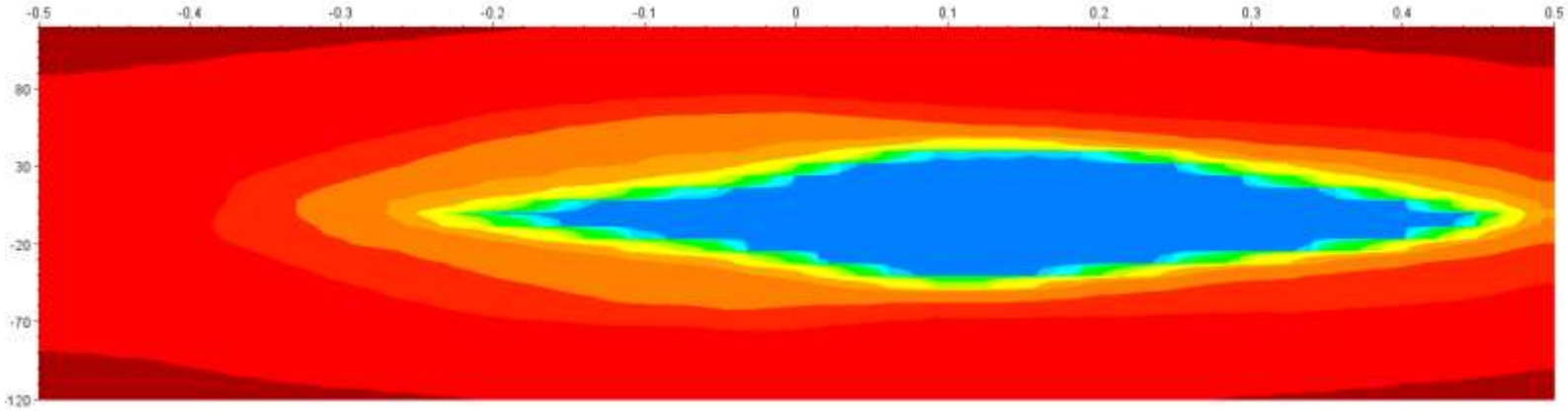
Eye Pattern



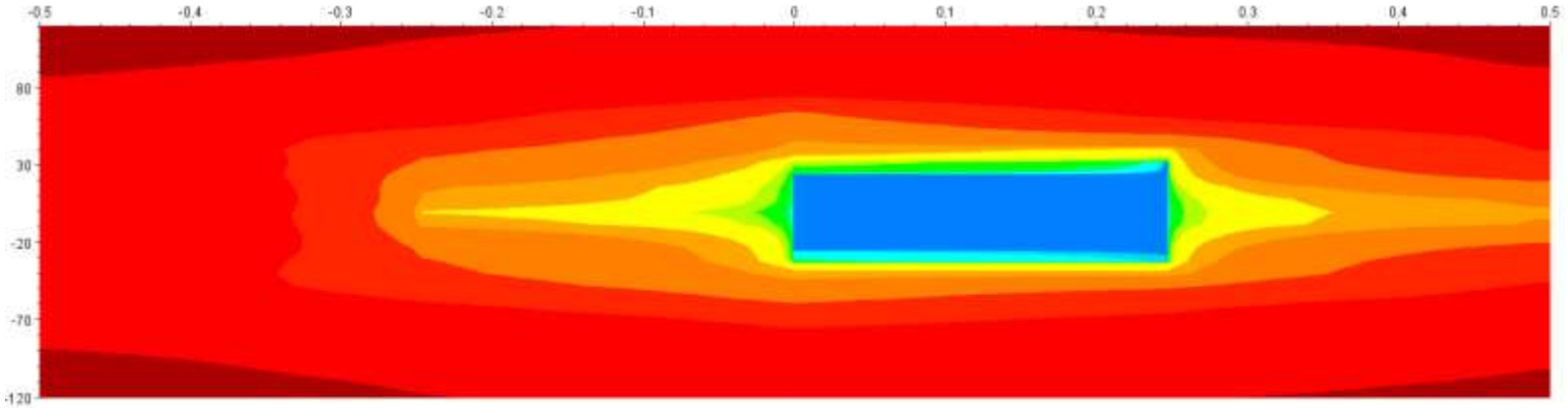
AMD XILINX

Eye Pattern

Horizantal incremental (1)



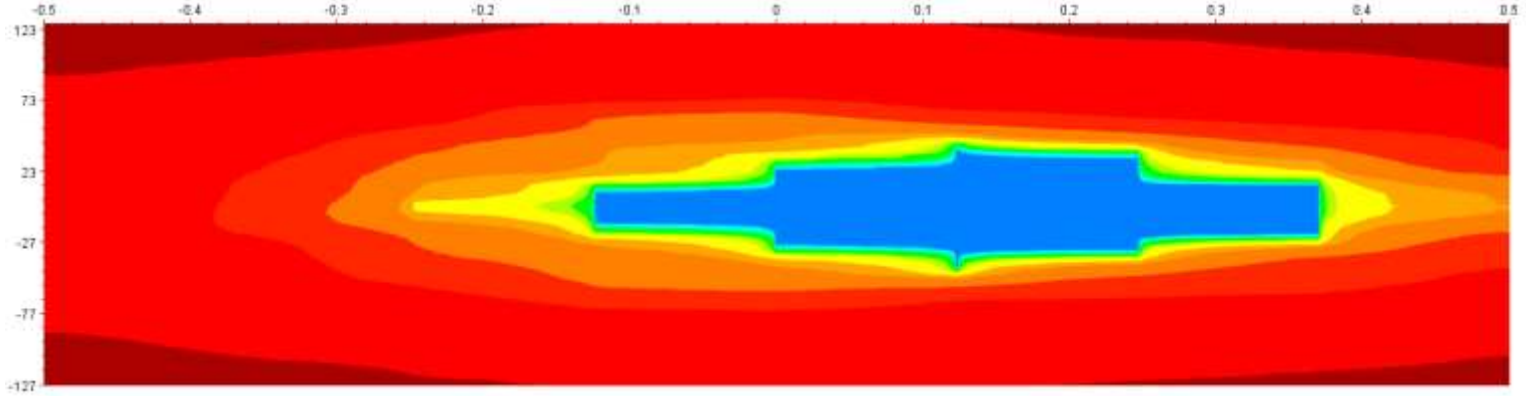
Horizantal incremental (16)



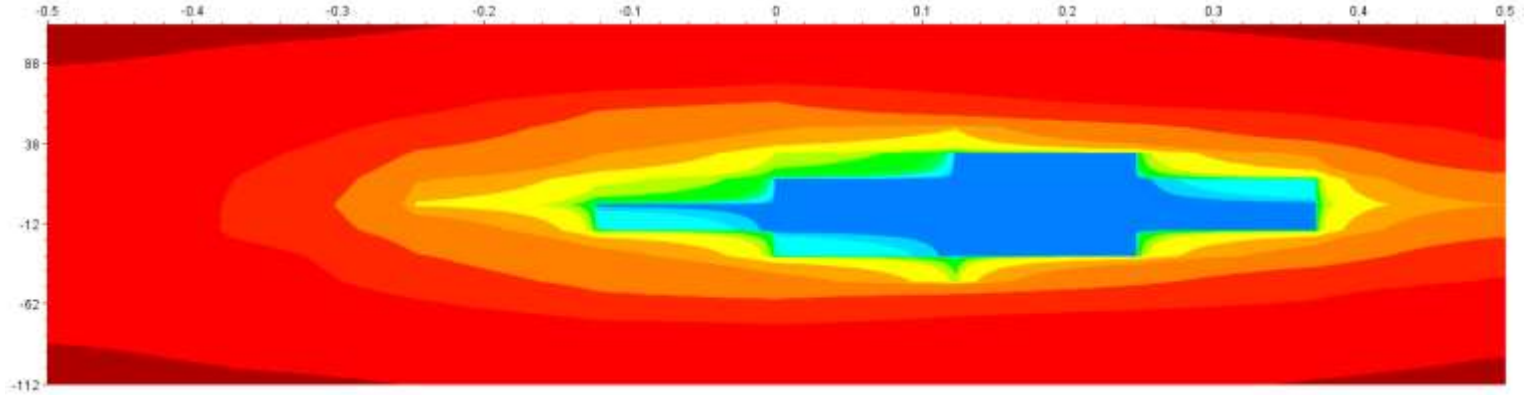
AMD XILINX

Eye Pattern

Vertical incremental (1)



Vertical incremental (16)



AMD
XILINX

AMD
XILINX

Thank you very much for your attention!

Course Agenda
2023