



Memory Interface Generator

Course Agenda
2023

Agenda

- ▶ **Introduction to the DDR**
- ▶ **MIG IP Setting**
- ▶ **7Series FPGAs Memory Interface Solution**
- ▶ **Calibration**
- ▶ **How to access DDR via MIG**

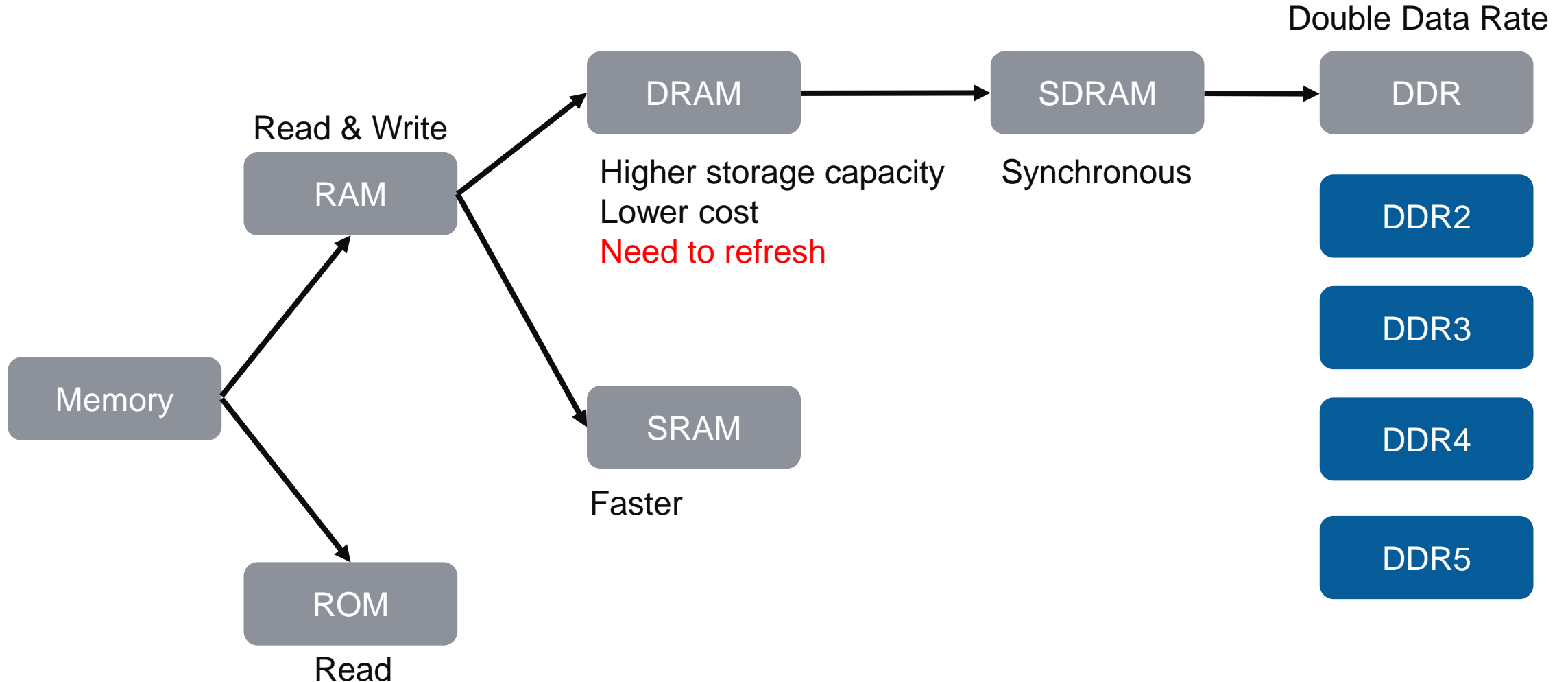


Double Data Rate Synchronous Dynamic Random Access Memory

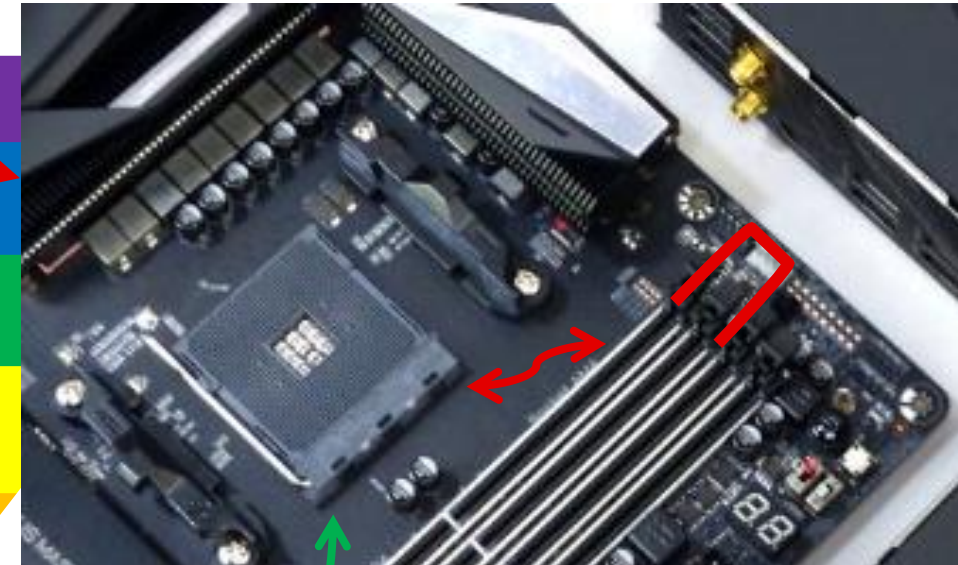
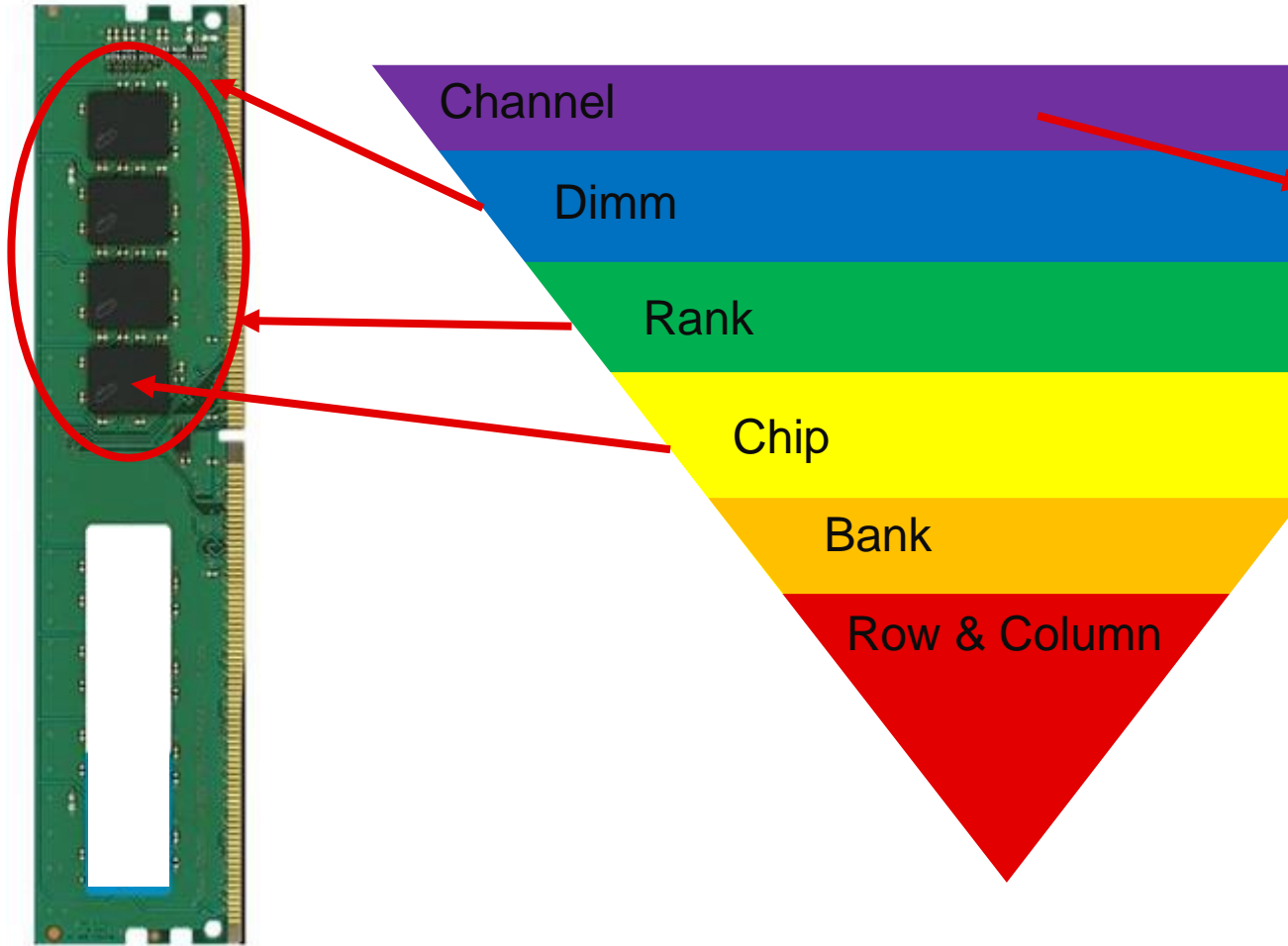
2023

What is the DDR?

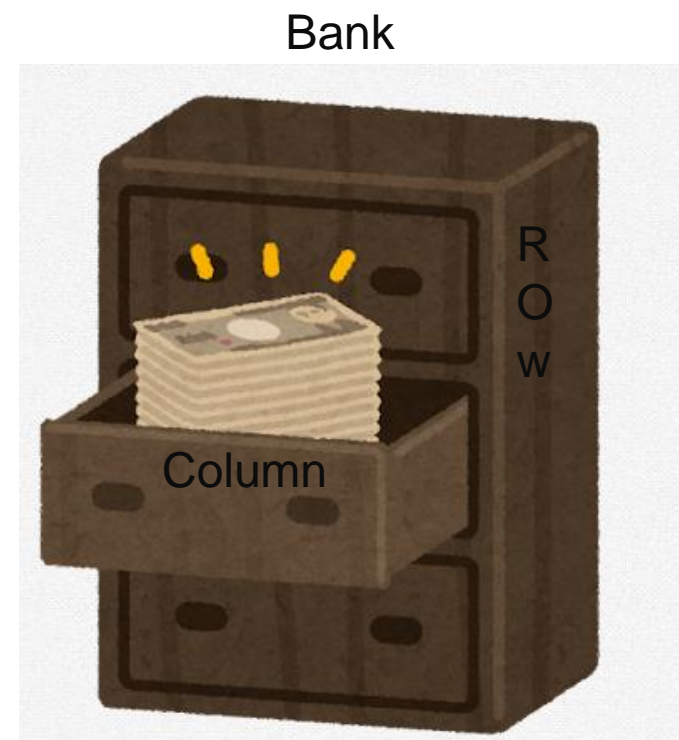
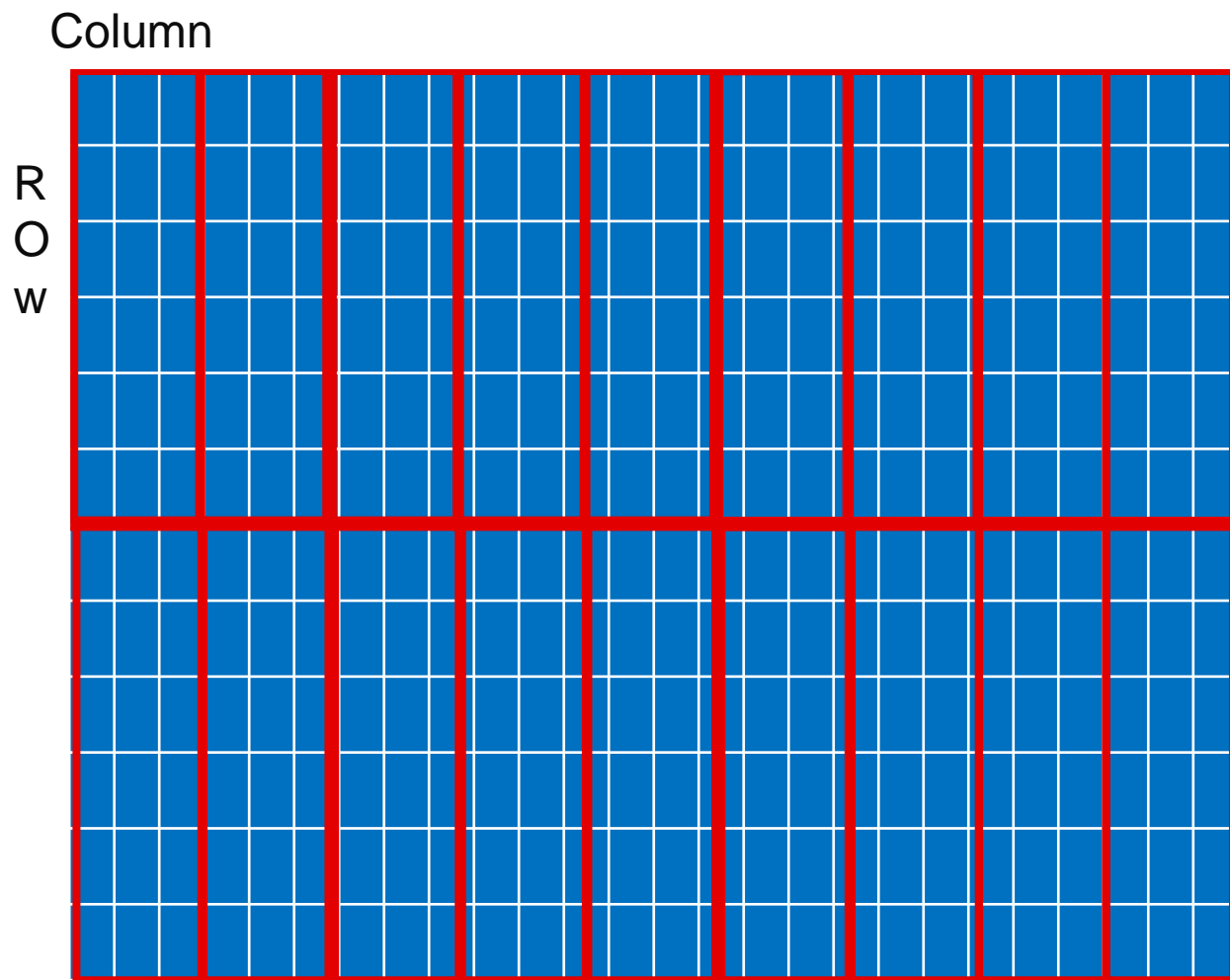
Double Data Rate Synchronous Dynamic Random Access Memory



What is the DDR?



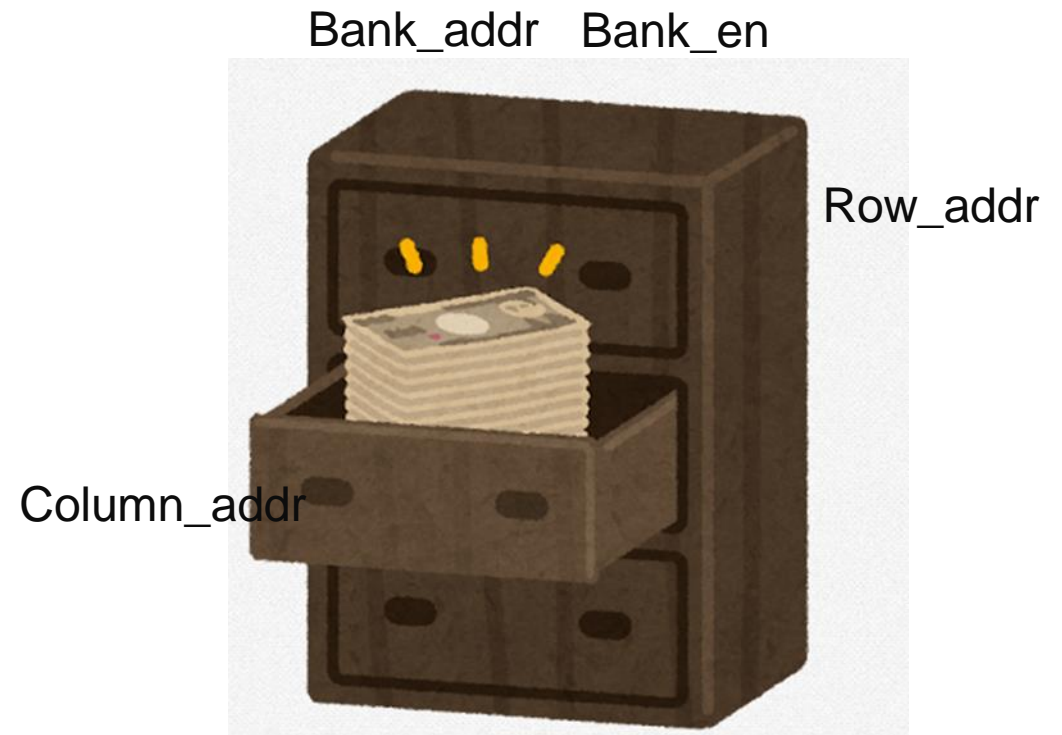
What is the DDR?



How DDR work?

31bit_addr

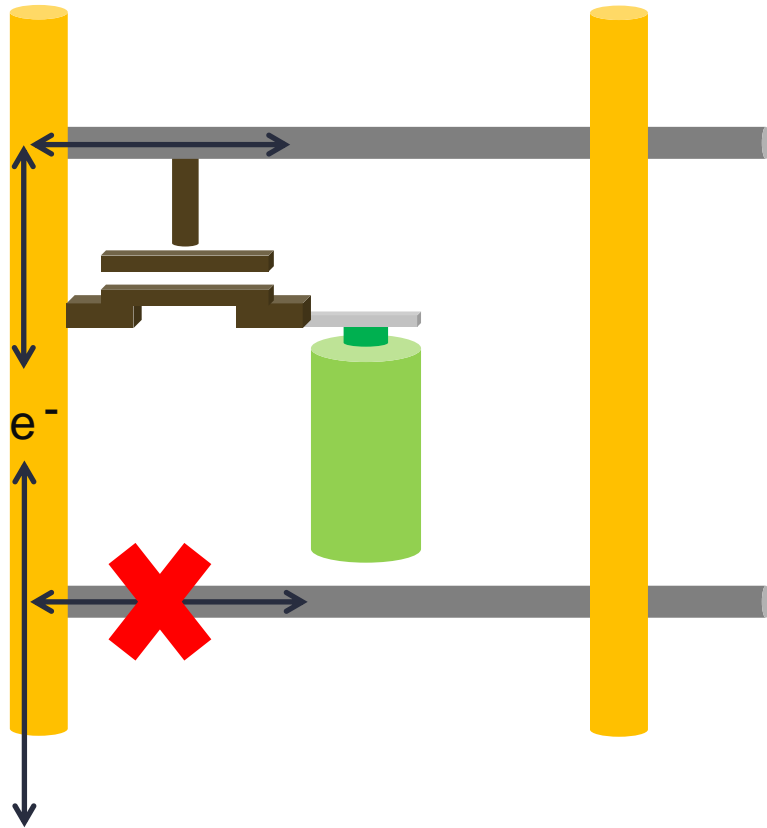
0011001100011010111001001000011
└──┬──────────┬──────────┘
Bank Row_addr Column_addr



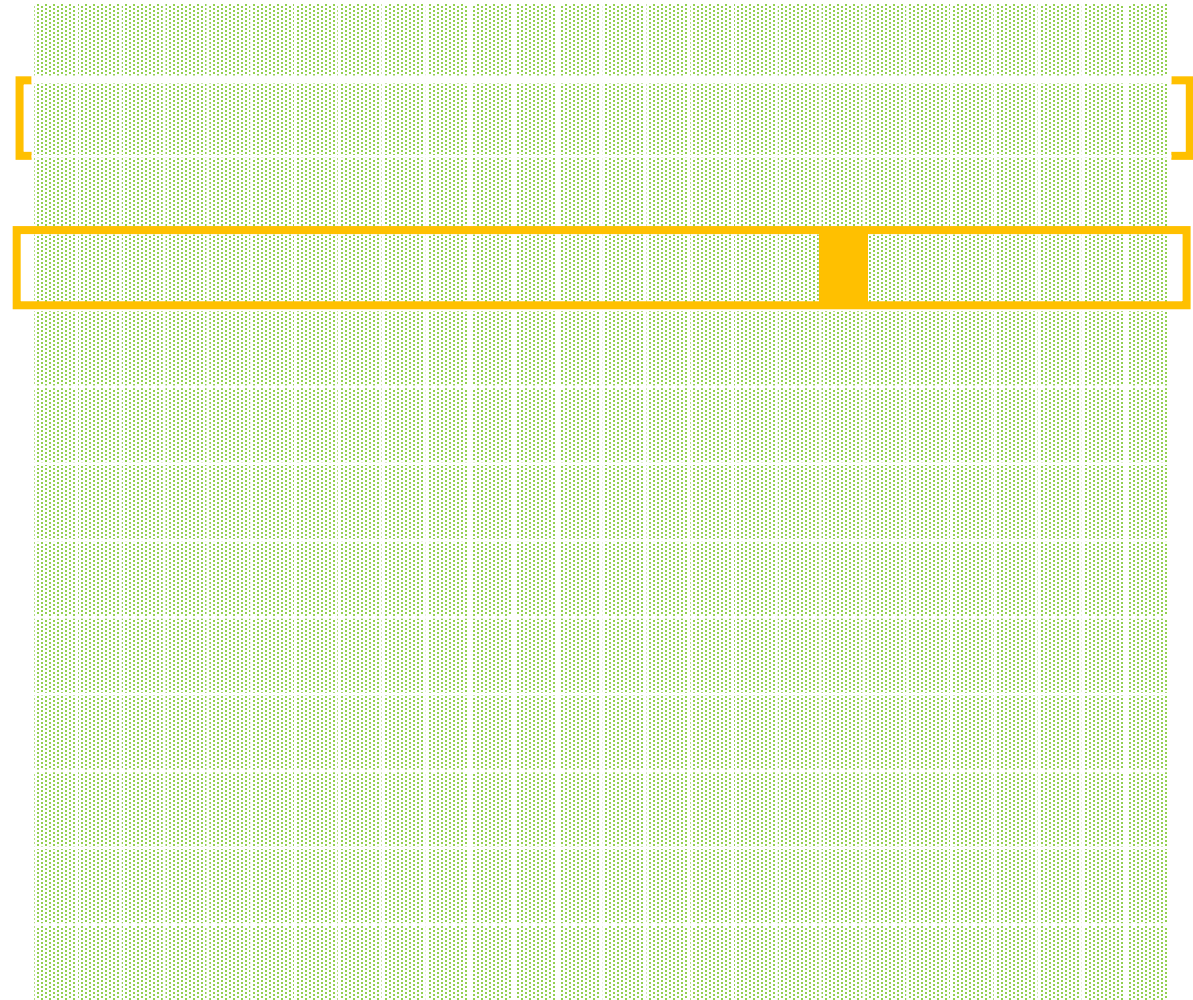
How DDR work?

31bit_addr

0011001100011010111001001000011



Bank





MIG Setting

Course Agenda
2023

MIG IP Setting

Project Summary x IP Catalog x

Cores | Interfaces

Q

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■

Search: Q- MIG (7 matches)

Name

▼ Vivado Repository

▼ Memories & Storage Elements

▼ External Memory Interface

DDR3 SDRAM (MIG)

DDR4 SDRAM (MIG)

LPDDR3 SDRAM (MIG)

QDRII+ SRAM (MIG)

QDRIV SRAM (MIG)

RLDRAM3 (MIG)

▼ Memory Interface Generators

Memory Interface Generator (MIG 7 Series)

Memory Interface Generator

The Memory Interface Generator (MIG) creates memory controllers for Xilinx FPGAs. MIG creates complete customized Verilog or VHDL RTL source code, pin-out and design constraints for the FPGA selected, and script files for implementation and simulation.

Vivado Project Options

This GUI includes all configurable options along with explanations to aid in generation of the required controller. Please note that some of the options selected in the Vivado Project Options will be used in generation of the controller. It is very important that the correct Vivado Project Options are selected. These options are listed below.

Selected Vivado Project Options:

Fpga Family : Kintex-7

Fpga Part : xc7k325t-ffg900

Speed Grade : -1

Synthesis Tool : VIVADO

Design Entry : VERILOG

If any of these options are incorrect, please click on "Cancel", change the Vivado Project Options, and restart MIG. This version of MIG is tested with Vivado 2018.3 or later, it is not tested with previous versions of Vivado.

AXI4	Production	Included	xilinx.com:ip:mig_7series:4.2
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MIG IP Setting

MIG Output Options



Create Design

Select this option to generate a memory controller. Generating a memory controller will create RTL, XDC, implementation and simulation files.



Verify Pin Changes and Update Design

Selecting this feature verifies the modified XDC for a design already generated through MIG. This option will allow you to change the pin out and validate it instantly. It updates the input XDC file to be compatible with the current version of MIG. While updating the XDC it preserves the pin outs of the input XDC. This option will also generate the new design with the Component Name you selected in this page.

Component Name

Please specify the component name for the memory interface. The design directories will be generated under a directory with this name. Three directories will be created "example_design", "user_design" and "docs". The user_design will contain the generated memory interface. The example_design adds a simple example application connected to the generated memory interface.

Component Name

Multi-Controller

Up to maximum of 8 controllers with a combination of DDR3 SDRAM, QDR II+ SRAM or RLDRAM II can be generated. The number of controllers that can be accommodated may be limited by the data width and the number of banks available in device. Refer user guide for more information

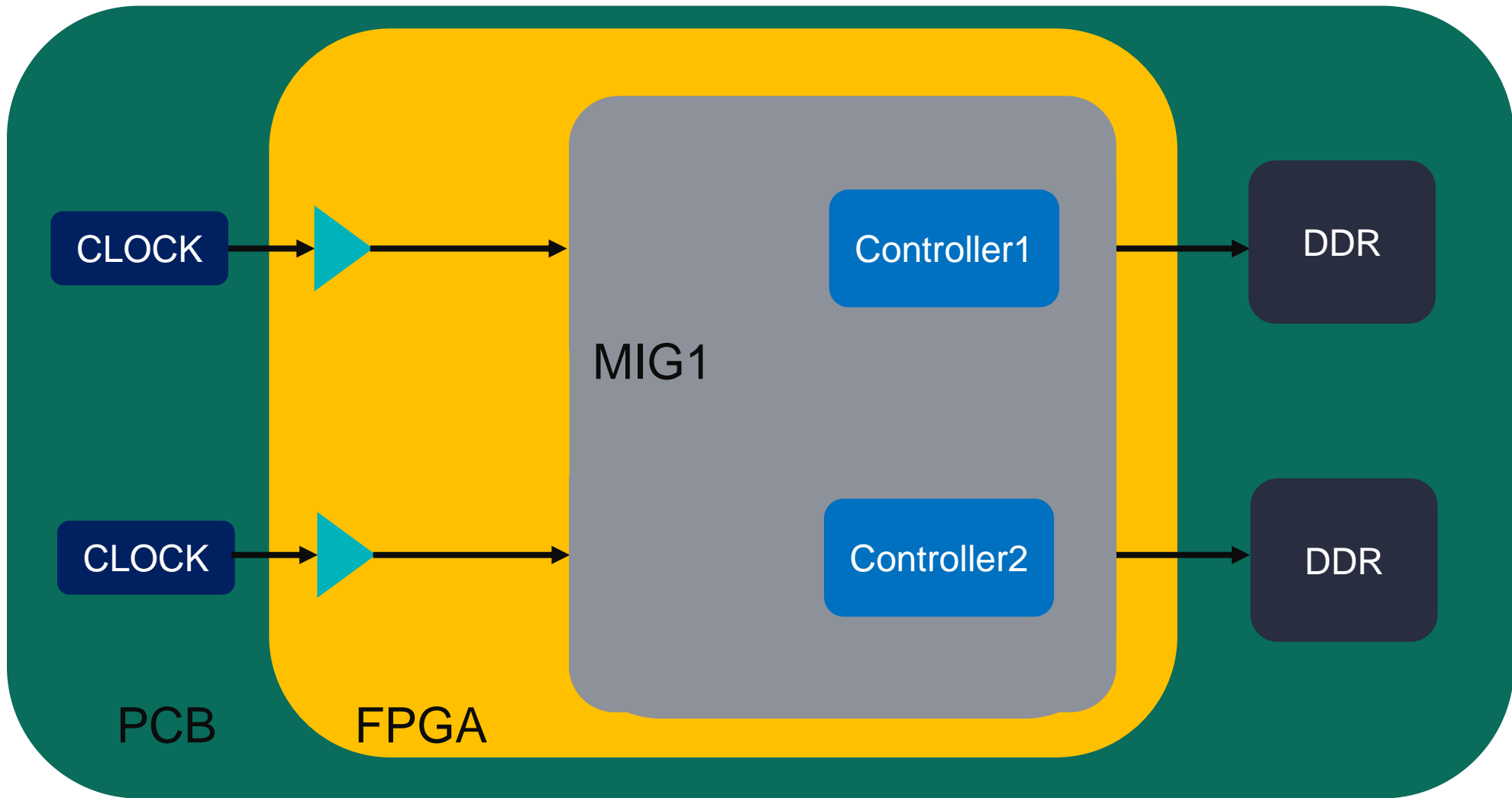
Number of controllers

AXI4 Interface

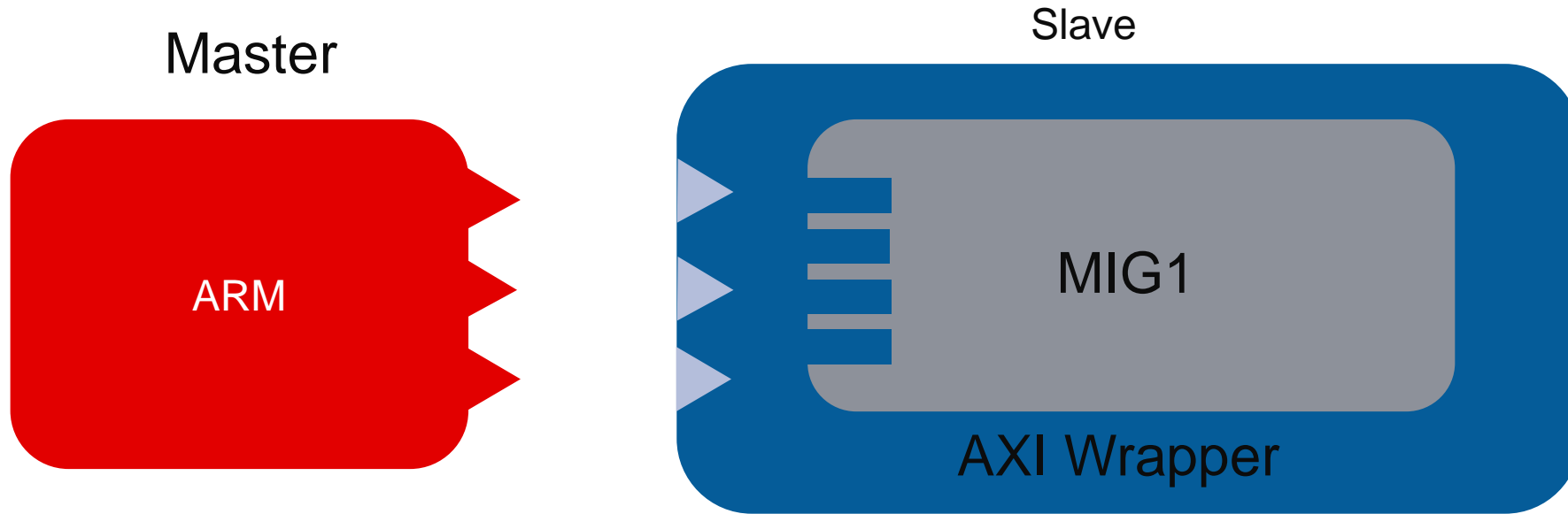
Enables the AXI4 interface. AXI4 interface is supported only for DDR3 SDRAM and DDR2 SDRAM controllers with Verilog design entry.

☐ AXI4 Interface

Multi-Controller



AXI-4 Interface



Ping Compatible

Pin Compatible FPGAs

Pin Compatible FPGAs include all devices with the same package and speed grade as the target device. Different FPGA devices with the same package do not have the same bonded pins. By selecting Pin Compatible FPGAs, MIG will only select pins that are common between the target device and all selected devices. Use the default XDC in the par folder for the target part. If the target part is changed, use the appropriate XDC in the compatible_ucf folder. **If a Pin Compatible FPGA is not chosen now and later a different FPGA is used, the generated XDC may not work for the new device and a board spin may be required.** MIG only ensures that MIG generated pin out is compatible among the selected compatible FPGA devices. Unselected devices will not be considered for compatibility during the pin allocation process.

A blank list indicates that there are no compatible parts exist for the selected target part and this page can be skipped.

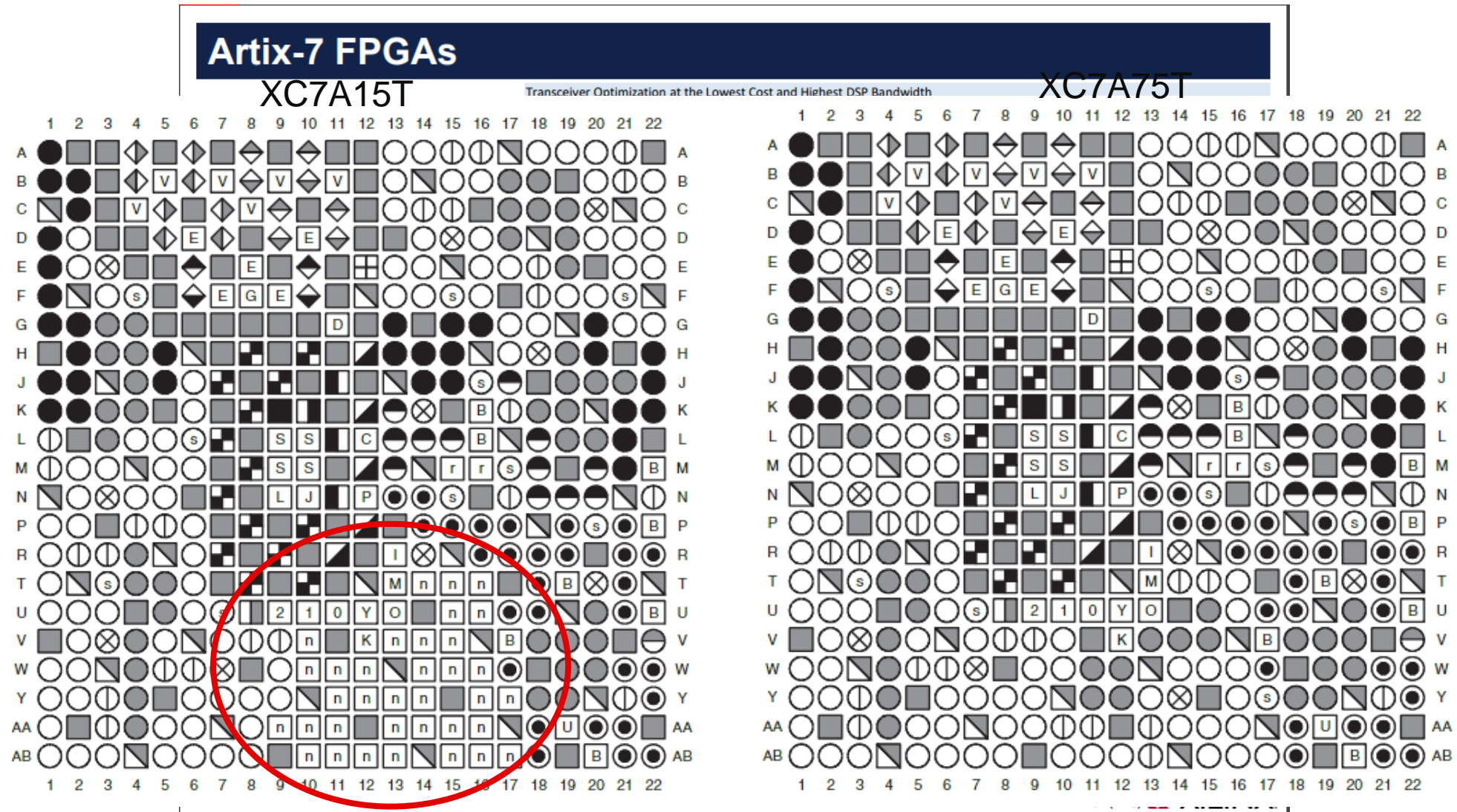
Note that different parts in the same package will have different internal package skew values. De-rate the minimum period appropriately in the Controller Options page when different parts in the same package are used. Consult the User Guide for more information.

Target FPGA:

Pin Compatible FPGAs

- ▼ ☐ kintex7
 - ▼ ☐ 7k
 - ☐ xc7k410t-ffg900

Ping Compatible



Memory Selection

Memory Interface Generator

VIVADO[®]

ML Editions

Pin Compatible FPGAs

Memory Selection

Controller Options

AXI Parameter

Memory Options

FPGA Options

Extended FPGA Options

IO Planning Options

Bank Selection

System Signals Selection

Summary

Simulation Options

PCB information

Design Notes

XILINX[®]

User Guide

Memory Selection

Select the type of memory interface. Please refer to the User Guide for a detailed list of supported controllers for each FPGA family. The list below shows currently available interface(s) for the specific FPGA, speed grade and design entry chosen.

Select the controller type:

☒ DDR3 SDRAM

☐ DDR2 SDRAM

☐ QDRII+ SRAM

☐ RLD RAM II

☐ RLD RAM III

☐ LPDDR2 SDRAM

Multi-Controller

Up to maximum of 8 controllers with a combination of DDR3 SDRAM, QDRII+ SRAM or RLD RAM II can be generated. The number of controllers that can be accommodated may be limited by the data width and the number of banks available in device. Refer user guide for more information

Number of controllers

Memory Selection

Select the type of memory interface. Please refer to the User Guide for a detailed list of supported controllers for each FPGA family. The list below shows currently available interface(s) for the specific FPGA, speed grade and design entry chosen.

Select the controller type:

DDR3 SDRAM

QDRII+ SRAM

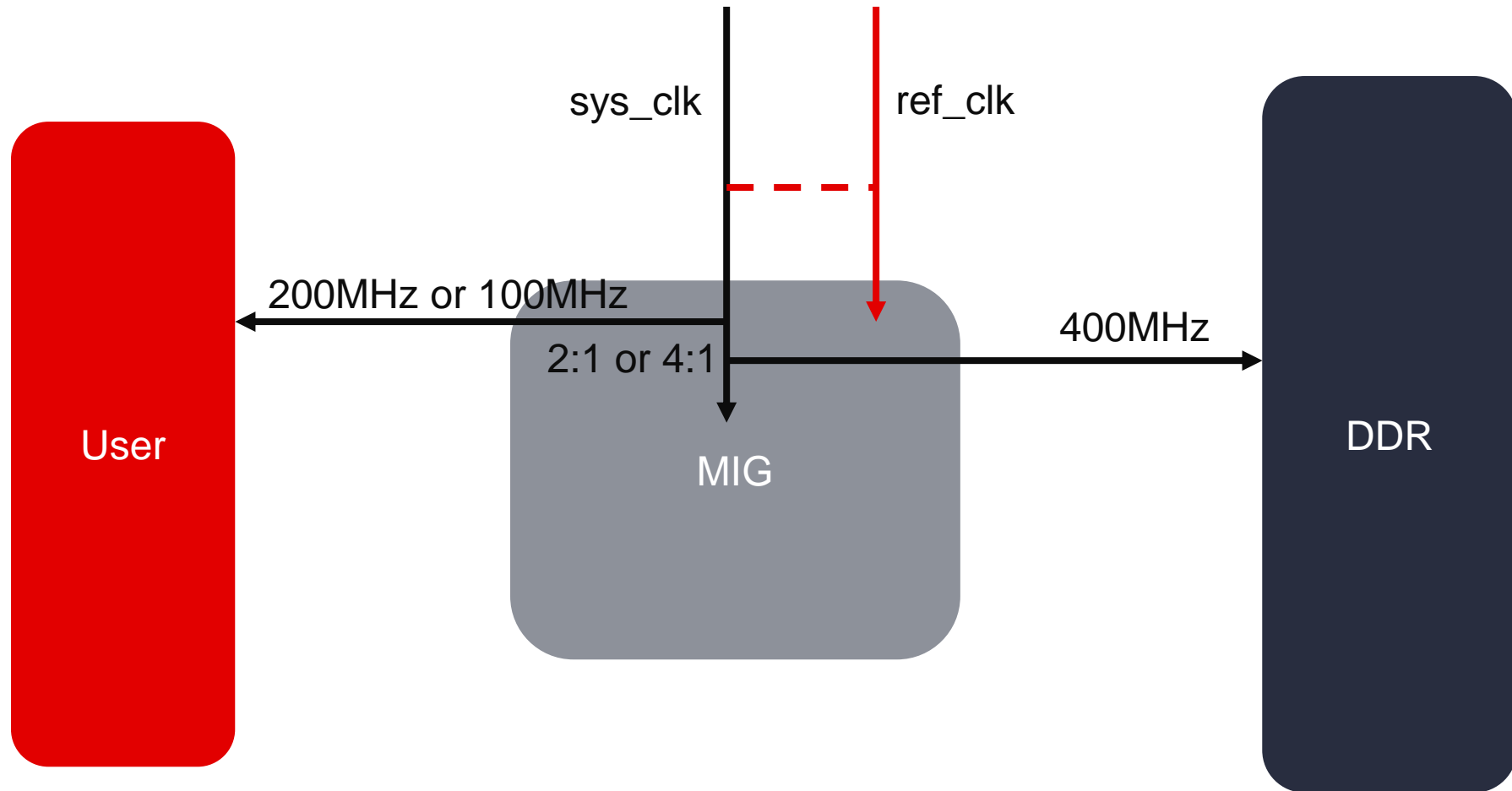
RLD RAM II

< Back

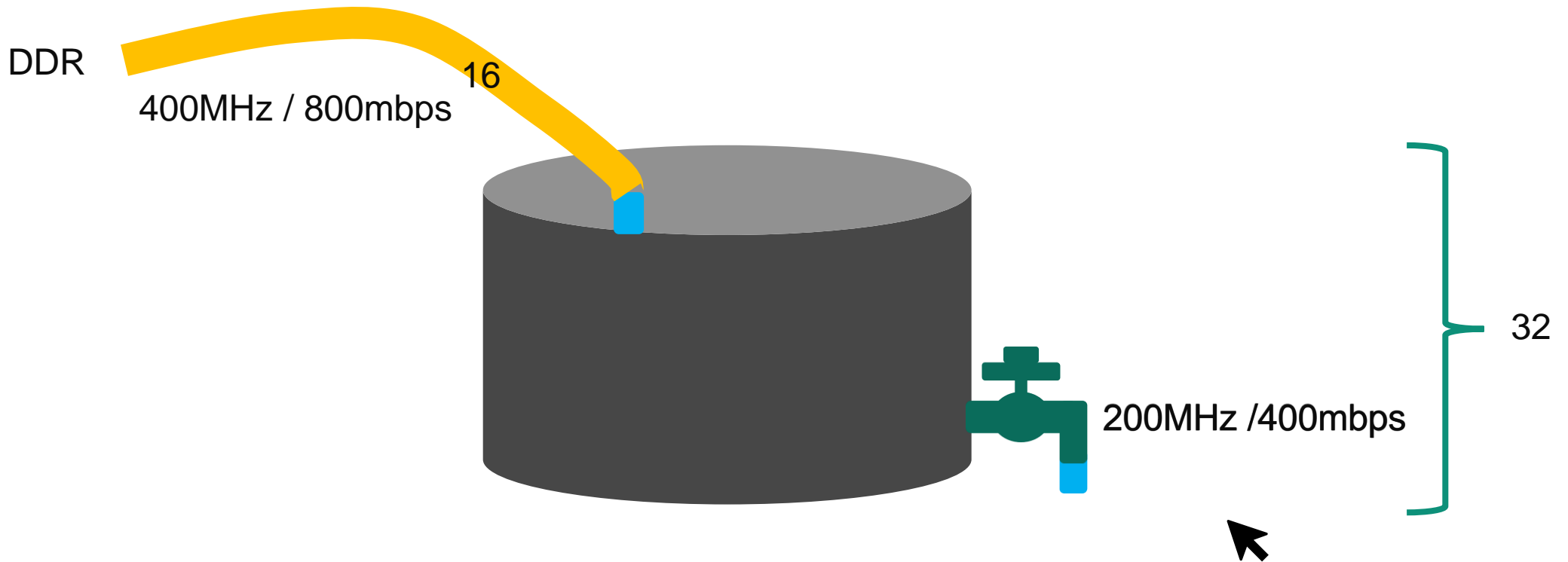
Next >

Cancel

Clock



PHY to Controller Clock Ratio



Controller Option

Options for Controller 0 - DDR3 SDRAM

Clock Period: Choose the clock period for the desired frequency. The allowed period range(1250 - 3300) is a function of the selected FPGA part and FPGA speed grade. Refer to the User Guide for more information.

1250 ps 800.0 MHz

PHY to Controller Clock Ratio: Select the PHY to Memory Controller clock ratio. The PHY operates at the Memory Clock Period chosen above. The controller operates at either 1/4 or 1/2 of the PHY rate. The selected Memory Clock Period will limit the choices.

4:1

Vccaux_io: Vccaux_io must be set to 2.0V in the High Performance banks for the highest data rates. Vccaux_io is not available in the High Range banks. Note that Vccaux_io is common to groups of banks. Consult the 7 Series Datasheets and FPGA SelectIO Resources User Guide for more information.

2.0V

Memory Type: Select the memory type. Type(s) marked with a warning symbol are not compatible with the frequency selection above.

Components

MT41J128M8XX-125

Create Custom Part

Memory Voltage: Select the Voltage of the Memory part selected.

1.5V

Data Width: Select the Data Width. Parts marked with a warning symbol are not compatible with the frequency and memory part selected above.

8

Create custom part

This option create a new memory part. Note that the new memory part will be modification of the 'Base Part' selected below. The timing parameters and density can be changed

Select base part: MT41J128M8XX-125

Enter new memory part name:

Change the required Timing Parameters. "Value" is the only field that can be edited.

Parameter	Value	Range	Unit	Description
tcke	5.625	5-20	ns	CKE minimum pulse width
tfaw	30	25-55	ns	Four Address Width
tras	36	33-37.5	ns	Active to Precharge command
trcd	13.5	10-15	ns	Active to Read or write delay
trefi	7.8	3.9-7.8	us	Average periodic refresh interval
trfc	160	90-350	ns	Refresh to Active or Refresh to Refresh
trp	13.5	10-15	ns	Precharge command period
trrd	6	5-20	ns	Activate minimum command period
trtp	7.5	7.5-20	ns	Read following a Write to the same de
twtr	7.5	7.5-20	ns	Read following a Write to the same de

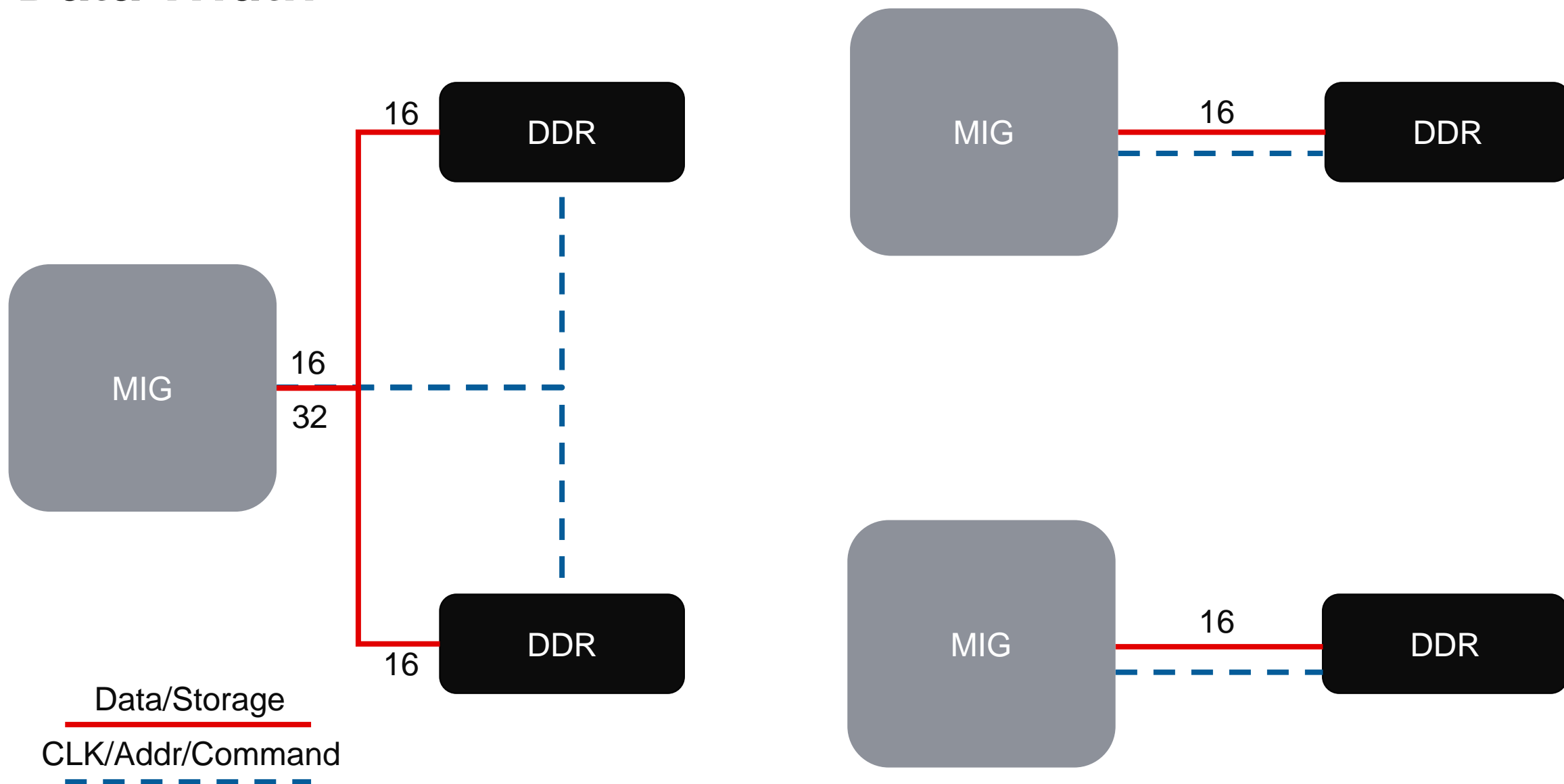
Row address: 15

Column address: 10

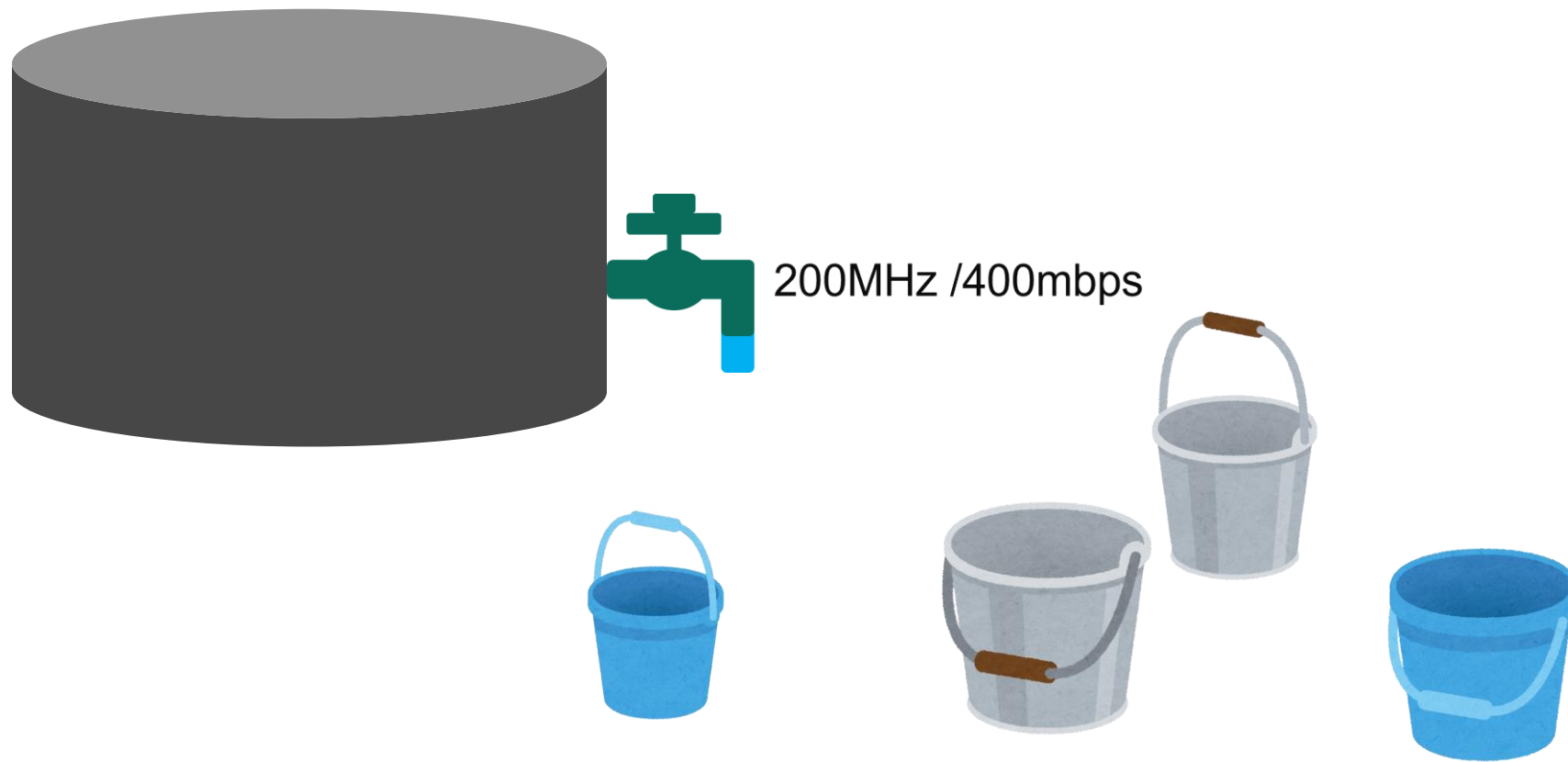
Bank address: 3

Save Delete Close

Data Width



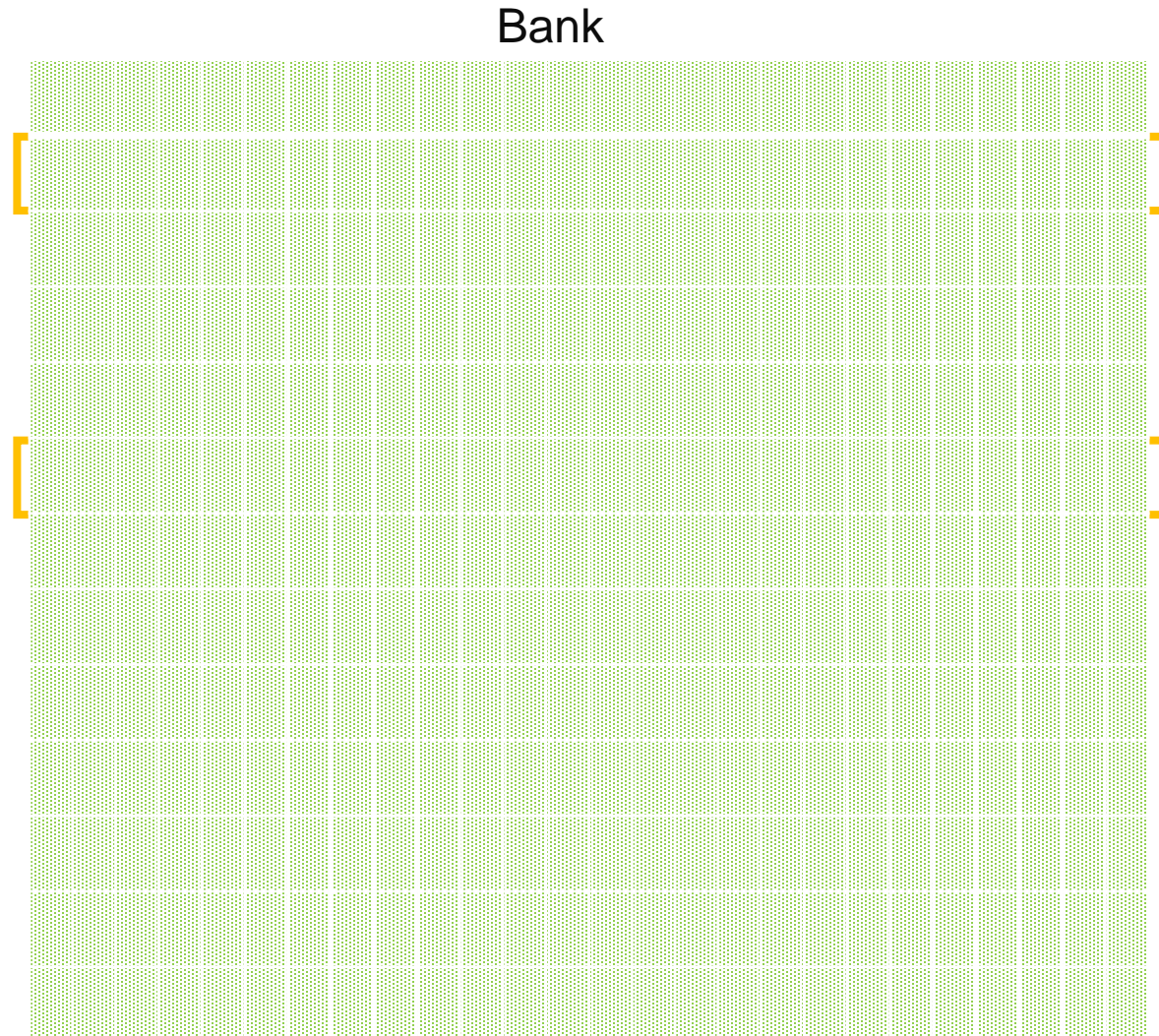
Bank Machine



Ordering

Row Hit ✨

Refresh



Memory Option

Memory Options C0 - DDR3 SDRAM

Input Clock Period: Select the period for the PLL input clock (CLKIN). MIG determines the allowable input clock periods based on the Memory Clock Period entered above and the clocking guidelines listed in the User Guide. The generated design will use the selected Input Clock and Memory Clock Periods to generate the required PLL parameters. If the required input clock period is not available, the Memory Clock Period must be modified.

1250 ps (800 MHz)

Choose the Memory Options for the memory device. Memory Option selections are restricted to those supported by the controller. Consult the memory vendor data sheet for more information.

Read Burst Type and Length

The burst type determines the data ordering within a burst. Consult the memory datasheet for more information. Burst length 8 is the only supported value.

Sequential

Output Driver Impedance Control

Programmable impedance for the output buffer.

RZQ/7

RTT (nominal) - On Die Termination (ODT)

Select the nominal value of ODT for the DQ, DQS/DQS# and DM signals on the component or DIMM interface. This must be set to RZQ/6 i(40 ohms) for data rates at 1333 Mbps and above. In 2 slot DIMM configurations this value will be used for the unwritten slot during a write and will also be used for the unselected slot during a read. Use board level simulation to choose the optimum value.

RZQ/4

Controller Chip Select Pin

The Chip Select (CS#) pin can be tied low externally to save one pin in the address/command group when this selection is set to 'Disable'. Disable is only valid for single rank configurations.

Enable

Memory Address Mapping Selection

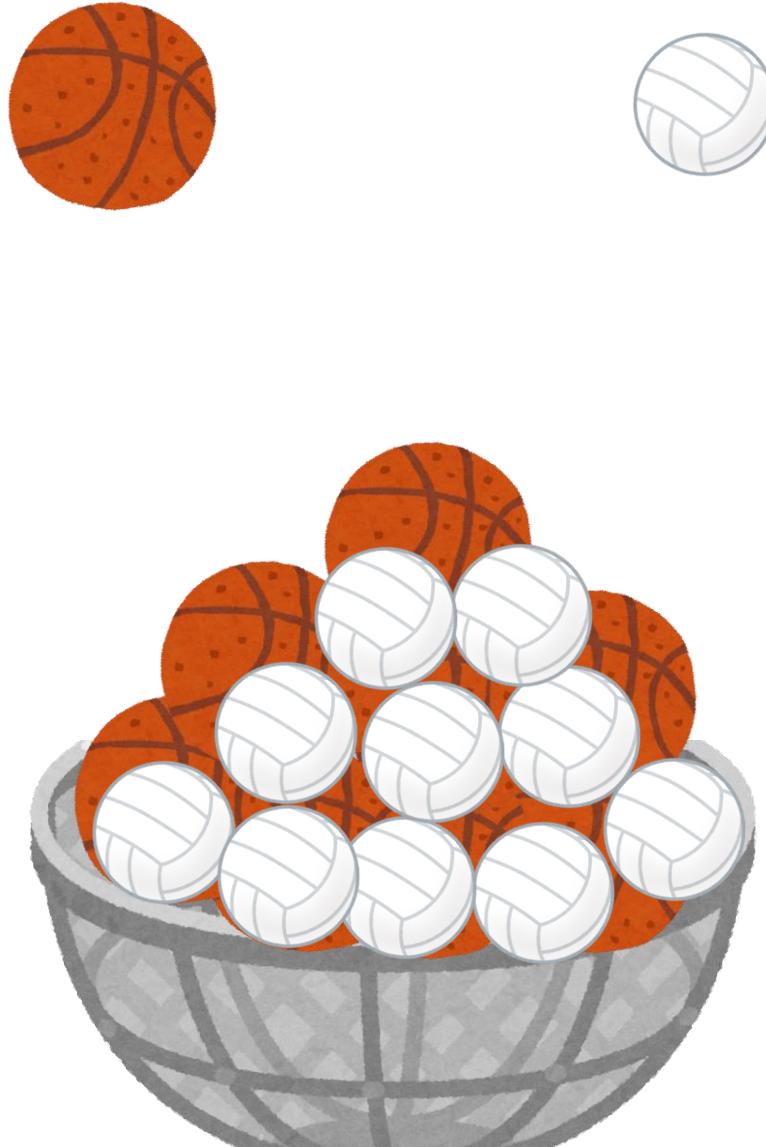
User Address

A
2
SA
D

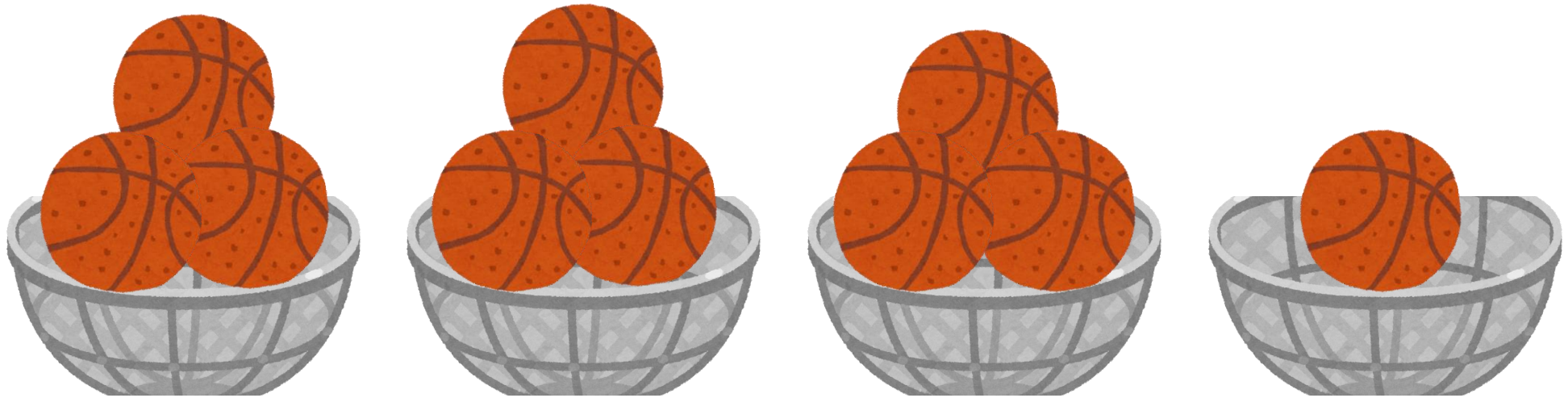
☐ ROW BANK COLUMN

☒ BANK ROW COLUMN

Burst



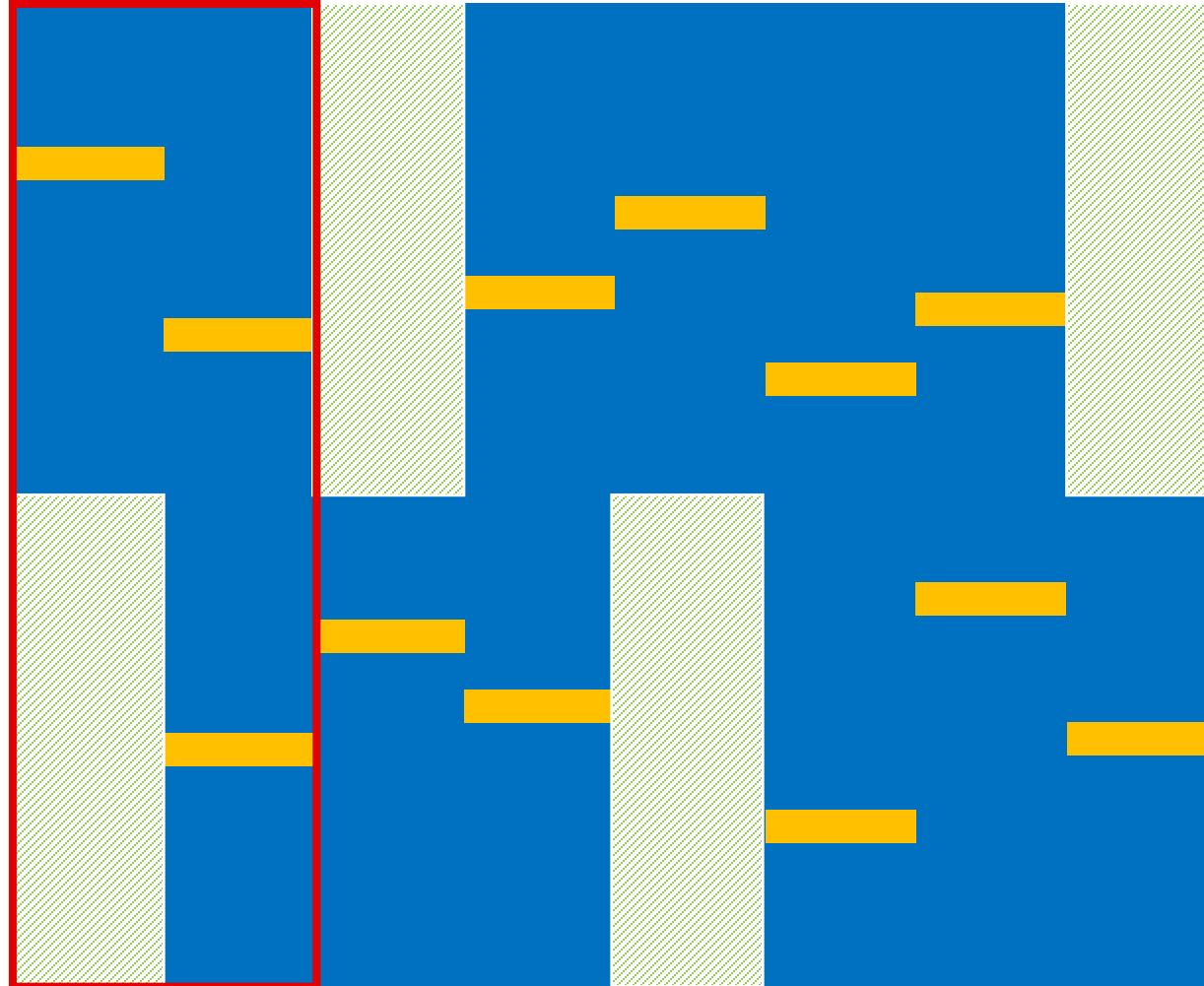
Interleaved



Sequential



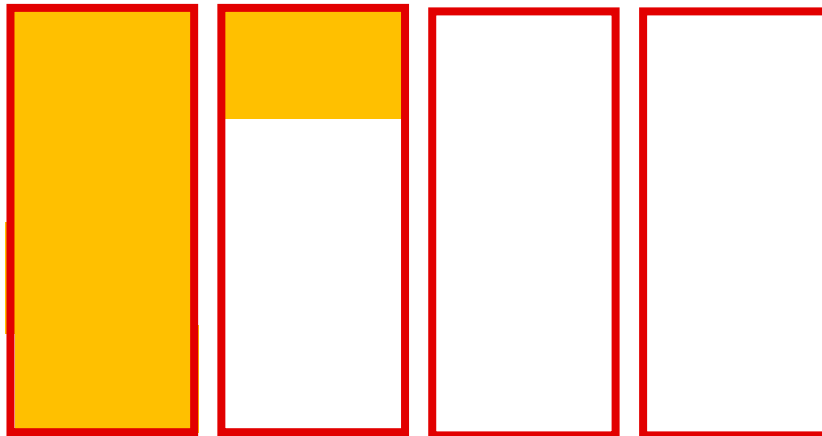
Bank



Memory Address Mapping

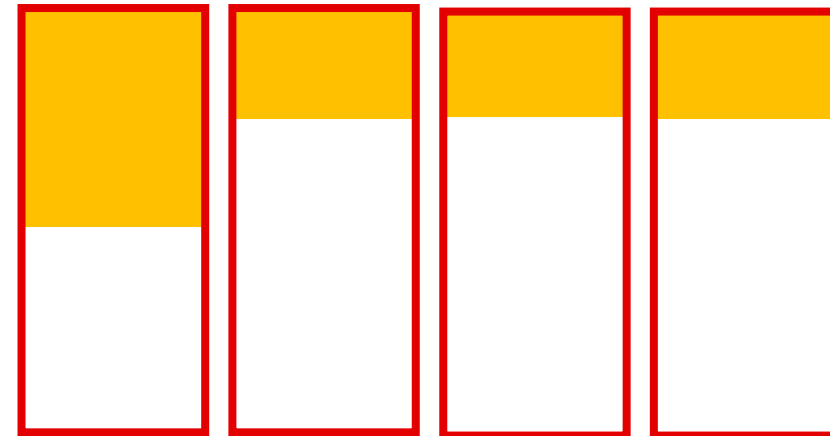
BANK	ROW	COLUMN
------	-----	--------

00	00
01	01
10	10
11	11



ROW	BANK	COLUMN
-----	------	--------

00	00
01	01
10	10
11	11



FPGA Option

System Clock

Choose the desired input clock configuration. Design clock can be Differential or Single-Ended.

System Clock Differential

Reference Clock

Choose the desired reference clock configuration. Reference clock can be Differential or Single-Ended.

Reference Clock Differential

System Reset Polarity

Choose the desired System Reset Polarity.

System Reset Polarity ACTIVE LOW

Debug Signals Control

This feature allows various debug signals present in the IP to be monitored on the ChipScope tool. The debug signals include status signals of various PHY calibration stages. Enabling this feature will connect all the debug signals to the ChipScope ILA and VIO cores in the example design top module. A part of each bus in the debug interface has been grounded so that users can replace the grounded signals with the required signals.

Debug Signals for Memory Controller OFF

Sample Data Depth

This selects the value of Sample Data depth for Chipscope ILA used in Debug logic.

Sample Data Depth 1024

Internal Vref

Internal Vref can be used to allow the use of the Vref pins as normal IO pins. This option can only be used at 800 Mbps and lower data rates. This can free 2 pins per bank where inputs are used. This setting has no effect on banks with only outputs.

Internal Vref ☐

IO Power Reduction

Significantly reduces average IO power by automatically disabling DQ/DQS IBUFs and internal terminations during WRITES and periods of inactivity

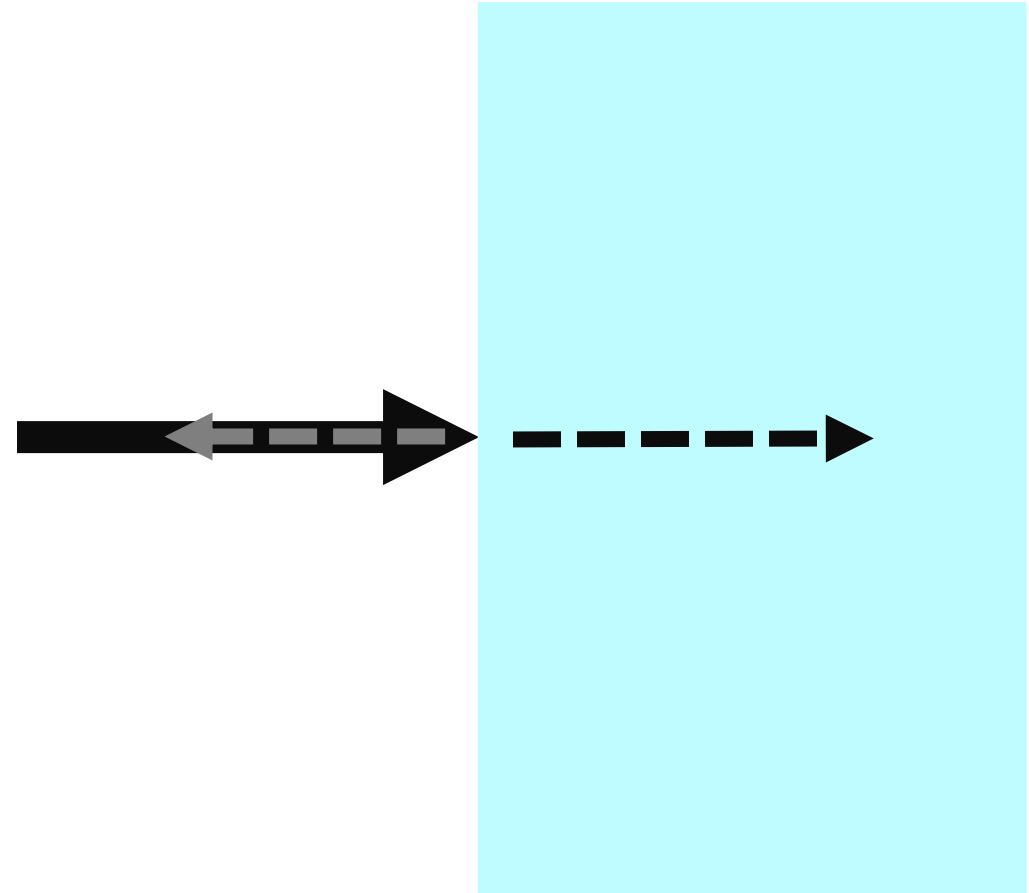
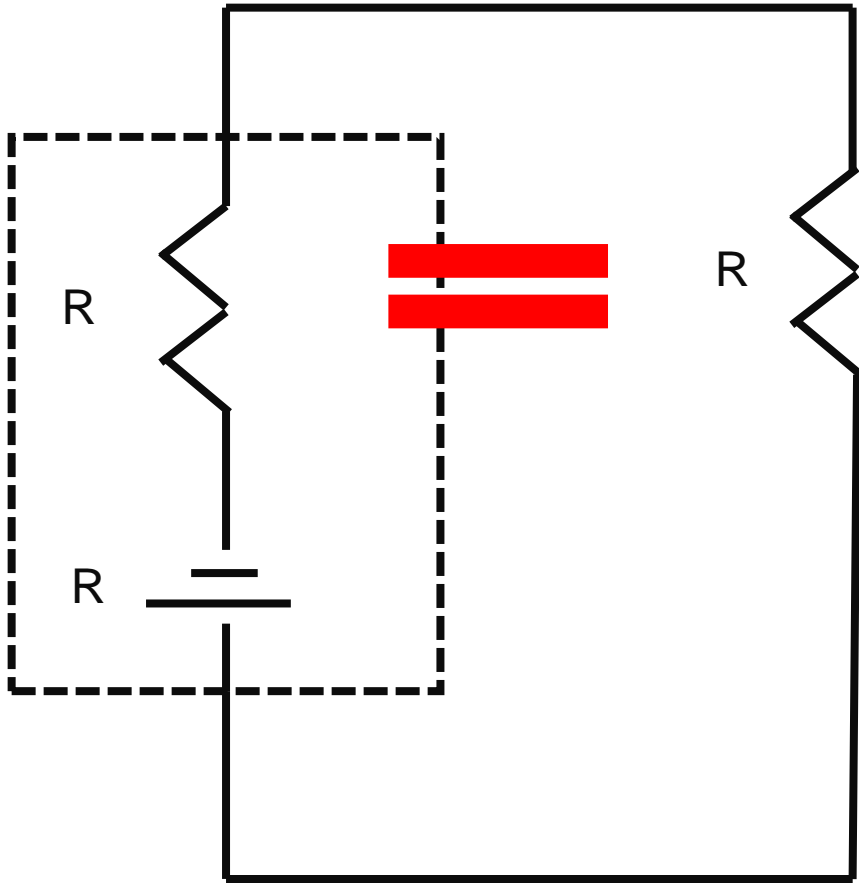
IO Power Reduction ON

XADC Instantiation

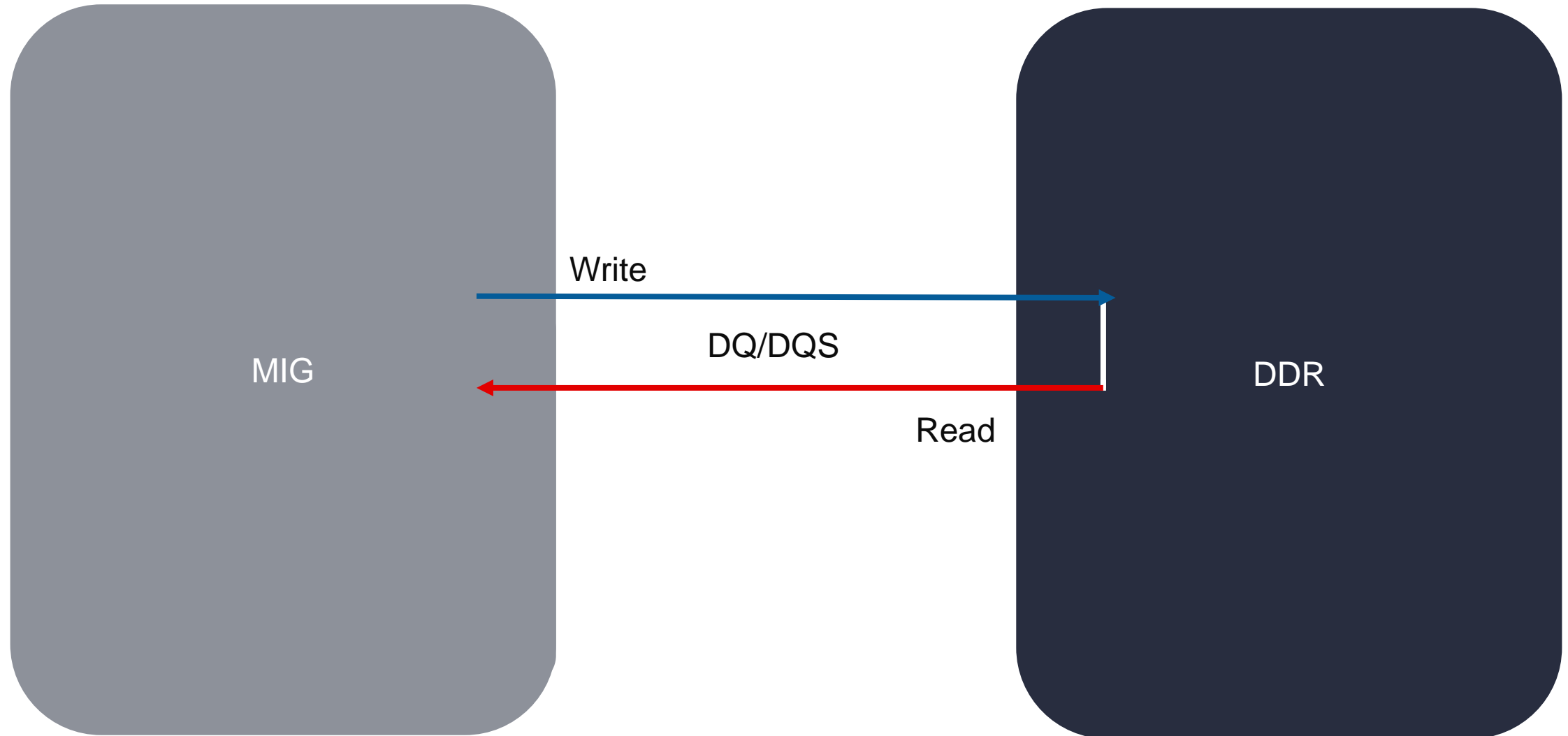
The memory interface uses the temperature reading from the XADC block to perform temperature compensation and keep the read DQS centered in the data window. There is one XADC block per device. If the XADC is not currently used anywhere in the design, enable this option to have the block instantiated. If the XADC is already used, disable this MIG option. The user is then required to provide the temperature value to the top level 12-bit device_temp_i input port. Refer to Answer Record 51687 or the UG586 for detailed information.

XADC Instantiation Enabled

Impedance matching



IO Power Reduction



FPGA Option

DDR3 SDRAM

Digitally Controlled Impedance (DCI)

The DCI (Digitally Controlled Impedance) I/O standards are applied appropriately in High Performance banks. DQ and DQS/DQS# signals utilize DCI standards (SSTL15_T_DCI for DQ's and DIFF_SSTL15_T_DCI for DQS and DQS#). DCI is not used for the Address/Control output signals. Consult the User Guide for more information and use IBIS simulation to determine the best termination strategy.

DCI Cascading Information

Select the DCI Cascade for the DCI reference pins to achieve better pin efficiency. The constraint file must be updated manually to select the Master/Slave banks.

DCI Cascade ☐

Internal Termination for High Range Banks

Select the internal termination (IN_TERM) impedance for the High Range (HR) banks. This setting applies **only** to the HR banks used in the interface.

Internal Termination Impedance

50 Ohms

Pin/Bank Selection Mode

- ☐ New Design: Pick the optimum banks for a new design
- ☒ Fixed Pin Out: Pre-existing pin out is known and fixed

Bank and Source

Bank Selection For Controller 0 - DDR3 SDRAM

Select the byte groups for the data and address/control in the architectural view below. Data and Address within 3 vertical banks. The interface cannot span horizontally. *Bank(s) 14,15 contain configuration of these banks for default configurations. If bank(s) 14,15 is selected for your memory controller ensure no conflicts with the configuration pin. For more information see [UG586 Bank and Pin rules](#). The Address/Control byte groups must be selected in the middle bank in interfaces using 3 banks. Bank selection may be restricted to High Performance interface data rate selected.

Address/Control : 25/25 Data : 11/11

Bank 14	Signal Sets	Bank 34	Signal Sets
Byte Group T0	Unassigned	Byte Group T0	Address/Ctrl-0
Byte Group T1	Unassigned	Byte Group T1	Address/Ctrl-1
Byte Group T2	Unassigned	Byte Group T2	Address/Ctrl-2
Byte Group T3	Unassigned	Byte Group T3	DQ[0-7]
HR Bank		HP Bank	
Bank 13	Signal Sets	Bank 33	Signal Sets
Byte Group T0	Unassigned	Byte Group T0	Unassigned
Byte Group T1	Unassigned	Byte Group T1	Unassigned
Byte Group T2	Unassigned	Byte Group T2	Unassigned
Byte Group T3	Unassigned	Byte Group T3	Unassigned
HR Bank		HP Bank	
Bank 12	Signal Sets	Bank 32	Signal Sets
Byte Group T0	Unassigned	Byte Group T0	Unassigned
Byte Group T1	Unassigned	Byte Group T1	Unassigned
Byte Group T2	Unassigned	Byte Group T2	Unassigned
Byte Group T3	Unassigned	Byte Group T3	Unassigned

System Signals Selection

Select the system pins below appropriately for the interface. Customization of these pins can also be made in the XDC after the design is generated. For more information see [UG586 Bank and Pin rules](#).

System Clock and Reference Clock pin selections will not be visible if the 'No Buffer' option was selected in the FPGA Options page.

System Clock Pin Selection

The `sys_clk` is used as the system clock for the memory interface. This signal should be connected to a low jitter external clock source via a differential (P/N) pair for best performance. This signal should be in the address/control bank, but may be placed in an adjacent bank if there are not enough pins available such as when fitting a 16 bit interface in a single

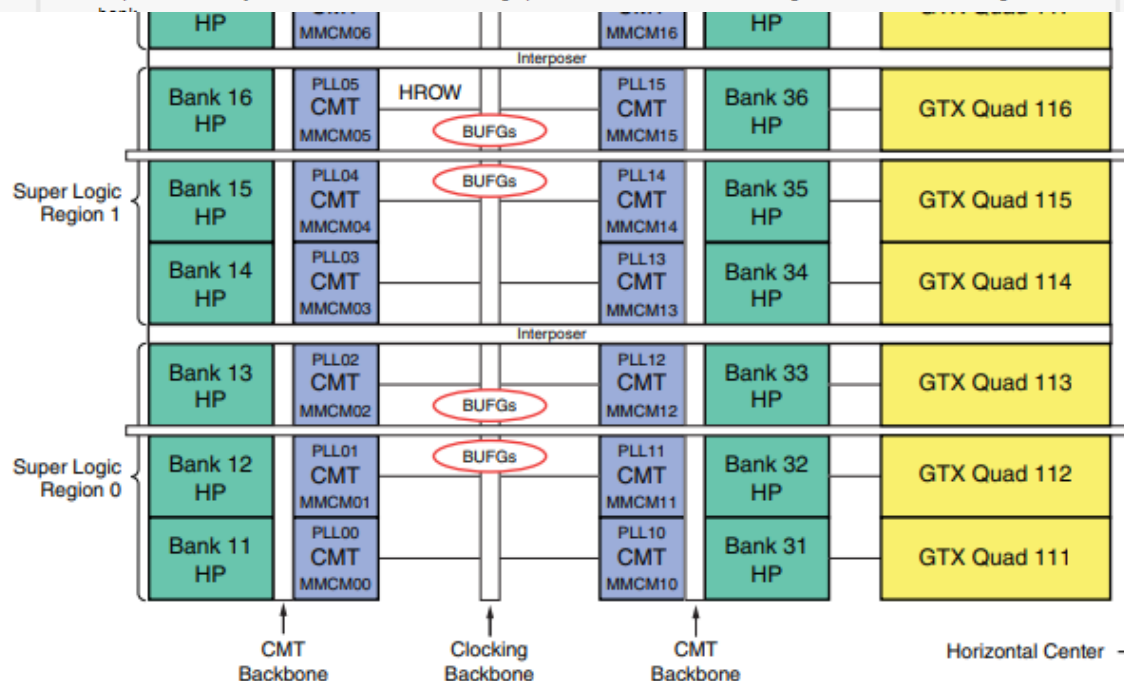


Figure 1-19: XC7V2000T Banks



7Series FPGAs Memory Interface Solution

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7Series FPGAs Memory Interface Solution

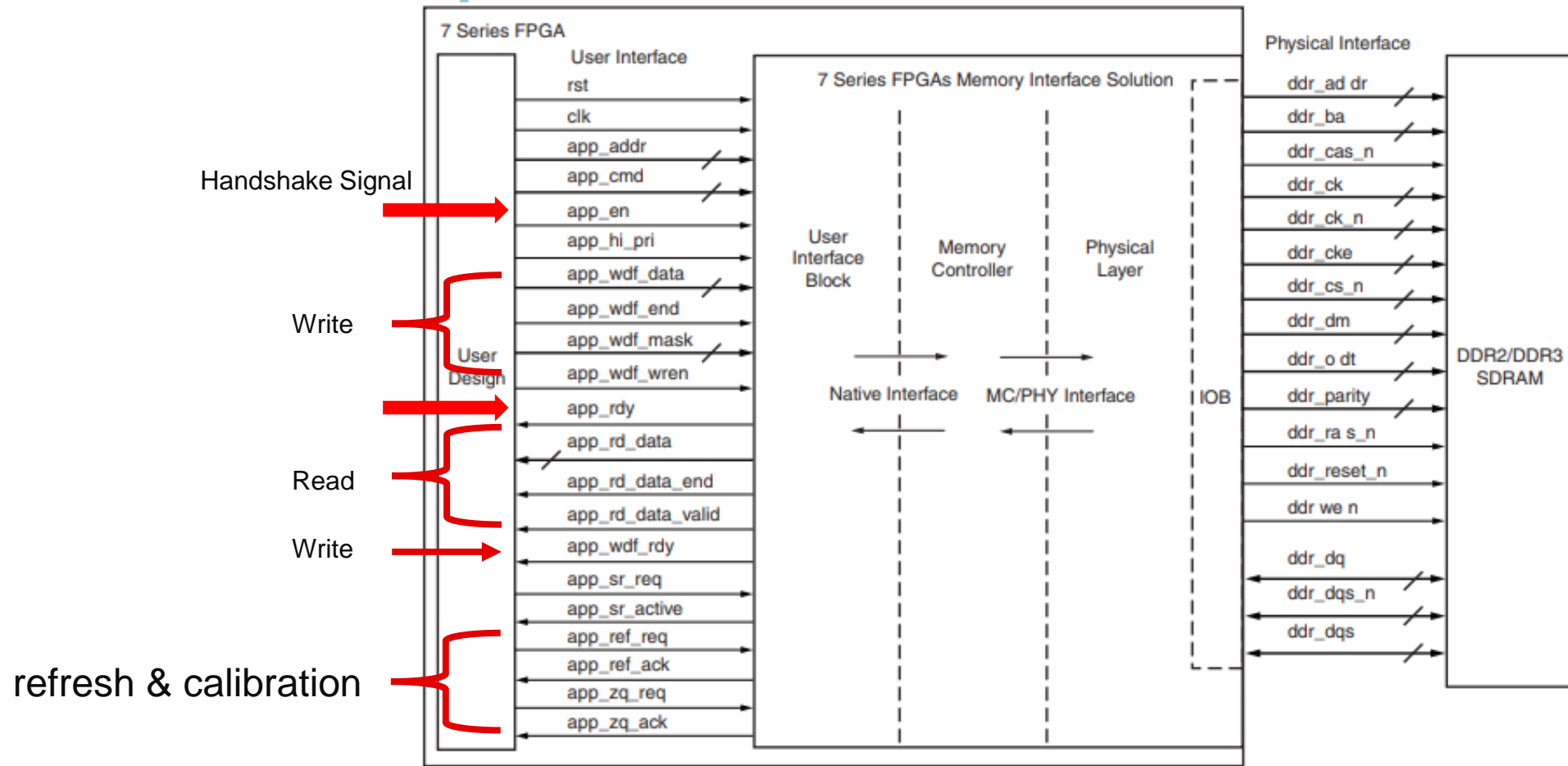
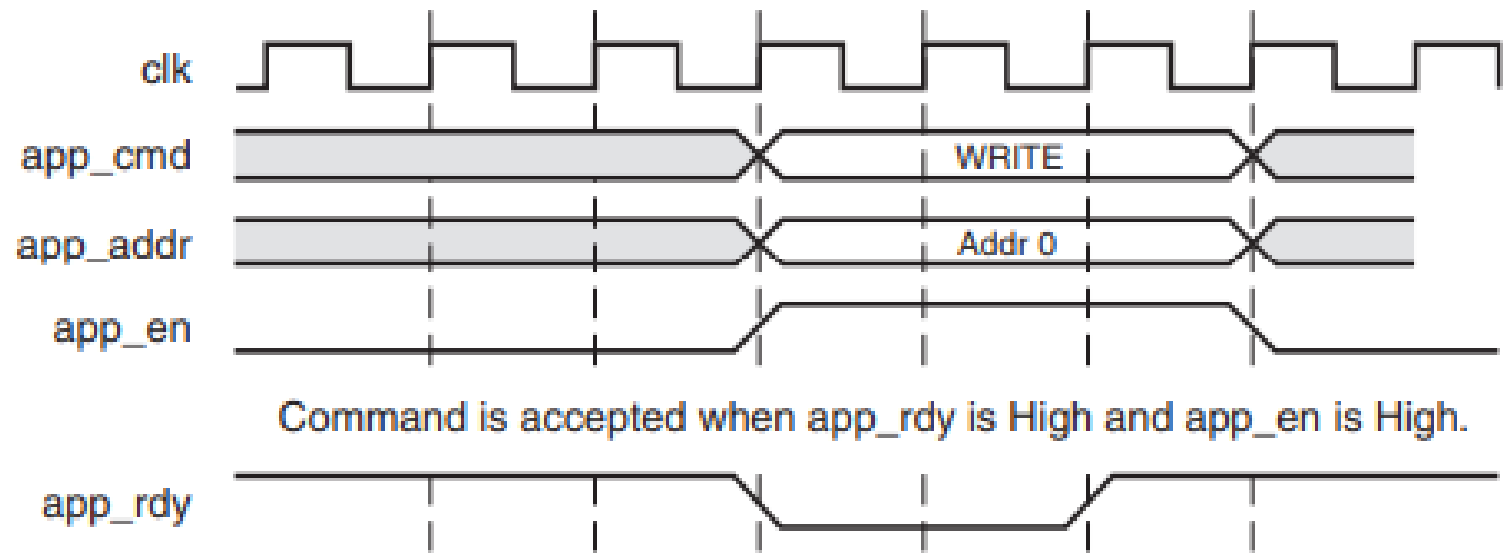


Figure 1-31: 7 Series FPGAs Memory Interface Solution

UG586_c1_43_120311

Command Path



UG586_c1_62_091510

Write Path

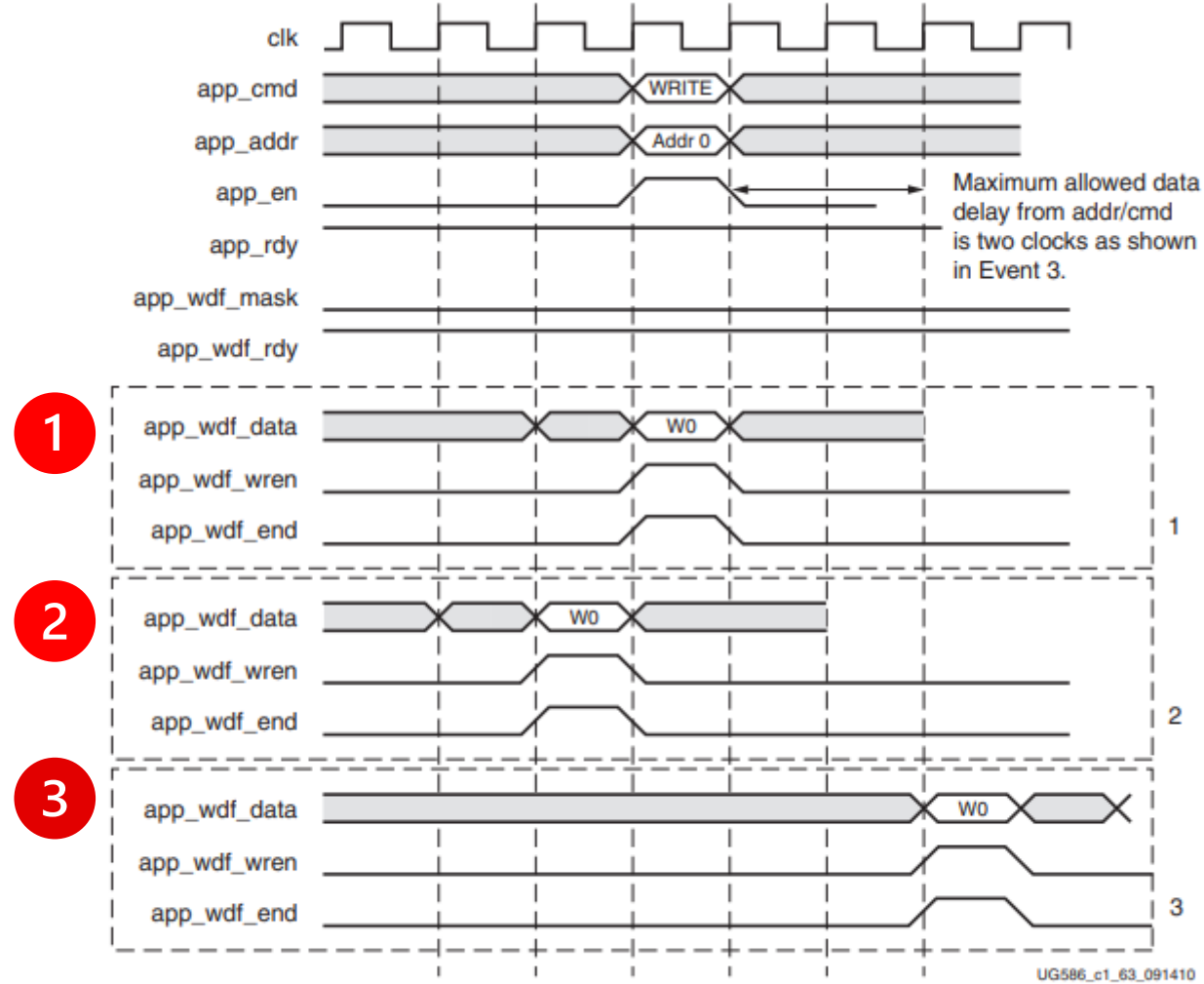
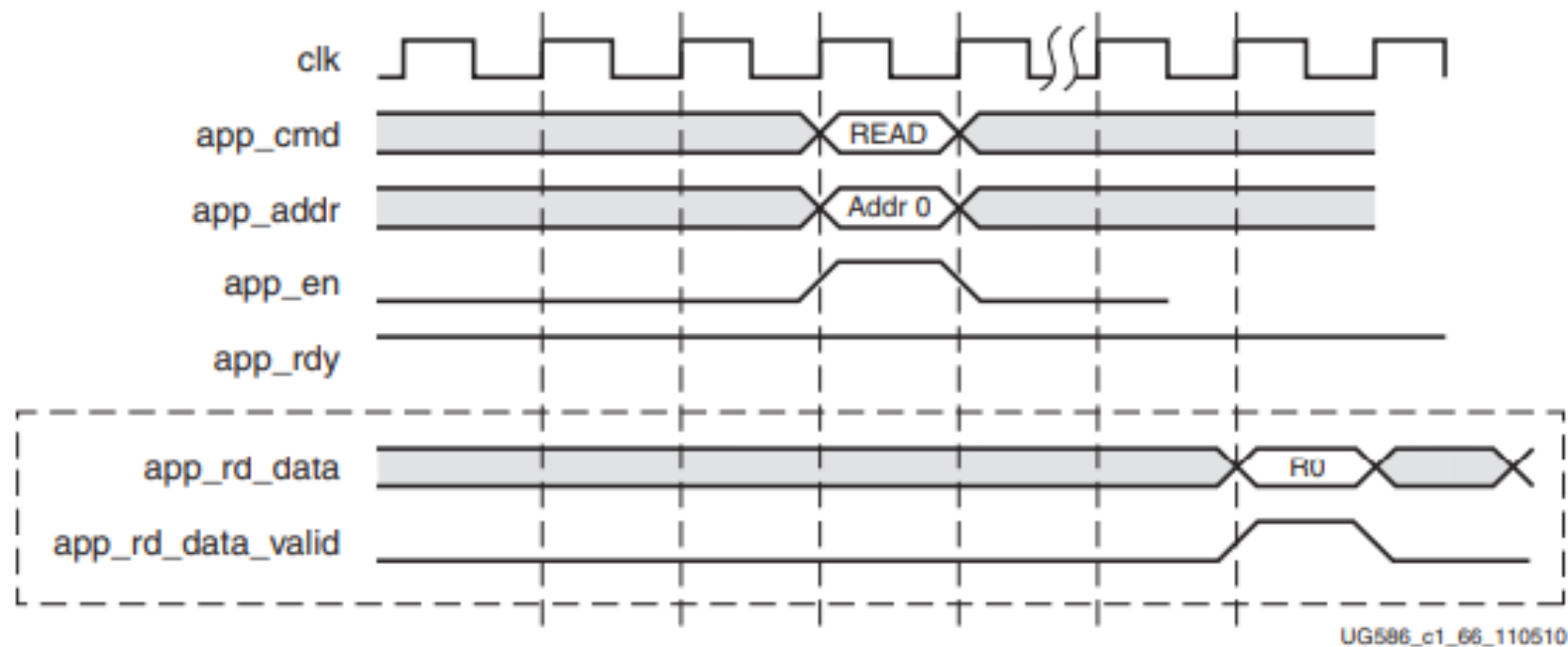


Figure 1-54: 4:1 Mode UI Interface Write Timing Diagram (Memory Burst Type = BL8)

Read Path



**Figure 1-60: 4:1 Mode UI Interface Read Timing Diagram
(Memory Burst Type = BL8)**

User Refresh & User ZQ

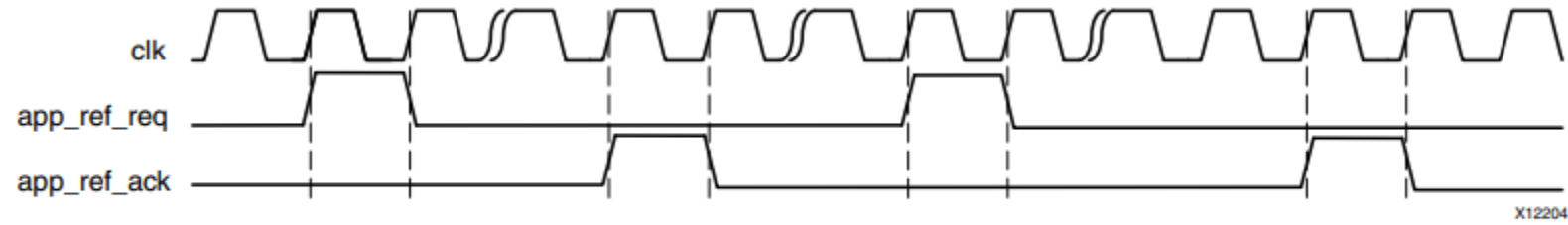


Figure 1-62: User-Refresh Interface

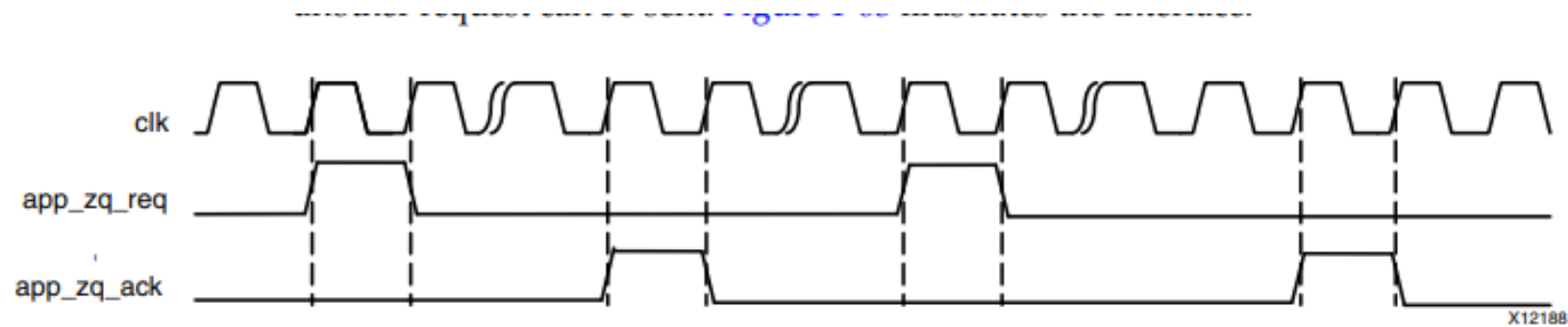


Figure 1-63: User ZQ Interface



Calibration

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Calibration

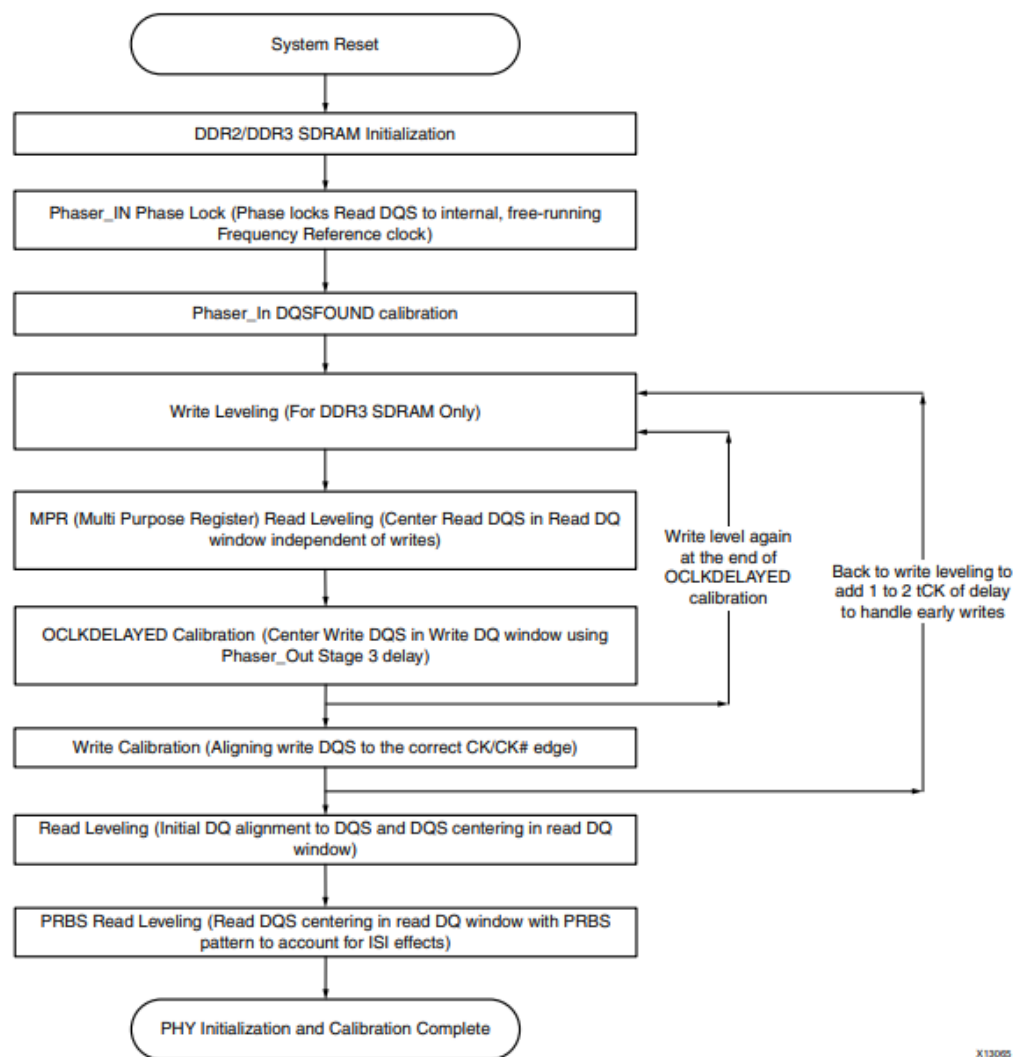
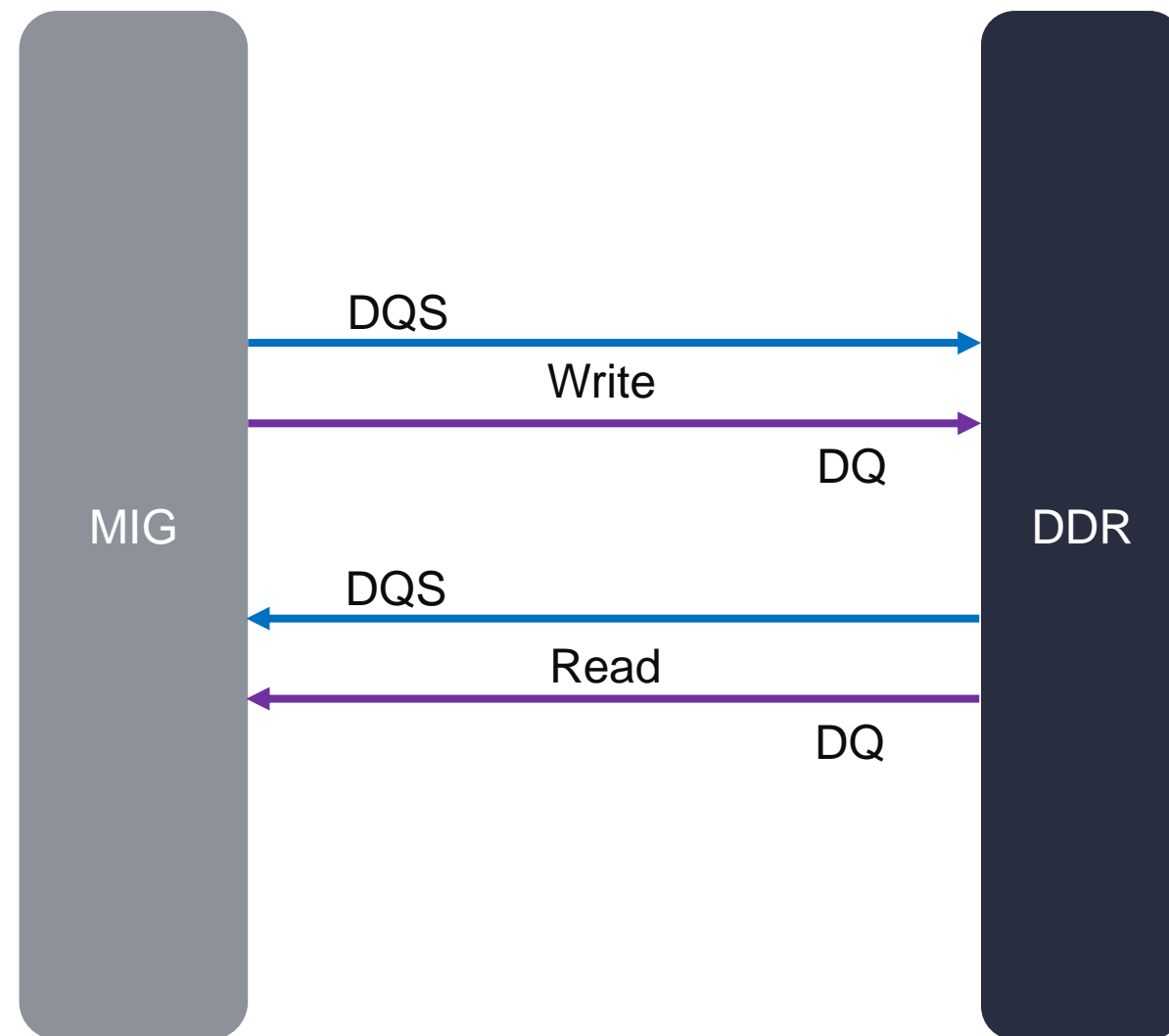
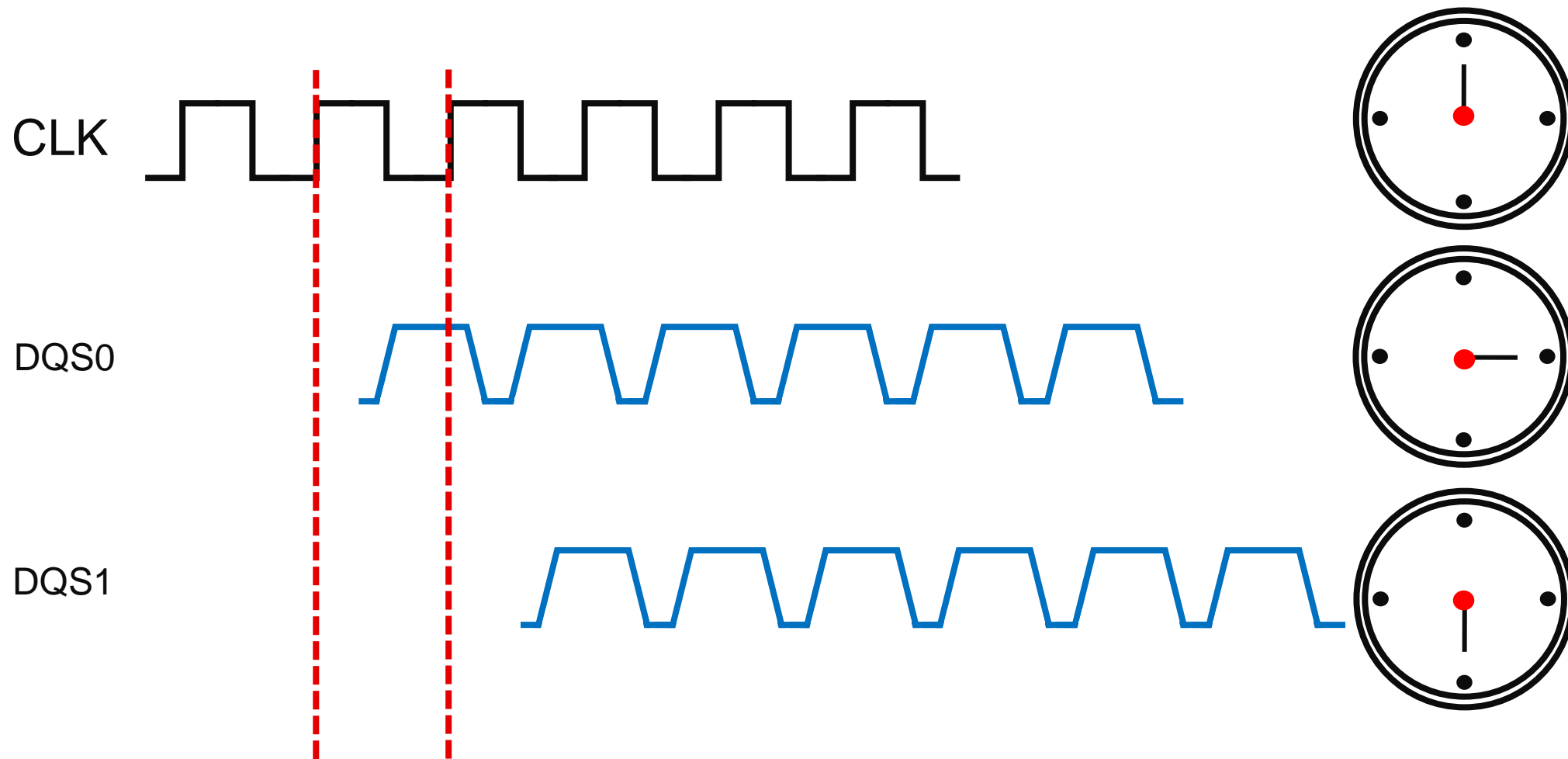


Figure 1-57: PHY Overall Initialization and Calibration Sequence

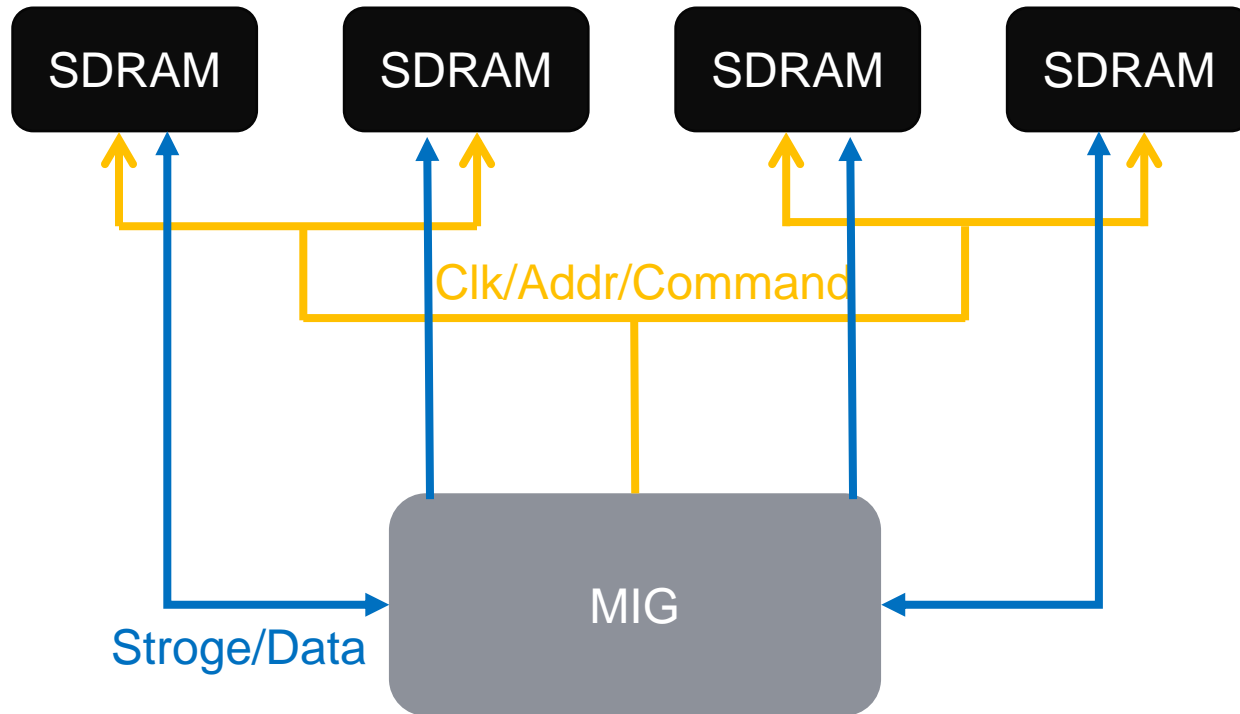


Phaser Lock



Write Leveling

T-topology



Write Leveling

Fly-by

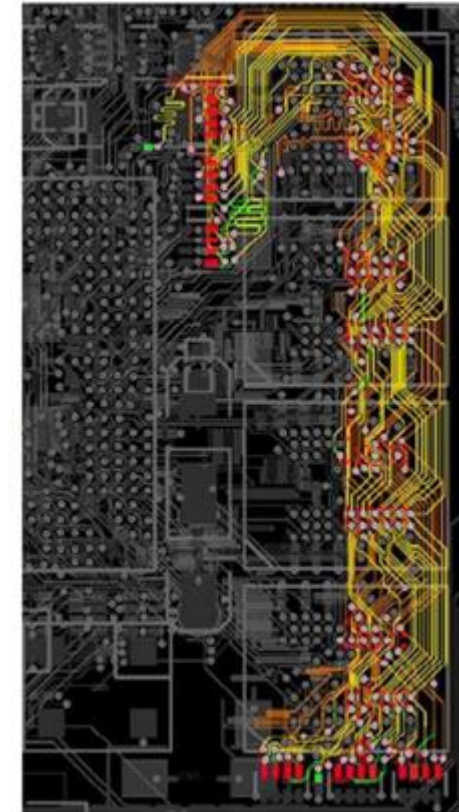


SDRAM

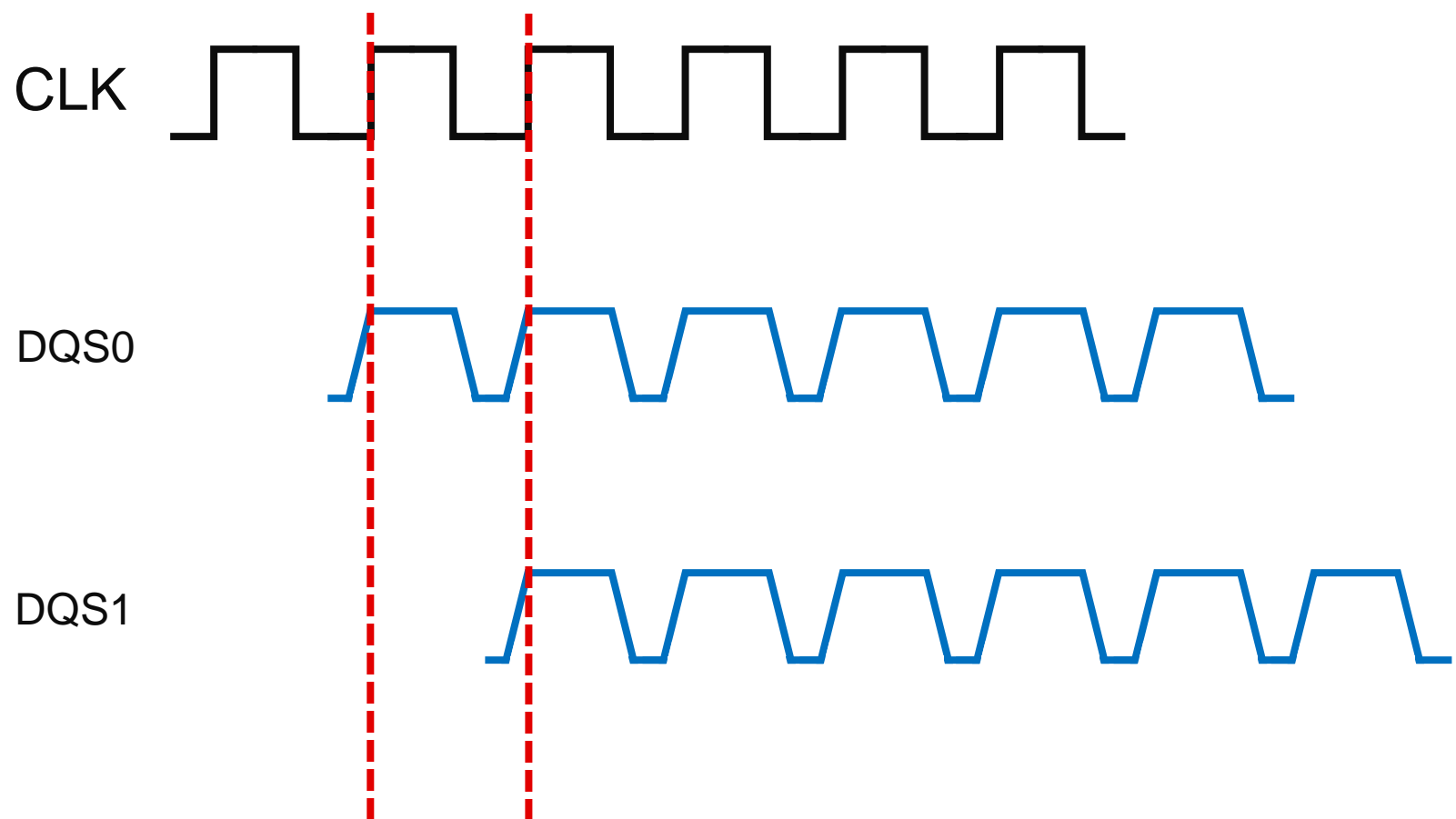
SDRAM

SDRAM

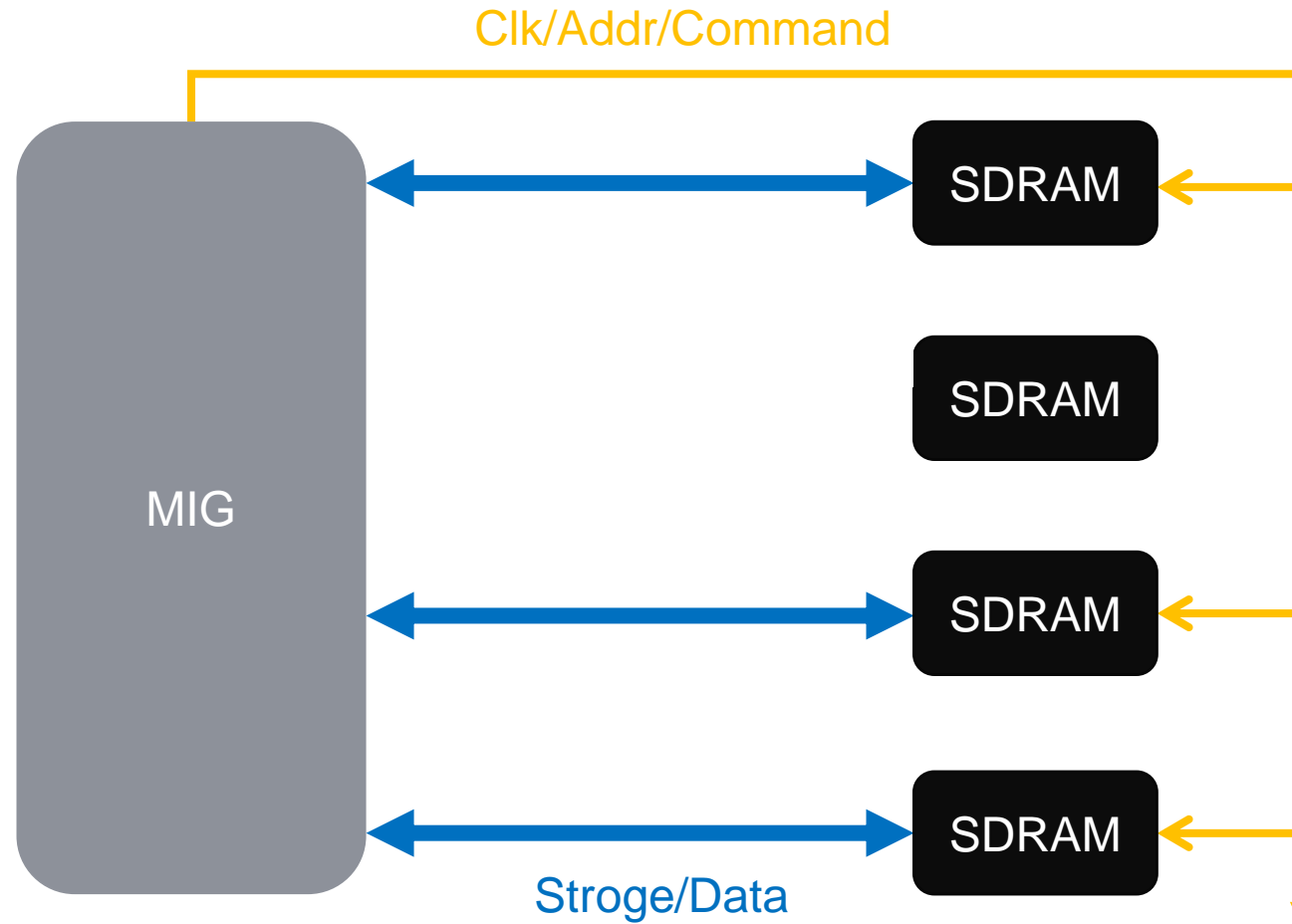
SDRAM



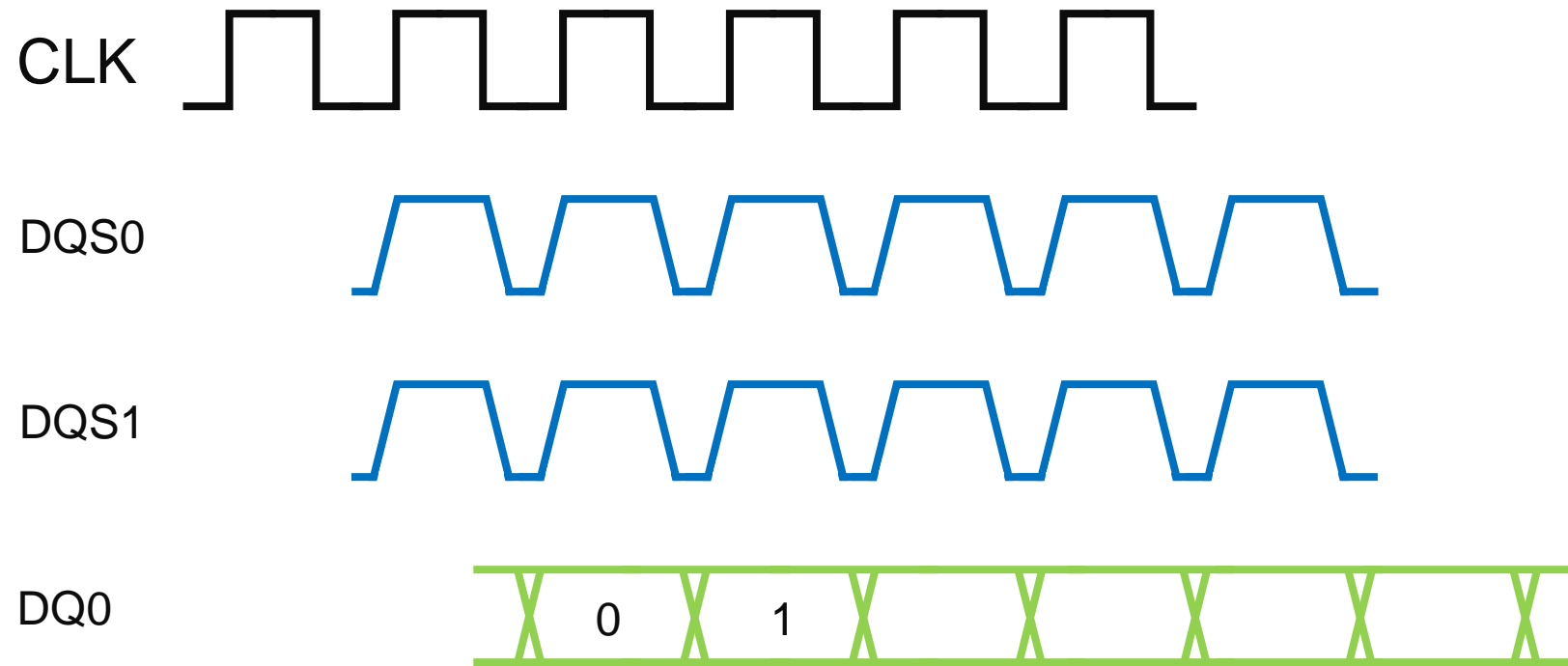
Write Leveling



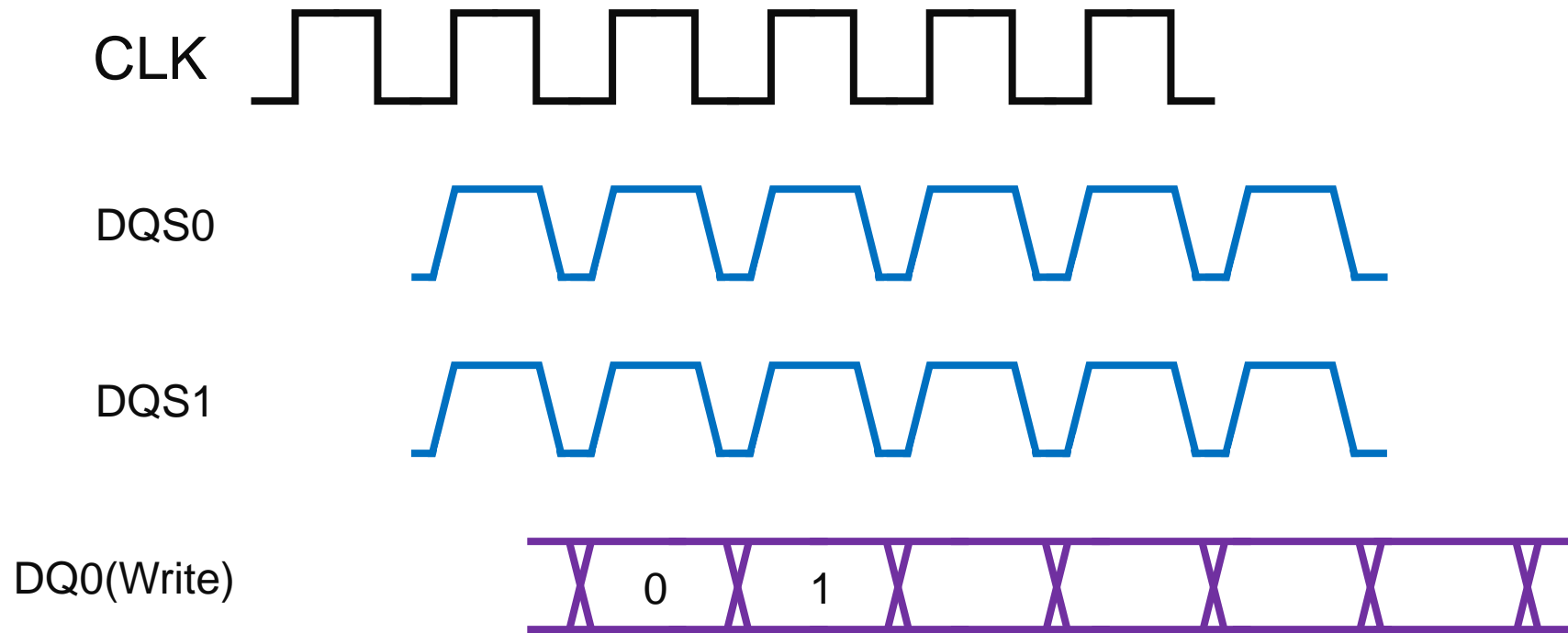
Read Leveling



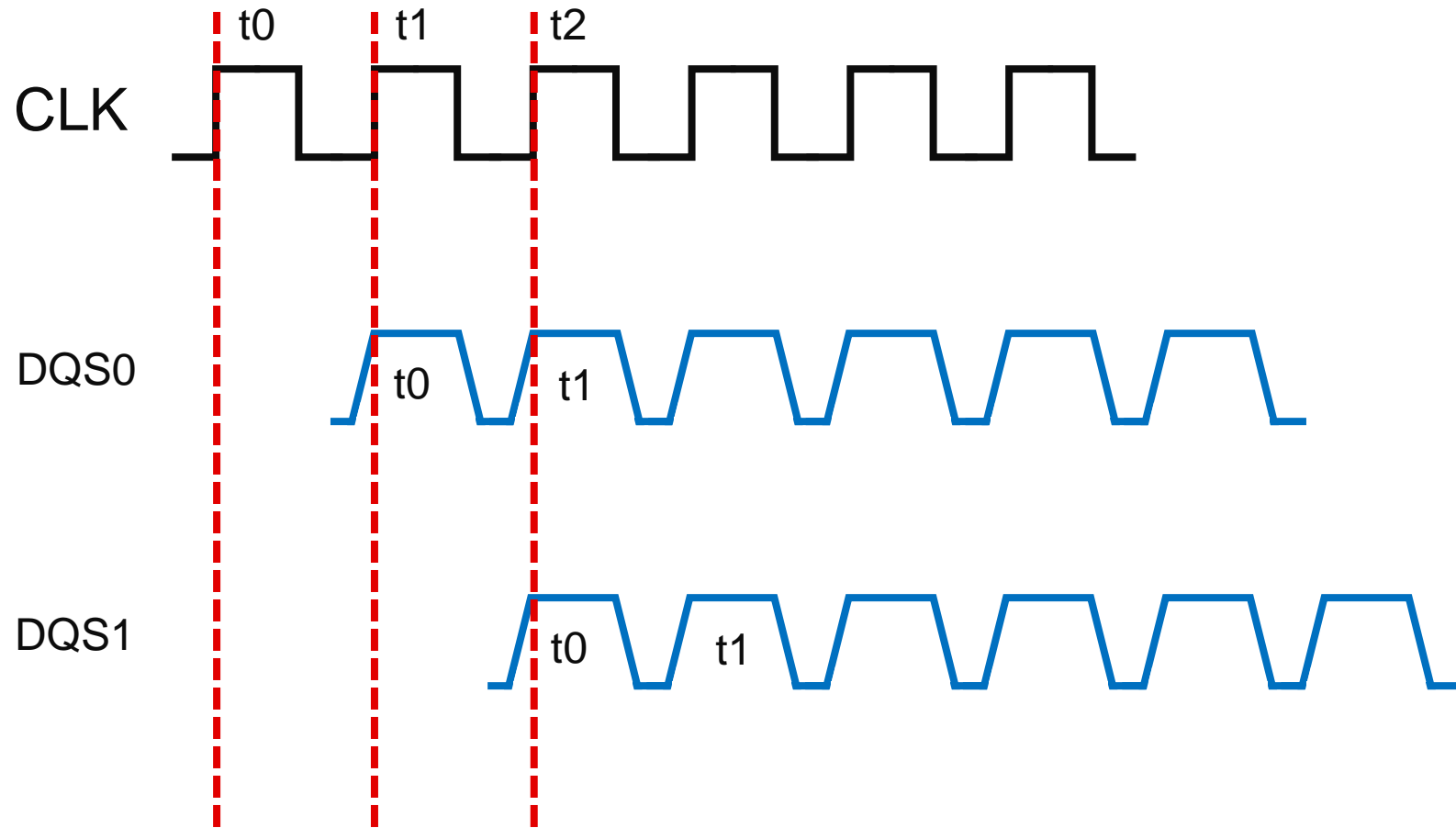
MPR Read Leveling



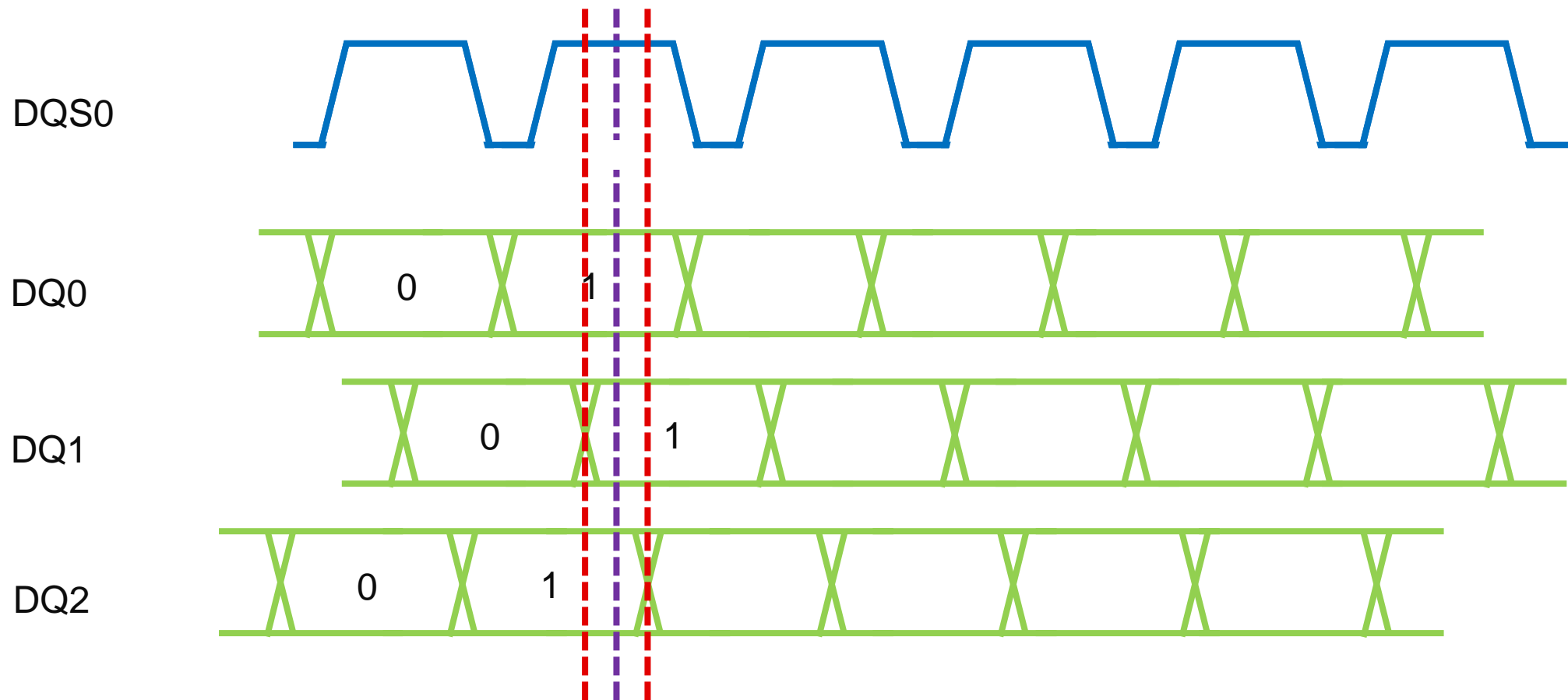
MPR Read Leveling



Write Calibration



Read Leveling & PRBS



Conclusion

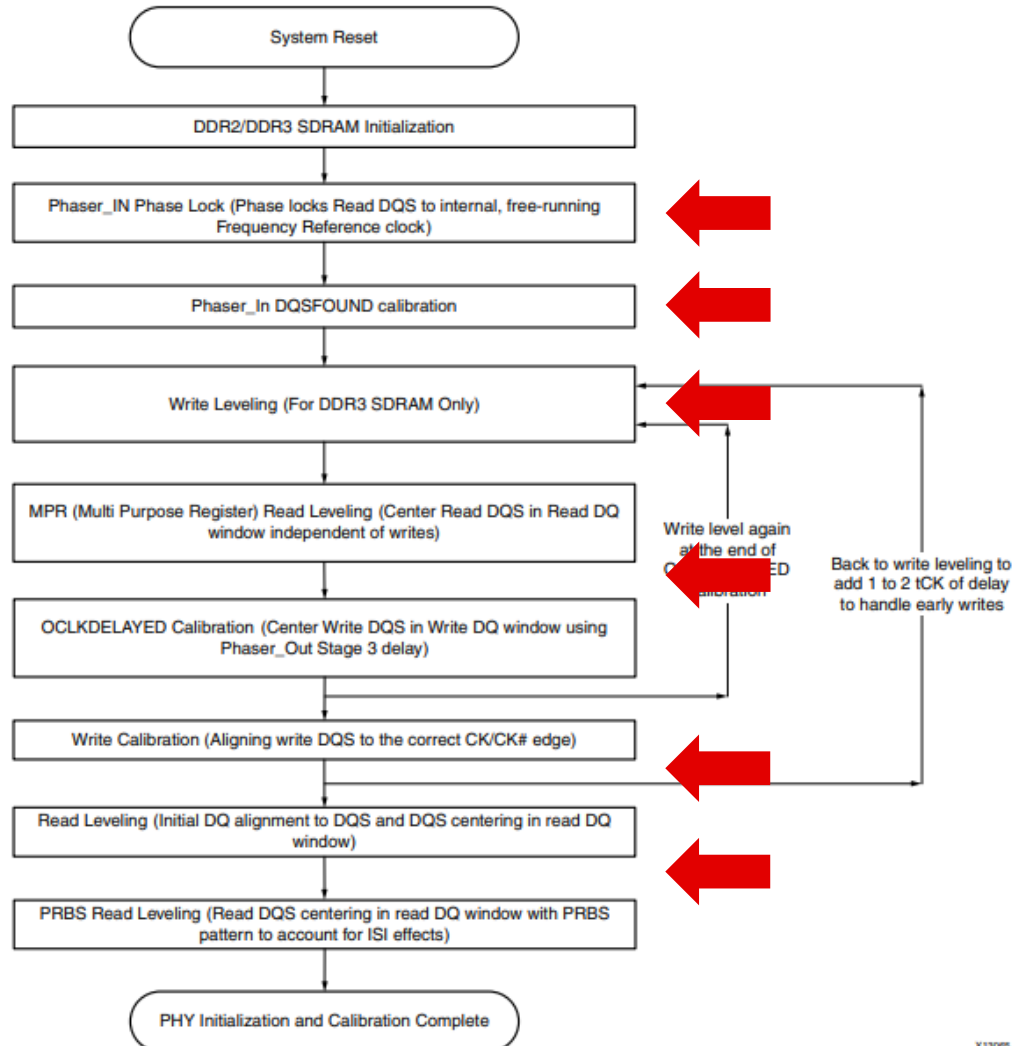
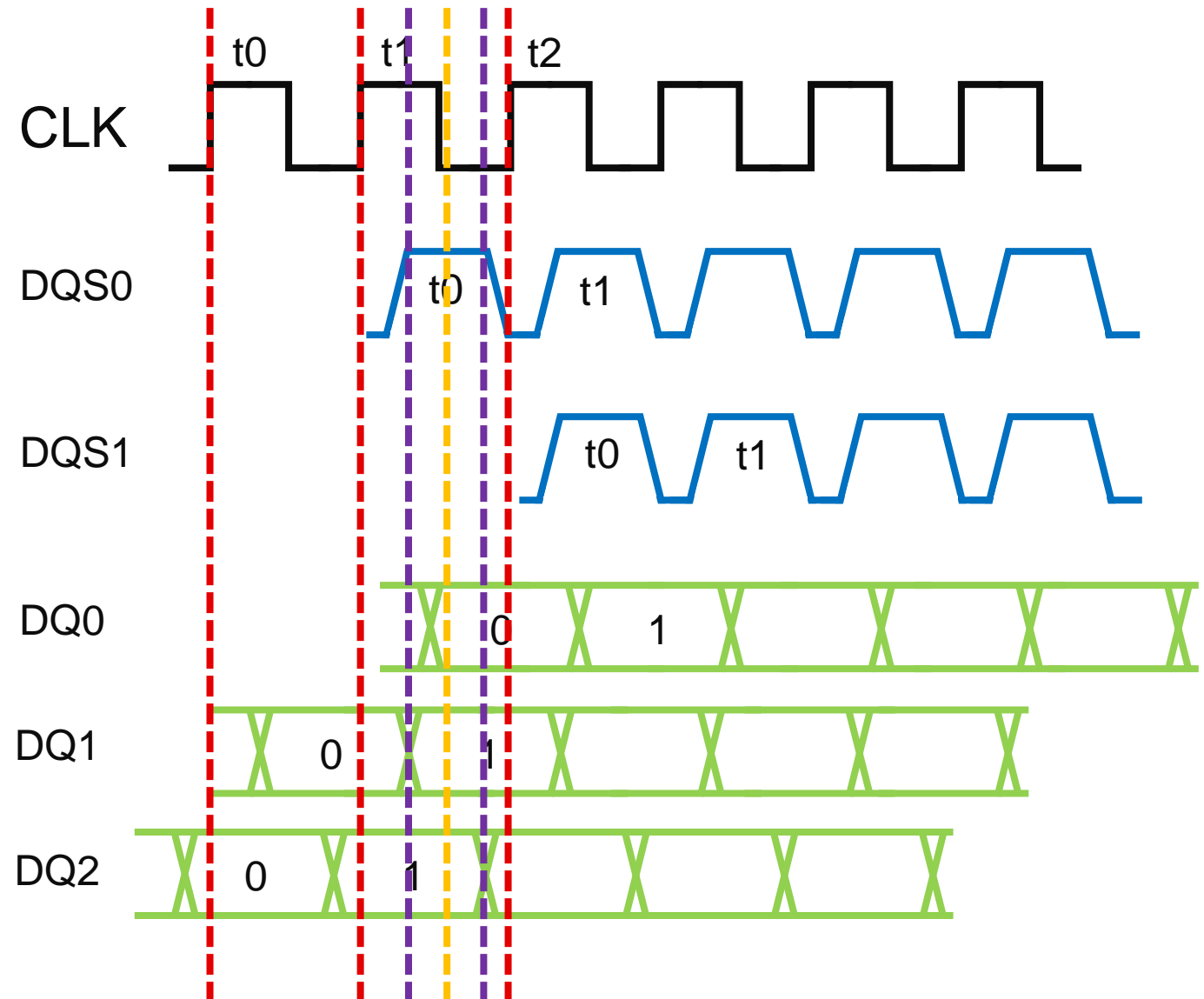


Figure 1-57: PHY Overall Initialization and Calibration Sequence





MIG_Test Lab

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IP Example Design

The screenshot displays the Vivado IP Catalog and the Sources window. The IP Catalog shows a search for "MIG" with 7 matches. The Sources window shows the context menu for the "mig_7series_0" IP.

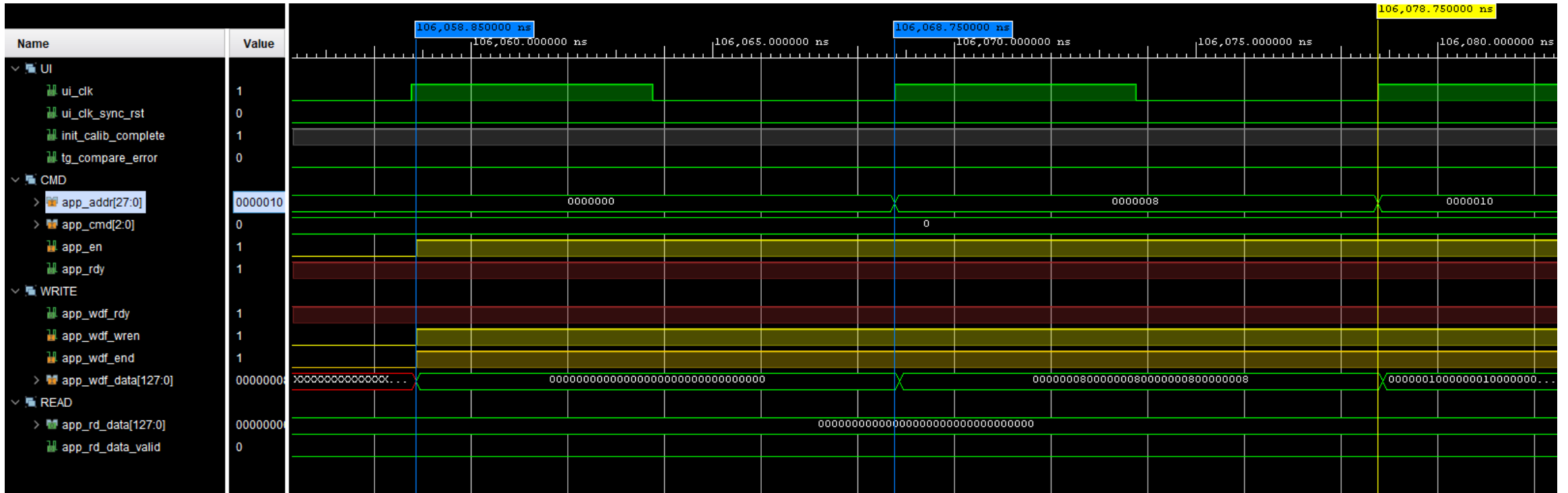
IP Catalog Search Results:

Name	AXI4	Status	License
Vivado Repository			
Memories & Storage Elements			
External Memory Interface			
DDR3 SDRAM (MIG)	AXI4	Not-Supported	Included
DDR4 SDRAM (MIG)	AXI4	Not-Supported	Included
LPDDR3 SDRAM (MIG)		Not-Supported	Included
QDRII+ SRAM (MIG)		Not-Supported	Included
QDRIV SRAM (MIG)		Not-Supported	Included
RLDRAM3 (MIG)		Not-Supported	Included
Memory Interface Generators			
Memory Interface Generator (MIG 7 Series)	AXI4	Production	Included

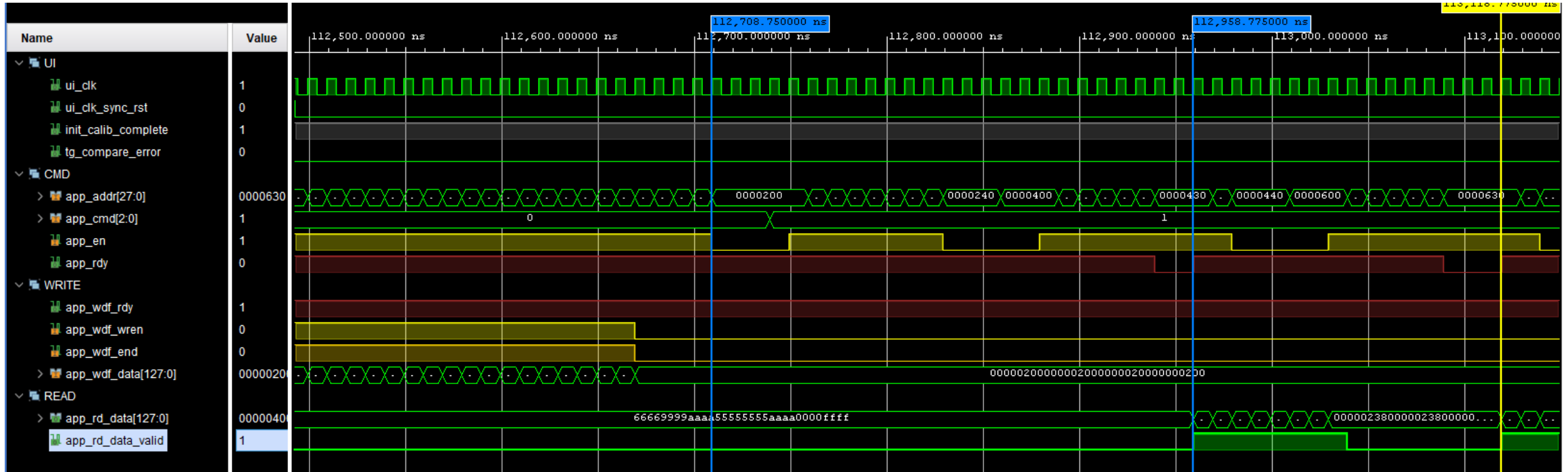
Sources Window Context Menu:

- Source File Properties... (Ctrl+E)
- Re-customize IP...
- Generate Output Products...
- Reset Output Products...
- Upgrade IP...
- Copy IP...
- Open IP Example Design...
- IP Documentation
- Copy Shared Logic into Project...
- Report IP Status
- Replace File...
- Copy File Into Project
- Copy All Files Into Project (Alt+I)
- Remove File from Project... (Delete)
- Enable File (Alt+Equals)
- Disable File (Alt+Minus)
- Set File Type...
- Set Used In...
- Copy Constraints Set...
- Edit Constraints Sets...
- Edit Simulation Sets...
- Add Sources... (Alt+A)

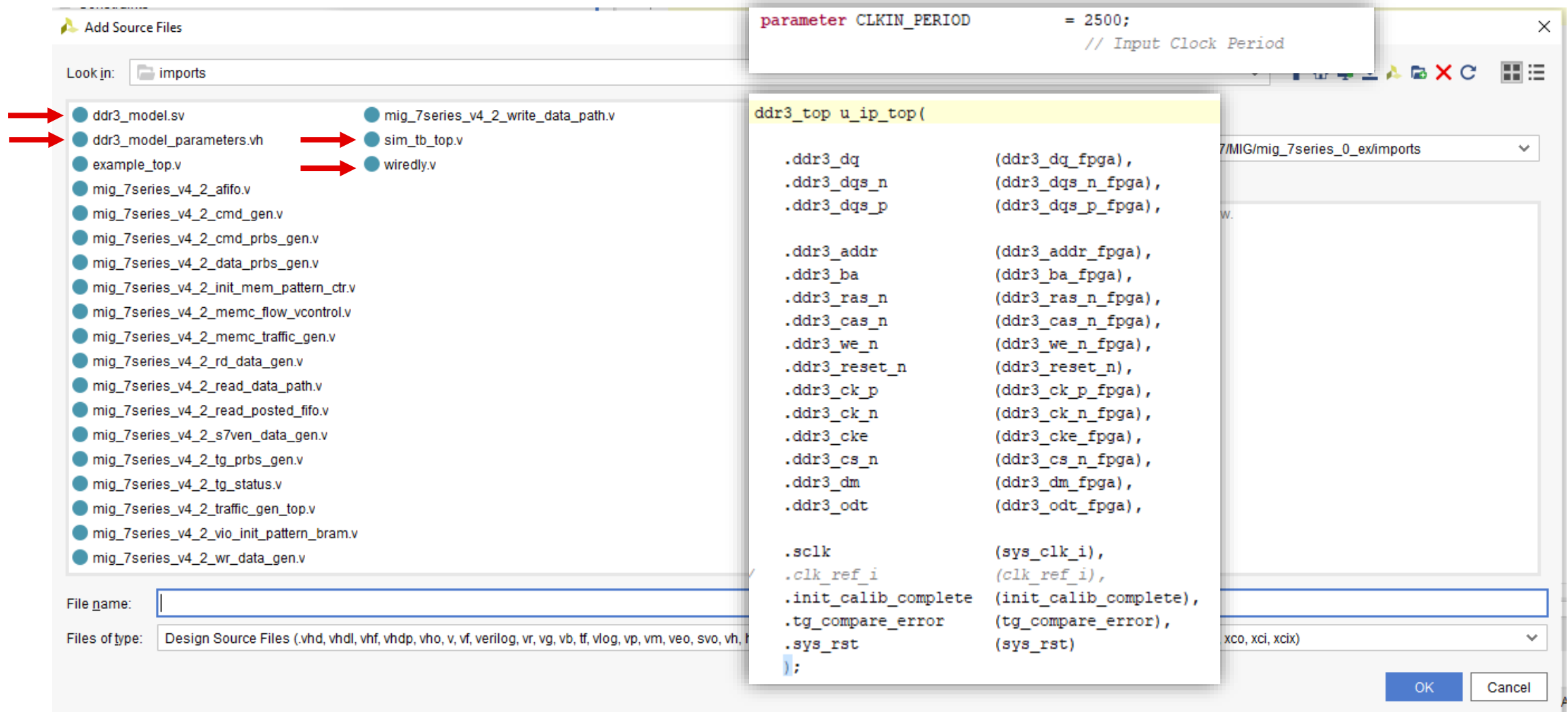
Example Design Simulation



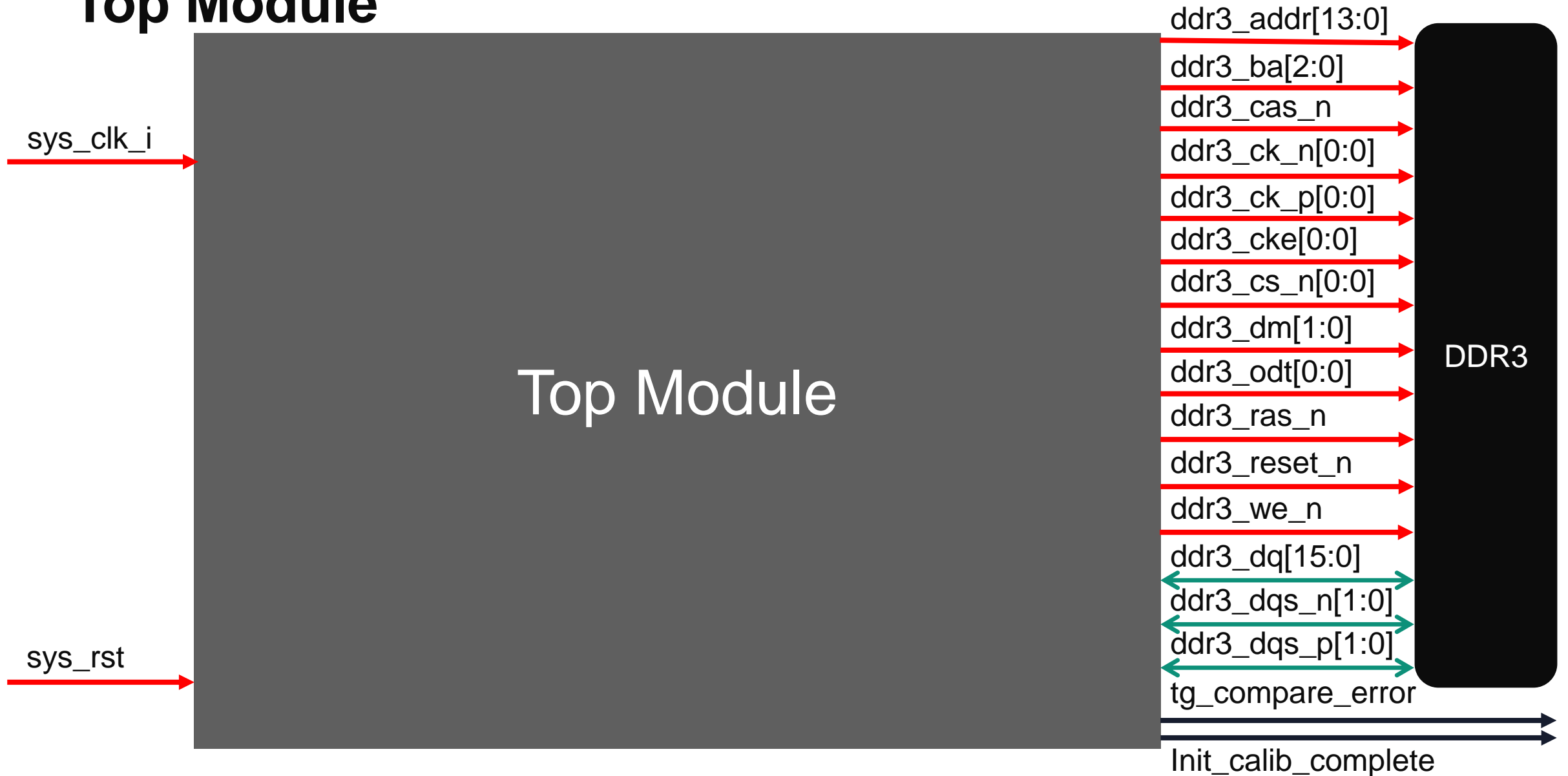
Example Design Simulation



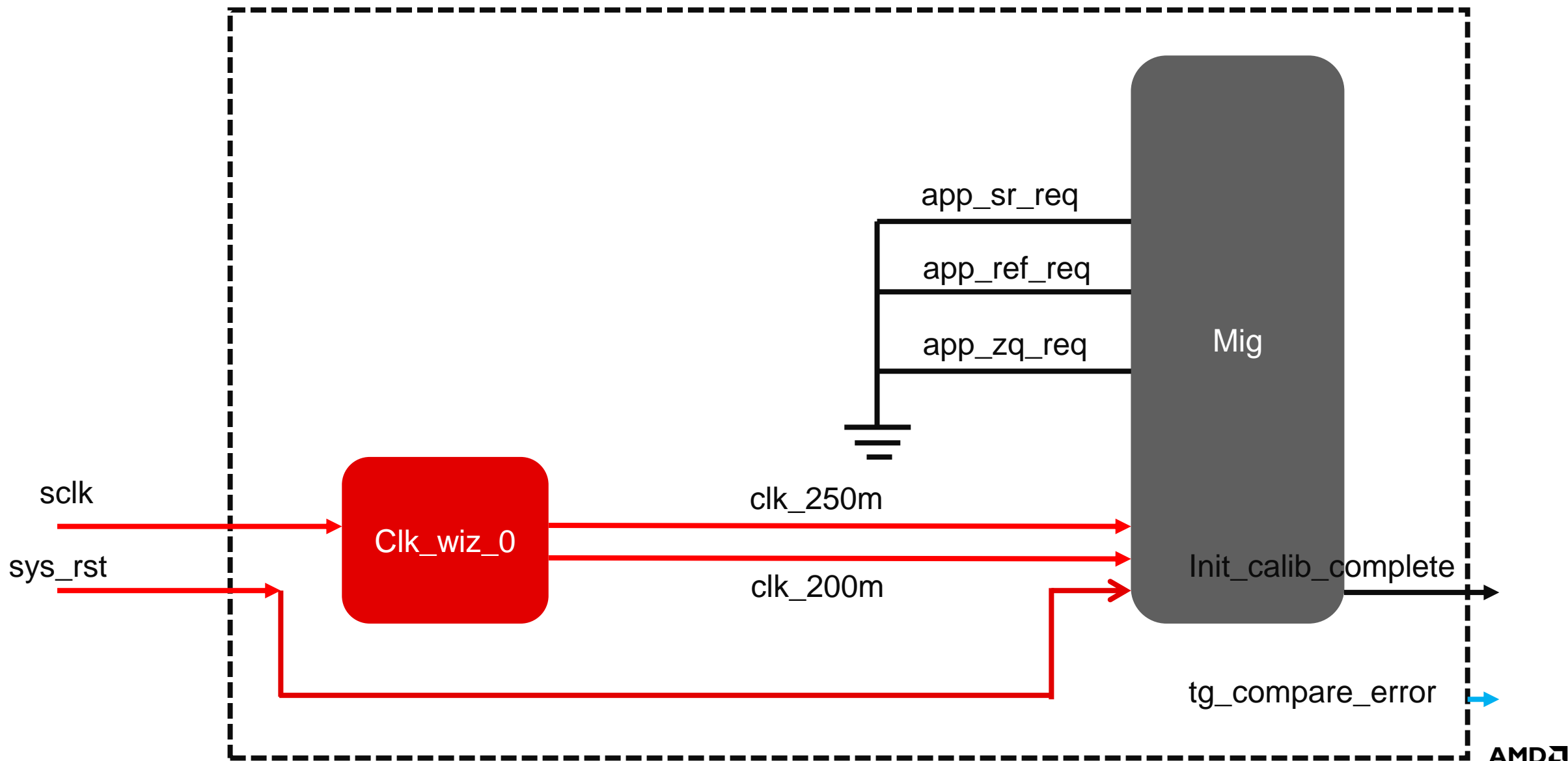
Simulation Setting



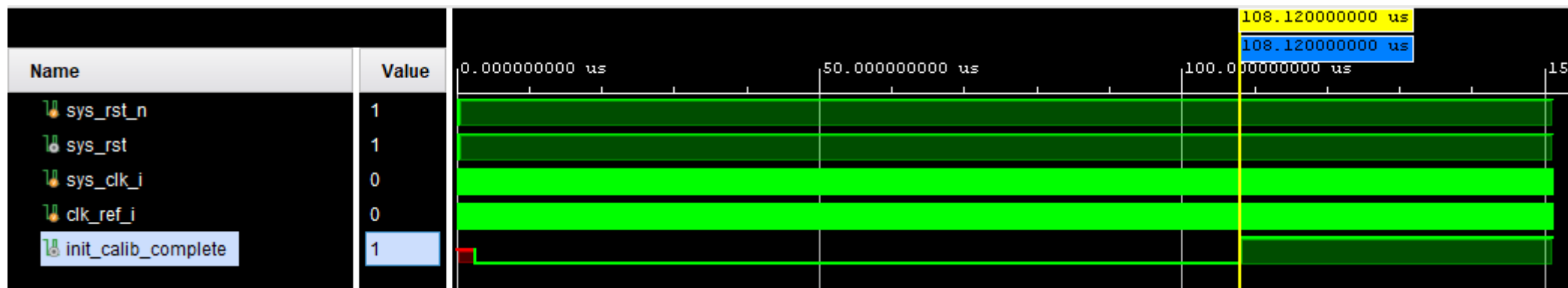
Top Module



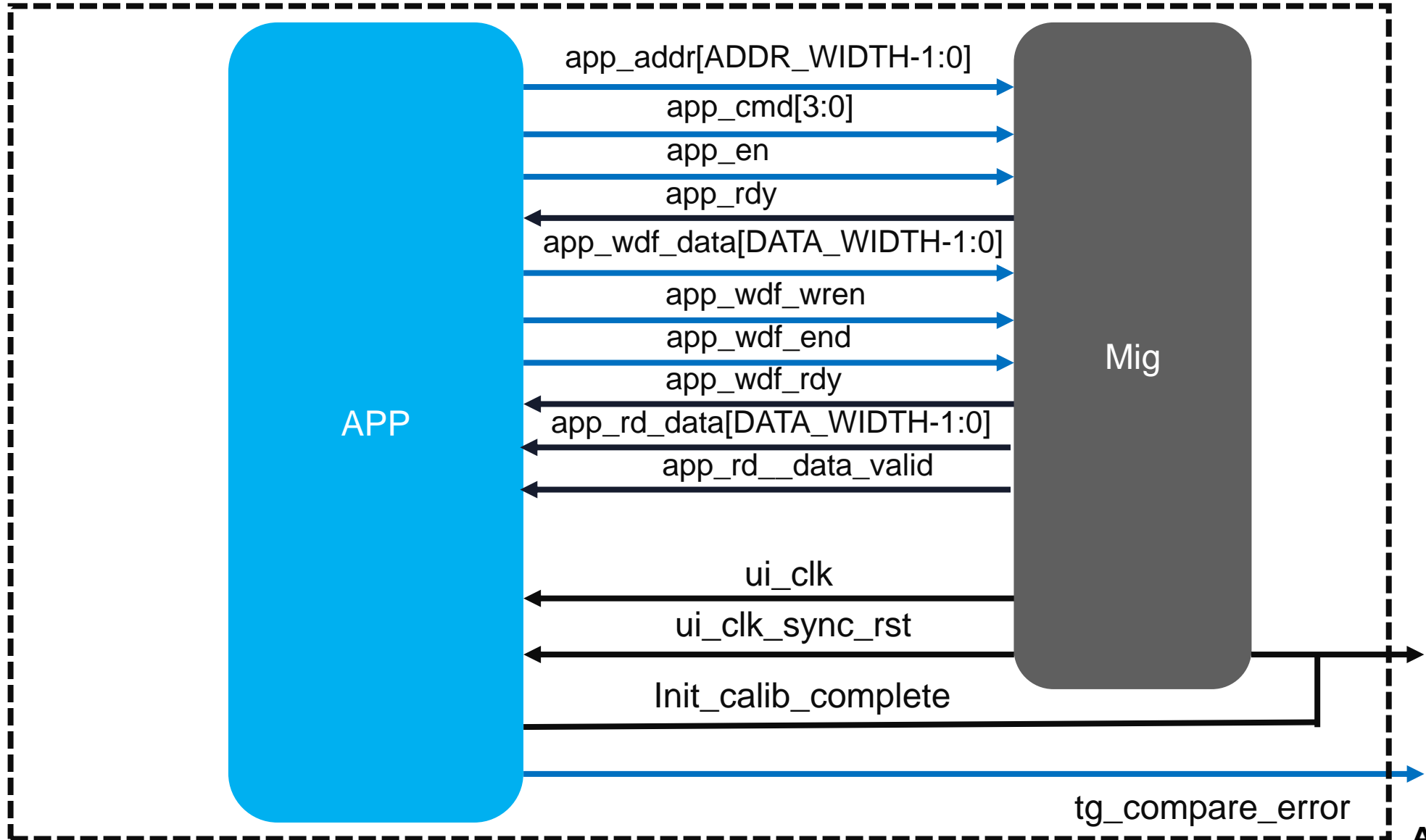
Simulation Setting



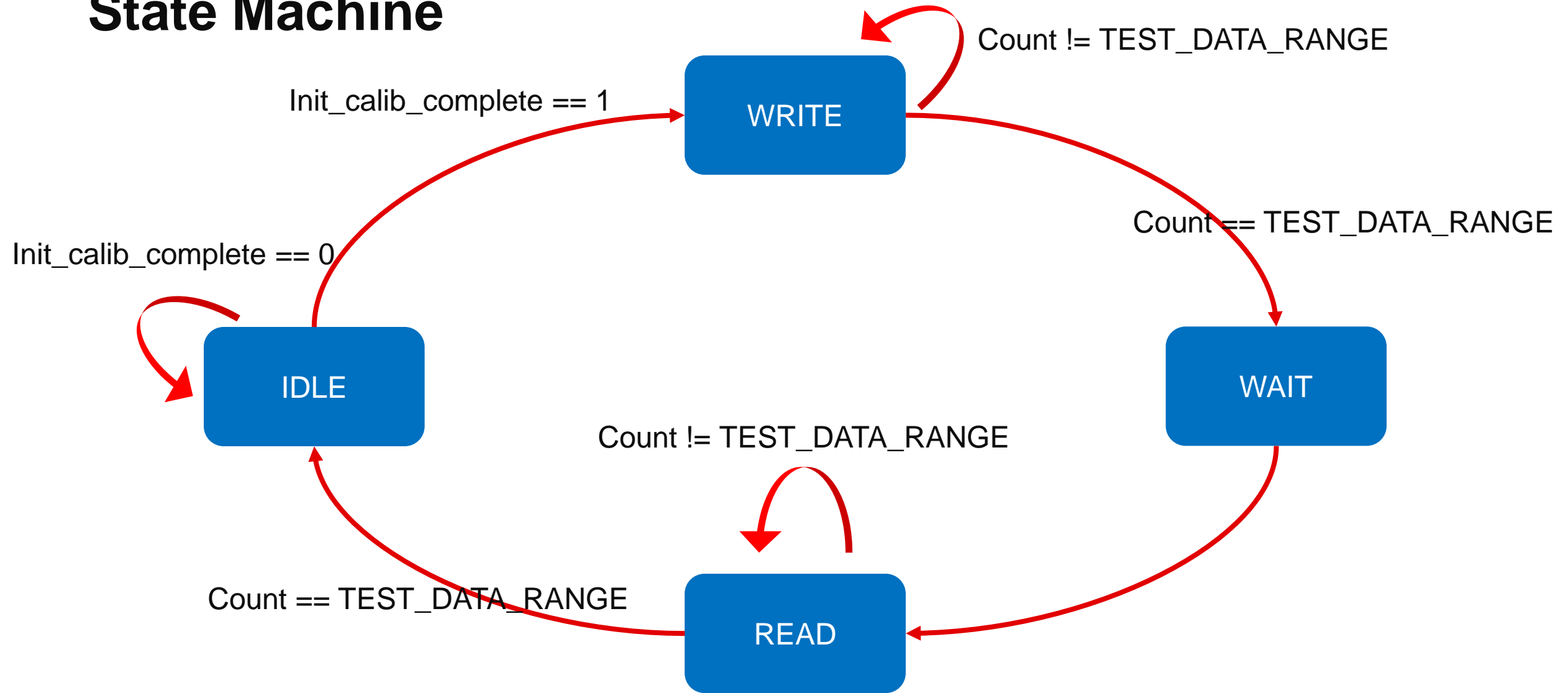
Simulation Setting



Application Interface



State Machine





Thank you very much for your attention!

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