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Memory Interface Generator

Course Agenda
2023

Agenda

- Introduction to the DDR
- MIG IP Setting
- 7Series FPGAs Memory Interface Solution
- Calibration
- How to access DDR via MIG

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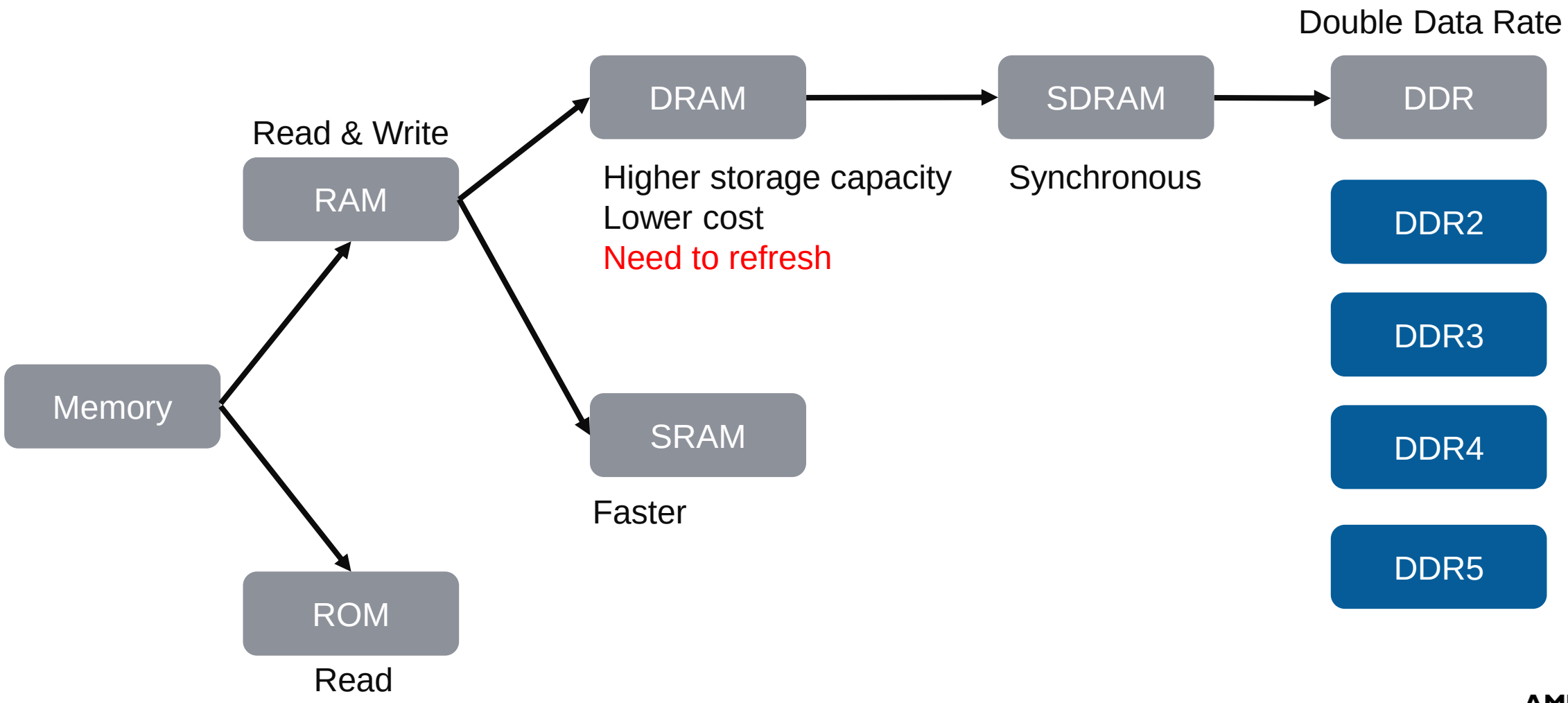
Double Data Rate Synchronous Dynamic Random Access Memory

2023

What is the DDR?

Double Data Rate Synchronous Dynamic Random Access Memory



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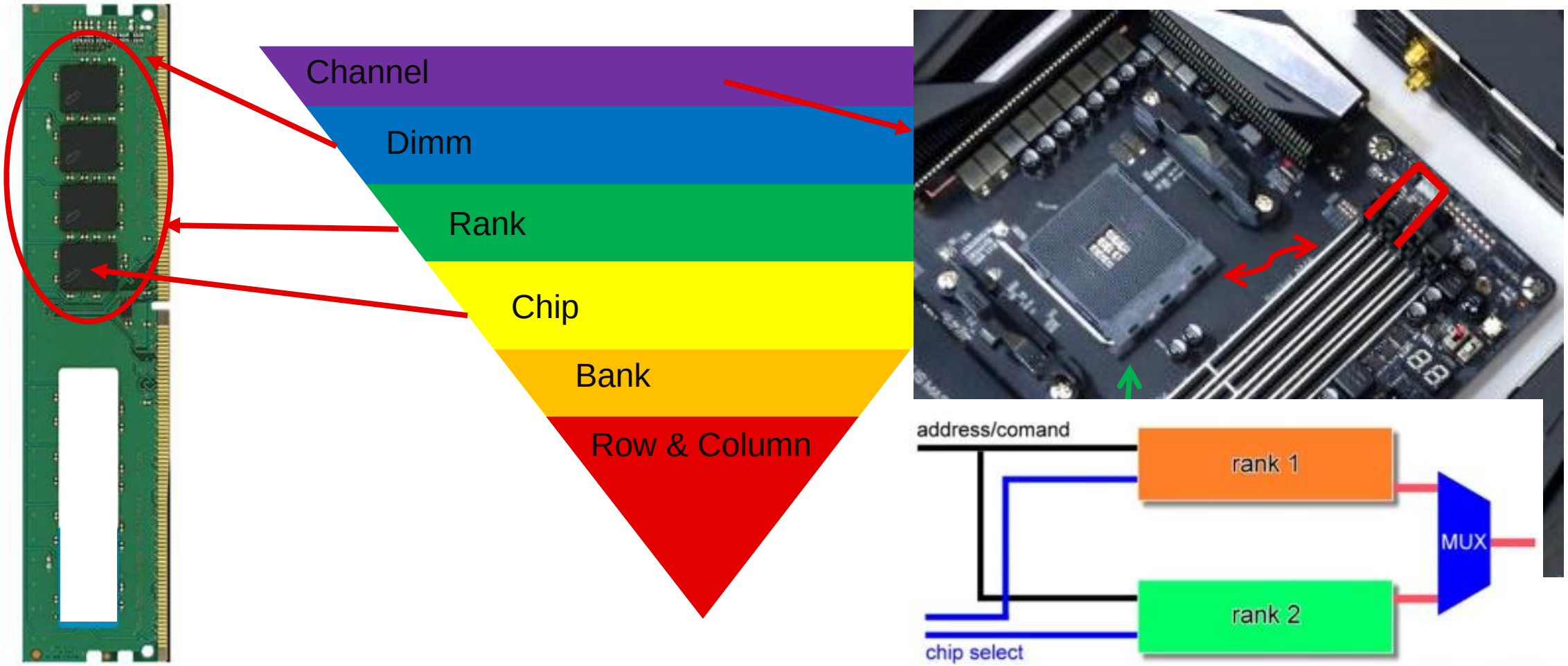
What is the DDR?



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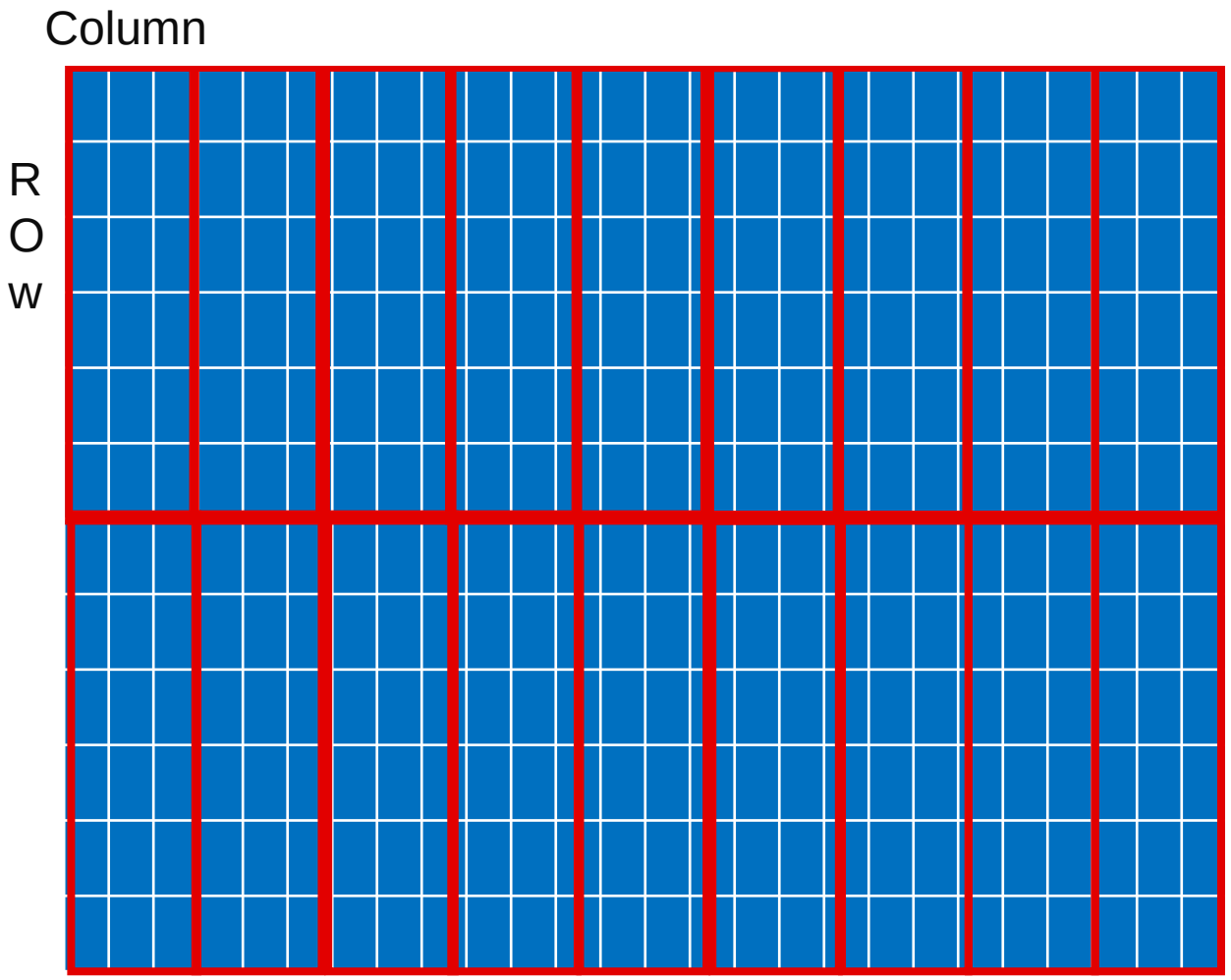
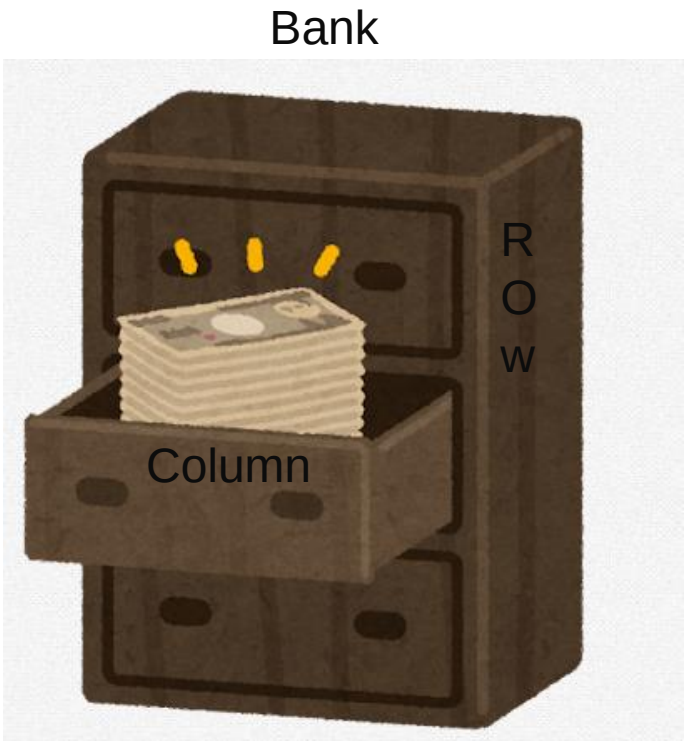
What is the DDR?





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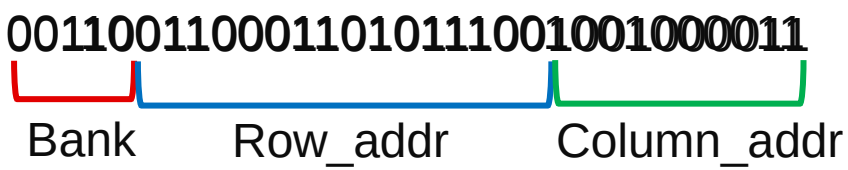
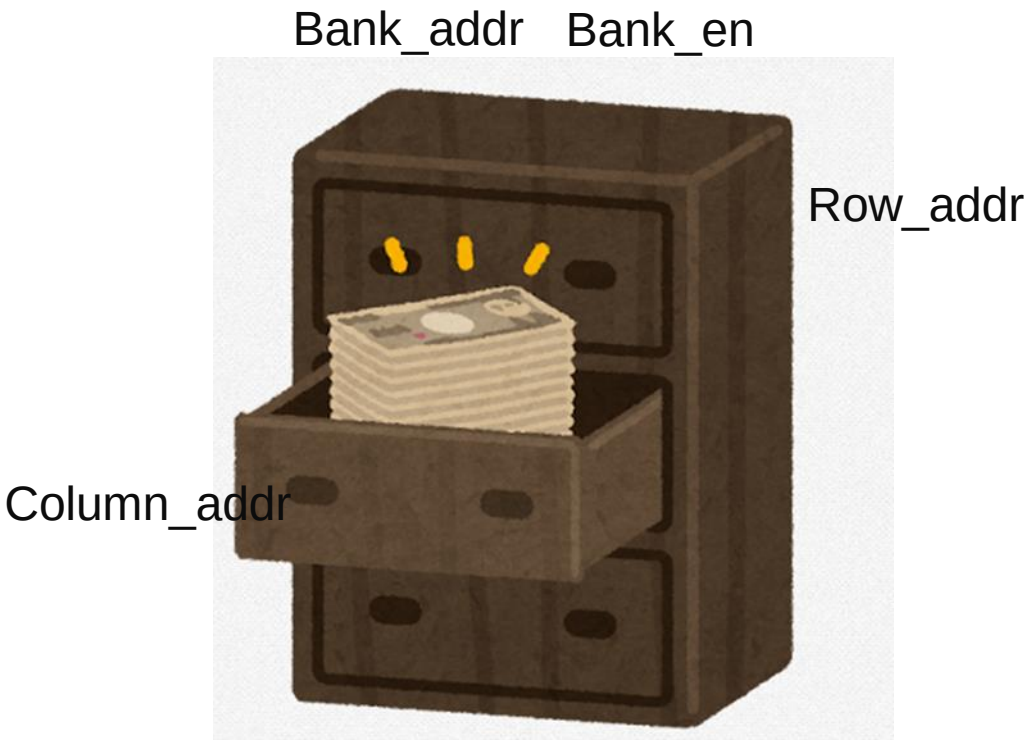
How DDR work?

31bit_addr





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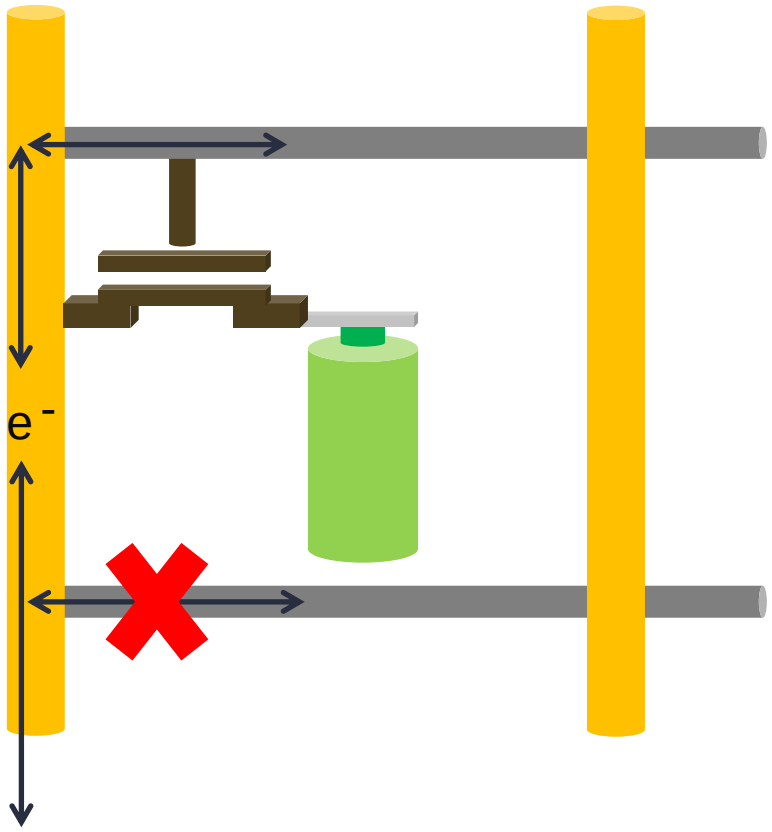
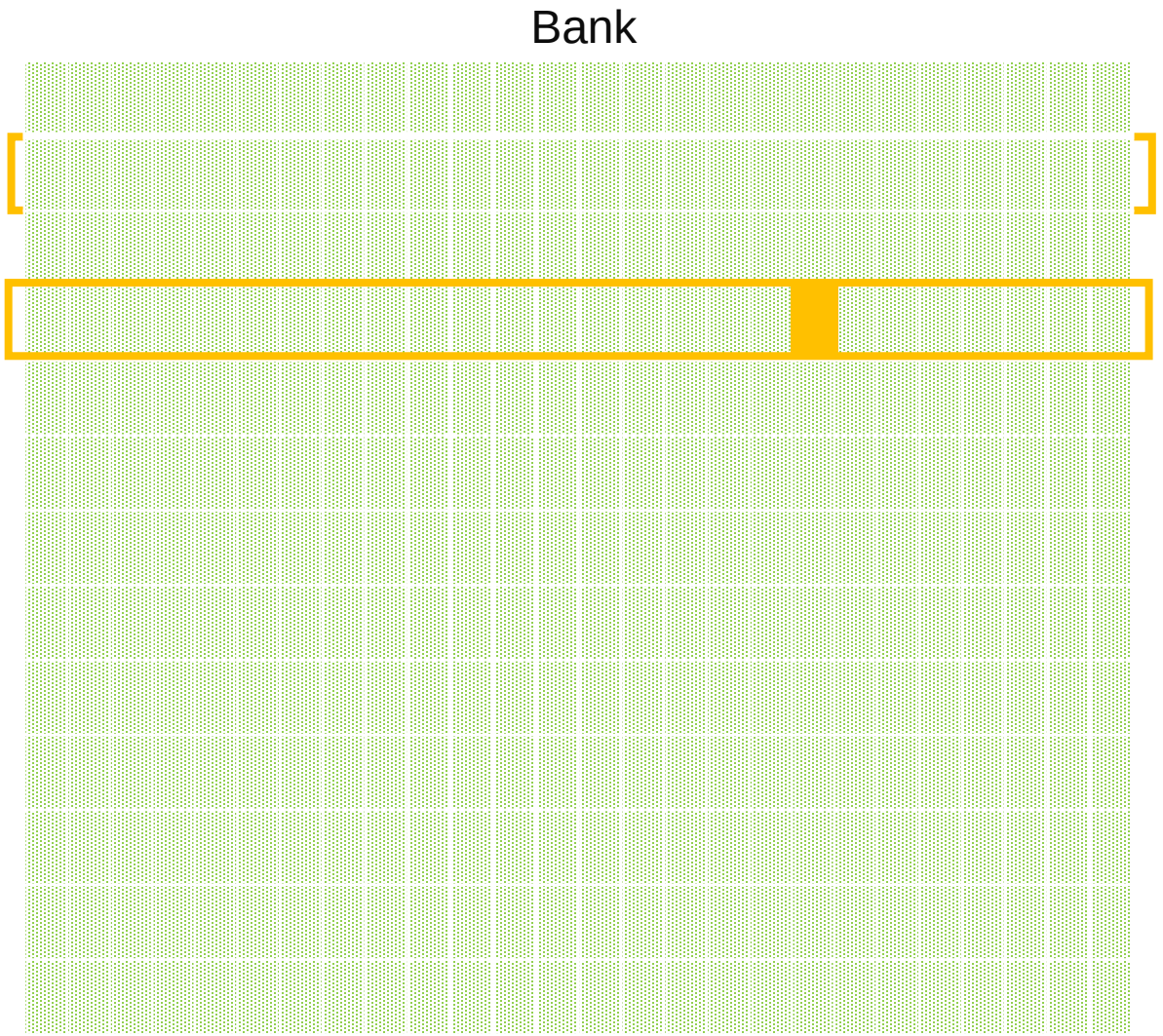
How DDR work?

31bit_addr

0011001100011010111001001000011





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MIG Setting

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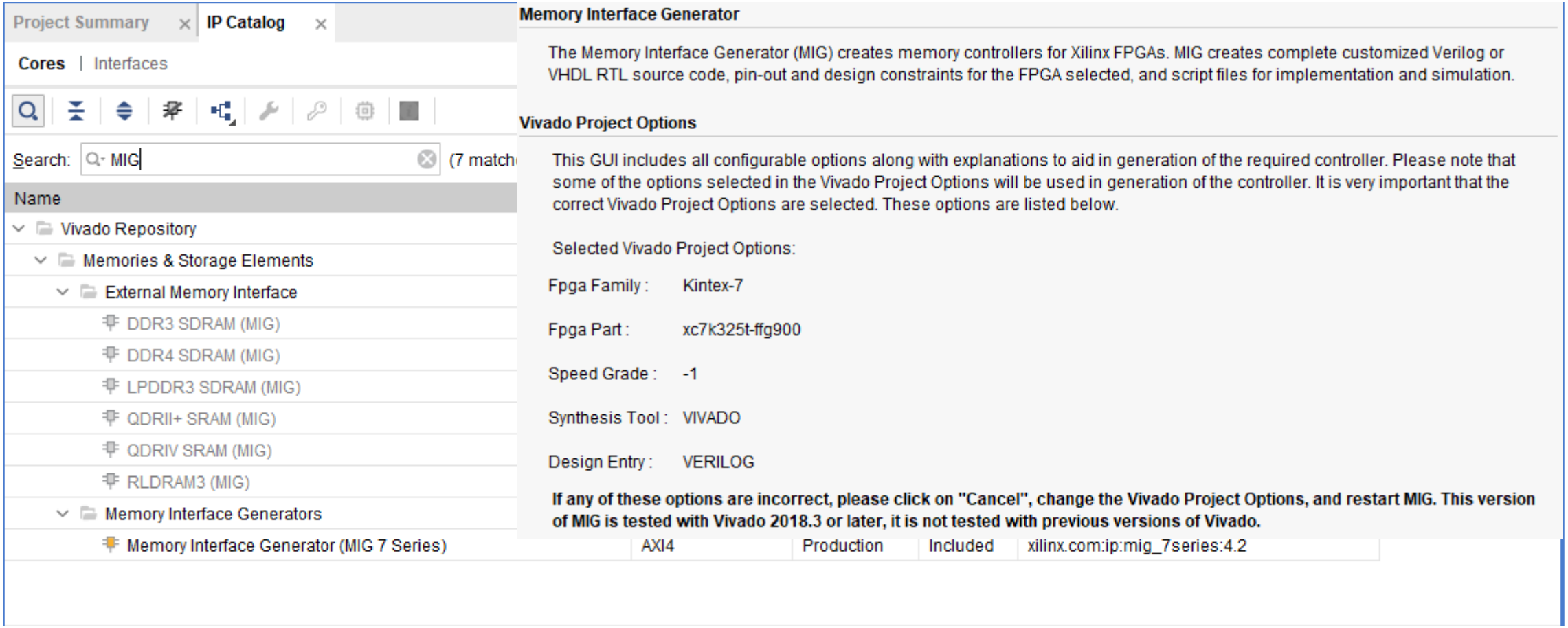
MIG IP Setting



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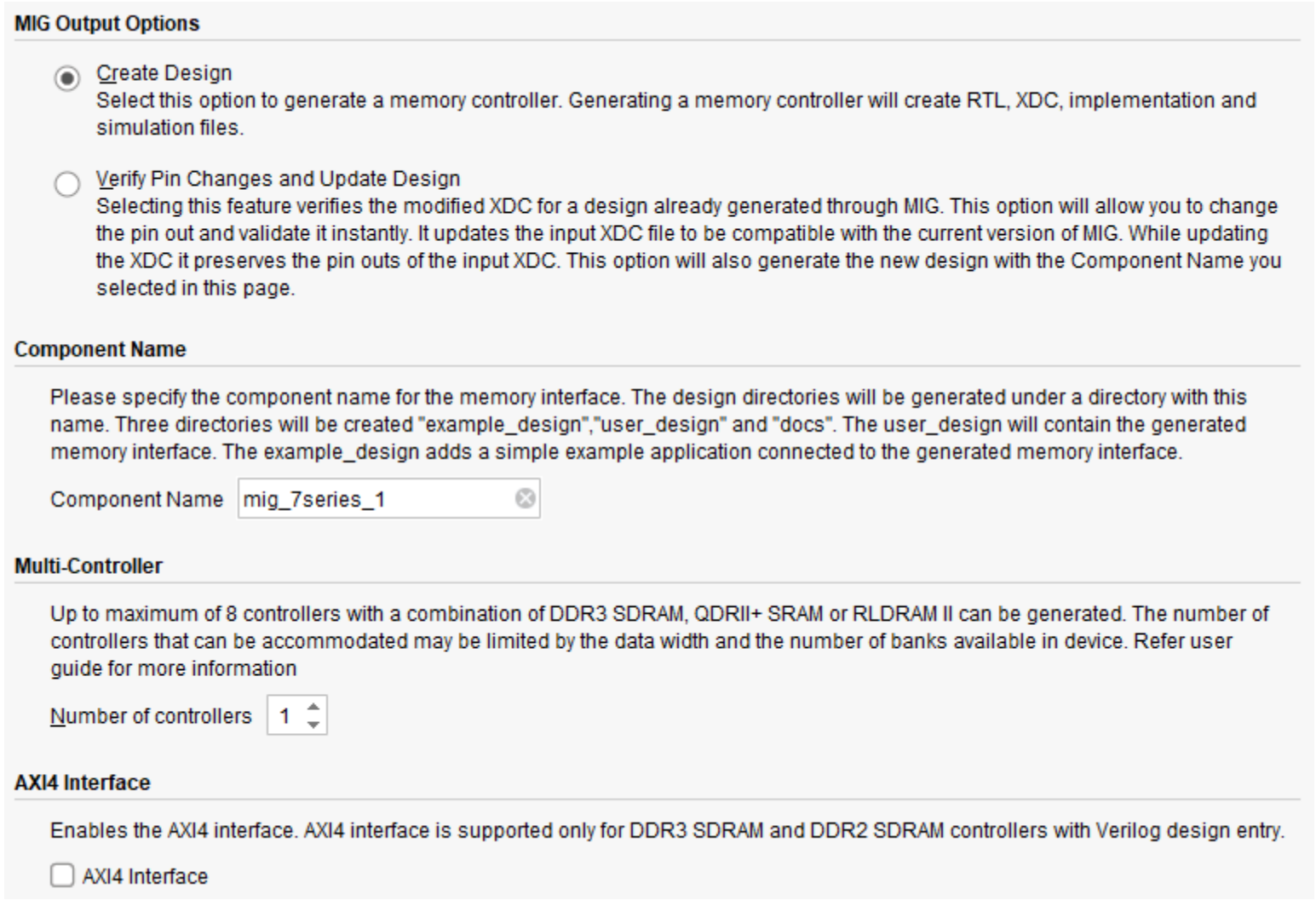
MIG IP Setting



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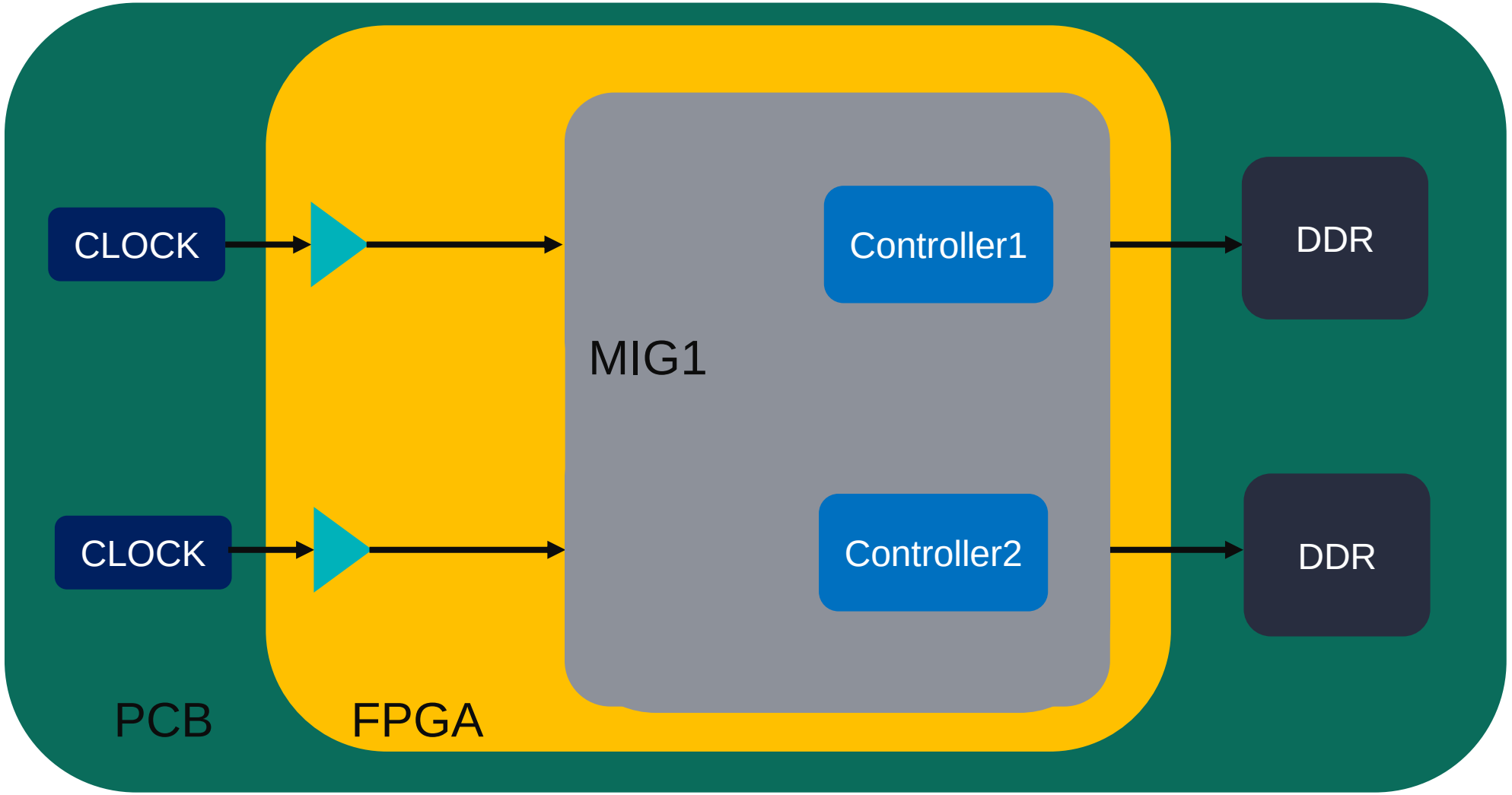
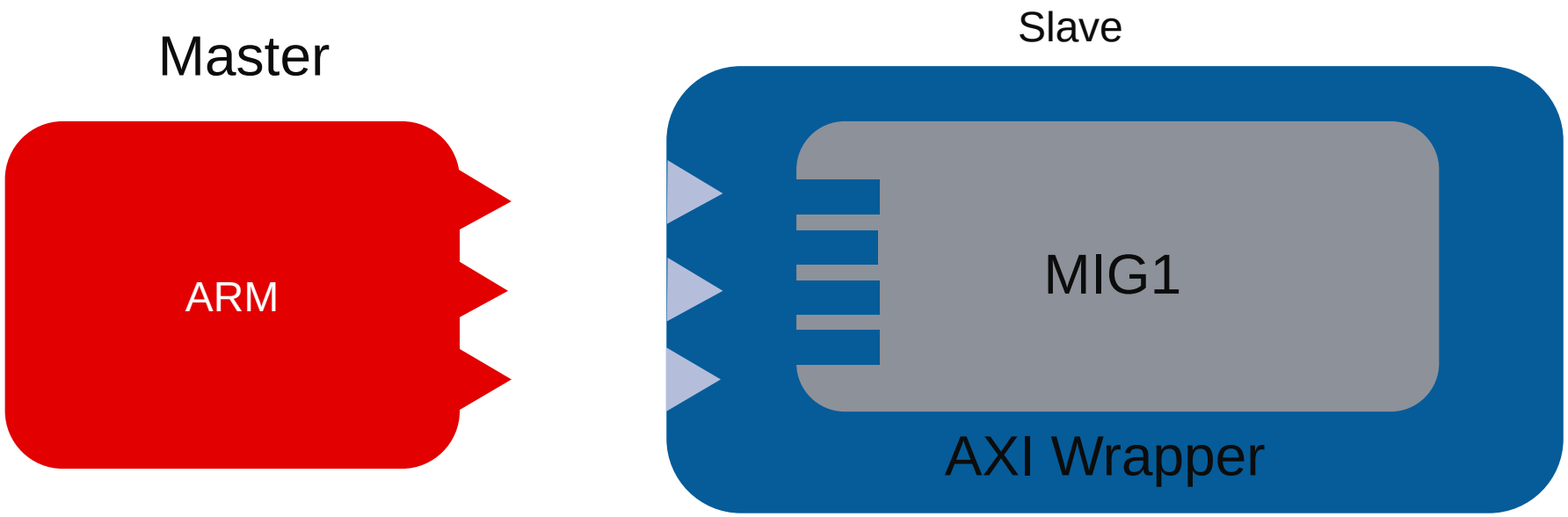
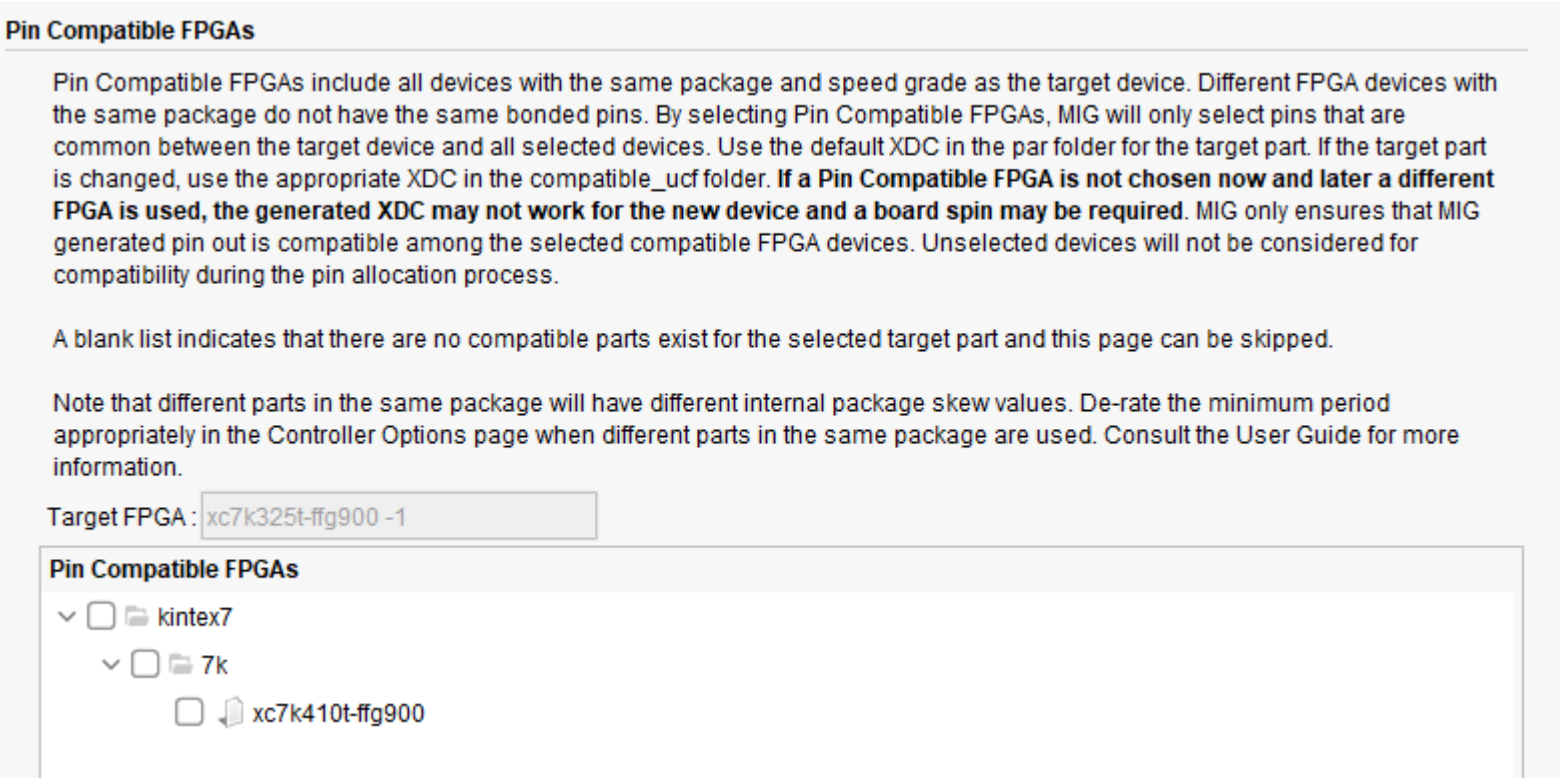
Multi-Controller



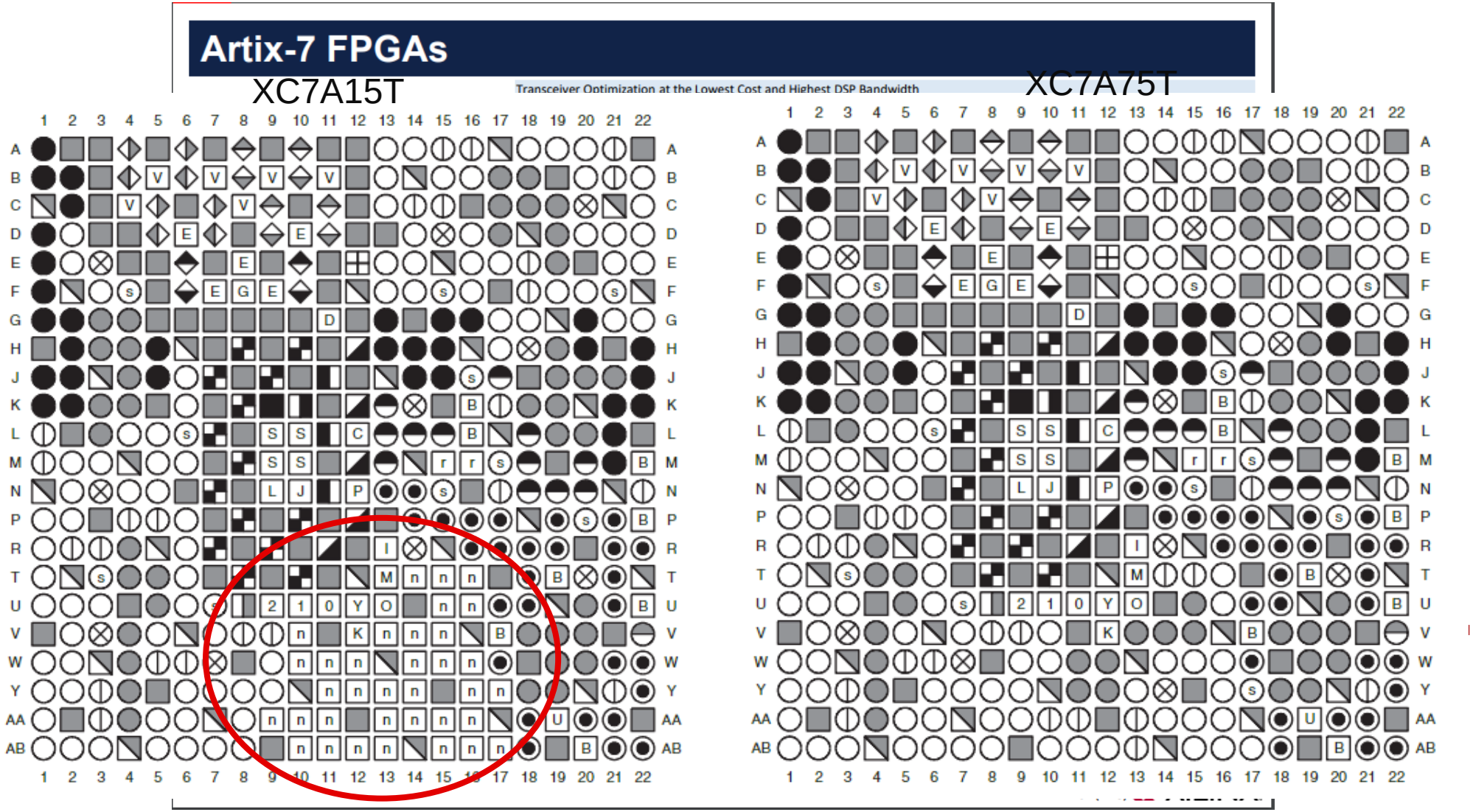
AXI-4 Interface



Ping Compatible



Ping Compatible



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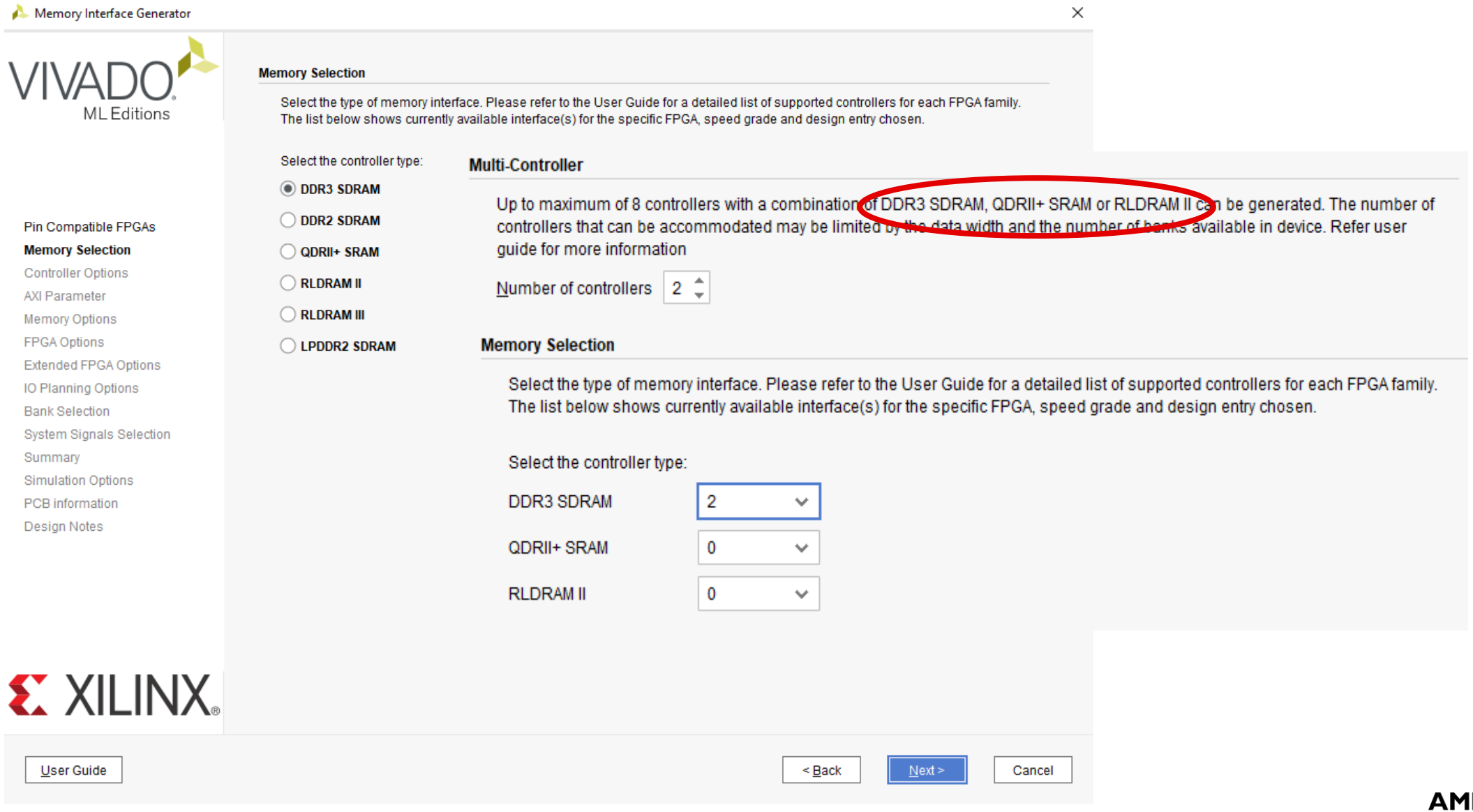
Memory Selection



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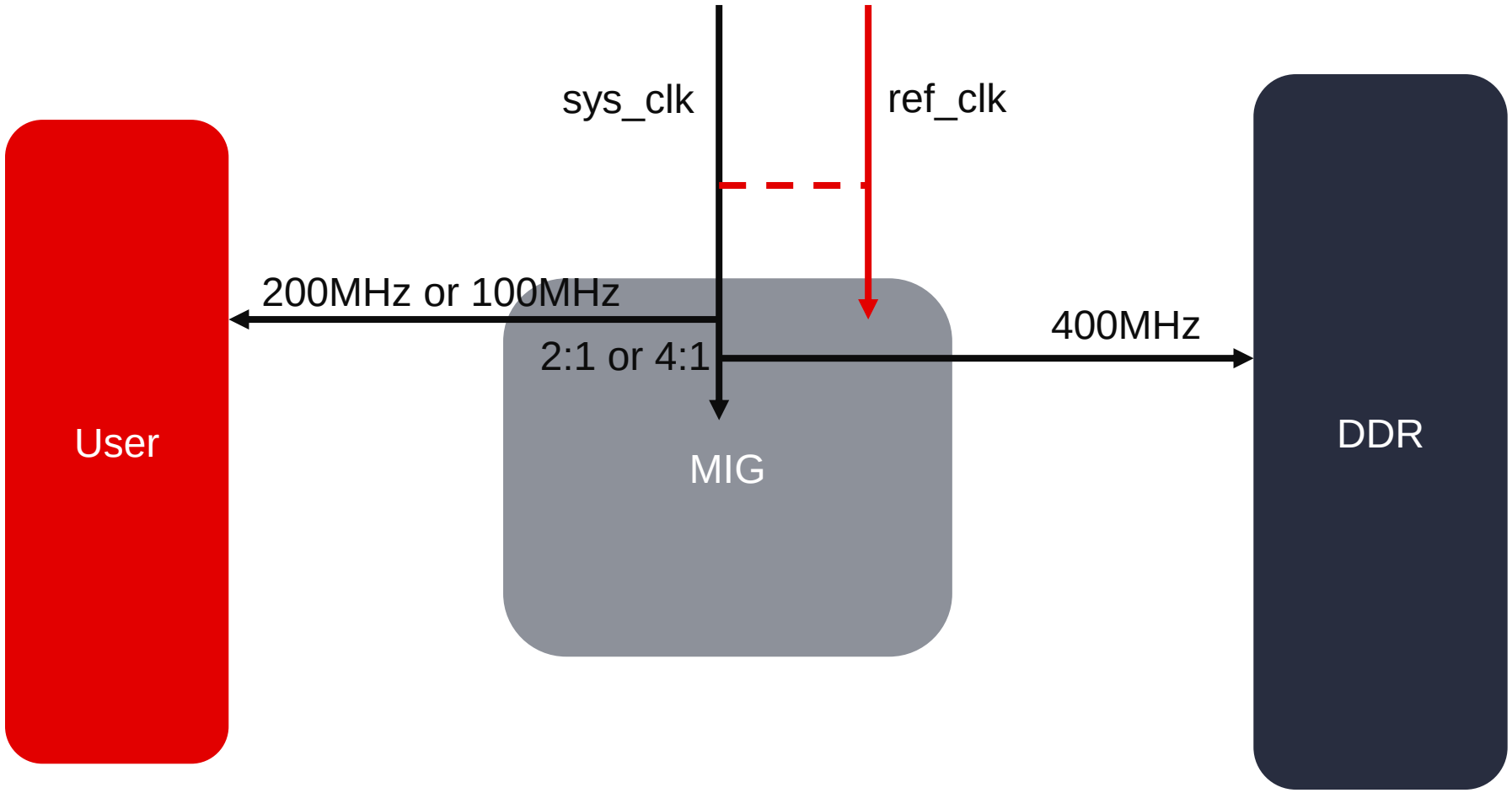
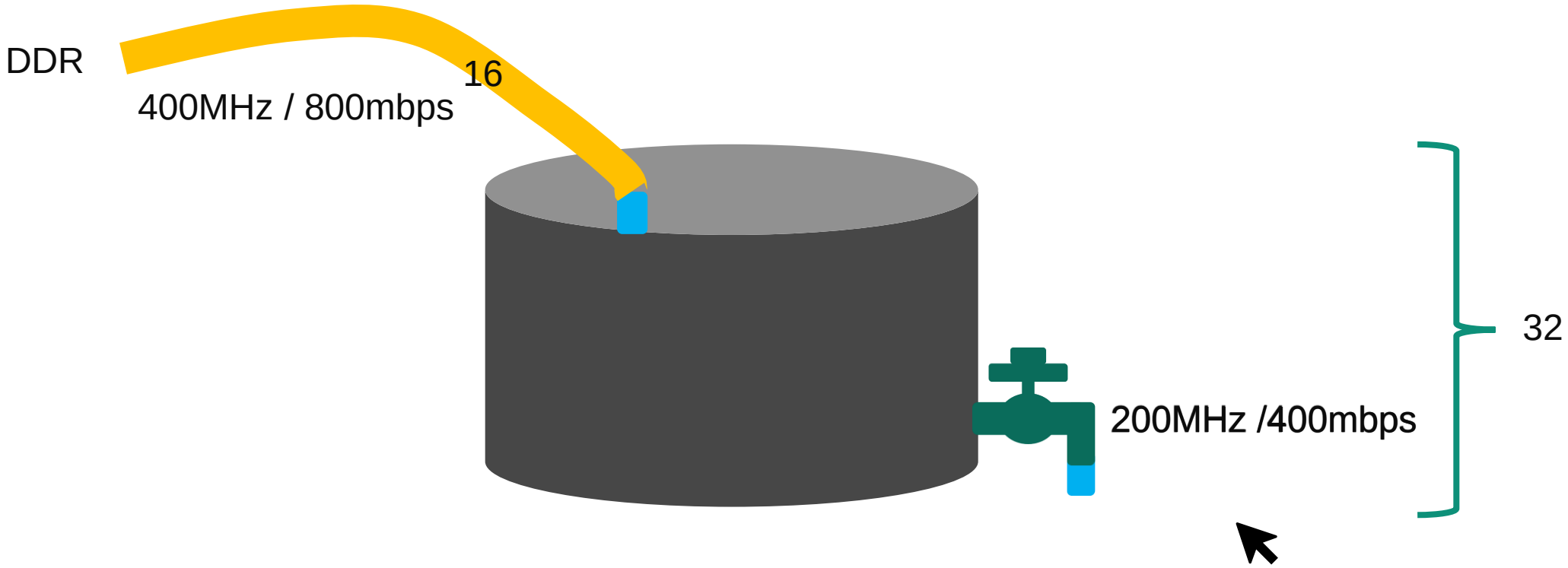
Clock



PHY to Controller Clock Ratio



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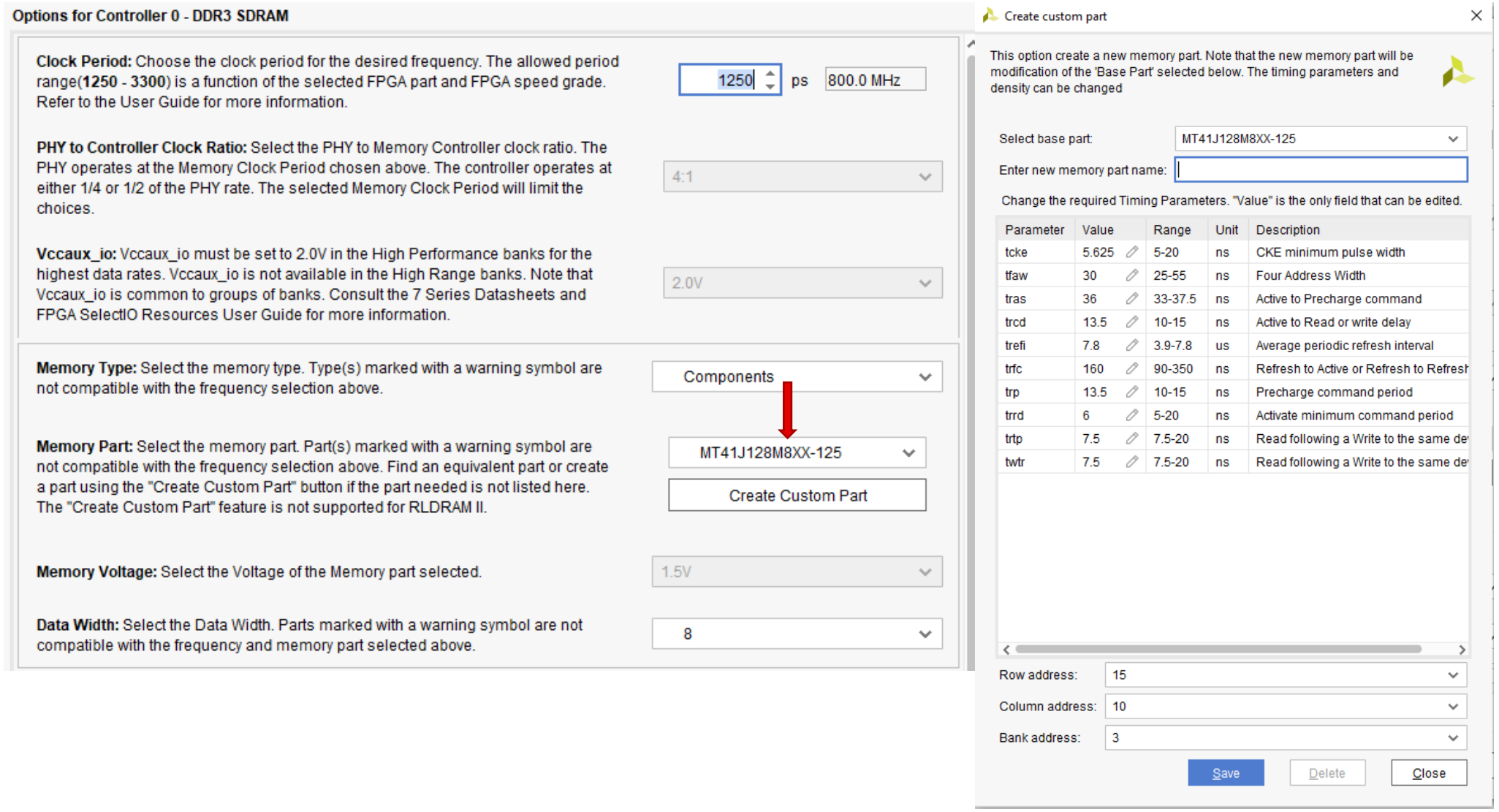
Controller Option



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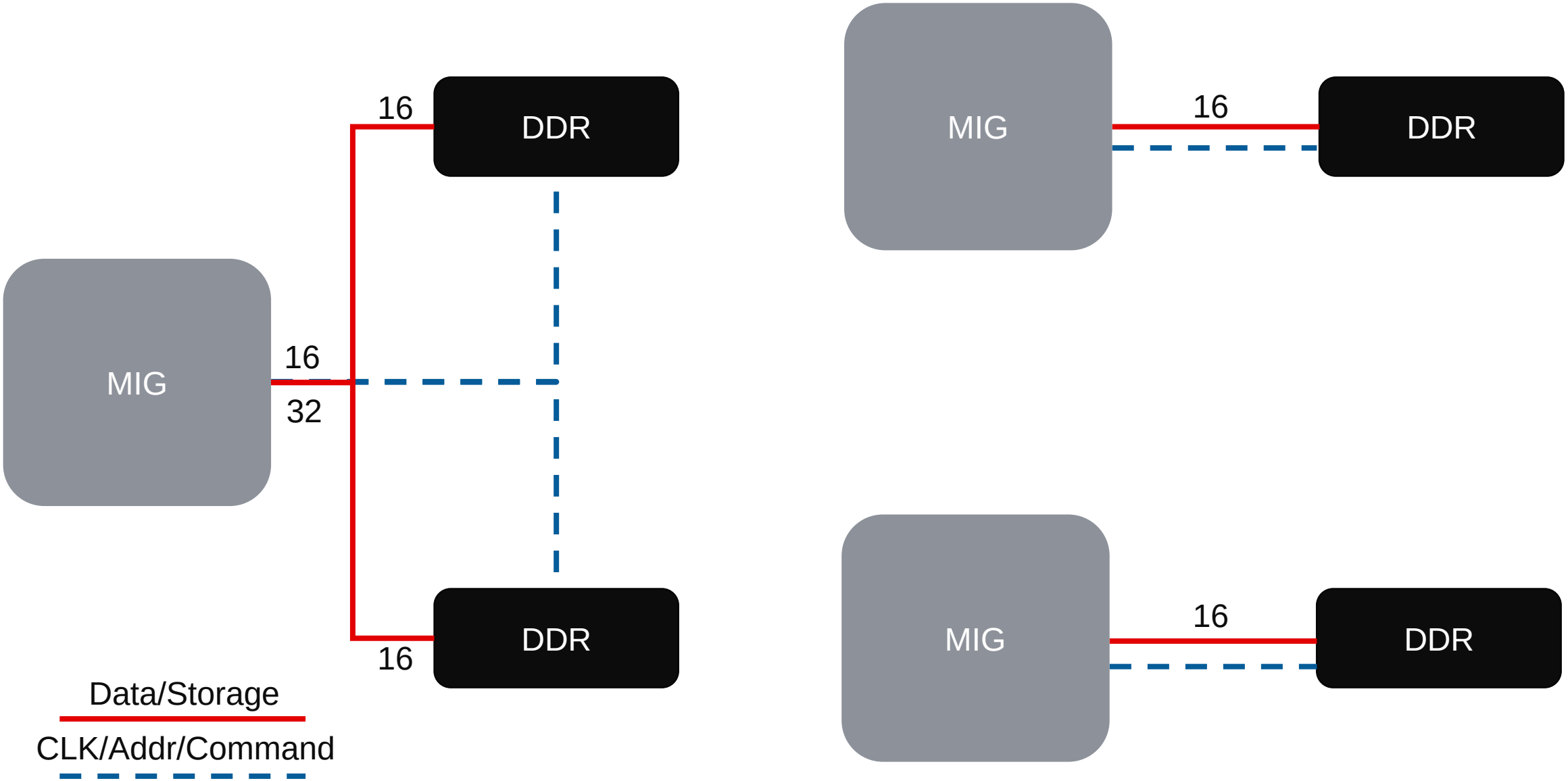
Data Width



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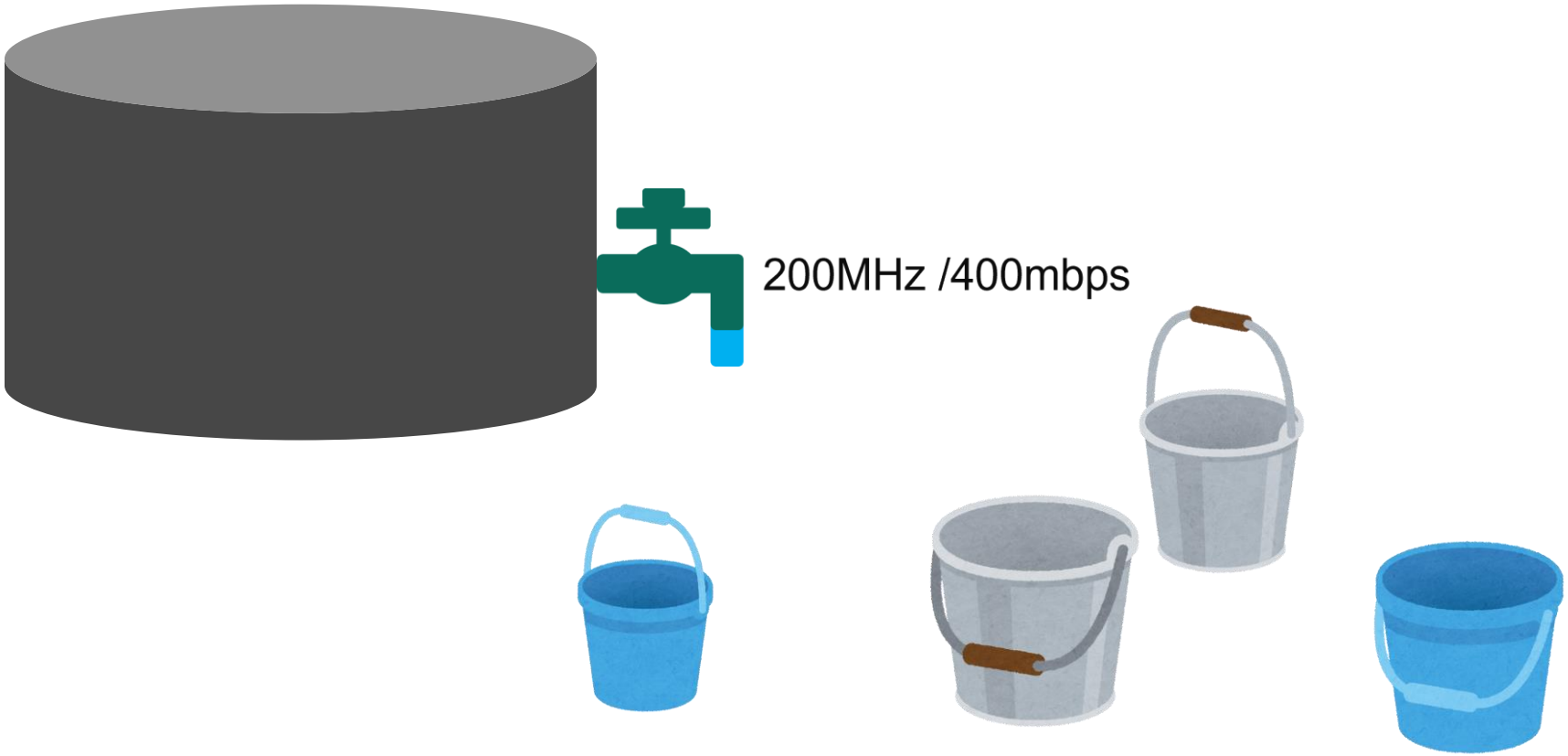
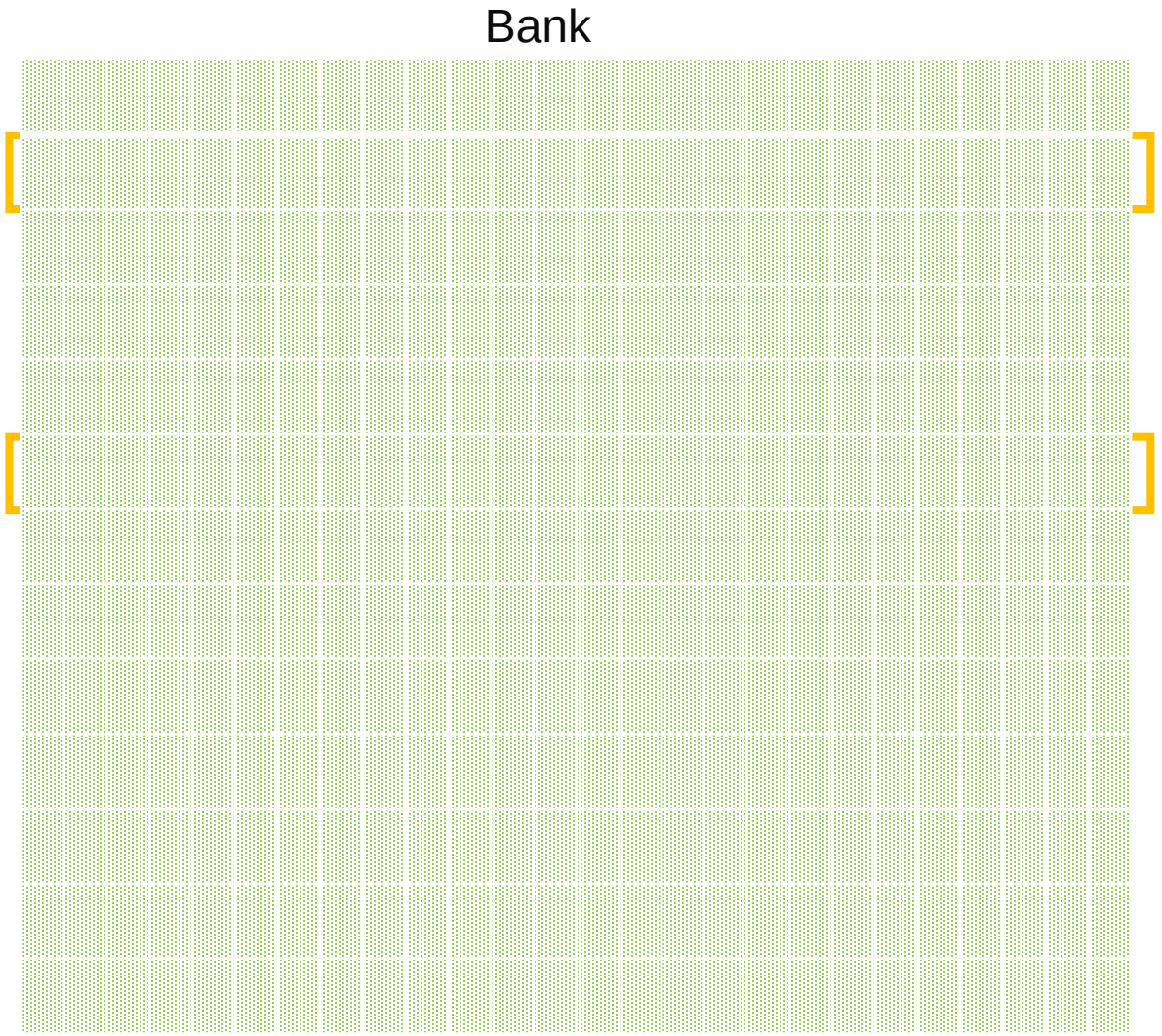
Bank Machine



Ordering

Row Hit

Refresh



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Memory Option

Memory Options C0 - DDR3 SDRAM

Input Clock Period: Select the period for the PLL input clock (CLKIN). MIG determines the allowable input clock periods based on the Memory Clock Period entered above and the clocking guidelines listed in the User Guide. The generated design will use the selected Input Clock and Memory Clock Periods to generate the required PLL parameters. If the required input clock period is not available, the Memory Clock Period must be modified.

1250 ps (800 MHz)

Choose the Memory Options for the memory device. Memory Option selections are restricted to those supported by the controller. Consult the memory vendor data sheet for more information.

Read Burst Type and Length

The burst type determines the data ordering within a burst. Consult the memory datasheet for more information. Burst length 8 is the only supported value.

Sequential

Output Driver Impedance Control

Programmable impedance for the output buffer.

RZQ/7

RTT (nominal) - On Die Termination (ODT)

Select the nominal value of ODT for the DQ, DQS/DQS# and DM signals on the component or DIMM interface. This must be set to RZQ/6 i(40 ohms) for data rates at 1333 Mbps and above. In 2 slot DIMM configuations this value will be used for the unwritten slot during a write and will also be used for the unselected slot during a read. Use board level simulation to choose the optimum value.

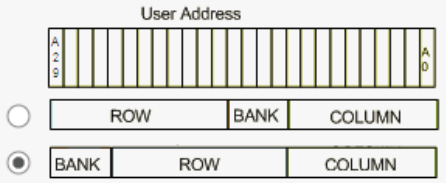
RZQ/4

Controller Chip Select Pin

The Chip Select (CS#) pin can be tied low externally to save one pin in the address/command group when this selection is set to 'Disable'. Disable is only valid for single rank configurations.

Enable

Memory Address Mapping Selection



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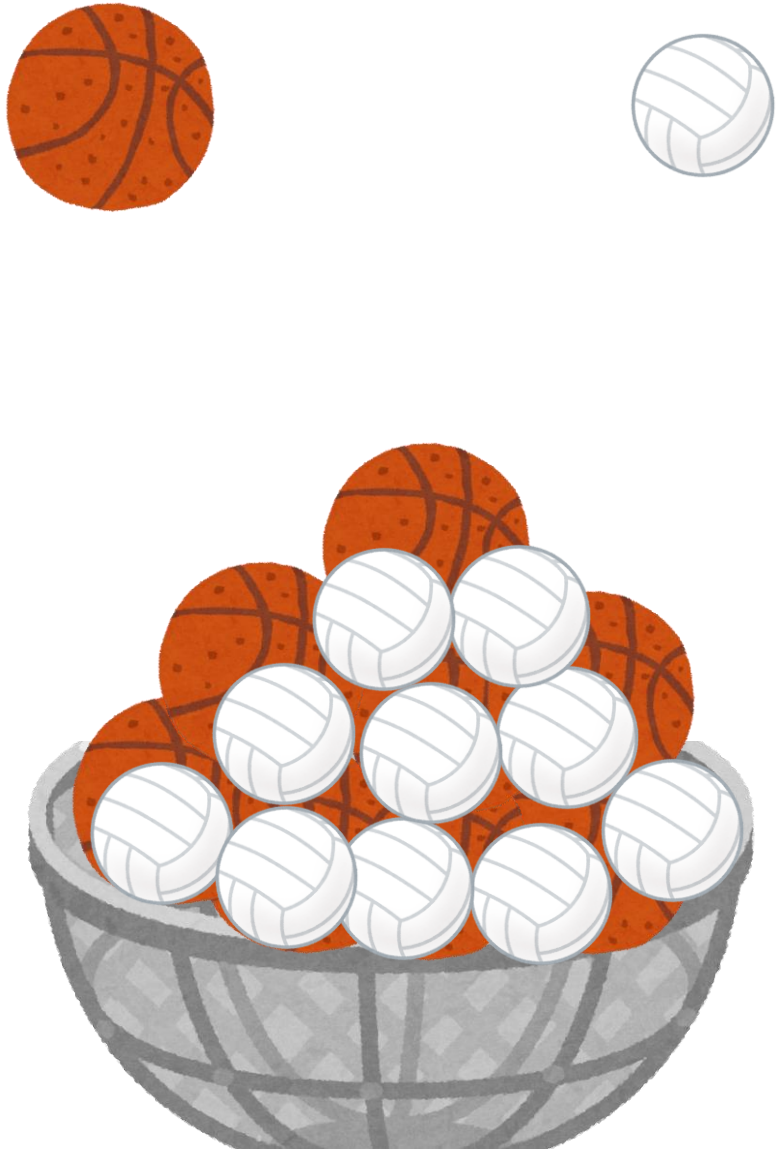
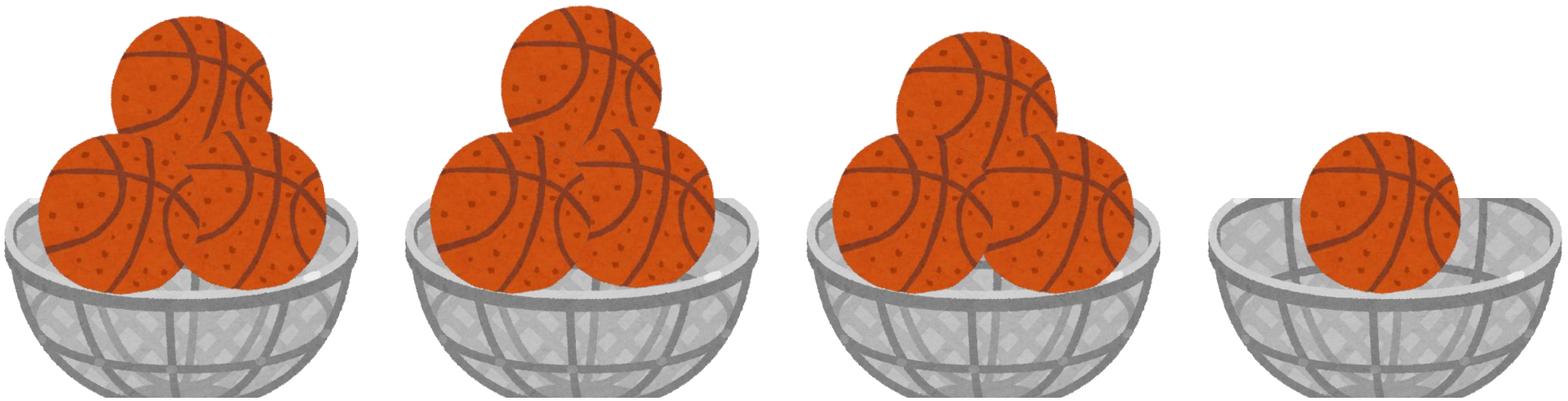
Burst

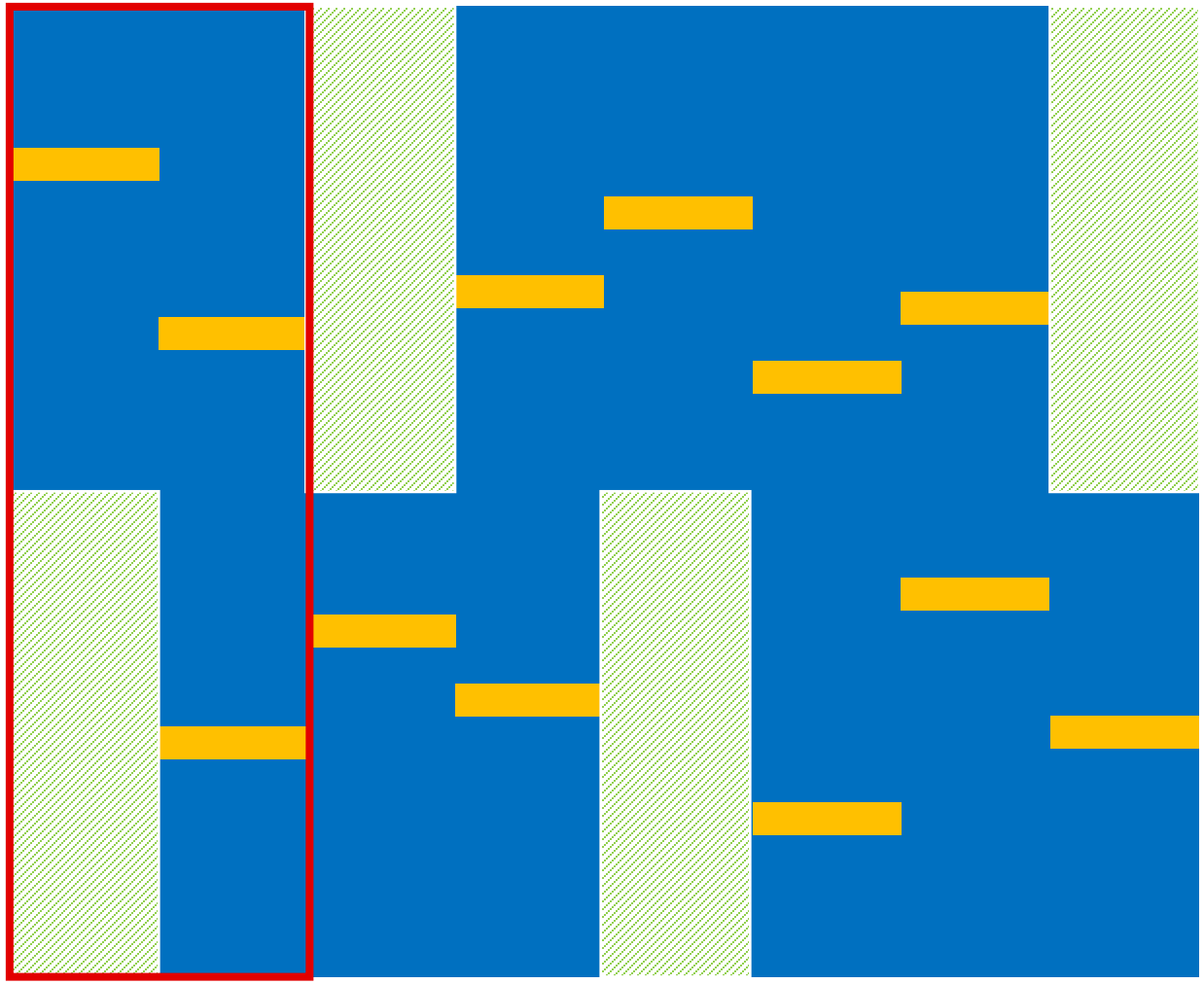


Interleaved



Sequential

Bank



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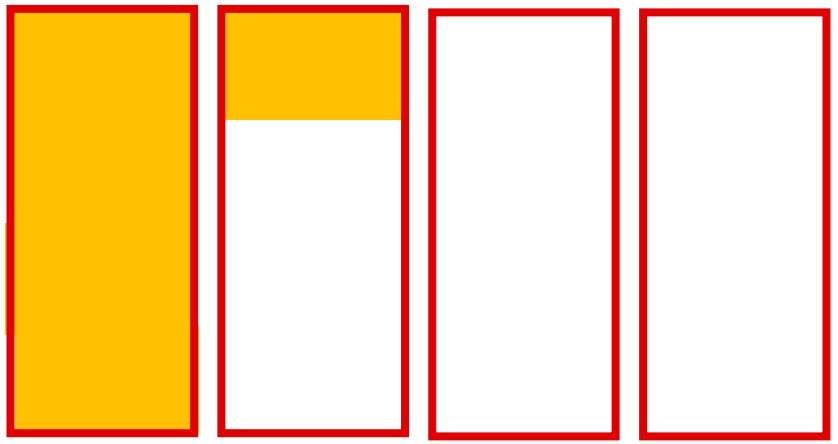
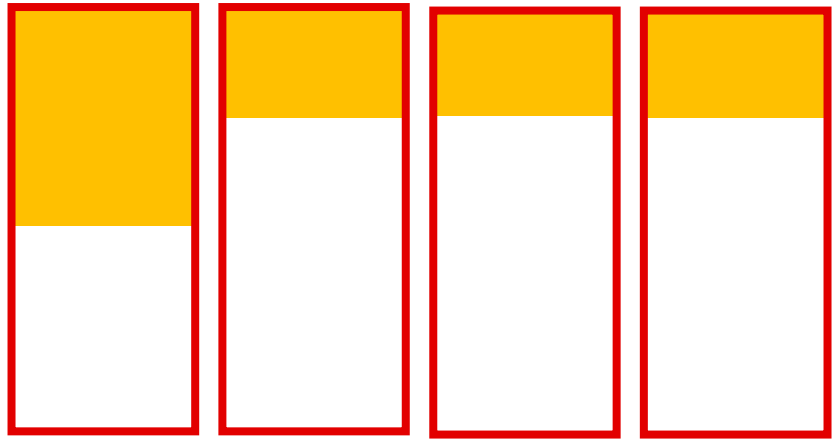
Memory Address Mapping

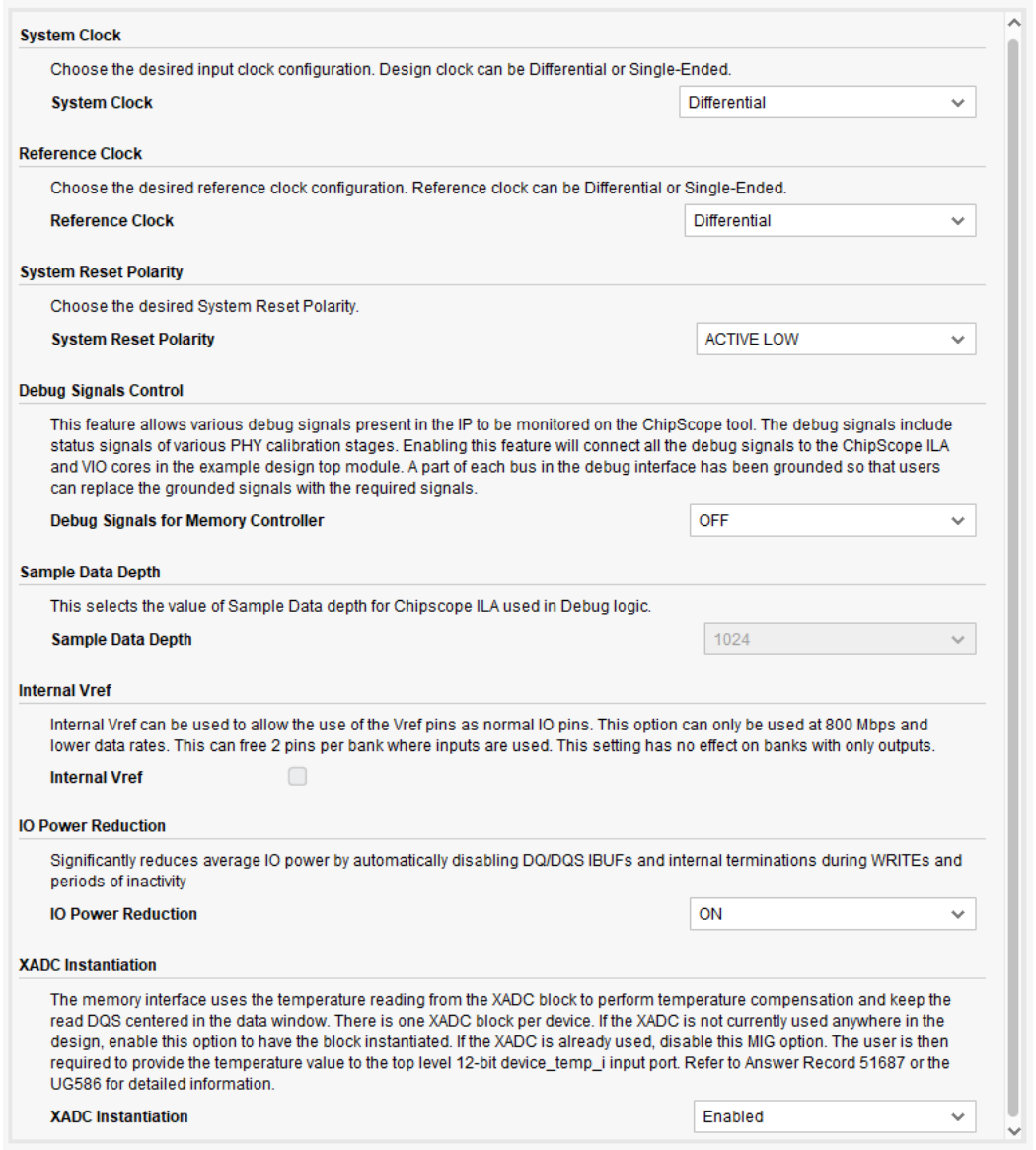
BANK	ROW	COLUMN
00	00	
01	01	
10	10	
11	11	



ROW	BANK	COLUMN
00	00	
01	01	
10	10	
11	11	



FPGA Option



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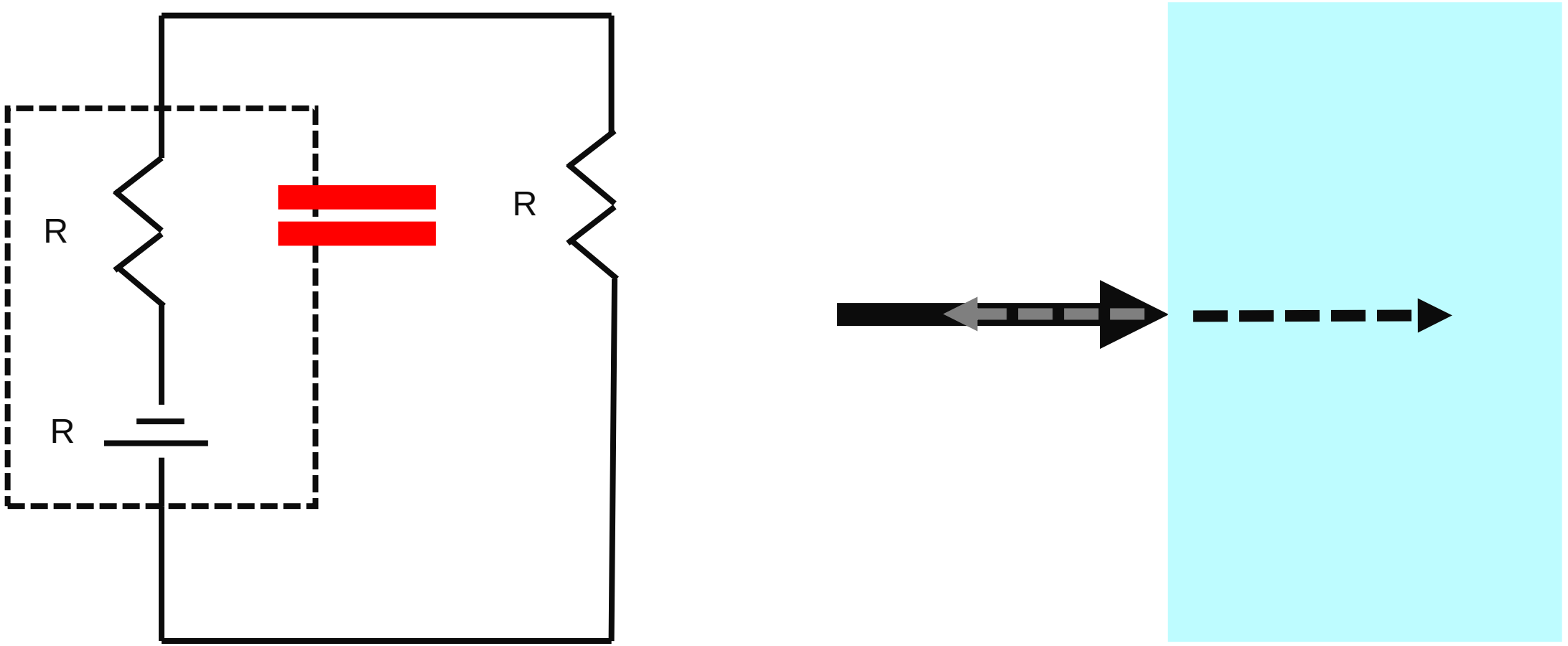
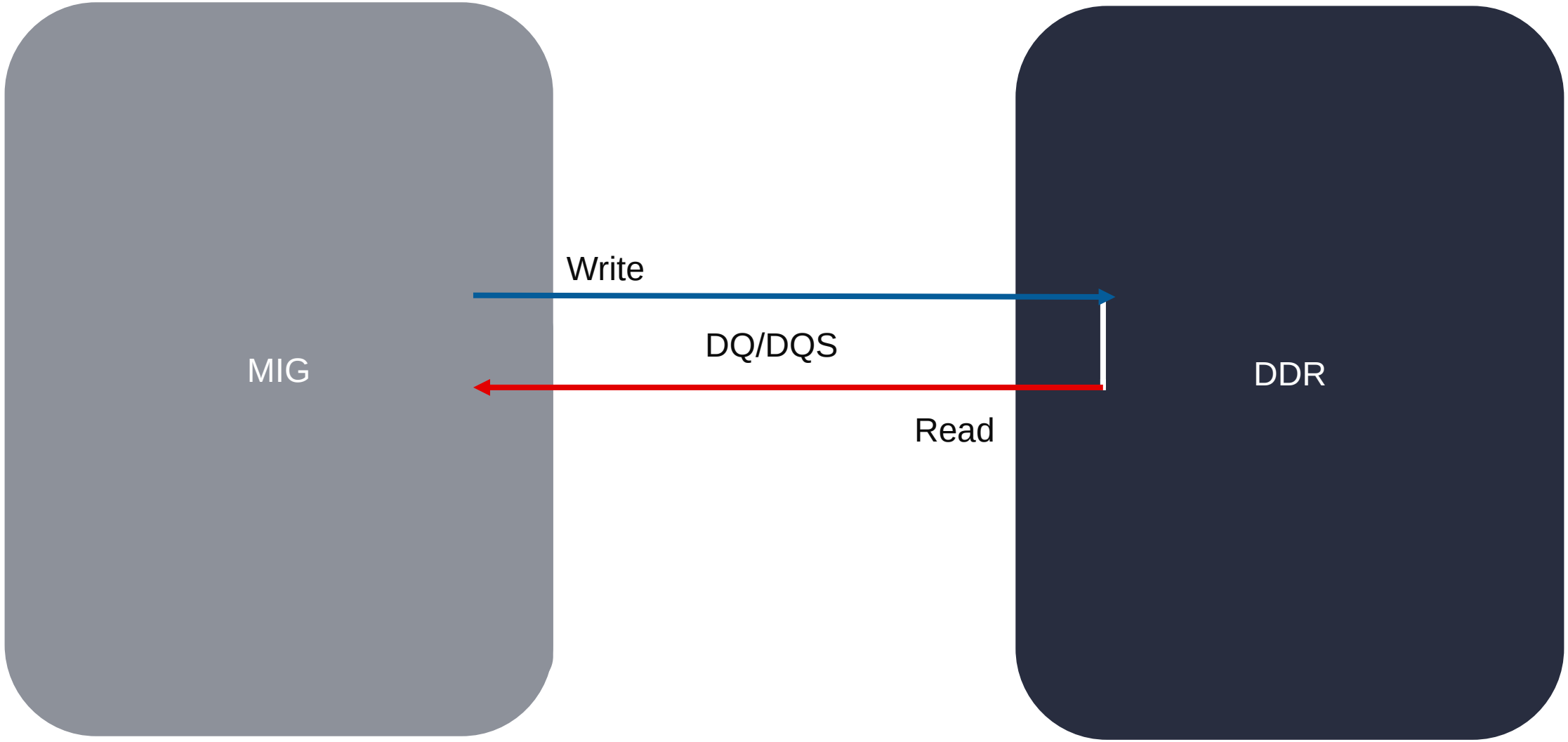
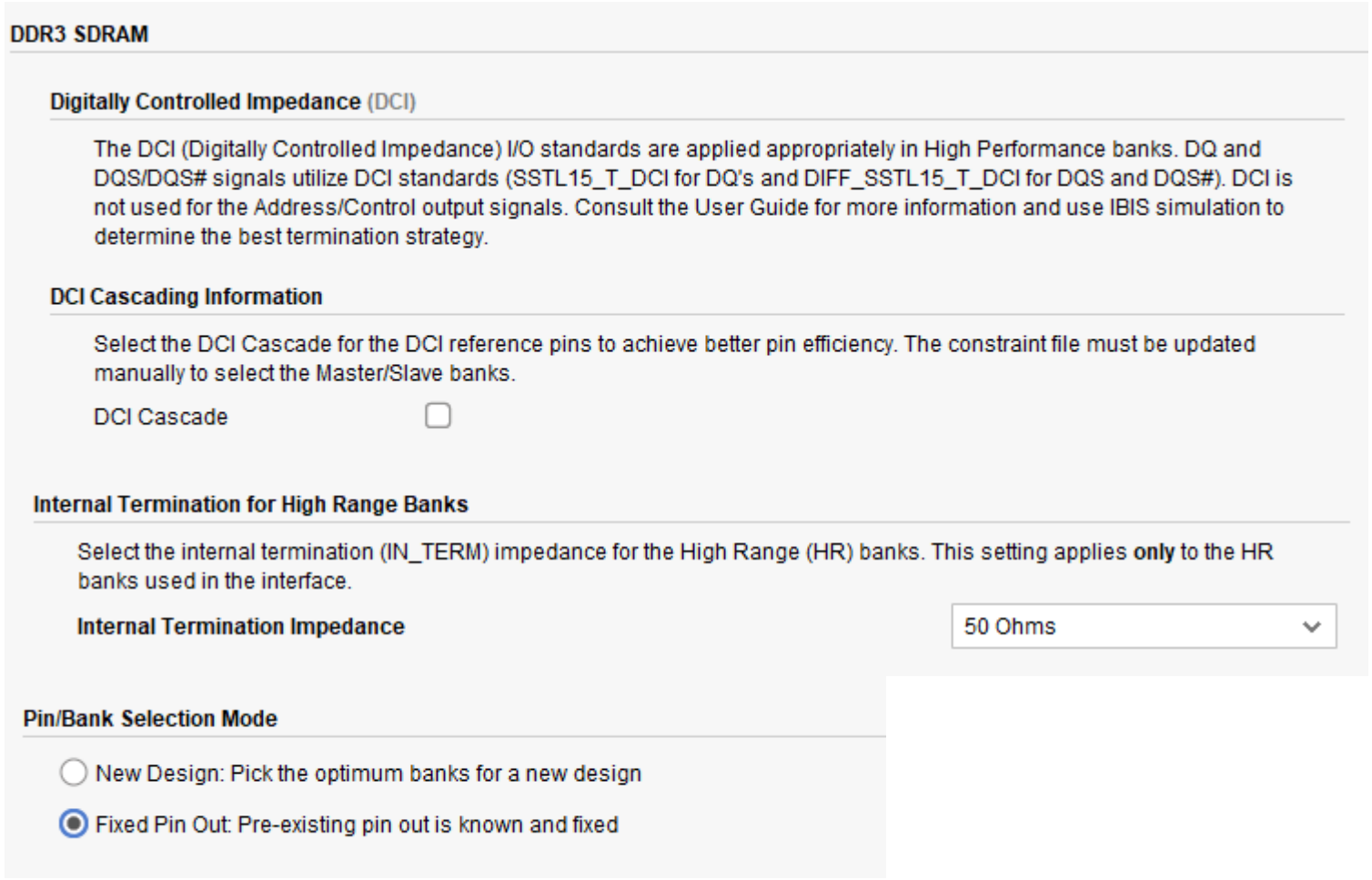
Impedance matching



IO Power Reduction



FPGA Option



Bank and Source

Bank Selection For Contoller 0 - DDR3 SDRAM

Select the byte groups for the data and address/control in the architectural view below. Data and Ad
within 3 vertical banks. The interface cannot span horizontally. ***Bank(s) 14,15 contain configuratio**
of these banks for default configurations. If bank(s) 14,15 is selected for your memory controlle
ensure no conflicts with the configuration pin. For more information see UG586 Bank and Pin rul
The Address/Control byte groups must be selected in the middle bank in interfaces using 3 b
groups must be selected in a single bank. Bank selection may be restricted to High Performan
interface data rate selected.

Address/Control : 25/25 Data : 11/11

Bank 14	Signal Sets
Byte Group T0	Unassigned
Byte Group T1	Unassigned
Byte Group T2	Unassigned
Byte Group T3	Unassigned

Bank 34	Signal Sets
Byte Group T0	Address/Ctrl-0
Byte Group T1	Address/Ctrl-1
Byte Group T2	Address/Ctrl-2
Byte Group T3	DQ[0-7]

HR Bank

Bank 13	Signal Sets
Byte Group T0	Unassigned
Byte Group T1	Unassigned
Byte Group T2	Unassigned
Byte Group T3	Unassigned

HP Bank

Bank 33	Signal Sets
Byte Group T0	Unassigned
Byte Group T1	Unassigned
Byte Group T2	Unassigned
Byte Group T3	Unassigned

HR Bank

Bank 12	Signal Sets
Byte Group T0	Unassigned
Byte Group T1	Unassigned
Byte Group T2	Unassigned
Byte Group T3	Unassigned

HP Bank

Bank 32	Signal Sets
Byte Group T0	Unassigned
Byte Group T1	Unassigned
Byte Group T2	Unassigned
Byte Group T3	Unassigned

System Signals Selection

Select the system pins below appropriately for the interface. Customization of these pins can also be made in the XDC after the design is generated. For more information see UG586 Bank and Pin rules.

System Clock and Reference Clock pin selections will not be visible if the 'No Buffer' option was selected in the FPGA Options page.

System Clock Pin Selection

The **sys_clk** is used as the system clock for the memory interface. This signal should be connected to a low jitter external clock source via a differential (P/N) pair for best performance. This signal should be in the address/control bank, but may be placed in an adjacent bank if there are not enough pins available such as when fitting a 16 bit interface in a single

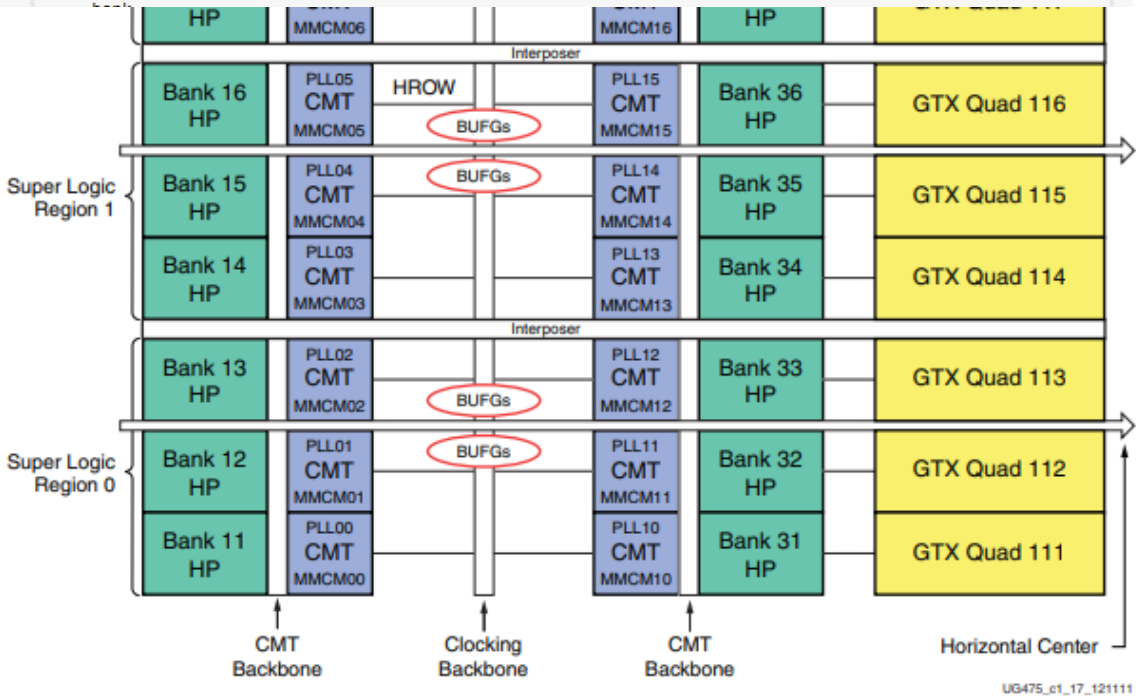


Figure 1-19: **XC7V2000T Banks**

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7Series FPGAs Memory Interface Solution

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2023

7Series FPGAs Memory Interface Solution

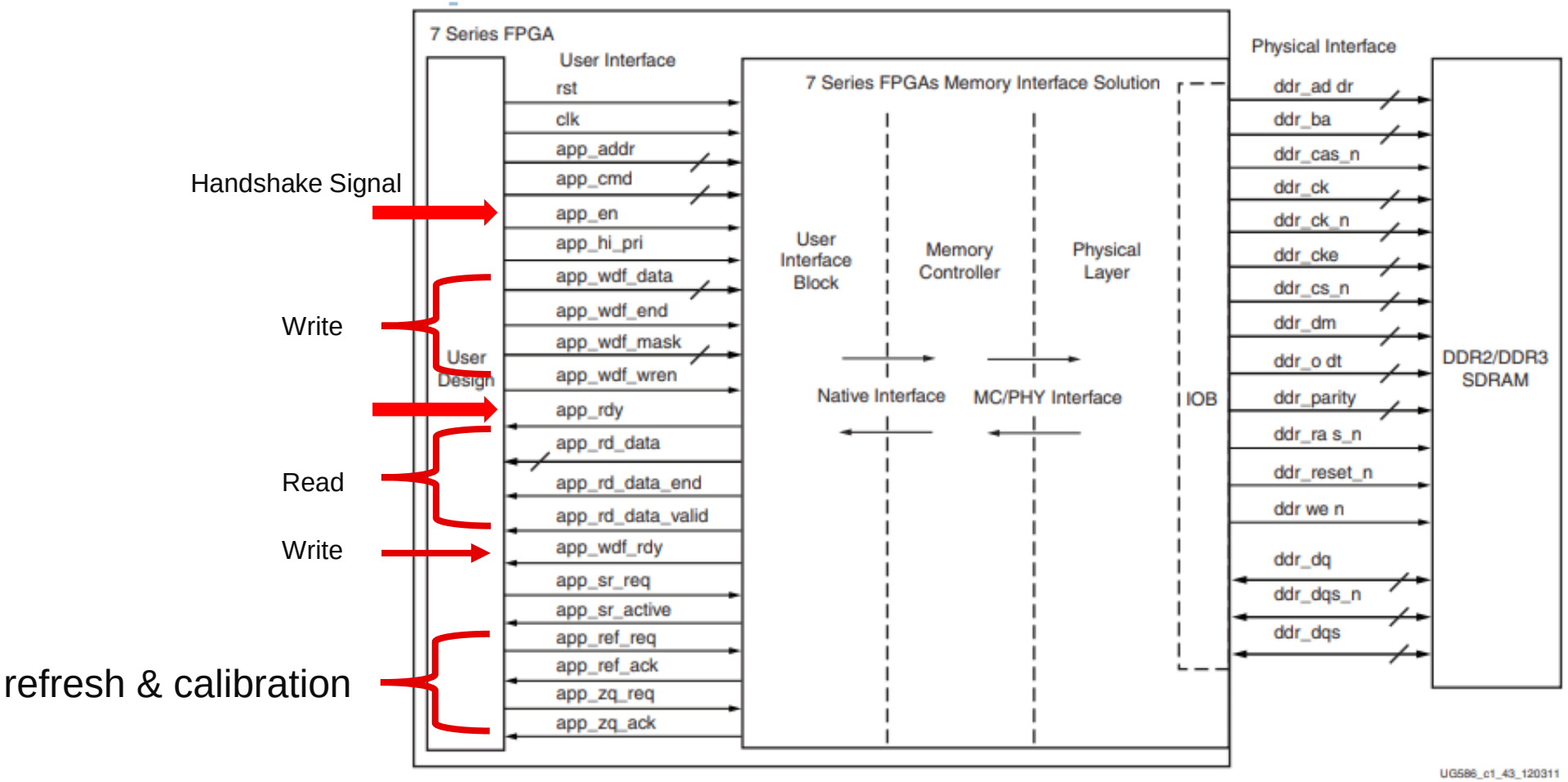

Figure 1-31: **7 Series FPGAs Memory Interface Solution**

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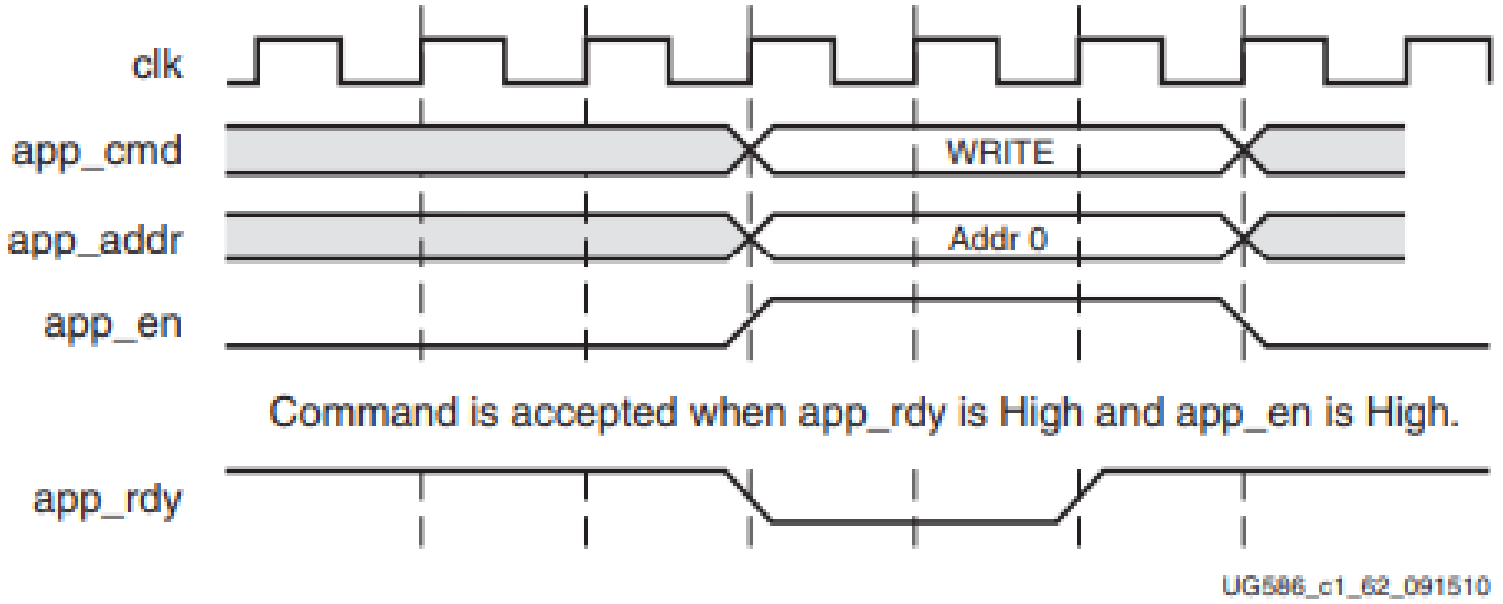
Command Path



Write Path

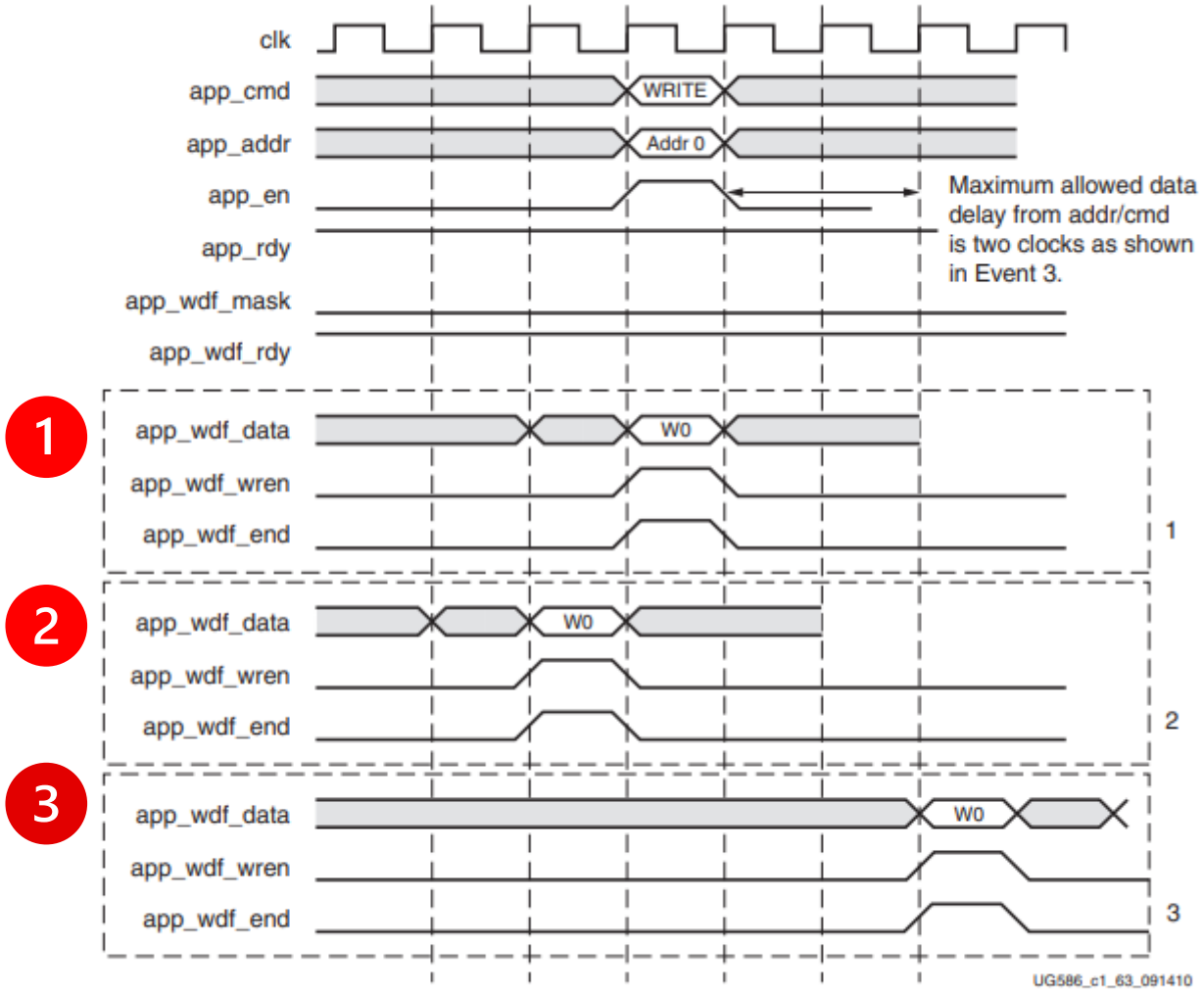


Figure 1-54: **4:1 Mode UI Interface Write Timing Diagram (Memory Burst Type = BL8)**

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Read Path

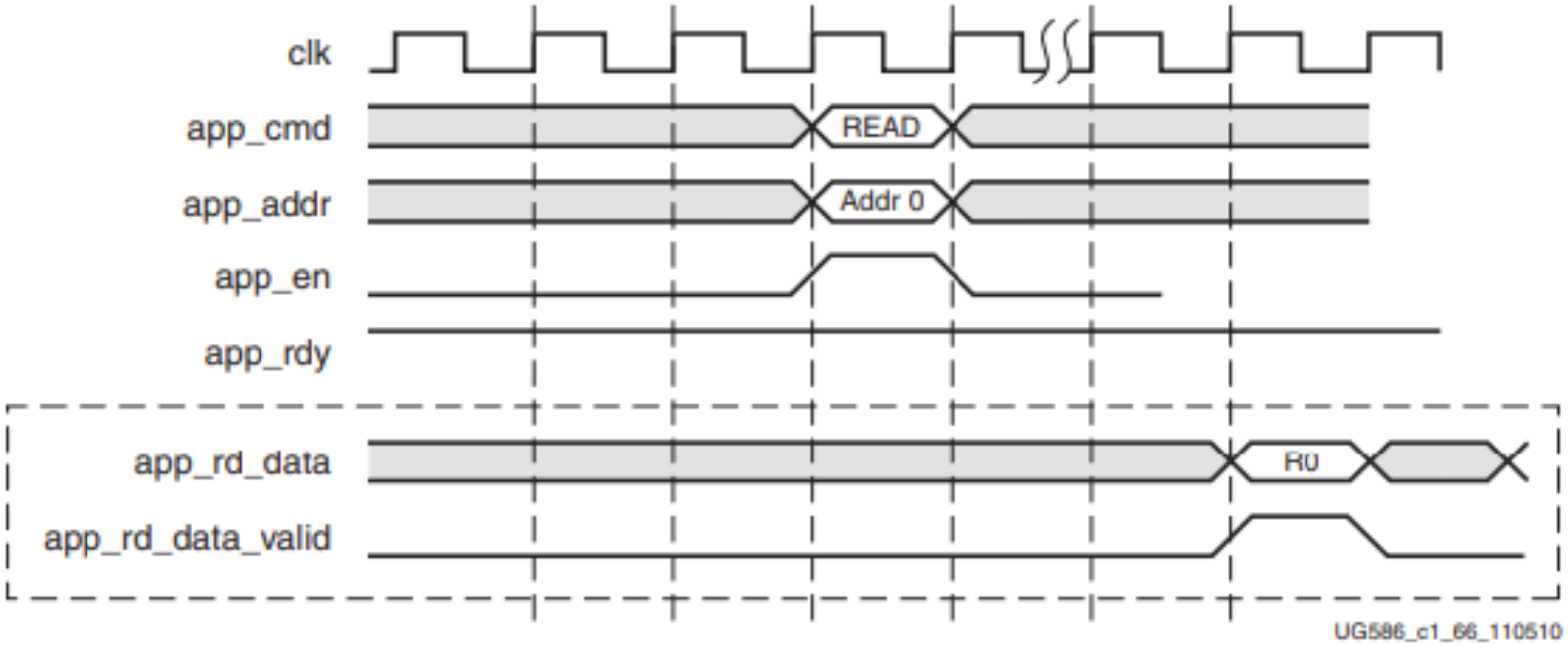

Figure 1-60: **4:1 Mode UI Interface Read Timing Diagram (Memory Burst Type = BL8)**

User Refresh & User ZQ

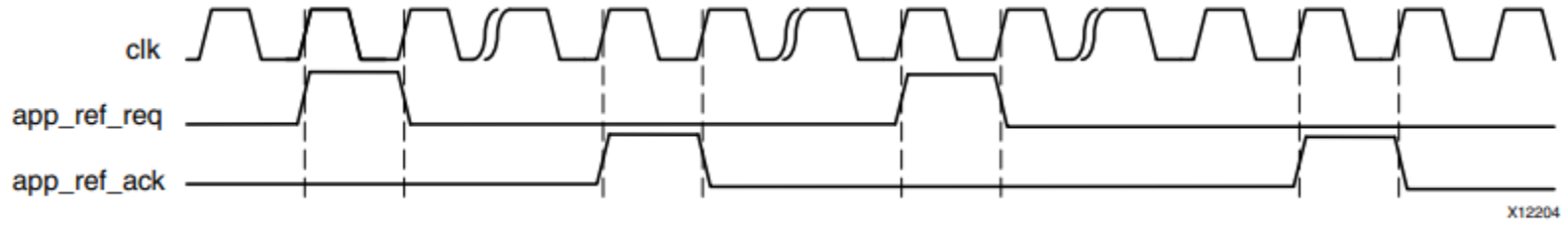

Figure 1-62: **User-Refresh Interface**

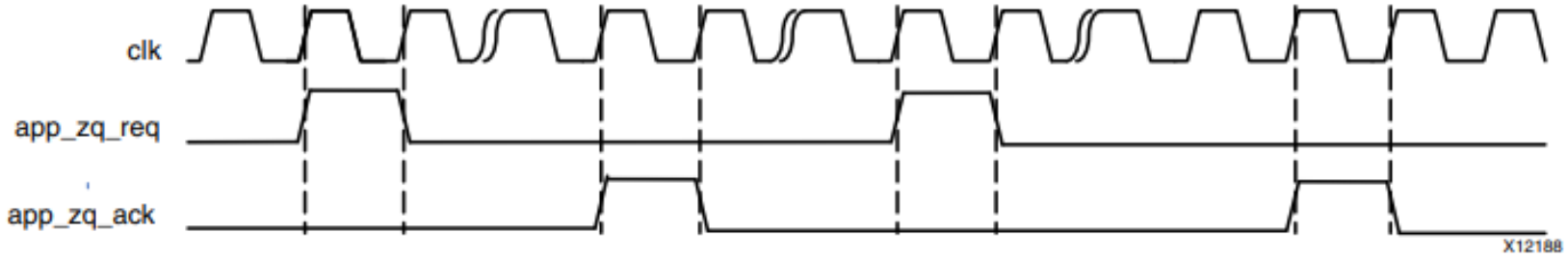

Figure 1-63: **User ZQ Interface**

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Calibration

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Calibration

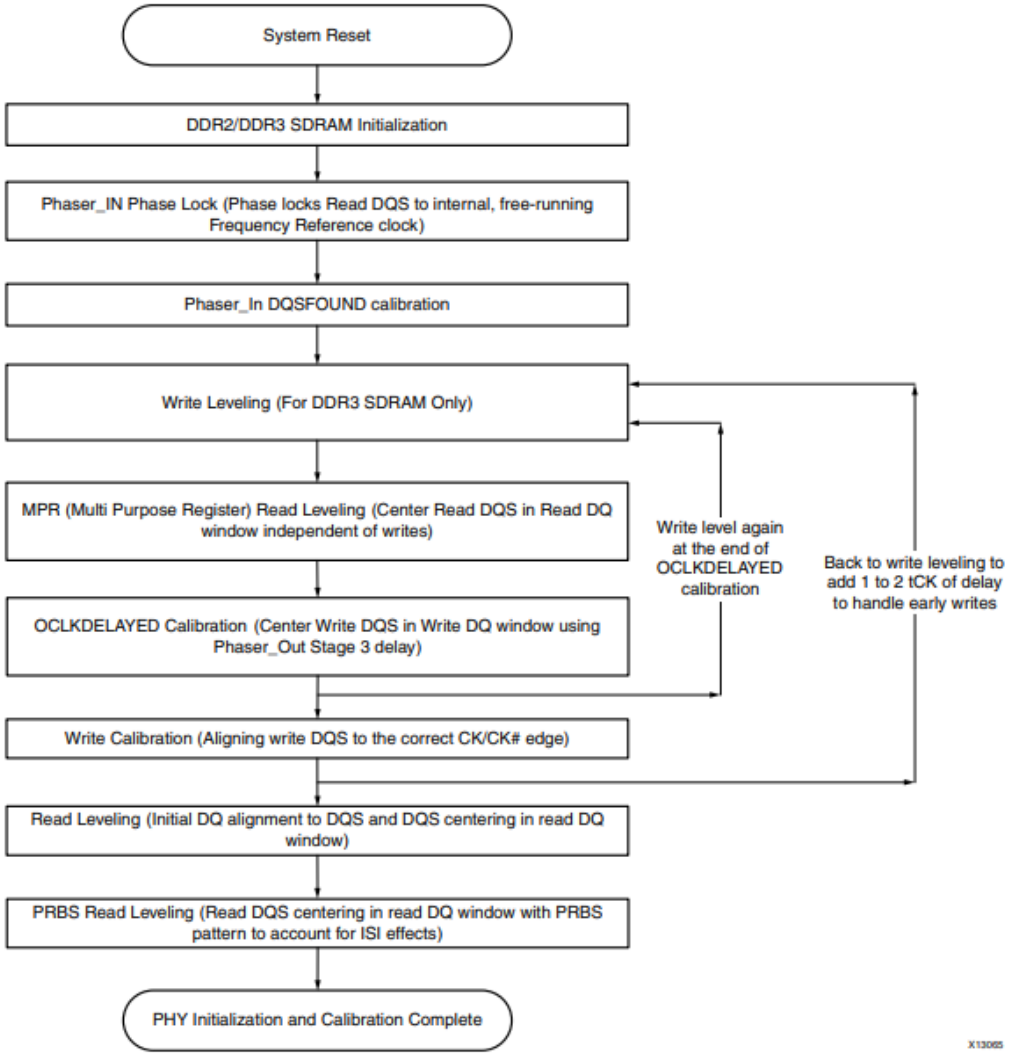
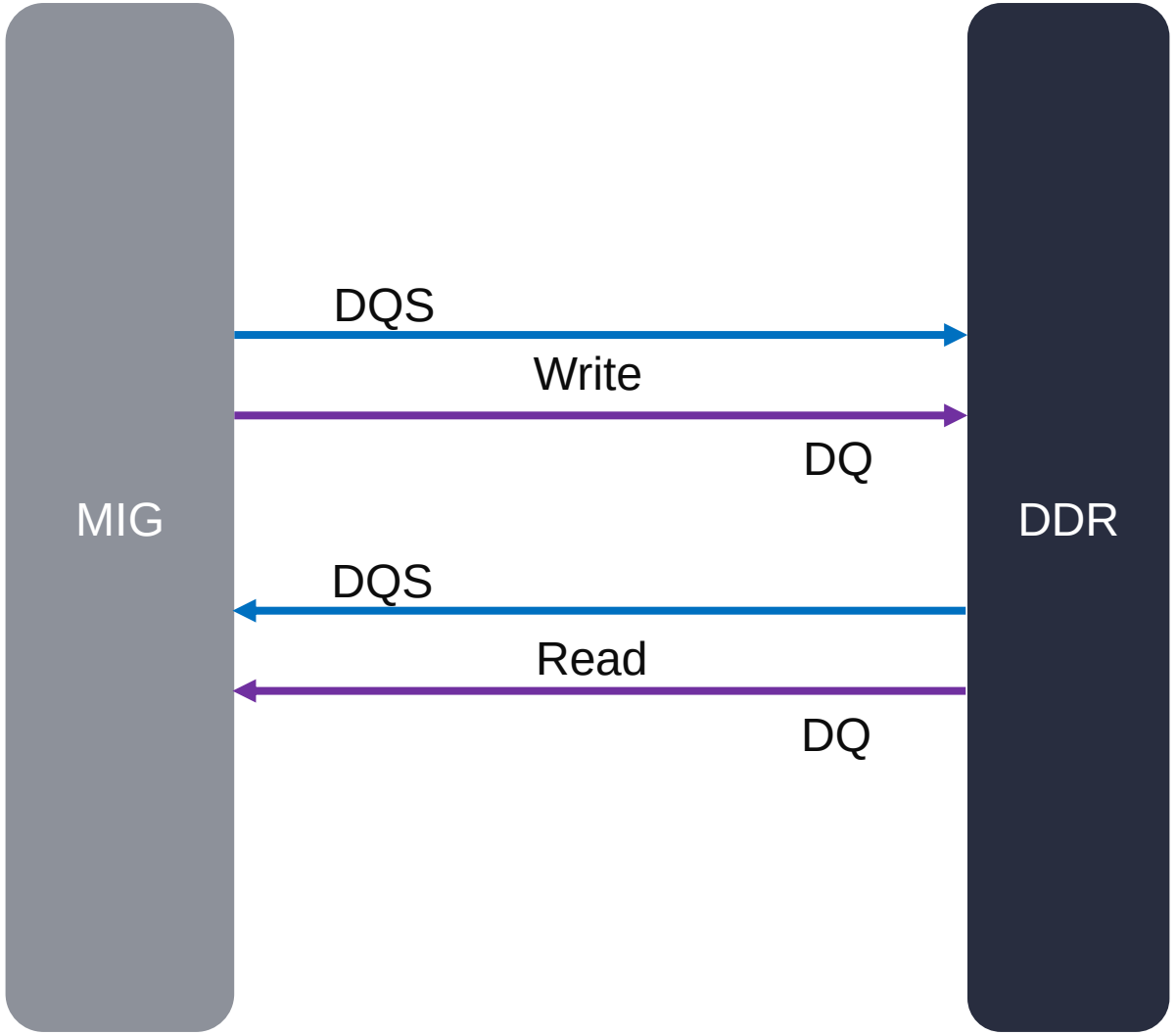
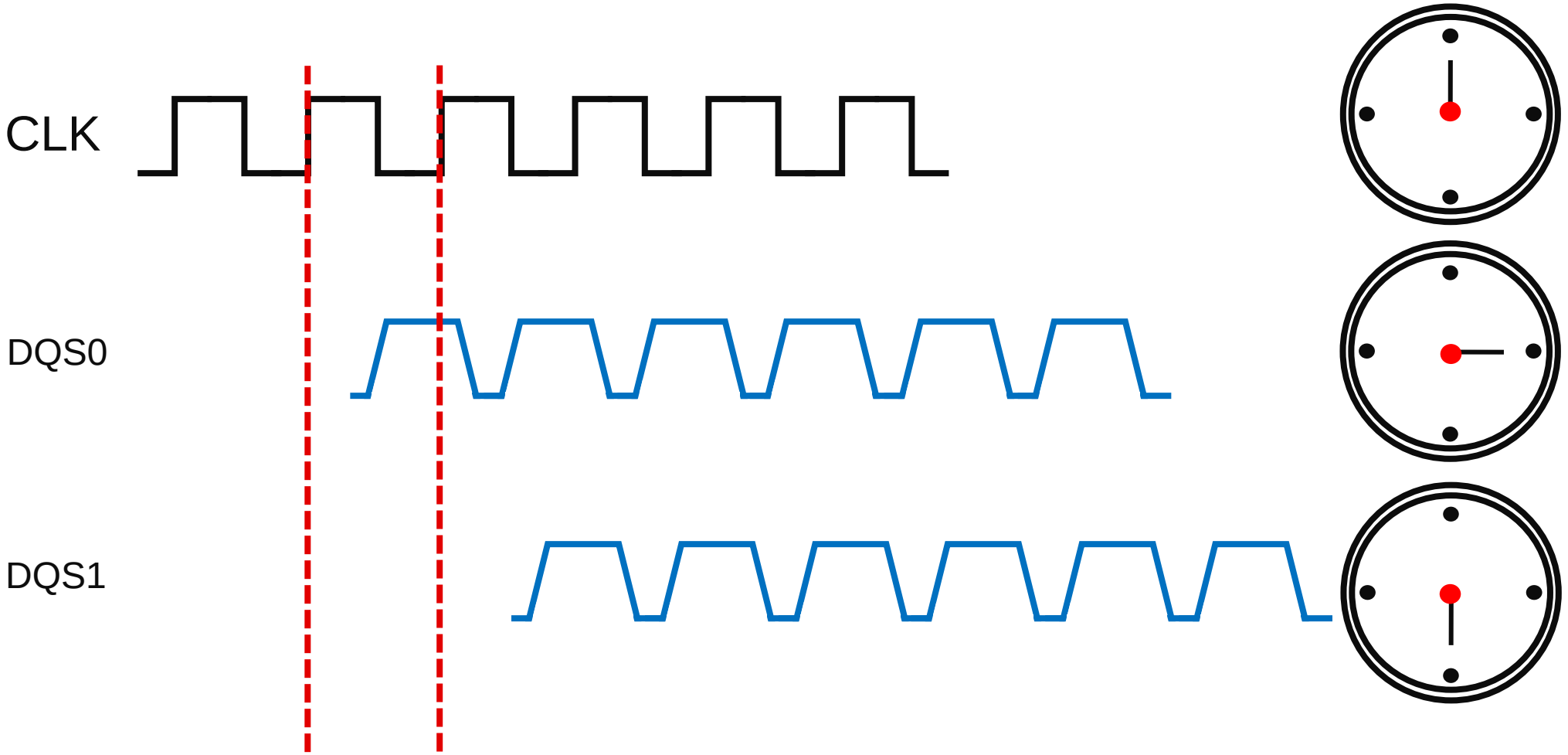


Figure 1-57: **PHY Overall Initialization and Calibration Sequence**

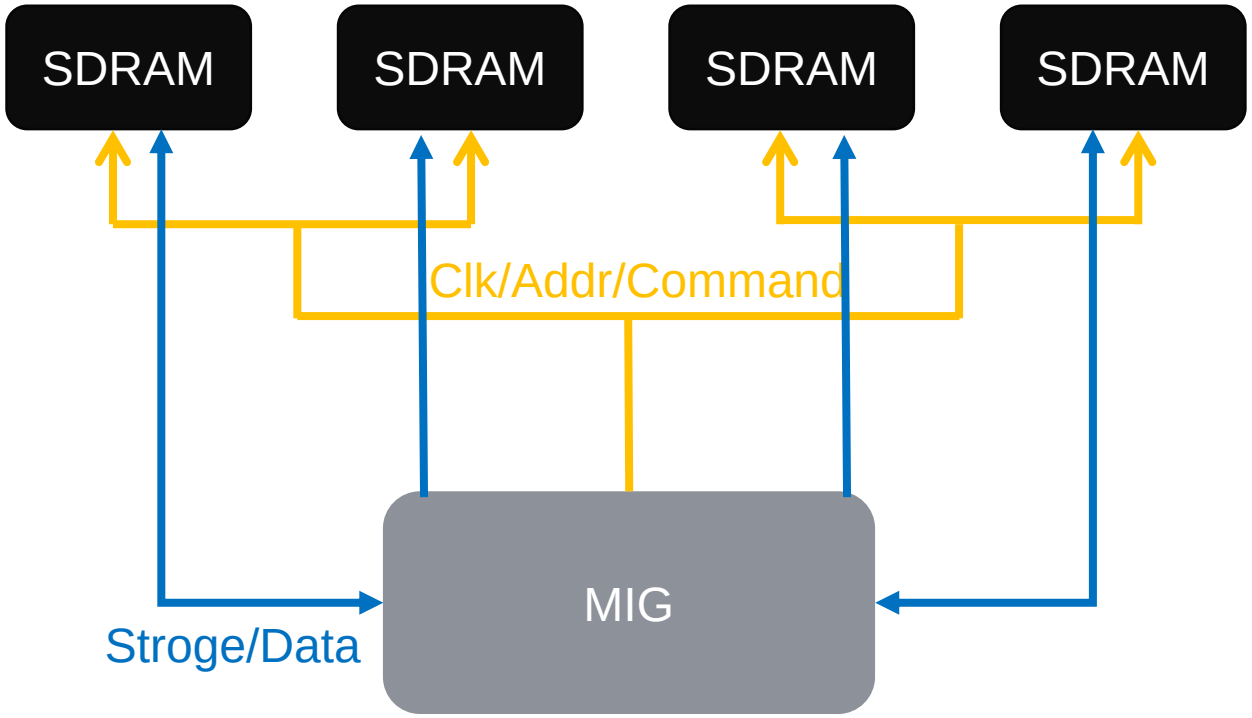


Phaser Lock



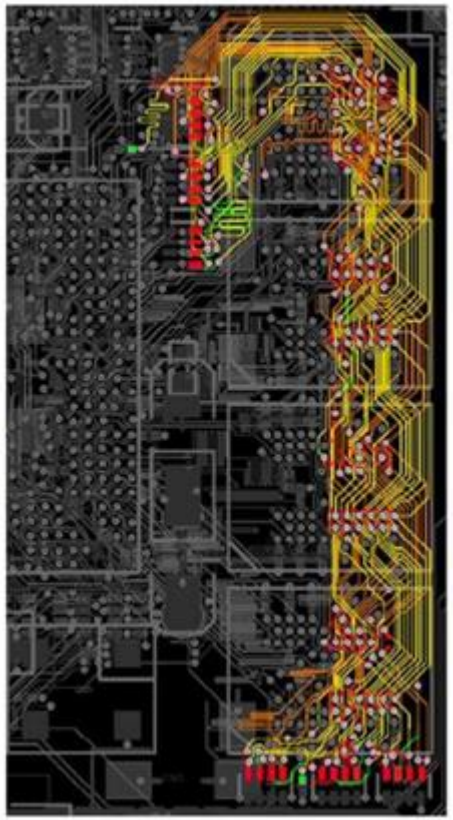
Write Leveling

T-topology

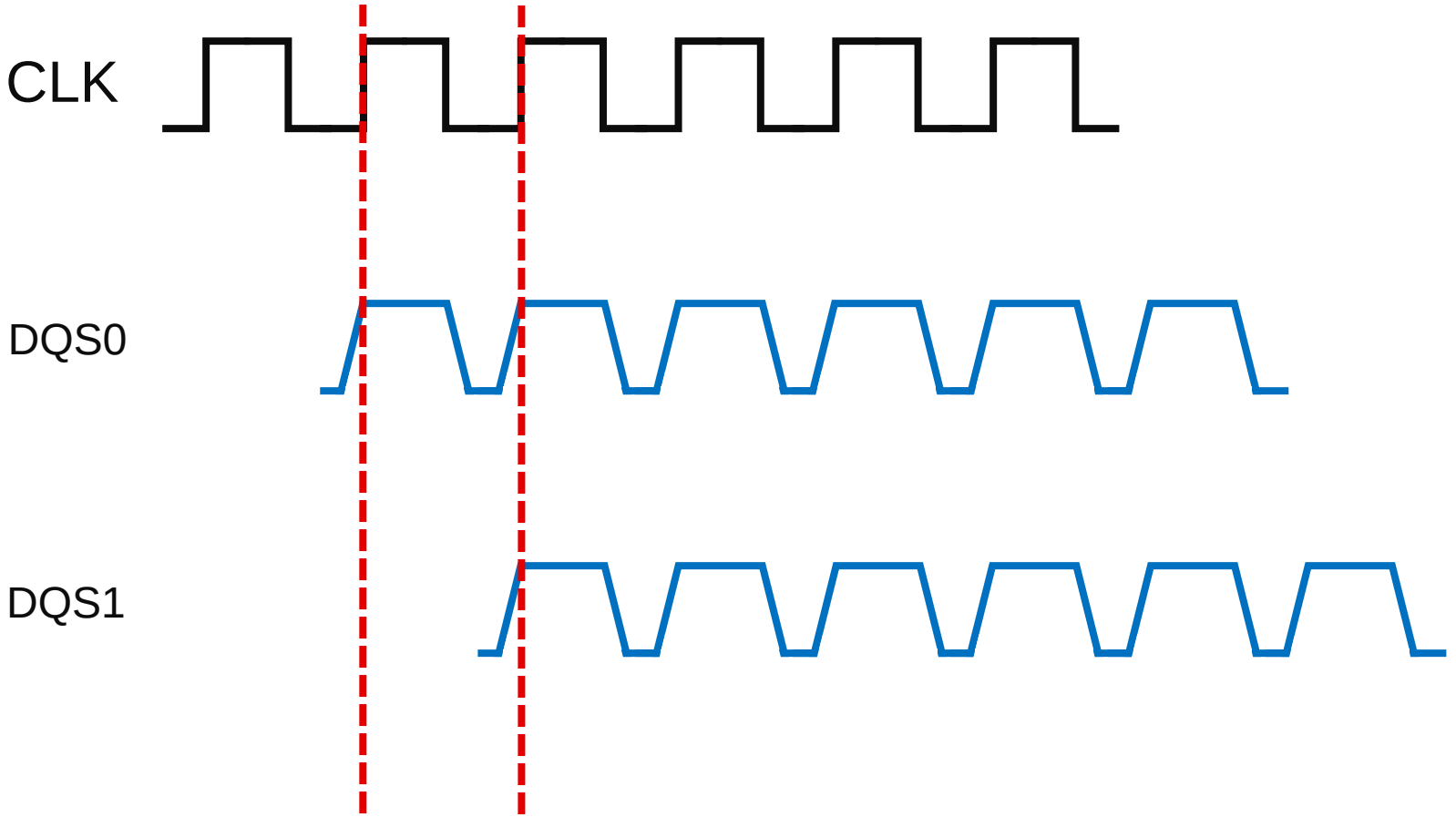


Write Leveling

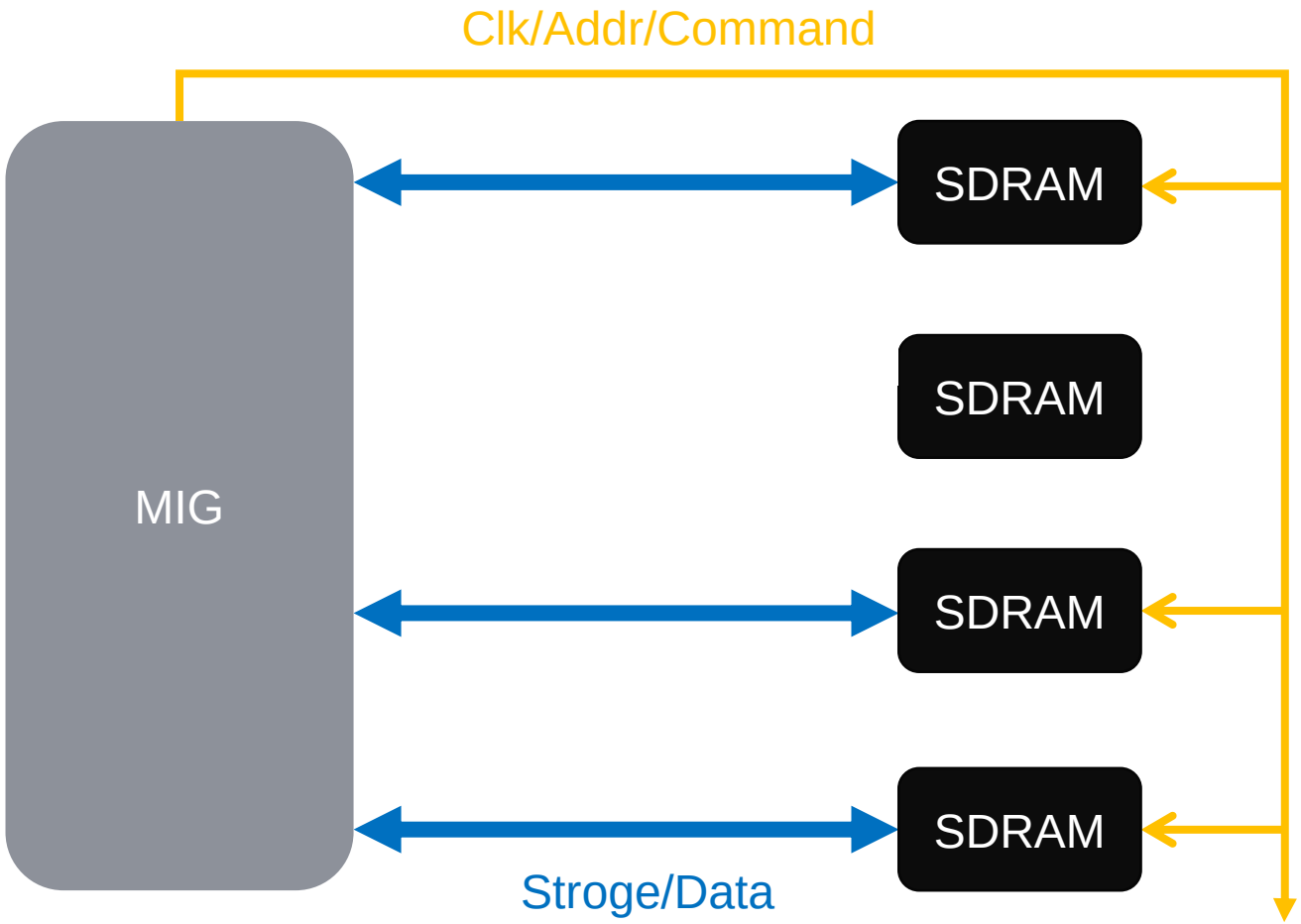
Fly-by



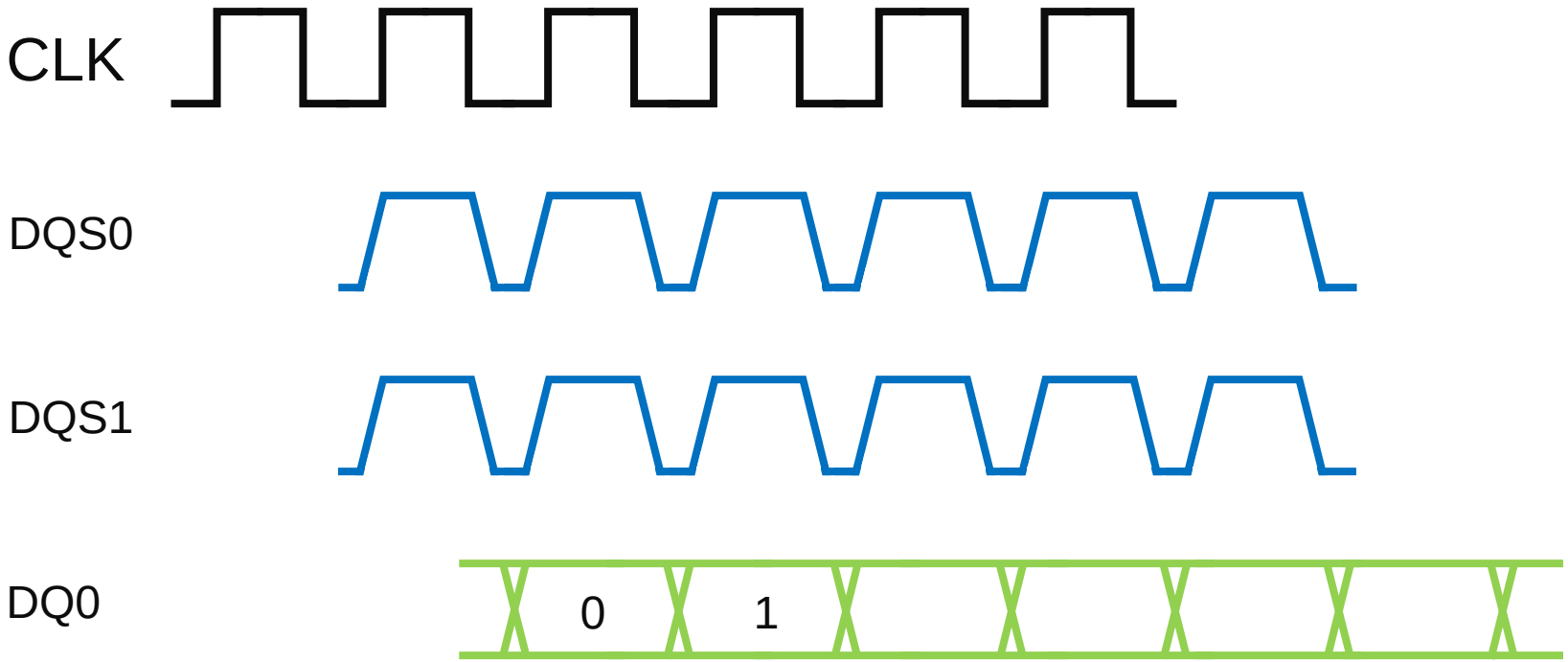
Write Leveling



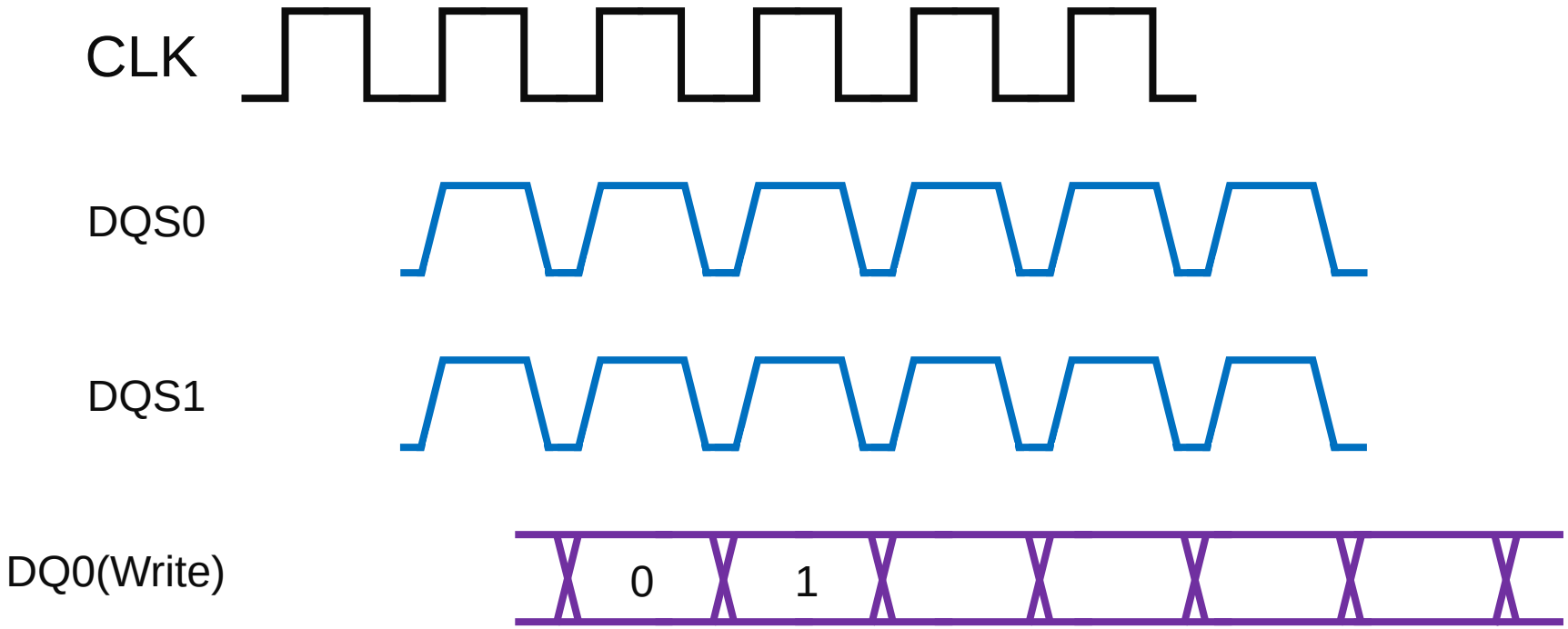
Read Leveling



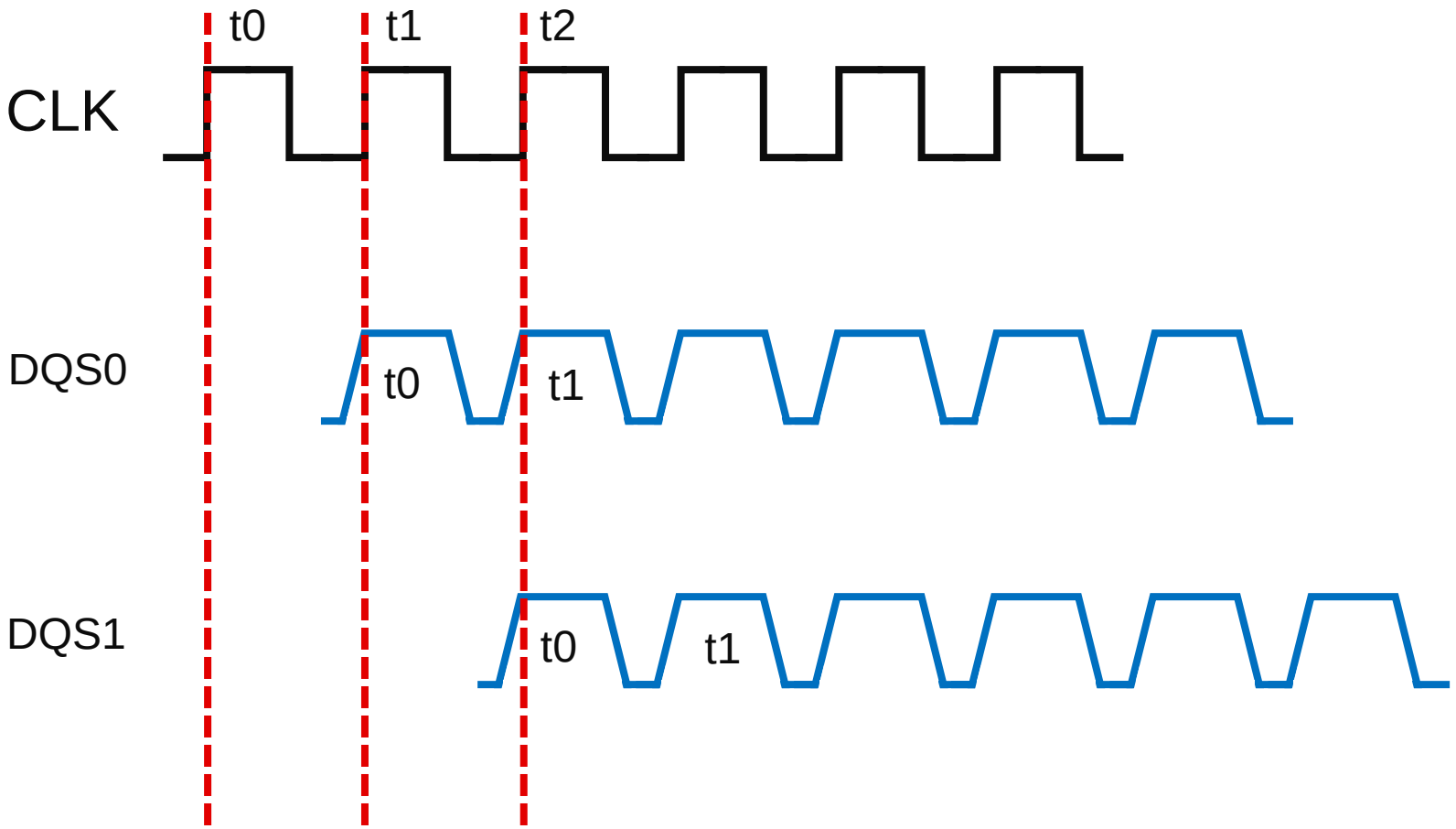
MPR Read Leveling



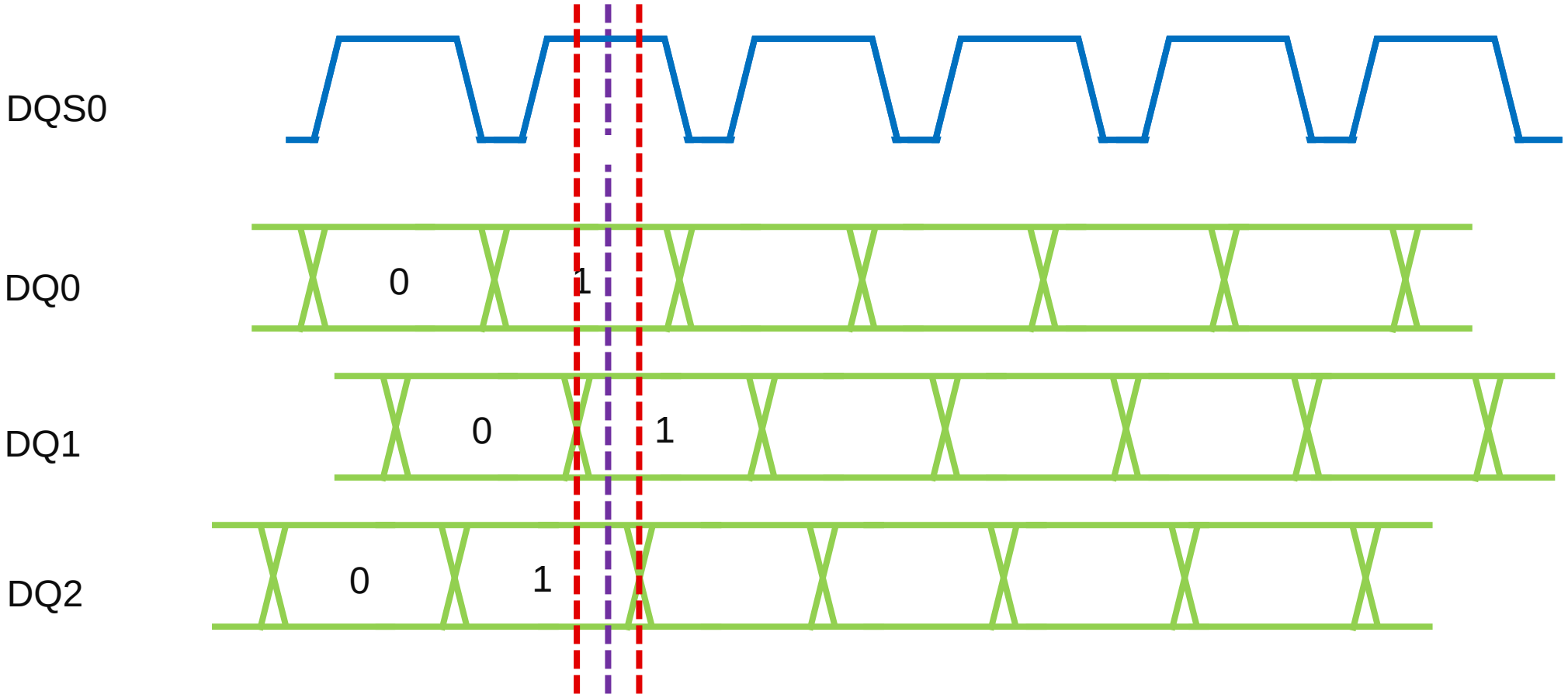
MPR Read Leveling



Write Calibration



Read Leveling & PRBS



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Conclusion

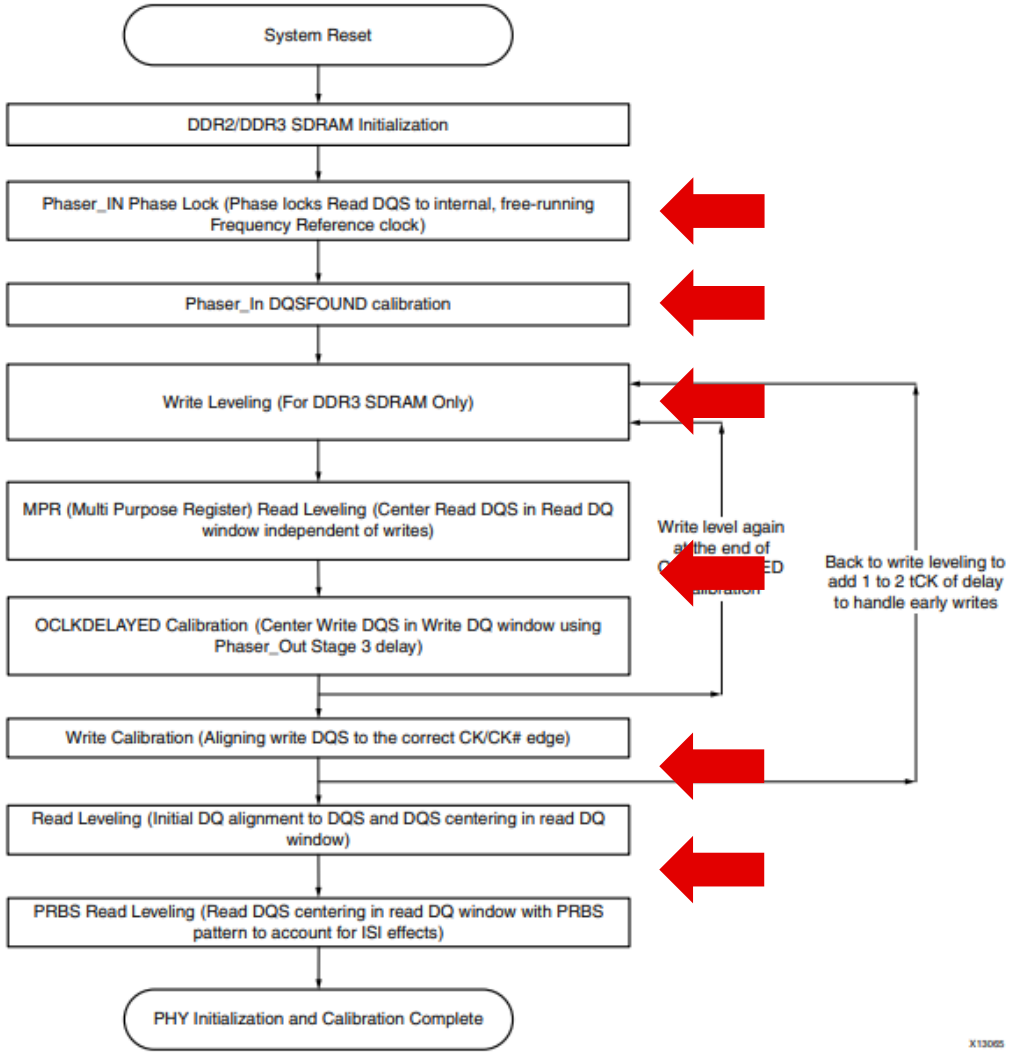
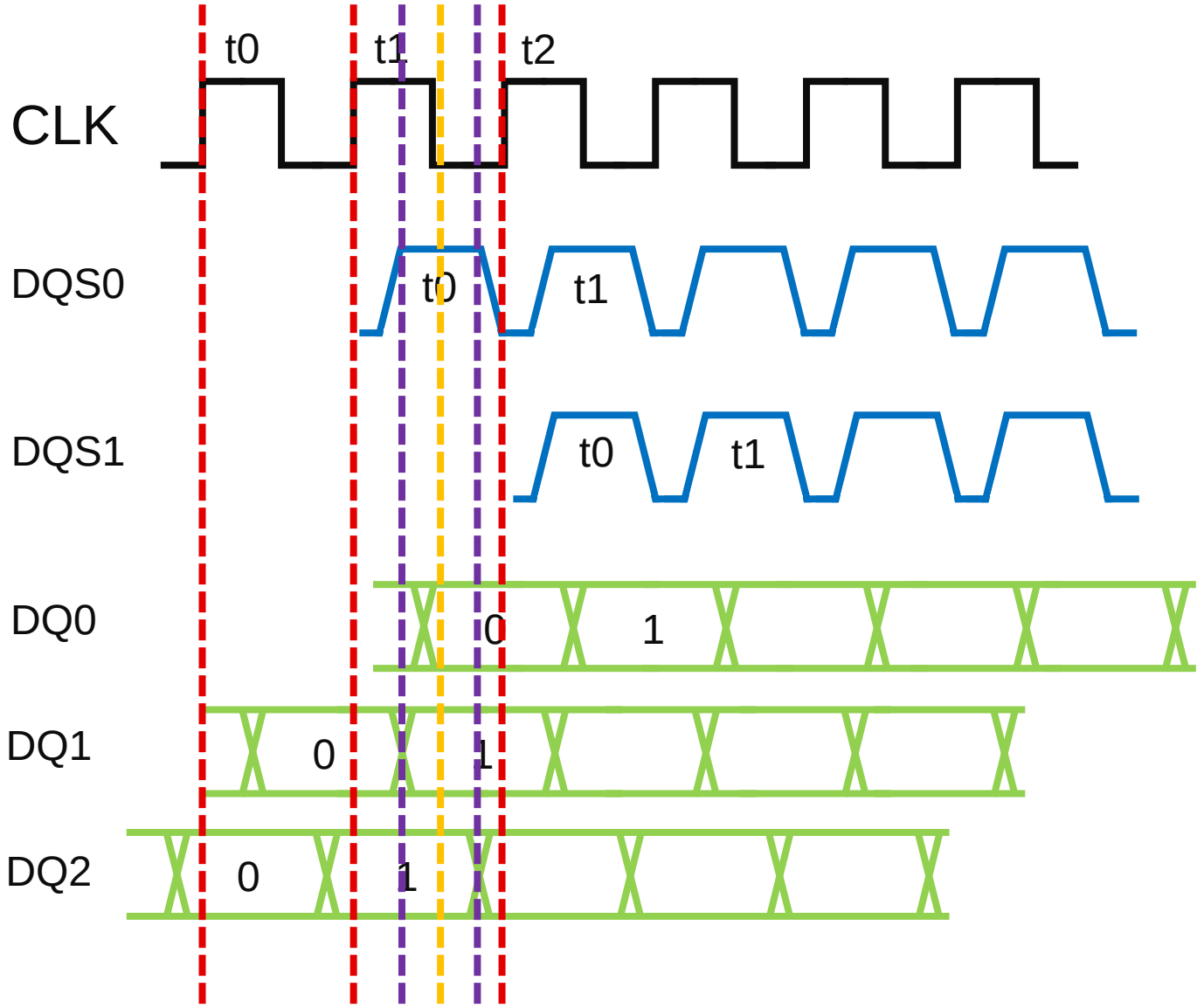


Figure 1-57: **PHY Overall Initialization and Calibration Sequence**



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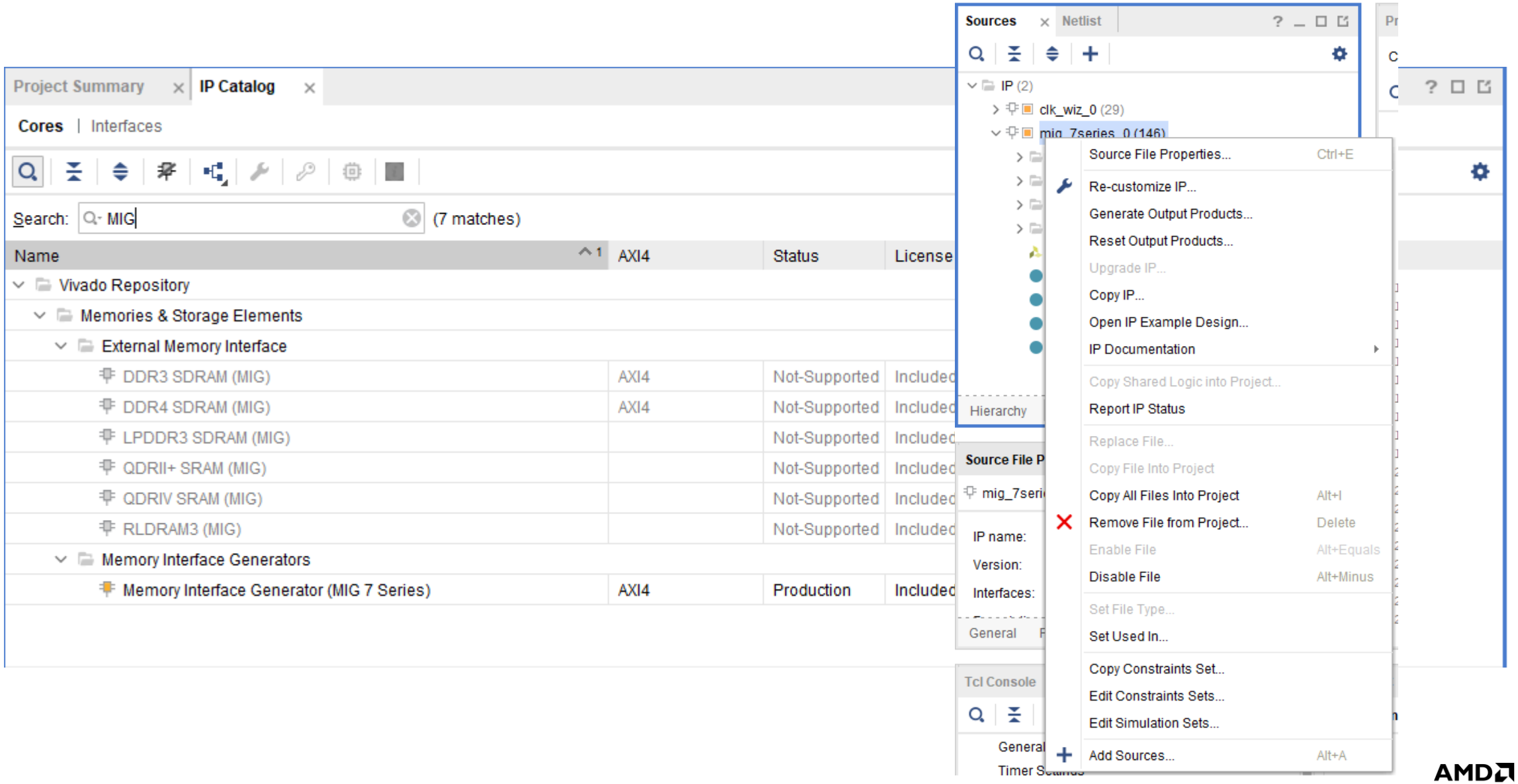
IP Example Design



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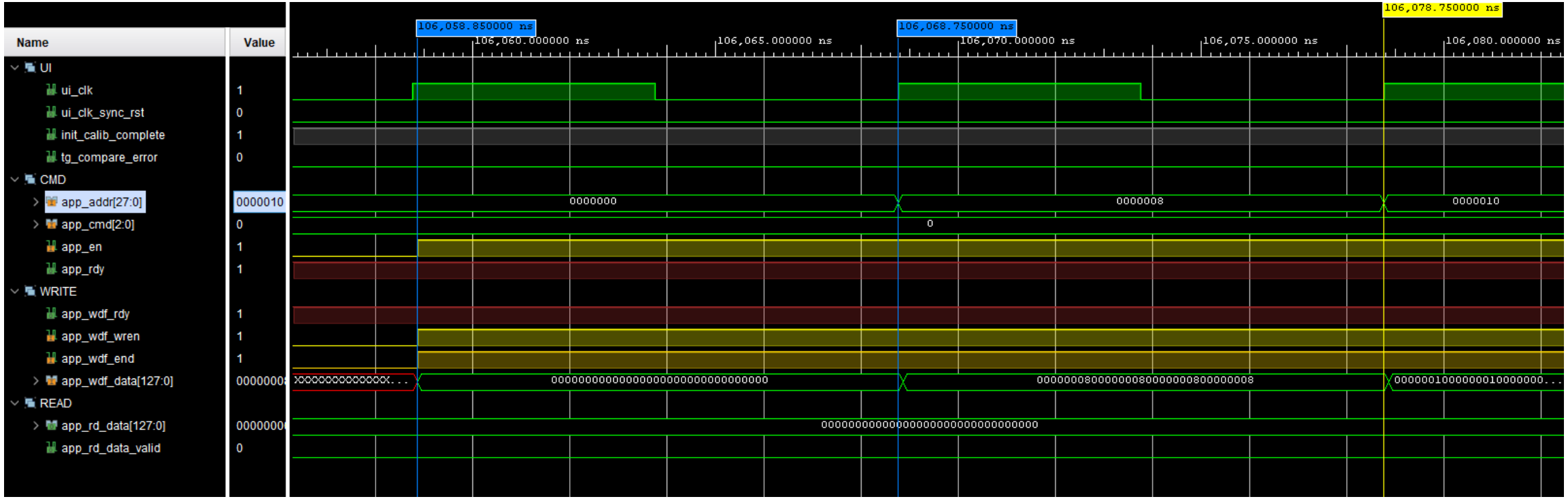
Example Design Simulation



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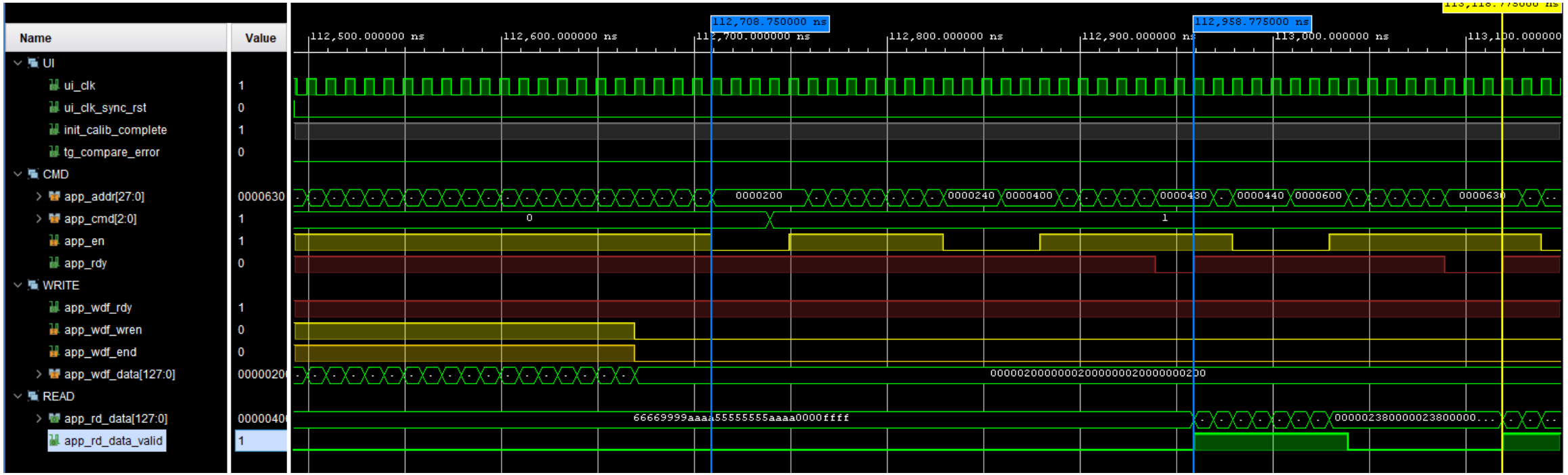
Example Design Simulation



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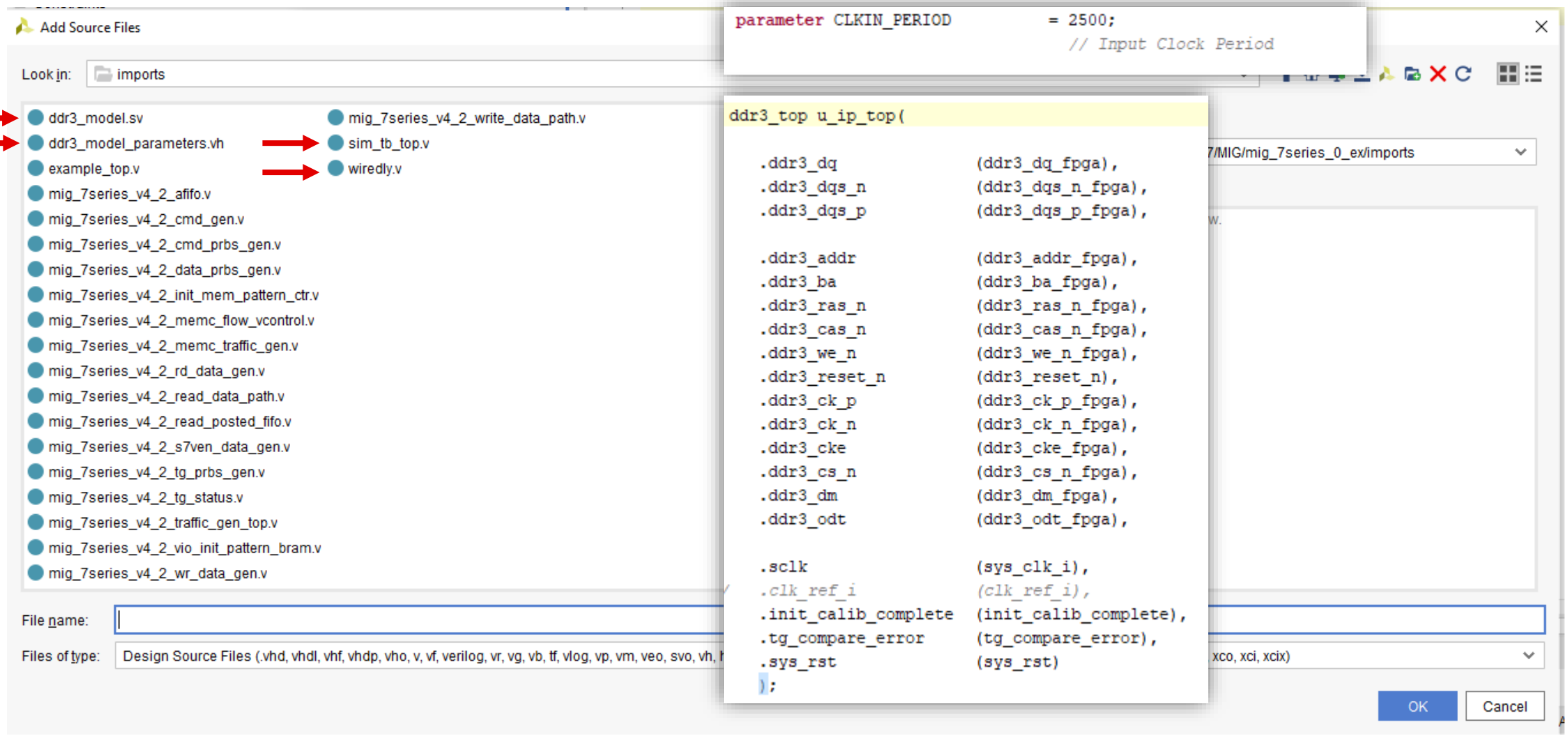
Simulation Setting



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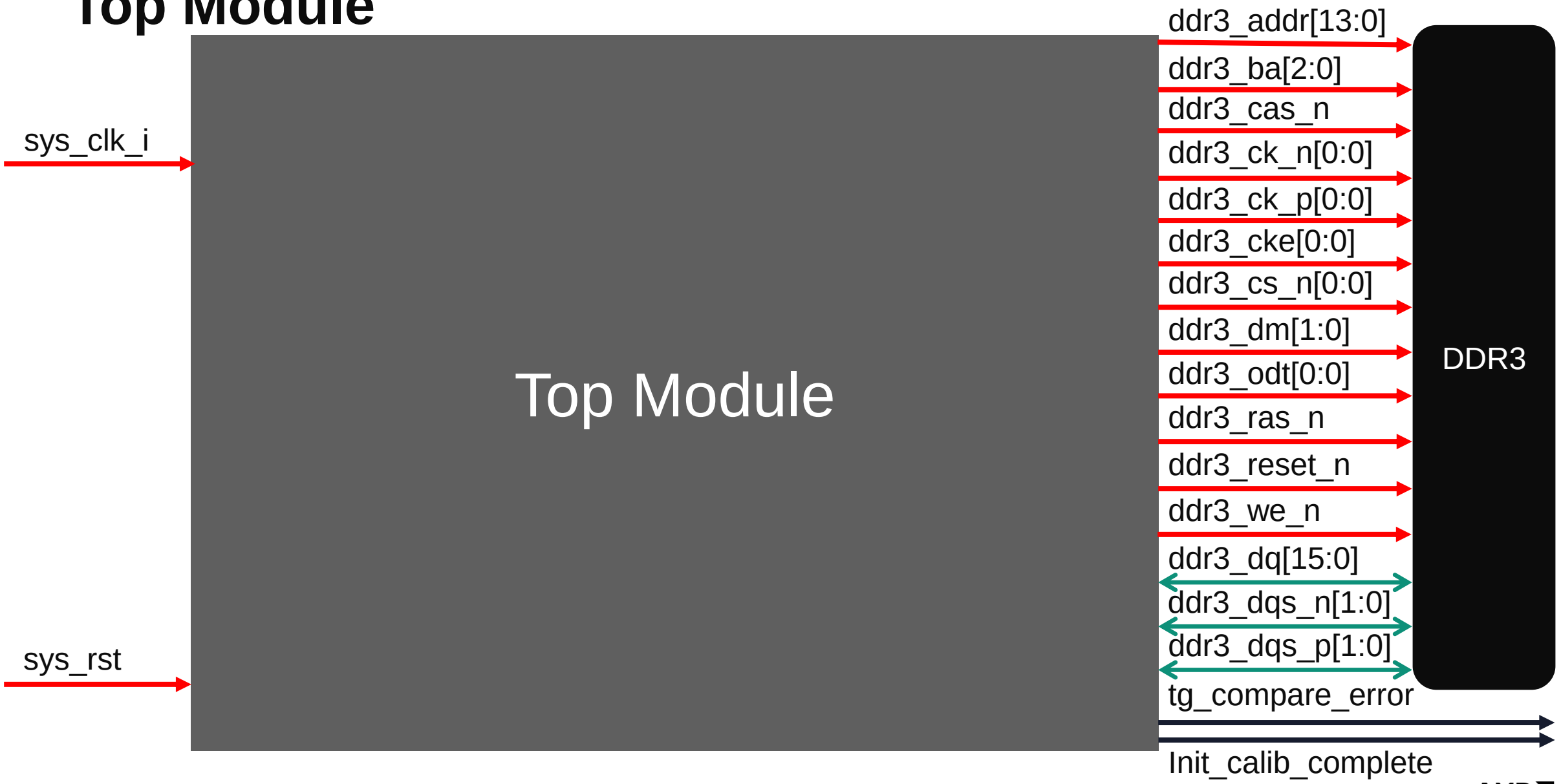
Top Module



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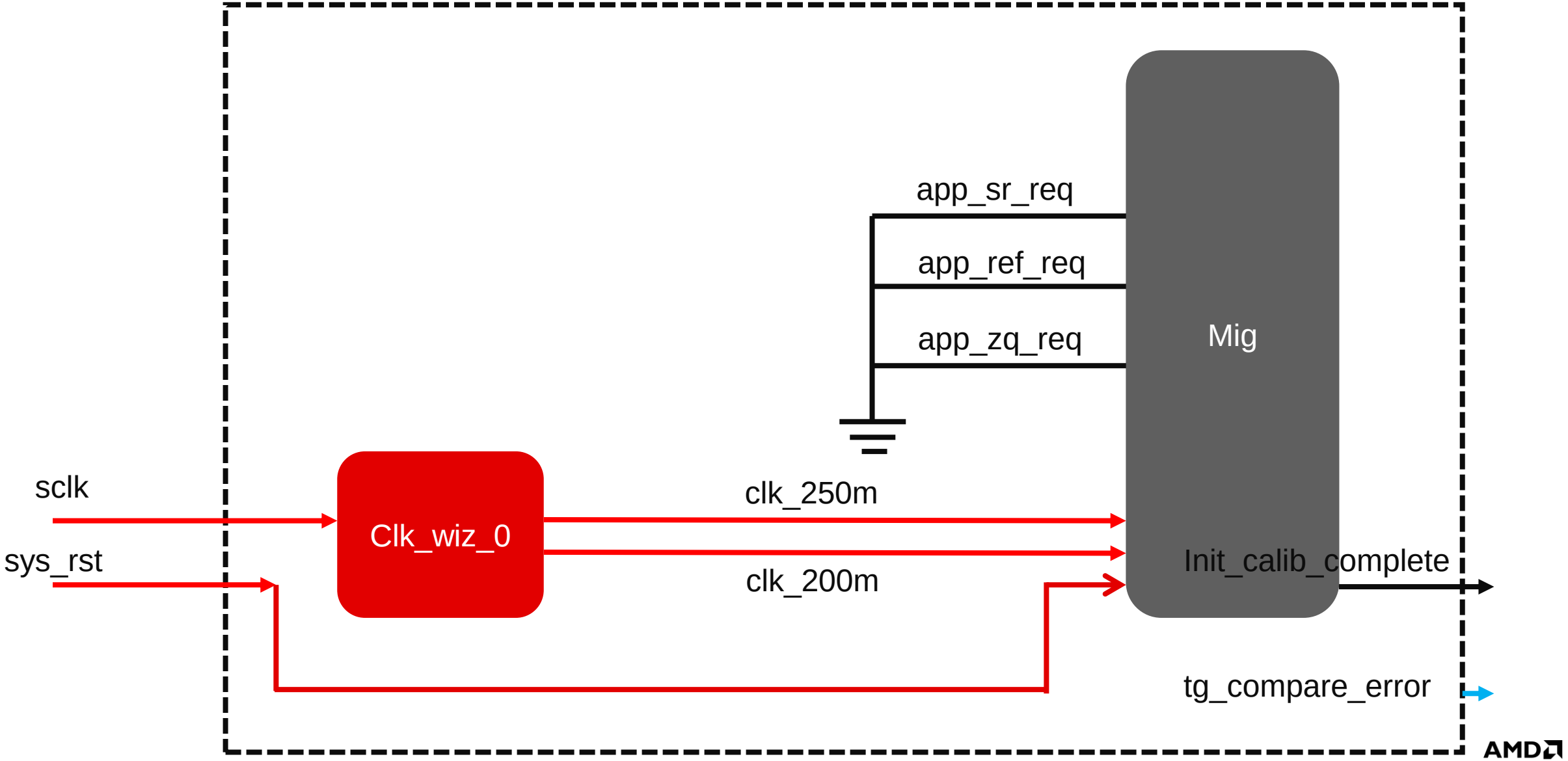
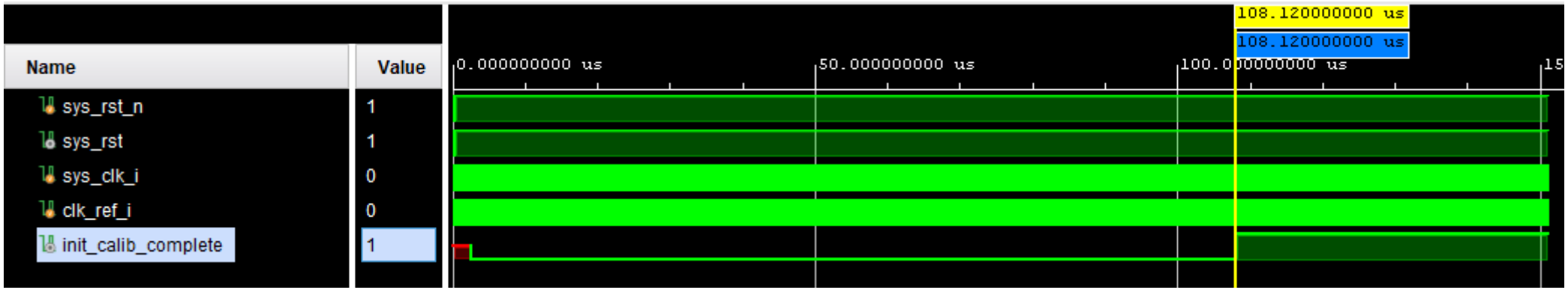
Simulation Setting



Simulation Setting



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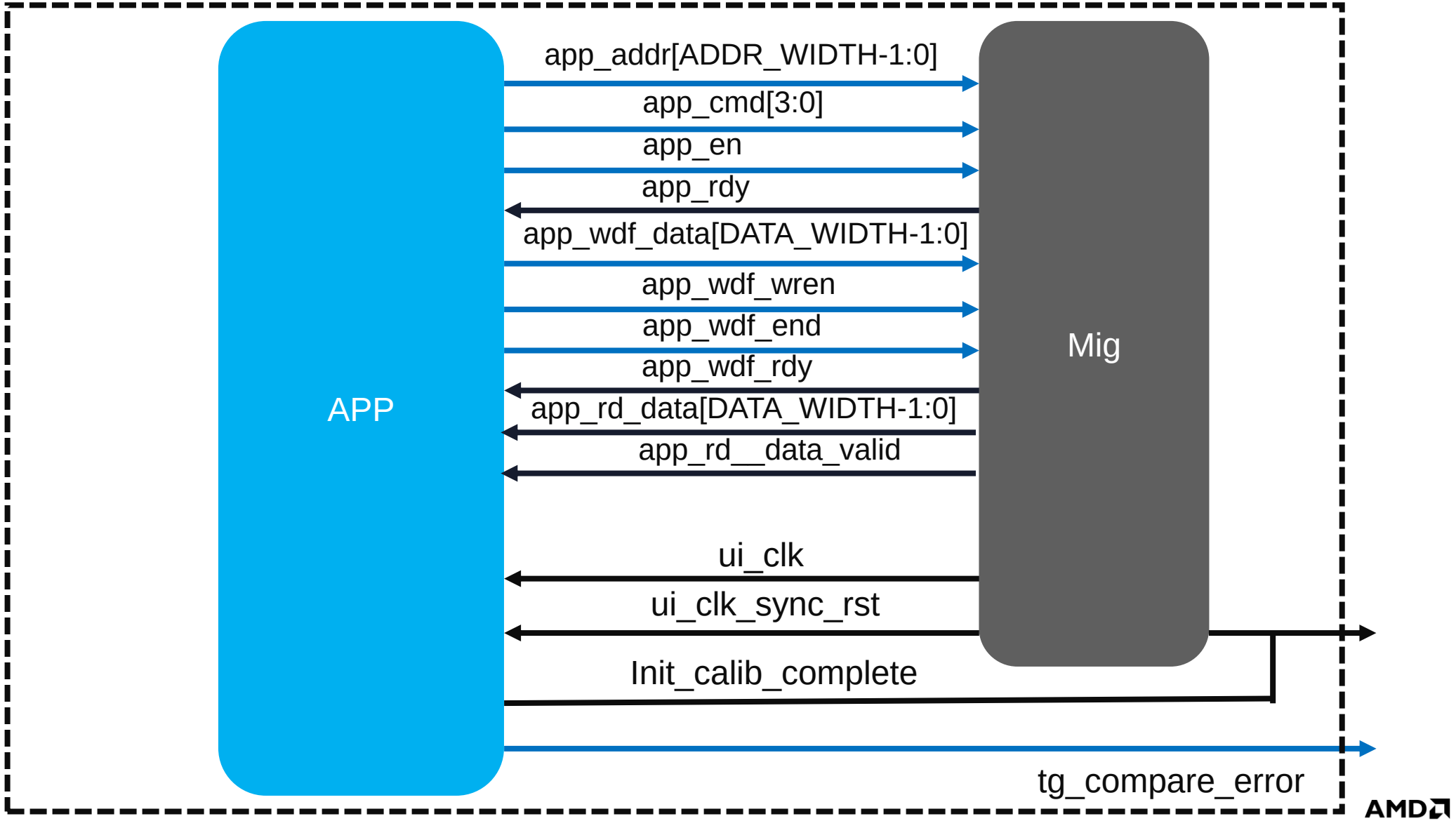
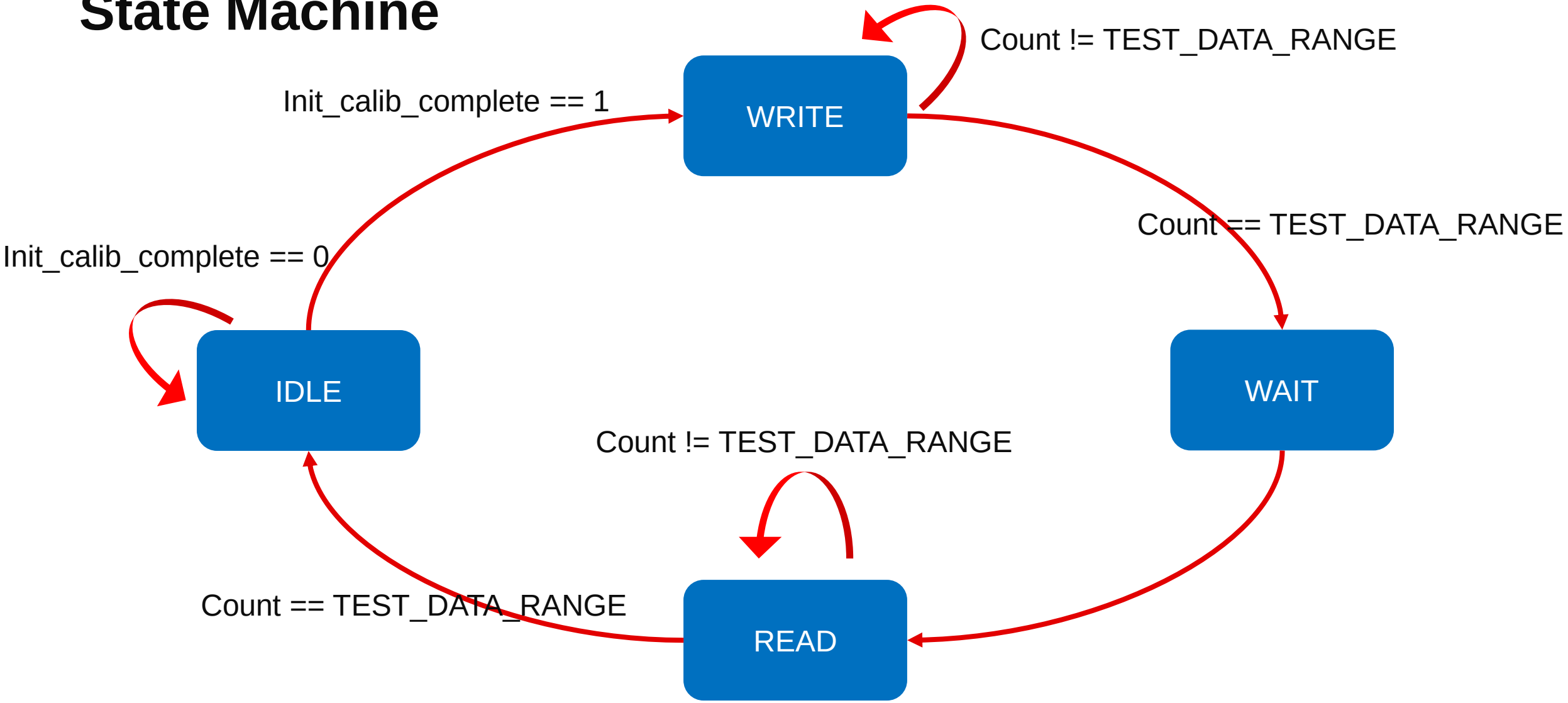
Application Interface



State Machine



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Thank you very much for your attention!

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