a place of mind

THE UNIVERSITY OF BRITISH COLUMBIA

ENGR 470: Microwave Engineering

School of Engineering

The University of British Columbia

Final Report: Microwave Amplifier Design

Presented to: Dr. Thomas Johnson

Submitted by:

Ana Ciocoiu	74255308
Hoda Dadashzadeh	71138689
Abdulwahab Elramali	48033154

Report submitted on: December 9th, 2019

Contents

Table of Figures

Table of Tables

Objectives

The goal of this lab is to design a working 1GHz amplifier using a NXP BFR520 NPN microwave transistor. The design will be implemented on a Rogers RO4350 substrate, and matching circuits are implemented using microstrip transmission lines. The design requirements for the amplifier are summarized in Table 1 below.

Table 1:Design Requirements

centre frequency	f_c: 1 GHz
bandwidth	f_b: 200 MHz
mid-band transducer gain at f_c	> 14.5 dB
$\|S_{11}\|$ over $[f_c - f_b/2, f_c + f_b/2]$	< -11 dB
$\|S_{22}\|$ over $[f_c - f_b/2, f_c + f_b/2]$	< -11 dB
input port connector	50 ohm female SMA connector
output port connector	50 ohm female SMA connector
base bias supply	variable voltage source
collector bias supply	variable voltage source
Substrate	Rogers RO4350
	Thickness: 0.030" (0.762 mm)
	Copper thickness (1 oz): 0.0014" (35.5 μm)
	Permittivity (measured at 2.5 GHz): 3.7
	Loss Tangent (measured at 2.5 GHz): 0.0031
Board Size	4 cm by 8 cm
Plated through vias	finished diameter of 0.43 mm

Theoretical Approach

Initially, the S-parameters for the transistor are obtained from the .s2p file in AWR. These are summarized in the table below.

Table 2: S-Parameters

S-Parameter	Magnitude	Angle (degree)
S11	0.135	-137.3
S21	4.799	83.4
S12	0.114	73.2
S22	0.365	-30.5

Assuming that stability conditions are met, the amplifier parameters can now be determined. Maximum gain will be realized when there is a conjugate match between the amplifier source or load impedance and the transistor.

Conjugate Matching

Maximum power transfer from the input matching network to the transistor will occur when:

$$\Gamma_{in} = \Gamma_s^*$$

Maximum power transfer from the transistor to the output matching network will occur when:

$$\Gamma_{out} = \Gamma_L^*$$

The matches will not be independent of each other for a bilateral ($S_{21} \neq 0$) transistor, so one match will affect the other. The matches must be done simultaneously.

To this effect, equations are derived as a function of the transistor S-Parameters, related to the reflection coefficients of the source and load. The goal of these equations is to show the dependence of the load reflection coefficient on the load reflection coefficient and vice versa.

For reference, the schematic of a two-port network is provided:

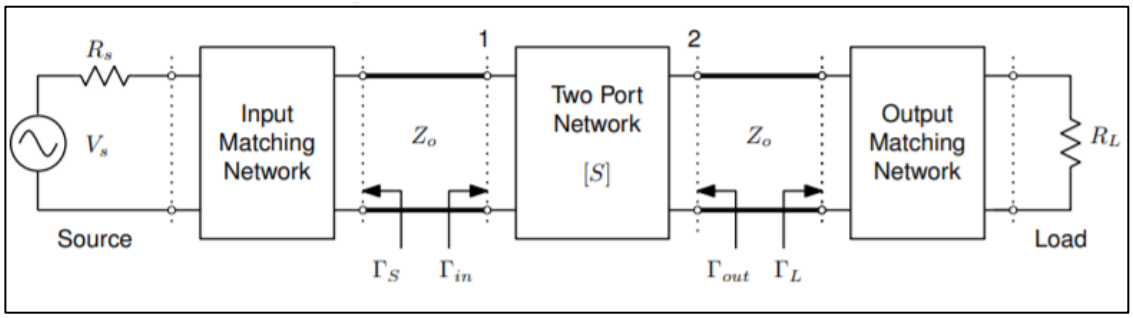


Figure 1: Two-port network

We can derive the equations that show interdependence between input and output reflection coefficients to derive the necessary values for Γ_L and Γ_S for use in the matching circuit. From the schematic above:

$$\Gamma in = \frac{V_1^-}{V_1^+} \text{ (1)} \qquad \Gamma out = \frac{V_2^-}{V_2^+} \text{ (2)} \qquad \Gamma s = \frac{V_1^+}{V_1^-} \text{ (3)} \qquad \Gamma_L = \frac{V_2^+}{V_2^-} \text{ (4)}$$

And
$$\begin{aligned} V_1^- &= S_{11}V_1^+ + S_{12}V_2^+ \\ V_2^- &= S_{21}V_1^+ + S_{22}V_2^+ \end{aligned} \quad (5)$$

Substituting (3) and (4) into (5) gives:

$$\begin{aligned} \frac{V_1^+}{\Gamma_s} &= S_{11}V_1^+ + S_{12}V_2^+ \\ \frac{V_2^+}{\Gamma_L} &= S_{21}V_1^+ + S_{22}V_2^+ \end{aligned} \quad (6) \qquad \text{and} \qquad \begin{aligned} V_1^+ &= \frac{S_{12}V_2^+\Gamma_s}{(1-S_{11}\Gamma_s)} \\ V_2^+ &= \frac{S_{21}V_1^+\Gamma_L}{(1-S_{22}\Gamma_L)} \end{aligned} \quad (7)$$

Substituting (7) back into (3) and (4) gives:

$$\Gamma out = \frac{S_{22} - \Gamma s\Delta}{1-\Gamma s S_{11}} \qquad \text{and} \qquad \Gamma in = \frac{S_{11} - \Gamma_L\Delta}{1-\Gamma_L S_{22}} \qquad (8)$$

Where $\Delta = S_{11}S_{22} - S_{12}S_{21}$ (9)

With further simplifications (see Chapter 12, Pozar) , the values necessary for Γs and Γ_L can be found:

$$\Gamma s = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1}, \Gamma_L = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \quad (10)$$

Where:

$$\begin{aligned} B_1 &= 1 + |S_{11}|^2 - |S_{22}|^2 - |\Delta|^2 \\ B_2 &= 1 + |S_{22}|^2 - |S_{11}|^2 - |\Delta|^2 \\ C_1 &= S_{11} - \Delta S_{22}^* \\ C_2 &= S_{22} - \Delta S_{11}^* \end{aligned} \quad (11)$$

These parameters are calculated using a MATLAB script and are found to be:

Γ_L = 0.6632 + 0.4883i and Γs = -0.7181 + 0.2629i

These are the values needed for simultaneous conjugate matching.

The transducer gain can be defined as:

$$G_T = \frac{P_L}{P_{AVS}} = \frac{1-|\Gamma_S|^2}{|1-\Gamma_S S_{11}|^2}|S_{21}|\frac{1-|\Gamma_L|^2}{|1-\Gamma_{OUT}\Gamma_L|} \quad (12)$$

where P_L is the power delivered to the load, and P_{AVS} is the maximum power available from the source in the case of a conjugate match at the input port.
In the case of a simultaneous conjugate match at both ports, $\Gamma_{in} = \Gamma_s^*$ and $\Gamma_{out} = \Gamma_L^*$,

$$G_T = \frac{P_L}{P_{AVS}} = \frac{1-|\Gamma_S|^2}{|1-\Gamma_S S_{11}|^2}|S_{21}|\frac{1}{|1-|\Gamma_L|^2|} \quad (13)$$

Maximum Unilateral Transducer Power Gain

The transistor we are using is not unilateral, because S12 is non-zero. However, we can, for theoretical purposes, calculate what the values for the reflection coefficients should be in the case of a unilateral device.

The transducer power gain can be defined as:

Under the unilateral device conditions, we note that equation (8) reduces to:

$$\Gamma out = S_{22}$$
$$\Gamma in = S_{11}$$

For a conjugate match, we would need to pick Γ_L = S22* and Γs = S11*.

The maximum transducer power gain in the unilateral case will then reduce to:

$$G_T = \frac{P_L}{P_{AVS}} = \frac{1}{|1-|\Gamma_S|^2|}|S_{21}|\frac{1}{|1-|\Gamma_L|^2|} \quad (14)$$

These expressions are numerically evaluated in the following table.

Table 3: Design Summary

Description	Value (Mag/ Angle)	Value (dB)
Γ_S for maximum unilateral transducer power gain	0.135∡137.3	-17.4
Γ_L for maximum unilateral transducer power gain	0.365∡-30.5	-8.754
Maximum unilateral transducer power gain	27.07 W/W	14.33
Γ_S for simultaneous conjugate match	0.76∡160	-2.33
Γ_L for simultaneous conjugate match	0.82∡36.36	-1.72
Transducer power gain with simultaneous conjugate match	36.2 W/W	15.6
Γ_S for final design	0.315 ∡137.4	-10.03
Γ_L for final design	0.382 ∡47.62	-8.36

Where the final design values are the same as the conjugate match values: the conjugate match design was incorporated into a two-port network and connected to the transistor. Any further optimization dealt solely in input return loss, output return loss, and gain optimization for the transistor.

* Note: The reflection coefficient dB values for unilateral parameters were found by taking 20log() of the table 2 values.

The reflection coefficient dB values for conjugate match parameters were found by taking 20log() of the values below:

Γ_L = 0.6632 + 0.4883i and ΓS = -0.7181 + 0.2629i

Practical Approach

In AWR, simultaneous matching can be accomplished by using the following circuit. The end goal is to match the reflection coefficient looking into ports 1 and 2 to the values of Γs and Γ_L.

Since Γ_L falls in the upper right half of the Smith chart, it would make sense to move upwards along the 1+jb circle after starting from a reflection coefficient of 0 right at the load. This can be achieved using an inductive or short circuit shunt stub. Since Γs falls in the upper left half of the Smith chart, it would make sense to move downwards along the 1+jb circle. This can be achieved using a capacitive or shunt open-circuit stub. The length of the stubs is tuned so that we obtain the desired absolute value of reflection coefficients $|\Gamma s|$ and $|\Gamma_L|$. All that the following series transmission line adds is phase, which will bring us to the correct values for reflection coefficients. The circuit schematic and Smith charts for the initial matchings are provided below.

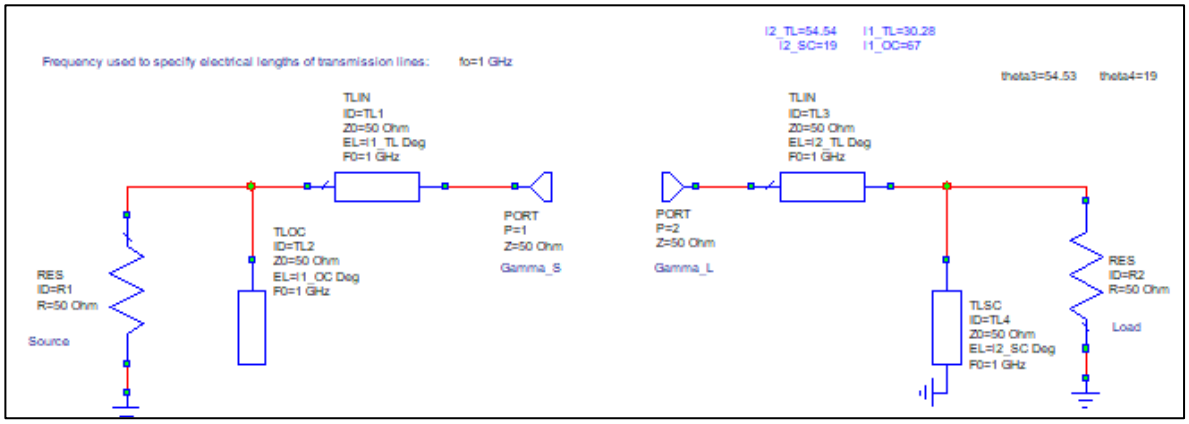


Figure 2: Simultaneous Matching Circuit

The electrical lengths for the transmission lines (TL) are shown in the table below.

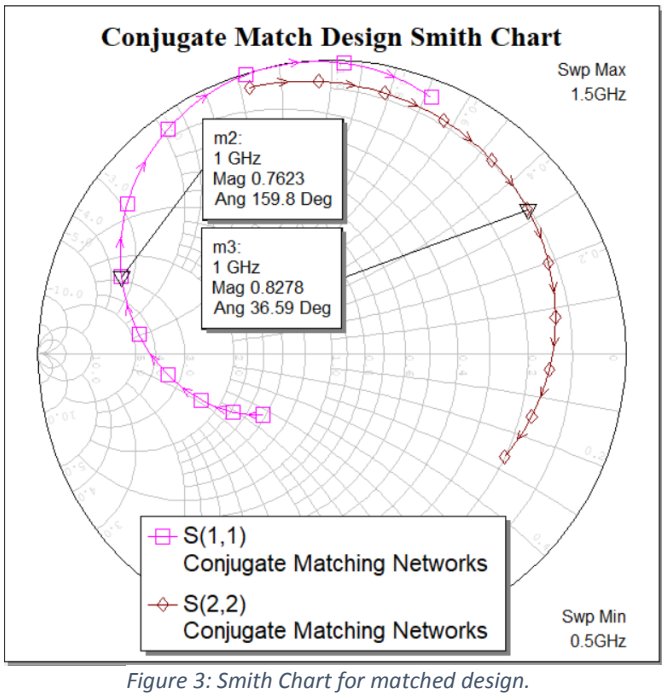


Figure 3: Smith Chart for matched design.

Table 4: Original Calculated TL Lengths (°)

TLOC	TLIN (P1)	TLIN(P2)	TLSC
67°	30.28°	54.64°	18.72°

The simultaneous conjugate matching is a good start, but it does not satisfy the gain and input and return loss requirements (all these graphs will be shown at the end of the report). The optimizer is run, and new lengths for the series and shunt stub transmission lines are calculated.

These are shown in the table below.

Table 5: Optimized Calculated TL Lengths (°)

TLOC	TLIN (P1)	TLIN(P2)	TLSC
39.2°	41.85°	44.58°	40.25°

Using the substrate parameters specified in Table 1, both the optimized and original TL values are converted to microstrip line (ML) lengths. The table below summarizes the design for the optimized microstrip design.

Because we are matching to a 50Ω load and source, the widths of the microstrip lines are fixed at 1.62982mm.

Table 6: Optimized Calculated ML Lengths (mm)

MLEF	MLIN (P1)	MLIN(P2)	MLSC
19.411	20.706	22.0558	19.9118

The microstrip design looks as follows:

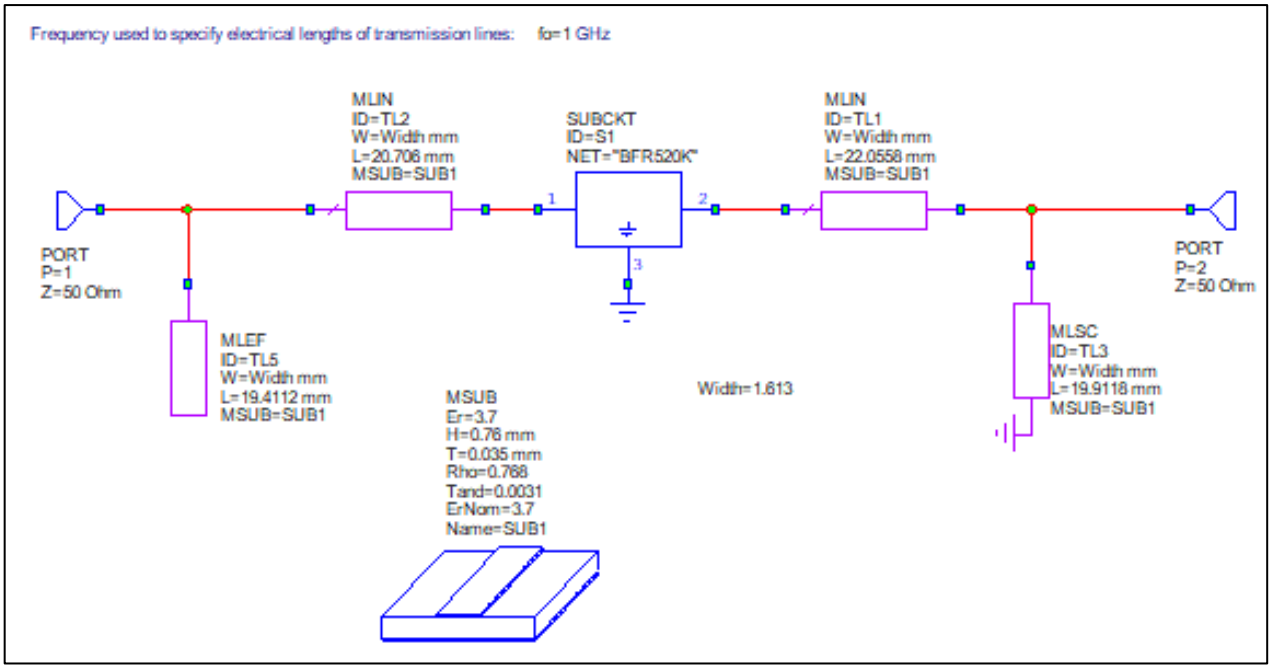


Figure 4: Microstrip design for the optimized conjugate matching networks.

The input return loss (S11), gain (S21) and output return loss (S22) for the original and optimized conjugate matches (TL) as well as initial and optimized conjugate match (ML) are shown in the graphs below.

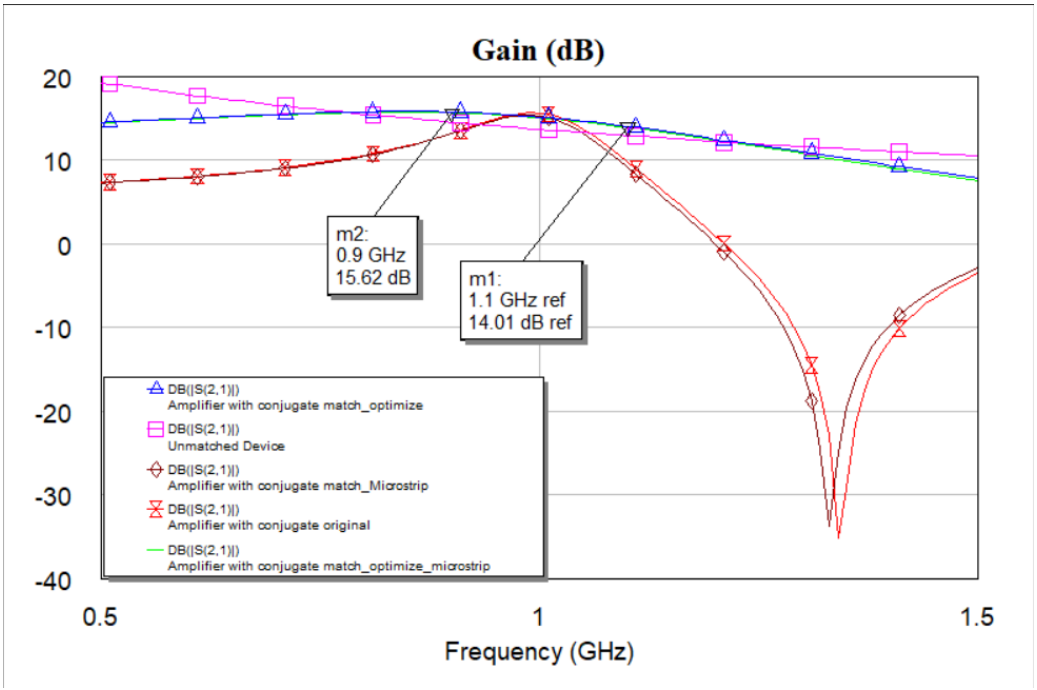


Figure 5: S21 or Gain in dB for all 4 amplifier designs

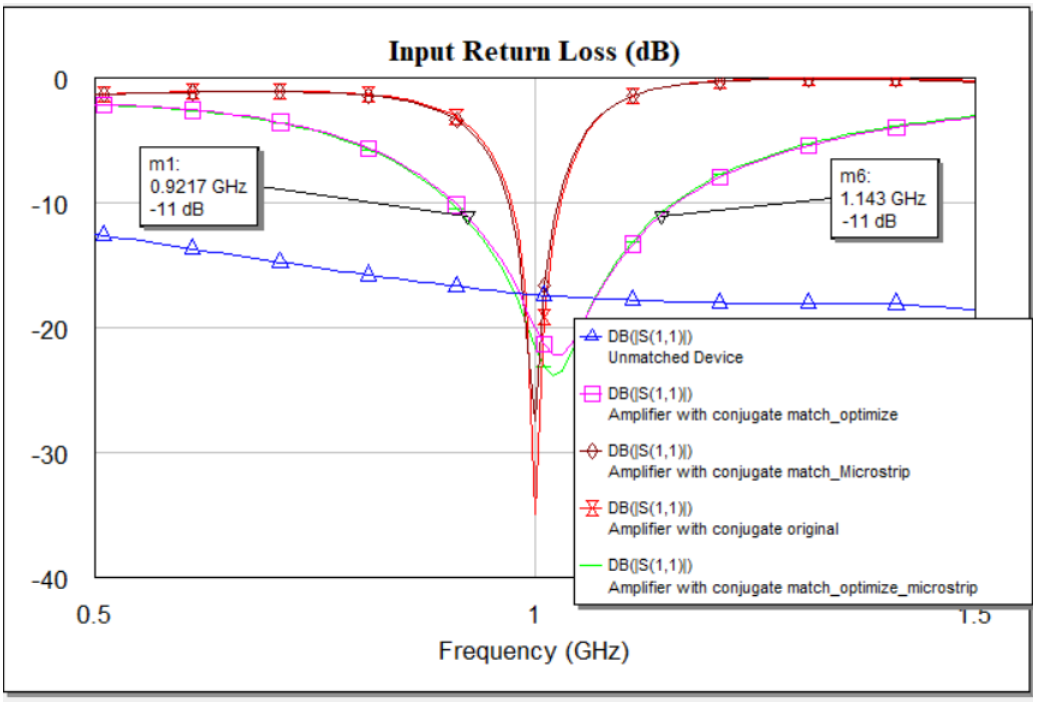


Figure 6: S11 or Input return loss in dB for all 4 amplifiers.

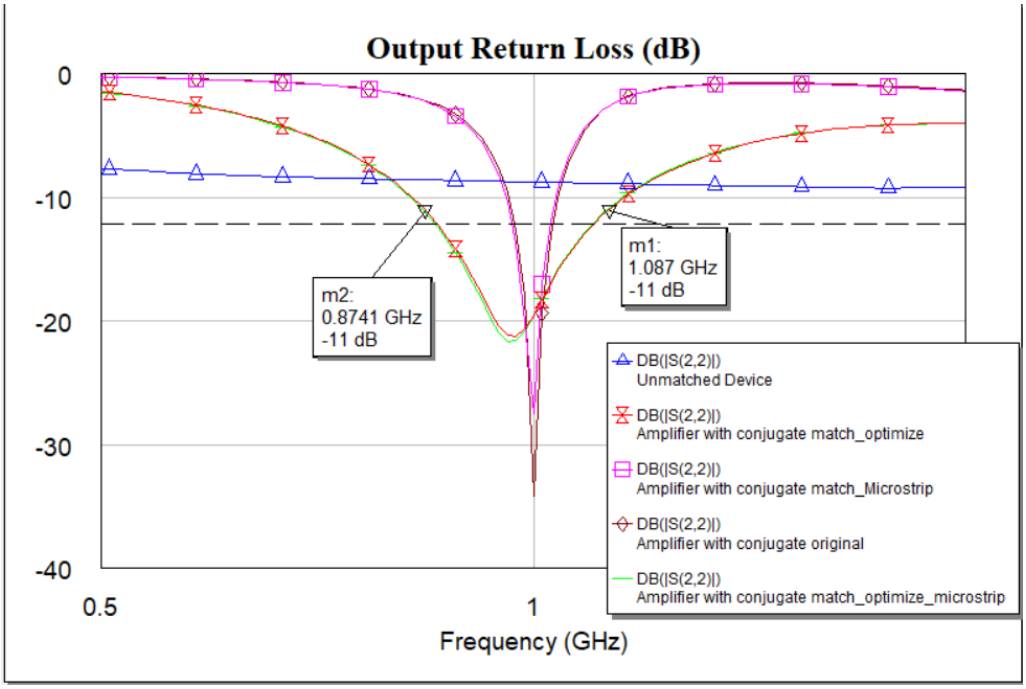


Figure 7: S22 or Output return loss in dB for all 4 amplifiers.

As can be seen, while the optimized design provides a better bandwidth than the initial design, it still fails to meet the specifications in Table 1. The design was tweaked as part of the final implementation, using multiple iterations of the optimizer function in AWR.

Final Implementation

In the final design, the bias of the transistor is presented. The capacitors C3, C4 and C5 are used as DC blocking capacitors, while C1 and C2 are used as an RF bypass capacitor (with an impedance inverter to create the illusion of an open circuit at high frequencies).

One of the requirements is to have a reactance equal to 10% of the characteristic impedance. As a result, the component values are calculated.

$$X = 10\% Z_o$$

$$1/\omega_c C = 10\% Z_o \rightarrow 1/2\pi C = 0.1*50 \rightarrow C = 31.8 pF$$

The 33 pF is chosen as it is the most suitable available capacitor.

The resistor value is selected to have a better control of the base current and voltage which result in smooth control of the DC biasing. With this implementation we can set the collector current to 20mA at V_{CE}= 6V.

The final design is shown in Figure 8. To provide a clear vision of the design Figure 8 was partition into two parts. Figure 9 shows part “a” while Figure 10 shows part “b”.

As it is discussed in the previous sections, the open circuit stub in the input and short circuit stub in the output are used for matching the input and output. However, the short circuit stub has a DC blocking capacitor “C5” connected between its terminal and the ground. DC blocking capacitor should not have significant impact on the performance of the short stub as it has been selected to have a reactance equal to 10% of the characteristic impedance. With this design, we were able to meet all the requirements as shown in Table 7.

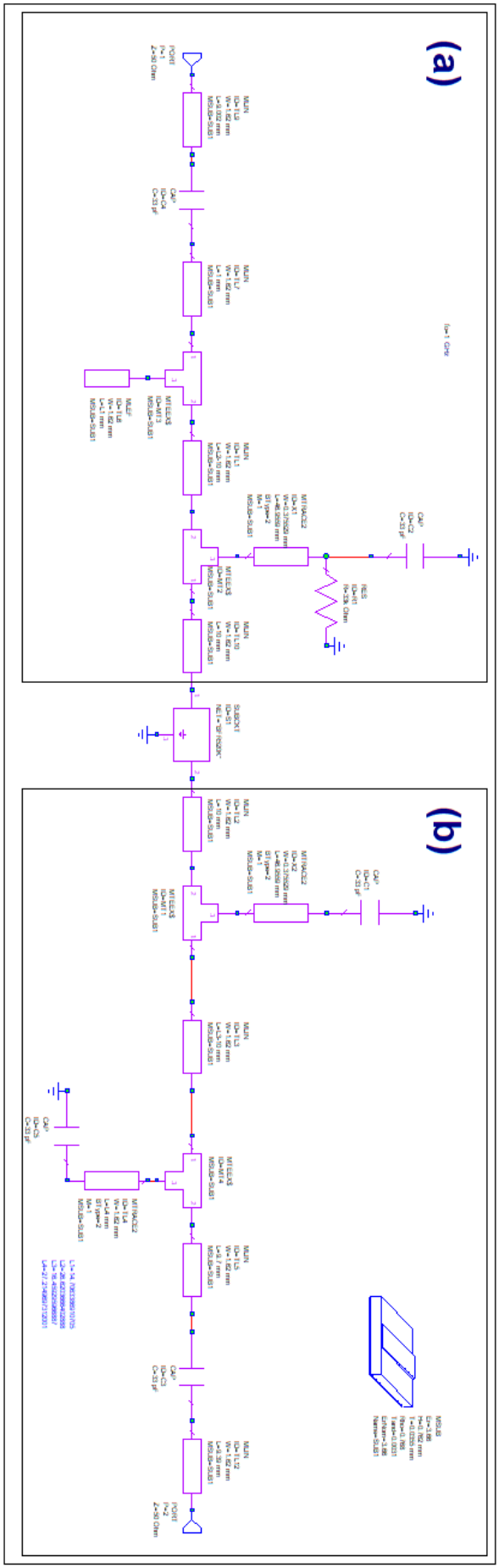


Figure 8: The final microstrip design

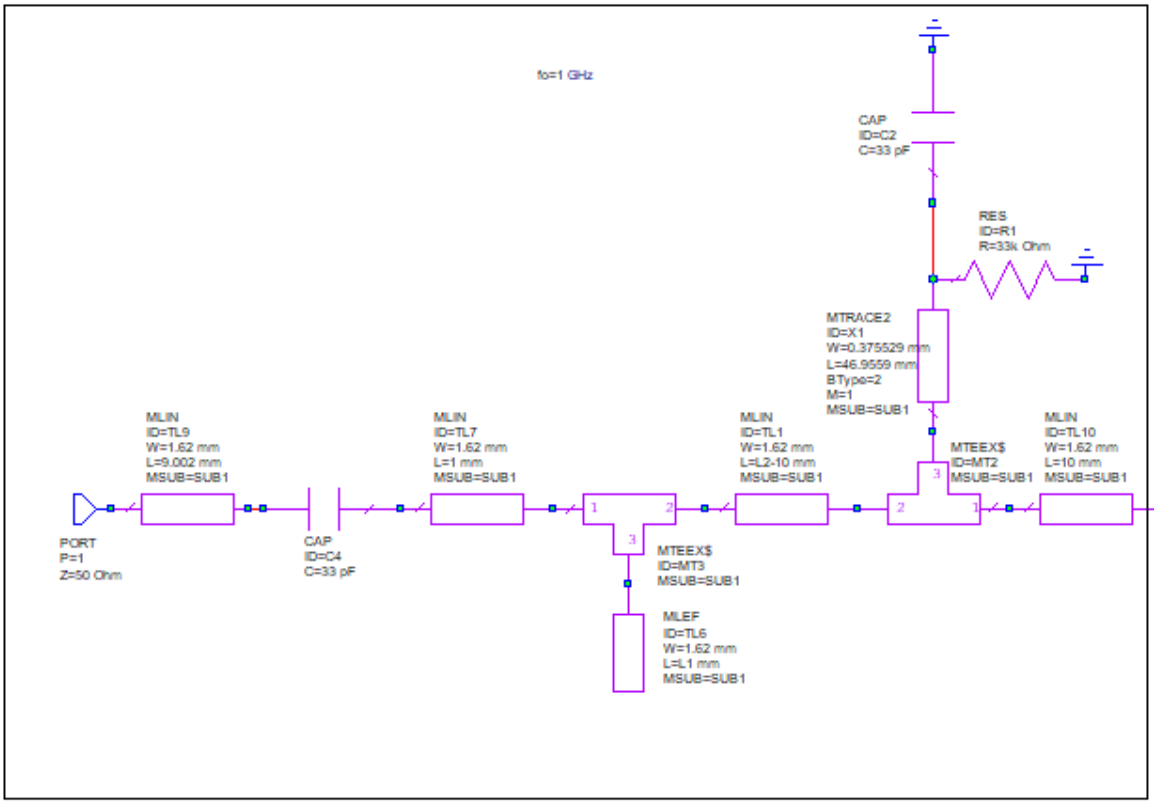


Figure 9: The final microstrip design part (a)

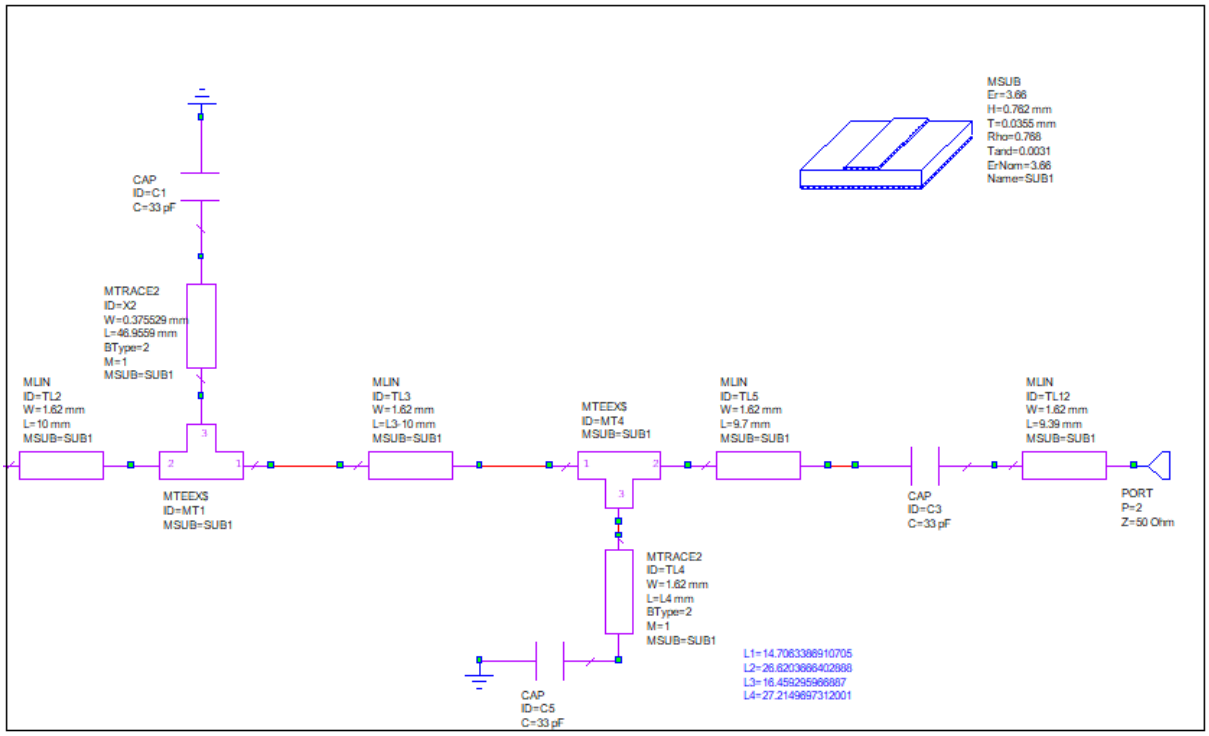


Figure 10: The final microstrip design part (b)

The gain (S21), input return loss (S11), and output return loss (S22) are shown in Figures 11 to 13, respectively. According to the simulation result, the design has met all the requirements.

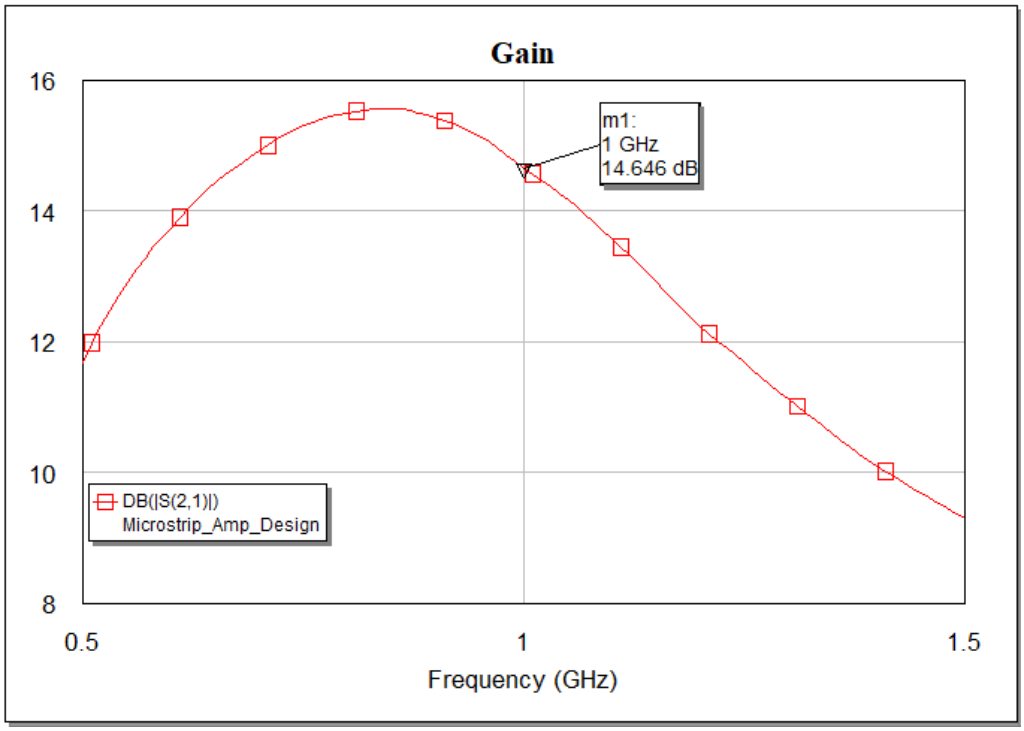


Figure 11: S21 or Gain in dB at 1 GHz

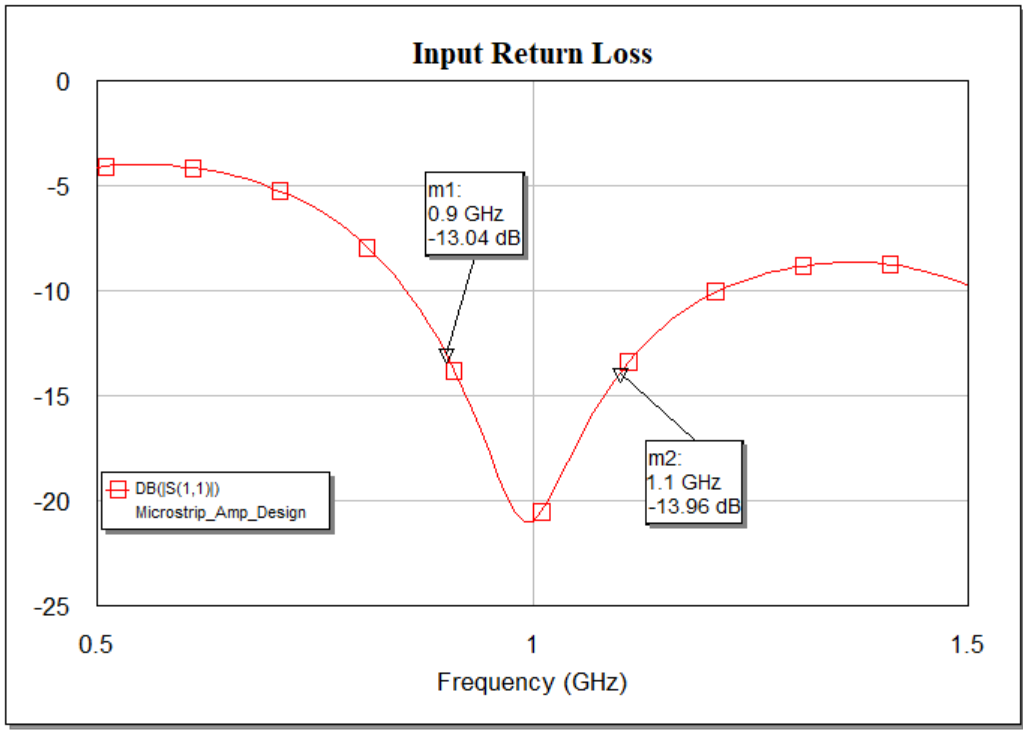


Figure 12: S11 or Return Loss in dB

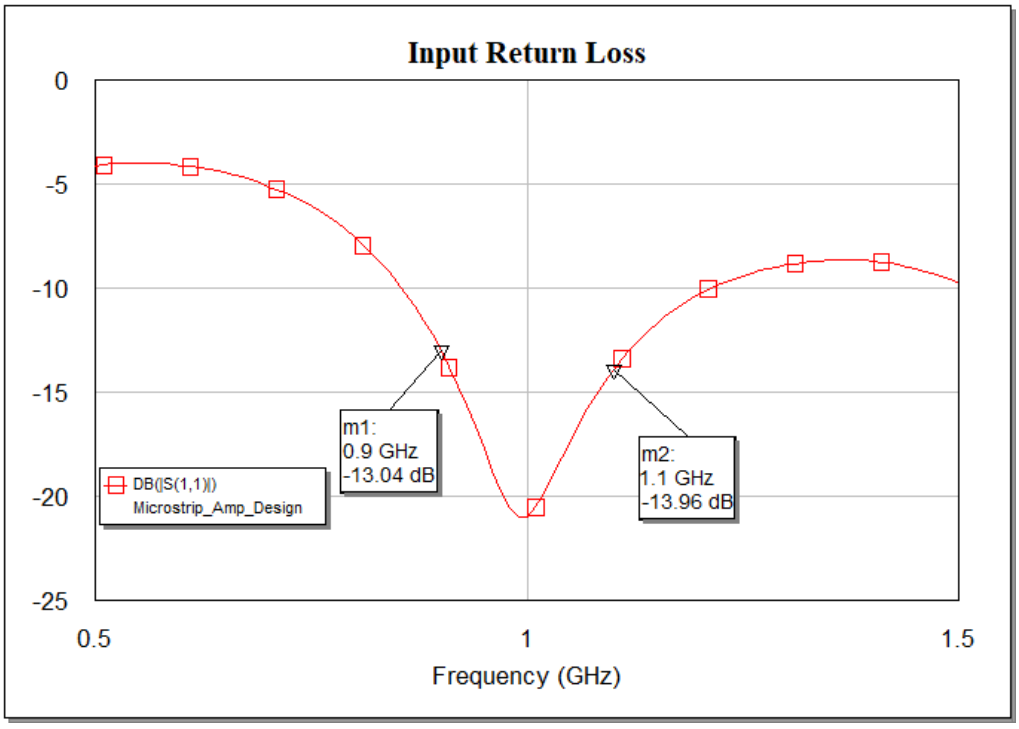


Figure 13: S22 or Output return loss in dB

Finally, after validating all the results, the design was sent out to be fabricated. Figure 14 (a) is the copper layout for the top layer of the printed circuit board design. Figure 14 (b) is a picture of the final circuit board after assembling and testing using the network analyzer in the lab.

As shown in Figure 14 (a) Vias are used to electrically and thermally join traces, pads, and polygons on different layers of a PCB. Vias are copper cylinders that are placed or formed in holes that have been drilled in a PCB. Since the bottom layer is the ground, we have used vias to provide pathways to ground.

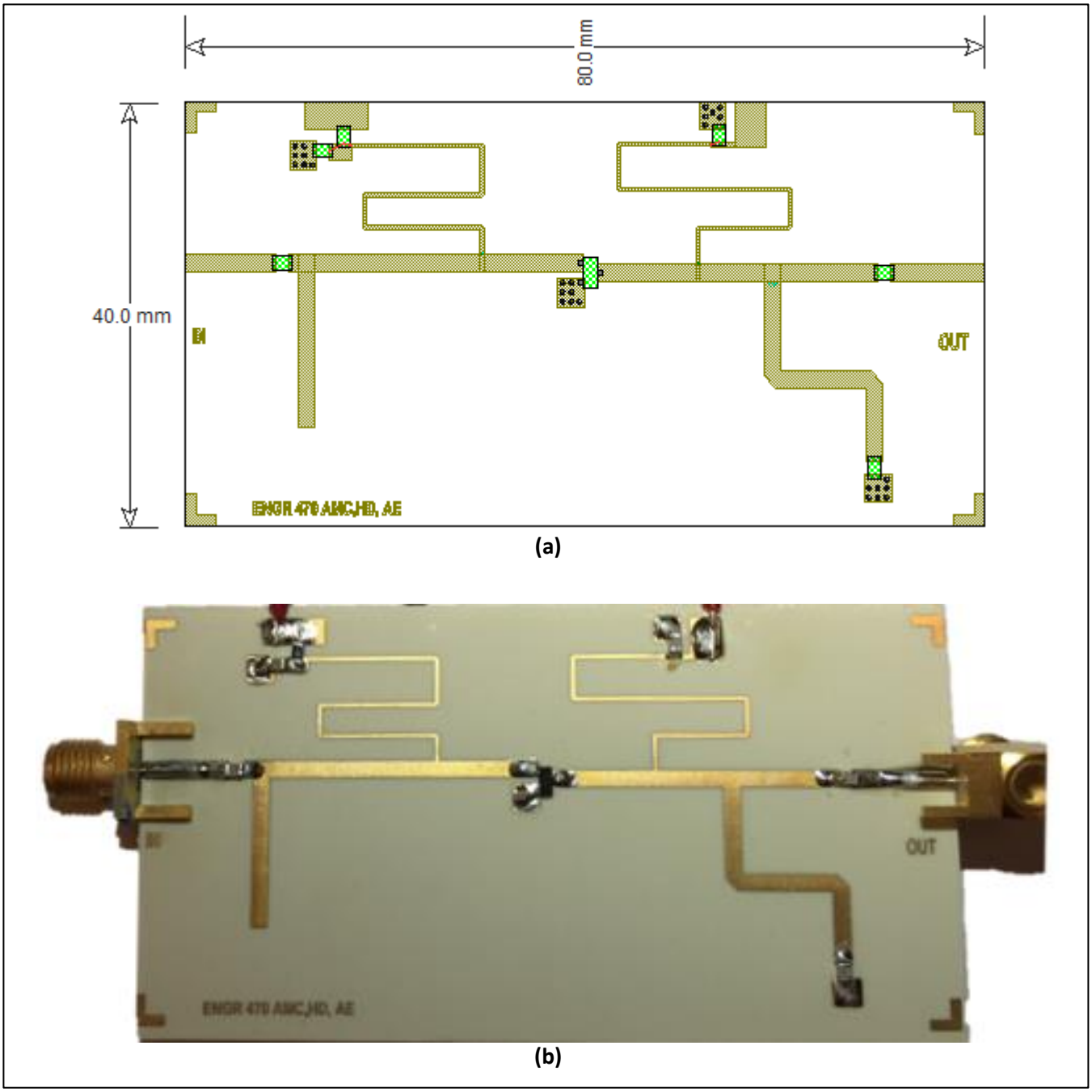


Figure 14: The layout design in AWR (a) and the fabricated circuit (b)

Experimental Results

The designed board was assembled in the lab. Once the prototype was ready, Scattering parameters of the designed amplifier was measured by Vector Network Analyzer (VNA). The experimental data are plotted and compared to the simulation responses.

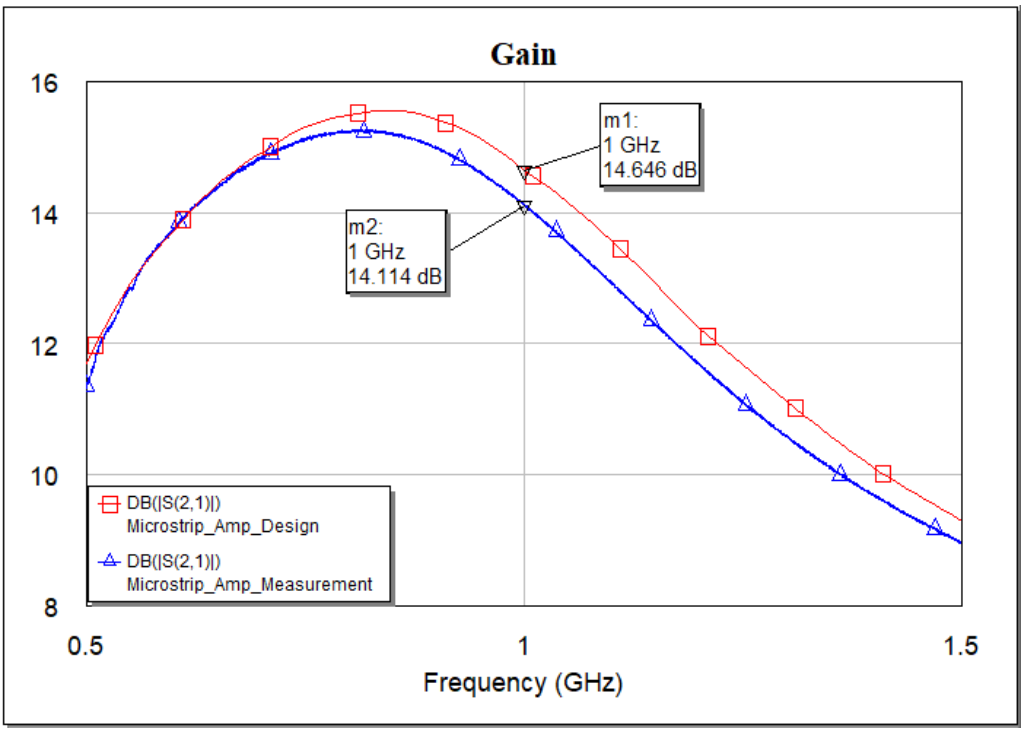


Figure 15: S21 or Gain in dB for the practical and simulation

As observed in Figure 15, the experimental gain of 14.114 dB is less than the simulated gain of 14.646 dB, showing a deviation by about 0.5 dB. The reasons behind this deviation are discussed at the end of this section.

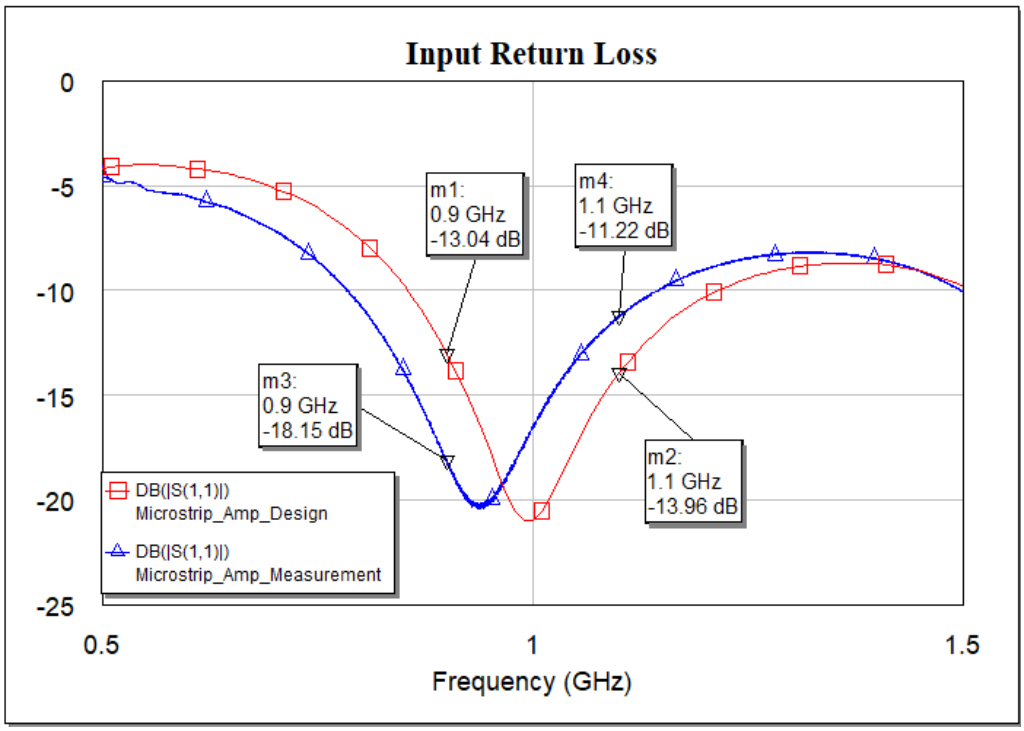


Figure 16: S11 or Return Loss in dB for the practical and simulation

From Figure 16, it is very noticeable that the experimental input return loss has an enhanced performance relative to the simulated design. Hence, the design was successful in meeting the criteria set forward.

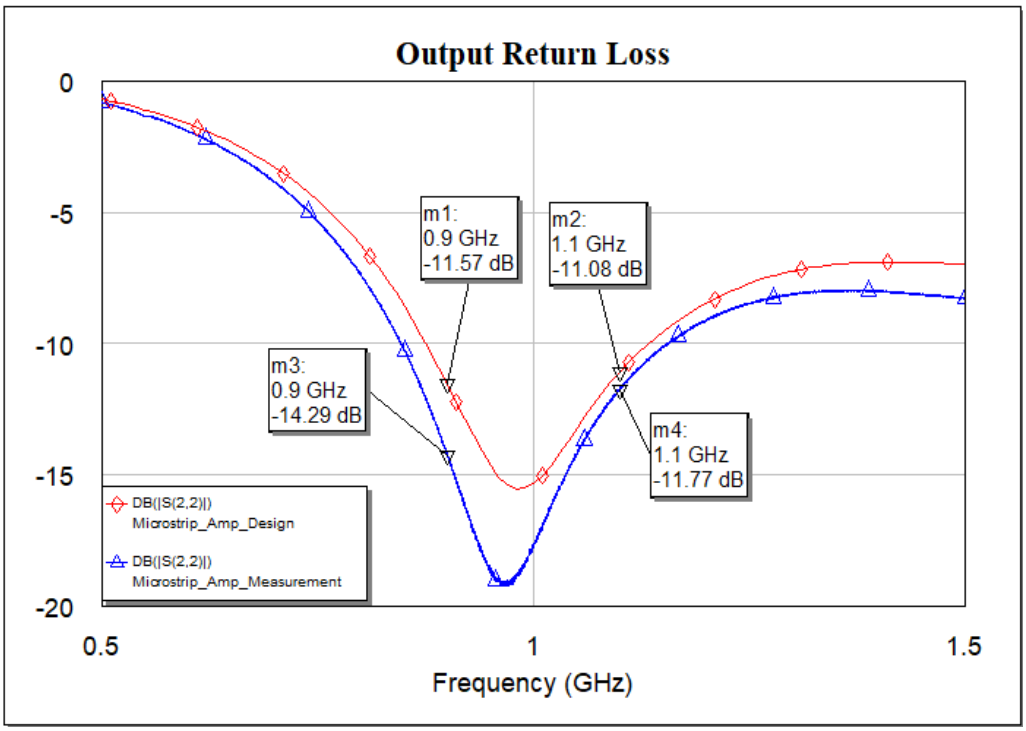


Figure 17: S22 or Output return loss in dB for the practical and simulation

From Figure 17, it can be deduced that the experimental output return loss is showing better output return loss bandwidth compared to the simulated result over the same frequency range.

In summary, the measurements show that the fabricated design has responses that maps the simulation part of the design. Although the gain witnessed 0.5 dB reduction in the measurements compared to the simulation, the input and output return loss have met the requirements in table 1. The difference between the simulation and the measurement could be due to the non-ideality of the components and the accuracy of etching and fabricating the transmission lines and the stubs. Another source of error could be due to the soldering as we did not account for this part in the simulation. Finally, the actual design lacked enough space to fully accommodate the SMA connector on the board. Thus, the floating connection of the SMA connector on the board may have introduced excess losses.

Measurement Summary

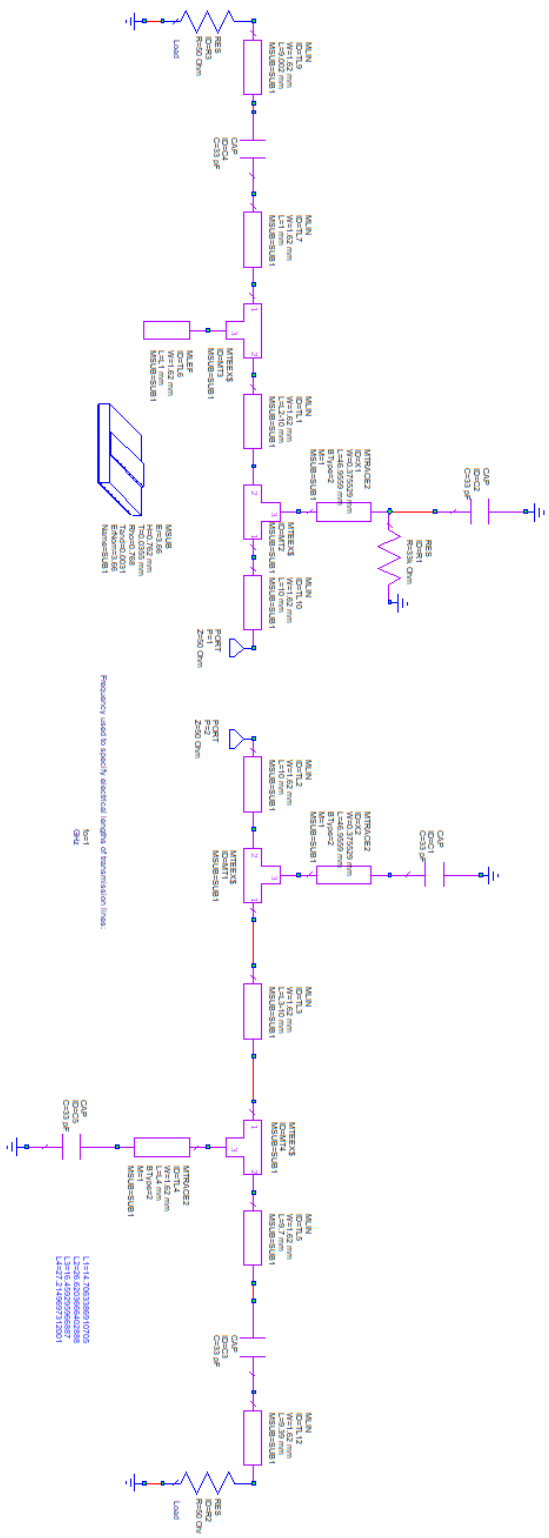
Table 7: Measurement Summary

Specification	Specification	Simulation	Measurement
Center frequency f_c : 1GHz	—	—	—
Bandwidth f_b : 200 MHz	—	—	—
mid-band transducer gain at f_c	$\|S21\|$ > 14.5dB	14.646 dB	14.114 dB
input match at $f_c + f_b/2$	$\|S11\|$ < −11dB	-11.22 dB	-13.96 dB
input match at $f_c + f_b/2$	|S11| < −11dB	-13.04 dB	-18.15 dB
output match $f_c + f_b/2$	|S22| < −11dB	-11.08 dB	-11.77 dB
Output match at $f_c + f_b/2$	|S22| < −11dB	-11.57 dB	-14.29 dB
Base bias current I_B	—	0.2 mA	0.16 mA
Base bias voltage V_{BE}	—	0.7 V	0.7 V
Collector bias current I_C	—	20 mA	20 mA
Collector bias voltage V_{CE}	—	6 V	6 V

Appendix

Γ_L and Γ_s for final design

The schematic used to find Γ_L and Γ_s



The smith chart used to find Γ_L and Γ_s