Advances in Modelling and Material Characterization of Hole Spin Qubits in Ge

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Abstract

Quantum computers have the ability to perform calculations that are currently intractable on the best supercomputers. While the creation of a universal quantum computer is far removed, an exciting near-term application of quantum computing lies in quantum simulation. Realization of these simulators would allow for computing things like many-particle interactions in materials, leading to scientific advancements. Spin qubits using holes in quantum dots are a promising option towards implementing these near-term quantum simulators, since they have been shown to have long coherence times and are compatible with existing silicon manufacturing technology, making them suitable for scaling.

State-of-the-art hole spin qubit systems include the development of two and four-qubit processors. Despite their potential, little work has been made towards enabling scalability of hole-spin qubit platforms. Current simulations employ computational approaches that rely on simplified models and do not take into account device design. In this thesis we develop a simulation framework for hole spin qubits in Ge using realistic gate patterns and examine the effect of this model on key properties of these qubits. We determine that significant differences emerge between the simplified and realistic models, and we quantify these differences. This work defines a minimal model that can be used to predict and optimize spin qubit performance.

Germanium is often used for spin qubit platforms because it forms a good ohmic contact with most metals. In doped Ge quantum wells, holes have high mobility and low effective mass, facilitating the confinement of spins. However, highly doped materials contain impurities that degrade the performance of quantum devices at low temperature. Although unexplored, there is interest in using

undoped and unstrained Ge epilayers in quantum devices, since they have a higher thermal budget than quantum wells and are an industrial material, allowing for more freedom in fabrication and scaling. In this thesis, we characterize a Ge epilayer substrate by designing and fabricating field-effect transistors and Hall bars to determine the electrical transport properties, carrier concentration and mobility at 4K. We determine that the device displays current-voltage characteristics typical of a transistor.

Together, these results advance knowledge on hole spin qubits in Ge.

Lay Summary

Quantum computers harness quantum mechanics to process information in ways classical computers cannot, allowing quantum computers to tackle selected but important problems that are too complex even for modern supercomputers. However, building a quantum computer is a formidable engineering challenge. Semiconductor spin qubits emerge as a promising candidate, since they have favorable properties and are easily manufactured. Both 2 and 4-qubit processors have been demonstrated, although scaling beyond this remains a challenge.

In this thesis, we develop a framework to simulate semiconductor qubits based on individual holes trapped in quantum dots to aid in the optimization of hole spin qubits for quantum computation. We also design, fabricate and measure electronic devices based on unstrained Germanium materials which in the future could be used to fabricate hole spin qubits with superior performance. This thesis supports and advances both theoretical and practical research into the properties of quantum dot hole spin qubits.

Preface

This thesis is based on a research project conducted by me under the supervision and guidance of Dr. Joe Salfi.

The research described in Chapter 2 was performed by me with input from Dr. Joe Salfi. The code for simulating the device potential was written by me, and the results of the calculations were analyzed by me, with input from Dr. Salfi and another group member, PhD candidate Mohammad Khalifa. The code for calculating the valence band states in the electric potential was written by Dr. Salfi and Dr. Jan Mol. The results from this work are the subject of a manuscript that is currently under review. I am first author of that manuscript.

The research described in Chapter 3 was performed by me. All devices described in this thesis were fabricated by me in the UBC Nanofabrication Facility. The wafers that the devices are built on in Chapter 3 were supplied by the group of Dr. Oussama Moutanabbir at Polytechnique Montréal. I contributed to the development of the fabrication process for the devices in Chapter 3, in a team led led by PhD candidate Mukhlasur Tanvir and postdoctoral fellow Dr. Ebrahim Sajadi in our group. The measurement and analysis of the devices presented in Chapter 3 were carried out by me, with input from the team described above as well as PhD candidate Mohammad Khalifa.

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I want to thank the group of Dr. Oussama Moutanabbir at Polytechnique Montréal for supplying us the wafers that made Chapter 3 possible. I would also like to acknowledge funding provided by NSERC CGS and CREATE programs.

I would like to thank Jonathan Holzman, who graciously allowed me to fiddle around in his lab during undergrad and gain the research experience that allowed me to begin a Master's degree. He was not only an incredibly dedicated professor and researcher but also an incredible mentor to his students. He sparked a lifelong

passion for both quantum computing and mountaineering, and shaped the person I am today.

Finally, I would love to thank my found family: Eric, Selman, Justin, Rosalie, Erin, Alexey, and Ewan for taking me on some of the most exciting adventures of my life and keeping me sane. They are the best friends I could ever hope for.

Dedication

This thesis is dedicated to Jonathan Holzman, who sparked and nourished my interest in quantum computing as an undergraduate student.

Chapter 1

Motivation and Background

1.1 Motivation

Quantum computers are able to, in theory, outperform classical computers in a specific subset of problems by exploiting the principles of quantum mechanics. Unlike a classical bit, which is limited to one of two binary states (either 0 or 1), a quantum bit of "qubit" can exist in a linear superposition of both a $|0\rangle$ state and a $|1\rangle$ state. A second quantum phenomenon, called entanglement, can be used to create correlated multi-qubit superposition states, giving a quantum computer an advantage over modern supercomputers [1]. For a specific subset of computational problems, there exist quantum algorithms that allow quantum computers to exploit these non-classical phenomena to their advantage.

However, creating these quantum computers has proven to be a remarkable challenge. Qubits are incredibly sensitive to noise and to unwanted effects from the external environment, and their quantum state can easily decay through a process called decoherence. To exploit a qubit's quantum properties reliably, an isolated and very low temperature environment is required [1]. However, it is impossible to completely isolate a qubit from its external environment, as it is only through these interactions that the qubit can be initialized, manipulated, and measured.

Despite these challenges, significant progress has been made after much investment and research. A 53-qubit processor with two-qubit gate error rates due to decoherence $<1\%$ has been demonstrated [2], and there exist classically intractable

calculations that can be performed on this processor. Quantum processors in the 50-100 qubit range with gate error rates around $> 0.1\%$ are loosely termed noisy intermediate-scale quantum (NISQ) computers [3]. These gate errors result from imperfect control systems and interactions of the qubits with the outside environment that cause decoherence. The 50-qubit threshold is significant because it represents systems too complex to be simulated on supercomputers [3]. Due to the significant overhead qubit cost required for error correction algorithms, NISQ devices are unable to employ these methods to mitigate errors. NISQ devices are therefore limited in the number of gates that they can execute before noise overwhelms the system. Finding ways to mitigate errors through other means remains an open challenge. In theory, as the number of qubits increases, so does the ability to employ error-correction algorithms that allow for more complex circuits to be created. However, to reach this milestone, significant improvements in qubit quality and connectivity need to occur. To employ error-correction algorithms, a processor needs to contain high-quality qubits with low physical error rates, as well as enough qubits to implement error-correction algorithms at a logical level. Developing a hardware platform capable of handling a scale-upto hundreds of thousands of high-quality qubits remains a massive challenge.

There are many different approaches to creating quantum computing hardware platforms. Among them are quantum dot spin qubits, which were proposed fairly early in the development stages of quantum hardware by Loss and DiVincenzo [4]. Their appeal lies in the ability to leverage decades of existing semiconductor technology during the fabrication process, allowing for compact fabrication of arrays, in which qubits can be electrostatically defined by applying voltages to metallic electrodes deposited on top of the semiconductor substrate. In addition, spins in semiconductor materials such as Si and Ge are shown to have long coherence times [5–14], which is a measure of how long a qubit can retain its quantum state before it is corrupted by interactions with the external environment. Long coherence times allow more quantum operations to be performed before a qubit loses its quantum state through decoherence. Initial research focused on QD platforms using electron spins in Si as qubits. Significant progress was made in this direction, with the state-of-the-art developments currently including the creation of high fidelity ($> 99.9\%$) single-qubit gates [15], the demonstration of small-scale algorithms in

[16] and most recently, the creation of a six-qubit quantum processor capable of creating 3-qubit entanglement [17].

Recently, hole spin qubits have emerged as having distinct advantages over electron spins due to their strong spin-orbit coupling that enables all-electrical control, unlike electron qubits which are controlled magnetically. Since it is far easier to apply and control electric fields on a quantum chip, hole spin qubit platforms are expected to be far more scalable. Indeed, small-scale two and four-qubit processors using hole spins have emerged [10, 14], but work remains to be done in creating platforms that can accommodate more than a handful of qubits. Hole spin qubits are promising candidates for achieving this goal, since they have been discovered to have points of optimal operation where dephasing due to electrical noise is minimized and qubit rotations are fastest [18, 19]. This phenomenon has been experimentally proven for holes in Si [20, 21].

Despite their strong potential, little work has been made towards enabling scalability of hole-spin qubit platforms compared to other approaches like superconducting or ion-trap qubits. This would involve the study of materials and creation of technologies to make rapid prototyping and testing of these platforms viable, with a view towards eventual commercialization.

Simulation platforms to aid in prototyping superconducting devices exist, and are in use industrially. For example, python packages to help compute interactions within superconducting junctions exists [22], as does a circuit simulator specific to Josephson junctions called WRSpice. However, to date nothing similar has been created for hole spin QD platforms. In Chapter 2 of this thesis, we develop a simulation framework that predicts key properties of a hole spin qubit QD platform (such as coherence time and manipulation time) using the potential distribution found in a realistic device. Ultimately, this would allow the design phase to be accelerated by allowing users to design and predict the properties of their designs without needing to run through multiple experimental and design iterations. The calculations are done for both strained and unstrained Ge, so that properties of interest such as qubit manipulation time can be compared.

Strain-relaxed Ge-on-Si epilayers are an industrial material, boasting a high thermal budget which relaxes fabrication constraints. If undoped, the substrate would lack the ionized impurities that contribute to instability in quantum devices

at low temperatures. Yet, quantum devices have yet to be demonstrated in unstrained planar Ge materials; most commonly, strained quantum wells are used. As shown in Chapter 2, unstrained Ge materials are predicted to offer faster qubit manipulation rates, as well as a higher thermal budget during fabrication. In Chapter 3 of this thesis, we make a first step towards using strain relaxed Ge epilayers in quantum devices. We have fabricated and measured field-effect transistors (FETs) suitable to demonstrate the ability to control charge, and Hall bar structures suitable for determining materials properties, on unstrained and nominally undoped Ge epilayers at 4K. We demonstrate operation of the FET at 4K by showing that a microfabricated gate electrode can be used to control the device conductance. The Hall bar structures are used to characterize the properties of carrier concentration and hole mobility at 4K. This demonstrates the basic elements of ohmic contacts and gate control needed to fabricate a Ge qubit, and allows us to assess the materials quality of the epilayer Ge in a low temperature environment.

1.2 Quantum Computation

In computer science, problems can be classed in terms of their time complexity, which is a measure of the amount of time taken for an algorithm to run, and depend on the size of the input. Two general classes of problems emerge: there are polynomial (P) problems, which can be solved in polynomial time, and nondeterministic polynomial (NP) problems, for which a solution can be verified in polynomial time, but requires exponential time to solve. The debate on whether NP problems can be solved in polynomial time by finding a clever classical algorithm is ongoing.

This is where quantum computers come in. Quantum algorithms, such as Shor's algorithm for factorization and Grover's algorithm for searching can be used to solve NP type problems that classical computers are unable to solve. For a quantum computer, computing power scales as 2^n where n is the number of qubits. This is due to a quantum mechanical property called superposition, in which a quantum bit is neither 0 nor 1, but in a linear superposition of both 0 and 1 simultaneously. This state is represented as $\alpha|0\rangle + \beta|1\rangle$. Upon measurement, this quantum state will collapse and a classical outcome of 0 or 1 will be obtained, with probabilities of $|\alpha^2|$ or $|\beta^2|$ respectively.

Another property that gives quantum computers their unique power is entanglement, in which one quantum state becomes linked to another, causing measurement outcomes to be correlated. Entanglement and superposition are the building blocks of all quantum algorithms. Computations can be performed using quantum circuits, which consist of a series of quantum gates that act on the qubits. A Hadamard gate is used to put qubits in a superposition, and the two-qubit CNOT gate is can be used to entangle two qubits. Any quantum circuit can be decomposed into one and two-qubit gates. Unlike some classical gates, all quantum gates are reversible, meaning that the original state can be obtained if the conjugate transpose of the gate is applied after the original gate. By creating a set of universal gates, that is, a set of gates that can approximate any quantum gates to any desired precision (for example, T,S,H,CNOT), it becomes possible to build the circuits that implement quantum algorithms.

However, in reality qubits are very susceptible to noise, which can come from the electronic control system or from the external environment. To account for this, quantum error correction (QEC) was invented [3]. By using QEC algorithms together with fault-tolerant circuit design, logical errors can be suppressed given that physical qubit errors fall below a certain threshold [3]. However, applying QEC algorithms requires a large number of physical qubits to encode the state of a single logical qubit. Modern quantum computers currently lie in the 50-100 qubit range. Since they are limited in terms of resources and gate fidelities (a measurement of how reliably gates can be implemented), QEC algorithms cannot be implemented [3]. Current research focuses on extending the power of existing technology by finding ways to lower the physical error rate of qubits, design noise-resilient algorithms, and improving QEC schemes for use in the near future noise-resilient algorithms [3].

1.3 Quantum Computer Hardware

In his seminal paper [23], David DiVincenzo defines five requirements for the implementation of quantum computation:

1. **A scalable system with well-characterized qubits**: This means that the system must have qubits containing well-defined and energetically degener-

ate ground and excited states, denoted $|0\rangle$ and $|1\rangle$. Well-characterized qubits means that the qubit's properties are known and its couplings to control systems and other qubits are controllable.

2. **The ability to initialize qubits to a known state**: the system should be able to initialize qubits to a low entropy state to (a) prepare a known state before executing a circuit and (b) to provide a continuous supply of $|0\rangle$ states for QEC.

3. **Long coherence times**: Fault-tolerant quantum computing refers to when multiple physical qubits make one logical qubit. To permit fault-tolerant quantum computation, coherence times should be 10^4 to 10^5 times longer than the gate operation time.

4. **A universal set of quantum gates**: a control architecture that allows implementation of a universal gate set with minimal errors.

5. **Reliable readout**: the ability to measure specific qubits with high quantum efficiency and speed no more than 10^{-4} of the coherence time.

While these requirements suffice for quantum computation, any useful quantum computer must also be capable of quantum information processing. DiVincenzo defines two requirements for quantum communication, which is integral to creating a quantum computer that can retain, transmit, and process information:

1. **The ability to inter-convert stationary and flying qubits**: a method to encode the state information of a stationary qubit to that of a flying qubit (defined below) should exist and vice versa,

2. **The ability to faithfully transmit flying qubits**: a scheme to reliably send these qubits long distances without affecting the encoded information should exist.

Flying qubits are carriers of information. Unlike stationary qubits used in local quantum computation, they transmit a quantum state across macroscopic distances. They must be stable at room temperature, and able to be read out reliably. An example of this would be the use of optical photons, which can become entangled

with a local quantum state such that their polarization (for example) encodes information about that state. Optical photons can be transmitted large distances at low loss through fiber-optic infrastructure.

Based on the above criteria, different hardware implementations of quantum processors have emerged. We briefly explain some of the most popular in the following subsections, and cherry-pick state of the art metrics across different works to show the absolute best performance achievable for each of these metrics.

1.3.1 Trapped Ion Qubits

Ions can be trapped in a oscillating electromagnetic field and laser-cooled such that they undergo small oscillations about the equilibrium position. Multiple ions can be trapped in a one-dimensional chain, and well separated so that they do not knock into each other. Because the ions are supercooled, their motion in space is quantized. If any one atom emits or absorbs a photon, the chain of ions will move together.

The qubit basis states are encoded into the atomic energy levels of an atom with unoccupied lower energy levels. A laser beam can be used to excite an electron from the ground state to the excited state. A sequence of timed laser pulses are used to implement single-qubit quantum gates.

The motion of the chain of atoms behaves like a harmonic oscillator, and can transmit energy through phonons [24]. Specific laser frequencies can excite the harmonic oscillator, allowing for the implementation of two-qubit gates. An advantage of trapped ion systems is their incredible coherence times, which are as large as 600 s [25]. Even though two-qubit gate times are quite slow compared to superconducting qubits, [26] this represents a ratios of coherence time to gate time of $\approx 10^6$. Additionally, high-fidelity operations have been achieved for trapped ions: this includes single and two-qubit gates as well as initialization and readout, which can all be done with fidelity greater than 99.9% [26].

A limitation of trapped-ion qubits is their slow two-qubit gates: the fastest demonstrated is about 1.6 μs [27], with typical times in the *ms* range [27]. This means that algorithms will take a fairly long time to execute, possibly to the point of being impractical to implement [26]. Additionally, it has been challenging to

scale to larger numbers of ions, as inter-ion connectivity suffers with scale. To date, entanglement between arbitrary sites in a > 100 ion system has not been demonstrated [26].

1.3.2 Superconducting Qubits

Alongside trapped ions, superconducting qubits were one of the earliest quantum processors explored, and remain promising to this day [28]. In superconductors, an interaction between electrons and phonons leads to the formation of Cooper pairs, which are bound electron pairs. These pairs no longer obey the Exclusion Principle, and so all electrons pairs are free to occupy the ground energy state.

A Josephson Junction (JJ) consists of two superconducting electrodes separated by an insulating barrier. Because the Cooper pairs are in a low-energy state, they can tunnel across the barrier without encountering any resistance from the lattice so long as the current is below the critical current of the junction. When the current exceeds this value, a time-varying voltage develops across the junction.

The most common type of qubit to be built with a JJ is a transmon qubit, which is created when the junction is placed in shunt with a capacitor. Due to the presence of the JJ, the energy level spacings in the superconducting circuit are non-uniform, meaning that two basis states for the qubit can be isolated. Reduced sensitivity to charge is achieved by choosing an appropriately large capacitance. Superconducting qubits are relatively easy to couple to each other using microwave cavities, and can be controlled using commercial microwave devices [28].

However, a limitation of superconducting qubits is the very low temperature that must be maintained to cool the anharmonic oscillator to its ground state. This is achieved by placing the qubits in devices called dilution refrigerators. As circuits scale up and circuitry becomes more complex, these low temperatures are harder to maintain. Due to their large size compared to other quantum systems, superconducting qubits suffer from relatively low coherence times, with the state of the art transmon qubits boasting coherence times of up to 0.3 ms [29]. While two-qubit gates can be performed with speeds in the tens of nanoseconds [26, 30], measurement is a slower process and poses challenges [28].

1.3.3 Spin Qubits

Loss and DiVincenzo first proposed the use of quantum dots to manipulate single electron spins as qubits [4]. In this scenario, electrons are confined to an interface via a quantum well, which is a stack of materials with different band gaps. A set of metal electrodes on the surface of the semiconductor can apply a voltage that traps the electrons laterally, confining them in three dimensions and creating a quantum dot (QD). Through careful manipulation of electrode voltages, a single electron in the conduction band (or hole in the valence band) can be confined to the QD. The spin $|\uparrow\rangle$ and spin $|\downarrow\rangle$ states form the qubit basis states when an external magnetic field is applied, separating them in energy.

While research into spin qubit platforms is relatively new compared to other technologies, they boast relatively long coherence times, achieving ≈ 30 ms for electrons [5] and ≈ 0.9 ms for holes [20]. Two qubit gate speeds have been demonstrated at 0.8 ns for electrons [31] and 75 ns [32] for holes. Unlike electron spin qubits, which have been studied for the many years, hole spin qubits have been realised in the past couple of years. This means that they lag electron spin qubits in terms of development; however, hole spin qubits are particularly promising, for reasons outlined in Section 1.1 and Section 2.1. However, spin qubit processors currently lag ion-trap and superconducting technologies in terms of qubit count [33]. This is because device fabrication, which has nanoscale features, is more challenging than superconducting circuits. Also, low-frequency charge noise makes frequent re-tuning necessary, which is time-consuming [33] and restricts the ability to commercialize these devices.

1.4 Quantum Dots as Qubits

A quantum dot (QD) is a semiconductor structure that confines the motion of an electron (or hole) in three dimensions, leading to the quantization of energy levels. In a quantum well material, a QD can be created by applying a voltage such that the confinement of the electrons is limited to the well.

QDs were first proposed as a means to implement qubits by Loss and DiVincenzo [4]. In this system, a QD can be used to trap a single electron spin that forms the qubit basis states, $|0\rangle$ and $|1\rangle$. In the case of a quantum well, the vertical

confinement is due to the heterostructure, and the lateral confinement is given by metallic gates deposited on the semiconductor.

A static magnetic field B_0 can be applied, which removes the degeneracy of the $|0\rangle$ and $|1\rangle$ states. Controlled rotations around any axis of the Bloch sphere (a 3-D representation of the qubit state) can be driven to implement quantum gates by switching on a time-varying magnetic field B_1 of a frequency that is resonant with the energy splitting between the $|0\rangle$ and $|1\rangle$ states. Single qubit logic can be implemented within a QD, and two qubit logic, in which two qubits are manipulated in order to perform quantum gates, can be implemented by using a system of double QDs that interact via exchange [4]. Electrons in a double QD system such as this are placed close enough together that their wavefunctions can overlap and facilitate the exchange interaction.

They are separated by an energy barrier that is raised or lowered with a metallic electrode; allowing the interaction of the electron spins to be controlled. If the barrier is raised, electrons in the dots can be isolated from each other. If the barrier is lowered such that tunneling becomes highly probable, the electrons can be made to tunnel between the two dots at a certain rate. This generates an effective interaction between the electrons known as the exchange interaction, which can be used to implement two-qubit gates.

However, a useful quantum system must also be able to read out the quantum states. Since the magnetic moment of an electron spin is too small to be measured directly, a method called spin-to-charge conversion [34] is used in QD qubits to convert a spin state to a corresponding charge state.

1.4.1 Quantum Device Fabrication

QD spin qubit devices are fabricated in many ways, and gate stacks can look vastly different from one platform to another. However, a generic outline of the fabrication process can be provided for single QD platform. A schematic of this simplified QD platform is provided in Figure 1.1.

The gate stack is built upon a substrate such as strained Ge/SiGe heterostructure. Since these materials have different bandgaps, a potential difference is created when they are brought together. This potential causes electrons to be confined to

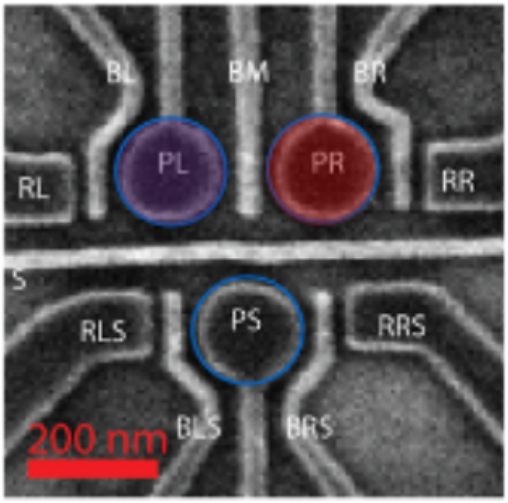

Figure 1.1: Top view of a simplified gate stack for a double QD spin qubit system is shown [35]. The ohmic contacts (RL/RR) define the reservoirs. The plunger gate (PL/PR) defines the quantum dot. The barrier gate (BL/BR) controls the tunnel coupling to the reservoir, while BM controls the interdot tunnel coupling.

the interface, forming a two-dimensional hole gas (2DHG), which is an effective sheet of holes confined move only laterally along the interface. With the application of a voltage on the plunger gate, holes can be confined to a small region below the plunger, forming a quantum dot.

First, a set of ohmic contacts are deposited directly onto the semiconductor. Depending on the feature size, a lift-off process using electron beam (for nanoscale features) or optical (for microscale features) lithography is used to define the pattern. Next, metal electrodes of a desired thickness are deposited using electron beam evaporation. These electrodes are used to define a hole reservoir, which is used to initialize and read out the qubit state within the quantum dot.

Next, an insulating oxide layer of an insulator such as Al_20_3 is grown using atomic layer deposition. This layer will separate the ohmic contact layer from the plunger and barrier gates.

Then, plunger and barrier gates are deposited using a similar fabrication pro-

cess as the ohmics. The barrier gates can be used to control the tunneling rate of charge from the reservoir into and out of the QD. The barrier gates can be used to deplete charge in the quantum dot until a the desired number of holes remain. In the case of multiple quantum dots, a second barrier gate can be used to control the tunnel coupling between quantum dots.

1.4.2 Lifetime of Qubits

In an idea world, quantum states are well-defined and preserved for an infinitely long time. In reality, the environment will interact with the quantum system, affecting its state over time. A simple way to model this interaction is by considering a qubit system, a control system that acts on the qubit, and an environment that couples to the qubit in uncontrolled ways. The density matrix ρ is the tool in quantum mechanics that allows a subsystem of a larger system, such as a qubit subsystem within an environment whose state is not well understood, to be described. Assuming the quantum system initially interacts with the environment, its density matrix can be found by tracing out the environment. The environment, and noise within the controlled qubit system, can cause relaxation and decoherence. This can manifest itself as random bit-flip (state changes from $|1\rangle$ to $|0\rangle$ or vice versa) or random phase-flip (state changes from $|+\rangle$ to $|-\rangle$ or vice versa). It can also manifest itself as a depolarization, where the off-diagonal terms that represent coherences in the density matrix decay [1]. The characteristic timescale over which qubit energy and phase are preserved are the relaxation and coherence times.

First, there is relaxation time, or T1, which describes the time scale over which a qubit decays from its excited energy state, $|1\rangle$ to its ground state, $|0\rangle$. In bulk semiconductors, relaxation processes typically occurs through inelastic phonon processes [36]. For example, a $|1\rangle$ state can decay into a $|0\rangle$ state through emission of an acoustic phonon. In QDs, electron and hole states are quantized, which modifies phonon processes compared to a bulk material[37].

Second, there is coherence time, or T2, which describes the time scale over which a qubit loses its phase coherence between different parts of a superposition state [38]. For example, a $|+\rangle$ state can become a $|-\rangle$ state due to a random shift in its precession frequency as a consequence of interacting with the environment.

In spin qubits, decoherence arises primarily due to nuclear noise and charge noise.

Nuclear spins in the host material couple to qubit spins through the hyperfine interaction. This nuclear spin bath couples the qubits in a way that can generate entanglement between the qubit spin and the nuclear spin, which in the qubit subspace, causes decoherence. Furthermore, fluctuations in a large number of nuclear spins resembles a classical fluctuating magnetic moment (magnetic noise), randomizing the spin's precession frequency and causing decoherence [38].

Nuclear noise is a major source of decoherence in electron spins in any group III-IV material, as all have isotopes with non-zero nuclear spins. While these can be reduced through isotopic purification they cannot be fully eliminated, because there is no stable isotop in the III-IV group with no net nuclear magnetic moment. However, group IV materials, such as Ge, have an advantage in this case. First, there is a high natural abundance of spin 0 nuclear isotopes in Ge [39]. Second, the p-type symmetry of the valence band suppresses the hyperfine interaction of holes with the nuclear spins in the lattice. Moreover, Ge can be isotope purified to completely eliminate the nuclear bath.

Charge noise is the second noise source that affects the value of T2. There are multiple sources of charge noise. One source is fluctuation of electron occupancy of trap levels at the semiconductor/dielectric interface, or inside the dielectric. Another source is the random motion of carriers inside metals (Johnson noise). Yet another source is tunneling two-level systems in dielectrics, which fluctuate down to zero temperature[40, 41]. Charge noise tends to have components at much higher frequencies than nuclear noise, even though it also possesses a low-frequency component. It also is both material and temperature-dependent. In today's semiconductor QD spin qubits, charge noise is thought to be one of the most important factors that degrades the fidelity of two qubit operations [40]. One method to minimize charge noise without sacrificing gate speed is to operate the qubit at 'sweet spots' where the derivative of the qubit splitting with respect to electric field (and therefore the coupling to noise) is zero.

1.4.3 State of the Art Spin Qubit Processors

Fault-tolerant processors rely on quantum error correction algorithms to mitigate errors that arise during operation. A quantum computer with a physical qubit error rate below a certain threshold can apply error-correcting algorithms to lower its logical error rate. Gate fidelity is a measure of the difference between the ideal and measured outcome of a quantum gate on a qubit, and represents the amount of confidence that can be had in the outcome of a computation. If qubits are prone to error, the gate fidelity is expected to be well below 100%. A gate fidelity greater than 99% is required to apply an error-correcting code like the surface code [42].

Future quantum computers will require a large number of qubits that can be implemented reliably, so that error-correction algorithms can be used. With a view towards scaling up QD spin qubit platforms, two properties of importance emerge: first, the one and two-qubit gate fidelities, and second, the number of interconnected qubits.

While significant progress has been made in pushing single-qubit gate fidelities above 99% for spin qubits in Si [32], until recently two-qubit gate fidelities had been unable to move beyond 98%. Achieving high-fidelity two-qubit gates is challenging, as it requires precise control as well as noise suppression techniques. In QDs, two-qubit gates are implemented by controlling the exchange interaction. Control schemes for two qubits gates must be fast, such that the operation lies within the coherence time of the qubits. This presents a design challenge, because simply implementing higher bandwidth pulses for faster gate operation will introduce unwanted noise into the system, leading to decoherence. Recently, a CNOT gate fidelity of 99.5% was demonstrated [42] using resonant exchange, in which the driving field frequency is calibrated to match the energy difference between the two spin qubits. This enhances the exchange interaction sufficiently to suppress the effects of charge noise during a fast operation [42].

For hole spin qubits in Ge, which have only been realized in the last two years, two-qubit operations with a fidelity have yet to reach the same level as electron spin qubits in silicon, which have been studied for 13 years[43]. However, single-qubit gates with a fidelity of 99.3% and speed of 20 ns have been demonstrated [14] in a Ge double QD. Rapid two-qubit gates are also realized via the exchange interac-

tion, with a sixfold increase in speed over state-of-the art electron spin qubits. The strong spin-orbit coupling experienced by holes in Ge enables fast, all-electrical manipulation, contributing directly to the rapid manipulation time for both one and two-qubit qubit gates.

While significant research has been done on increasing the qubit count in semiconductor QD processors, these systems currently lag behind superconducting or ion-trap system in terms of qubit count [17]. Maintaining a high gate, initialization, and readout fidelity across qubits is a challenge. Recently, work by [17] addressed this issue. A six-qubit quantum processor using electron spins in Si was shown to have single-qubit gate fidelities $>$99%, two-qubit gate fidelities in the 89-94% range, and measurement visibilities in the 93-98% range; the latter is similar in value to state-of-the two-qubit processors [44].

Several novel techniques contribute to this achievement. First, a mutli-layer gate pattern is developed, allowing fine control over the charge occupation of each QD, and of the tunnel-coupling between QDs. Second, qubit initialization is performed by using real-time feedback instead of tunneling to a reservoir, reducing external noise. These improvements allow for universal control over the six qubit array, and present new methods of designing scalable QD platforms that enable high connectivity across qubits without sacrificing control.

For holes in Ge, a four-qubit processor was recently demonstrated [10] by implementing a 2D QD array in a strained Ge quantum well. The low hole effective mass and material uniformity permits precise control over the inter-dot coupling, allowing for the implementation of three and four qubit gates. The ability to independently couple anywhere from one to four spins all-electrically represents an advancement towards creating scalable QD platforms in Ge.

When aiming to scale QD platforms, one of the main challenges lies in scaling up the connections for the control electronics. Research has been done on different QD platform topologies that enable the integration of on-chip control electronics in a scalable manner [45].

1.4.4 Previous work on CAD of Qubits

The need to improve the hardware design cycle for quantum processors was identified early on in the field of quantum computing [46]. There is a great desire to understand the capabilities of proposed processor designs through simulation, which reduces the time spent on an otherwise lengthy fabrication and experimental cycle. As the push for low error rates and increased qubit capacity continues, it becomes even more crucial to develop software tools that can assist the design process [47].

Most recently, work by [47] outlines a simulation-to-test pipeline in which readily available multiphysics modeling techniques can be used to simulate key interactions. The calculations are not limited to extracting the potential energy distribution from a CAD-modeled QD platform, but encompass all aspects of the design process, from modelling current transport across charge sensors used in spin readout, to using band-structure solvers to compute qubit wavefunctions, allowing for the calculation of single and two-qubit gate times. This work outlines how a multiphysics approach can be used to accelerate in scaling qubit prototypes to a larger-scale quantum processor [47].

While there is no previous work on modeling hole spin qubits through combined CAD design and simulation, something similar has previously been done for electron QDs in Si [46]. In this work [46], a platform that can accommodate 4 QDs was designed. It consists of a strained Si quantum well substrate to confine electrons vertically, and a series of split top-gates that confine them laterally. Two-qubit interaction are achieved by controlling the strength of the exchange coupling. The potential energy distribution is extracted through a finite-element electrostatic simulation, so that the effect of linear combinations of gate voltages can be analyzed. The system is modeled using configuration interaction to understand the effect of the gate voltages in controlling the strength of the exchange interaction. These results are then used to calculate the error rate in the exchange coupling based on the noise in the control pulses. Their results stress the importance of using realistic CAD models when calculating gating errors, as the exchange coupling is sensitive to uncertainties in gate voltage.

However, the effects of spin-orbit coupling are not considered in that work.

These effects are not negligible, especially not in hole qubits where the spin-orbit coupling strength is strong and highly sensitive to electric field fluctuations. There is a need to develop realistic CAD models for hole spin qubit platforms so that the effects due to a both a non-separable confining potential and control pulse noise can be understood.

1.4.5 Error Correction

Achieving the full potential of quantum computation will require billions of quantum operations to be performed [48]. State-of-the art quantum processors currently have error rates of about 10^{-3} per gate [48], which is far too high for any reliable implementation. Therefore, a method of correcting these errors is required. Error correction algorithms function by using multiple physical qubits to encode the state of a logical qubit. Information is encoded in the state of the logical qubit, and operations are performed on these logical qubits as well: these qubit groups are better protected from decoherence than if the state were encoded simply into a physical qubit. There are many ways to map a group of physical qubits to a logical qubit; many types of error correcting codes exist.

To date, progress has been made in demonstrating quantum error correction on codes able to detect and correct a single error, e.g, [49], as well as demonstrating fault-tolerant control [50] of single logical qubit composed of 13 trapped ions. Fault-tolerant systems contain the spread of errors; without fault-tolerance, errors arising from one part of the system can cascade into another. Work in [50] demonstrates a fault-tolerant error correcting code applicable to all operations required of a quantum processor: state preparation, measurement, logical gates and error detection. Put simply, fault-tolerant operation of a quantum processor requires reliable detection and correction of both bit-flip and phase-flip errors [49]. If the number of physical qubits is increased, the size of the error correcting code can be increased and the number of errors that can at least be detected and corrected per error-correction cycle increases [49].

Recently, a team at Google [48] proved that a larger error-correcting code size reduces logical error rates in a real device. By scaling up to a 72-qubit superconducting device, they were able to implement an error-correcting code that

corrected two types of errors, and demonstrated that it outperformed a smaller error-correcting code in terms of error-detection accuracy and logical error occurrence. By demonstrating that logical errors are better suppressed with larger error-correcting codes, this work achieves a critical step towards scalability of quantum processors.

Chapter 2

Computer-Aided Design of Hole Spin Qubits in Germanium Quantum Dots

2.1 Introduction

Classical electronic circuit design employs simplified models extracted from device-level simulations. Similarly, the design of large-scale quantum circuits will benefit from a thorough understanding of how device design impacts quantum circuit performance. This approach is beginning to be adopted within the superconducting qubit community, employing electromagnetic extraction of parameters in quantized circuit models in superconducting devices, and development of design frameworks [22, 51–53]. The understanding of spin qubits in semiconductors[4] is at an earlier stage of development[47, 54, 55] and could benefit from a similar approach, given recent rapid experimental progress [9, 10].

Spin qubits, implemented as quantum dots (QDs) [5–14] or dopants [20, 56, 57] in group-IV materials, are of interest because they utilize the most common materials in the semiconductor industry, and because isotope purification in group-IV materials permits the elimination of the nuclear spin bath, enabling long spin coherence times [5, 20, 56, 58]. Spin qubits based on valence band holes have recently

attracted significant attention in Si [6, 7, 20, 57] and Ge [10–14]. This is due to the strong spin-orbit interaction (SOI) experienced by spins in the valence band, which enables electric qubit manipulation through electric dipole spin resonance (EDSR) [59], as well as long-ranged two-qubit operations mediated by superconducting resonators [60] or mutual capacitances [18]. Holes also lack the valley degree of freedom that complicates operation of electron spin qubits in group-IV materials [19, 61]. Moreover, the p-type character of the orbitals of valence band holes suppresses nuclear-spin-induced decoherence compared to conduction band electrons [62].

For hole spin qubits, the presence of Rashba SOI that enables the desirable electric control generally ties qubit properties to electric potentials, and makes the qubits more susceptible than electron spin qubits to decoherence and relaxation from electric fluctuations and phonons. Indeed, reported T_2^* coherence times for hole spin QDs are typically around ≈ 1 μs [11, 12, 14], compared to ≈ 100 μs [5] for electrons, while reported Hahn-echo coherence times T_2 range from 0.2-1.9 μs [7, 14] for holes, compared to ≈ 30 ms for electrons [5]. Theoretical studies have identified sweet spots combining fast electric operation and long coherence and relaxation times for hole spins bound to Si:B dopants and QDs [18, 19, 63, 64], and hole spin coherence times rivaling electron spin in Si have now been observed experimentally in Si:B dopants [20] and Si quantum dots [21]. Understanding achievable coherence times both experimentally and theoretically for hole QDs is immensely important because coherence times set upper bounds on quantum operation fidelities (e.g. for one- and two-qubit gates), and improving coherence could increase the time between costly error correction cycles anticipated in future fault tolerant quantum computers. To date, theoretical models that account for realistic properties of holes in the valence band have not considered the role of realistic electric confining potentials produced by the gates, on qubit coherence and manipulation rates [18, 19, 39, 59, 63, 64].

Theoretical studies of planar QD hole spin qubits typically employ simplified electric potentials with harmonic lateral confinement and a spatially uniform gate electric field [19, 39, 65]. While it is expected that the qubit properties depend on device details, the deviation from ideal potentials and its impact on qubit performance have received scant attention. In a real device, the effects of the confining

potential and the vertical electric field cannot be completely separated as both are controlled by the applied voltages on the same set of gates. It is important to determine the extent of accuracy of the simplified models on hole qubit properties, such as coherence time and manipulation rates.

Here, we theoretically investigate the properties of QD based hole spin qubits in electric potentials produced by realistic gate patterns, under different conditions for strain and applied magnetic field direction. We compare the results obtained for potentials in realistic devices with results from toy potentials used in previous work. In this chapter we discuss the simulation attributes and setup used in this investigation. An overview of key parameters studied is also provided.

2.1.1 Spin-Orbit Coupling

In semiconductors the valence band orbitals are p-type in character, with an orbital angular momentum value $L = 1$. The resulting spin angular momentum value of $J = 3/2$ results in spin properties vastly different from those of electrons in the conduction band. The valence band contains heavy hole (HH) states, with $m_j = \pm 3/2$ and light hole (LH) states, with $m_j = \pm 1/2$. A third band called the split-off hole bad (SO) also exists, but its effects can be discounted in Ge as its separation in energy from the other bands is large [66].

The effect of vertical confinement in a quantum well will cause the degeneracy of the HH and LH subbands to be lifted when the wavevector $k = 0$, leading to a 'top' band composed of HH states at this point. At finite values of k, there will be mixing between the HH and LH bands, and the 'top' band will no longer be entirely composed of HH. This coupling between bands will contribute to the spin-orbit interactions that are so crucial to qubit operation.

Spin-orbit coupling (SOC) is a relativistic effect that occurs when a particle with a magnetic moment moves and experiences an effective magnetic field in its rest frame. In semiconductors, the existence intrinsic SOC alongside broken inversion symmetry leads to spin splitting of the doubly degenerate HH and LH bands at finite k values. At $k = 0$, spin degeneracy can be lifted by a applying a magnetic field B, and transitions between these spin states can be driven all-electrically.

Inversion asymmetry in semiconductors can either stem from properties of the crystal structure or from the confining potential. The latter will lead to the existence of Rashba SOC, while the former will lead to Dresselhaus SOC. In Ge quantum wells, Rashba SOC is the dominant method of spin-orbit interaction because the crystal has inversion symmetry..

Rashba SOC is crucial to the operation of hole spin qubits because it evovles non-linearly as a function of an applied electric field [19]. Thanks to this behavior, dephasing due to electric fields can be suppressed at optimal operation points for the qubit, leading to 'sweet spots' where the spin splitting between the qubit basis states is insensitive to electric field noise.

2.1.2 Luttinger-Kohn Model

The Luttinger-Kohn model is a flavor of $k \cdot p$ perturbation theory, a theoretical model used to approximate the band structure of materials [67]. Application of this model to a quantum-well heterostructure provides insights into the effect of SOC and strain on the energy splitting.

The Luttinger-Kohn model represents a wave-function as a sum over valence band Bloch functions at the Γ point, where $k = 0$, multiplied with slowly varying functions that depend on a periodic potential $U(r)$. Perturbation theory is used to account for areas outside the Γ point. The adjustment to the Hamiltonian is proportional to $k \cdot p$ and can be expanded in powers of the wave-vector components k_x, k_y, k_z.

In the case of valence band holes in a strained Ge heterostructure, the Luttinger-Kohn Hamiltonian H_{LK} can be written in the basis of HH and LH states, which have total angular momentum $J = 3/2$ and projected angular momentum $m_J = \pm 3/2$ and $m_J = \pm 1/2$ respectively. Split-off hole ($J = 1/2$) states are not considered in this work, which can be justified in Ge because the split-off valence band is 300 meV away.

H_{LK} is written in the basis of HH and LH states $\left\{|\frac{3}{2},\frac{3}{2}\rangle|\frac{3}{2},-\frac{3}{2}\rangle|\frac{3}{2},\frac{1}{2}\rangle|\frac{3}{2},-\frac{1}{2}\rangle\right\}$

as:

$$H_{LK} = \begin{bmatrix} P+Q & 0 & L & M \\ 0 & P+Q & M^* & -L^* \\ L^* & M & P-Q & 0 \\ M^* & -L & 0 & P-Q \end{bmatrix}, \tag{2.1}$$

where

$$P = \frac{\hbar^2\gamma_1}{2m_0}(k^2 + k_z^2) \tag{2.2}$$

$$Q = \frac{-\hbar^2\gamma_2}{2m_0}(2k_z^2 - k^2) \tag{2.3}$$

$$L = \frac{-\sqrt{3}\hbar^2\gamma_3}{2m_0}k_- k_z \tag{2.4}$$

$$M = \frac{-\sqrt{3}\hbar^2}{2m_0}\left(\left(\frac{\gamma_2+\gamma_3}{2}\right)k_-^2 + \left(\frac{\gamma_3-\gamma_2}{2}\right)k_+^2\right), \tag{2.5}$$

and m_0 is the free electron mass, γ_1, γ_2, γ_3 are Luttinger band-structure parameters with values of 13.15, 4.4, and 5.69 respectively [68]. The wave vector k is given by $k^2 = k_x^2 + k_y^2$ and $k_\pm = k_x \pm ik_y$.

2.1.3 Spin-Electric Dipoles

The coupling of spin qubits to homogeneous electric fields is described by the longitudinal and transverse spin-electric dipoles, χ and v, respectively. These electric dipoles are constructed from integrals p_{ijl},

$$p_{ijl} = \int \psi_i(r)^* q x_l \psi_j(r) d^3r. \tag{2.6}$$

that express couplings between states i and j due to an electric field along the l axis. The transverse electric dipole $v_l = p_{12l}$ determines the frequency $t_{\text{rabi}}^{-1} = vE_{AC}/h$ of the oscillation between qubit states $i = 1$ and $j = 2$ due to an applied electric field of magnitude E_{AC}, oscillating at the qubit frequency, along the l axis in space. The electric dipole matrix elements with $i = j$ describe the shift in energy of state i due to an electric field E along the l direction, and the longitudinal electric dipole $\chi_l = p_{22l} - p_{11l}$ determines the change in qubit energy $\Delta\varepsilon = \chi E$ due to that field.

In the presence of charge noise due to a fluctuating electric field, χ causes pure dephasing, limiting the coherence time of the qubit.

2.1.4 Electric Spin Manipulation

When a static magnetic field B is applied the degeneracy of the spin energy levels is lifted. Previously degenerate HH and LH states now each split into a spin-up and spin-down sublevels, with the energy separation proportional to the magnetic field, $\Delta E = g\mu_B B$, where g is the Landé g-factor, and μ_B is the Bohr magneton. The corresponding frequency $\omega = \Delta E/\hbar$ is called the qubit's Larmor frequency.

This external magnetic field is used to define the quantization axis of the spin qubit, and will cause the spins to precess around that axis. However, to create a set of universal quantum gates rotation about the qubit's other axes is required. This is accomplished using a time-varying in-plane electric field E_{AC} that causes the hole to oscillate in its plane of confinement. This orbital motion is then converted into spin oscillations through SOC [39]. When the frequency of the electric drive is on-resonance with the qubit's Larmor frequency, rotations about the selected axis can be driven. By adjusting the time duration during which the driving field acts on the qubit, specific quantum gates can be realized. The Rabi time t_{rabi} is the time taken to accomplish a gate operation, and is proportional to the product of the transverse electric dipole ν and the amplitude of the driving field E_{AC} as seen in Section 2.1.3. Since the Rashba SOC effect is electrically controllable, the Rabi time can be tuned by changing the amplitude of the vertical confining field E_z in the qubit. The Rashba SOC is also responsible for providing a correction to the qubit Larmor frequency in the case of non-zero electric field E_z. Due to the electrical tunability of the Rashba SOC, it is possible to optimize the qubit to operate in regions of maximum coherence time and maximum electric driving speed at the same time [19]. This is further discussed in Section 2.3.

2.1.5 Quantum Dot Occupation

Due to Coulomb repulsion, the occupation of the quantum dot can be controlled by changing the voltage on the gate electrode. The Hubbard model can be used to model the behavior of confined spins and to determine the occupancy of a quantum

dot system [69]. If quantum effects such as hopping are neglected, the Hamiltonian for a single QD with occupance of 0,1, or 2 holes can be modeled as $H = -\mu_1 \hat{n}_1 + U_C \hat{n}_{1\uparrow} \hat{n}_{1\downarrow}$, where $\hat{n}_{1\sigma}$ is the number operator, $\hat{n}_1 = n_{1\uparrow} + \hat{n}_{1\downarrow}$, μ_1 is the chemical potential, and U_C is the Coulomb repulsion integral between two holes residing in the same QD, defined as:

$$U_C = \iint |\psi(\mathbf{r_1})|^2 \frac{q}{4\pi\varepsilon_0\varepsilon_r|\mathbf{r_1} - \mathbf{r_2}|} |\psi(\mathbf{r_2})|^2 d^3\mathbf{r_1} d^3\mathbf{r_2} \tag{2.7}$$

where ψ is the ground-state wavefunction of a single hole. The eigenernergy can be expressed as $E = -\mu_1 n_1 + \frac{U_1}{2} n_1(n_1 - 1)$. For a QD with zero hole occupancy, $E_0 = 0$. For single-hole ocucpancy, $E_1 = -\mu_1$, and for two-hole occupancy, $E_2 = -2\mu_1 + U_C$. The charge state of the QD can be found be determining the lowest energy state.

2.2 Methods

The following section outlines the simulation set-up and analysis methods.

2.2.1 Simulation Design

The simulation makes use of QDs defined in strained Ge, using the the gate pattern shown in Figure 2.1. The structure consists of three gate layers separated by Al_2O_3 dielectric. The plunger gate diameter is 90 nm. The Al_2O_3 is 30 nm thick, with 15 nm between the gate and the active region of the device, 2.5 nm of the dielectric spacing between the plunger and the centre barrier. A hole QD forms beneath the plunger gate within the Ge when a negative voltage is applied to the plunger. Positive voltages applied to the barrier gates create a barrier to a reservoir (not shown). We assume the substrate growth direction is along $\hat{z} \parallel (001)$.

We obtain the eigenstates of the QD using the three-dimensional Kohn-Luttinger Hamiltonian for holes in the valence band. The valence band has p-like symmetry (orbital angular momentum $L = 1$). Heavy hole (HH) states are the states with total angular momentum $J = 3/2$ and projected angular momentum $m_J = \pm 3/2$ and light hole (LH) states are the states with $J = 3/2$ and projected angular momen-

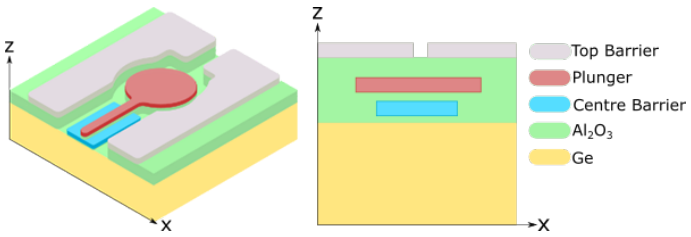

Figure 2.1: Isometric (left) and front view (right) of the single QD. Gates are contained within a 30 nm thick Al_2O_3 dielectric, which has been partially made transparent for clarity. Spacing is 2.5 nm between Al_2O_3 interface and centre barrier, 2.5 nm between centre barrier and plunger, and 5 nm between plunger and top barrier.

tum $m_J = \pm 1/2$, while split-off states are not considered for Ge as explained in Section 2.1.2. The Hamiltonian describing a single hole QD is:

$$H = H_{LK} + H_\varepsilon + H_Z + U(\mathbf{r}) \tag{2.8}$$

Here, H_{LK} is the Kohn-Luttinger Hamiltonian for the valence band [67], which accurately describes both QDs[59] and acceptor dopants [70, 71] and is defined in Section 2.1.2. In the total Hamiltonian, H_ε is a Bir-Pikus Hamiltonian for strain [70, 71], $U(\mathbf{r})$ is the electric potential energy, and H_Z is the Zeeman coupling between the hole and external magnetic field $\mathbf{B}$, given by

$$\begin{aligned} H_Z = \mu_B \big(& g_1 (J_x B_x + J_y B_y + J_z B_z) \\ & + g_3 (J_x^3 B_x + J_y^3 B_y + J_z^3 B_z) \big) \end{aligned} \tag{2.9}$$

where g_1, g_3 are the linear and cubic Lande g-factors respectively, μ_B is the Bohr magneton.

A summary of the simulation workflow is provided in Figure 2.3. First, the realistic gate pattern shown in Figure 2.1 is modeled using CAD tools. The voltages chosen for the gates (Figure 2.1) define the potential energy $U(\mathbf{r})$ for the QD, which is obtained from a finite element electrostatic calculation employing the gate pattern. The relative dielectric permittivity of different materials is taken into account. For comparison, a slice of the realistic potential alongside a harmonic

potential fitted to its curvature is shown in Figure 2.2.

We solve the full Hamiltonian numerically in the finite difference approximation, using the external potential $U(\mathbf{r})$, to find the eigenstates ψ_i (spin-3/2 spinors) and eigen-energies ε_i, and qubit energy $\varepsilon = \varepsilon_2 - \varepsilon_1$. The numerical solver uses infinite well boundary conditions in order to make direct comparisons with previous work [19, 39, 63, 64]. All calculations are presented for compressive strained Ge with -0.6 % strain, similar to the value expected for Ge quantum wells in the literature [11], and for comparison, strain-relaxed Ge quantum wells of 15.4 nm depth are also described.

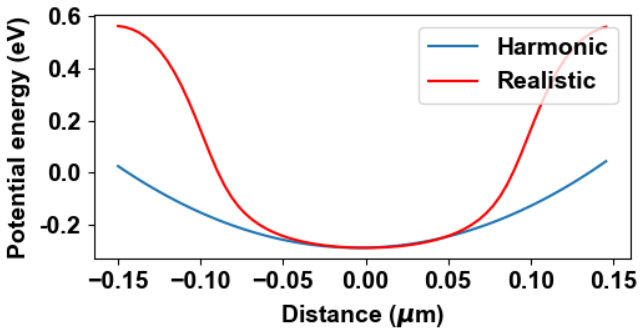

Figure 2.2: A slice of the realistic potential through the top of the semiconductor substrate is taken, with coordinates passing through the centre of the quantum dot. The plunger gate voltage is chosen to be -0.5V, and the barrier voltage is 1.06V. A harmonic potential is plotted for comparison, and fitted to have the same curvature as the bottom of the realistic potential. While clearly similar at the bottom of the potential, the two are very different far from the centre of the quantum dot.

The eigenstates ψ_i are computed numerically using two different assumptions: first, using a separable potential with a varying electric field, induced by the gate, in the vertical direction, and an electric-field-independent harmonic confinement in plane (toy potential), and second, using potentials predicted from voltages applied to the gates in Figure 2.1 (realistic potential).

The Kohn-Luttinger model contains terms incredibly sensitive to electric fields, so we think that the total Hamiltonian will look quite different based on the potential used. Key parameters such as coherence time and manipulation time can then

be extracted via numerical analysis. For the toy potential, a $a_0 = 13$ nm radius QD is modeled with a laterally harmonic potential and independently tunable vertical electric field E_z, $U(\mathbf{r}) = \frac{1}{2} m_p {\omega_0}^2 (x^2 + y^2) + qE_z z$, where $m_p = m_0/(\gamma_1 + \gamma_2)$ is the in-plane effective mass of the heavy holes and $\omega_0 = \hbar/(m_p a_0^2)$ is the harmonic oscillator frequency.

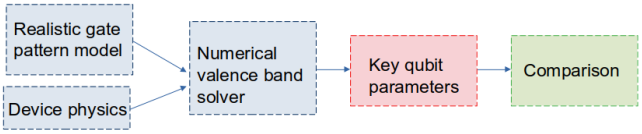

Figure 2.3: Chart showing simulation workflow.

2.3 Results and Discussion

In this section, the results from simulations of hole spin dynamics in a single QD using both harmonic and realistic potentials are presented, compared, and analyzed in the case of both strained and unstrained substrates.

2.3.1 g-factor and QD radius

For the toy potential, the effective qubit g-factor defined by the computed qubit energy splitting $\varepsilon = g\mu_B B$, is plotted as a function of vertical field E_z in Figure 2.4(a). The result of our finite numerical solution to the Kohn-Luttinger equations is in qualitative agreement with the variational calculation in ref. [19]. That is, we observe a local minimum in the g-factor, occurring here at $E_z \approx 7$ MV/m (strained) and $E_z \approx 3$ MV/m (unstrained) associated with the vanishing of dephasing from voltage fluctuations on the gates. This non-monotonic behavior of g as a function of the gate field was previously identified to arise from the non-monotonic behaviour of the Rashba SOI coefficient and enhanced coherence times in refs [72] and [19] respectively.

For the realistic potential, the effective qubit g-factor (QD radius) is plotted as a function of plunger gate voltage and average vertical electric field in Figure 2.4(c).

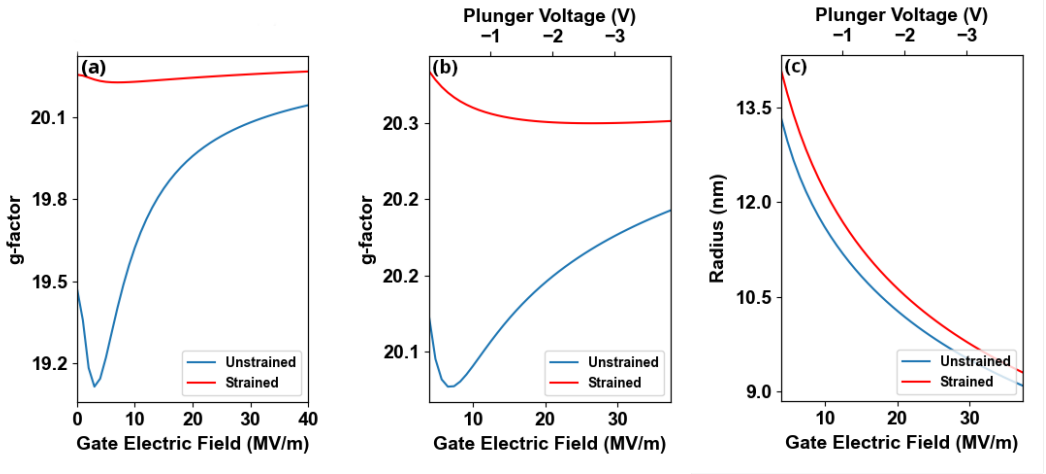

Figure 2.4: (a) Computed g-factor for toy potential as a function of vertical electric field, E_z, with fixed radius of 13 nm for strained (red, sweet spot at 7 MV/m) and unstrained (blue, sweet spot at 3 MV/m) cases (b) Computed g-factor for realistic potential versus plunger voltage and average gate-induced vertical electric field, $\langle E_z \rangle$, for barrier voltage of 1.06 V for strained (red, sweet spot at 26.6 MV/m) and unstrained (blue, sweet spot at 6.5 MV/m) cases. (c) Computed QD radius versus plunger gate voltage and $\langle E_z \rangle$ for the same barrier voltage as (b). All calculations use an out-of-plane magnetic field of 22 mT.

We define the average vertical electric field as $\langle E_z \rangle = \langle \Psi | - (d/dz) U(\mathbf{r}) | \Psi \rangle$ since the hole does not experience a uniform electric field E_z in realistic devices. For the realistic potential, we observe the local minimum in the g-factor for an average electric field of $\langle E_z \rangle \approx 26.6$ MV/m (strained) and $\langle E_z \rangle \approx 6.5$ MV/m (unstrained).

The appearance of the local minimum in the g-factor (or "sweet spot") in the realistic potential case is important because it means that qubit coherence is expected to be robust to voltage fluctuations in real devices, where the potentials differ from the toy potential in two material ways. First, the toy potential is purely harmonic, while the single qubit electric potential in Figure 2.1 is anharmonic, tending to zero far away from the QD. Second, the effective radius of the QD varies with average electric field, varying from 13.5 nm to 9.0 nm for the device we considered, as shown in Figure 2.4(c). When the realistic potential is taken into account,

we find that the "sweet spot" shifts to higher operation gate voltages in both the unstrained and strained cases, from 7 MV/m to 26.6 MV/m for the strained case, and 3 MV/m to 6.5 MV/m for the unstrained case, for QDs with the same nominal diameter (Figure 2.4). This occurs because of changes in the finite size of the QD with gate voltage, as follows. For the realistic potential, increasing the gate voltage magnitude modifies not only the Rashba coefficient via the electric field[19, 72], but also reduces the QD radius. At a fixed electric field, smaller radius reduces QD g-factor[73]. This reduction in g-factor from QD radius reduction (at fixed field) competes with the upturn in g-factor from increasing QD electric field (at fixed radius), pushing the "sweet spot" to higher electric fields. This shift is more pronounced for the strained device, moving the sweet spot from 7 MV/m to 26.6 MV/m, because the strained device has a smaller g curvature with E_z, at fixed QD radius (Figure 2.4).

2.3.2 Transverse and Longitudinal Dipoles

We now calculate the longitudinal electric dipole for the qubit states ψ_i for the realistic potential. The results are shown in Figure 2.5, which is are found to have stronger variation with electric field in the unstrained material, as expected from the smaller LH-HH splitting. Importantly, there exists a choice of gate voltage (electric field) where the longitudinal dipole vanishes both for strained and unstrained materials, *e.g.*, where dephasing from homogeneous electric fields vanishes to first order in electric field amplitude.

Protection from voltage noise and electric field noise would be preferable at the same operating point, but while this occurs for the toy potential, it does not necessarily occur for realistic potentials. This is directly shown in our results. For the realistic potential, the average electric field where the qubit is insensitive to voltage noise (Figure 2.4(b), strained: 26.6 MV/m, unstrained: 7 MV/m) is different from the gate voltage where the qubit is insensitive to electric field noise (Figure 2.5(b), strained: 10 MV/m, unstrained: 4.5 MV/m). For the toy potential, the average electric field where the qubit is insensitive to voltage noise (Figure 2.4(a), strained: 7 MV/m, unstrained: 3 MV/m) is the same as the average electric field where it is insensitive to electric field fluctuations (Figure 2.5(a)). In practice, there are

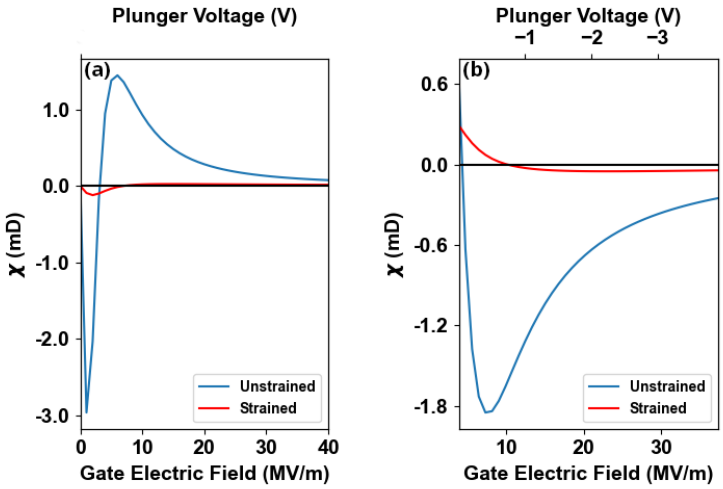

Figure 2.5: (a) Longitudinal dipole for the toy potential for both the unstrained and strained case exhibiting zero-crossings where the longitudinal dipole vanishes (strained: 7 MV/m, unstrained: 3 MV/m). (b)Same as (a), but for realistic potential case, exhibiting zero-crossings where the longitudinal dipole vanishes (strained: 10 MV/m, unstrained: 4.5 MV/m). Conditions for the calculation are the same as Figure. 2.

multiple sources of noise, including gate voltage noise, charge fluctuations, and electric dipole fluctuations. With our model, the impact of design choices on the properties of qubits experiencing realistic sources of electrical noise such as gate voltage noise, charge fluctuators, and electric dipole fluctuators, could be assessed, and designs and operating points could be identified which provide the best overall qubit performance.

It is easy to show that for the toy potential, the minimum for the g-factor will occur at the same average electric field as the vanishing of the longitudinal dipole, but for the realistic potential, the two do not necessarily coincide. For the toy potential, the perturbing potential for a fluctuating electric field δE_z is $\delta U(\mathbf{r}) = qz\delta E_z$ and the corresponding qubit energy perturbation is $\delta\varepsilon = \langle 2|qz\delta E_z|2\rangle - \langle 1|qz\delta E_z|1\rangle = \delta E_z\chi$, where $\chi = \langle 2|qz|2\rangle - \langle 1|qz|1\rangle$ is the longitudinal electric dipole. Therefore, the local minimum of g, which occurs at roots of $\partial\delta\varepsilon/\partial\delta E_z = \chi$, occurs exactly when the longitudinal dipole vanishes ($\chi = 0$). For the realistic

potential, the qubit energy perturbation due to the gate voltage change arises from changes in the potential $\delta U(\mathbf{r})$, and is given by $\delta\varepsilon = \langle 2|\delta U(\mathbf{r})|2\rangle - \langle 1|\delta U(\mathbf{r})|1\rangle$. The g-factor is independent of electric field when $\partial\varepsilon/\partial E_z = (\partial/\partial E_z)(\langle 2|\delta U(\mathbf{r})|2\rangle - \langle 1|\delta U(\mathbf{r})|1\rangle) = 0$. However, the potential $\delta U(\mathbf{r})$ cannot be characterized by a single value of E_z. Specifically, $E_z = -(1/q)(d/dz)U(\mathbf{r})$ varies with x and y (non-separable potential) and varies with z. Consequently, for the realistic potential, there is no reason to expect that the longitudinal dipole will vanish and g-factor will be minimized at the same electric field. In practice there will be multiple electric noise sources including voltage on gates, fluctuating charges on traps, and fluctuating charged dipoles in glasses.

2.3.3 One-hole regime alignment and dephasing time

We show now a procedure to shift sweet spots to the 1-hole regime, so that they can be exploited in single-hole qubits, and after that, calculate quasi-static T_2 to demonstrate that long coherence times can be obtained over large ranges of gate space. To determine the gate voltage range of the one-hole regime, we calculated the energy of the zero-hole, one-hole and two-hole states by considering the Coulomb interactions on a single QD[69]. We set the zero-hole energy E_0 as a reference point. Then, the one-hole energy E_1 is the ground state energy eigenvalue, ε_1, obtained from the numerical solver using the realistic gate potential as $U(\mathbf{r})$. The two-hole energy E_2 is $E_2 = \varepsilon_1 + \varepsilon_2 + U_C$, where U_C is the Coulomb repulsion integral as defined in Section 2.1.5. We have calculated the Coulomb repulsion integral by Monte-Carlo integration. The results for E_0, E_1 and E_2 are plotted as a function of applied gate voltage and average electric field in Figure 2.6. The one-hole regime occurs when the energy of the single-hole state is lower than the zero and two-hole states, $E_1 < E_0$ and $E_1 < E_2$.

To line up the one-hole regime, where $E_1 < E_2$ and $E_1 < E_0$, with the local minimum of the g-factor, we take advantage of the fact that the QD experiences a potential produced by multiple in-plane gates. We employ the insight that the difference between the plunger and the barrier gate voltages mostly controls electric field $\langle E_z\rangle$ experienced by the qubit, which should set the location of the sweet spot, and the mean value of the plunger and barrier controls mainly occupation.

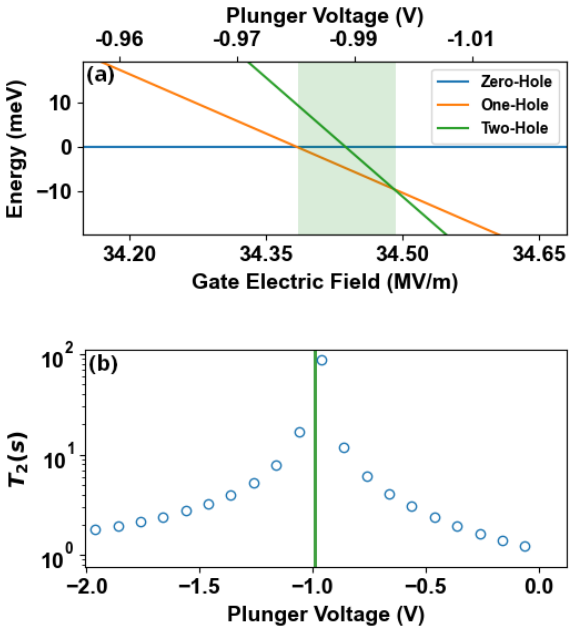

Figure 2.6: (a) Plot of the zero, one, and two-hole energies as a function of plunger voltage and $\langle E_z \rangle$ for the realistic potential. Note that the one-hole regime resides over a window of 15 mV in the plunger voltage range of $\sim$0.98-0.995 V. The sweet spot resides within this one-hole regime, having been shifted due to the application of a larger barrier voltage of 7 V. Conditions for the calculation are the same as Fig. 2. (b) The quasi-static T_2 time as a function of plunger gate voltage, and shaded region of one-hole regime, showing the line-up of the maximum (sweet spot) to the one-hole regime. One-hole regime is shaded in green for (a) and (b). Results are for strained Ge.

Varying the barrier gate voltage, we find that this shifts the plunger voltage where the g-factor minimum is found in Figure 2.4(b), and that the average value $\langle E_z \rangle$ of the electric field where the g-factor minimum experiences only small changes, due to the changing plunger gate voltage. This allows us to line up the local minimum at 34.46 MV/m with the one-hole regime in Figure 2.6 in the strained case (Figure 2.7 in the unstrained case). Interestingly, the local minimum has shifted from 26.6 MV/m to 34.46 MV/m during this procedure, due to the repulsive voltages

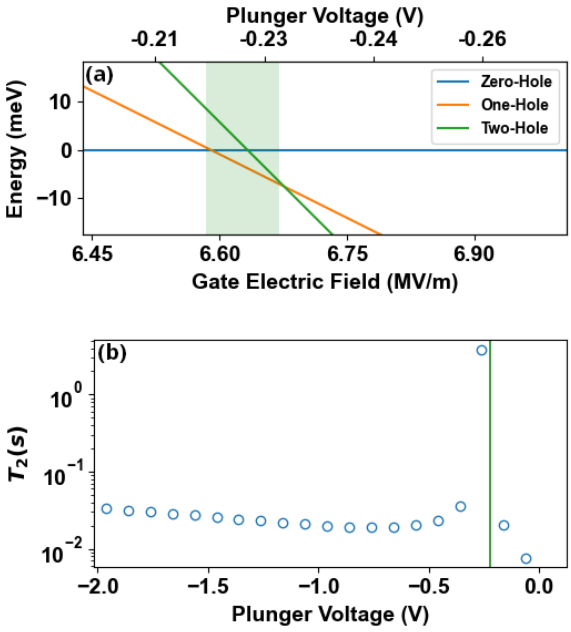

Figure 2.7: Plot of the zero, one, and two-hole energies (a) as a function of realistic gate potential and $\langle E_z \rangle$ for a barrier voltage of 1.3V. Note that the one-hole regime resides in the plunger voltage range of 0.227-0.217 V, giving the region a width of 10 mV. The sweet spot resides within this one-hole regime, having been shifted due to the application of a larger barrier voltage. The out-of-plane magnetic field is 22 mT, and the substrate is 15.4 nm thick unstrained Ge. The quasi-static T2 time is shown in (b). Note that the maximum occurs at the new sweet spot and thus within the one-hole regime. Results are for unstrained Ge.

applied to the barrier gates that further confine the QD, compared to the scenario in Figure 2.4(b). Similarly, the sweet spot can be shifted to the 1-hole regime also in the unstrained case (Figure 2.7).

To further investigate coherence at the predicted sweet spots in the realistic devices, we have computed quasi-static T_2 for the strained Ge, taking into account typical values of voltage fluctuations on the electric gates. The quasi-static T_2 is given by $T_2 = h/((\partial\varepsilon/\partial V)\delta V)$ where $\varepsilon = g(V)\mu_B B$. We use a plunger voltage noise $\delta V_p = 2\ \mu$V typical for quantum dots. Results are presented in Figure 2.6(b),

showing that the coherence time is maximized at a plunger around -1.0 V similar to the plunger voltage where the 1-hole regime is obtained Figure 2.6(a). The small curvature of the g-factor for the strained device results in long predicted coherence times over large ranges of gate space, compared to the unstrained case presented Figure 2.7(b).

As a consistency check, we examine the lever-arm of the plunger gate, which indicates the change in electrochemical potential of the QD per unit change in the electrostatic energy of the electrode [74]. The gate lever-arm is calculated using the average value for U_C as defined in Section 2.1.5 over a sweep of the plunger gate voltage at fixed barrier gates voltages, divided by the width of the one-hole regime. It is found to be ≈ 0.636, reflecting the relatively small dielectric thickness in the device design (Figure 2.1). As expected, the lever-arm is higher than values from the literature where gates are farther from the well. A lever-arm of ≈ 0.2 was found for Ge QWs capped with 22 nm GeSi and 20 nm Al_2O_3 [11, 14]. Our predicted lever-arm is similar to the lever-arm of 0.85 found for nanowire field-effect transistor based QDs with effective oxide thicknesses of < 2 nm [6].

2.3.4 Rabi time

We have evaluated the transverse dipole defined in Section 2.1.3 in order to understand the impact of the realistic device potential on the qubit manipulation rate. The EDSR Rabi time is obtained from the transverse dipole v using

$$t_{rabi} = \frac{h}{E_{AC}|v|}, \tag{2.10}$$

where E_{AC} is the strength of an oscillating in-plane electric field on resonance with the qubit. The trends in t_{rabi} and v are plotted as a function of applied gate voltage and average electric field in Figure 2.8.

Comparing the realistic and toy potential calibrated to the same curvature (QD radius), we find that the transverse dipole is significantly underestimated by the toy potential. Since our harmonic potential is chosen to reproduce the same curvature at the bottom of the anharmonic potential, the difference in the results is only due to anharmonicity. In particular, for realistic devices, the potential $U(\mathbf{r})$ approaches a finite value far away from the gates, where the energy level density becomes

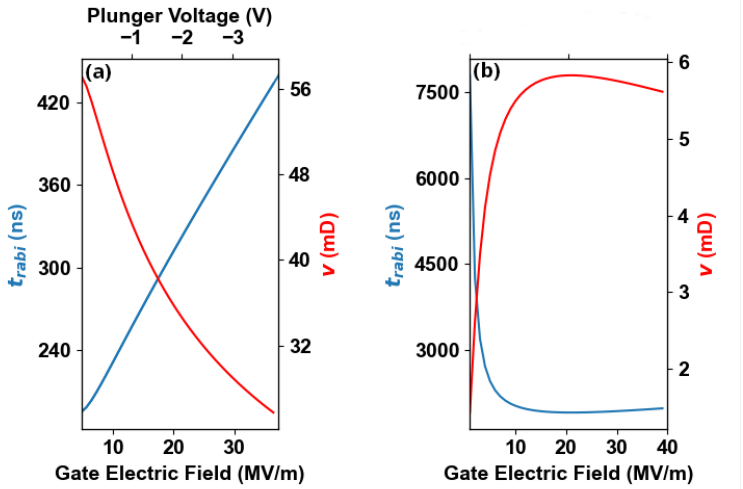

Figure 2.8: t_{rabi} (blue) and transverse electric dipole v (red) plotted as a function of applied gate voltage and average electric field for (a) realistic potential and (b) toy potential. The value of the driving field E_{AC} is 18 kV/m. All conditions are the same as Fig. 2.

very large compared to equally spaced levels in a harmonic potential. Though the toy potential is clearly unphysical for sufficiently highly excited states and at large distances where the potential diverges, it is convenient because it is usually believed to describe the lowest energy states well.

Our results imply that the toy potential is inadequate to describe the transverse electric dipole of the qubit. In particular, the change to wavefunctions and energy level densities from the anharmonic potential impacts the EDSR matrix elements greatly. In the framework of Schrieffer Wolff transformations [66, 75], the higher excited state energies and smaller wavefunctions of the unbounded parabolic potential reduce the transverse dipole and increase the EDSR time compared to the realistic potential.

The EDSR Rabi time is around 10 times smaller for the realistic potential, compared to the toy potential, for the same QD size. Specifically, for the same value of gate voltage ($\approx$ 10 MV/m) and AC electric field (18 kV/m), the EDSR Rabi time for the strained qubit is around 220 ns (2400 ns) for the realistic (toy) potential, for the device we have considered. This is a remarkable quantitative difference

between two approaches so similar at first glance, and highlights the importance of considering the anharmonic laterial confinement and inhomogenous vertical field to produce accurate qubit performance predictions. The increase of the transverse electric dipole compared to a harmonic potential implies a $\sim$100$\times$ increase in long-range two-qubit coupling mediated by electric dipoles, which is relevant to circuit quantum electrodynamics and direct electric dipole-dipole interactions [18, 60].

2.4 Conclusion

These results constitute the first predicted results of qubit properties that rely on a realistic description of lithographically defined QD devices, strain, and quantum mechanical theory for spin in the valence band. It is found that (a) sweet spots with long coherence times and fast electric control can still be identified for realistic devices where gate voltage not only controls the Rashba coefficient, but also changes the QD radius, and that the sweet spots occur for strained and unstrained devices, and (b) the qubit manipulation rate is significantly underestimated by harmonic potentials compared to realistic anharmonic device potentials. The increase by 10x of the transverse electric dipole compared to a harmonic potential implies a $\geq$ 100x increase in long-range two-qubit coupling mediated by electric dipoles, a significant result. From a high level, these results demonstrate a minimal model to evaluate the properties of qubits from device layouts, and underscore the need to describe both the device and quantum mechanical states of the valence band. In the future, this work could be extended to describe multi-qubit circuits.

2.5 Further Work

In the near term, some useful additions to this model would include the ability to calculate single qubit gate fidelities, as well as relaxation time T1. This should be relatively simple to implement and would make the model more versatile for predicting the properties of qubit systems.

Once these properties are determinable, a next step would be to model the platforms (and resulting potential) used in experimental work and compare the results obtained from the simulator to those obtained experimentally. This would provide a greater degree of validation for the simulator.

Long-term, the goal would be to transform this simulation framework into a simulation platform, so that it is more flexible and not only limited to single-qubit interactions. Quantum systems are challenging to model using classical means as they require computational resources that scale exponentially with the size of the system (solving this modeling problem is precisely why Feynman suggested building a quantum computer in the first place [76]) but it should be possible to model a two-qubit, double QD system. However, scaling the current model to two qubits would be challenging, since any model that accounts for two qubits must also treat the single qubit systems individually. This is something that can be explored.

Any simulation platform aiming to predict the properties of qubits will be fundamentally limited by complexity: for example, while it may be possible to model two qubits and their interactions to a reasonable degree of accuracy, but adding additional functionality, e.g., readout, will include the modeling and integration of another full quantum system (in this case, readout would be complex to model as it requires coupling of another quantum mechanical system, including a model for photons inside a resonator.

Chapter 3

Epitaxial Ge-Based Field-Effect Devices

A promising approach to solid-state quantum computing lies in using semiconducting materials to host qubits based on the spin of a single hole or electron, trapped in a quantum dot. Among the semiconductors investigated, silicon (Si) and germanium (Ge) emerge as the most promising for the realization of spin qubits due to their favorable properties and ability to leverage decades of knowledge in MOS fabrication techniques.

Devices based on Si and Ge both exhibit long coherence times [77, 78] enable quantum gate operations with high fidelity [79] due to the existence of nuclear spin-free isotopes.

Hole-spin based quantum dots are of particular interest due to their strong spin-orbit coupling, which allows for all-electrical manipulation. This allows for more flexibility and scalability in chip design compared to electron-spin qubits, which require on-chip magnetic fields [59].

For hole spin qubits, Ge presents several advantages over Si. Ge is able to form good ohmic contacts with most metals, facilitating the injection of holes into the the device [80]. Holes lack in Ge lack a valley degree of freedom, enabling better defined energy levels than are possible in electron spin qubits [78, 80]. Holes in doped Ge heterostructures exhibit the highest mobility of any 2-D hole system [81], and light effective mass [80] due to compressive strain in the quantum well.

This allows fabrication constraints to be relaxed, and facilitates the confinement of spins.Ge/GeSi quantum wells find applications as high sensitivity heterojunction photodetectors [82], optical modulators [83], and low-noise amplifiers [84]. However, ionized impurities are present in highly doped materials, and this leads to charge noise, leakage, and instability of the quantum device at low temperatures [80, 85]. For this reason, there is interest in developing quantum devices on nominally undoped Ge. Previous reasearch has developed fabrication processes for hole-FETs on undoped Ge/SiGe [80], and demonstrated that high hole mobilities and low effective masses are still achievable [85] in this material. There is also interest in developing quantum devices on unstrained Ge as opposed to strained Ge QWs. The use of epilayers over quantum wells would allow for higher thermal budgets during fabrication. The lack of strain also permits faster qubit manipulation times (as seen in Chapter 2). Finally, Ge-on-Si epilayers are an industrial material, with implementations in FinFETS [86], MOSFETs [87, 88], thermovoltaic cells [89], and avalanche photodiodes [90]. A sample gate stack for a strained Ge QW is shown alongside the gate stack for the unstrained Ge epilayer used to fabricate devices in this thesis in Figure 3.1.

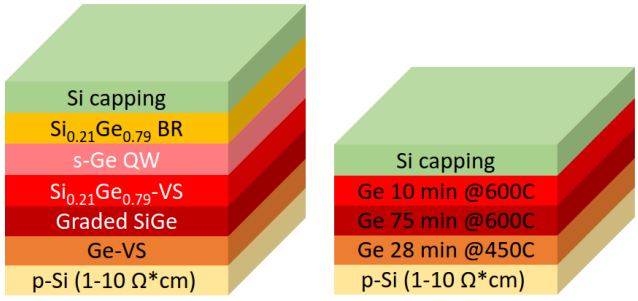

Figure 3.1: Left: Sample gate stack for Ge/GeSi strained QW based on a material received from Polytechnique Montreal. The Ge/SiGe heterostructure is grown on a Si buffer and consists of a Ge layer, graded SiGe layer, a strain-relaxed SiGe spacer, a Ge quantum well, a SiGe spacer, and a Si cap. Right: Gate stack of the Ge epilayer used in this work. It is grown on an Si buffer and consists of unstrained and nominally undoped Ge grown at different temperatures for different durations.

Here, we demonstrate the operation of an FET in an unstrained and nominally undoped Ge epilayer at 4K. We develop the gate stack, fabricate it in the UBC Nanofabrication facility, and test it at cryogenic temperatures. The device consists of metal source and drain contacts separated from the gate by a thin oxide layer. The FET works by applying a negative voltage to the gate, which accumulates holes beneath the oxide layer. A voltage applied between source and drain allows a current to flow in the channel.

We also develop, fabricate and measure Hall bar structures to determine the carrier concentration and mobility at 4K.

In this chapter we discuss the process used to design and fabricate the Ge FETs. An overview of the experimental setup used to characterize the transport properties of the devices is also provided.

3.0.1 Metal-Semiconductor Interfaces

A metal-semiconductor junction behaves either like a Schottky junction or an ohmic contact based on the energy barrier that an electron must surmount to move from the metal into the semiconductor. The height of this barrier depends on the difference between the metal and semiconductor work functions. Schottky junctions exhibit an asymmetric exponential I-V curve, and the energy barrier prevents current flow under zero bias conditions. The barrier can be overcome for appropriate voltages.

An ohmic contact exhibits a symmetric, linear I-V curve, and has a very small energy barrier: is a low-resistance junction. The barrier can be overcome through tunneling.

In practice, most metal-semiconductor interfaces form barriers, with the barrier height being relatively independent from the metal work function due the Fermi level in the semiconductor being pinned at a constant value near the valence band [91].

When the semiconductor is lightly doped the barrier is wide, preventing tunneling, and the barrier cannot be overcome by thermal excitation at cryogenic temperatures. A solution to this problem is to reduce the width of the depletion region through the use of highly doped semiconductors [92]; as the width of the region

narrows, tunneling from the metal to the semiconductor is increased. Thankfully, the barrier height of metal-Ge contacts is lower [91] than most other semiconductors [93], meaning that high doping concentrations are not required to fabricate quality ohmic contacts. In this work, we develop a fabrication method to create working Al ohmics on the Ge epilayer. The results are discussed in section Section 3.2.1.

3.0.2 FET Operation

A MOSFET is a type of voltage controlled transistor where the gate terminal is electrically isolated from the rest of the device by a dielectric layer. At its simplest, a MOSFET consists of either n or p-type doped substrate. A source and drain region are defined by heavily doped regions, which provide ohmic-type contacts to the source and drain metallized contacts. A gate electrode is deposited on top of a thin dielectric layer, creating a capacitor between the gate and body electrode.

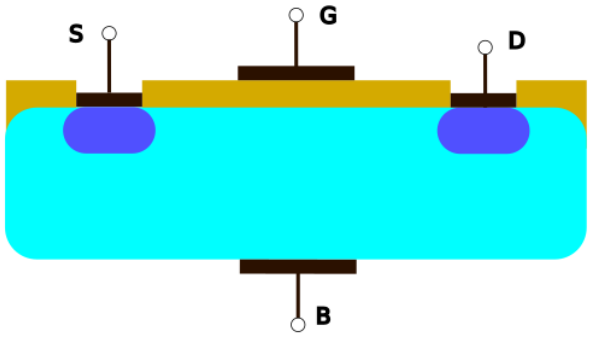

Figure 3.2: Simple schematic of a MOSFET showing the substrate (cyan), doping regions (dark blue), oxide layer (gold) and contact pads (black). The source (S), drain (D), gate (G) and body (B) contacts are shown.

When biased, this gate induces an electric field within the body of the MOSFET. For a p-type substrate, a negative voltage will cause accumulation layer of majority carriers (holes) to form near the semiconductor-oxide interface. Even if a source-drain bias is applied in this instance, current will not flow due to the existence of a reverse biased p-n diode in the path from source to drain. In the absence of these doped regions for source and drain, a current will flow.

If a positive voltage V_{GS} is applied to the gate, there will be a displacement of holes away from the interface, creating a layer of fixed acceptor atoms called a depletion region. The valence band edge bends down away from the Fermi level near the interface.

If the positive voltage is increased, the electric field strength increases, and with it the width of the depletion region. If the Fermi level dips below the intrinsic Fermi level near the interface, the substrate becomes n-type in character and an inversion layer begins to form. For $V_{GS} > V_T$, the threshold voltage of the semiconductor, the inversion layer becomes a channel connecting the source to the drain.

For gate voltages above V_T, applying a small drain voltage (V_{DS}) will cause the electrons in the inversion layer to flow from the source to the positive drain terminal, giving a current I_d. In this region, the channel behaves like a resistor where the channel conductance g_d is modulated by the gate voltage.

As V_{DS} increases, the effective voltage drop across the oxide at the drain end decreases, reducing the amount of inversion layer charge. This decreases the slope of the $I_D - V_{DS}$ curve. For values of $V_{DS} < V_{GS} - V_T$, the device is in the linear regime of operation. As V_{DS} is increased above the aforementioned threshold, the channel at the drain begins to pinch off, entering the saturation region.

Since mobility of the carriers is not constant due to the application of a varying electric field, the transconductance is defined as $g_m = \frac{\partial I_D}{\partial V_{DS}}$. The current-voltage relation in the linear regime is $I_D = \frac{WC\mu_{FE}}{L}(V_{GS} - V_T)V_{DS}$ where W is the channel width, L is the channel length, and C is the capacitance of the gate oxide. If this relationship is used in the equation for transconductance, the field-effect mobility can be extracted as $\mu_{FE} = \frac{Lg_m}{WV_{DS}C}$. This makes sense: it is expected that the transconductance increases linearly with V_{DS} but is independent of V_{GS} in the linear regime.

The field-effect mobility for a fabricated FET is extracted in section Section 3.2.1.

3.0.3 Hall Effect

A Hall Effect device is used to measure common semiconductor parameters of carrier mobility, carrier concentration, and carrier type (electrons or holes). When a charge carrier is moving with velocity $\vec{v}$ in a magnetic field $\vec{B}$, it will experience a

Lorentz force $\vec{F} = q\vec{v} \times \vec{B}$ in a direction orthogonal to the field and to its movement. These charge carriers will be deflected by the field and build up on the surface of the semiconductor, creating an electric field $\vec{E}$. In steady state, the net force on the charge carriers is zero, so (assuming a current I_{xx} in a field B_z), $E_y = v_x B_z$. The Hall voltage is then given as $V_{xy} = E_y W$, where W is the width of the Hall Bar. This is illustrated in Figure 3.3.

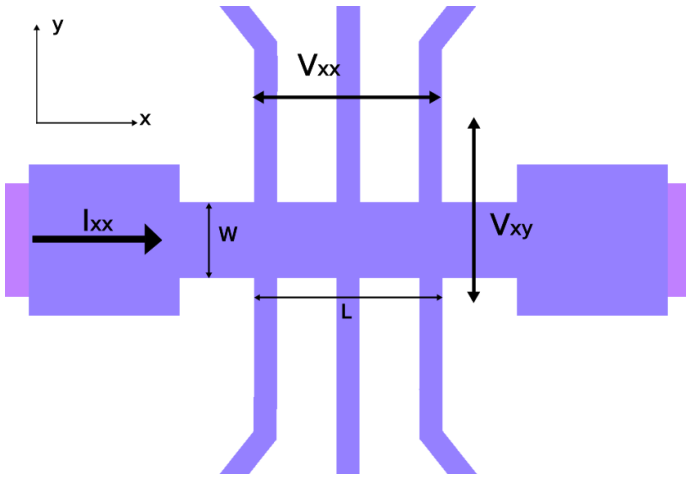

Figure 3.3: Schematic of a Hall bar showing the direction of current and measured Hall voltage V_{xy} as well as longitudinal voltage V_{xx}. Note that the voltages are, in reality, measured at bond pads that are not shown in the image. Dimensions of the Hall bar, W and L are also shown.

For a p-type semiconductor, the velocity of holes in an electric field is given as $v_x = \frac{I_{xx}}{qpWt}$, where p is the charge density of holes and t is the thickness of the semiconductor. By defining the transverse resistivity as $\rho_{xy} = V_{xy}/I_{xx}$, the former relations can be substituted to give an expression for the hole concentration: $p = \frac{B_z}{\rho_{xy} t q}$.

In addition to measuring the transverse resistivity ρxy, a measurement of the longitudinal resistivity ρ_{xx} can be obtained in the absence of magnetic field, simply be measuring the voltage developed across the direction of the current. This second measurement is necessary to determine the Hall mobility of the charge carriers. The mobility can be extracted by considering the current density along the direction of motion: $\mu_p = \frac{I_{xx} L}{qpV_{xx}Wt}$. If the transverse resistivity is defined as $\rho_{xx} = \frac{V_{xx}W}{I_{xx}L}$, then

the mobility can be found as $\mu_p = \frac{r_H}{\rho_{xx}}$, where r_H is the Hall coefficient, $\frac{1}{ptq}$.

3.1 Experimental Methods

The following section outlines the fabrication and measurement process for the device.

3.1.1 Device Design

The design of the FET is as follows: the ohmic contacts for the source and drain are made of Al which is deposited on the Ge wafer. The source and drain contacts have a width W of 20μm and a separation distance, L of 10μm. This separation distance is where the channel will form upon application of a gate voltage. After deposition of a thin dielectric oxide layer, a gate layer is deposited overtop the source and drain. The gate has a width of 40 μm and overlaps the source and drain electrodes by 15 μm on the sides and bottom. The reason for the overlap is to allow the channel to form as close as possible to the source and drain.

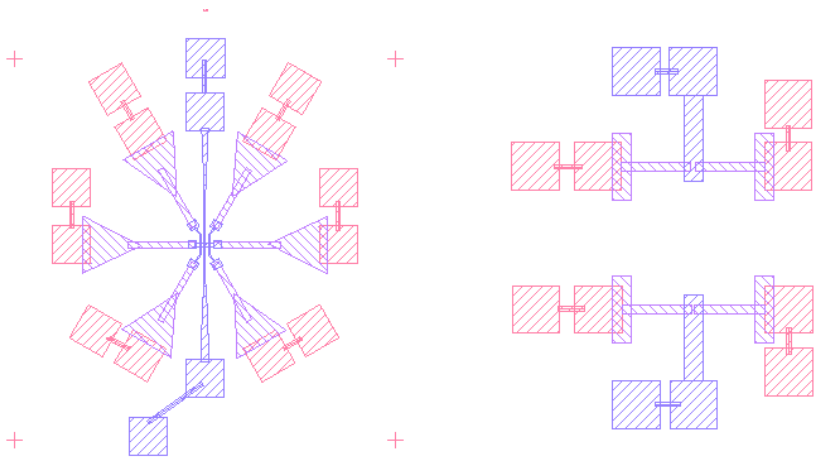

Figure 3.4: Top view of the layout design file for the Hall Bar (left) and FET (right) with scale bar. The ohmic bond-pads are red, the ohmic contacts are purple, and the gate layer is blue.

The Hall bars are fabricated as follows. The ohmic bond pads are placed far enough away from the centre of the device so to accommodate a second back-up

bond pad (in the case of poor electrical contact during wire-bonding) and allow sufficient space between the ohmic contacts. The ohmic contacts are tapered towards the centre of the device, and sufficient spacing is left between the ohmic contacts to allow space for the gate layer. The gate layer consists of a 10 μm by 20 μm rectangle where a channel is expected to form. The dimensions of this area are chosen to be much larger than the expected phase coherence length expected from Hall measurements in this type of material [94]. This central area is bordered by six horizontal contacts that overlap with the ohmic contacts. The voltage probes leading to these contacts are made as thin as possible to allow precise voltage measurements along the length of the Hall Bar. The minimum feature size is 3 μm. This is a convenient physical size for devices fabricated by optical lithography, which becomes challenge for features sizes below 1 μm. Two thin gate electrodes are added and connected to the Hall Bar centre with a tapered connection. These electrodes will allow for the application of a gate voltage, if desired, during the magneto-transport measurements. The gate layer is isolated electrically from the ohmics layer by the oxide. The design of the FET and Hall Bars is illustrated in Figure 3.4.

3.1.2 Device Fabrication Process

The FET and Hall Bars are fabricated on a Ge substrate. The material consists of unstrained, nominally undoped Ge layers epitaxially grown on a Si wafer and capped with an thin Si layer which itself has a thin SiO_2 layer on top, formed by partial oxidation of the thin Si layer. The thickness of the Ge layers is 3μm and the Si layer has a thickness of 4 nm. The devices are fabricated in the UBC Nanofabrication facility using a three-step process. The ohmic and gate pattern are created by lift-off, which benefits from am undercut resist profile. The undercut resist profile was obtained using the image-reversal mode of the AZ5214 resist in optical lithography. After the resist is developed for the ohmic layer, the chip subjected of oxygen plasma treatment and then dipped in diluted hydrofluoric acid. The former removes any remaining resists in the pattern area, and the latter removes a thin native oxide that can affect the formation of ohmic contacts.

The ohmic contacts are created by depositing 20 nm of Al by e-beam evapo-

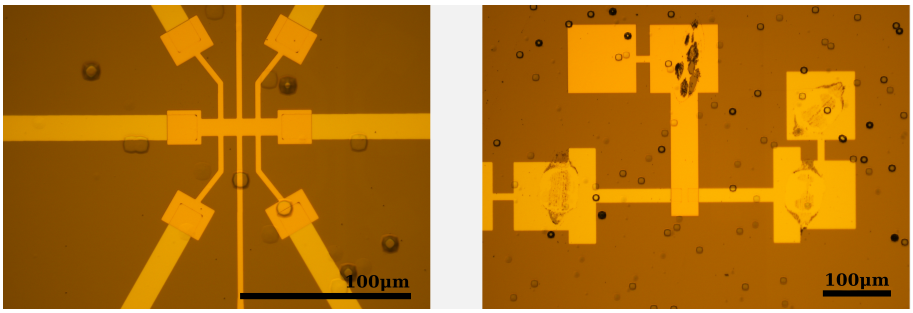

Figure 3.5: Top view optical microscope images of a fabricated Hall Bar (left) and FET (right) with scale bar. The ohmics are light gold in color, and the gate layer is a darker gold. Black dots are carbon impurities present in the wafer.

ration. A 20 nm layer of Al_20_3 is then chemically deposited at a temperature of 250 °C using an atomic layer deposition (ALD) system. This is followed by deposition of a gate and bond-pad layer consisting of 80 nm Au with a thin 5 nm layer of Ti underneath to improve adhesion. The bond pads allow electrical connections to be made to the device.

The Al_2O_3 oxide is then etched from the ohmic bond-pads with hydrofluoric acid, and the devices gate and ohmic bond-pads are wirebonded. Ideally, a mesa would be etched into the Hall bars to create a well defined channel for conduction. However, the process was expected to etch away up to 3 μm of the Ge waver as well. The Ge layer is a total of 3 μm thick, which makes removing the layer somewhat difficult, a step we omitted from the process.

An image of the fabricated devices is shown in Figure 3.5.

3.1.3 Measurement Setup

Two different sets of measurements are done on the fabricated devices.

First, the Ge FETs are tested in a dunker at 4K. The measurement is done inside a Dewar of liquid 4He. The chip is mounted on a chip holder that is built-in to a cold finger. This cold finger is mounted on a dip stick which is inserted into the dunker and sealed off from the external environment. A breakout box is electrically connected to the chip via a 1 $k\Omega$ resistor inside the dip stick. The breakout

box contains switches that are each connected to a different pad on the chip holder. A Keithley 2400 source is used to provide the gate voltage and connected to one of the input lines on the breakout box. In addition to acting as a DC voltage source, it also has an internal ammerter in series which allows it to simulataneously measure currents. Therefore, it is also used to measure the gate leakage current. A Stanford Research Systems lock-in amplifier is used to provide a constant drain-source voltage and also to measure the drain-source current. Its voltage output and current input lines are connected to the breakout box as well. Both the Keithley and lock-in are controlled remotely via a GPIB cable and a Python interface, so the voltage can be programatically set and the measured current sampled during testing. A schematic of this setup is included in Figure 3.6.

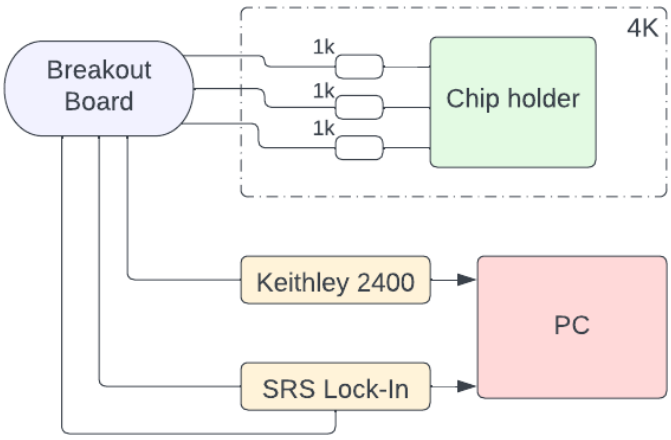

Figure 3.6: A diagram of the measurement setup for the dunker. The Keithley provides a voltage and contains a built-in ammeter. The lock-in also supplies a voltage and has a separate input to measure current.

The Ge Hall bars were tested in a Quantum Design Physical Property Measuring System (PPMS). The PPMS provides an isolated and controllable environment in which to run magnetotransport experiments. The temperature and magnetic field that the Hall bars experience is remotely controllable. The chip is mounted onto a chuck with contact pads that allows for the application of a current, and allows the resulting voltages that develop to be measured. The temperature is chosen to be

5K and the magnetic field is swept during the experiment.

3.2 Results and Discussion

In this section, experimental results of both Ge FETs and Hall Bars are presented and their significance is discussed.

3.2.1 Ge FET Measurement

The purpose of the 4K test in the dunker is to determine whether a) the ohmics are functional at low temperature and capable of sourcing current to the FET and b) whether the voltage applied to the gate electrode can control the source-drain current. First, it is necessary to verify that the gate dielectric acts as an electrical insulator. This is done by measuring the current that flow from the gate to the source under zero applied bias from source to drain. The current should ideally be far less than the expected value of the drain-source current. Otherwise, the device cannot be used as an FET. During testing, this gate leakage current is found to about 0.1 nA, indicating that the gate dielectric is sufficiently insulating. The next steps is to apply a small drain source bias such that $V_{DS} \leq k_B T$ and to measure the current I_D in the linear regime of operation. During this test, the gate voltage is swept from positive to negative values and vice versa several times. Figure 3.7 shows a measurement of the conductance $G_{DS} = I_D/V_{DS}$ extracted from the measurements of the current I_D for one of the FET devices.

The device operation is p-type, since current increases up as gate bias decreases (holes are accumulated). Further, there is no noticeable change in conductance for highly positive voltage in the 4-6V range. The device functions in accumulation mode, as it is already conducting at 0V. The most visible change in conductance occurs from 4 to 3 V, with the current appearing to begin saturating around -4V. There is a significant amount conductance even in the region where a highly positive gate voltage would be expected to turn the device fully off. This indicates that there is a significant amount of of background conduction, which suggests that the wafer was unintentionally doped. These dopants form a conductive background that cannot be controlled by the gate electrode. Hysteresis effects are also observed in the sweeps of V_{GS}, indicating the build-up of charge at the semiconductor-oxide

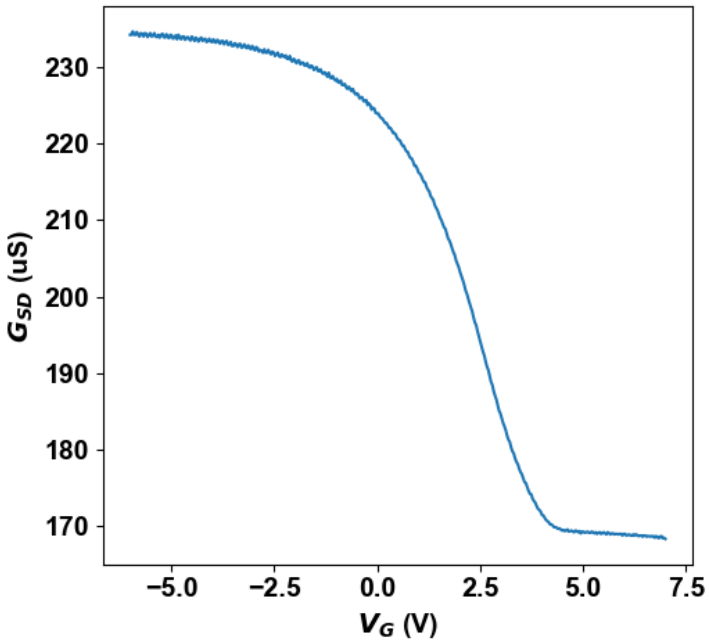

Figure 3.7: Sweeps of source-drain conductance vs gate voltage for an FET with channel length (width) of 20 μm (10 μm).The drain-source voltage is 400 μV.

interface.

A second possible explanation for the saturation of the drain current would be the existence of interface states. This is plausible as there is a large amount of background conduction observed, meaning that the existence of donor states near the semiconductor oxide interface is possible. These states provide energy levels that can trap holes, reducing the amount of mobile charge carriers and contributing to scattering effects near this surface. This has the effect of saturating I_D and triggering hysteresis [95].

The total resistance between the source and the drain can be modeled as $2R_c + R_{ch} + 2R_m$ where R_c is the contact resistance, R_{ch} is the channel resistance, and R_m is the resistance of the metallic contacts, assumed to be negligible. From this curve we can extract an upper bound on the contact resistance. If the saturation of the drain current in the ohmic regime is assumed to be due to the channel resistance

dropping well below the contact resistance, the contact resistance can be upper bounded by the total resistance which is given by 2.15 $k\Omega$.

Because R_c increases as $1/W$, the value of $R_c \times W$ can be compared to devices fabricated using the same fabrication procedure. For an FET with 30 nm Pd ohmics and a W value of 5 μm, the value of $R_c \times W$ is found to be 0.01 Ωm [35], which is similar to value of 0.02 Ωm obtianed for this measured device's $R_c \times W$ value.

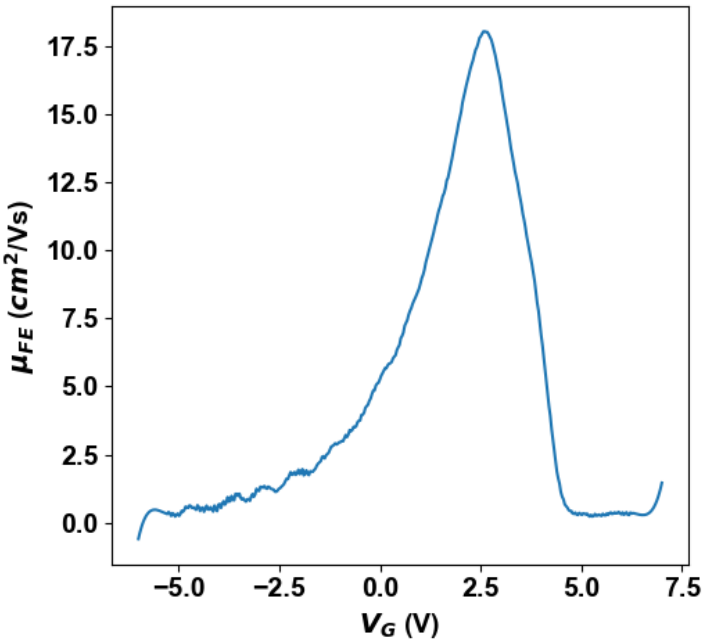

Figure 3.8: Sweeps of field-effect mobility vs gate voltage for an FET with channel length (width) of 20 μm (10 μm). The blue curve represents a sweep from +6 to -6 V on the gate. The drain-source voltage is 400 μV.

The field-effect mobility μ_{FE} is extracted from the transconductance data as explained in Section 3.0.3. Its peak value is found to be 17.5 cm^2/Vs. This mobility value represents the mobility of carriers in the semiconductor that are induced in the channel. These carriers come from the dopants in the substrate or are sourced from the ohmics. This mobility value is quite low compared the value of 400 cm^2/Vs obtained in a similar device also fabricated using a Ge epilayer and Al ohmics. [87]. One difference between the fabrication methods of the devices in

[87] and the ones in this work that may account for the disparity in mobility values is the temperature at which the gate oxide is deposited. The annealing of the ohmic contacts takes places during the deposition of the Al_2O_3 layer, and is performed at 250 °C for the devices in this work, and at 400 °C for the devices in [87]. The higher temperature may have led to stronger diffusion of Al atoms into the substrate, resulting in a higher p-doped area. As doping reduces the barrier width that carriers need to surmount, the observed mobility is likely higher in [87].

Another possible explanation for this disparity comes by analyzing the doping concentration. Since there is strong background conduction in the FET independent of gate voltage, it is possible that this device has been unintentionally doped with a high enough concentration to surpass the insulator-to-metal threshold of $2.3\times10^{17}cm^{-3}$ [96]. Since mobility is inversely proportional to doping concentration, it is likely the fabricated device experiences more ionized impurity scattering, leading to lower mobility.

3.2.2 Ge Hall Bar Measurement

The goal of the PPMS measurements is to determine the concentration of carriers in the substrate determine the Hall mobility of these carriers. The Hall bar is cooled to 5K inside the PPMS and a current of 50 μA is applied to the horizontal electrodes as illustrated in Figure 3.3. The magnetic field is swept from -5 to 5 Tesla and the resulting resistivity values, ρ_{xx} and ρ_{xy}, are measured and saved. The transverse (R_{xx}) and longitudinal (R_{xy}) resistance values are plotted as a function of magnetic field in Figure 3.9.

The longitudinal resistance data exhibits weak antilocalization, which has been previously observed in Ge epilayers [94]. The observation of weak antilocalization indicates that there is strong spin-orbit coupling present. The Hikami-Larkin-Nagaoka (HLN) model can be used to extract the phase coherence length l_ϕ, which is a measure of the distance an hole can propagate while maintaining phase information for the orbital degree of freedom. By fitting the data in Figure 3.9 to the HLN model, the phase coherence length is found to be $\sim$90 nm. A plot of the original and fitted data is shown in Figure 3.10.

The Hall mobility (μ_H) and carrier concentration (p) are extracted from the

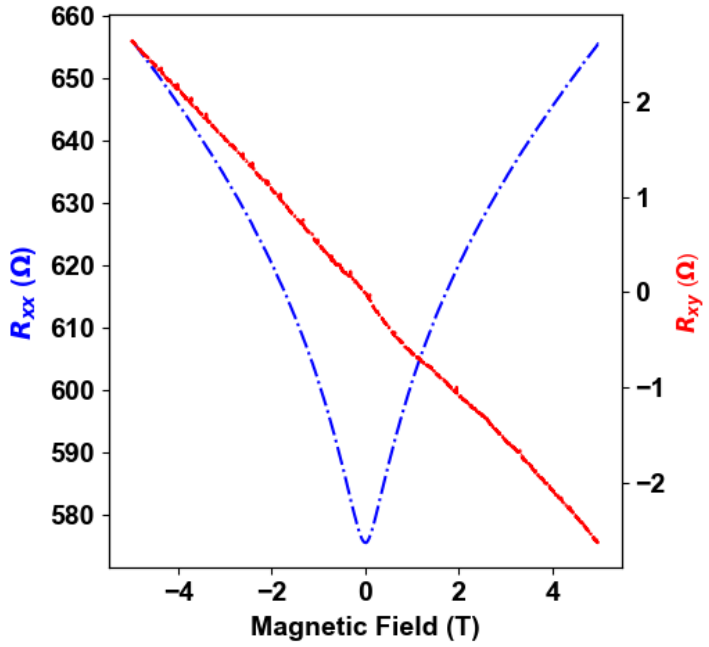

Figure 3.9: Longitudinal (R_{xx}) and Transverse (R_{xy}) resistance as a function of magnetic field at 5K for a Ge epilayer 3 μm thick. R_{xy} is scaled to show the change in conductivity relative to the zero field conductivity.

data as explained in Section 3.0.3 and the results of all the measurements done on the Ge devices are summarized in Table 3.1.

There is no gate voltage applied to the Hall bar during testing. When comparing the Hall mobility obtained to the field-effect mobility, it is reasonable to compare it not to the peak value but the gate voltage value similar to the built in voltage of the device. By taking the difference between the work functions of semiconductor (Ge) and metal (Al) we can find this 'effective' gate voltage to be 0.67V. At this value, the field-effect mobility is 3.5 cm^2/Vs.

Typically, the field effect mobility will be lower than the Hall mobility. This is the case for the devices tested, even though the Hall mobility and field-effect mobility values are quite similar. This is likely due to a high concentration of impurities near the semiconductor-oxide interface, leading to carriers sourced from ohmic contacts experiencing the same scattering effects as carriers in the substrate.

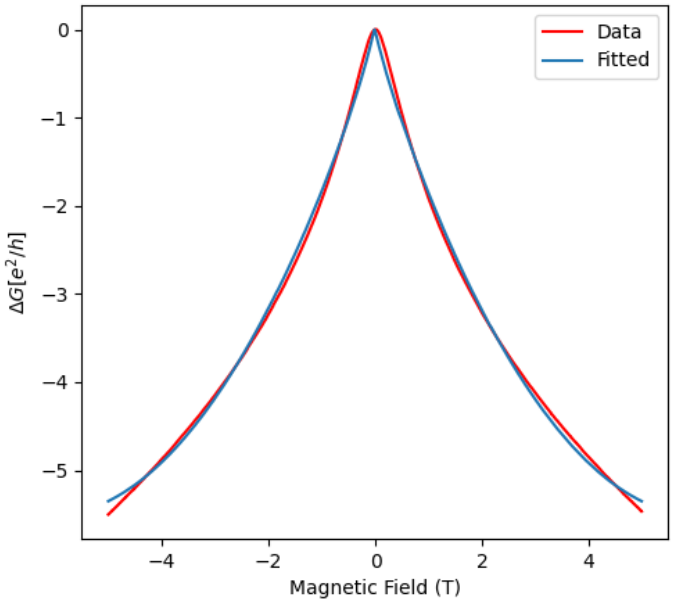

Figure 3.10: Plot of ΔG, the change in conductivity relative to the zero field conductivity, for both the original data (red) and fitted data (blue). The fit was done using the HLN model.

μ_{FE} $[cm^2/Vs]$	μ_H $[cm^2/Vs]$	p $[cm^{-3}]$
17.5	9.8	5×10^{18}

Table 3.1: Key properties extracted from Hall bar and FET measurements.

It is also apparent that the unintentional doping of $5\times10^{18}cm^{-3}$ in the substrate is significant. This represents an increase of two orders of magnitude compared to the concentration in [87]. This is past the insulator-to-metal transition value, supporting the hypothesis behind the high background conduction seen in Section 3.2.1.

At these doping levels, there is minimal effect of temperature on Hall mobility, so the Hall mobility of holes in similarly doped Ge at 77K [97] can be compared to

that found at 4K. The mobility at 77K is 500 cm^2/Vs, which is significantly higher than the μ_H of the germanium epilayer device, 9.8 cm^2/Vs. The low mobility is likely due to scattering effects from impurities.

3.2.3 Conclusion

I designed and fabricated accumulation mode field-effect transistors (FETs) and Hall bars based on a nominally undoped and unstrained germanium epilayer wafer. The FET was tested at 4K and it was determined that the ohmics were capable of sourcing current at low temperature, and that the voltage applied to the gate electrode can indeed control the source-drain current.This is a novel result, given that no studies on fabricating ohmic contacts for unstrained Ge spilayers for operation at low temperatures exists.

The device followed typical $I_d - V_G$ characteristics, an impressive result considering that this is the first low-temperature test of an unstrained Ge epilayer device. Significant background conduction was observed, and the field-effect mobility was low compared to similar devices [87]. For this reason, the material quality would need to be significantly improved if intended for use in quantum dot devices.

Analysis of the magneto-transport data from the Hall bars showed that there was significant unintentional doping in concentrations higher than the metal-to-insulator transition threshold for Ge: it is likely that this unintentional doping contributes to the high background conduction and low mobility observed in the FETs.

Chapter 4

Conclusion

Quantum computers are able to perform calculations that are intractable on classical computers. Their increase in computational power is due to their ability to harness and manipulate quantum properties such as superposition and entanglement. Rapid technological advancements has led towards a push in scaling up the number of qubits in quantum processors. State-of-the-art hardware is capable of achieving two-qubit operations with an error rate $> 0.1\%$, and it is not known whether this can be maintained when scaling up to larger systems. Because of the significant error rates present. While small-scale executions of quantum algorithms algorithm have been demonstrated [98], modern quantum processors are limited in size due to noise. While quantum error-correction (QEC) algorithms exist, they require a large number of physical qubit to encode a logical qubit state, far more than are currently available. Therefore, it is not expected that these processors will be able to achieve quantum supremacy, that is, to perform calculations that are demonstrably intractable on a classical computer [3]. In the meantime, research is focused on the development of hybrid quantum-classical algorithms, in which a quantum processor is used to prepare an n-qubit state, then measure and process the outcomes using a classical optimizer. There is hope that this approach will allow near-term quantum processors to achieve some advantage over classical methods. A processor with several million qubits is predicted to be able to not only implement QEC but implement quantum algorithms capable of breaking modern encryption [99]. Scaling up from current state-of-the art processors to ones containing several mil-

lion qubits poses a great challenge, both in the quality of the qubits and the control electronics required. Many different quantum hardware platforms exist. Among them are quantum dot (QD) spin qubits, which are the subject of this thesis. They are an appealing option because of their compatibility with existing CMOS fabrication techniques, their long coherence times, and their compact design which allows for denser packing of larger numbers of qubits.

For processors in Si, state-of-the-art developments include high fidelity single-qubit gates [15], small-scale algorithms [16], and a six-qubit processor capable of 3-qubit entanglement [17]. However, there are significant challenges to scaling up to more than 50 qubits. Some of these challenges include mitigating electric noise, and allowing for precise control over individual qubits.

Hole spin qubits are an attractive option to the electron spin qubit mentioned above. They have strong spin-orbit coupling (SOC) so they can be manipulated all-electrically, removing the need for complex magnet designs required on electron spin qubit platforms. Additionally, they are able to operate at locations called sweet spots where the effects of voltage and electric field noise are negligible while maintaining long coherence times [19]. State-of-the art advances in hole spin qubits include the demonstration of two and four-qubit processors [10, 14]. These properties and recent advances make hole-spin qubits a very promising candidate for scalable quantum computers. Despite their potential, very little work has been done towards enabling the scalability of hole-spin qubits. One avenue towards enabling scalability that has been explored for superconducting devices is the creation of simulation software. We believe that if something similar were created for hole-spin qubits, it would aid in rapid design and prototyping that would enable the creation of high-quality, mutli-qubit processors.

Typically, properties of hole spin systems are determined using simplified electric potentials that assume complete separability between a harmonic lateral confining potential and a linear vertical confining potential. These idealized models are then used to compute key qubit properties such as coherence and manipulation rates [18, 19, 39]. In a realistic device, the potential is not separable. Since the SOC strength is strong and highly sensitive to variations in electric field, it is likely that device geometry, and therefore potential, will have a significant impact on qubit properties. It is important to determine the effect of using realistic potentials

on qubit performance, if any, and to compare these results to existing calculations to determine whether there is a noticeable change in qubit properties when using realistic device potentials.

In this thesis, we develop a simulation framework that predicts key properties of hole spin qubits in Ge QDs by using the potential distribution found in a realistic device. To check the validity of our simulator, it is first tested with a standard harmonic potential, and compared qualitatively to previous work [19]. Once the simulator is validated, a realistic potential is used to calculate qubit properties such as the g-factor, spin-electric dipoles, and coherence times in the case of both strained and unstrained Ge substrates. It is shown that (a) a sweet spot where the qubit is insensitive to voltage noise still exists for the realistic potential case, despite significant QD radius variation due to a non-harmonic potential, and that his sweet spot occurs for both strained and unstrained devices, (b) long coherence times and fast electric control still exists at these sweet spots, and (c) the qubit manipulation rate is significantly underestimated by harmonic potentials compared to realistic potentials by about 10x. This implies a 100x increase in two-qubit gate times, which is a very significant result. We determine that device geometry has a significant effect on qubit properties that must be accounted for, and that therefore a minimal model that evaluates the properties of qubit based on device layout is an critical tool that necessitates further development. In the future, this work could be extended to describe multi-qubit processors. Ultimately, the creation of a comprehensive simulator for hole-spin qubits would allow the design phase to be accelerated by allowing users to predict the properties of their designs without needing to run through multiple iterations.

Another avenue towards expanding the scalability of hole spin qubit platforms is the development of quantum devices using industrial materials. Ge is a common material used in QD spin qubits because it forms good ohmic contacts to most metals, and boasts both a high hole mobility and low effective mass. Strain-relaxed Ge epilayers are commonly used in FinFETS [86] and MOSFETs [87, 88], and have higher thermal budgets than strained Ge quantum wells, allowing for fabrication constraints to be relaxed. Hole qubits in unstrained material are also shown to have higher manipulation rates. Furthermore, there is interest in using nominally undoped Ge for quantum devices because the lack of ionized impurities reduce the

amount of instability experienced by a quantum device at low temperature. Hole-FETs have been demonstrated on undoped Ge epilayers, showing that the high mobility and low effective mass is preserved in the undoped material. However, to date there has not been any exploration into the use of an undoped and unstrained Ge epilayer for use in quantum devices. In this thesis, we design, fabricate, and test a hole-FET and Hall bar based on a nominally undoped and unstrained Ge epilayer. We test whether the FET is capable of controlling charge at 4K by varying the voltage on a microfabricated gate electrode while holding the source-drain voltage constant. We determine that the design is capable of controlling charge by observing a change in device conductance as a function of gate voltage similar to a typical $I_d - V_{DS}$ curve. We also extract the field-effect mobility of the holes in the device. Significant background conduction was observed, and the field-effect mobility was low compared to similar devices.

We test the Hall bar structures at 5K to determine material properties, such as Hall mobility and carrier concentration. The transverse and longitudinal resistance values are obtained from this measurement. The Hall mobility is found to be similar to the field mobility, indicating a high concentration of impurities near the semiconductor-oxide surface. The wafer is found the be unintentionally doped, as the calculated carrier concentration is significantly above the insulator-to-metal transition value.

The properties of this type of Ge epilayer have never been tested before at low temperature. Demonstration of a working FET indicates a successful realization of quality ohmic contacts in this material. Furthermore, the data extracted from transport studies of the FET and Hall bar are novel. While the material quality will need to be improved if intended for further use in quantum devices, this work represents a positive first step towards exploring this material for use in quantum devices with superior performance.

This thesis supports the advancement of both theoretical and experimental research into the properties of quantum dot hole spin qubits in Ge.

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