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ECE3110J/VE311 Electronic Circuits

BJT Circuit

Microelectronic Circuit Design, Chapter 13
Fundamentals of Microelectronics, Chapter 5

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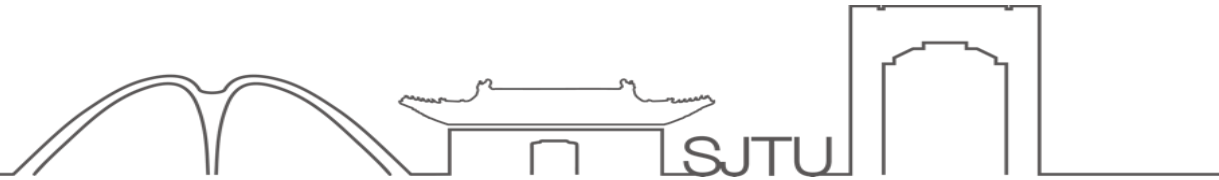
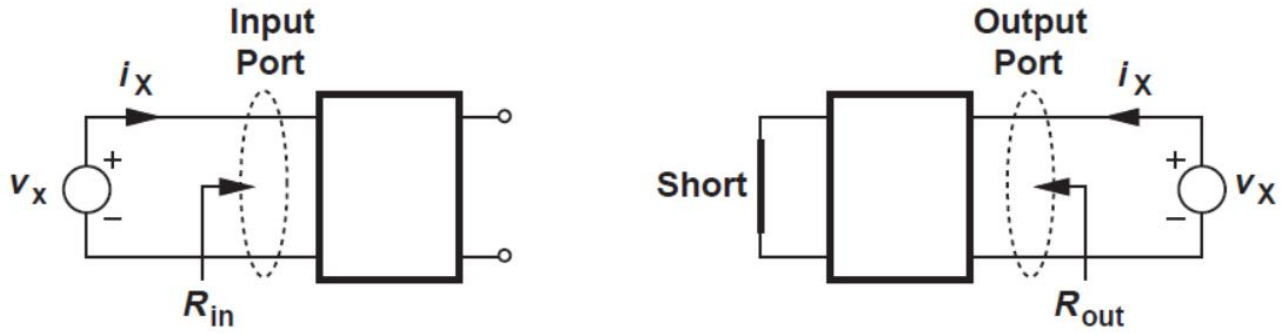


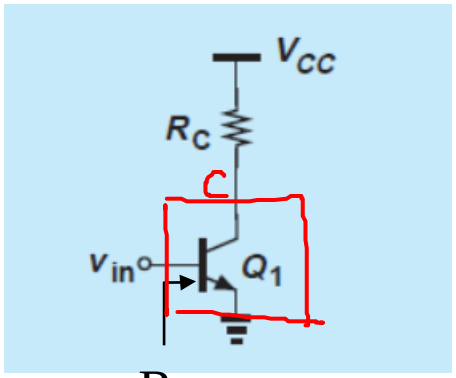
Input and Output Impedances of BJT

We have seen operation mechanisms and parameters of BJT physics. In addition to those, the **input and output (I/O) impedances** of an amplifier play a critical role in its capability to interface with preceding and following stages.

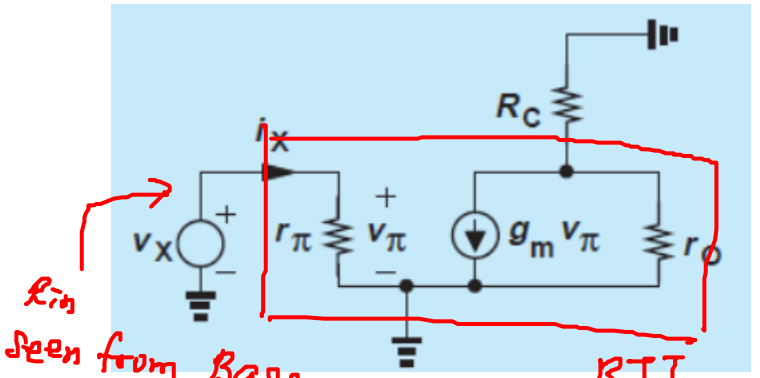


The input (output) impedance is measured between the input (output) nodes of the circuit while **all independent sources in the circuit are set to zero**. The method involves applying a voltage source to the two nodes of interest, measuring the resulting current, and defining $\mathbf{v_X/i_X}$ as the impedance.

Example 1 Assuming that the BJT operates in the forward active region, determine the input impedance seen looking into the base. Please consider the **Early effect**.



R_{in}



$R_{in} = r_\pi$.

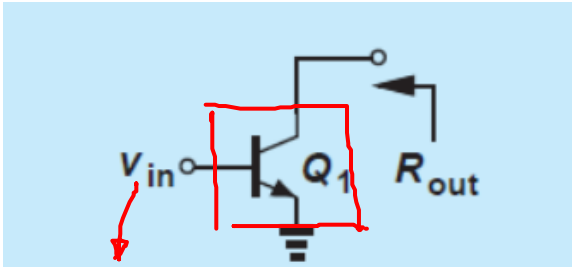
$-V_X + r_\pi i_X = 0$

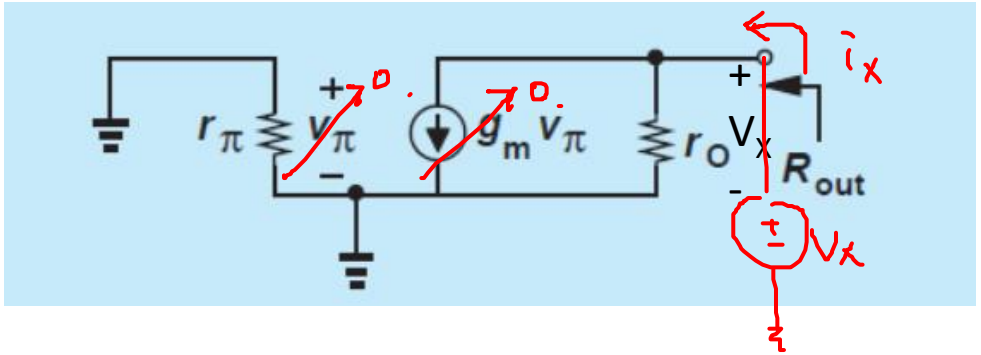
$V_X / i_X = r_\pi$.

$$by\ KVL, -v_X + i_X r_\pi = 0$$

$$\frac{v_X}{i_X} = r_\pi$$

Example 2 Assuming that the BJT operates in the forward active region, determine the impedance seen into the collector of Q_1. Please consider the **Early effect**.

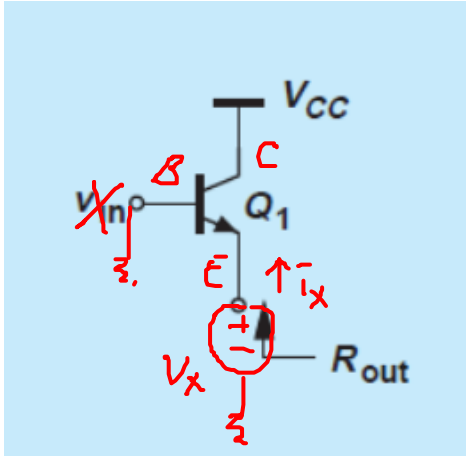


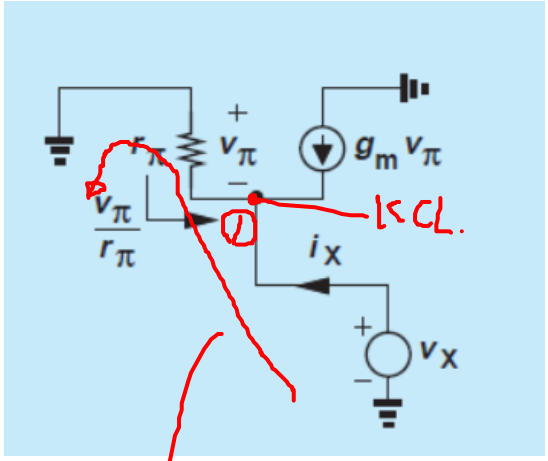


By KCL, $i_X = \frac{V_X}{r_o} + g_m v_\pi$ *where* $v_\pi = 0$

Thus, $\frac{V_X}{i_X} = r_o$

Example 3 Assuming that the BJT operates in the forward active region, determine the impedance seen at the emitter. Please **neglect the Early effect** for simplicity.





KCL.

node ① $\tilde{i}_x + \frac{v_\pi}{r_\pi} + g_m v_\pi = 0$.

$\tilde{i}_x - \frac{v_x}{r_\pi} - g_m v_x = 0$

$r_\pi = \beta / g_m$

$\left(\frac{1}{r_\pi} + g_m \right) v_x = \tilde{i}_x$

$R_{out} = \frac{v_x}{i_x} = \frac{1}{\frac{1}{r_\pi} + g_m} \simeq \frac{1}{g_m}$

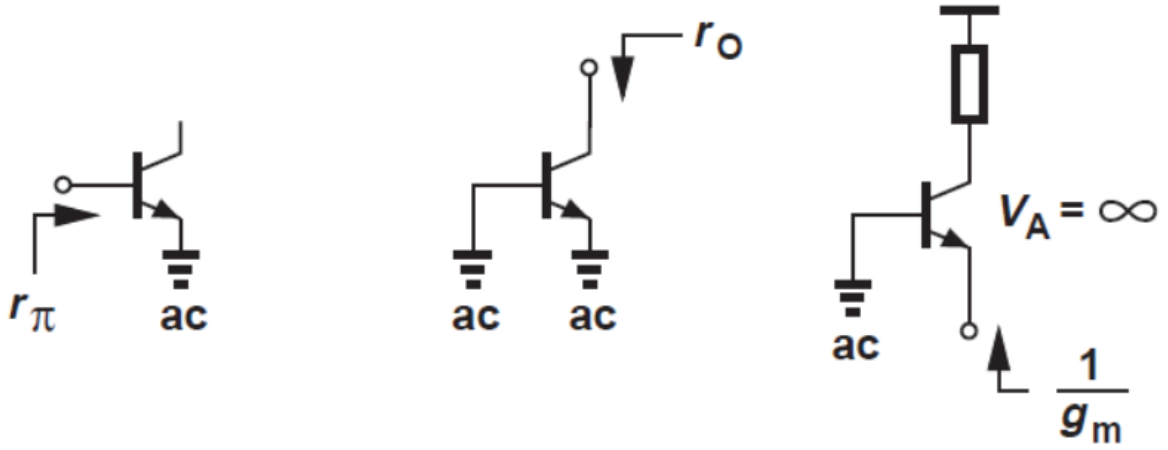
KVL: $-v_x - v_\pi = 0$

$v_\pi = -v_x$

By KCL, $-i_X = \frac{V_\pi}{r_\pi} + g_m v_\pi$

By KVL, $v_\pi = -v_X$

Thus, $\frac{V_X}{i_X} = \frac{1}{\frac{1}{r_\pi} + g_m}$



The three examples provide three important rules.

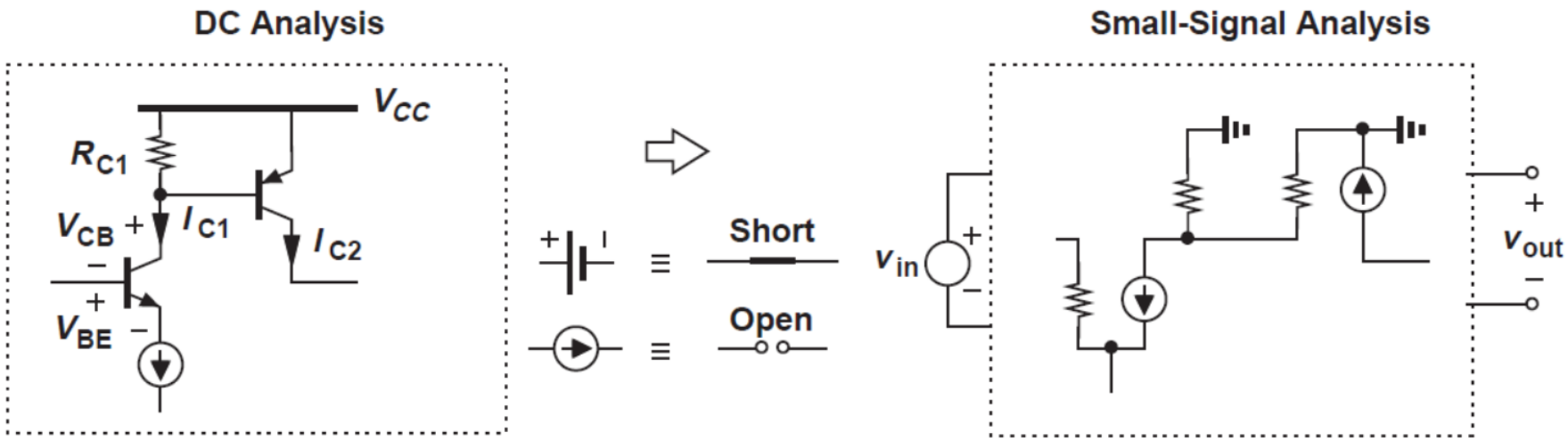
(1) Looking into **the base**, we see $\mathbf{r_\pi}$ if the emitter is (ac) grounded.

(2) Looking into **the collector**, we see $\mathbf{r_O}$ if the emitter is (ac) grounded.

(3) Looking into **the emitter**, we see $\mathbf{1/g_m}$ if the base is (ac) grounded and the Early effect is neglected.

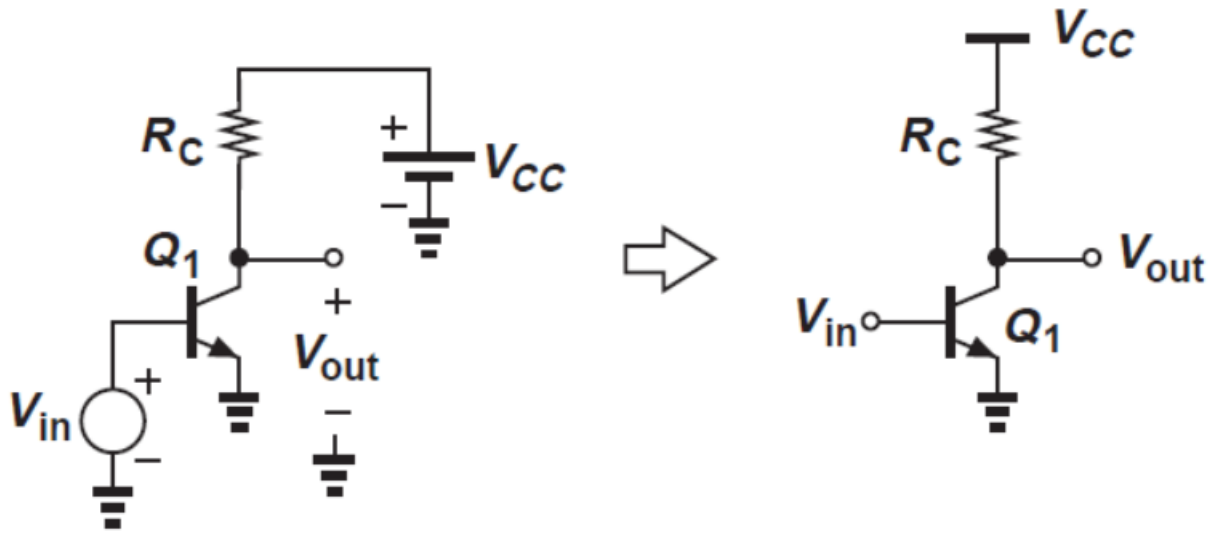
$$\frac{1}{\frac{1}{r_\pi} + g_m}$$

DC and Small-Signal Analysis



How to analyze a BJT circuit? (1) we determine the **effect of constant voltages and currents while signal sources are set to zero**; (2) we analyze the response to signal sources while **constant sources are set to zero**, i.e. ground all constant voltage sources and open all constant current sources while constructing the small-signal equivalent circuit.

***Circuit drawing**

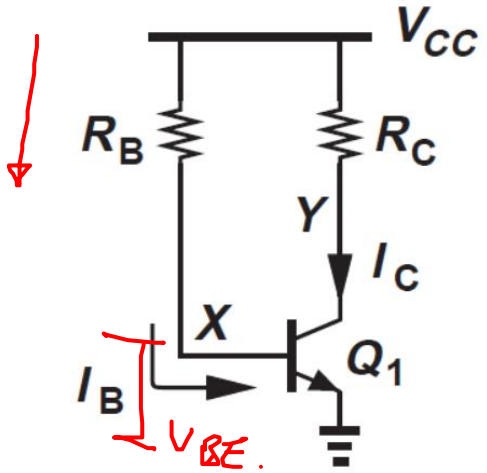


We will employ some **simplified notations** and symbols. Illustrated in Figure above is an example where the battery serving as the supply voltage is replaced with **a horizontal bar** labeled V_{CC}. Also, the input voltage source is simplified to **one node** called V_{in}, with the understanding that the other node is ground.

Operating Point Analysis and Design

Before we study BJTs' amplifier topologies, we begin with the **DC analysis and design of BJT stages**, developing skills to determine the **terminal voltages and currents** and obtain the conditions that ensure **biasing in the (forward) active mode**.

Simple biasing



By KVL, $R_B I_B + V_{BE} = V_{CC} \rightarrow I_B = \frac{V_{CC}-V_{BE}}{R_B}$

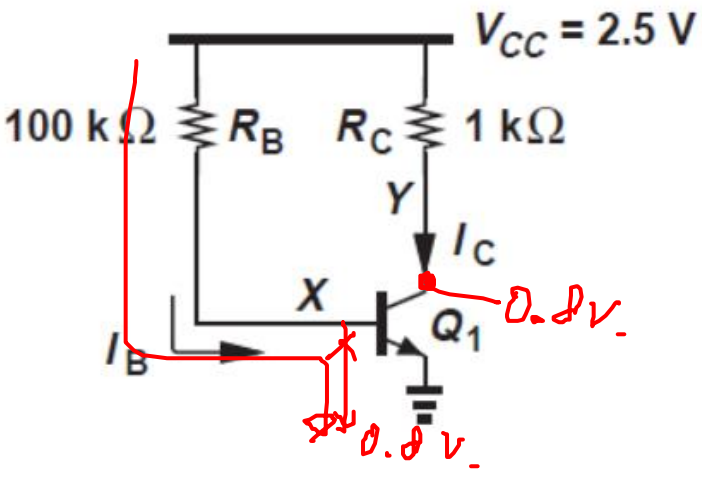
As $I_C = \beta I_B = \beta \frac{V_{CC}-V_{BE}}{R_B}$

By KVL, $V_Y = \mathbf{V_{CE}} = V_{CC} - R_C I_C = V_{CC} - \beta \frac{V_{CC}-V_{BE}}{R_B} R_C$

$V_{CE} \geq V_{BE}$.

To avoid an operation of BJT in a saturation mode, V_{CE} needs to remain above the base voltage, i.e. $\mathbf{V_{CE}} = V_{CC} - \beta \frac{V_{CC}-V_{BE}}{R_B} R_C > V_{BE}$

Example 4 For the circuit below, determine the collector bias current. Assume $V_T = 0.025$ V, $\beta = 100$ and $I_S = 10^{-17}$ A. Verify that Q_1 operates **in the forward active region**. Use $V_{BE} = 800$ mV as the trial voltage at first.



800mV

$-2.5 + R_B I_B + V_{BE} = 0$.

↓

100kΩ.

$I_B = 17\mu A$.

$I_C = \beta I_B = 1.7mA$.

$I_C = I_S\left[\exp\left(V_{BE}/V_T\right) - 1\right] = 1.7mA$.

V_{BE}'

$V_{R_C} = 1k \times 1.7mA = 1.7V$

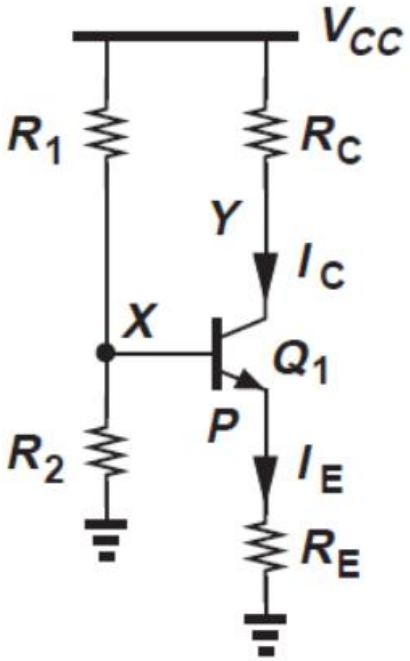
$V_{CB} = 0$.

$I_C = I_S\ \alpha\ e$, $V_T = 1.7V$. $I_B = I_C/\beta$.

$V_{BE} =$

Biasing with Emitter Degeneration

Resistor R_E appears in series with the emitter, thereby lowering the sensitivity to V_{BE}, called emitter degeneration.

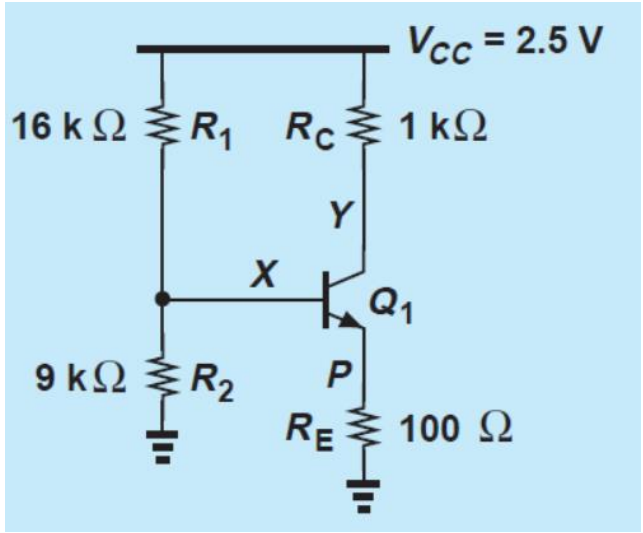


Neglecting I_B as is 1% of I_C generally,

$$V_X = \frac{R_2}{R_1 + R_2} V_{CC}, and\ V_P = V_X - V_{BE}$$

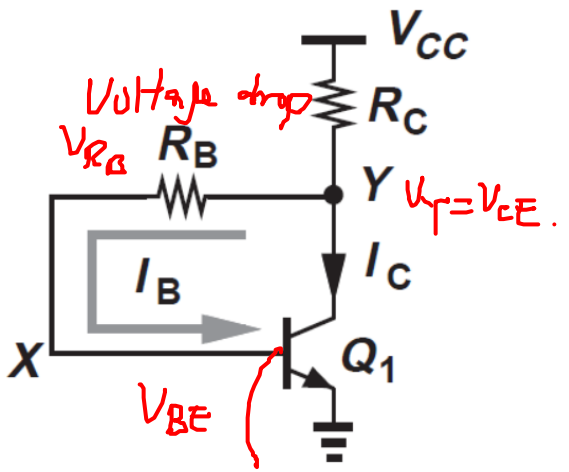
$$I_E = \frac{V_P}{R_E} = \frac{1}{R_E}\left(\frac{R_2}{R_1 + R_2} V_{CC} - V_{BE}\right) \approx I_C$$

Example 5 Calculate the bias currents in the circuit below and verify that Q_1 operates **in the forward active region**. I_B can be neglected. Assume $\beta = 100$ and $I_S = 5\times10^{-17}$ A. Use $V_{BE} = 0.8$ V as the initial guess. $V_T = 0.025$ V.



Self-Biased Stage

Another biasing scheme commonly used in discrete and integrated circuits is a **self-biased stage**, because I_B and V_B are provided from the collector, this stage exhibits many interesting and useful attributes.



$$V_Y = V_{CC} - R_C I_C$$

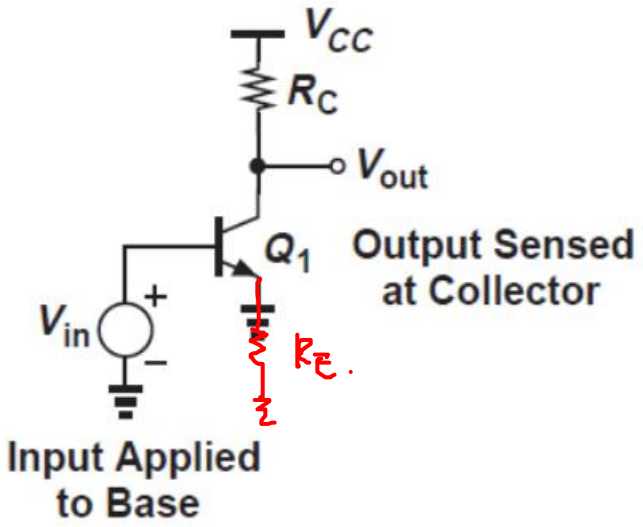
$$V_Y = R_B I_B + V_{BE} = \frac{R_B I_C}{\beta} + V_{BE}$$

$$\rightarrow V_{CC} - R_C I_C = \frac{R_B I_C}{\beta} + V_{BE}$$

$$\boldsymbol{I_C = \frac{V_{CC} - V_{BE}}{R_C + R_B/\beta}}$$

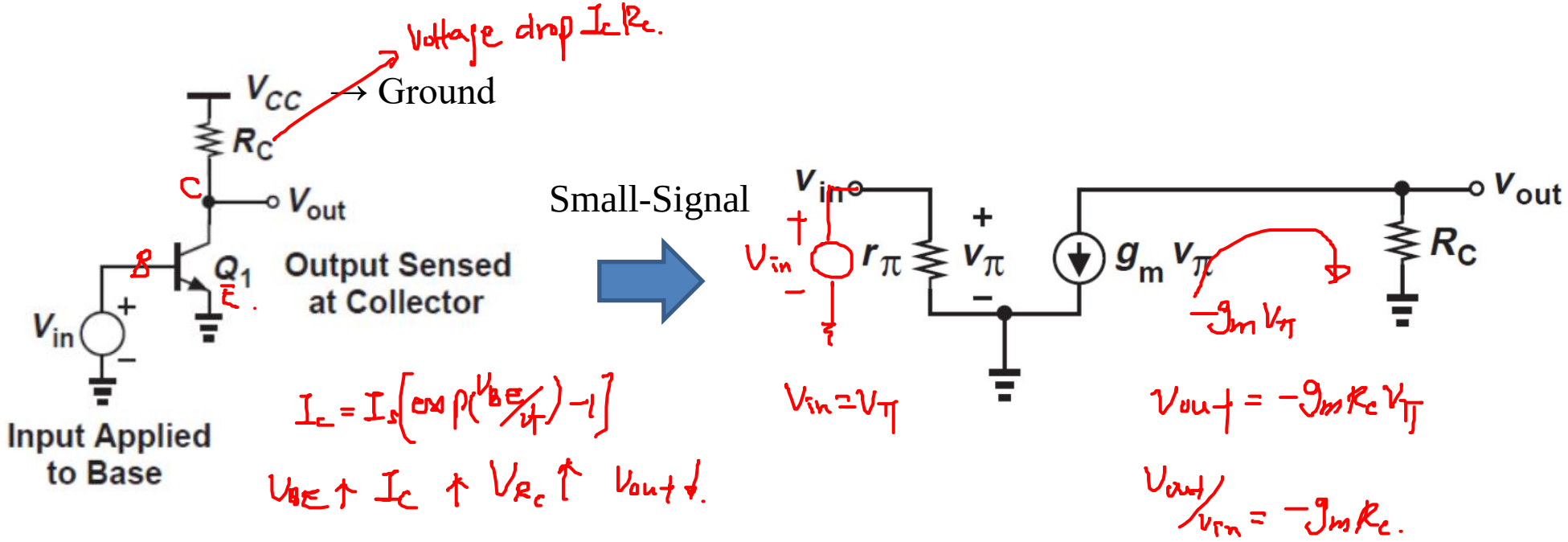
V_B is always lower than V_C as $V_X = V_Y - I_B R_B$. The self-biasing guarantees that **Q_1 operates in the active mode** regardless of device and circuit parameters.

Common-Emitter (C-E) Amplifier



If the input signal is applied to base (B) and the output signal is sensed at the collector (C), the circuit is called a **common-emitter (C-E) stage, i.e. emitter (E) is grounded and appears in common to the input and output.**

Without Early Effect



***Recall: Ground all constant voltage sources and open all constant current sources for small signal model.**

By KCL: $-g_m v_\pi = {}^{v_{out}}/_{R_C}$ where $v_{in} = v_\pi$

Thus, $-g_m v_{in} = {}^{v_{out}}/_{R_C}$

$$ {}^{v_{out}}/_{v_{in}} = \boldsymbol{A_v = -g_m R_C} $$

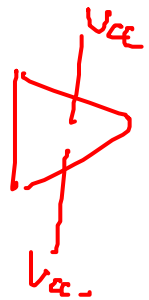
Interesting and important properties of the CE stage:

(1) The small-signal gain is negative, i.e. $V_{BE}\uparrow$ and $I_C\uparrow$ lower V_{out}.

(2) A_v is proportional to g_m and the collector resistor R_C.

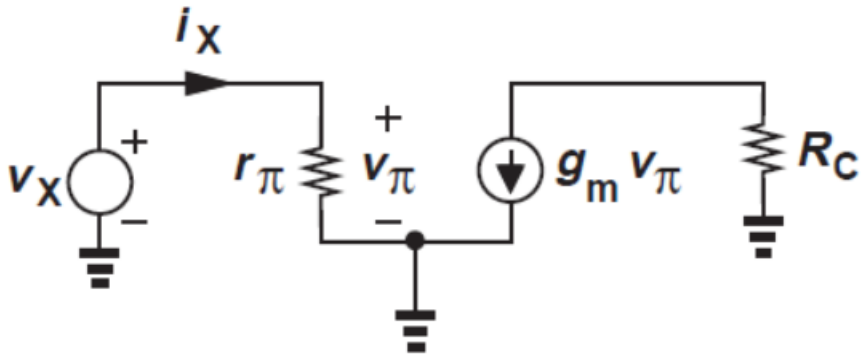
(3) The voltage gain of the stage is limited by the supply voltage.

$\mathbf{|A_v| = g_m R_C \rightarrow \frac{I_C R_C}{V_T}}$ ($\mathbf{g_m = {I_C}/{V_T}}$) and $I_C R_C$ indicates the voltage drops at the collector resistor R_C. Because $I_C R_C < V_{CC}$, $\mathbf{|A_v| < \frac{V_{CC}}{V_T}}$. Finally, as the BJT is in the active region, we can say that , $\mathbf{|A_v| < \frac{V_{CC} - V_{BE}}{V_T}}$



Input and Output Impedances of CE stage

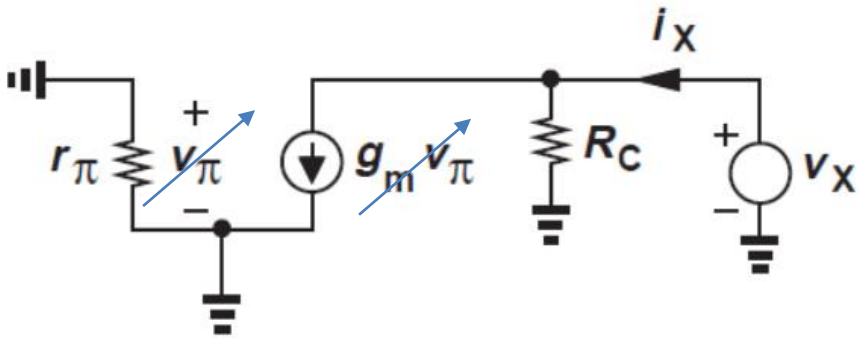
$\mathbf{R_{In}}$



By KVL: $-v_X + i_X r_\pi = 0$

$$\rightarrow {}^{v_X}/_{i_X} = \boldsymbol{r_\pi} = \frac{\boldsymbol{\beta}}{\boldsymbol{g_m}} = \frac{\boldsymbol{\beta V_T}}{\boldsymbol{I_C}}$$

$\mathbf{R_{Out}}$



$${}^{v_X}/_{i_X} = \boldsymbol{R_C}$$

Example 7 Design a CE core with V_{CC} = 1.8 V, V_{BE} = 800 mV, and a power budget P ($I_C \cdot V_{CC}$) of 1 mW while achieving maximum voltage gain. Use V_T = 0.026.

$P = 1mW = I_c \times V_{cc}$.

$I_c = \frac{1mW}{1.8V} \approx 0.556mA$

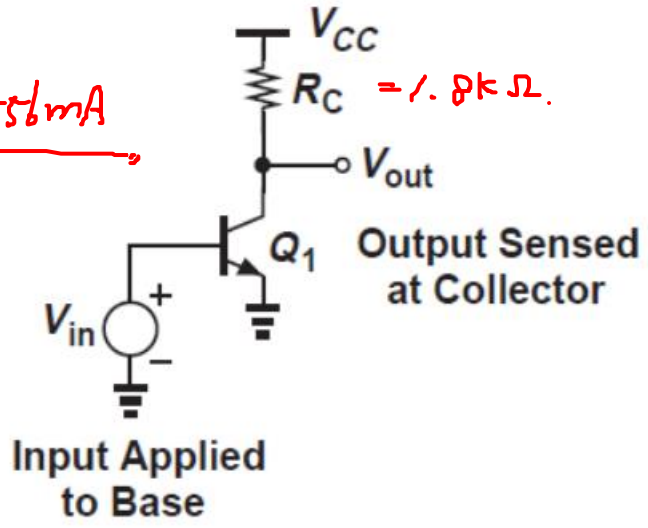
$V_{CE} \geq V_{BE}$.

$V_{CC} - R_C I_C = V_{CE} \geq 800mV$.

$1.8 - R_c \times 0.556mA \geq 0.8V$.

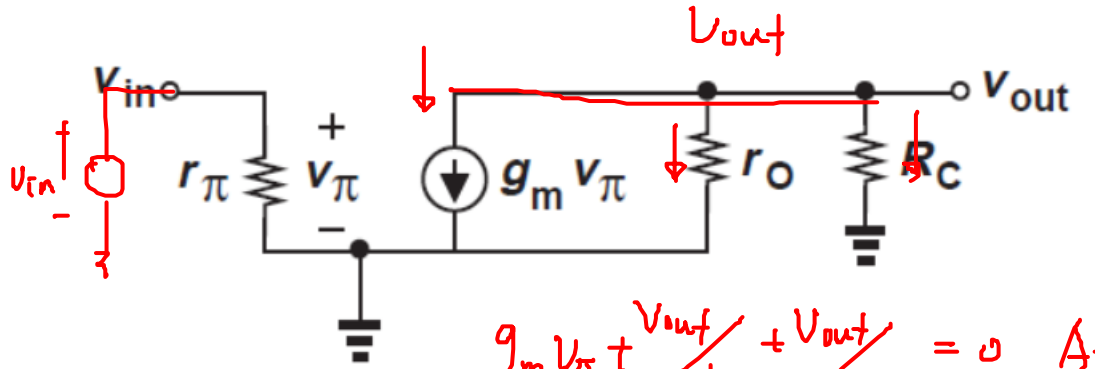
$R_c \leq 1.8K\Omega$.

$A_V = -g_m R_c$.



With Early Effect

$A_v = -g_m R_C$ suggests that **the voltage gain of the CE stage can be increased indefinitely if $R_C \to \infty$** while g_m remains constant. This trend appears valid if V_{CC} is also raised to ensure the BJT remains in the active mode. However, in reality, **the Early effect limits the voltage gain** even if R_C approaches infinity.



$g_m v_\pi + \frac{v_{out}}{r_o} + \frac{v_{out}}{R_C} = 0$ $A_V = \frac{v_{out}}{v_{in}} = \frac{g_m}{\frac{1}{R_C} + \frac{1}{r_o}}$

$v_\pi = v_{in}$

∞.

As r_O appears in parallel with R_C, $^{v_{in}}/_{v_{out}} = A_v = -g_m(R_C \| r_O)$ $-g_m(R_C \| r_O)$

Similarly, $\mathbf{R_{out}}$ is $R_C \| r_O$

$\Rightarrow -g_m r_o$.

$\mathbf{R_{in}}$ remains the same as r_π

If $R_C \rightarrow \infty$ then **the gain $A_v = -g_m r_O$**. This emphasizes that no external device loads in the circuit, and **$g_m r_O$ represents the maximum voltage gain** provided by a single BJT, which is called as the **intrinsic gain**.

By substituting g_m with I_C/V_T and $r_O = V_A/I_C$, $|\boldsymbol{A_v}| = \frac{\boldsymbol{V_A}}{\boldsymbol{V_T}}$

Example 8 The circuit below is biased with I_C of 1 mA, V_T = 0.025 V and R_C = 1 kΩ. If $\beta = 100$ and V_A = 10 V, determine the small-signal voltage gain and I/O impedances.

Include Early effect

$A_V = -g_m(R_C \| r_o)$

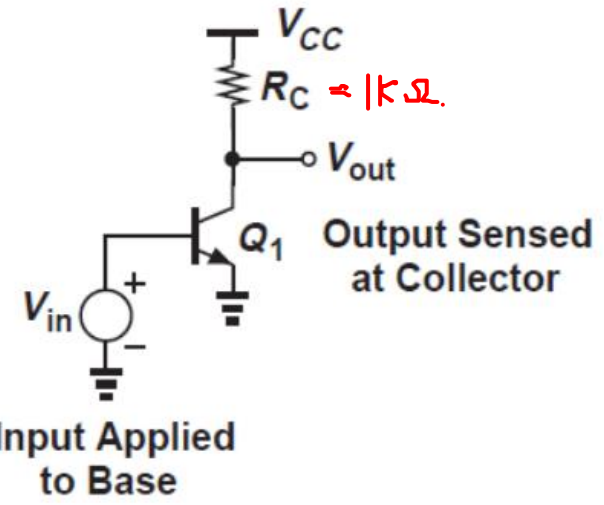
$R_{out} = R_C \| r_o$

$R_{in} = r_\pi$

$g_m = I_C/V_T = 1/25$

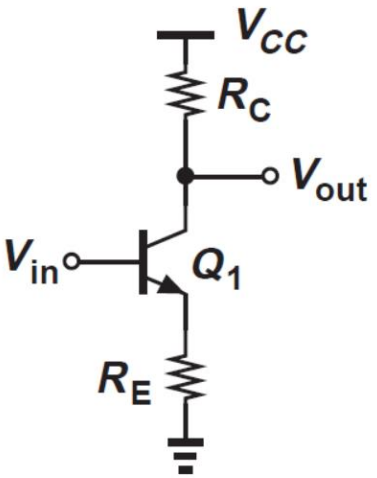
$r_o = V_A/I_C = 10K$

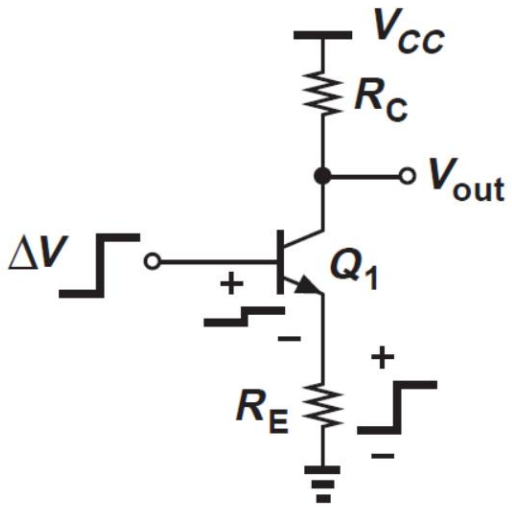
$r_\pi = \beta/g_m = 100/(1/25)$



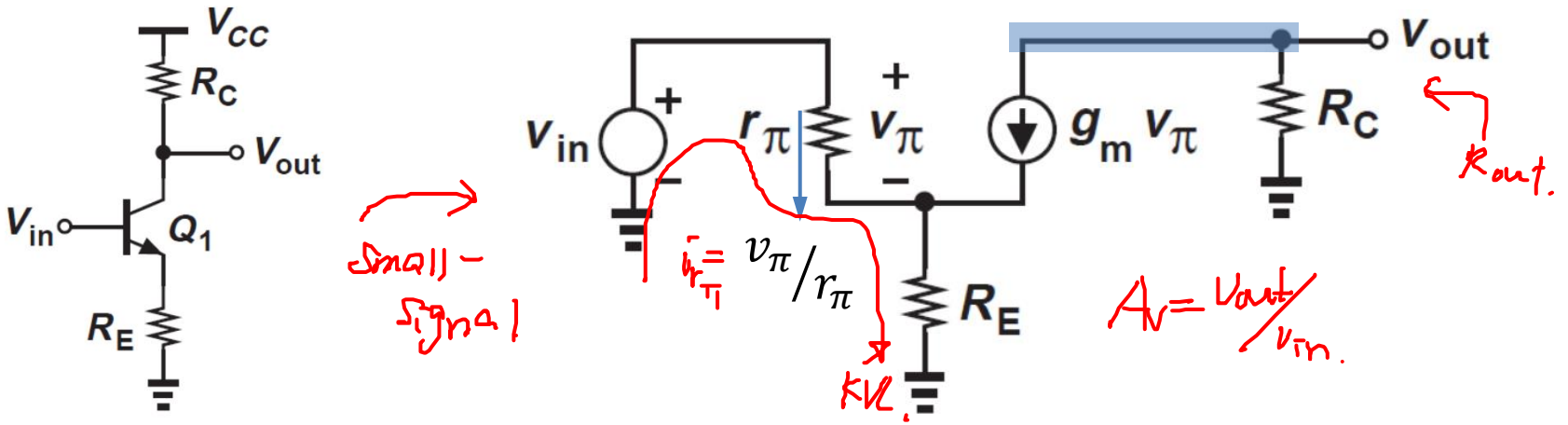
CE Stage With Emitter Degeneration (Without Early Effect)

Emitter degeneration has a resistor **R_E which appears in series with the emitter**. This technique **improves the linearity of the circuit.**





When the input signal raises the base voltage by ΔV
If $R_E = 0$, then V_{BE} would also increase by ΔV, producing a I_C change of $g_m\Delta V$.
With $R_E \neq 0$, some fraction of ΔV appears across R_E, thus leaving a voltage change across the BE junction that is less than ΔV. Consequently, the I_C change is also less than $g_m\Delta V$.



from blue node.

By KCL, $-g_m v_\pi = {}^{v_{out}}/_{R_C} \rightarrow v_\pi = -{}^{v_{out}}/_{g_m R_C}$

CE stage

$A_V = -g_m R_C$.

Current through $R_E = {}^{v_\pi}/_{r_\pi} + g_m v_\pi$

By KVL: $-v_{in} + v_\pi + v_{R_E} = 0$ *where* $v_{R_E} = ({}^{v_\pi}/_{r_\pi} + g_m v_\pi) R_E$

Thus, $v_{in} = v_\pi + ({}^{v_\pi}/_{r_\pi} + g_m v_\pi) R_E = v_\pi \left[1 + ({}^{1}/_{r_\pi} + g_m) R_E\right]$

$$\frac{v_{out}}{v_{in}} = -\frac{g_m R_C}{1 + \left({}^{1}/_{r_\pi} + g_m\right) R_E}$$

R_{out}

$$\frac{v_{out}}{v_{in}} = -\frac{g_m R_C}{1 + \left(\cancel{1/r_\pi} + g_m\right) R_E}$$

g_m $r_\pi = \beta/g_m$

$1/r_\pi = g_m/\beta > 100$

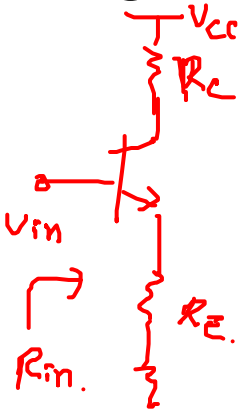
The magnitude of the voltage gain is lower than $g_m R_C$ for $R_E \neq 0$

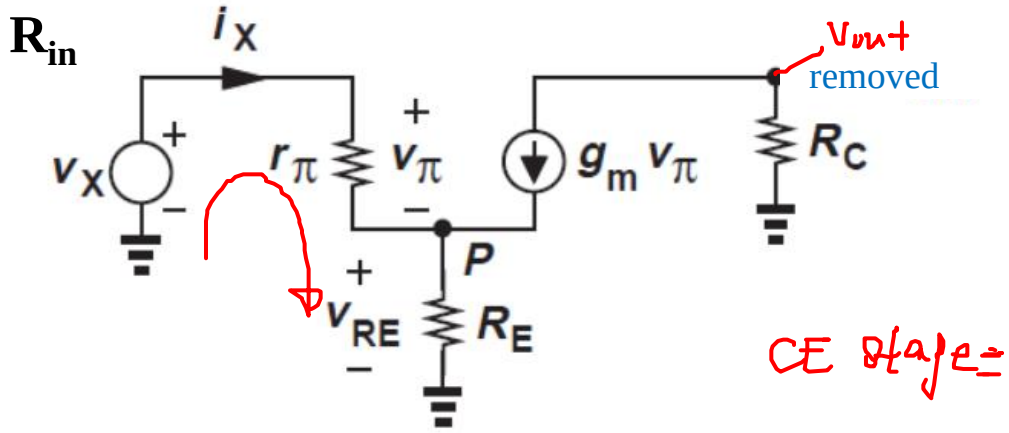
With $\beta \gg 1$ (generally 100), $g_m \gg 1/r_\pi = g_m/\beta$ $\left(r_\pi = \beta/g_m\right)$

$$\boldsymbol{A_v = -\frac{g_m R_C}{1+g_m R_E}} \rightarrow \textbf{The gain falls by the factor of } \mathbf{1+g_m R_E}$$

The voltage gain of the degenerated stage is lower than that of the CE core with no degeneration. **The reduction in gain is incurred to improve other aspects of the performance**.

CE Stage With Emitter Degeneration-Input and Output Impedance





CE stage = r_π

$v_\pi = r_\pi i_x$

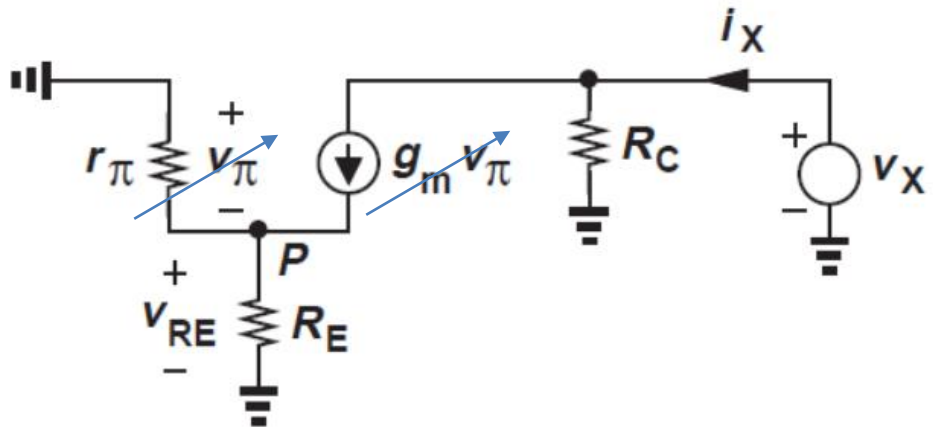
Current through R_E is $i_x + g_m v_\pi = i_x + g_m r_\pi i_x = (\mathbf{1} + \boldsymbol{\beta}) \boldsymbol{i_X}$ as $r_\pi = {}^{\beta}/_{g_m}$

KVL $v_x = r_\pi i_x + R_E(1 + \beta) i_X$ and thus $\boldsymbol{R_{in}} = {}^{v_x}/_{i_x} = \boldsymbol{r_\pi} + (\boldsymbol{\beta} + \mathbf{1}) \boldsymbol{R_E}$

$v_x / i_x = R_{in}$

Emitter degeneration **increases the input impedance**—Any impedance tied between the emitter and ground is **multiplied by β+1** when 'seen from the base'.

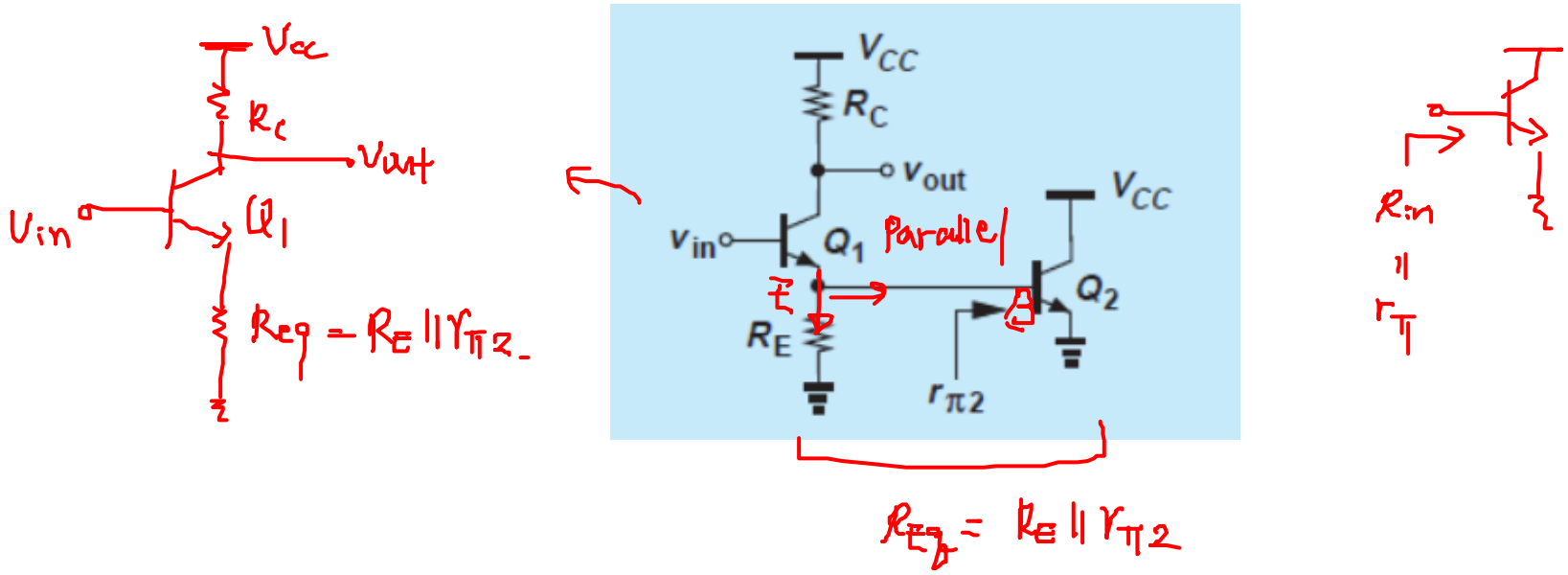
R_{out}



$v_\pi = 0$, all i_X flows through R_C and thus $R_{out} = R_C$

The emitter degeneration **does not alter R_{out}** if the Early effect is neglected.

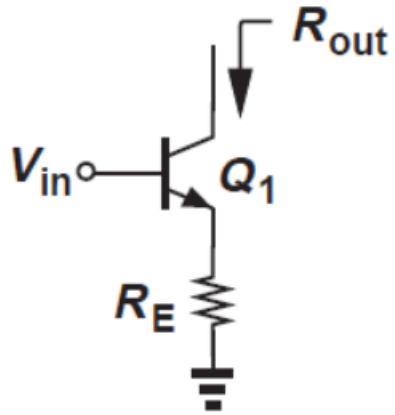
Example 9 Determine the voltage gain of the stage shown below. No Early effect.



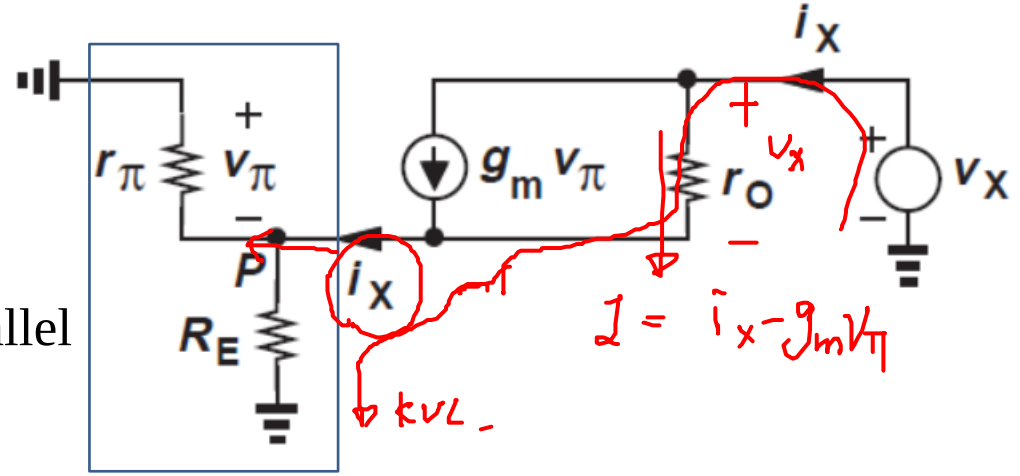
Voltage gain of CE stage with emitter degeneration

$$A_v = -\frac{g_m R_C}{1 + g_m R_E} = -\frac{R_C}{1/g_m + R_E}$$

Effect of Transistor Output Resistance with Early Effect



Parallel



$v_\pi = -i_x(R_E \| r_\pi)$

$i_x = g_m v_\pi + {}^{v_x}/_{r_O}$ or a current through r_O is $i_X - g_m v_\pi$

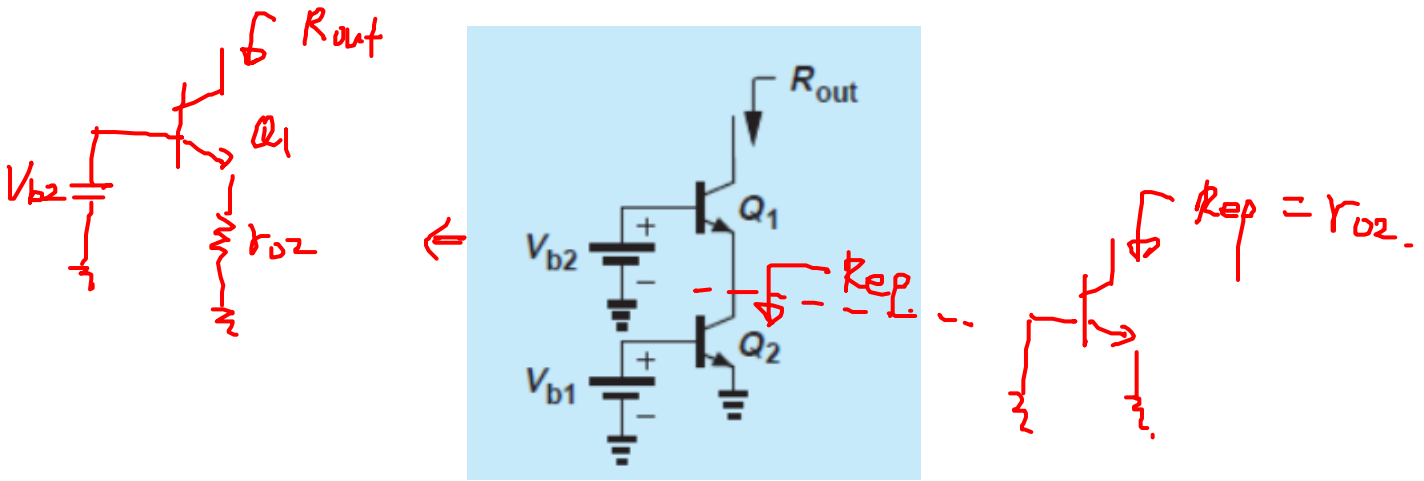
By KVL: $-v_X + r_O(i_X - g_m v_\pi) - v_\pi = 0 \rightarrow \boldsymbol{v_X = r_O[i_X + g_m i_x(R_E \| r_\pi)] + i_x(R_E \| r_\pi)}$

$\boldsymbol{R_{out}} = {}^{v_X}/_{i_X} = r_O[1 + g_m(R_E \| r_\pi)] + (R_E \| r_\pi) \rightarrow \boldsymbol{r_O + (g_m r_O + 1)(R_E \| r_\pi)}$

$\boldsymbol{R_{out} \approx r_O[1 + g_m(R_E \| r_\pi)]}$ **as** $\boldsymbol{g_m r_O \gg 1}$ $\boldsymbol{(intrinsic\ gain)}$

Increase in the output impedance r_O produces amplifiers with a higher gain.

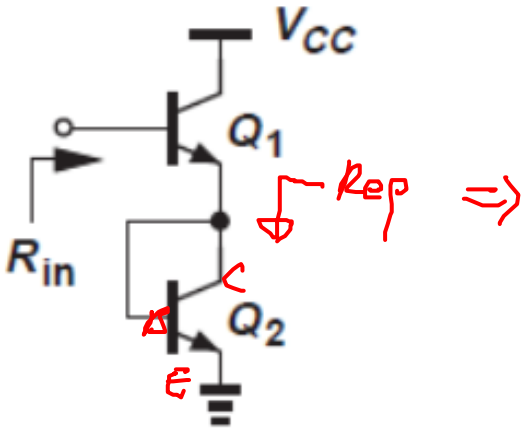
Example 10 Determine the **output resistance** of the circuit below. With Early Effect.



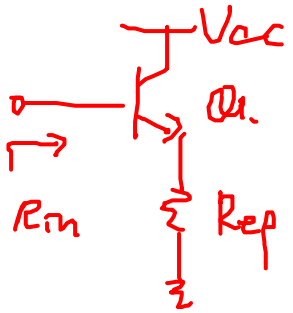
Single stage $R_{out} \approx r_O[1 + g_m(R_E \| r_\pi)]$

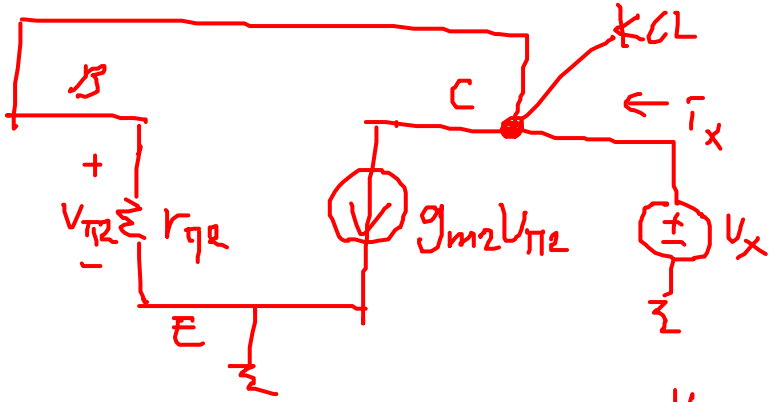
Thus, $R_{out} \approx r_{O1}[1 + g_{m1}(r_{o2} \| r_{\pi 1})]$

Example 11 Determine the **input** of the circuit below. **There is no Early Effect.**



$\Rightarrow$





$$i_x = g_{m2}V_{\pi 2} + V_{\pi 2}/r_{\pi 2} \Rightarrow i_x = \left(g_{m2} + 1/r_{\pi 2}\right)V_x$$

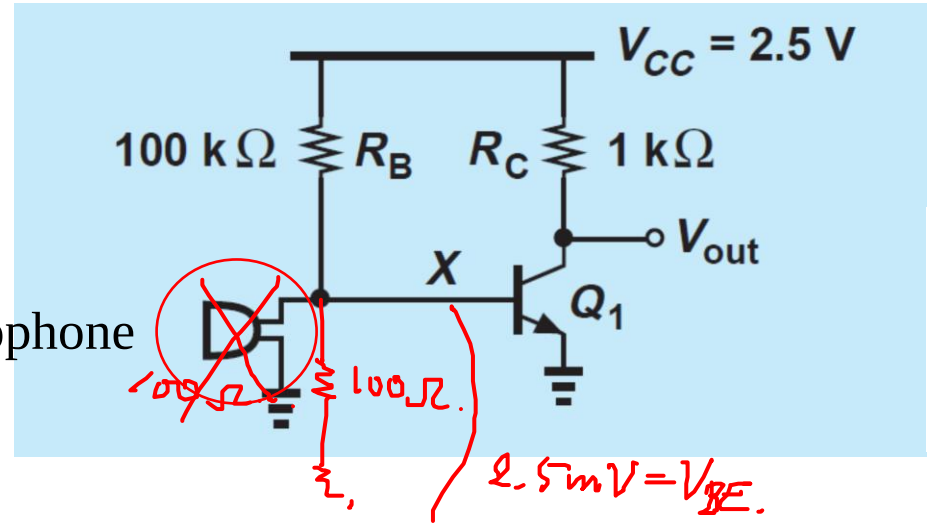
$$V_x = V_{\pi 2}$$

$$R_{ep} = V_x/i_x = \frac{1}{1/r_{\pi 2} + g_{m2}} = r_{\pi 2} \,||\, 1/g_{m2}$$

$$R_{in} = r_\pi + (1+\beta)(r_{\pi 2} \,||\, 1/g_{m2})$$

Coupling capacitor

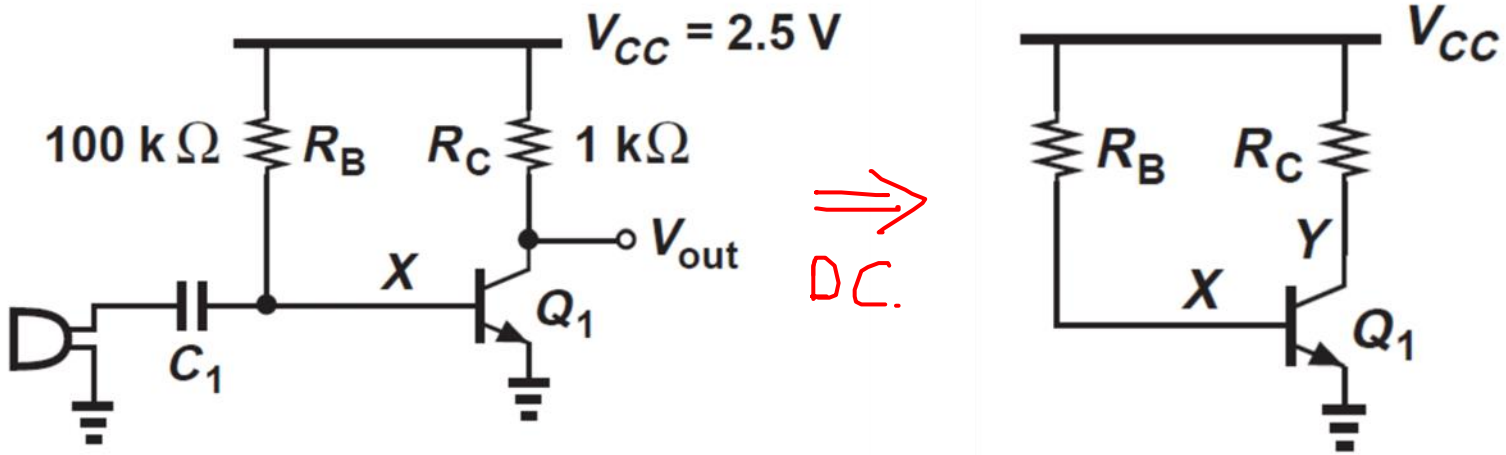
A student constructed the circuit shown below to **amplify the signal** produced by a microphone with a small low-frequency resistance of 100 Ω. Unfortunately, Q_1 carries no current, failing to amplify.



$$V_X = \frac{100\ \Omega}{100\ \text{k}\Omega + 100\ \Omega} \times 2.5\ \text{V}$$

$$\approx 2.5\ \text{mV}.$$

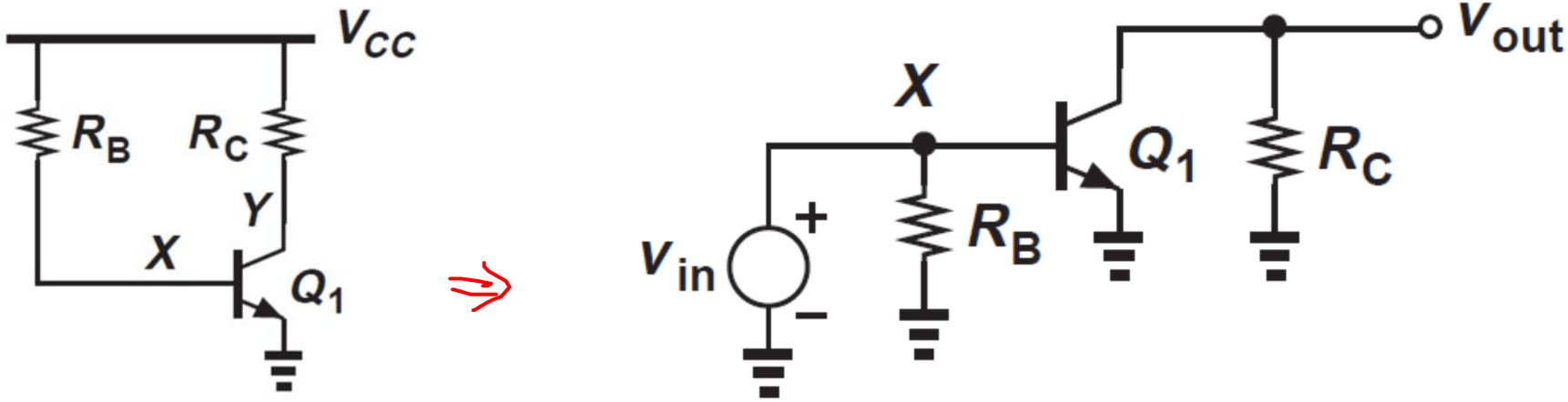
Too small bias



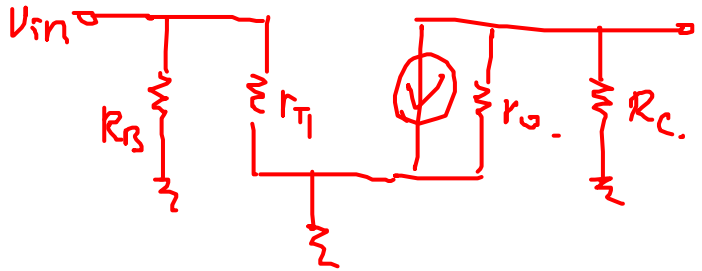
With DC bias, no interference of microphone to bias point of Q_1

Since only the signal generated by the microphone is of interest, **a series capacitor** can be inserted so as to **isolate the dc biasing of the amplifier from the microphone**.

The bias point of Q_1 remains independent of the resistance of the microphone because **C_1 carries no bias current (DC Open)**. The value of C_1 is chosen so that it provides a relatively low impedance for the frequencies of interest **(AC Short)**. C_1 is a **coupling capacitor** and the input of this stage is **ac-coupled** or **capacitively coupled**.



Simplified stage under DC bias **Simplified stage under small-signal**

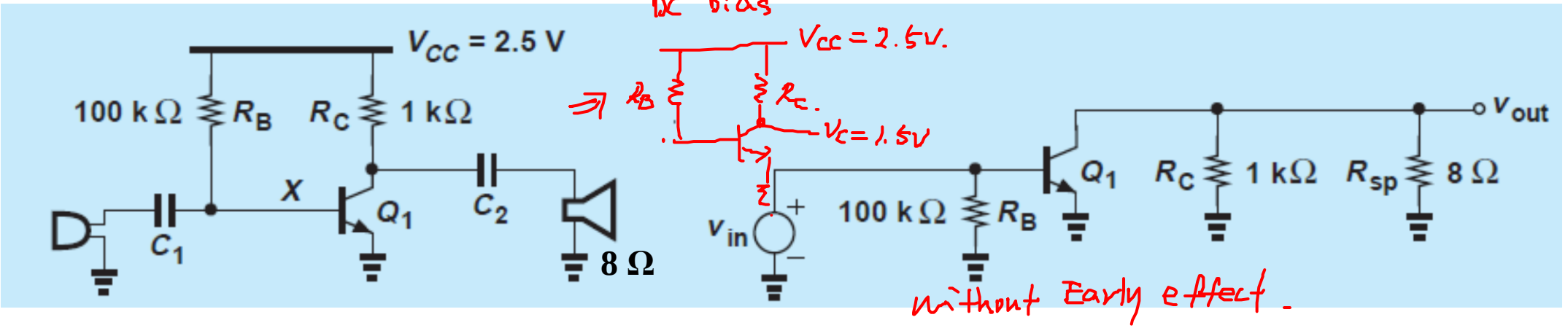


By the small-signal analysis, we get

$$\frac{v_{out}}{v_{in}} = -g_m(R_C \| r_o)$$

$R_{in2} = r_\pi \| R_B$ Bias resistor R_B negligibly impacts the performance of the stage

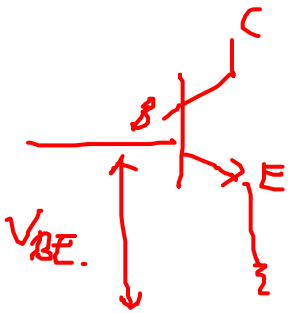
$R_{out} = R_C \| r_o$, or we can say simply R_C



The student now improved the circuit as above and applied ac coupling to the output as well. The collector bias voltage is 1.5 V and Q_1 in the active region. However, the student still observes no gain in the circuit. $I_S = 5 \times 10^{-17}$ A and $V_A = \infty$.

$V_T = 0.026$ V

What is V_{BE}, I_B, β, and A_v of the transistor?



$I_C = \frac{2.5-1.5}{1K} = 1mA = I_S\left[\exp\left(V_{BE}/V_T\right)-1\right]$, $V_T = 0.026V$.

$\Rightarrow V_{BE} = 0.796$ V.

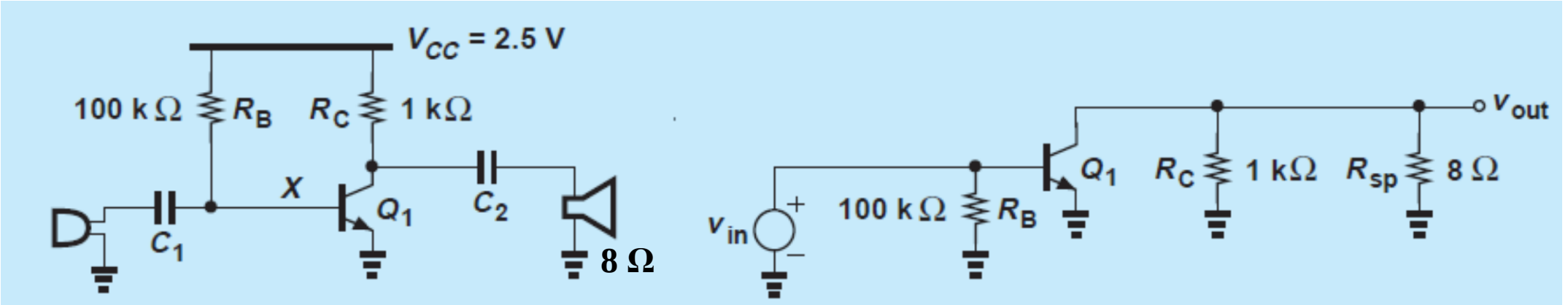
$2.5 - R_B I_B = V_{BE} \Rightarrow I_B = 17\mu A$.

$\beta = I_C/I_B = 59$

$A_v = |g_m (R_C \| R_{sp})|$ $\quad 1K \| 8$

$g_m = I_C/V_T = 0.038\cdots$

$= 0.038\cdots \times 8 = 0.30$



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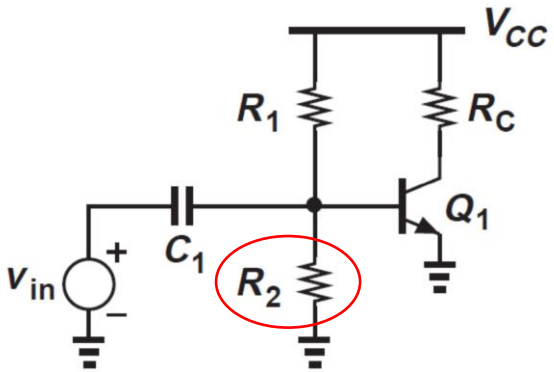
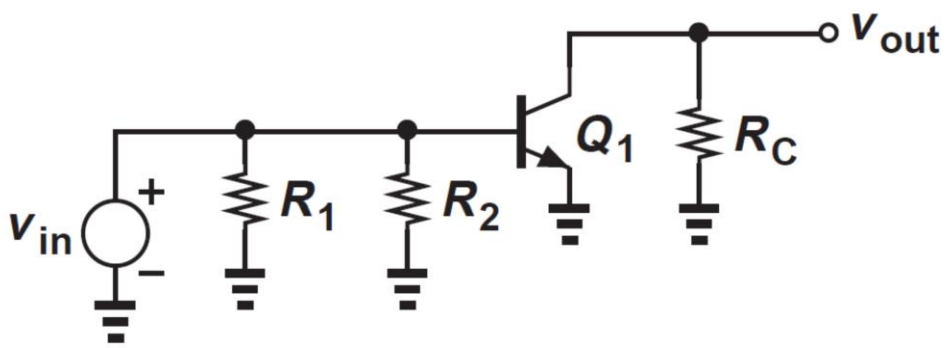
$V_T = 0.026$ V

What is V_{BE}, I_B, β, and A_v of the transistor?

Improper interface between an amplifier and a load

Further improvement..

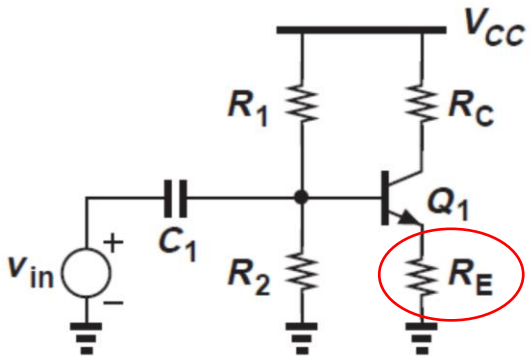


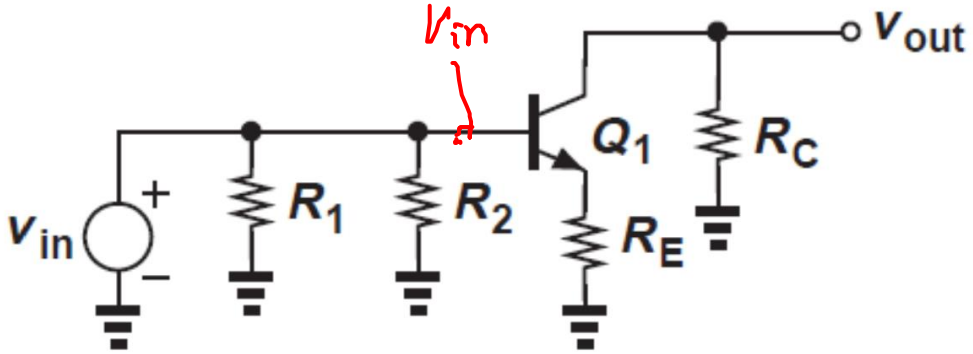


$$\frac{v_{out}}{v_{in}} = -g_m(R_C \| r_o)$$

$$R_{in} = r_\pi \| R_1 \| R_2$$

$$R_{out} = R_C \| r_o$$



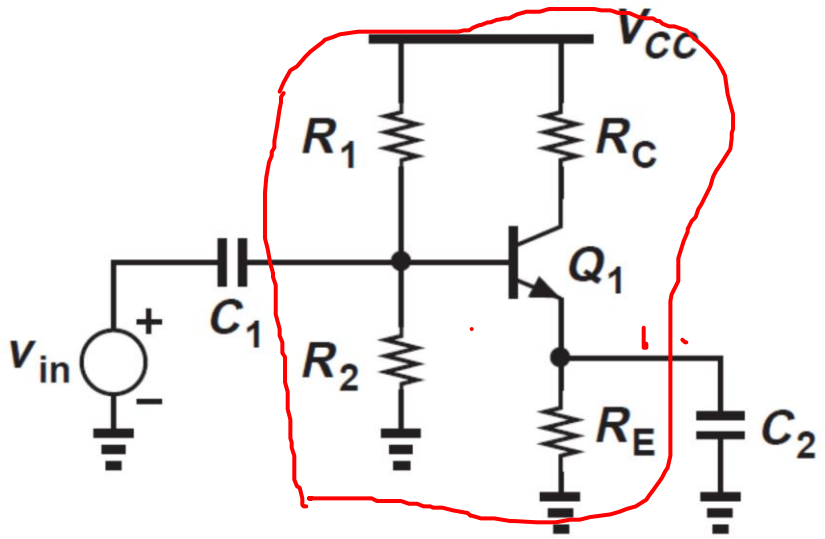


$$\frac{v_{out}}{v_{in}} = \frac{-R_C}{\frac{1}{g_m} + R_E}$$

$$R_{in} = [r_\pi + (\beta + 1)R_E] \| R_1 \| R_2$$

$$R_{out} = R_C$$

The use of emitter degeneration can effectively stabilize the bias point. However, degeneration also lowers the gain. **Is it possible to apply degeneration to biasing (DC) but not to the signal (AC)**?



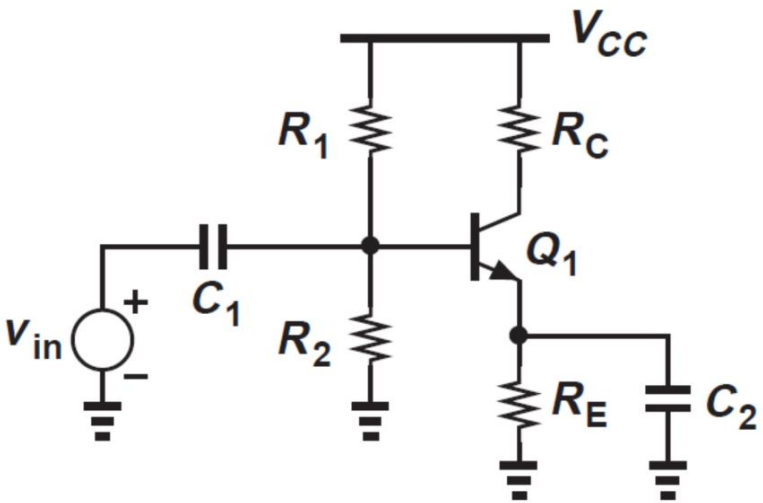
Above shows a general topology for the CE stage where C_2 is large enough to act as a short circuit for signal frequencies of interest.

$$\frac{v_{out}}{v_{in}} = -g_m R_C$$

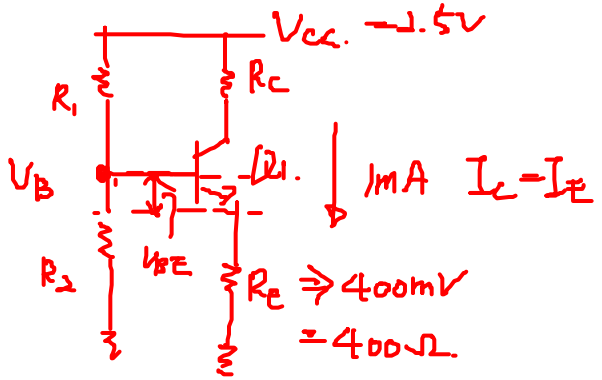
$$R_{in} = r_\pi \| R_1 \| R_2$$

$$R_{out} = R_C$$

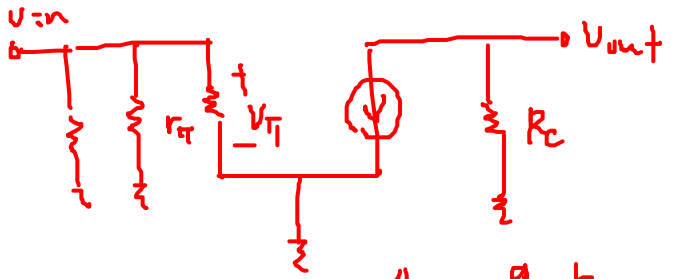
Example 12 Design the stage below to satisfy the following conditions: I_C = 1 mA, voltage drop across R_E = 400 mV, voltage gain = 20 in the audio frequency range 20 Hz to 20 kHz, input impedance > 2 k. Assume β = 100, $I_S = 5 \times 10^{-16}$, and V_{CC} = 2.5 V. Assume the npn BJT is ideal, and C_1 and C_2 work properly as coupling capacitors.



DC analysis



AC small-signal small



$A_v = -g_m R_C$

$g_m = I_C / V_T = \frac{1mA}{0.026} = 0.038$

$R_C = \frac{20}{0.038} = 526.32\ \Omega.$

$I_C = 1mA = I_S\left[\exp\left(V_{BE}/V_T\right) - 1\right] \Rightarrow V_{BE} = 0.736$

$V_T = 0.026$

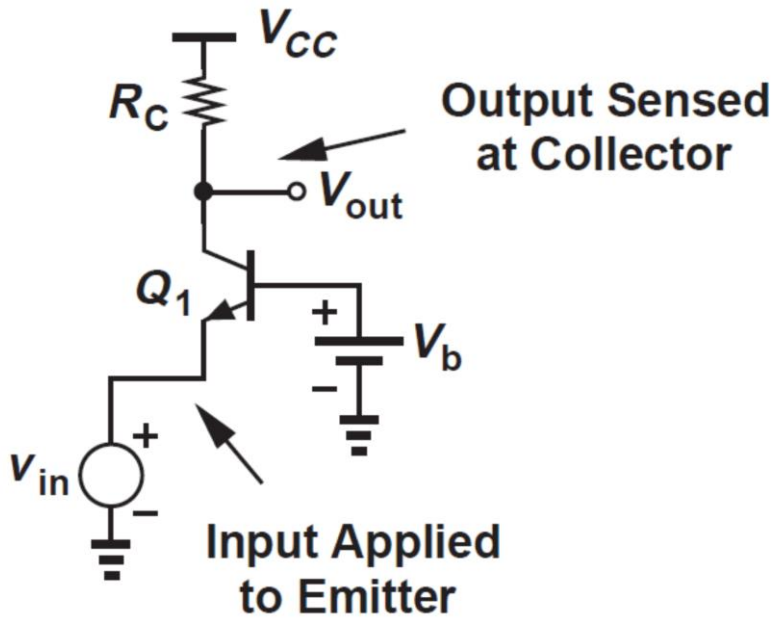
$V_B = V_{BE} + V_E = 1.136\ V$ by voltage division $V_{CC} \times \frac{R_2}{R_1 + R_2} = 1.14\ V \Rightarrow 1.136R_2 - 1.14R_1 = 0.$

$R_{in} = r_\pi \| R_1 \| R_2 > 2K.$ $I_B = I_C/\beta = 1mA/100 = 10\ \mu A.$

$R_1 = 27K$

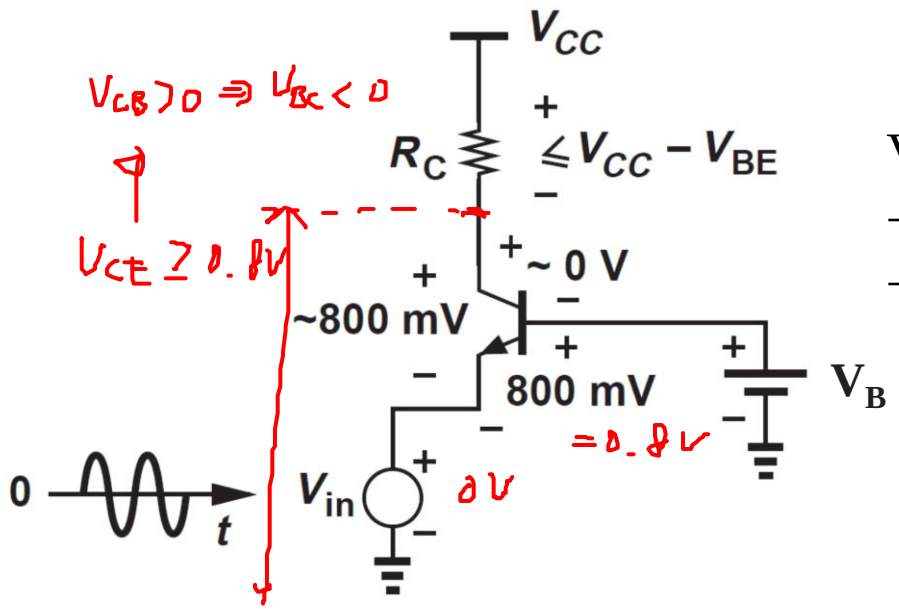
$R_2 = 23K$

Common-Base (CB) Topology



The input is applied to the emitter and the output is sensed at the collector. Biased at a proper voltage, **the base acts as ac ground** and hence as a node "common" to the input and output ports.

Circuit's Headroom Limitations



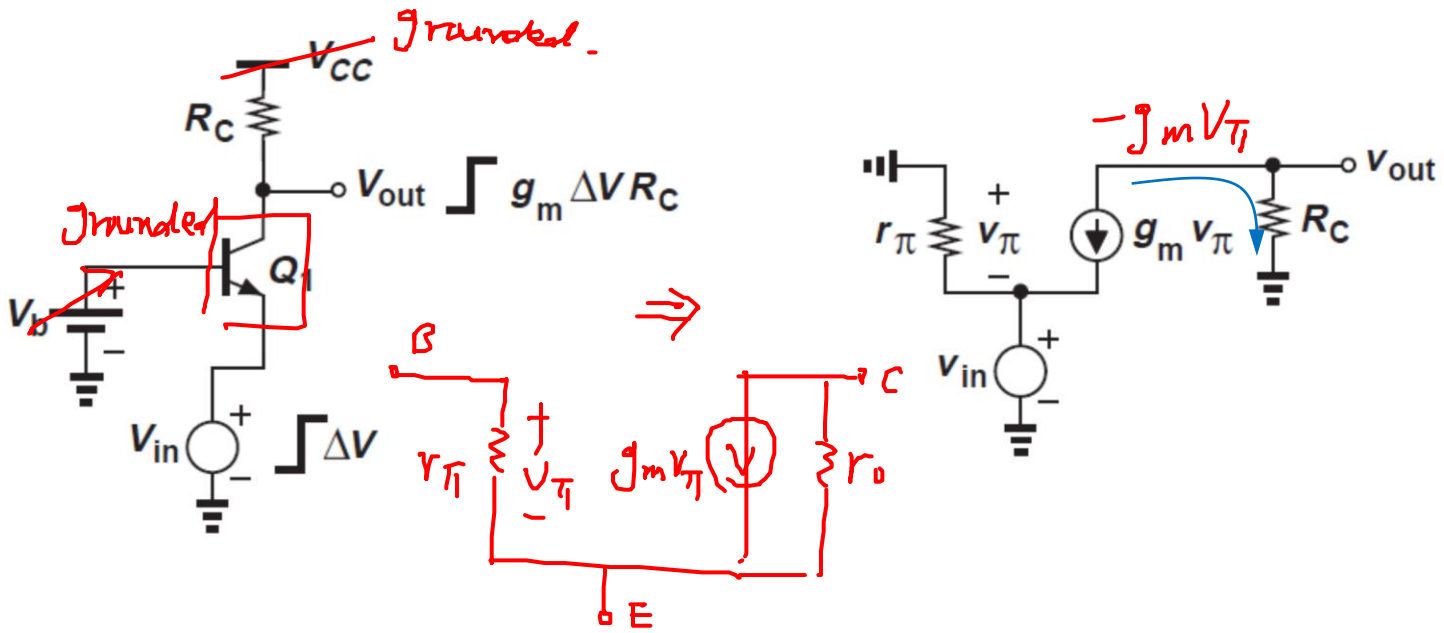
$V_{CC} - V_{R\_C} \geq V_{CE}$ (= V_{CB} (e.g. 0 V) + V_{BE})

$\rightarrow V_{CC} - V_{R\_C} \geq V_{BE}$

$\rightarrow V_{CC} - V_{BE} \geq V_{R\_C}$

As the operation in the active region requires $V_{BE} > 0$ and $V_{BC} \leq 0$ for npn, V_B must remain higher than the input (V_E). For example, if the dc level of the input (V_E) is zero and $V_B \sim 800$ mV, then the output (V_{CE}) must not fall below approximately 800 mV, i.e. $V_{BC} < 0$, meaning that the voltage drop across R_C cannot exceed $V_{CC} - V_{BE}$.

Analysis of CB Core

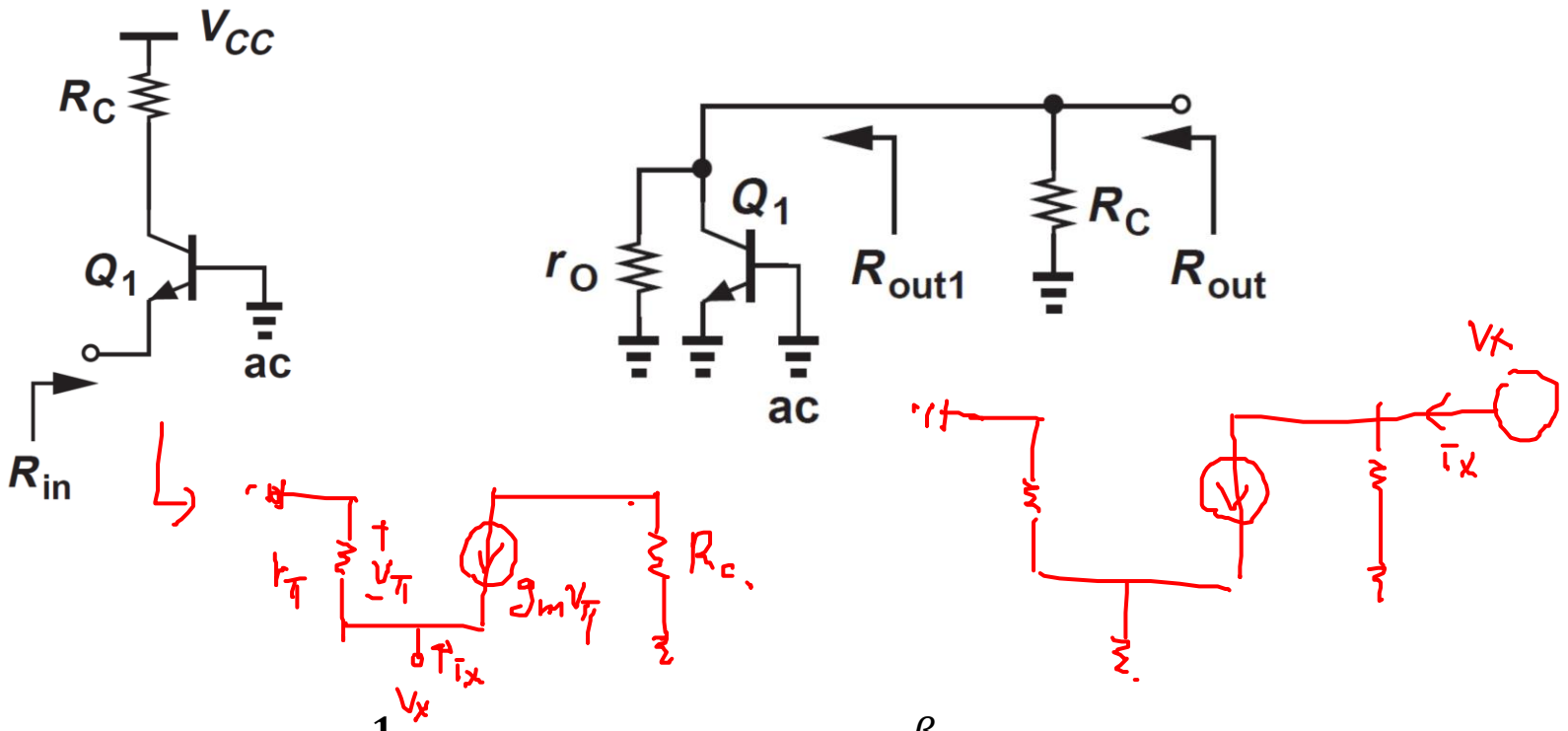


Small signal analysis without Early effect

$V_{out} = -g_m v_\pi R_C$ where $v_{in} = -v_\pi$

Therefore, the gain $\mathbf{A_v = g_m R_C}$

I/O impedances of the CB topology

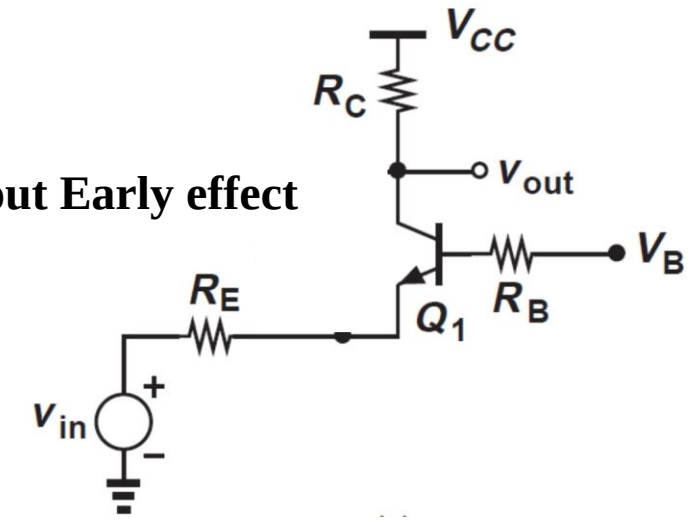


R_{in} in the circuit above is $\frac{1}{g_m}$ $\leftrightarrow$ R_{in} of CE stage = $\frac{\beta}{g_m}$

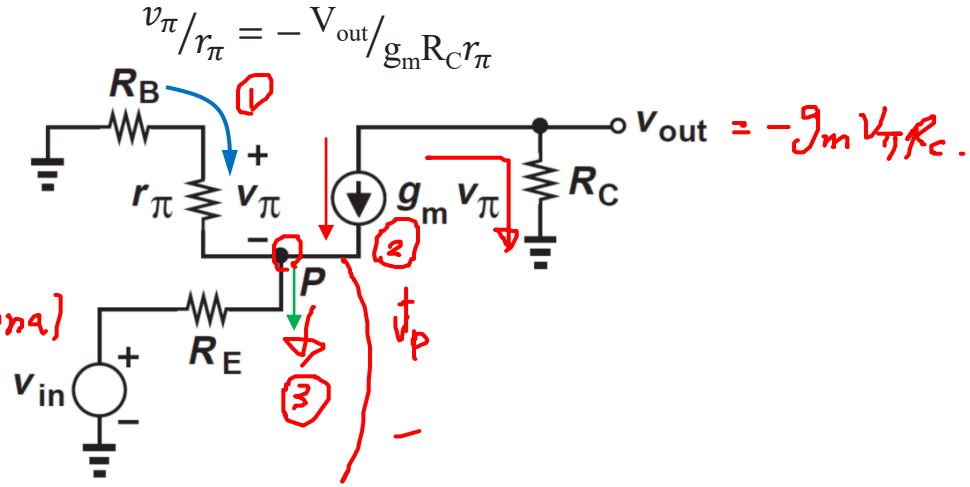
Similarly, $R_{out} = \boldsymbol{R_C \| r_o}$, or we can say simply R_C

General case of the CB topology

Without Early effect



$\Rightarrow$ Small-Signal model

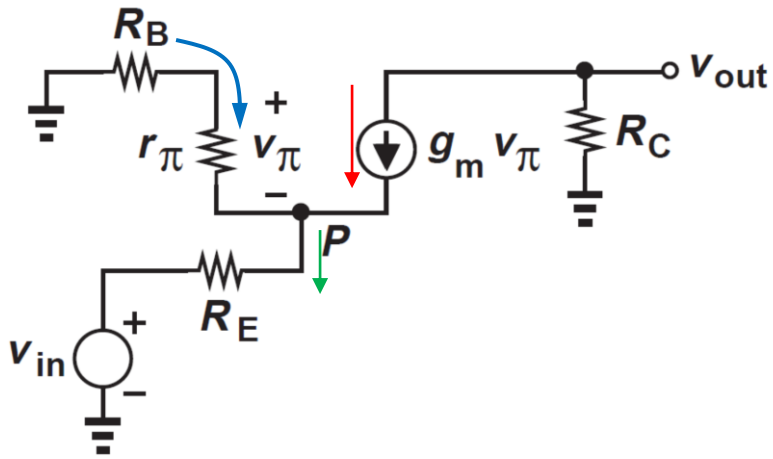


It is obvious that $v_{out} = -g_m v_\pi R_C \rightarrow v_\pi = -V_{out} / g_m R_C$

The current through the v_π node is $v_\pi / r_\pi = -V_{out} / g_m R_C r_\pi$

Therefore, voltage at node p is $v_p = +V_{out} / g_m R_C r_\pi (R_B + r_\pi) = +V_{out} / \beta R_C (R_B + r_\pi)$ $\quad *\boldsymbol{r_\pi = \frac{\beta}{g_m}}$

KCL at node P, we get $\frac{v_\pi}{r_\pi} + g_m v_\pi = \frac{v_p - v_{in}}{R_E}$



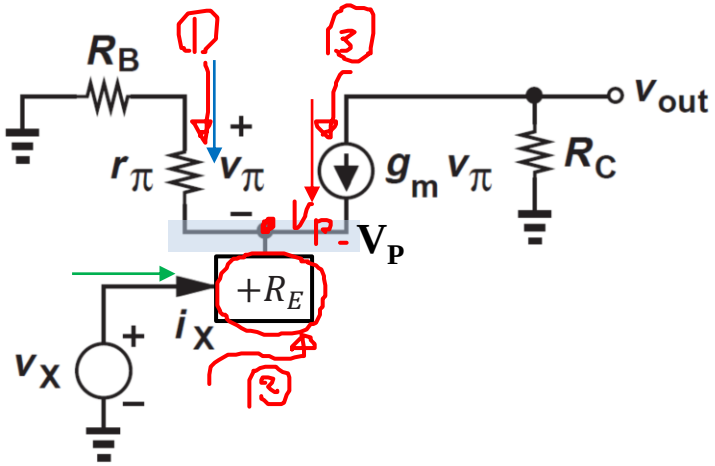
KCL at node P, we get: $\frac{v_\pi}{r_\pi} + g_m v_\pi = \frac{v_p - v_{in}}{R_E}$ (1)

where $v_\pi = -{}^{v_{out}}/_{g_m R_C}$ and $v_p = -{}^{v_{out}}/_{\beta R_C}(R_B + r_\pi)$.

Put v_π and v_p into the equation (1) and rearrange terms, we get

$$\frac{v_{out}}{v_{in}} = \frac{\beta R_C}{(\beta+1)R_E + R_B + r_\pi} \; or \; \approx \frac{R_C}{R_E + \frac{R_B}{\beta+1} + \frac{1}{g_m}}$$

Input Resistance of General CB Topology



$$-v_\pi = \frac{r_\pi}{R_B + r_\pi} v_p, v_p = v_x - R_E i_x$$

KCL at node P gives $\frac{v_\pi}{r_\pi} + i_x + g_m v_\pi = 0$

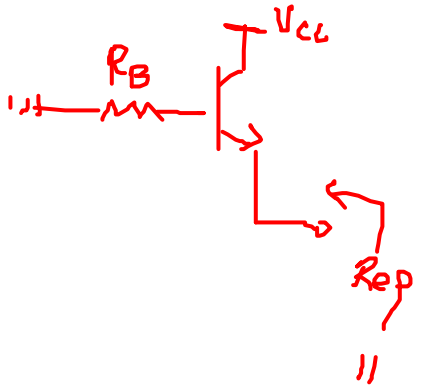
This results in $\left(\frac{1}{r_\pi} + g_m\right) v_\pi + i_x = 0$ where $-v_\pi = \frac{r_\pi}{R_B + r_\pi}(v_x - R_E i_x)$

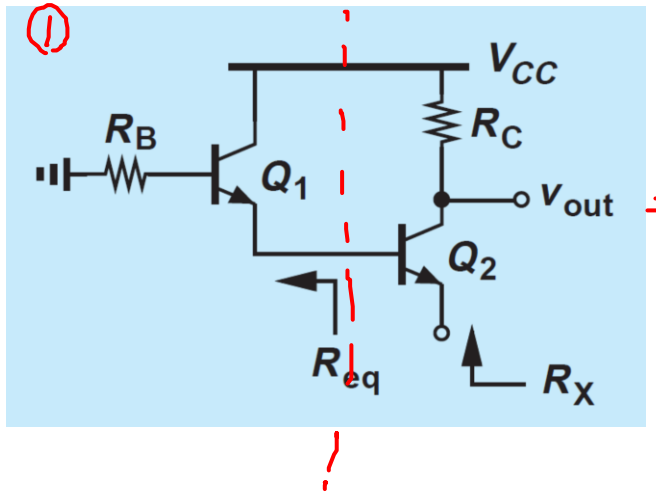
$\left(\frac{1}{r_\pi} + g_m\right) \frac{r_\pi}{R_B + r_\pi}(v_x - R_E i_x) = i_x$ $\quad *\boldsymbol{r_\pi = \frac{\beta}{g_m}}$

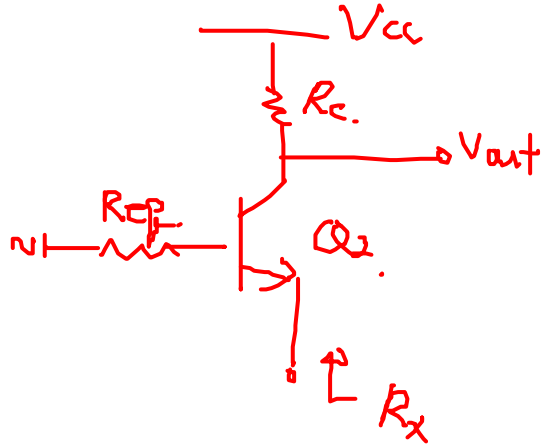
$= 1+\beta$

Rearrange terms we get $\frac{v_x}{i_x} = \boldsymbol{R_E + \frac{R_B + r_\pi}{\beta + 1}}$ or without R_E (series R) $\frac{v_x}{i_x} = \frac{\boldsymbol{R_B}}{\boldsymbol{\beta + 1}} + \frac{\boldsymbol{1}}{\boldsymbol{g_m}}$

Example 13 Determine the impedance seen at the emitter of Q_2 if the two transistors are identical and $V_A = \infty$.







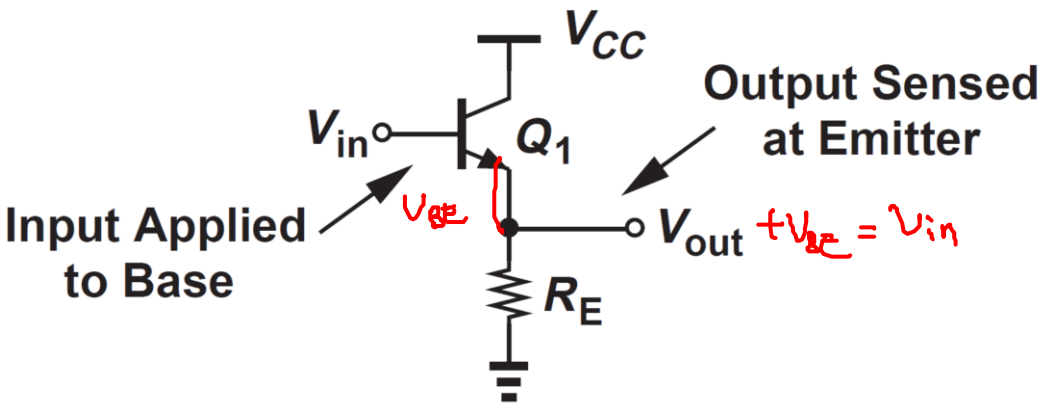
$$R_x = \frac{1}{g_{m2}} + \frac{R_{eq}}{\beta+1}$$

As we just saw $R_{eq} = \frac{1}{g_{m1}} + \frac{R_B}{\beta+1}$

Similarly, $\boldsymbol{R_X} = \frac{1}{g_{m2}} + \frac{R_{eq}}{\beta+1} = \frac{\mathbf{1}}{\boldsymbol{g_{m2}}} + \frac{\mathbf{1}}{\boldsymbol{\beta+1}}\left(\frac{\mathbf{1}}{\boldsymbol{g_{m1}}} + \frac{\boldsymbol{R_B}}{\boldsymbol{\beta+1}}\right)$

$$= \frac{1}{g_{m2}} + \frac{1}{\beta+1}\left(\frac{1}{g_{m1}} + \frac{R_B}{\beta+1}\right)$$

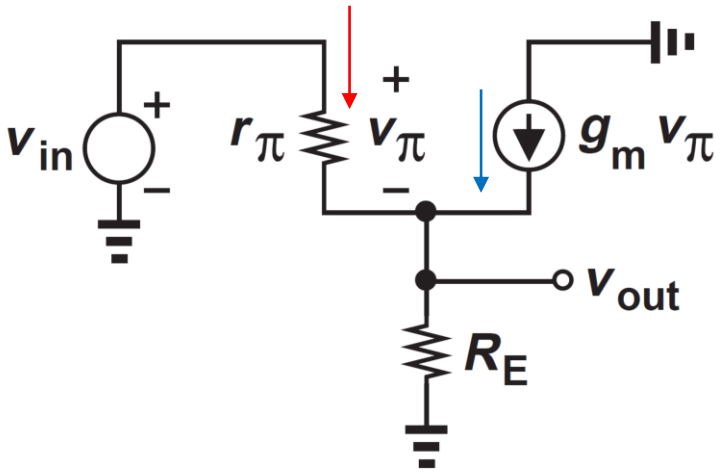
Emitter Follower



If **V_{in} rises** by a small amount V_{in}, the collector and emitter currents increase, leading to a greater drop across R_E and hence **a higher V_{out}**. V_{out} is always lower than V_{in} by an amount equal to V_{BE}, and the circuit is said to provide **level shift**. Also, $V_{out} < V_{in}$ implies that the follower exhibits a **voltage gain less than unity**.

Even though the voltage gain is less than unity, the **input and output impedances** of the emitter follower make it a particularly useful circuit for some applications.

$V_A = \infty$



By small signal analysis, the equivalent circuit yields

$$\frac{v_\pi}{r_\pi} + g_m v_\pi = \frac{v_{out}}{R_E}$$

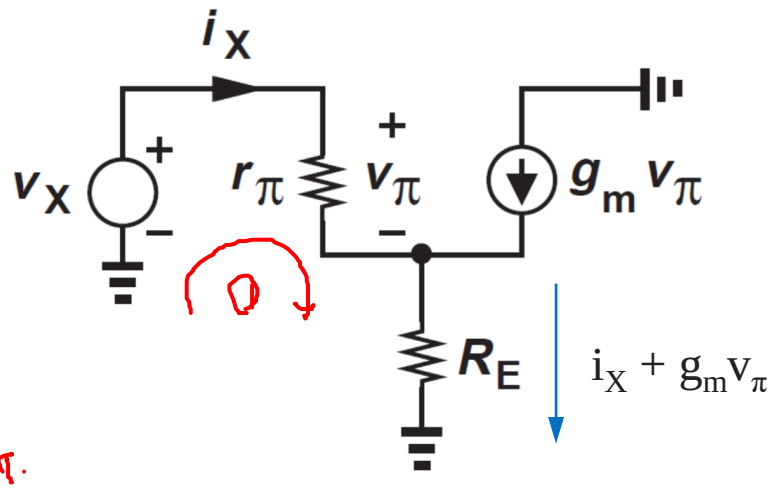
$$v_\pi = \frac{r_\pi}{\beta+1} \cdot \frac{v_{out}}{R_E}$$

$$v_{in} = v_\pi + v_{out}$$

$$\frac{v_{out}}{v_{in}} = \frac{1}{1+\frac{r_\pi}{\beta+1}\cdot\frac{1}{R_E}} \approx \frac{R_E}{R_E+\frac{1}{g_m}}$$

$r_\pi = \beta / g_m \Rightarrow g_m = \beta / r_\pi$

Input Impedances



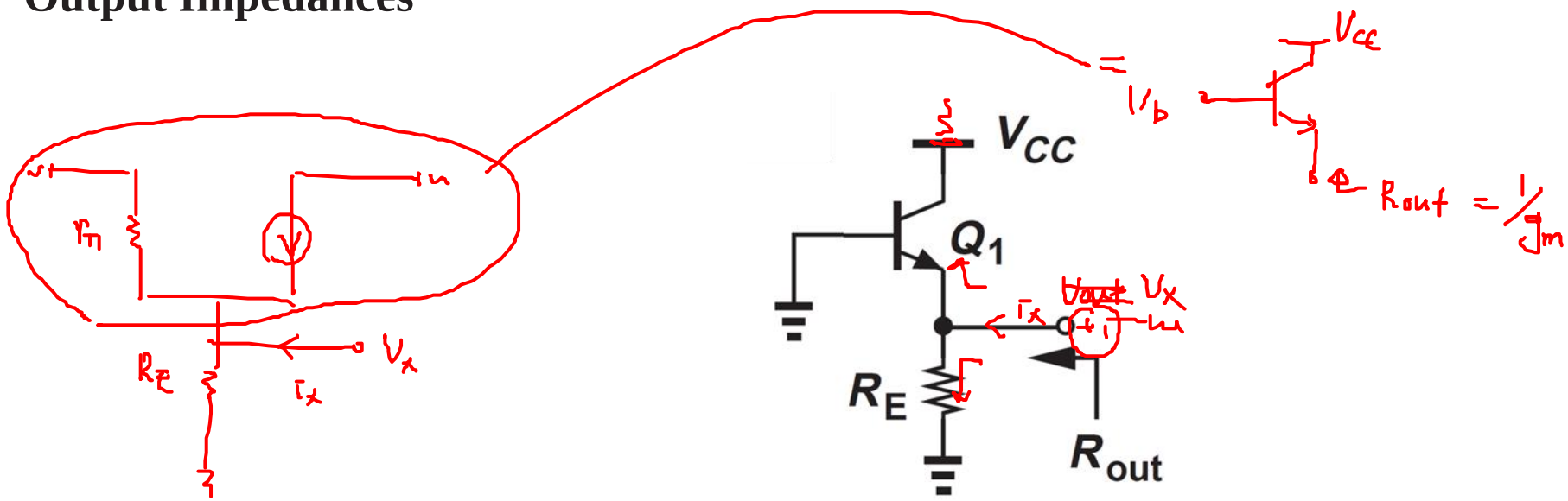
From the circuit above, we can derive
$v_\pi = i_X r_\pi$; a voltage drop at $R_E = (i_X + g_m v_\pi)R_E$

By KVL, we have $v_X = v_\pi + (i_X + g_m v_\pi)R_E = i_X r_\pi + (i_X + g_m v_\pi)R_E$

$\rightarrow \boldsymbol{R_{in} = \frac{v_X}{i_X} = r_\pi + (1 + \beta)R_E}$

The follower transforms the load resistor R_E to a larger value, thereby serving as an **efficient buffer**

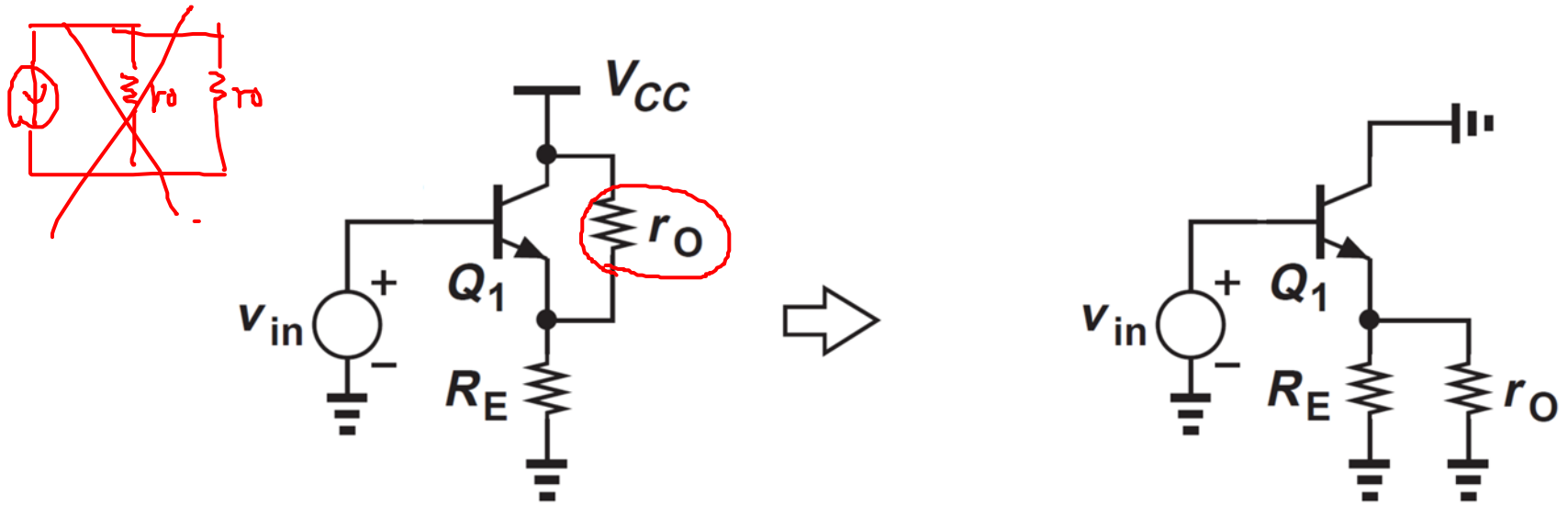
Output Impedances



R_{out} can be obtained by inspection as **R_{out} can be viewed as the parallel combination** of two components: one seen looking up into the emitter and another looking down into R_E.

$$\boldsymbol{R_{out} = \frac{1}{g_m} \| R_E}$$

With Early effect



In small-signal operation, **r_O appears in parallel with R_E**

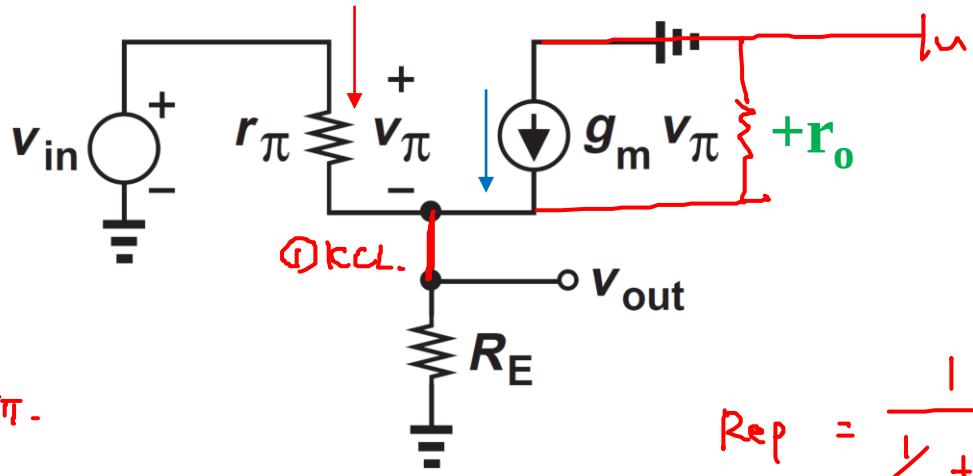
$$A_v = \frac{R_E \| r_O}{R_E \| r_O + \frac{1}{g_m}}$$

$$R_{in} = r_\pi + (1+\beta)(R_E \| r_O)$$

$$R_{out} = \frac{1}{g_m} \| R_E \| r_O$$

With Early effect

(1) Gain



$r_\pi = \beta / g_m \Rightarrow g_m = \beta / r_\pi$.

$R_{eq} = \dfrac{1}{1/R_1 + 1/R_2 + \cdots}$.

By small signal analysis, the equivalent circuit yields

① $\dfrac{v_\pi}{r_\pi} + g_m v_\pi = \dfrac{v_{out}}{R_E} + \dfrac{v_{out}}{r_o} \Rightarrow \left(\dfrac{1}{R_E} + \dfrac{1}{r_o}\right) V_{out}$

$\hookrightarrow \dfrac{1}{R_E \| r_o}$.

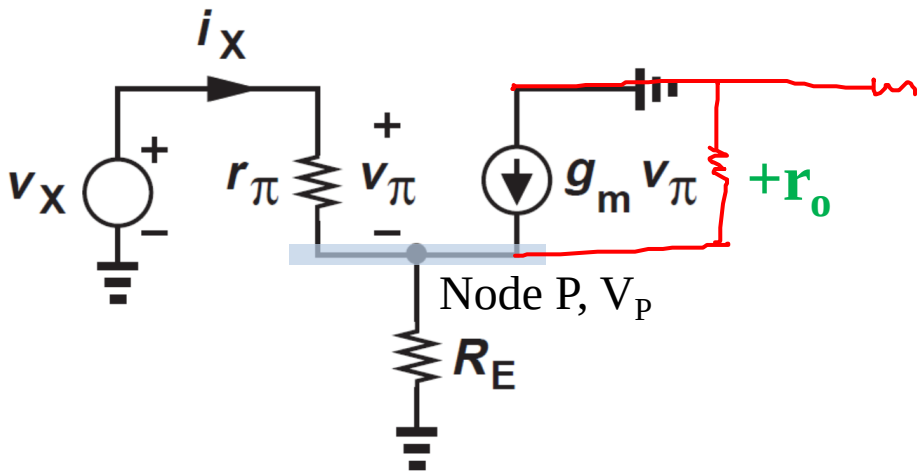
$v_\pi = \dfrac{r_\pi}{\beta+1} \cdot \dfrac{v_{out}}{R_E \| r_o}$

$v_{in} = v_\pi + v_{out}$

$$\frac{v_{out}}{v_{in}} = \frac{1}{1+\frac{r_\pi}{\beta+1}\cdot\frac{1}{R_E \| r_o}} \approx \frac{R_E \| r_o}{R_E \| r_o + \frac{1}{g_m}}$$

With Early effect

(2) Input Impedances



From the circuit above, we can derive

$v_\pi = i_X r_\pi$; $V_P = v_X - v_\pi = v_X - i_X r_\pi$

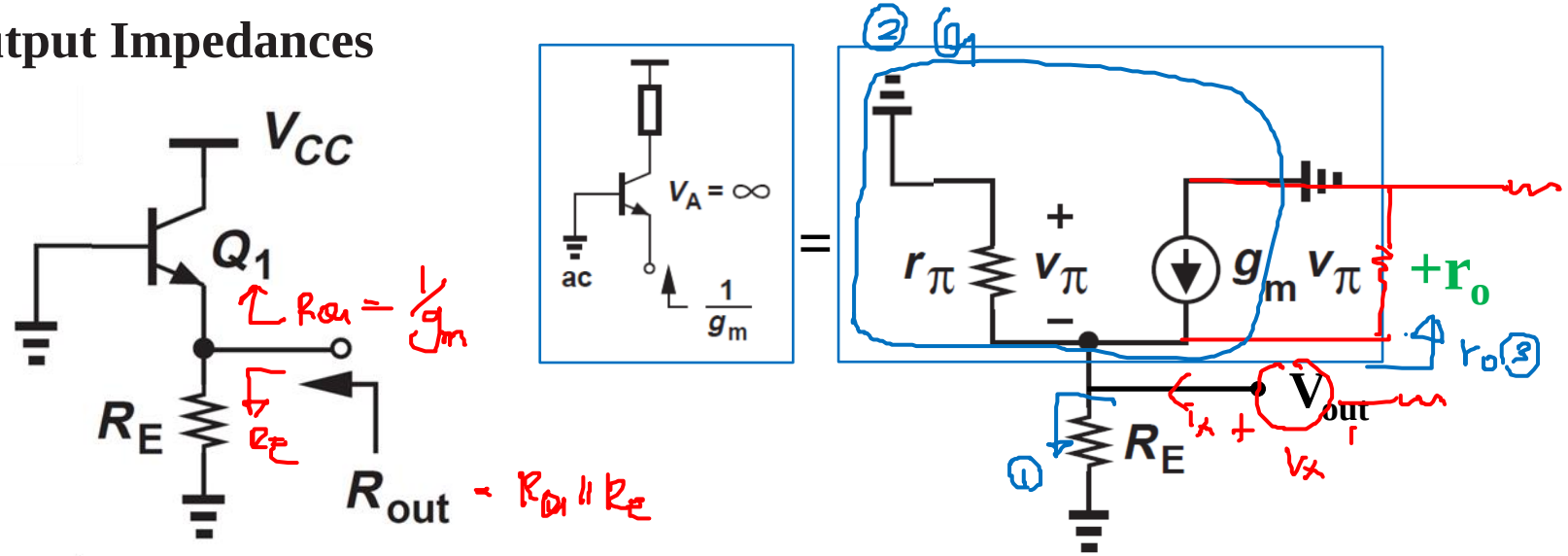
$R_E \| r_o$

By KCL at node P, $i_X + g_m v_\pi = \frac{V_P}{R_E} + \frac{V_P}{r_o}$ where $\frac{1}{R_E} + \frac{1}{r_o} = \frac{1}{R_E \| r_o}$

$$\rightarrow \boldsymbol{R_{in} = \frac{v_X}{i_X} = (1 + g_m r_\pi)(R_E \| r_o) + r_\pi = (1 + \beta)(R_E \| r_o) + r_\pi}$$

With Early effect

(3) Output Impedances

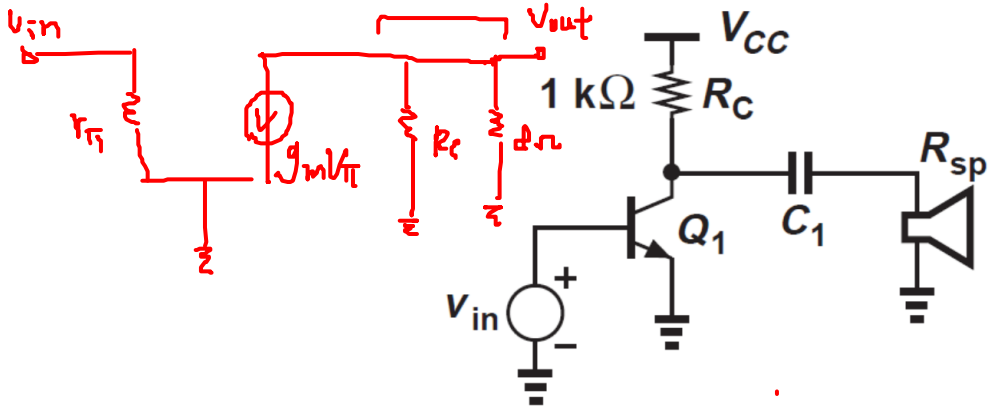


$$\boldsymbol{R_{out}} = \frac{1}{g_m} \| R_E \| r_o$$

Example 14 A CE stage exhibits a voltage gain of 20 and an output resistance of 1 kΩ. Determine the voltage gain of the CE amplifier if

(a) The stage drives an 8 Ω speaker directly.

(b) An emitter follower biased at a current of 5 mA is interposed between the CE stage and the speaker. Assume β = 100, $V_A = \infty$, and the follower is biased with an ideal current source.

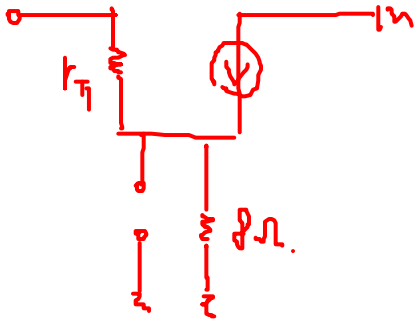


R_c 118 Ω.

$A_v = |-g_m R_c|$

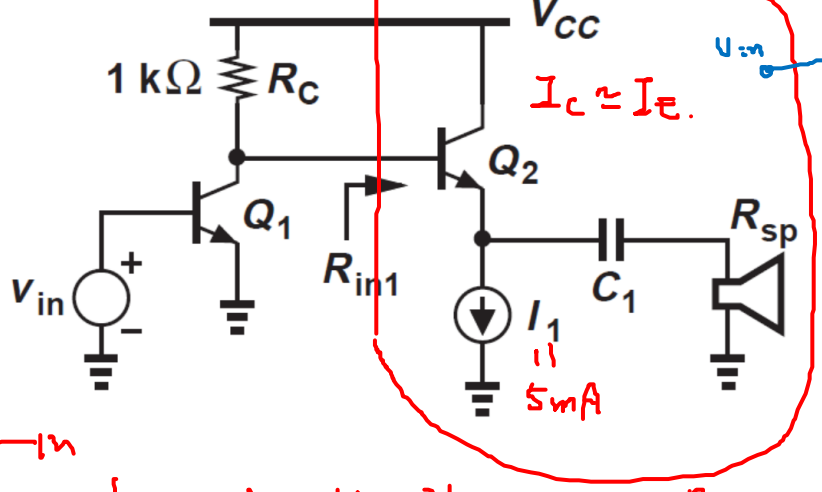
$A_v' = |-g_m (R_c \| 8\Omega)|$.

$= 20 \times \frac{8}{1K} = 0.16$

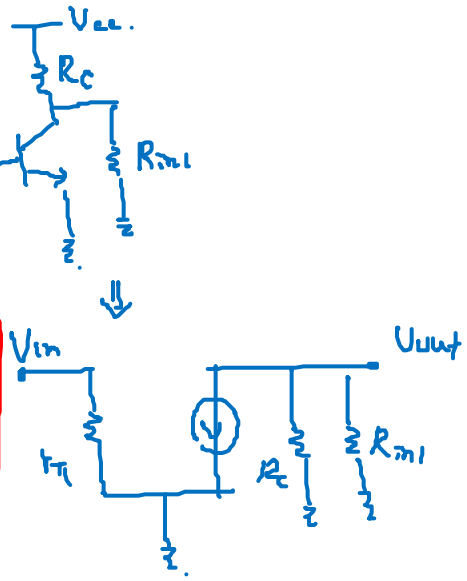


$20 \times \left(\frac{1K \| 1328.8}{1K} \right)$

$A_v'' = -g_m (R_c \| R_{in2}) = 11.41$



$I_C \simeq I_E$.



$R_{in} = r_\pi + (\beta+1) R_E$

$r_\pi = \beta / g_m$

$R_E = R_{sp}$.

$r_\pi = 100 / 0.192$

$g_m = I_C / V_T = \frac{5mA}{0.026} = 0.192$

$R_{in} = 520.8 + 101 \times 8 = 1328.8$ Ω