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ECE3110J/VE311 Electronic Circuits

Current Mirrors

Design of Analog CMOS Integrated Circuits, Chapter 5
Fundamentals of Microelectronics, Chapter 9

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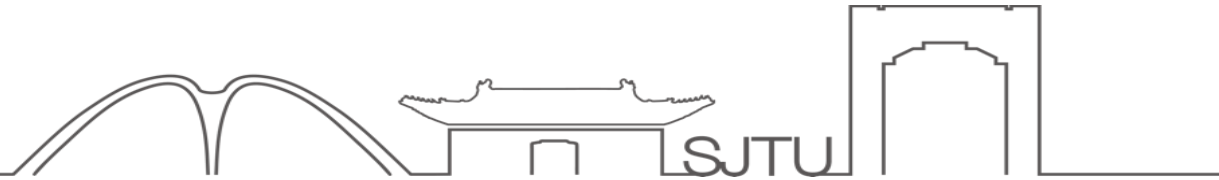
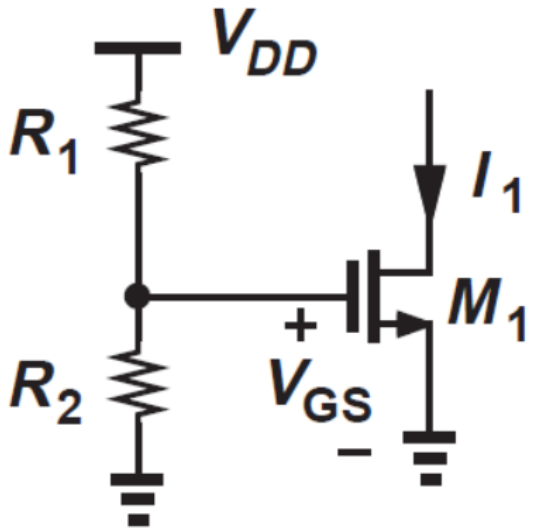


Current Mirror - Initial Thoughts

The biasing techniques studied for MOS amplifiers till now prove inadequate for high-performance microelectronic circuits. For example, **the bias current of CE (BJT) and CS (MOS) stages is a function of the supply voltage**. However, in practice, this voltage experiences some variation, e.g. battery in a cellphone or laptop. **This mandates the circuits operate properly across a range of supply voltages.**

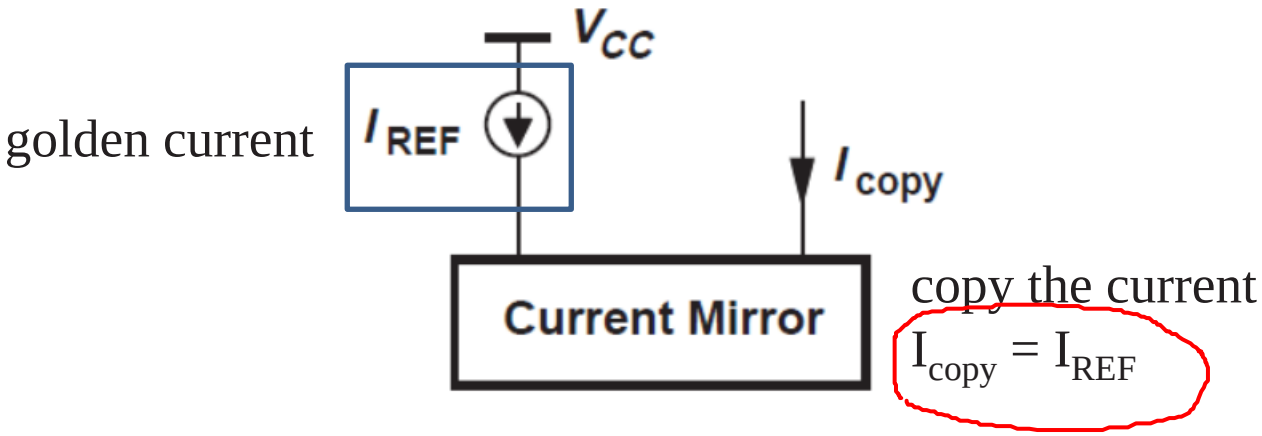
Another critical issue in biasing relates to **ambient temperature variations**. A cellphone must maintain its performance at −20 °C in Finland and +50 °C in Saudi Arabia.



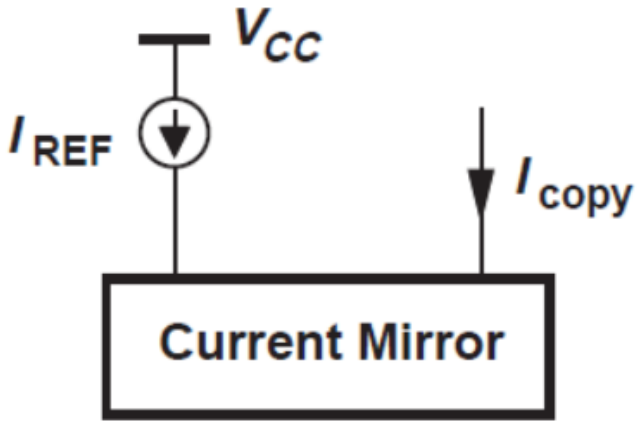
A MOS current source biased by means of a resistive divider **suffers from dependence on V_{DD} and temperature**. Since both the mobility and the threshold voltage vary with temperature, **I_1 is not constant** even if V_{GS} is.

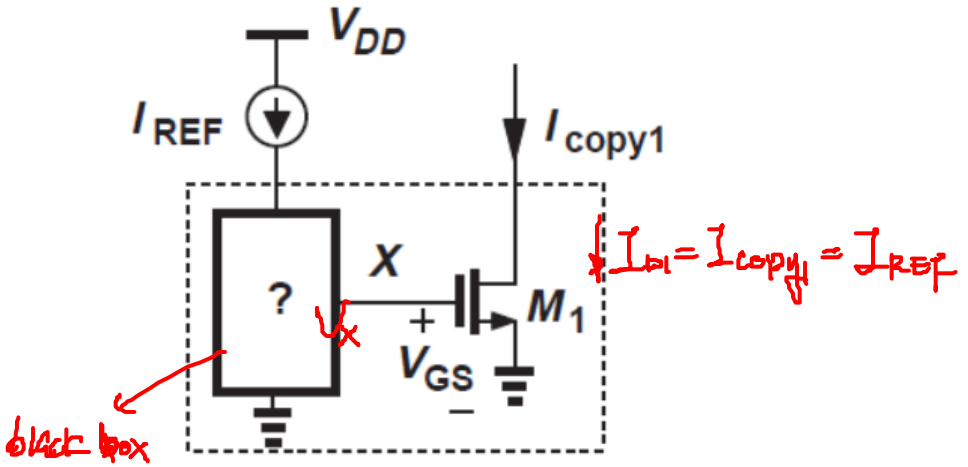
The typical biasing schemes that we have seen so far **fail to establish a constant collector or drain current** if the supply voltage or the ambient temperature are subject to change.

An elegant method of creating **supply- and temperature-independent voltages and currents** exists and appears in almost all microelectronic systems. Called the "**bandgap reference circuit**" and employing several tens of devices, this scheme is studied in more advanced books. However, the complexity of the bandgap prohibits its use for each current source in a large integrated circuit.



In order to avoid supply and temperature dependence, a bandgap reference can provide a "golden current" while requiring a few tens of devices. **We must therefore seek a method of "copying" the golden current without duplicating the entire bandgap circuitry**. This can be done by **current mirrors**.



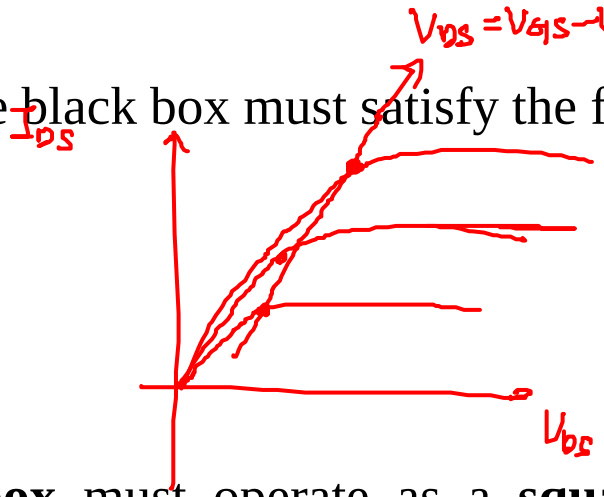


Comparing the diagram and the circuit, the current mirror resembles the topology on the right where **M_1 operates in the saturation region (constant current)** and the **black box guarantees $I_{copy} = I_{REF}$** regardless of temperature or transistor characteristics.

The black box generates an **output voltage, $V_X = V_{GS}$**, such that M_1 carries a current equal to I_{REF} where channel length modulation is neglected.

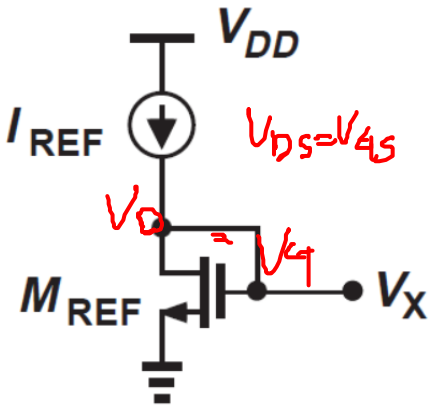
$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_X - V_{TH1})^2 = I_{REF}$$

Therefore, the black box must satisfy the following input/output characteristic:



$$V_X = \sqrt{\frac{2I_{REF}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{TH1}$$

The black box must operate as a **square-root** circuit, i.e. always in saturation. **A diode-connected MOSFET** provides such a characteristic. Diode-connected MOSFET is always in saturation because $V_{DS} \geqq V_{GS} - V_{TH}$, or $V_X \geqq V_X - V_{TH}$ (NMOS)

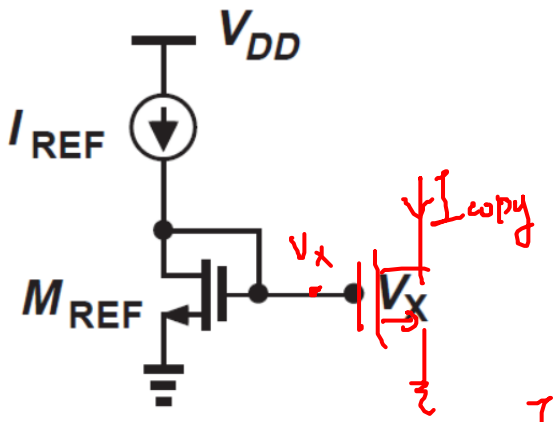


In Triode region,

$$I_D = \mu_n C_{ox} \frac{W}{L_{eff}}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

In saturation,

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L'}(V_{GS} - V_{TH})^2$$



$$I_{REF} = I_{D-REF} = \frac{1}{2}\underbrace{\mu_n C_{ox}}_{k'}\left(\frac{W}{L}\right)_{REF}\underbrace{(V_{GS}-V_{TH})}_{V_{OV-REF}}^2$$

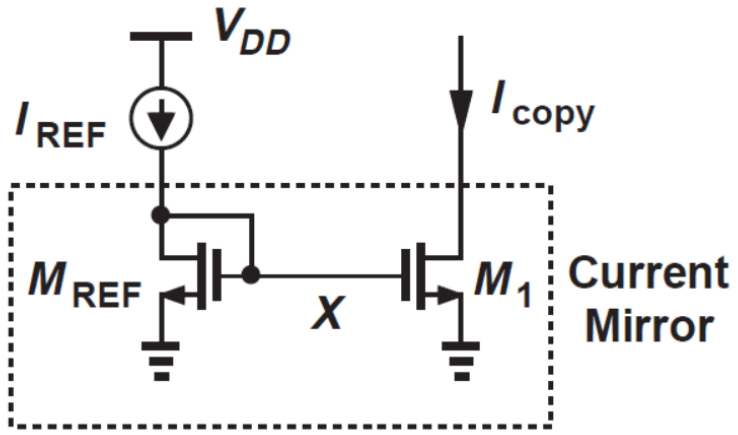
$$V_{OV-REF} = \sqrt{\frac{2I_{REF}}{k'\left(\frac{W}{L}\right)_{REF}}}$$

$$I_{copy} = \frac{k'}{2}\left(\frac{W}{L}\right)_1 (V_X - V_{TH1})^2 \quad , \quad V_X = V_{OV-REF} + V_{TH-REF}$$

$$= \frac{k'}{2}\left(\frac{W}{L}\right)_1 \left(\underbrace{V_{OV-REF}}_{\text{II}} + V_{TH-REF} - V_{TH1}\right)^2$$

$$= \frac{k'}{2}\left(\frac{W}{L}\right)_1 \left(\sqrt{\frac{2I_{REF}}{k'\left(\frac{W}{L}\right)_{REF}}} + V_{TH-REF} - V_{TH1}\right)^2 \quad \text{if } V_{TH-REF} = V_{TH1}$$

$$I_{copy} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_{REF}} \times I_{REF}$$



We can view the circuit's operation from two perspectives:
(1) M_{REF} takes the square root of I_{REF} and M_1 squares the result, or equivalently
(2) The drain currents of the two transistors can be expressed as

$$I_{D,REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{REF}(V_X - V_{TH})^2$$

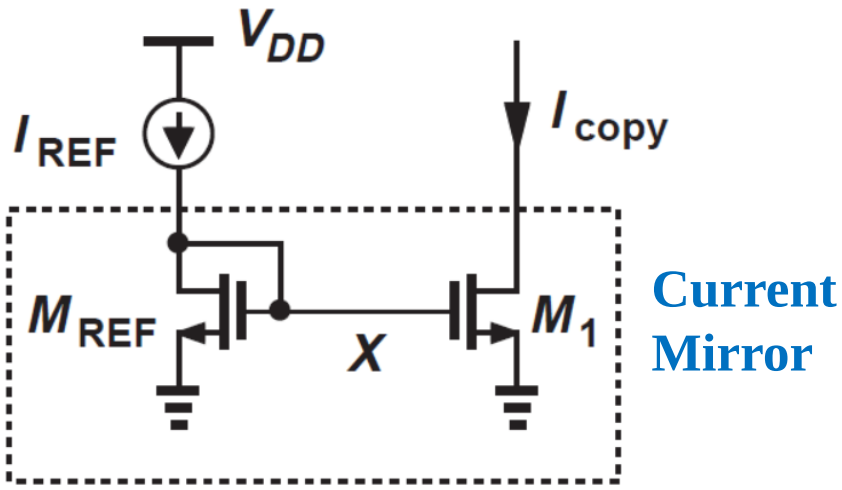
$$I_{copy} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1(V_X - V_{TH})^2,$$

$$I_{copy} = \frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_{REF}} I_{REF},$$

if $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_{REF}$

$I_{copy} = I_{REF}$

$I_{copy} = I_{REF}$ if the two transistors and V_{TH} are identical.



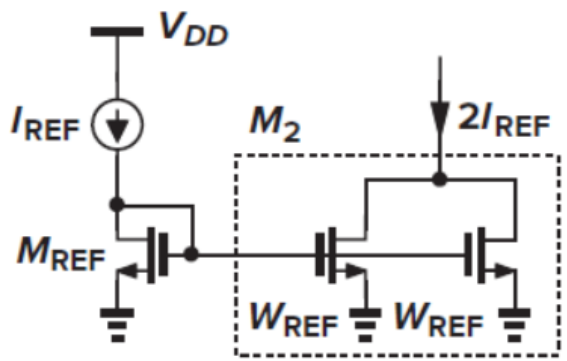
Or simply put, two identical MOS devices that have **equal V_{GS} and operate in saturation carry equal currents.**

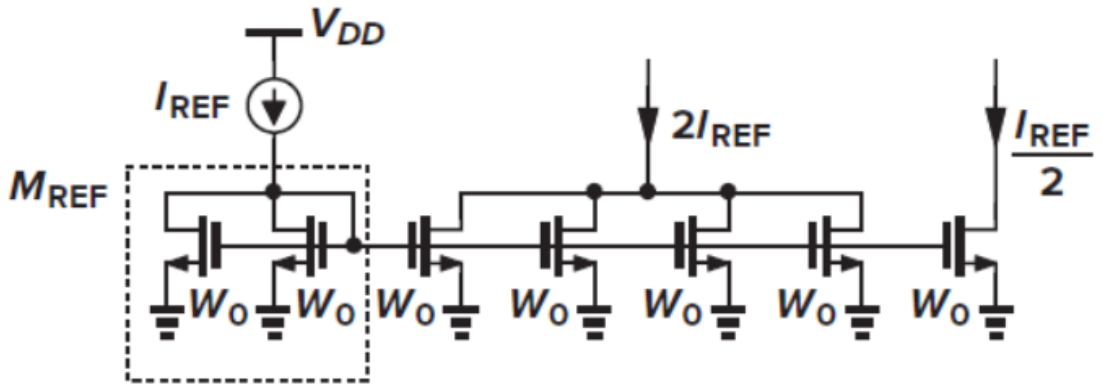
Current mirror allows **precise copying of the current** with no dependence on process and temperature. The ratio of I_{copy} and I_{REF} is given by the ratio of device dimensions, a quantity that can be controlled with reasonable accuracy.

Multiplication of I_{REF}

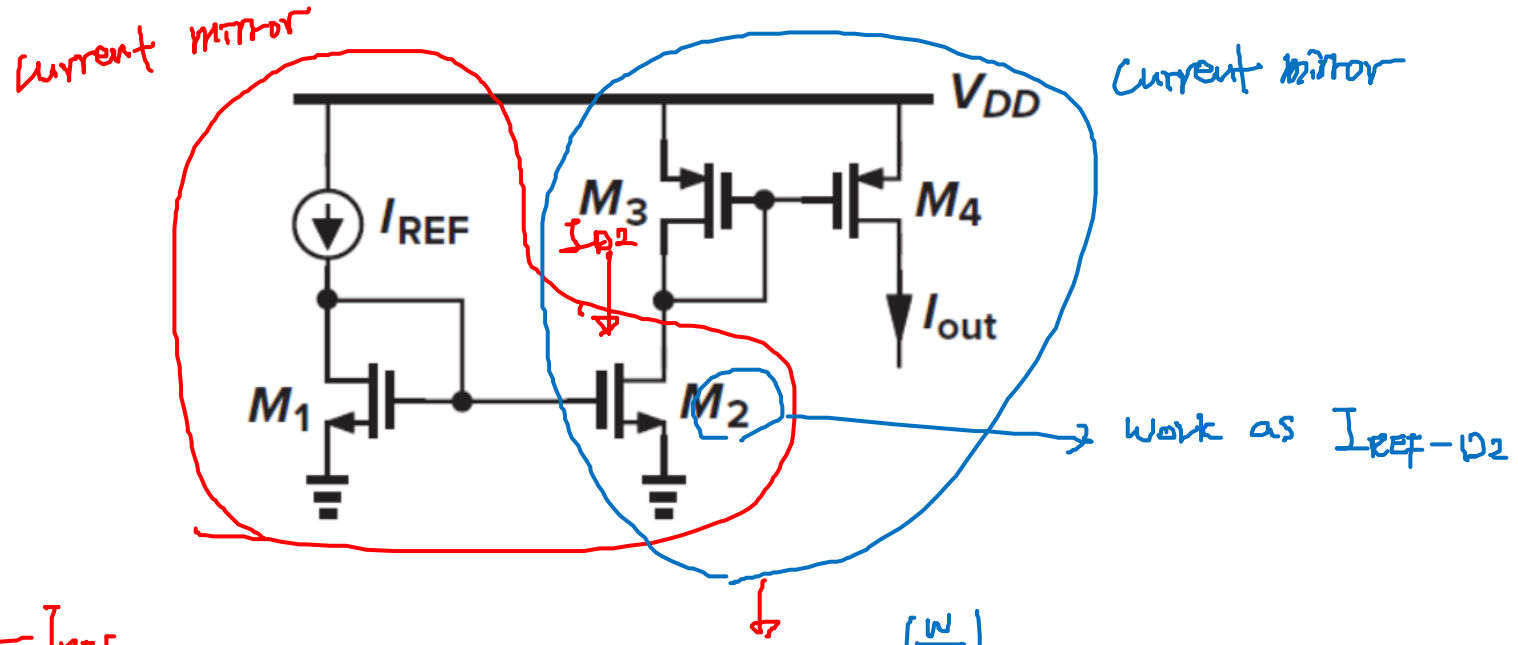
Suppose we wish to **copy a reference current I_{REF} and generate $2I_{REF}$**. We employ a "unit" transistor and **create copies by repeating** such a device.

Then, how about a current equal to **$I_{REF}/2$** from I_{REF}? The diode-connected device itself must consist of two units, each carrying $I_{REF}/2$.





Example 1 Find the drain current of M_4 if all of the transistors are in saturation.

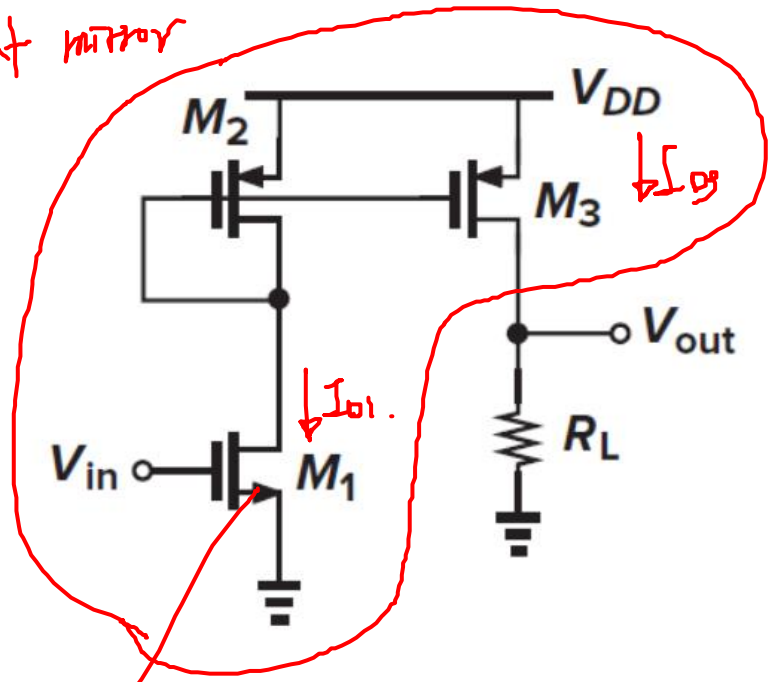


$$I_{D2} = \frac{(W/L)_2}{(W/L)_1} I_{REF}$$

$$I_{out} = I_{D4} = \frac{(W/L)_4}{(W/L)_3} I_{D2}$$

$$I_{out} = \frac{(W/L)_4}{(W/L)_3} \times \frac{(W/L)_2}{(W/L)_1} \times I_{REF}$$

Example 2 Calculate the small-signal voltage gain of the circuit.



$$I_{D3} = \frac{(W/L)_3}{(W/L)_2} \times I_{D1}$$

$$V_{out} = R_L \times I_{D3}$$

$$\Delta V_{out} = R_L \times \Delta I_{D3}$$

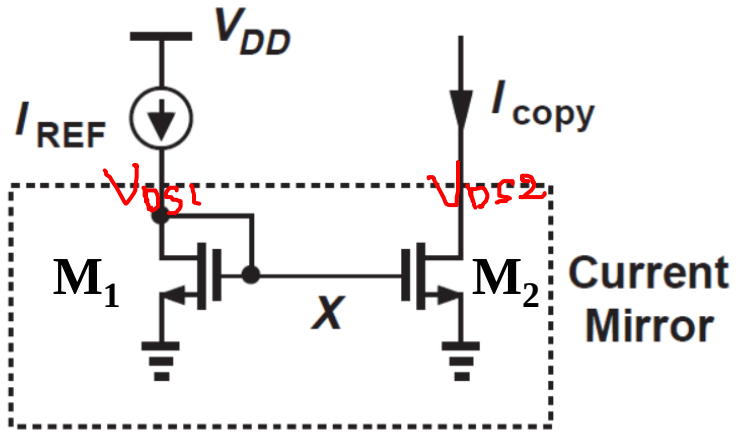
$$= R_L \times \frac{(W/L)_3}{(W/L)_2} \times \Delta I_{D1}$$

$$\Delta I_{D1} = g_{m1} \Delta V_{in}$$

$$A_V = \frac{\Delta V_{out}}{\Delta V_{in}} = R_L \frac{(W/L)_3}{(W/L)_2} g_{m1}.$$

Cascode Current Mirror

In our discussion of current mirrors thus far, we have **neglected channel-length modulation**. In practice, the channel length modulation produces **significant error** in copying currents.



$V_{DS1} = V_{GS1} = V_{GS2}$
V_{DS2} may not equal V_{GS2}

$V_{DS2} \neq V_{DS1}$

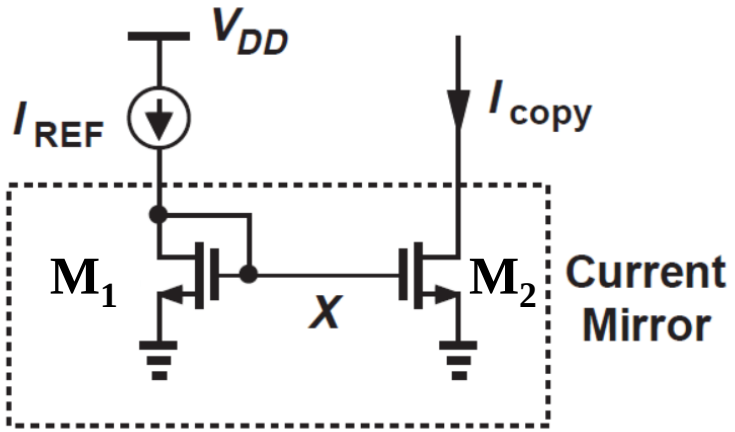
$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS1})$$

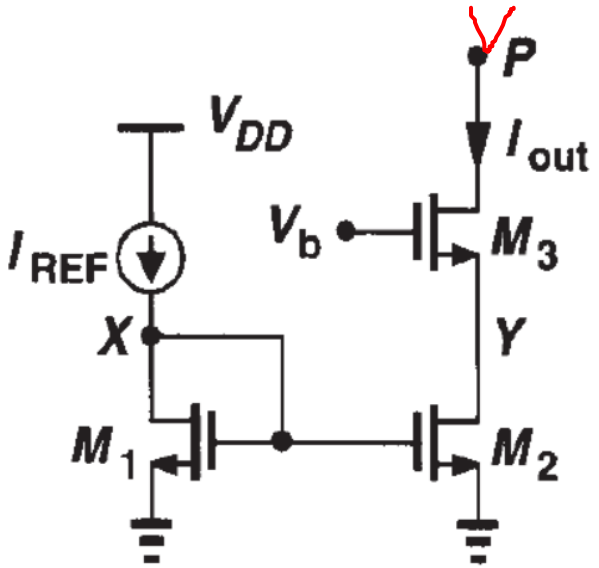
$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS2})$$

V_T

$$\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$

Modification of current mirror structure





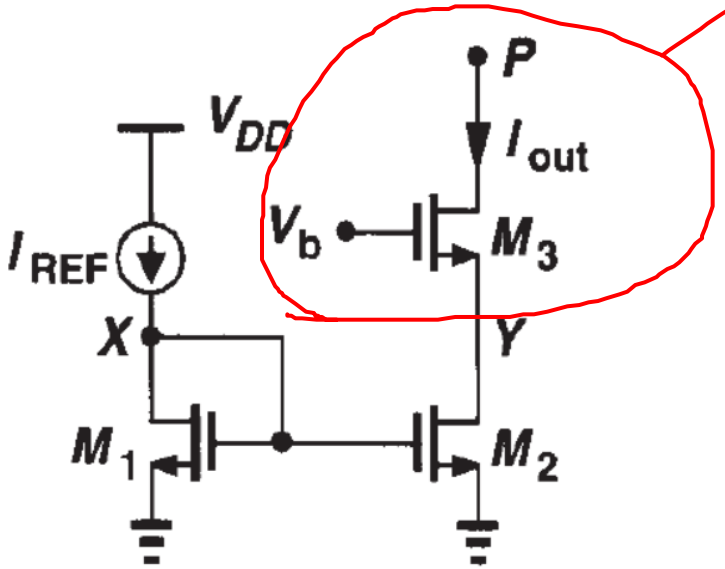
In order to suppress the effect of channel-length modulation, **a cascode current source** can be used. **V_b needs to be chosen such that $V_Y = V_X$, then I_{out} closely tracks I_{REF}.**

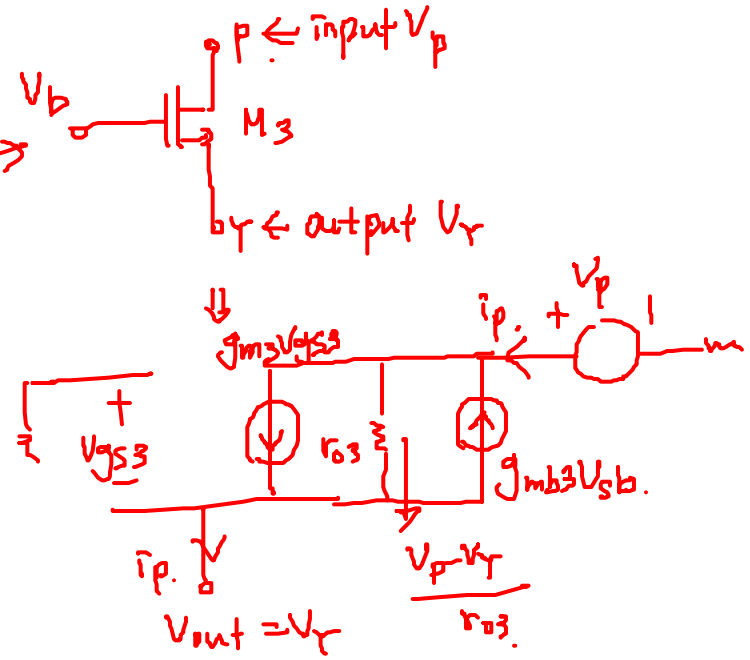
Attributed to cascode design, there is minimal changes between V_P and V_Y, i.e. **changes in V_{DS2} by V_P is minimal**. Therefore, **V_Y remains close to V_X** and hence $I_{D2} \approx I_{D1}$ with high accuracy.

$$\Delta V_Y \approx {\Delta V_P}\Big/{[(g_{m3} + g_{mb3})r_{O3}]}$$

V_Y remains close to V_X ?

$$\Delta V_Y \approx \Delta V_P \Big/ [(g_{m3} + g_{mb3}) r_{O3}]$$





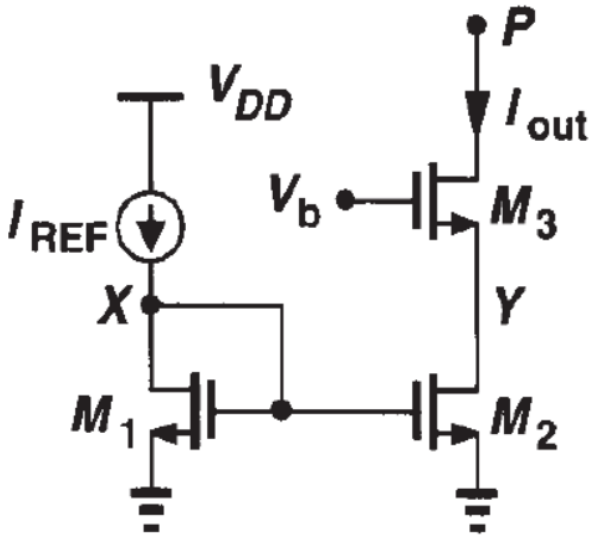
$$-V_{gs3} = V_{out} = V_r = V_{sb}$$

$$g_{m3}V_{gs3} + \frac{V_p - V_r}{r_{O3}} - g_{mb3}V_{sb} = 0$$

V_p and V_r.

$$\Rightarrow V_r = \frac{1}{1 + r_{o3}(g_{m3} + g_{mb3})} V_p$$

Biasing condition for V_b



$\rightarrow V_{GS3} = V_b - V_X$

To ensure $V_Y \approx V_X$, we must guarantee $\mathbf{V_b - V_{GS3} = V_X}$.

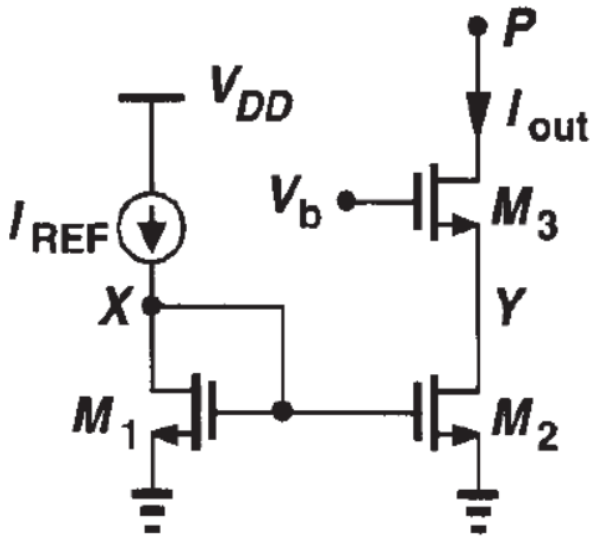
As $V_Y = V_{S3}$ and $V_b = V_{G3}$, $V_{GS3} = V_b - V_Y$. Comparing $V_{GS3} = V_b - V_Y$ and $V_{GS3} = V_b - V_X$ if $V_{GS3} = V_b - V_X$ we guarantee $V_Y \approx V_X$

$V_X + V_{GS3} = V_b$.

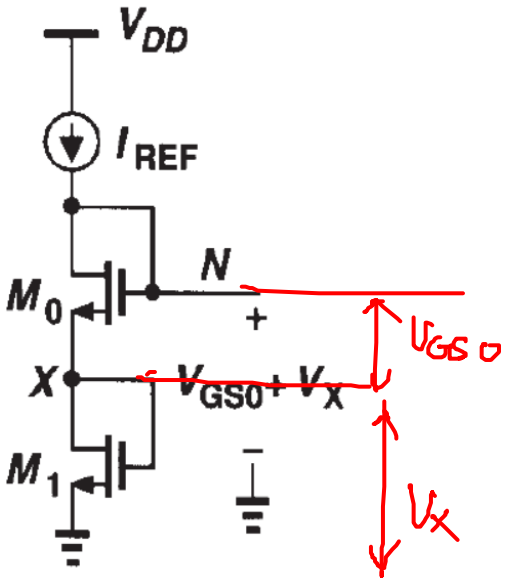
This indicates that **if a V_{GS3} is added to V_X, the required value of V_b can be obtained.**

→ circuit modification required.

Re-modification of current mirror structure

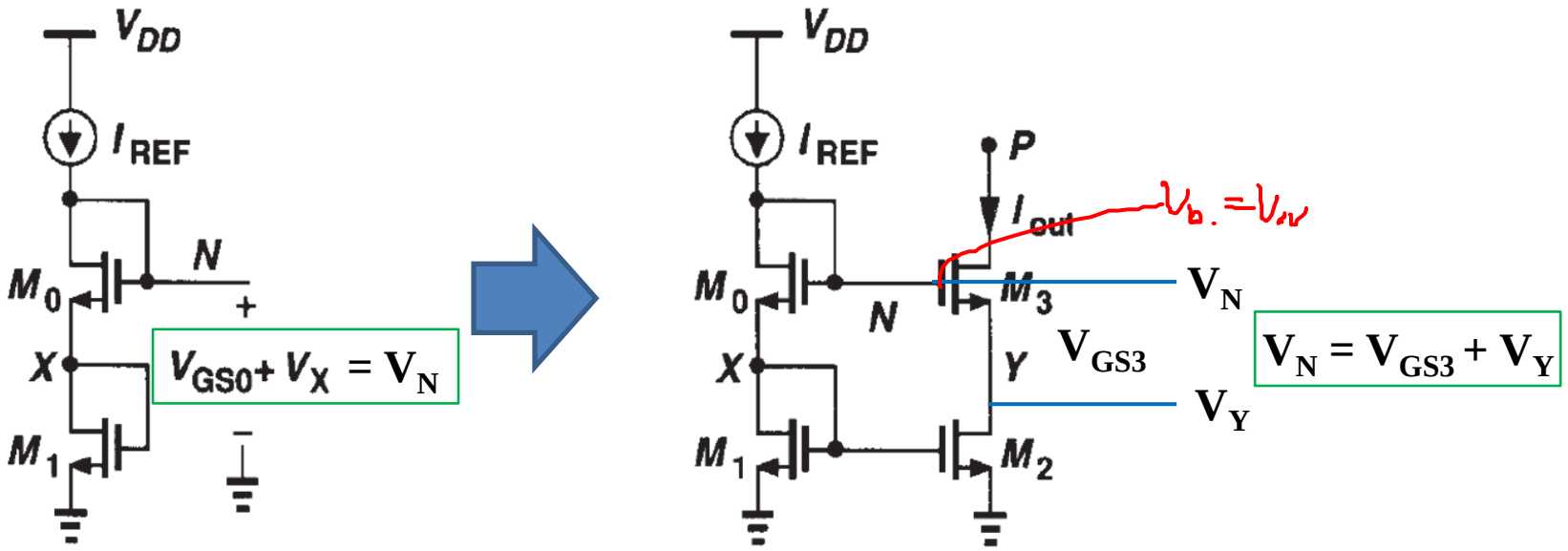


$V_X = V_b - V_{GS3}$



As we saw that $\mathbf{V_X = V_b - V_{GS3}}$, meaning **a $\mathbf{V_{GS3}}$ is added to $\mathbf{V_X}$ to obtain the required value of $\mathbf{V_b}$**. To achieve this, we add **another diode-connected device**, M_0 in series with M_1.

This gives $\mathbf{V_N = V_{GS0} + V_X}$ as $V_G = V_N$ and $V_S = V_X$



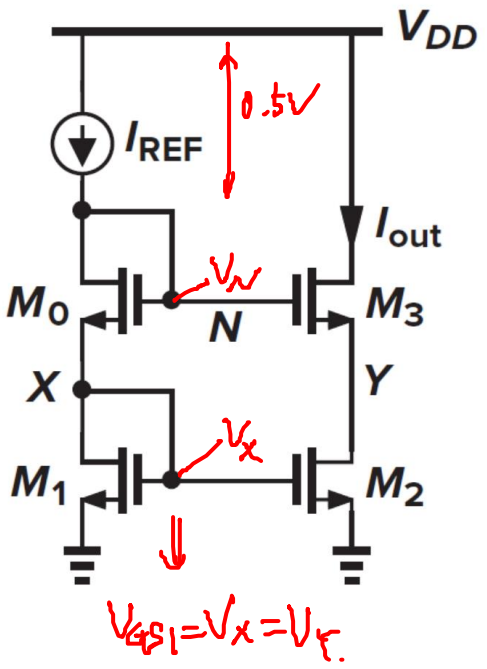
In the modified circuit, V_G of M_0 and $M_3 = V_N$. Thus, $\mathbf{V_N = V_{GS0} + V_X = V_{GS3} + V_Y}$.

Current mirror M_0 and M_3: $\frac{(W/L)_3}{(W/L)_0}$, Current mirror M_1 and M_2: $\frac{(W/L)_2}{(W/L)_1}$

Currents through M_0 (= M_1) = M_3 (= M_2) if $\frac{(W/L)_3}{(W/L)_0} = \frac{(W/L)_2}{(W/L)_1}$, $\mathbf{V_{GS3} = V_{GS0}}$, **and** $\mathbf{V_X = V_Y}$.

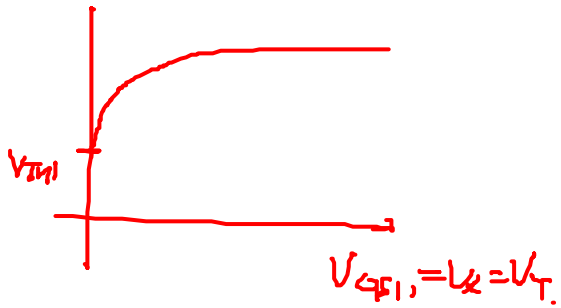
This can be achieved **by a proper choice of the dimensions** of M_0 with respect to those of M_3 yields I_{D0} (= I_{D1}) = I_{D3} (= I_{D2}) because $V_X = V_Y$ (V_{DS}) and $V_{GS0} = V_{GS3}$.

Example 3 Sketch V_X and V_Y as a function of I_{REF}. If I_{REF} requires 0.5 V to operate as a current source, what is its maximum value?



$$I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS1}-V_{TH1})^2$$

$$\Rightarrow V_{GS1} = V_X = V_T = \sqrt{\frac{2I_{REF}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{TH1}$$

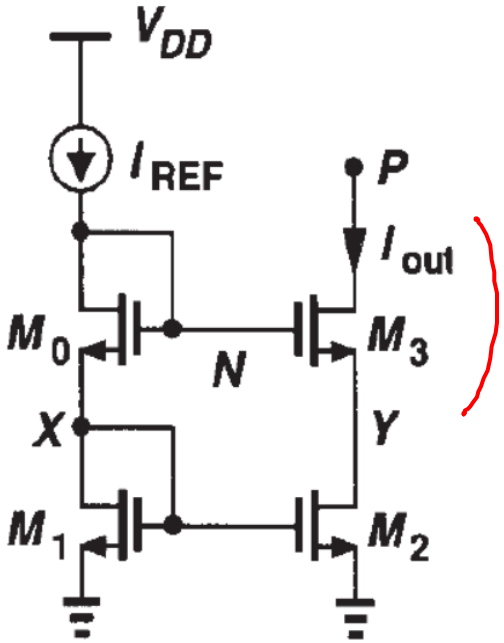


$$V_{DD}-0.5 = V_N \leftarrow V_N = V_{GS0}+V_{GS1} = \sqrt{\frac{2I_{REF}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_0}} + \sqrt{\frac{2I_{REF}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{TH0}+V_{TH1}$$

$$V_{DD}-V_N = 0.5$$

$$I_{REF} = \frac{(V_{DD}-0.5-V_{TH0}-V_{TH1})^2 \times \mu_n C_{ox}}{2\left[\sqrt{\left(\frac{W}{L}\right)_0}+\sqrt{\left(\frac{W}{L}\right)_1}\right]^2}$$

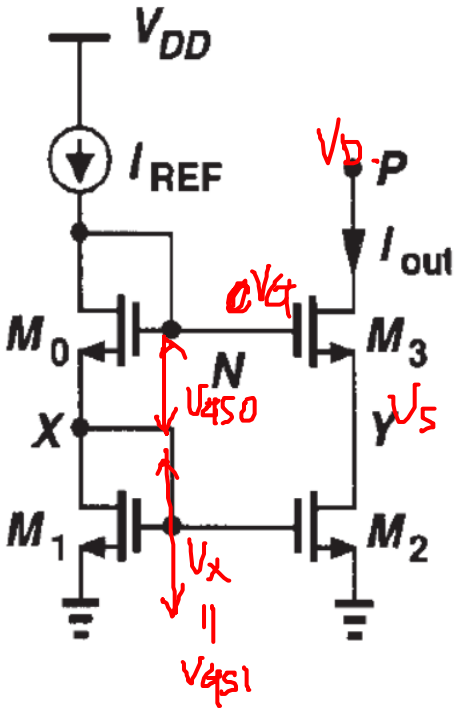
Issues in voltage headroom



$V_{DS} = V_{GS} - V_{TH}$ edge of sat.
"
min. voltage required

While operating as a current source with a high output impedance and accurate value, the modified topology nonetheless **consumes substantial voltage headroom**.

Assume no the body effect and all of the transistors are identical, **the minimum allowable voltage for saturation at node *P*** is $\mathbf{V_P = V_N - V_{TH}}$ overdrive voltage



$$\mathbf{V_P = V_N - V_{TH}}$$

because

$V_{GS} = V_N - V_Y$

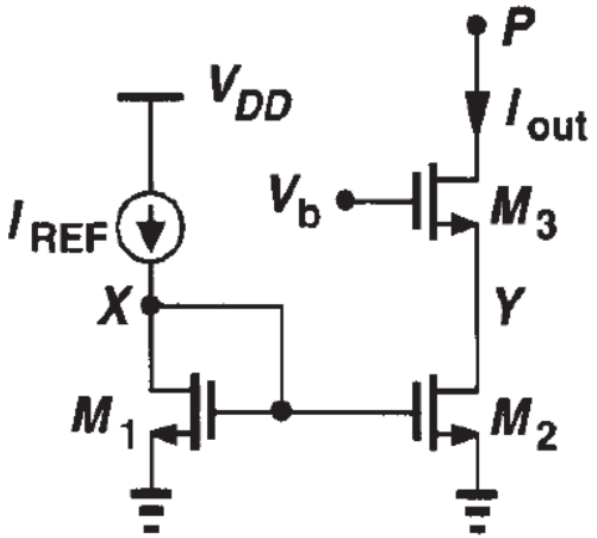
$V_{DS} = V_P - V_Y$

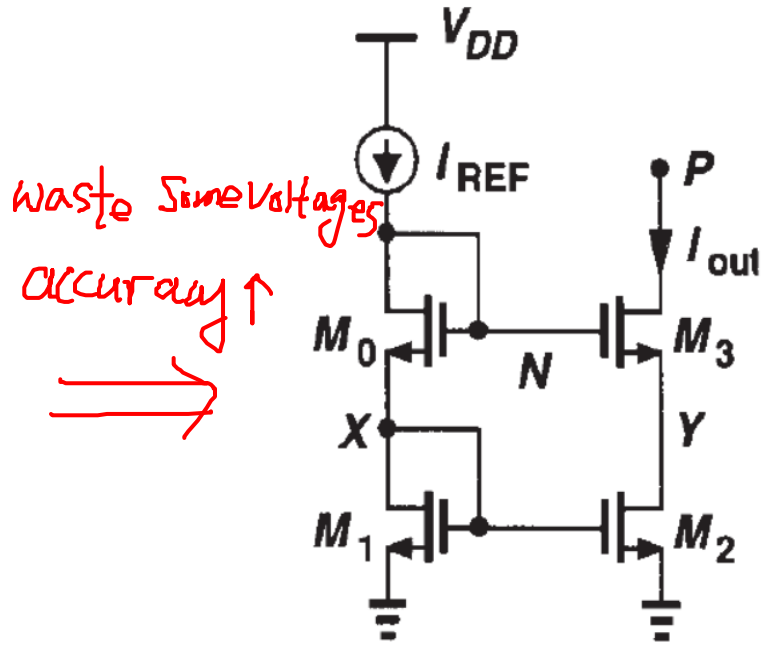
Minimum saturation condition $V_{DS} = V_{GS} - V_{TH}$

Thus, $\mathbf{V_P - V_Y = V_N - V_Y - V_{TH}} \rightarrow \mathbf{V_P = V_N - V_{TH}}$

$$\mathbf{V_N} = V_{GS0} + V_X = \mathbf{V_{GS0} + V_{GS1}} \rightarrow V_P = V_N - V_{TH} = V_{GS0} + V_{GS1} - V_{TH}$$

$$= \mathbf{(V_{GS0} - V_{TH}) + (V_{GS1} - V_{TH}) + V_{TH}}$$



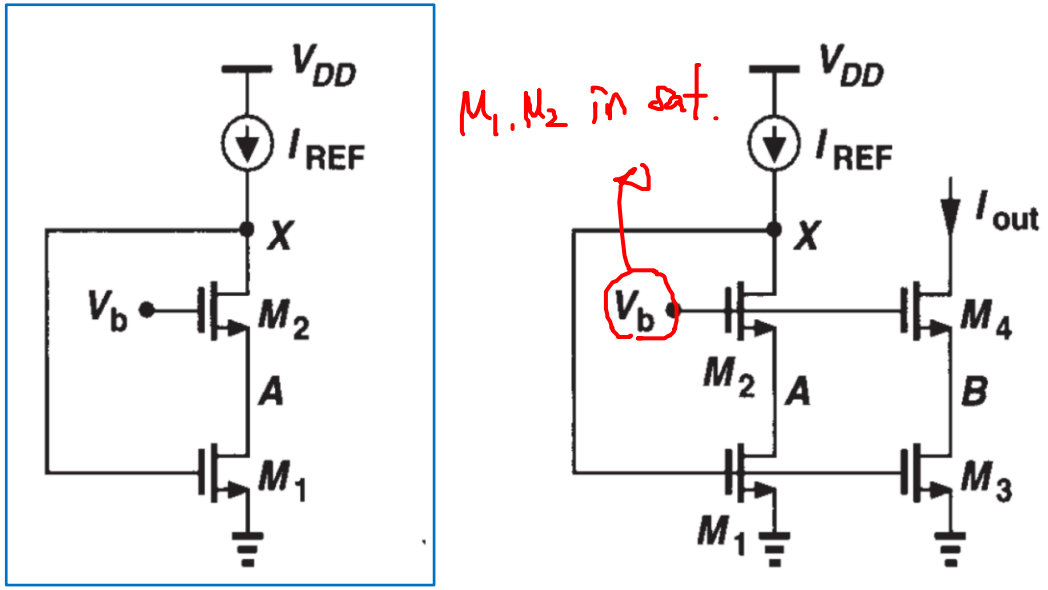


$V_{DS} = V_{GS} - V_{TH}$.

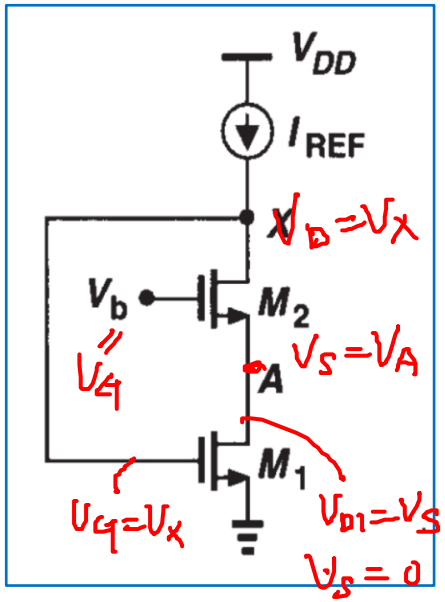
Meanwhile, the previous model (**Left**) offers minimum saturation conditions: $\mathbf{(V_{GS2} - V_{TH2}) + (V_{GS3} - V_{TH3})}$ as for M_2 and M_3 in saturation: $V_{DS} = V_{GS} - V_{TH}$

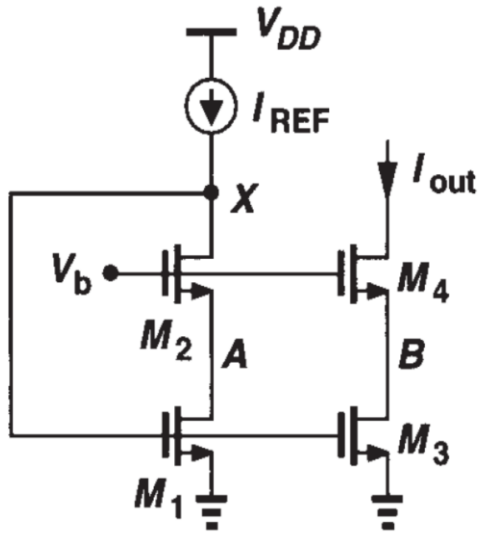
Therefore, the model (**Right**) **wastes one threshold voltage in the headroom**.
The model left, however, suffers from **lower accuracy** as we discussed, due to the fact that $V_X \neq V_Y$.

Re-remodification of current mirror structure



In order to eliminate the accuracy-headroom trade-off, we modify the circuit design again. Consider the **first circuit (left)** which is a cascode topology where output is shorted with its input, **V_b needs to be determined so that both M_1 and M_2 are in saturation**.





For M_2 in saturation

$V_{DS} \geq V_{GS} - V_{TH2}$ where $V_{DS} = V_X - V_A$ and $V_{GS} = V_b - V_A$

Thus, $\mathbf{V_X \geq V_b - V_{TH2}}$, **or** $\mathbf{V_b \leq V_X\ (= V_{GS1}) + V_{TH2}}$

max.

For M_1 in saturation

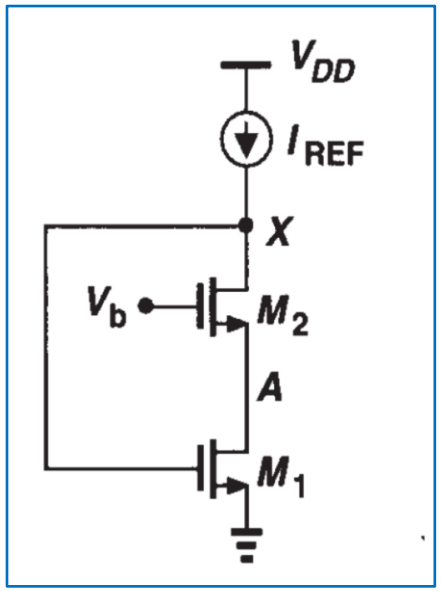
$V_{DS} = V_A$ and $V_{GS} = V_X$, thus $\mathbf{V_A \geq V_X - V_{TH1}}$

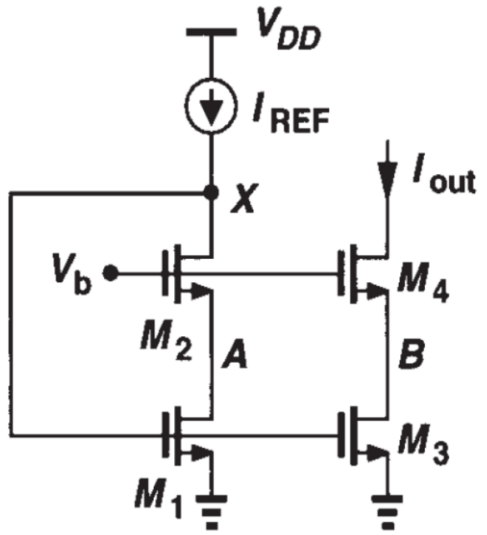
Because $V_A = V_b - V_{GS2}$, $\mathbf{V_b - V_{GS2} \geq V_X - V_{TH1}}$, **or** $\mathbf{V_b \geq V_X\ (= V_{GS1}) - V_{TH1} + V_{GS2}}$

from V_{GS2} of M_2.

bias condition to make M_1 and M_2 in sat

Thus, finally, $\mathbf{V_{GS1} - V_{TH1} + V_{GS2} \leq V_b \leq V_{GS1} + V_{TH2}}$



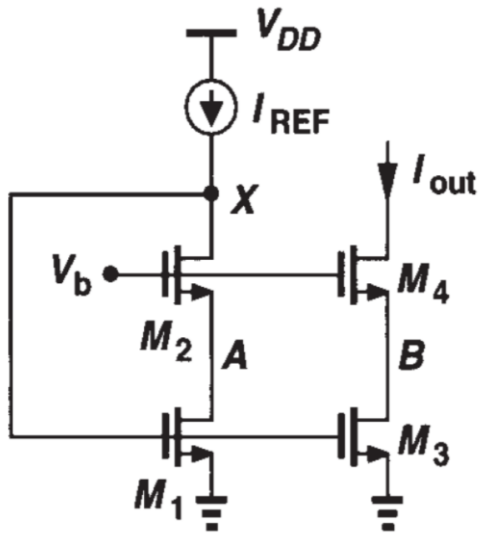


overdrive

$(V_{GS1} - V_{TH1}) + V_{GS2} \leq V_{GS1} + V_{TH2}$, or $\mathbf{V_{GS2} - V_{TH2} \leq V_{TH1}}$

We must therefore **size M_2 down** such that its overdrive voltage remains less than one threshold voltage.

Low voltage cascode current mirror

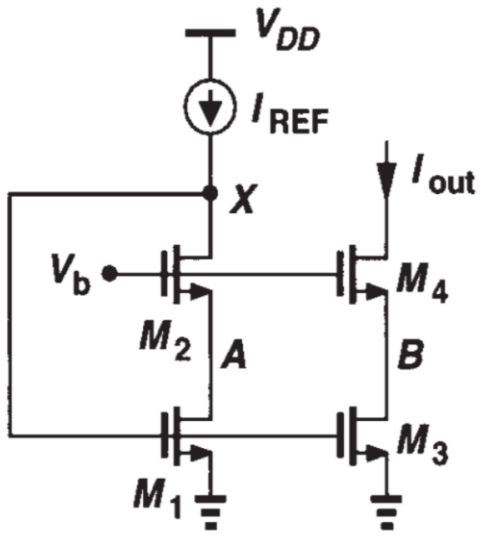


Given condition.

We now modify the circuit as shown above and assume that **M_1-M_4 are in saturation** and proper rationing ensure that **$V_{GS2} = V_{GS4}$**

V_{GS4} V_{GS3} V_{TH3}

Referring to the result in previous slide, we set **$V_b = V_{GS2} + (V_{GS1} - V_{TH1})$**, which gives us biasing condition to M_3 and M_4 of **$V_{GS4} + (V_{GS3} - V_{TH3})$**



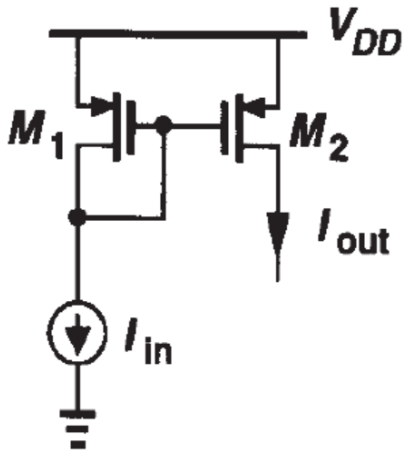
Same $2V_{TH}$.

Consumes minimum headroom of $\mathbf{V_{GS4} + (V_{GS3} - V_{TH3})}$ while M_1 and M_3 sustain **equal** $\mathbf{V_{DS}}$.
Guarantees **accurate copying of** $\mathbf{I_{REF}}$.

For minimal voltage headroom consumption, V_A (= V_{DS}) = $V_{GS1} - V_{TH1}$
And $V_{GS2} = V_b - V_A$, and thus, approximately $\mathbf{V_b = V_{GS2} + V_{GS1} - V_{TH1}}$

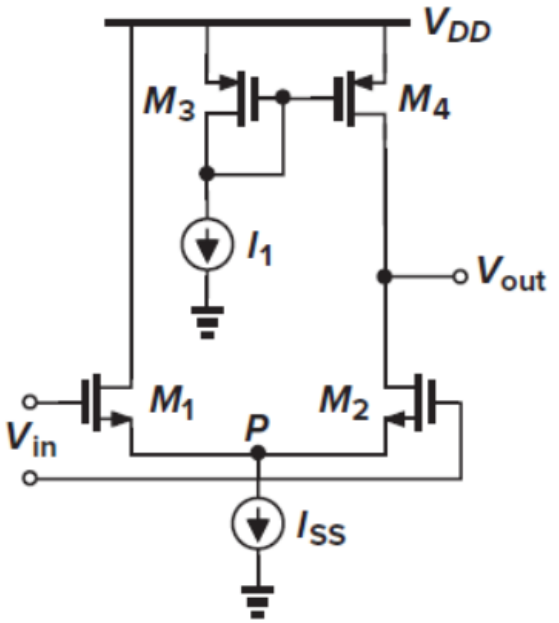
Active Current Mirror

Current mirrors can also process signals, i.e., operate as **active elements**. Particularly useful is a type of mirror topology used in conjunction with differential pairs.



If M_1 and M_2 with $\lambda = 0$ are identical, the current mirror design left has $\mathbf{I_{in} = I_{out}}$**.** The circuit performs no inversion, meaning that if $\mathbf{I_{in}}$ **increases by ΔI, so does** $\mathbf{I_{out}}$.

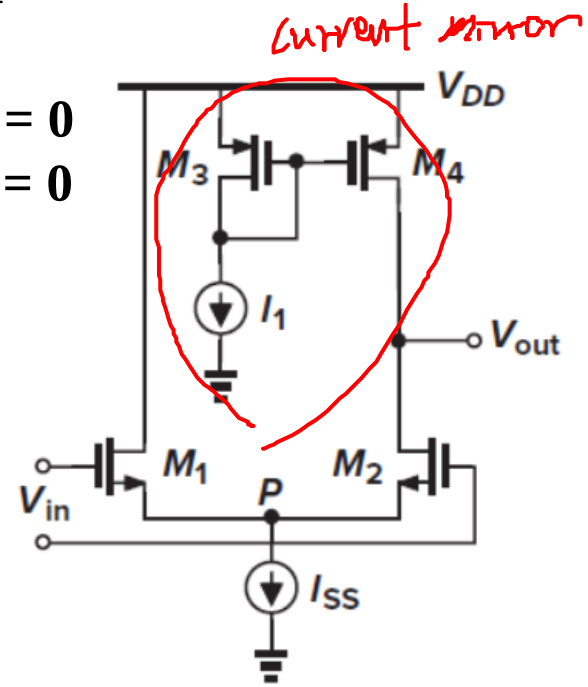
We now **combine this current mirror with differential amplifier.** What is the small-signal gain of this circuit?



Approach 1

$\lambda = 0$

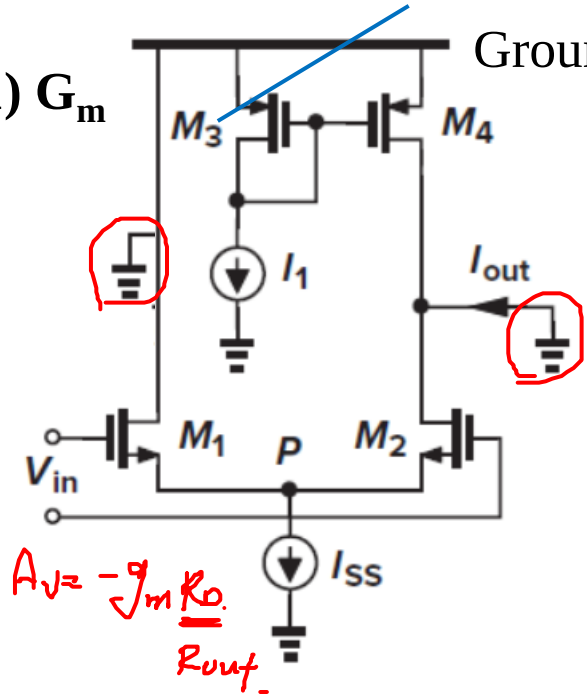
$\gamma = 0$



In small signal

(1) G_m

Ground



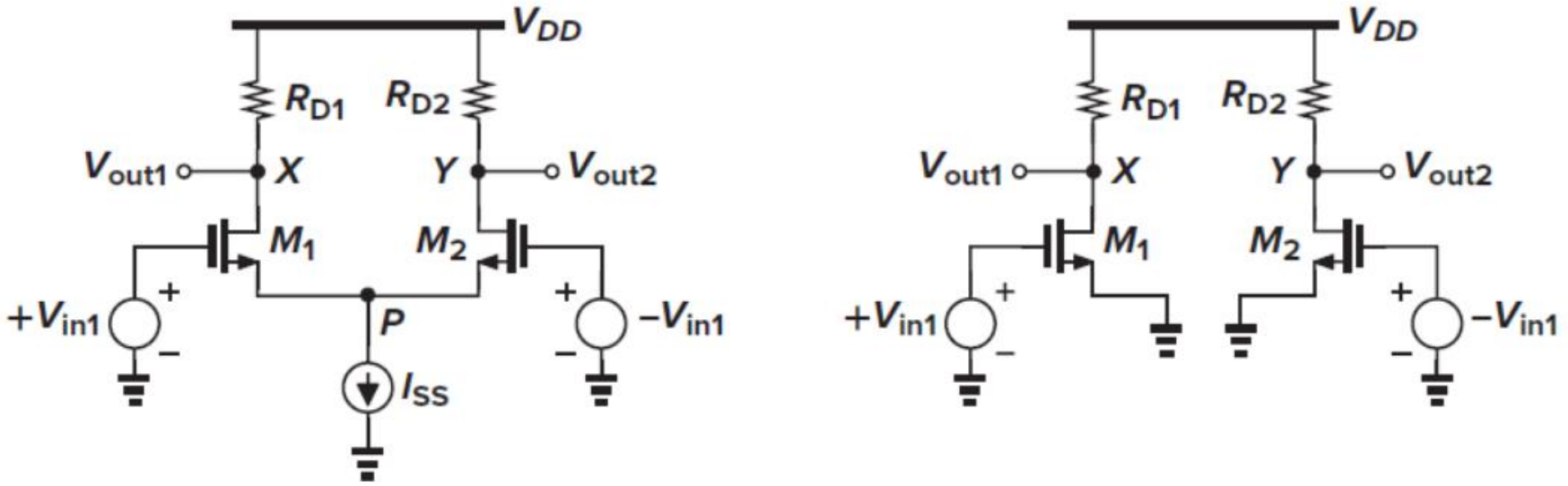
Gain of the circuit is $|A_v| = G_m R_{out}$

In a small signal model to find G_m, **M_1 and M_2 become symmetric** when the output is shorted to ac ground. We use **half circuit analysis** where there is only one output.

Therefore, $|G_m|$ is halved and is $g_{m1}/2$

$v_{out} = -G_m v_{in} R_{out}$, V_{out} **is halved, then G_m is halved**

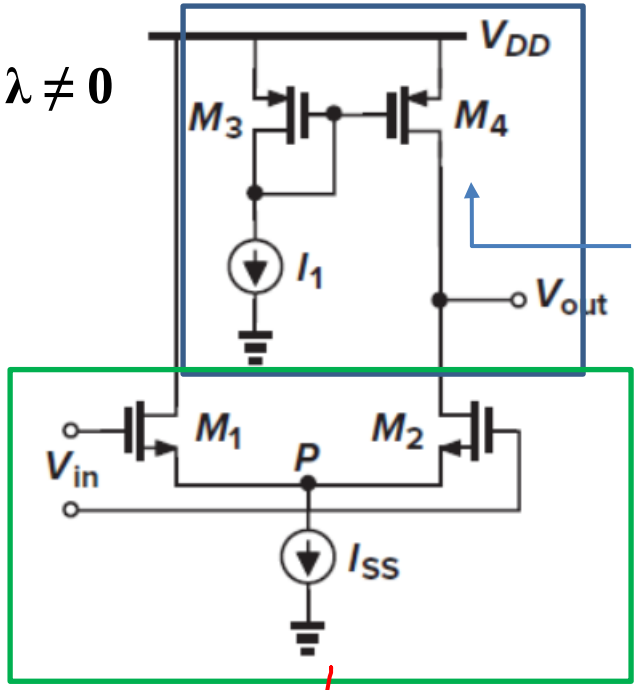
Recall: If a fully-symmetric differential pair senses differential inputs, then the concept of 'half circuit' can be applied.



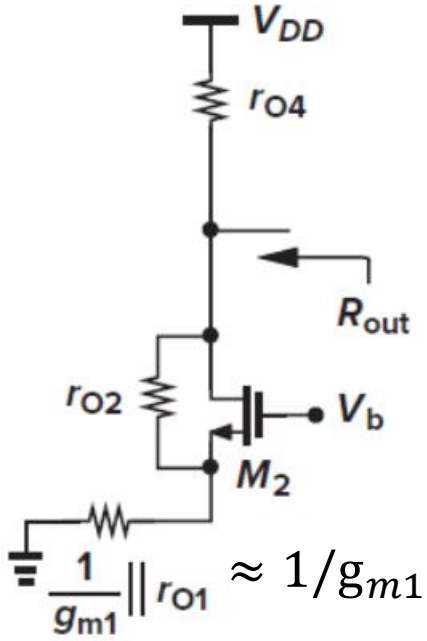
We can write $V_X/V_{in1} = -g_mR_D$ and $V_Y/(-V_{in1}) = -g_mR_D$. Thus, $\mathbf{(V_X - V_Y)/(2V_{in1}) = -g_mR_D}$.

(2) R_{out}

$\lambda \neq 0$



$R_{out4} = r_{o4}$



↳ CS stage with.

CS stage with a source degeneration (green box)

$\mathbf{R_{out}} = r_{o1} + R_S + (g_{m1} + g_{mb1})r_{o1}R_S$

From the small signal model,

R_{out4} (blue box) = r_{o4}

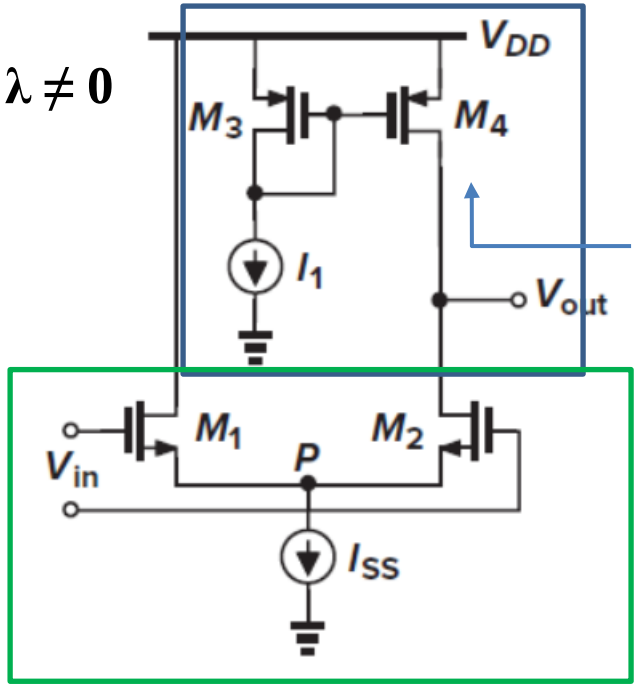
$R_{out1,2}$ (green box) = $\mathbf{r_{o2} + \frac{1}{g_{m1}} + \frac{g_{m2}r_{o2}}{g_{m1}}}$.

If M_1 and M_2 are symmetry, $g_{m1} = g_{m2}$, and thus, $\mathbf{R_{out1,2} = 2r_{o2} + \frac{1}{g_{m1}} \approx 2r_{o2}}$

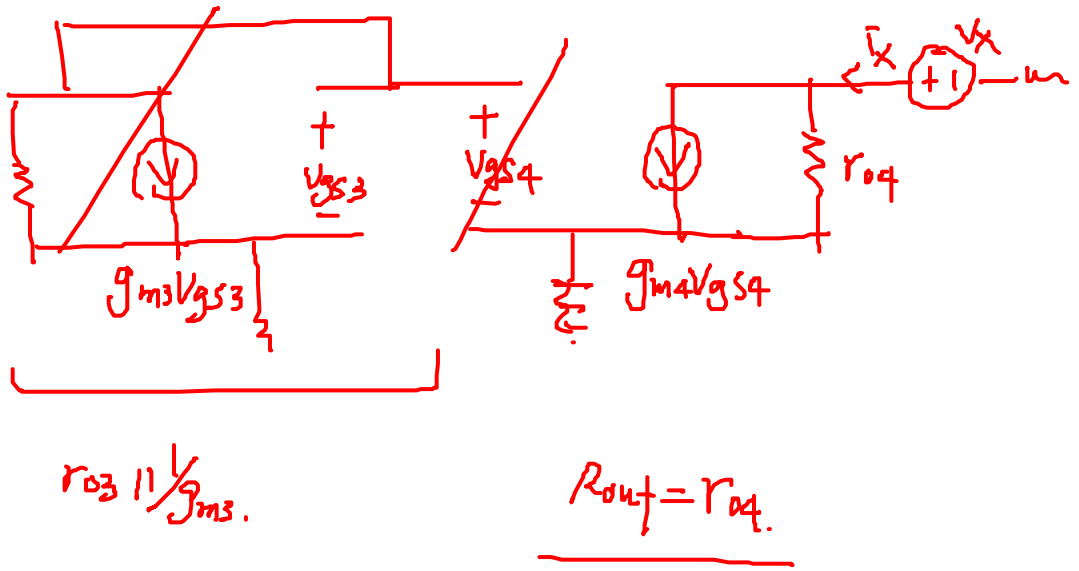
Finally, total $\mathbf{R_{out} = 2r_{o2} \parallel r_{o4}}$

(2) R_{out}

$\lambda \neq 0$



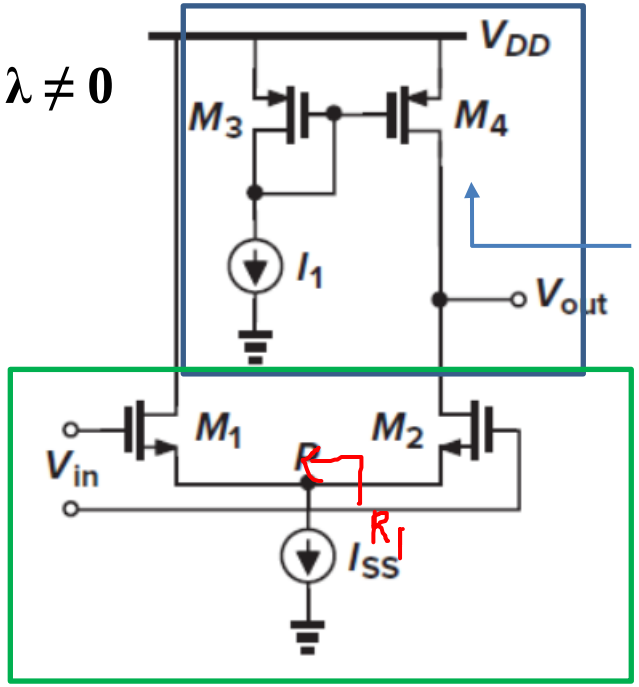
$R_{out4} = r_{o4}$



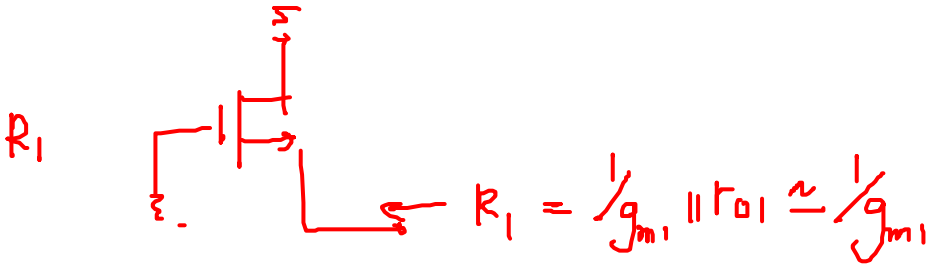
From the small signal model,
R_{out4} (blue box) = r_{o4}

(2) R_{out}

$\lambda \neq 0$



$\mathbf{R_{out4} = r_{o4}}$



$r_{o2} + \frac{1}{g_{m1}} + g_{m2} r_{o2} \frac{1}{g_{m1}}$.

CS stage with a source degeneration (green box)

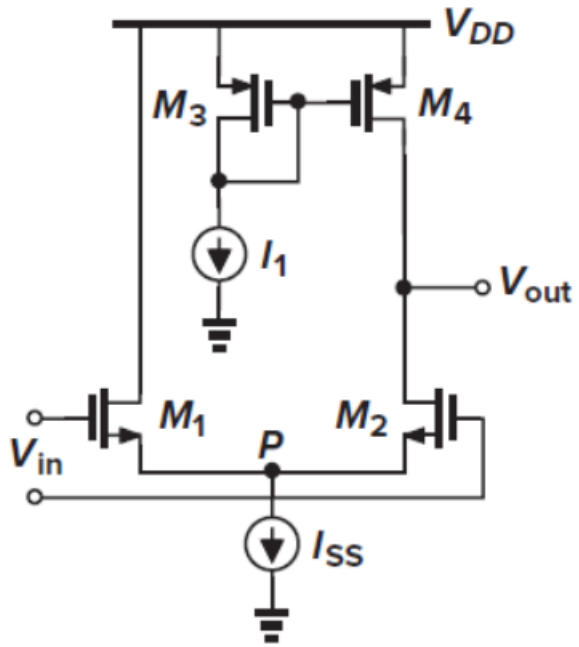
$\mathbf{R_{out}} = r_{o1} + R_S + (g_{m1} + g_{mb1}) r_{o1} R_S$

From the small signal model,

$R_{out1,2}$ (green box) = $\mathbf{r_{o2} + \frac{1}{g_{m1}} + \frac{g_{m2} r_{o2}}{g_{m1}}}$.

If M_1 and M_2 are symmetry, $g_{m1} = g_{m2}$, and thus, $\mathbf{R_{out1,2} = 2r_{o2} + \frac{1}{g_{m1}} \approx 2r_{o2}}$

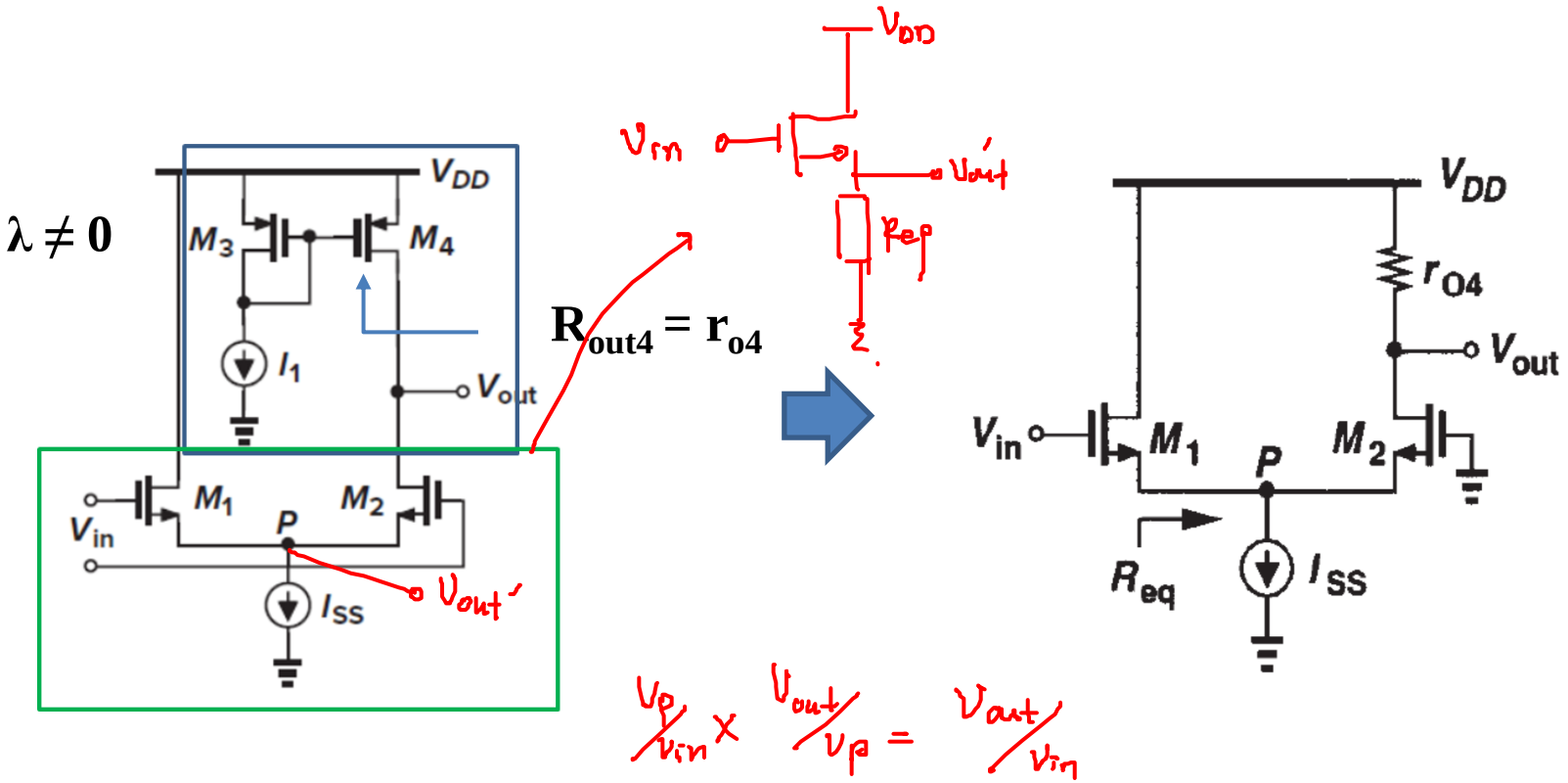
Finally, total $R_{out} = 2r_{o2} \| r_{o4}$



The gain of the circuit above is $|A_v| = G_m R_{out}$ where $\mathbf{|G_m| = {g_{m1}}/{2}}$

$\mathbf{R_{out} = 2r_{O2} \parallel r_{O4}}$

Approach 2

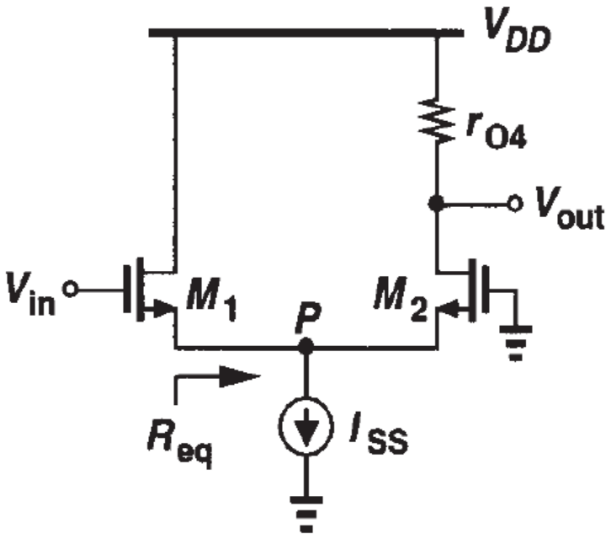


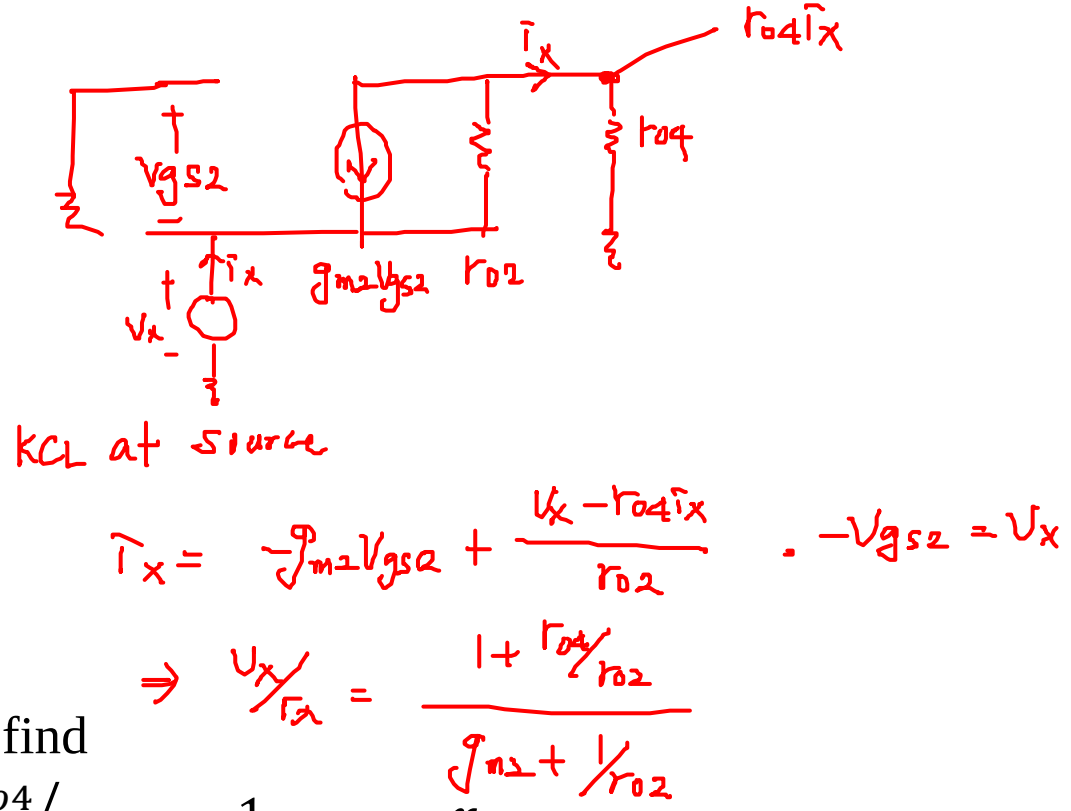
We also can get a gain by calculating $\mathbf{V_P/V_{in}}$ and $\mathbf{V_{out}/V_P}$ and multiply the results to obtain $\mathbf{V_{out}/V_{in}}$.

(1) $^{V_P}/_{V_{in}}$: M_1 as a source follower with $\mathbf{R_S}$ **of** $\mathbf{M_2}$ **(=** $\mathbf{R_{eq}}$**).**

*Gain of source follower = $\dfrac{g_m}{(g_m+g_{mb}+{}^1/_{r_{o1}}+{}^1/_{R_S})} \approx \dfrac{R_S}{({}^1/_{g_m}+R_S)}$

Thus, $^{V_P}/_{V_{in}} = \dfrac{R_{eq}}{({}^1/_{g_m}+R_{eq})}$



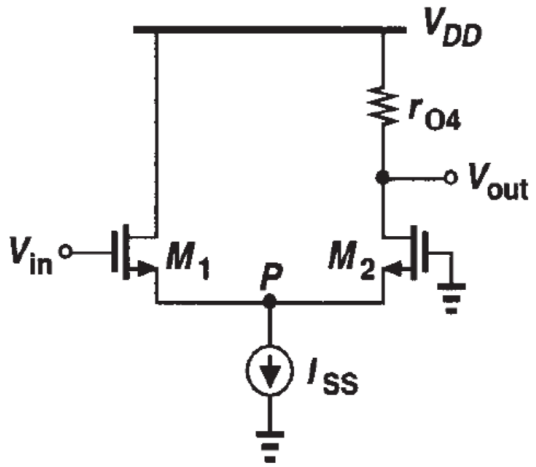


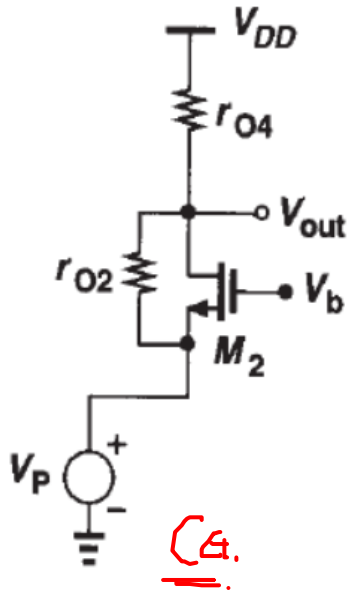
From the small signal analysis, we can find

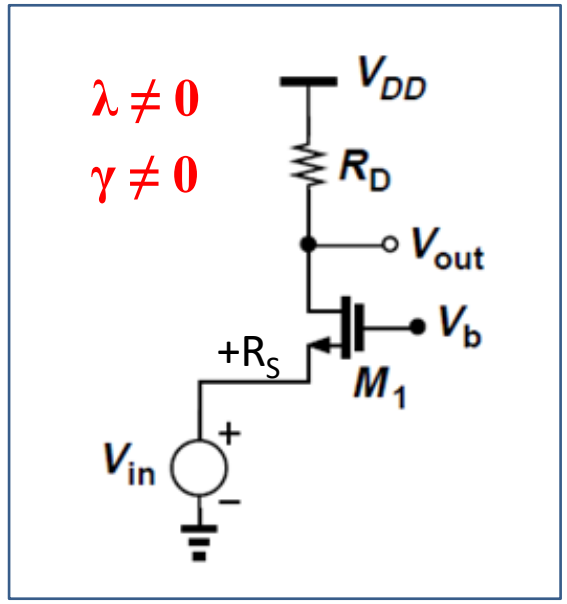
$$R_{eq} = \frac{1 + {r_{o4}}/{r_{o2}}}{g_{m2} + {1}/{r_{o2}}} \approx \frac{1}{g_{m2}} + \frac{r_{o4}}{g_{m2} \times 2r_{o2}}$$

Therefore, $\mathbf{V_P/V_{in}}$ becomes

$$\boldsymbol{V_P/V_{in}} \approx \frac{\mathbf{1} + {\boldsymbol{r_{o4}}/\boldsymbol{r_{o2}}}}{\mathbf{2} + {\boldsymbol{r_{o4}}/\boldsymbol{r_{o2}}}}$$





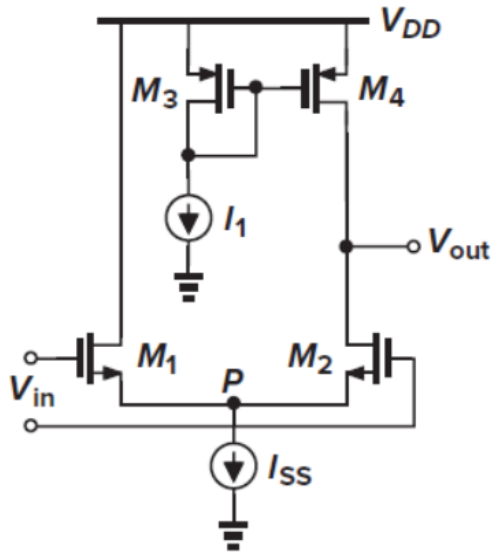


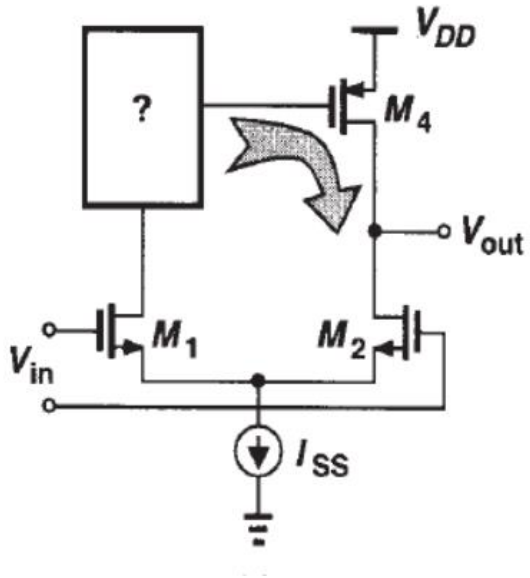
(2) V_{out}/V_p

Seen from the circuit, it is **a CG stage**.
The gain of CG stage ($\lambda \neq 0$ and $\gamma \neq 0$) is $A_v = \dfrac{(g_m + g_{mb})r_o R_D + R_D}{r_o + R_S + R_D + (g_m + g_{mb})r_o R_S}$

$R_S = 0$
$R_D = r_{O4}$
$r_O = r_{O2}$
$g_{mb} = 0$

Therefore, the gain of the circuit is $A_v = \dfrac{V_{out}}{V_P} = \dfrac{g_{m2}r_{o2}r_{o4} + r_{o4}}{r_{o2} + r_{o4}} = \dfrac{g_{m2}r_{o2} + 1}{r_{o2}/r_{o4} + 1} \approx \dfrac{g_{m2}r_{o2}}{1 + r_{o2}/r_{o4}}$



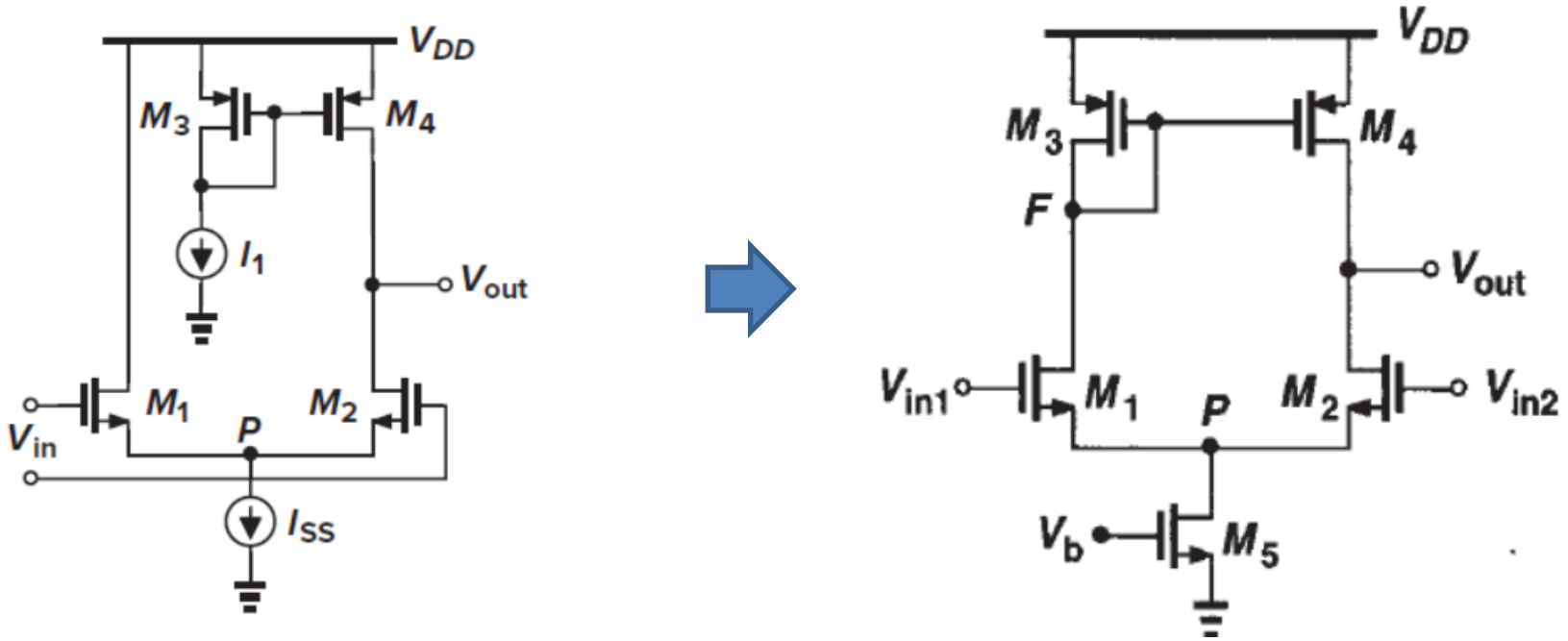


$$\boldsymbol{V_P/V_{in}} \approx \frac{1+{r_{o4}}/{r_{o2}}}{2+{r_{o4}}/{r_{o2}}} \; and \; \boldsymbol{V_{out}/V_P} \approx \frac{g_{m2}r_{o2}}{1+{r_{o2}}/{r_{o4}}}$$

Final gain of the active current mirror is

$$\frac{\boldsymbol{V_{out}}}{\boldsymbol{V_{in}}} = \frac{1+{r_{o4}}/{r_{o2}}}{2+{r_{o4}}/{r_{o2}}} \times \frac{g_{m2}r_{o2}}{1+{r_{o2}}/{r_{o4}}} = \frac{g_{m2}r_{o2}r_{o4}}{2r_{o2}+r_{o4}} = \frac{\boldsymbol{g_{m2}}}{\boldsymbol{2}}(\boldsymbol{2r_{o2}\|r_{o4}})$$

However, the current circuit topology waste the small-signal drain current of M_1

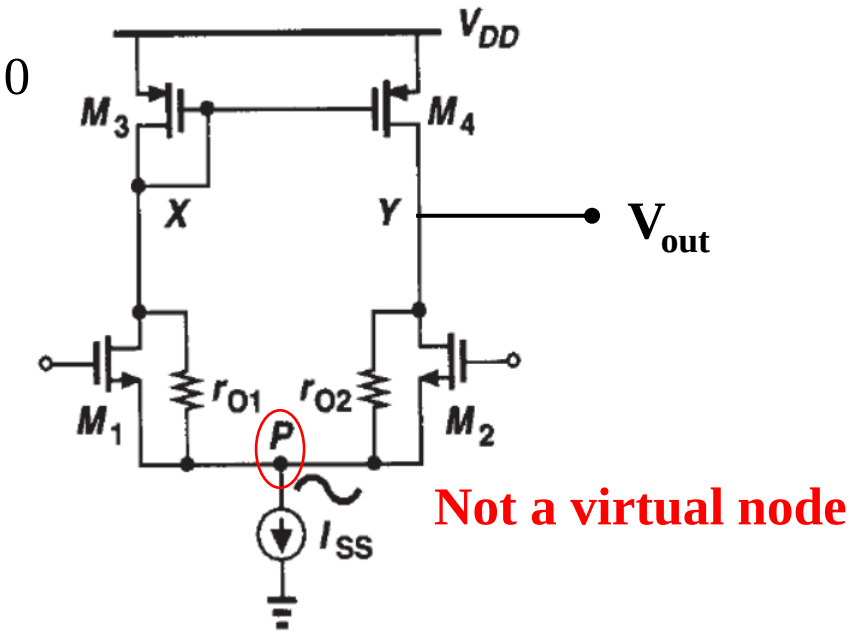


To fully utilize current of M_1, we modify the circuit from the left to the right one. The right design is called **a differential pair with active current mirror**, or **a differential pair with active load.**

A differential pair with active current mirror

Small Signal Analysis
(1) Differential Mode

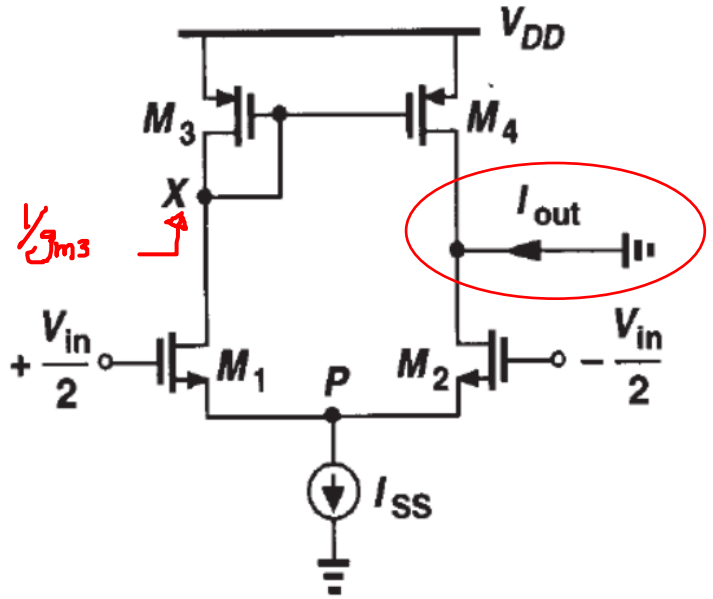
$\gamma = 0$



Not a virtual node

We cannot apply the half-circuit concept for this as M_3 yields a much lower voltage gain compared to M_4, resulting in **V_X and V_Y at node P do not cancel** each other.

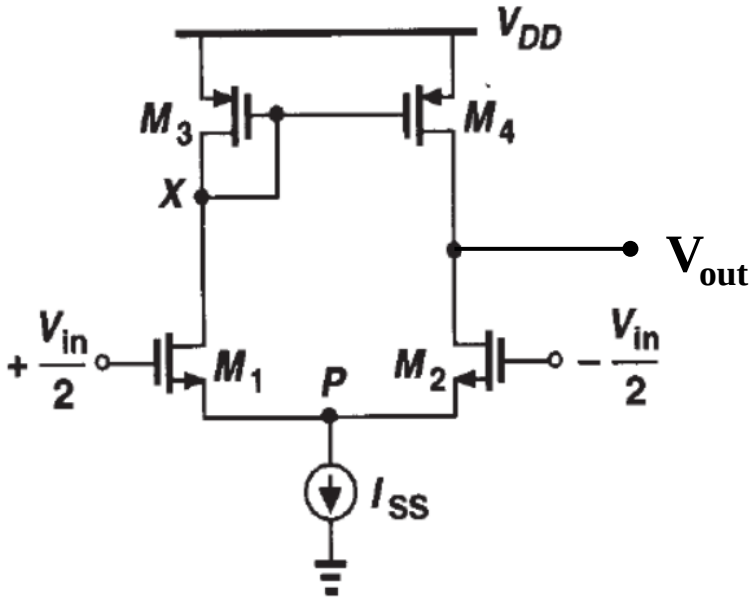
G_m and R_{out}

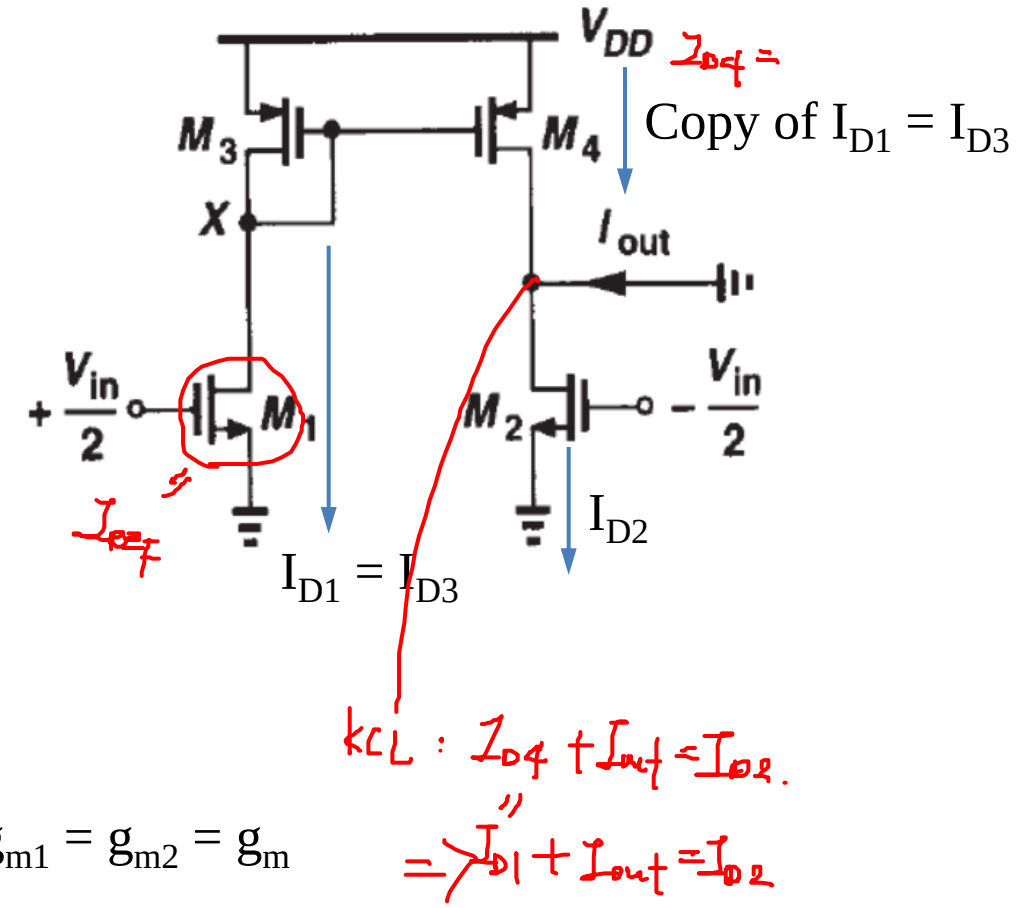


Grounded V_{out} makes the circuit almost symmetry, and thus we can apply a virtual ground concept.

R_{eq} of M_3 stage seen from node X is relatively small $\sim 1/g_{m3}$, and the gain of the diode connected MOS (M_3) is negligibly small (unity). Therefore, **node X can be viewed as ground**. This leads to the symmetry of the circuit, and thus we can apply **the virtual ground concept** at node P.

G_m



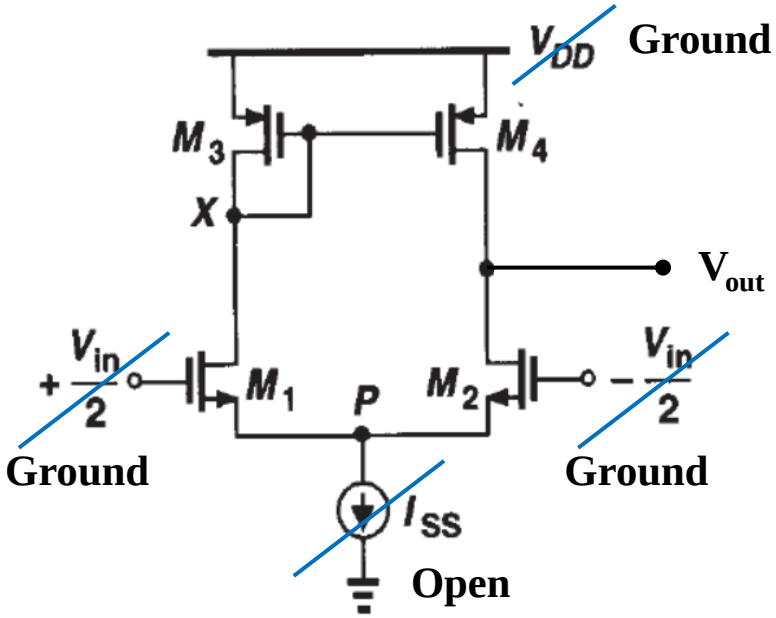


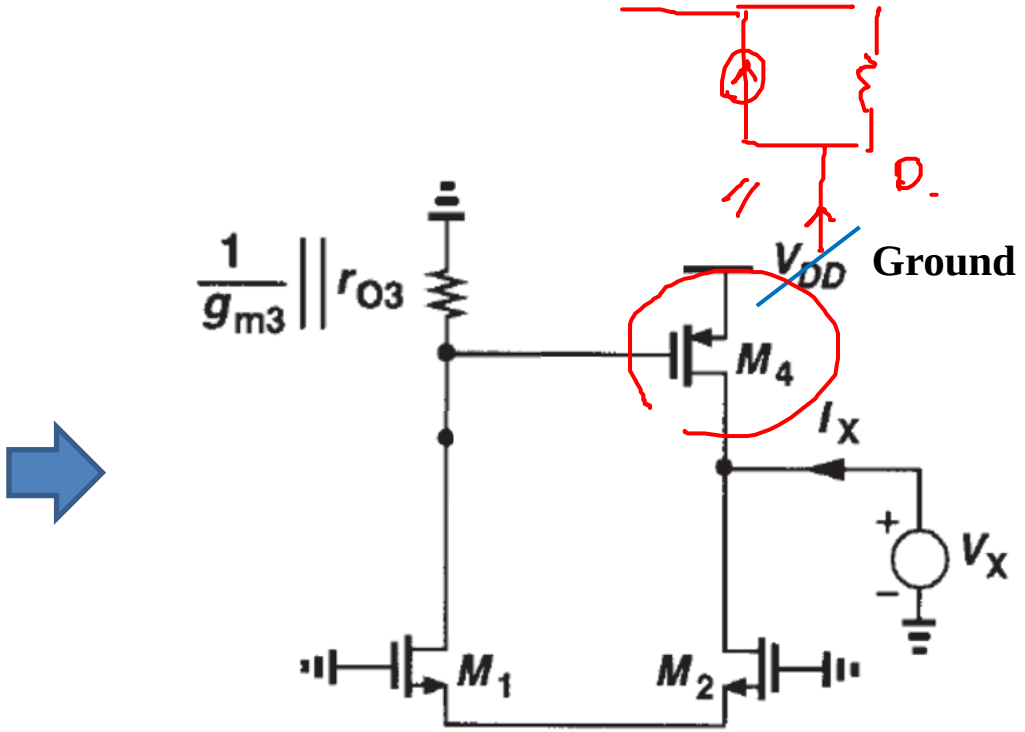
$I_{D1} = g_{m1}V_{in}/2$ and $I_{D2} = -g_{m2}V_{in}/2$ where $g_{m1} = g_{m2} = g_m$

$I_{out} = -g_m V_{in}$

Therefore, $|G_m| = g_m$

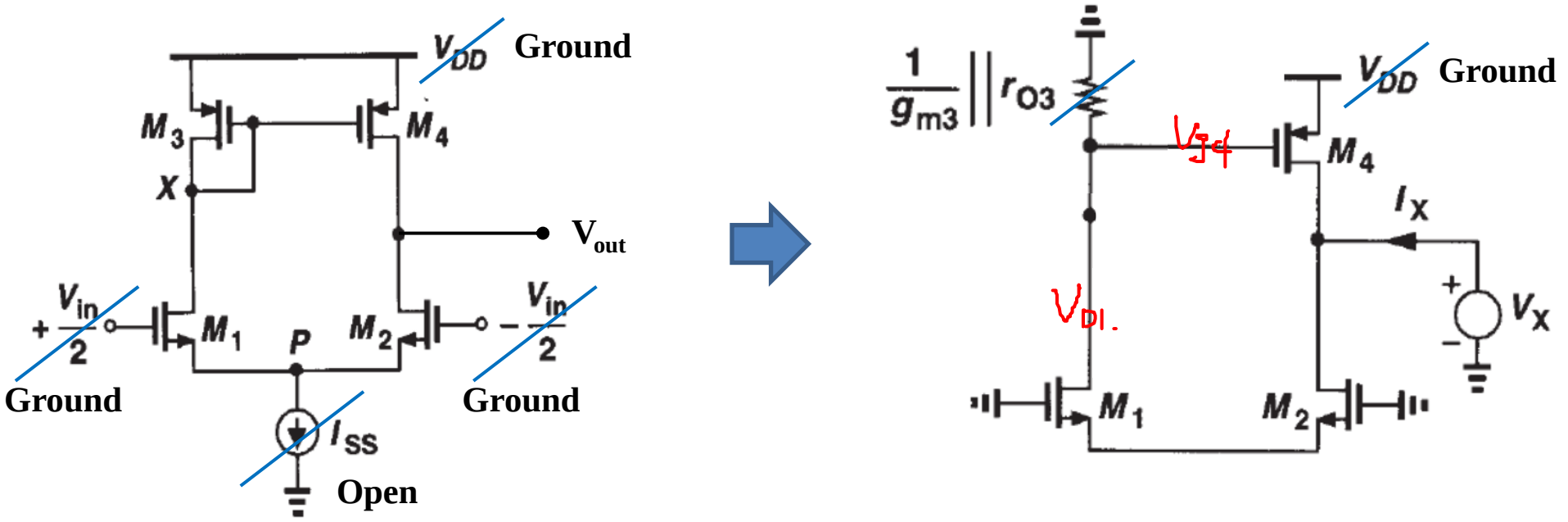
R_{out}





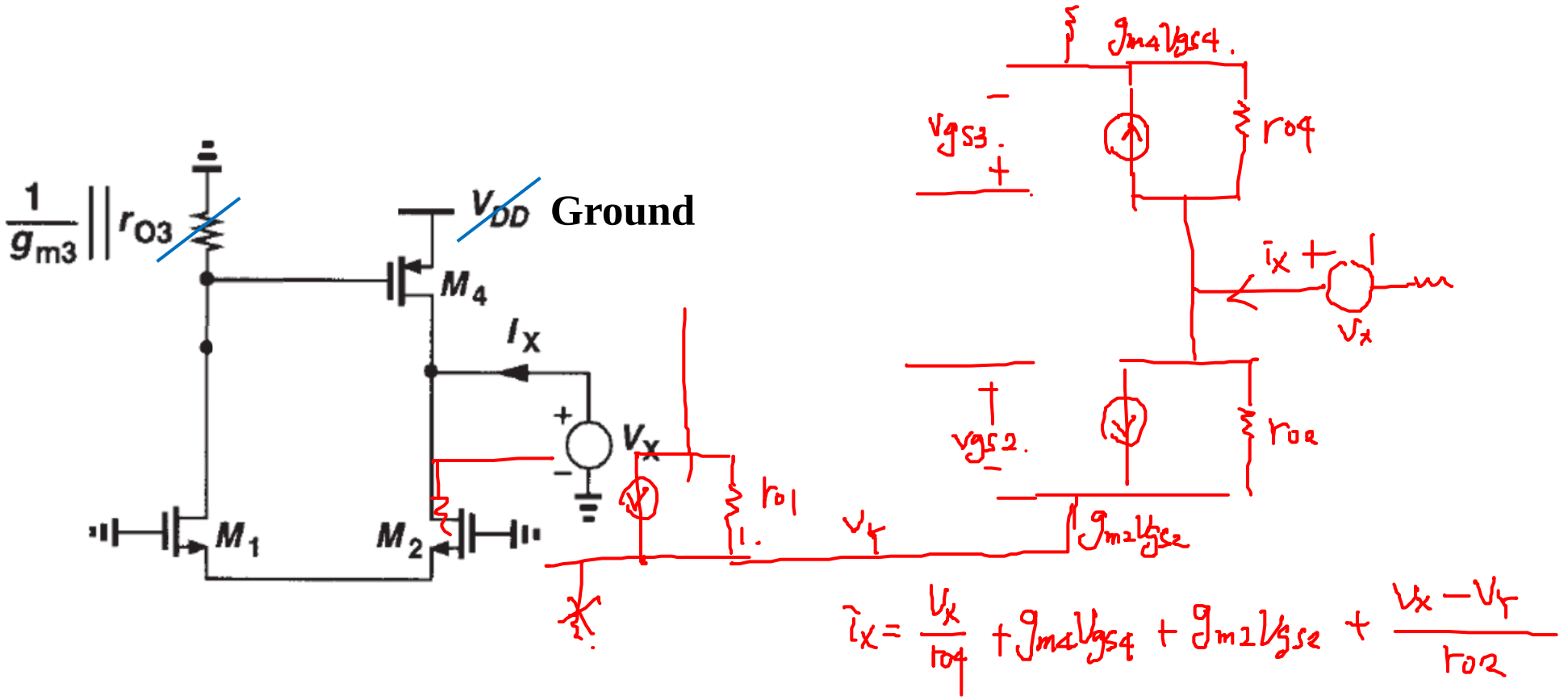
From a small signal model of the circuit on the right, $I_X = {}^{V_X}/_{r_{O4}} + g_{m4}V_{gs} + {}^{V_X}/_{r_{O2}} + g_{m2}V_{gs}$

Approximately, $V_{gs4} = 0$, and thus R_{eq} of $M_4 = r_{O4}$



From a small signal model of the circuit on the right, $I_X = {}^{V_X}/_{r_{O4}} + g_{m4}V_{gs} + {}^{V_X}/_{r_{O2}} + g_{m2}V_{gs}$

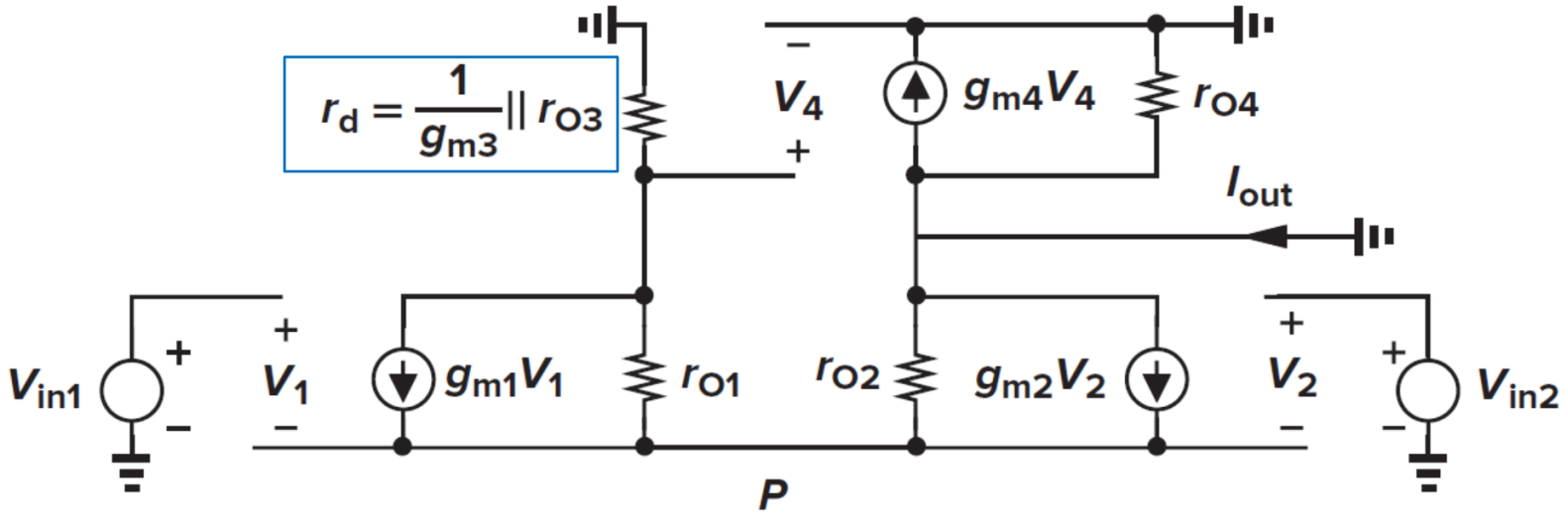
Approximately, $V_{gs4} = 0$, and thus R_{eq} of $M_4 = r_{O4}$



From small signal analysis, we get ${}^{V_X}/_{I_X} \sim r_{O4} \| 2r_{O2} \sim \boldsymbol{r_{O4} \| r_{O2}}$

Finally, gain of the active current mirror is $\mathbf{g_m(r_{O4} \| r_{O2})}$. If we compare this with the exact analysis we can see that there is slight mismatch due to too many approximations

Exact analysis

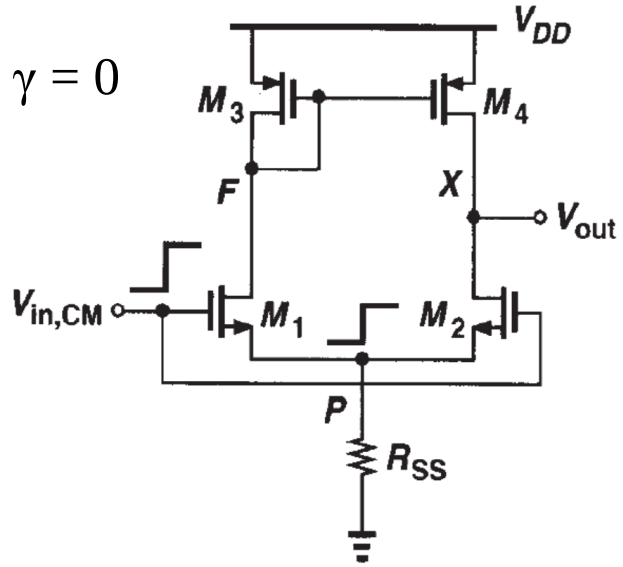


Another way is to find gain without approximation, i.e. exact analysis, using the small signal model above.

$$G_m = -g_{m1}r_{O1}\frac{g_{m4}r_d + 1}{r_d + 2r_{O1}} \qquad 1/R_{out} = \frac{(1 + g_{m4}r_d)r_{O4} + 2r_{O1} + r_d}{(2r_{O1} + r_d)r_{O4}}$$

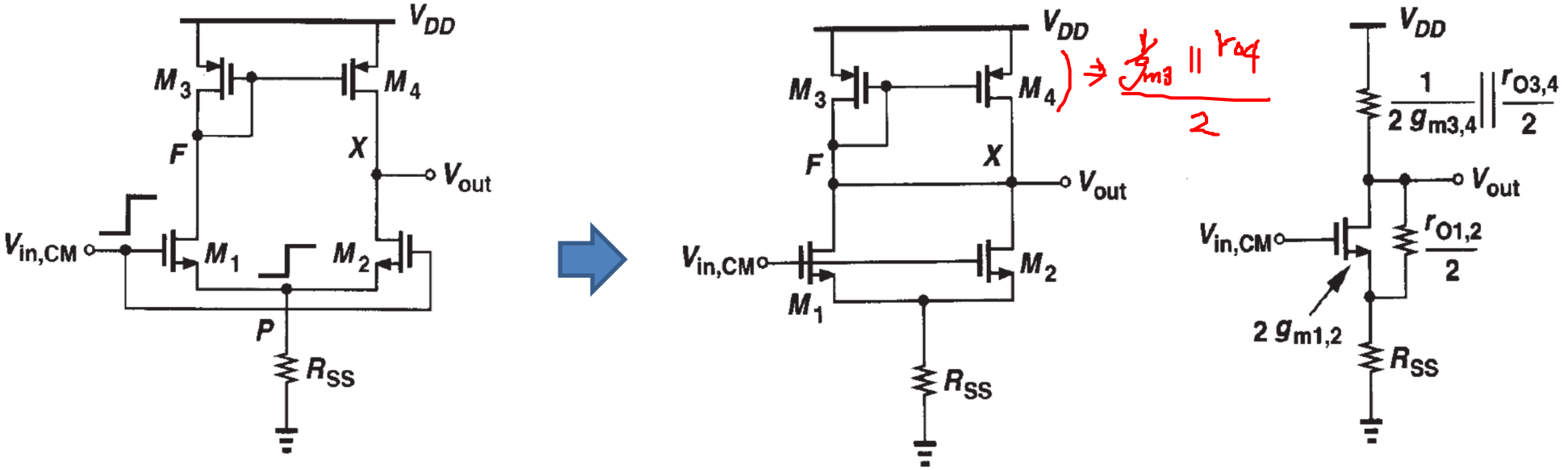
$$|A_v| = g_{m1}(r_{O1}||r_{O4})\frac{2g_{m4}r_{O4} + 1}{2(g_{m4}r_{O4} + 1)} \qquad r_{O1} = r_{O2}$$

Small Signal Analysis
(2) Common Mode



Due to a finite output impedance R_{SS}, a change in the input CM level leads to a change in the bias current of all of the transistors.

$$A_{CM} = \frac{\Delta V_{out}}{\Delta V_{in,CM}}$$



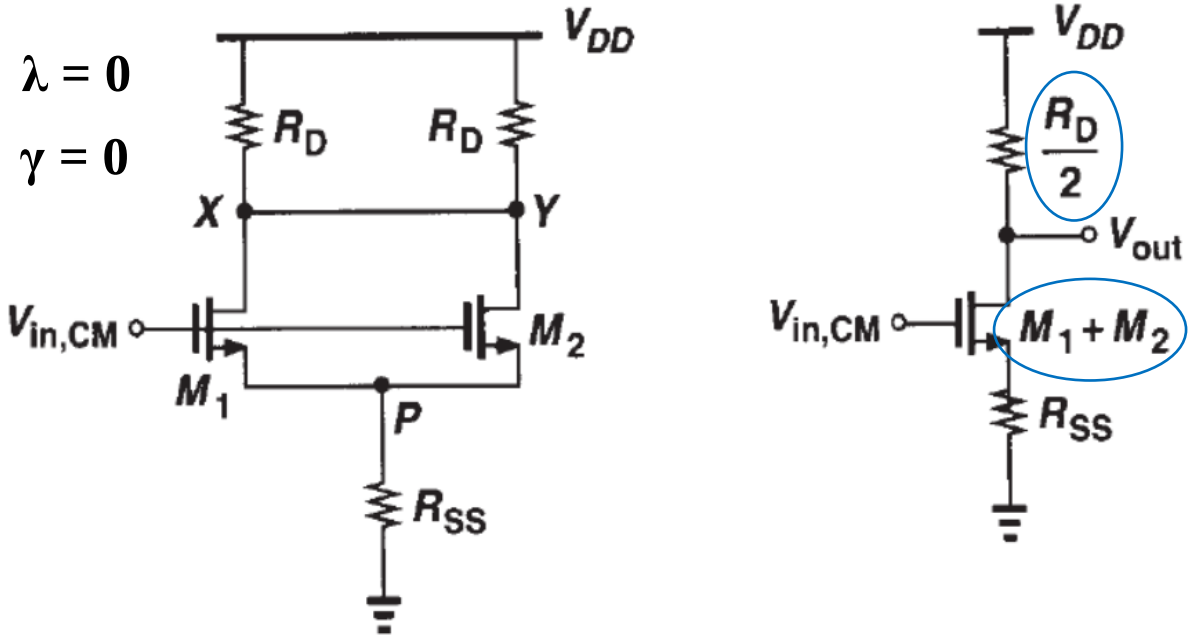
Parallel MOS

Resistance/2

Transconductance*2

Due to the properties of the common level input, changes in $V_{in,CM}$ influences both node F and V_{out}. E.g. If $V_{in,CM}$ increases, V_F decreases and so does V_{out} (CS stage). Thus, F and X can be shorted. Then, we can apply **a parallel MOSFET concept** to analyze the circuit.

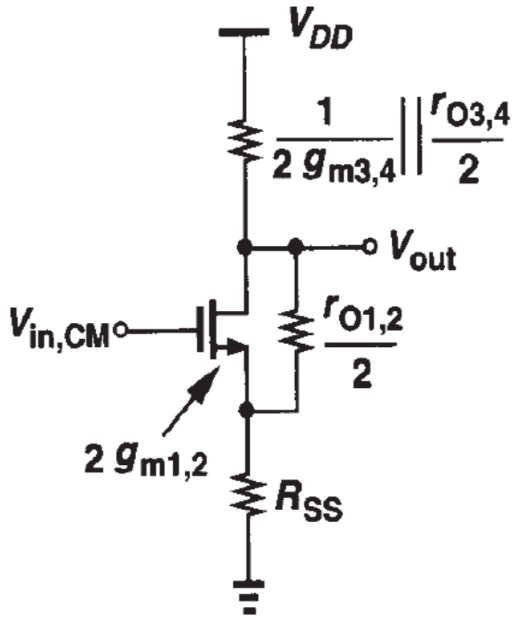
Recall:



If the circuit is symmetric, V_X remains equal to V_Y. Thus, we can view the circuit as two parallel transistor circuits.

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \times 2$$ and the same for the transconductance $\mathbf{g_m \times 2}$

From small-signal model, we get $A_{v,CM} = -\frac{R_D/2}{1/2 g_m + R_{SS}}$



R_{eq} of $M_3 = {}^{1}/_{g_{m3}} \| r_{o3} \sim {}^{\mathbf{1}}/_{\mathbf{g_{m3}}}$

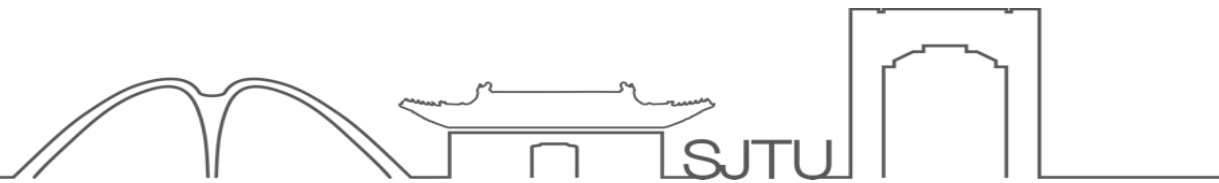
R_{eq} of $M_4 = r_{o4}$

As $A_{v,CM} = -\frac{{}^{R_D}/_2}{{}^{1}/_{2g_m} + R_{SS}}$, the circuit above has $A_{v,CM} \approx -\frac{\frac{1}{2g_{m3,4}} \| {}^{r_{o3,4}}/_2}{{}^{1}/_{2g_{m1,2}} + R_{SS}} = -\frac{1}{1+2g_{m1,2}R_{SS}} \frac{g_{m1,2}}{g_{m3,4}}$

by assuming that $\frac{1}{2g_{m3,4}} \ll r_{o3,4}$ and neglect the effect of ${}^{r_{o1,2}}/_2$

$$\boldsymbol{CMRR} = \left|\frac{A_{DM}}{A_{CM}}\right| = \frac{g_{m1,2}(r_{o1,2} \| r_{o3,4})}{\left(\frac{1}{1+2g_{m1,2}R_{SS}} \frac{g_{m1,2}}{g_{m3,4}}\right)} = (1+2g_{m1,2}R_{SS}) g_{m3,4} (r_{o1,2} \| r_{o3,4})$$

THE END

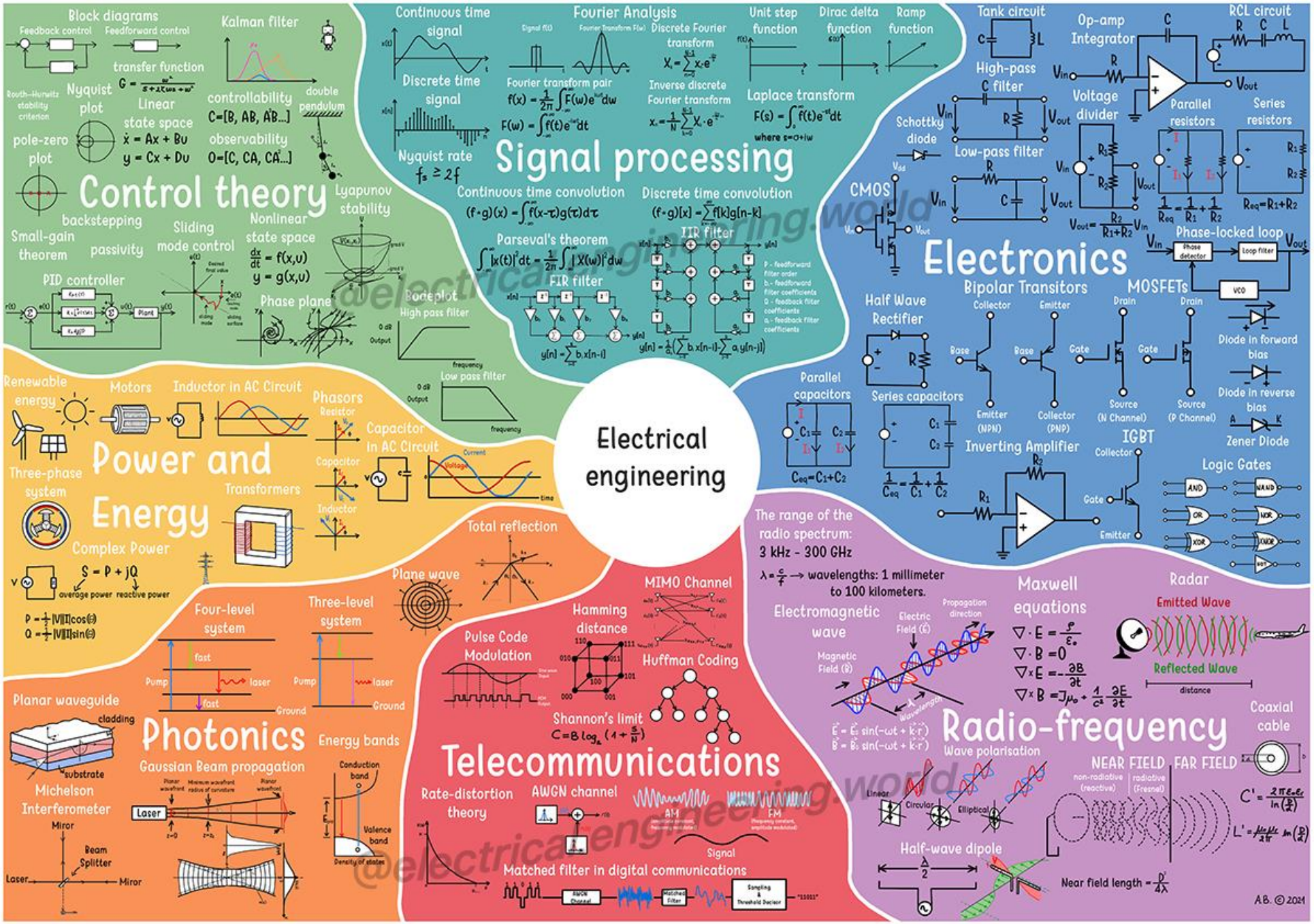


What we have learned in ECE3110J/VE311

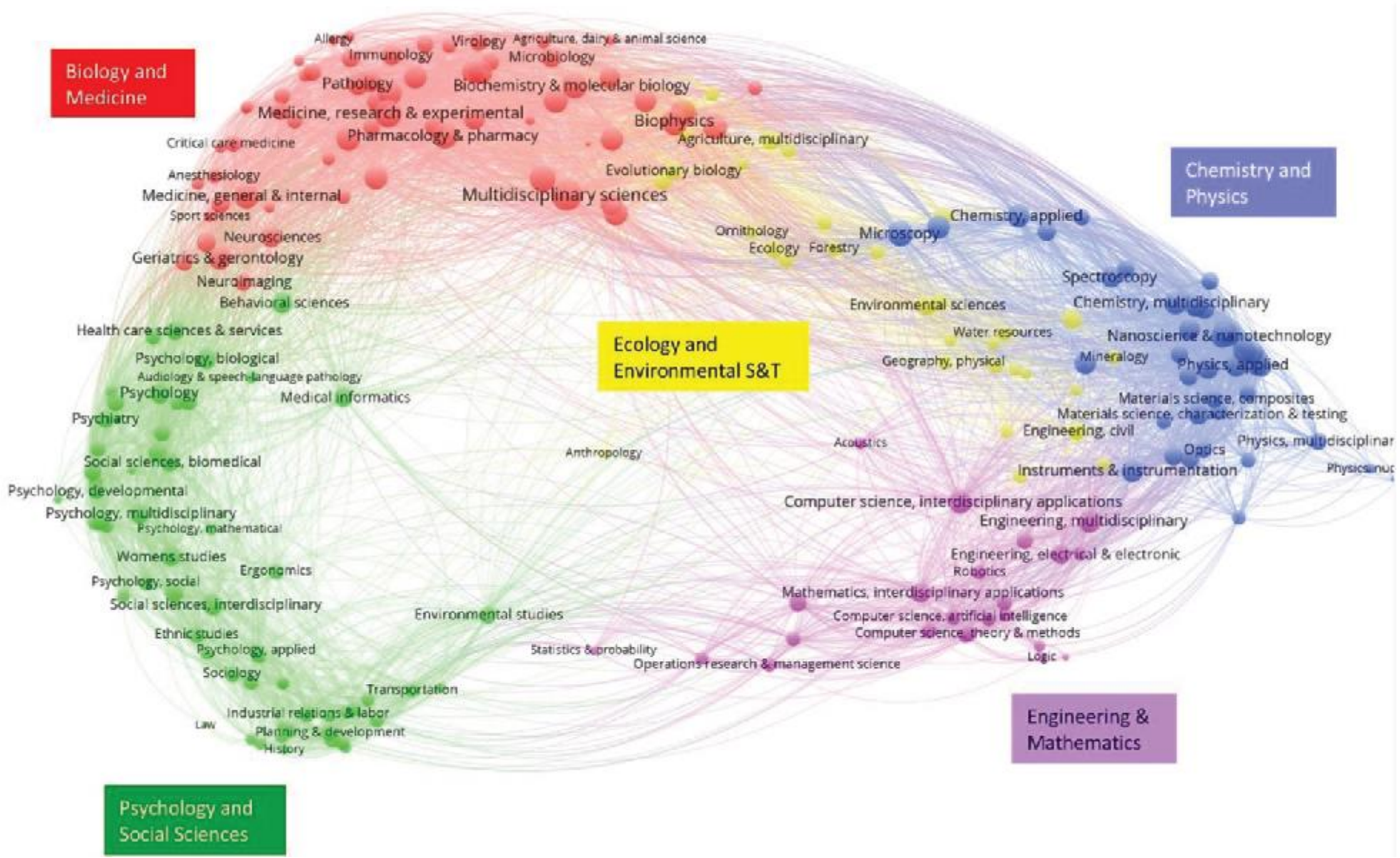
1. Introduction and Solid-State Electronics
2. Diode and Diode Circuit
3. Bipolar Junction Transistor (BJT)
4. BJT Circuit
5. Basic MOS Device Physics
6. MOS Single Stage Amplifier
7. MOS Differential Amplifier
8. Current Mirror

Field of EE

$\frac{E}{CS}$ +

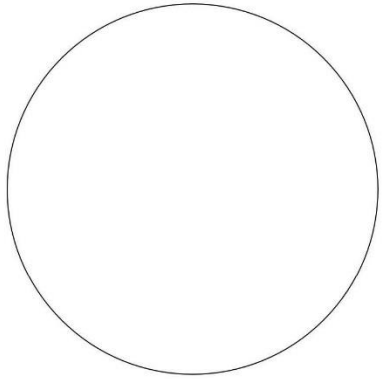


Interdisciplinary studies

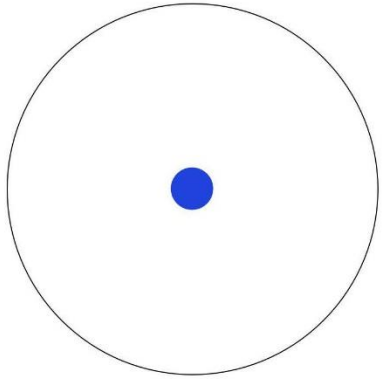


Studying one subject is..

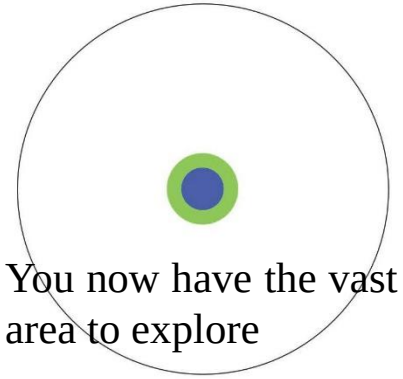
All the knowledges



By the time you finish elementary school, you know a litt

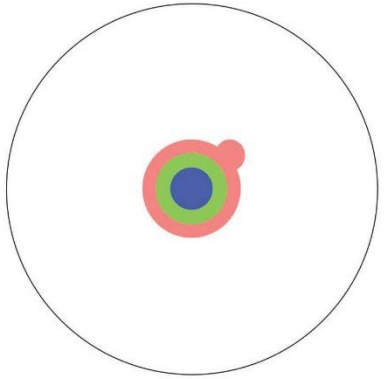


By the time you finish high school, you know a bit more:

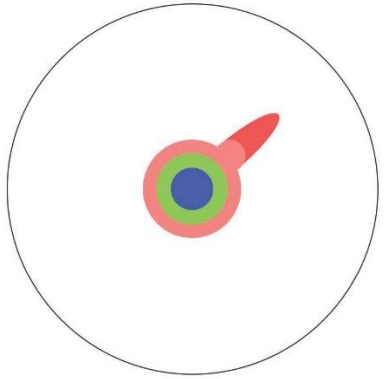


You now have the vast area to explore

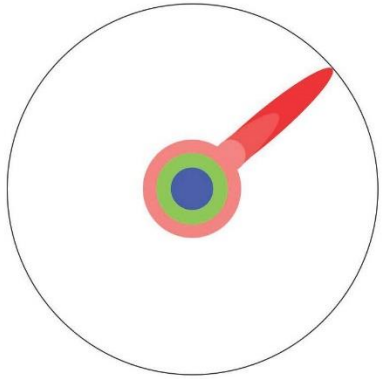
With a bachelor's degree, you gain a specialty:



A master's degree deepens that specialty:

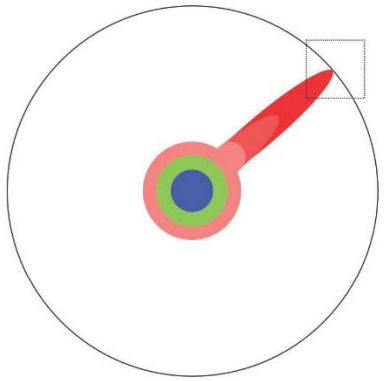


Reading research papers takes you to the edge of human knowledge:

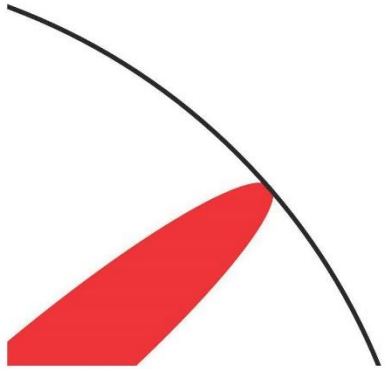


Once you're at the boundary, you focus:

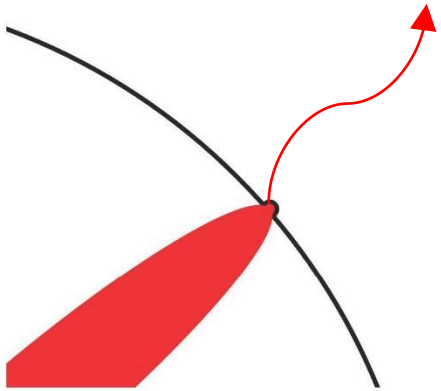
Enlarged the total knowledge for human beings,
meaning that we keep expanding our knowledges.



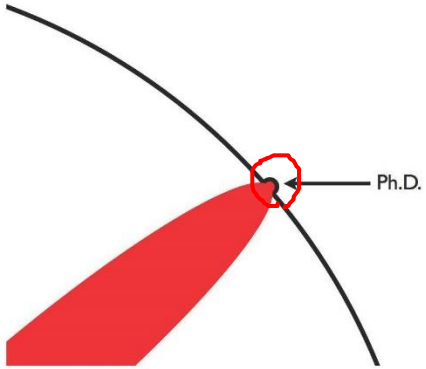
You push at the boundary for a few years:



Until one day, the boundary gives way:

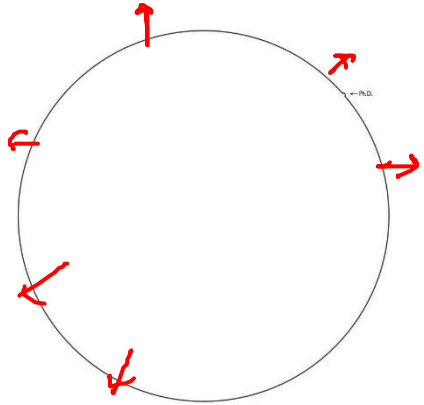


And, that dent you've made is called a Ph.D.:



Of course, the world looks different to you now:

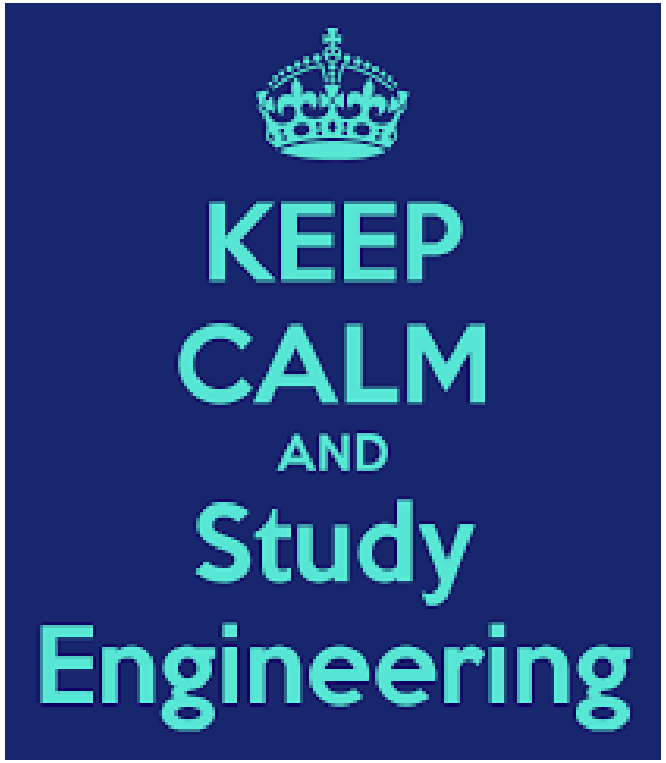
So, don't forget the bigger picture:



Keep pushing.

He who has dreamed for a long resembles his dream.

Andre Malraux



Learning is life-long a process.
Please don’t be anxious and impatient if you think you are slow.