JOINT INSTITUTE
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ECE3110J/VE311 Electronic Circuits

Mid-term Summary

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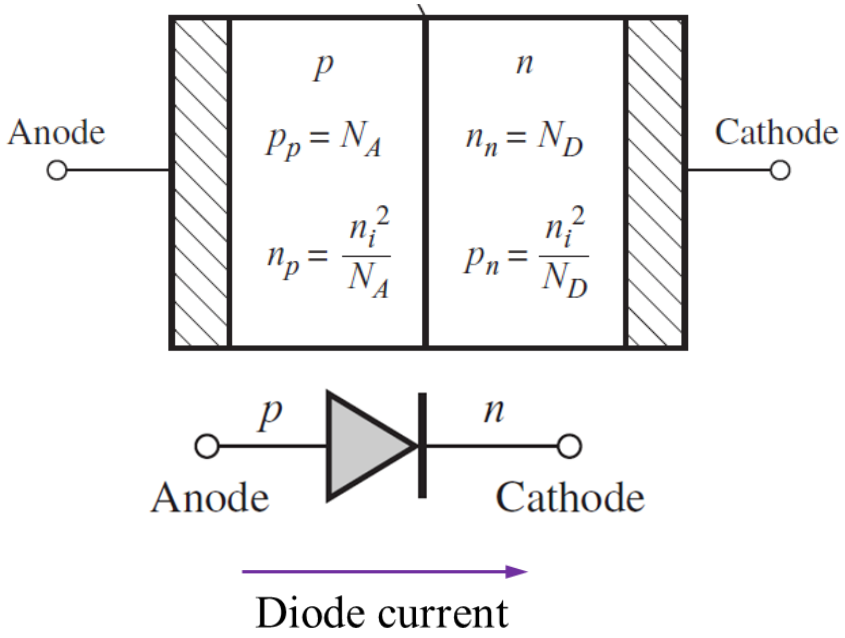
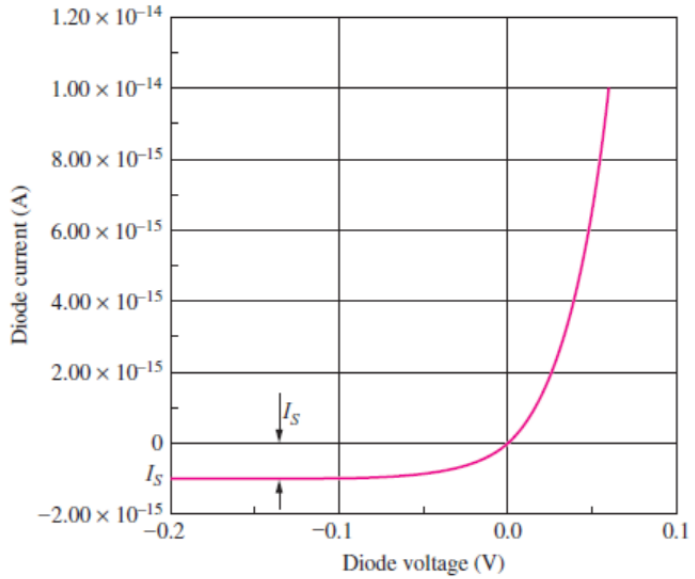
PN Junction Diode

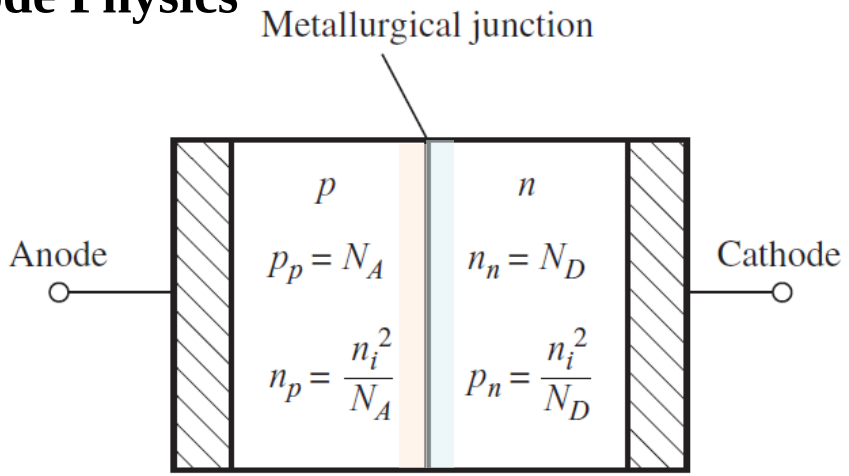
The pn junction diode is formed by fabrication of a p-type semiconductor region in intimate contact with an n-type semiconductor region.

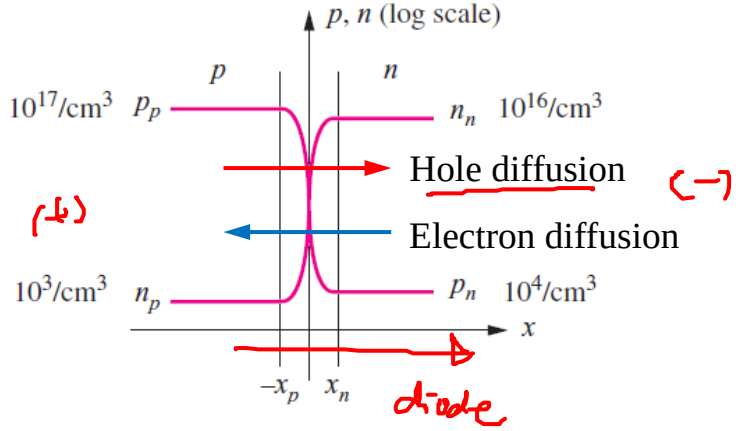


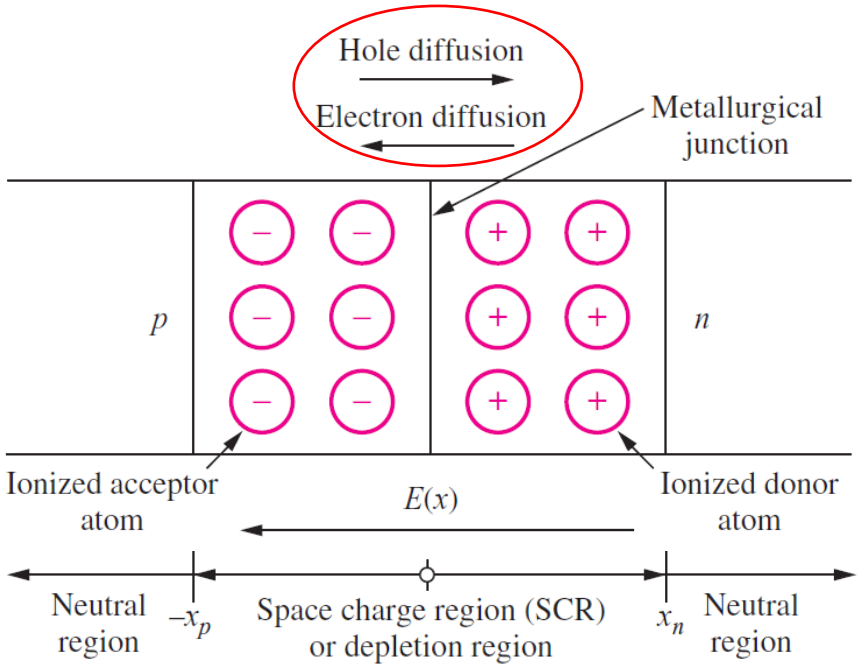


Non-linear, or rectifying, behavior

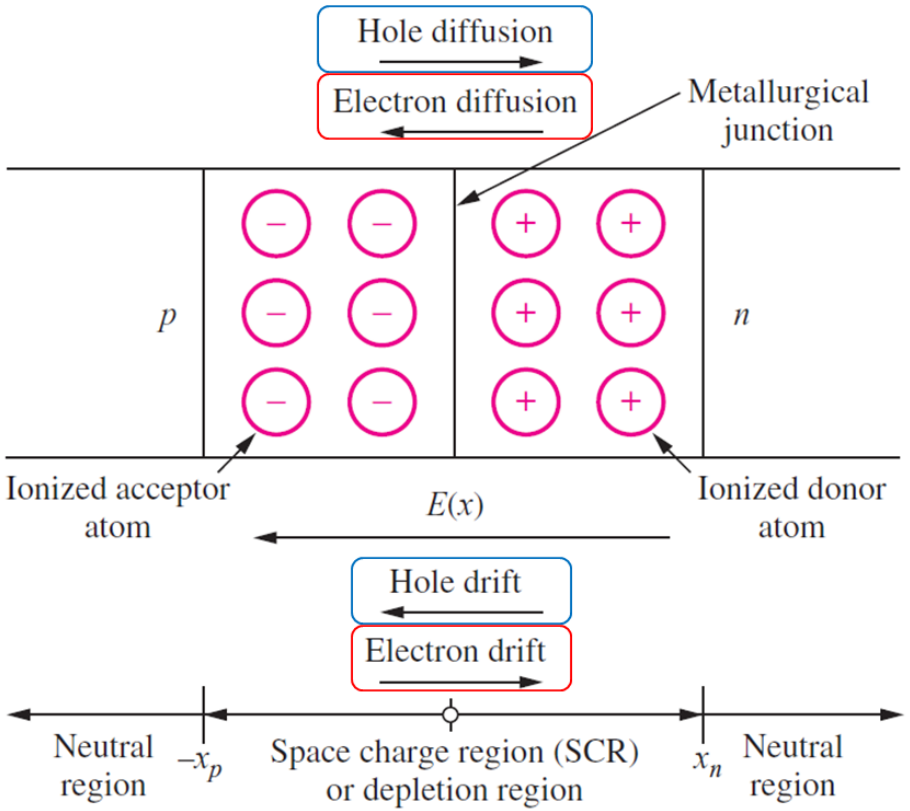
PN diode Physics





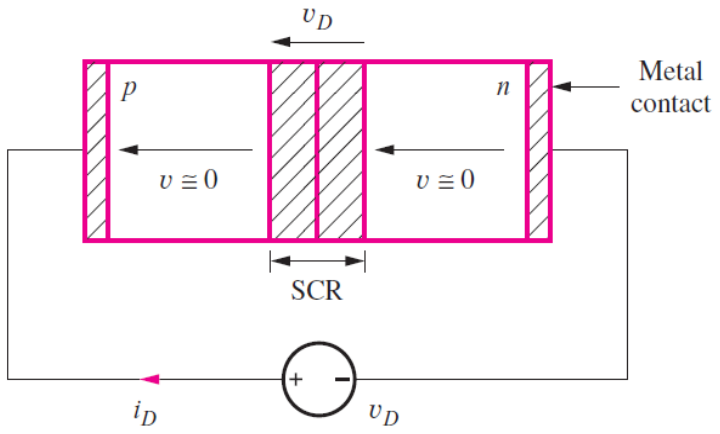


As a result of the diffusion of charges, immobile ionized charges (atoms) are revealed, generating an electric field, or **built-in potential**.

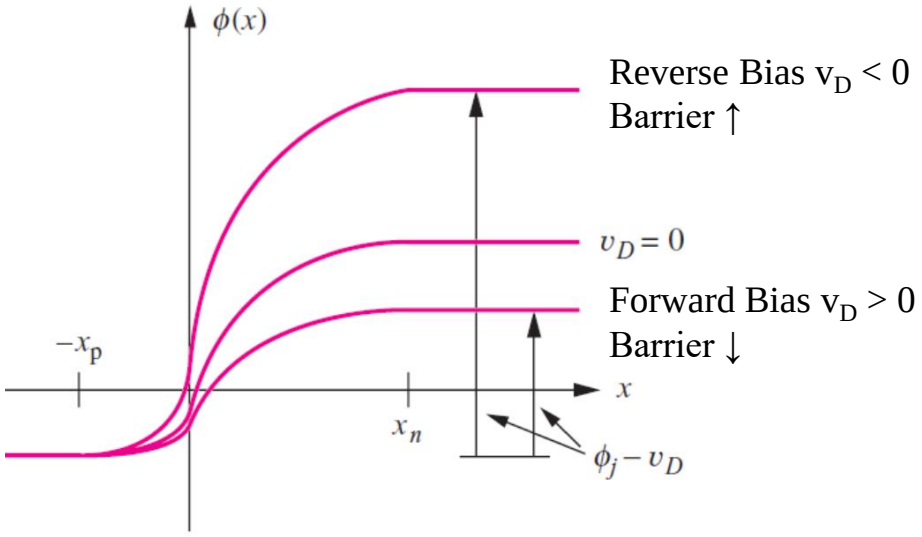


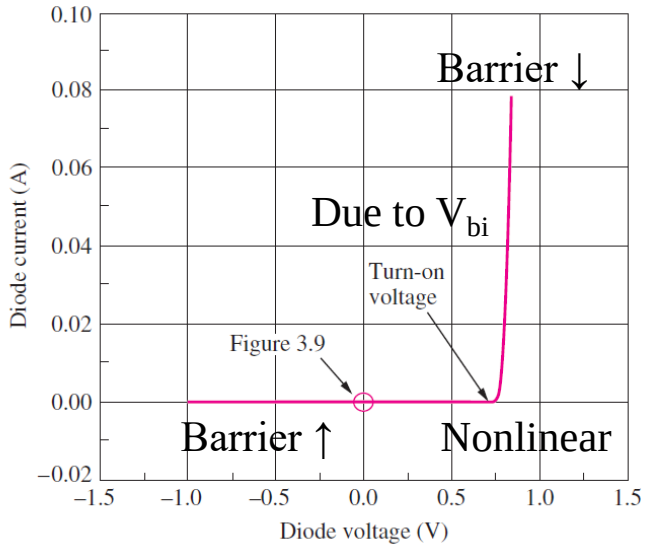
The carriers **drift in directions opposite the diffusion** of the same carrier species. Because the terminal currents must be zero, **a dynamic equilibrium** is established in the junction region. Hole diffusion is precisely balanced by hole drift, and electron diffusion is exactly balanced by electron drift.

I-V Characteristics of Diode



Under Bias (Non Equilibrium)



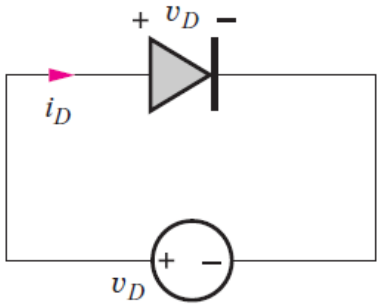


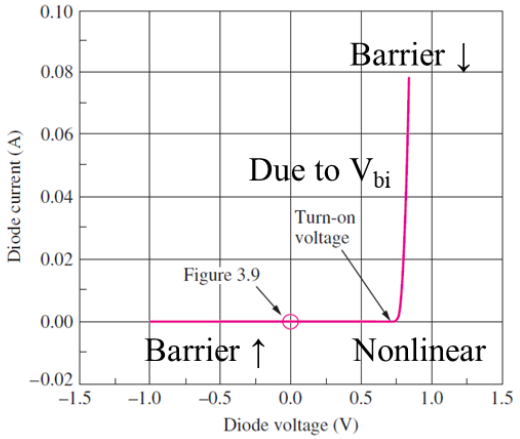
The diode permits **current to flow in one direction in a circuit**, but prevents movement of current in the opposite direction **due to the barrier, or built-in potential**. We will find that this nonlinear behavior has many useful applications in electronic circuit design.

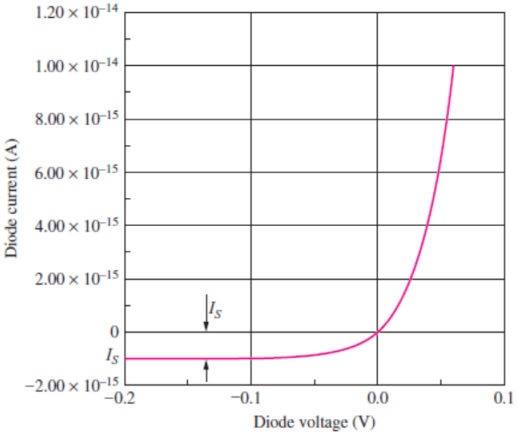
- Turn-on voltage typically 0.5 to 0.7 V
- Saturation current (I_S) typically 10^{-18} to 10^{-9} A
- kT/q = 0.025875 V at 300 K

Diode Equation and Diode Under Bias

Forward bias, i.e. $v_D > 0$, **diode is on**: Current flows from P to N
Reverse bias, i.e. $v_D < 0$, **diode is off**: Current does not flow, but saturation current exists







The total current through the diode is i_D, and the voltage drop across the diode terminals is v_D.

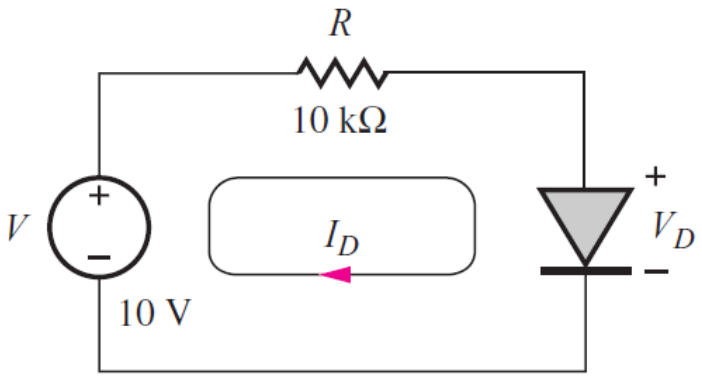
$\mathbf{I_D = I_S\left(e^{\frac{qV_d}{kT}} - 1\right)}$ $\boldsymbol{or}$ $\boldsymbol{I_S(e^{v_D/V_T} - 1)}$ where k is Boltzmann's constant.

e.g. v_D = 1 V, $i_D = I_S\left(e^{v_D/V_T} - 1\right) = I_S\left(e^{1/0.025} - 1\right)$

e.g. v_D = -1 V, $i_D = I_S\left(e^{v_D/V_T} - 1\right) = I_S\left(e^{-1/0.025} - 1\right) = I_S * (-1) \approx -I_S$

Diode Circuit Analysis

One common objective of diode circuit analysis is to find the **quiescent operating point** (Q-point), or **bias point,** for the diode. The Q-point consists of the dc current and voltage (I_D, V_D) that define the point of operation on the diode's *i*-*v* characteristic.



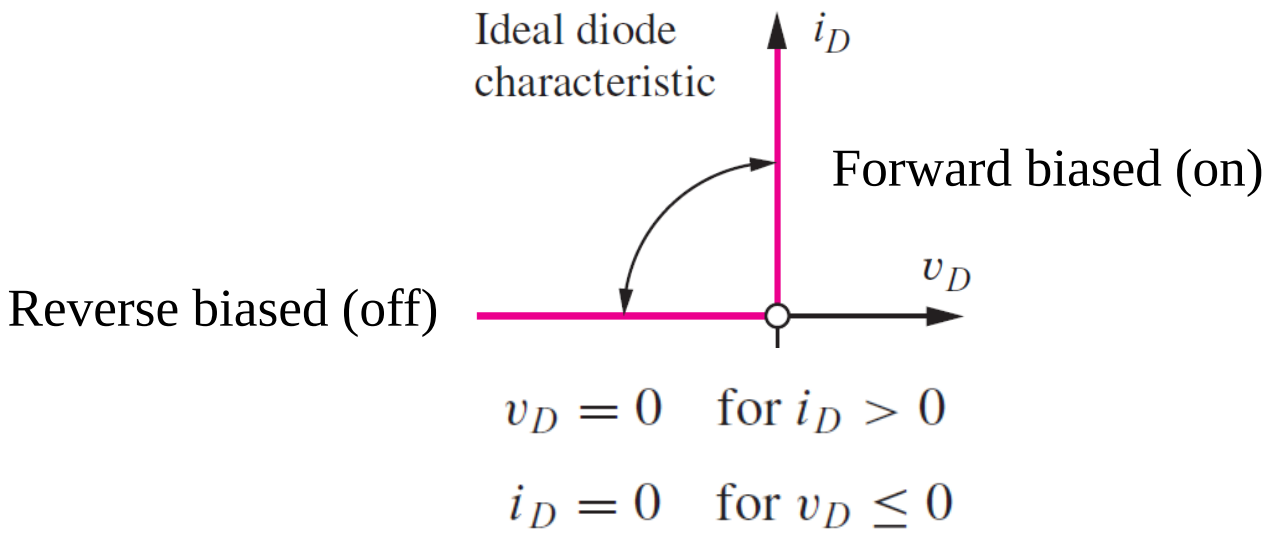
$V = I_D R + V_D$

$I_D = ?$

$V_D = ?$

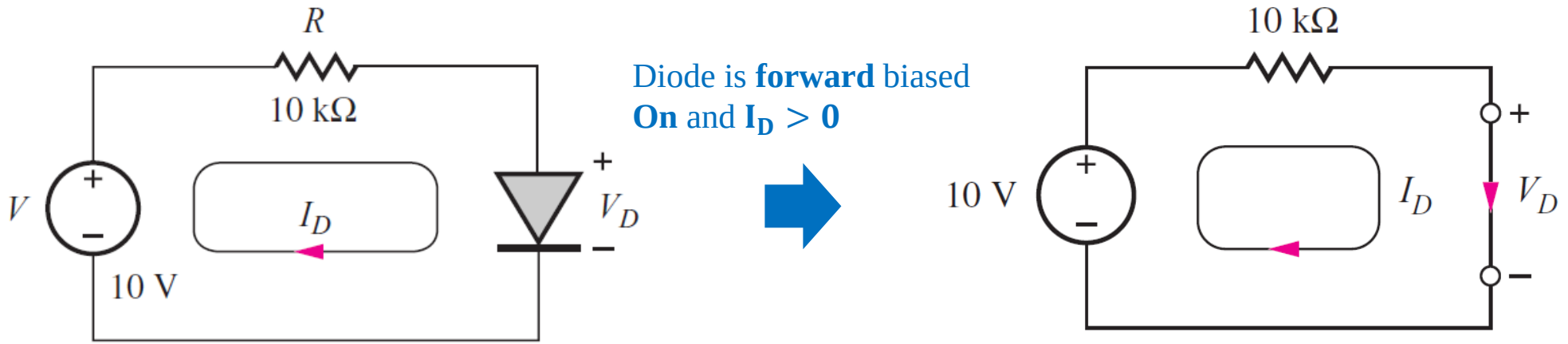
1. **Graphical analysis**
2. **Mathematical analysis**
3. **Simplified analysis** (ideal diode)
4. **Simplified analysis** (constant voltage drop)

Simplified Analysis (Ideal Diode)



Though the diode i-v curve is not linear we can use **piecewise linear** approximations for the diode i-v characterization. The **ideal diode model** is the simplest model for the diode. The *i-v* characteristic for the **ideal diode consists of two straight-line segments.**

(1) Forward bias

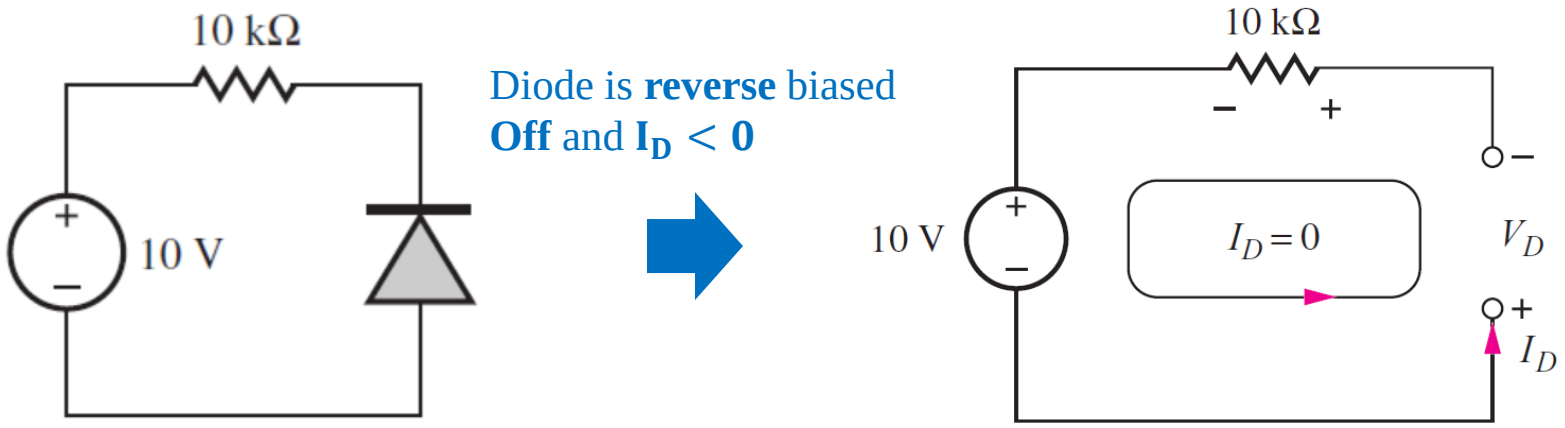


Based on the ideal diode model, we can find that the diode is forward biased and operating with a current of 1 mA as follows.

$$I_D = \frac{10\ V}{10k\Omega} = 1\ mA$$

Q-point is 0 V and 1 mA.

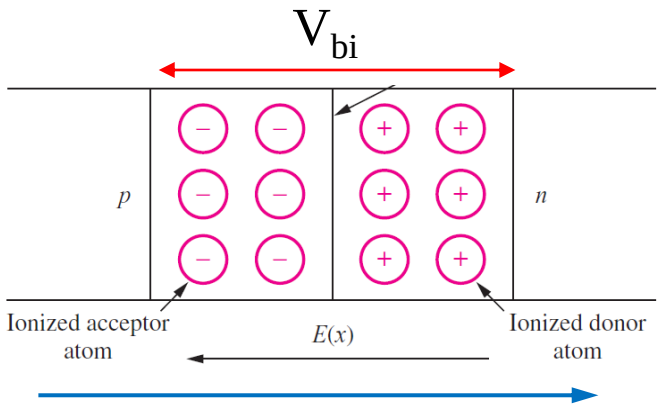
(2) Reverse bias

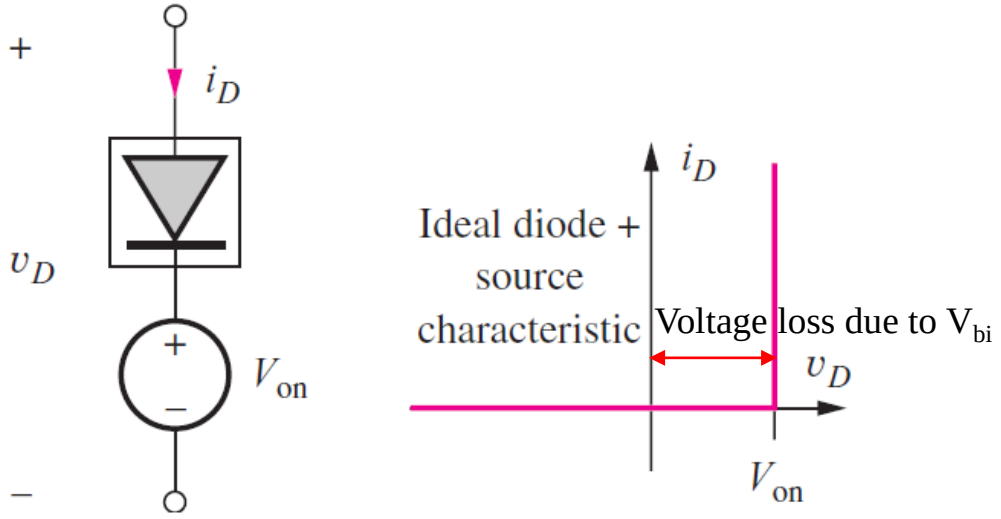


As the diode is off, the circuit is open.
$I_D = 0$ and $V_D = -10$ V

Q-point is -10 V and 0 A.

Simplified Analysis (Constant Voltage Drop)

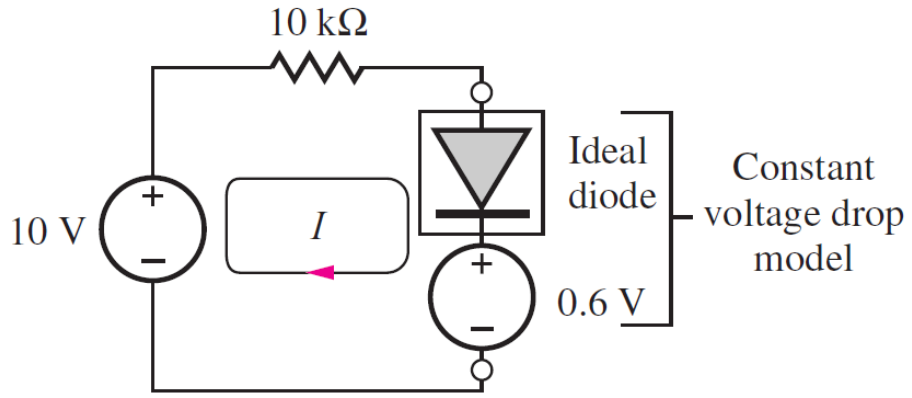


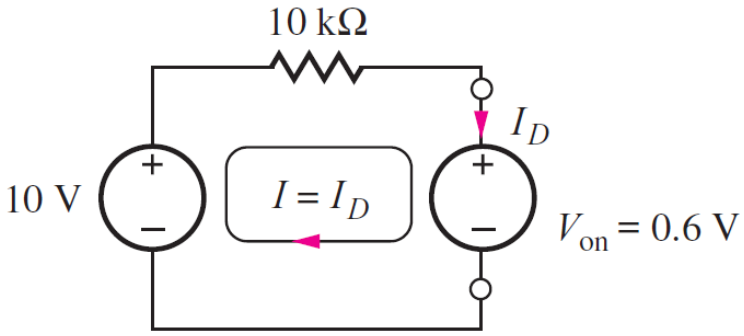


Voltage required to turn on the diode

The diode current flows when electric charges **overcome the built-in potential**, i.e. voltage loss, which can be viewed as the **turn-on voltage V_{on}** of the diode. The piecewise linear model for the diode can be improved by adding a constant voltage **V_{on}** in series with the ideal diode. This is the **constant voltage drop (CVD) model.**

We can think V_{on} as the voltage required to turn on the diode by overcoming V_{bi}.





The diode is forward biased and thus the diode is on with 0.6 V of voltage loss in the circuit.

$v_D = v_{on} =$ **0.6 V** and $I_D = \frac{10-0.6}{10k\Omega} =$ $\boldsymbol{0.94\ mA}$

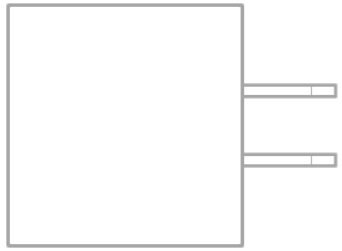
Thus, Q-point is 0.6 V and 0.94 mA.

Half-Wave Rectifier Circuit

The basic rectifier circuit converts an ac voltage to a pulsating dc voltage. A filter is added to eliminate the ac components of the waveform and produce a nearly constant dc voltage output. In fact, majority of electronic circuits are powered by a dc source, usually based on some form of rectifier.

Input Voltage	**240 Volts (AC)**
Wattage	65 watts
Output Voltage	**19.5 Volts (DC)**
Power Source	Corded Electric
Current Rating	3.34 Amps
Frequency Range	60 hertz

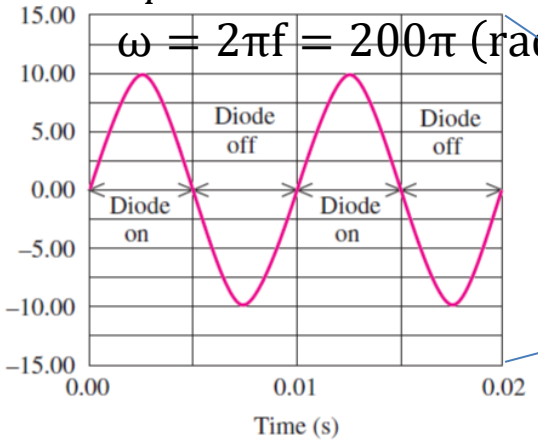
Frequency: 50 to 60 Hz, single phase
Line Voltage: **100 to 240 VAC**
Output Voltage/Current: **9 VDC/2.2 A**
Minimum Power Output: 20 W

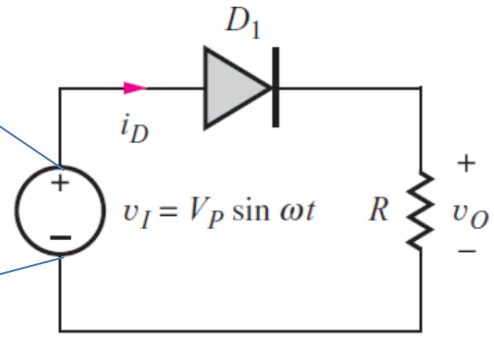


Half-wave rectifier with resistor load

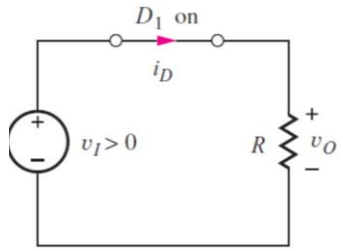
$V_P = 10$ V

$\omega = 2\pi f = 200\pi$ (rad/sec)

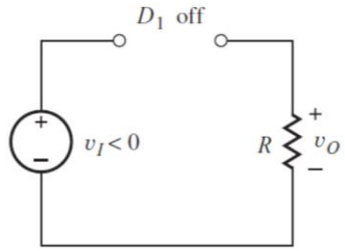




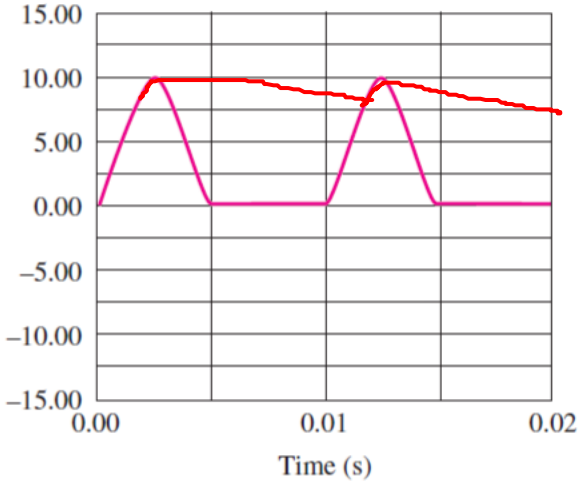
$V_I > 0$, D_1 is on



$V_I < 0$, D_1 is off



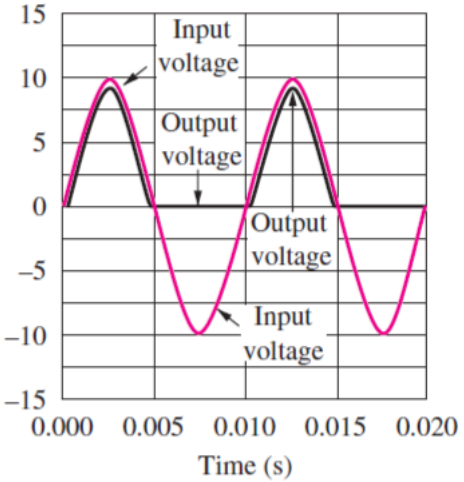
If $V_{on} = 0$ V, $V_O = V_I$



DC like.

v_o is not DC.

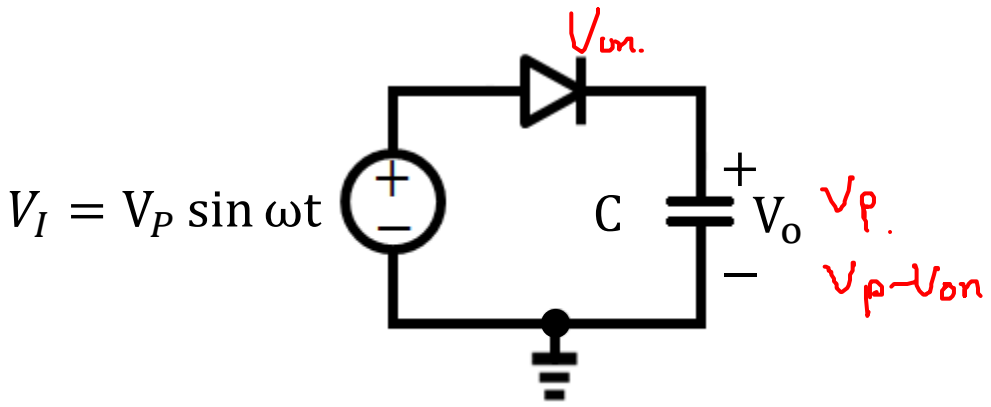
If $V_{on} = 0.7$ V, $V_O = V_P \sin \omega t - V_{on}$



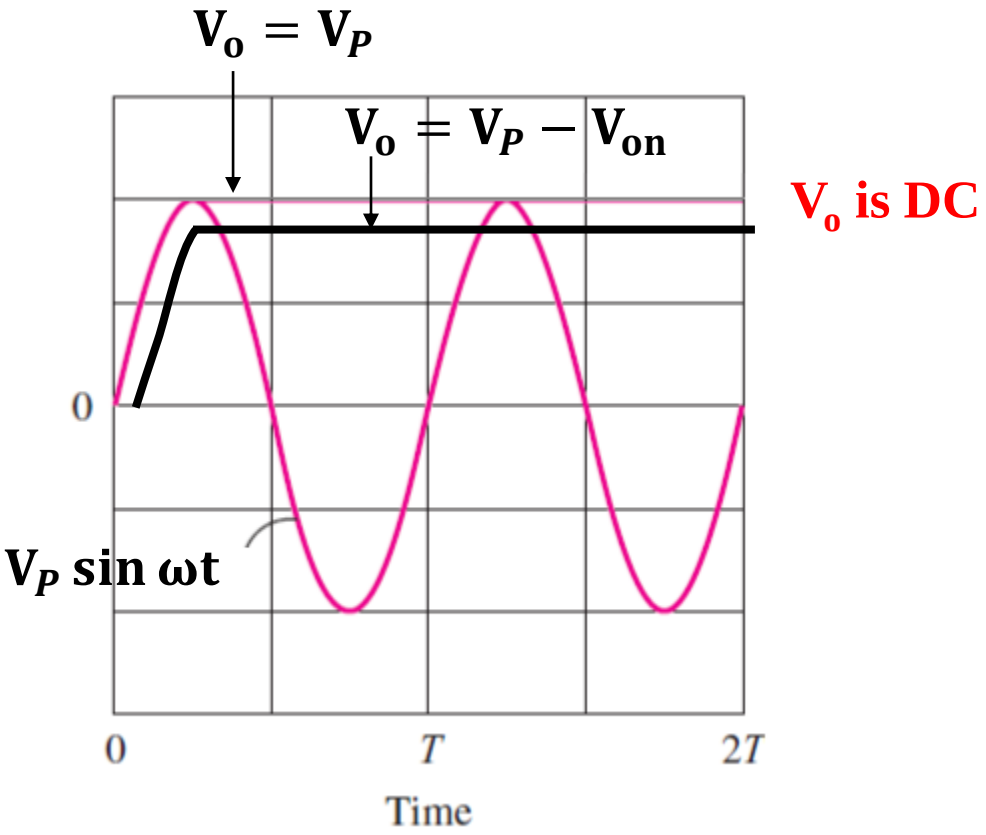
v_o is not DC.

Half-Wave Rectifier with RC Load

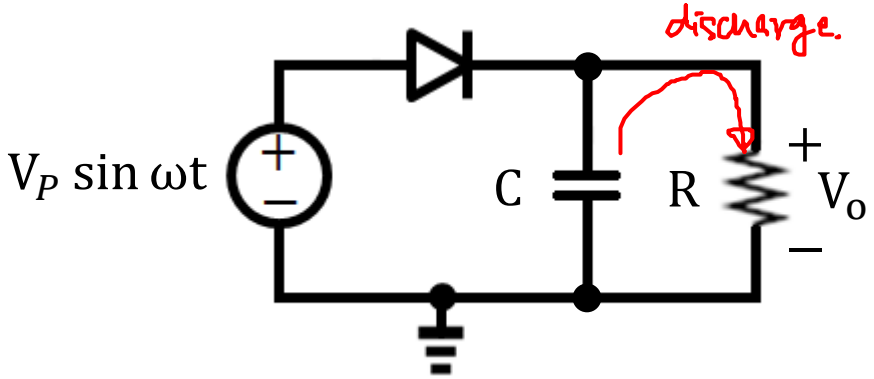
To understand operation of the rectifier filter, we first consider operation of the peak-detector circuit consisting of the input source, diode, and capacitor. The cap was initially discharged $V_o(0) = 0$ V

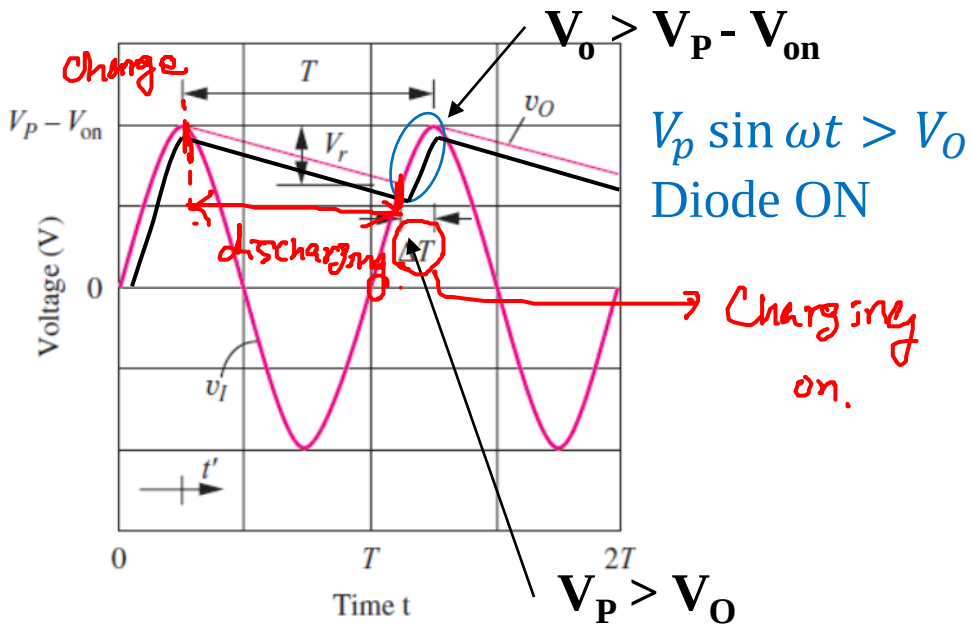


No path for cap discharge when diode is off



By connecting a load R to the peak-detector circuit, now we provide power to the load R, meaning that **there is a path available to discharge the capacitor** during the time the diode is not conducting.





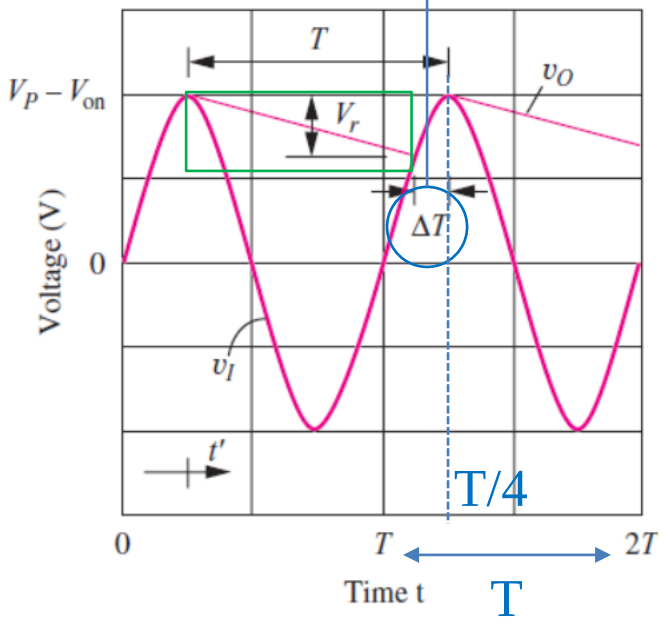
The output voltage is no longer constant, but has **a ripple voltage V_r**. Also, the **diode only conducts for a short time ΔT** during each cycle. We are interested in three parameters:

(1) Ripple voltage V_r

(2) Conduction interval ΔT

(3) Conduction angle $\theta_c = \omega\Delta T$

Ripple Voltage



Recall VE215, **a RC response** without a source (discharge period) is

$$v_o(t) = (V_P - V_{on}) \exp\left(-\frac{t}{RC}\right)$$

Ripple voltage V_r can be described as

$$\boldsymbol{V_r = Peak\ point\ - RC\ response}$$

$$= (V_P - V_{on}) - v_o(t)$$

$$= (V_P - V_{on})\left[1 - \exp\left(-\frac{T-\Delta T}{RC}\right)\right]$$

When diode is off, i.e. RC response

Discharging period

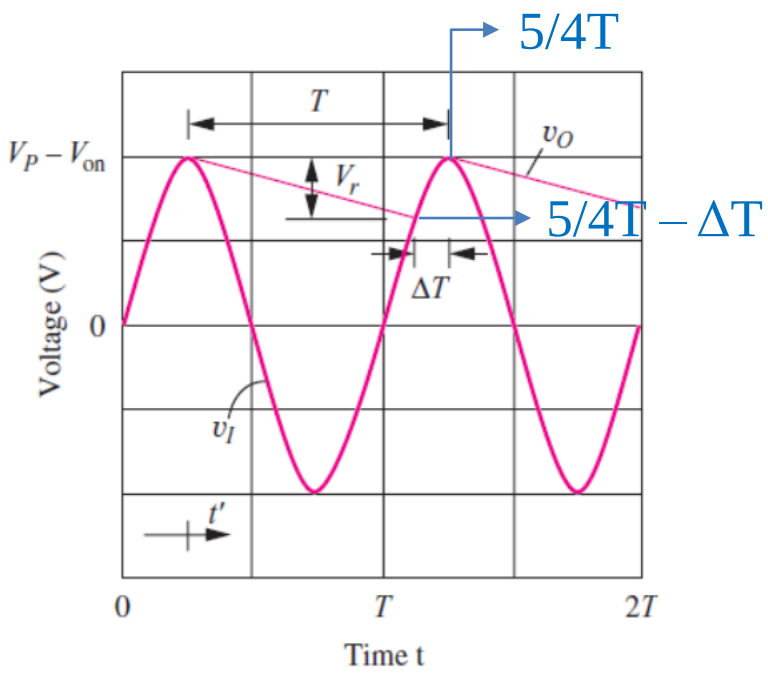
By Taylor series, $e^{-x} = 1 - x$, **ripple voltage V_r** becomes

$V_r = (V_P - V_{on})\left[1 - \left(1 - \frac{T-\Delta T}{RC}\right)\right]$, and to attain stable DC V_r needs to be minimized.

From the graph above, we can see that if $\Delta T \ll T$, V_r becomes smaller.

Thus, finally, $\boldsymbol{V_r = \frac{(V_P - V_{on})}{R}\frac{T}{C}}$

Conduction angle and interval



At 5/4T – ΔT, the input voltage ($V_P - V_{on}$) just exceeds the output voltage (V_O). **Diode is ON**.

$$\Theta = \omega t = 2\pi f \cdot t = \frac{2\pi}{T}\left(\frac{5}{4}T - \Delta T\right) = \frac{5\pi}{2} - \theta_C \; as \; \theta_C = \omega \Delta T$$

At 5/4T – ΔT, **Input sine wave – V_{on} = (Peak of Sine wave – V_{on}) – V_r**

$$V_P \sin\left[\omega\left(\frac{5T}{4} - \Delta T\right)\right] - V_{on} = (V_P - V_{on}) - V_r$$

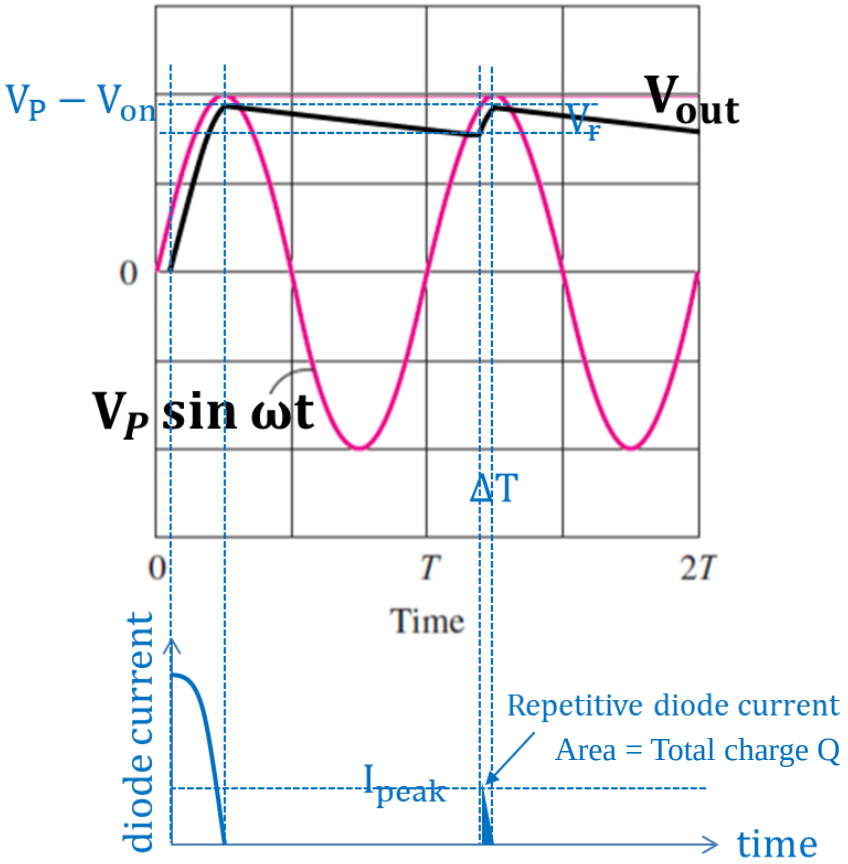
$$\longrightarrow V_P \sin\left(\frac{5\pi}{2} - \theta_c\right) - V_{on} = (V_P - V_{on}) - V_r$$

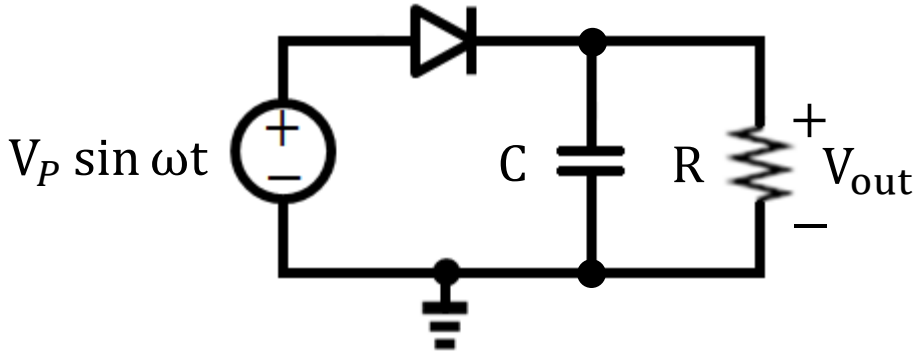
Thus, the equation becomes $V_P \cos\theta_c = V_P - V_r \longrightarrow \cos\theta_c = \frac{V_P - V_r}{V_P} \cong 1 - \frac{\theta_c^{\,2}}{2}$ if θ_c is very small

$$\boldsymbol{\theta_c = \sqrt{\frac{2V_r}{V_P}}} \qquad \boldsymbol{\Delta T = \frac{\theta_c}{\omega} = \frac{1}{\omega}\sqrt{\frac{2V_r}{V_s}}}$$

Diode Current

Diode current flows for only a very small fraction of the period T. **The capacitor is charged during ΔT and is discharged during $T - \Delta T$.**





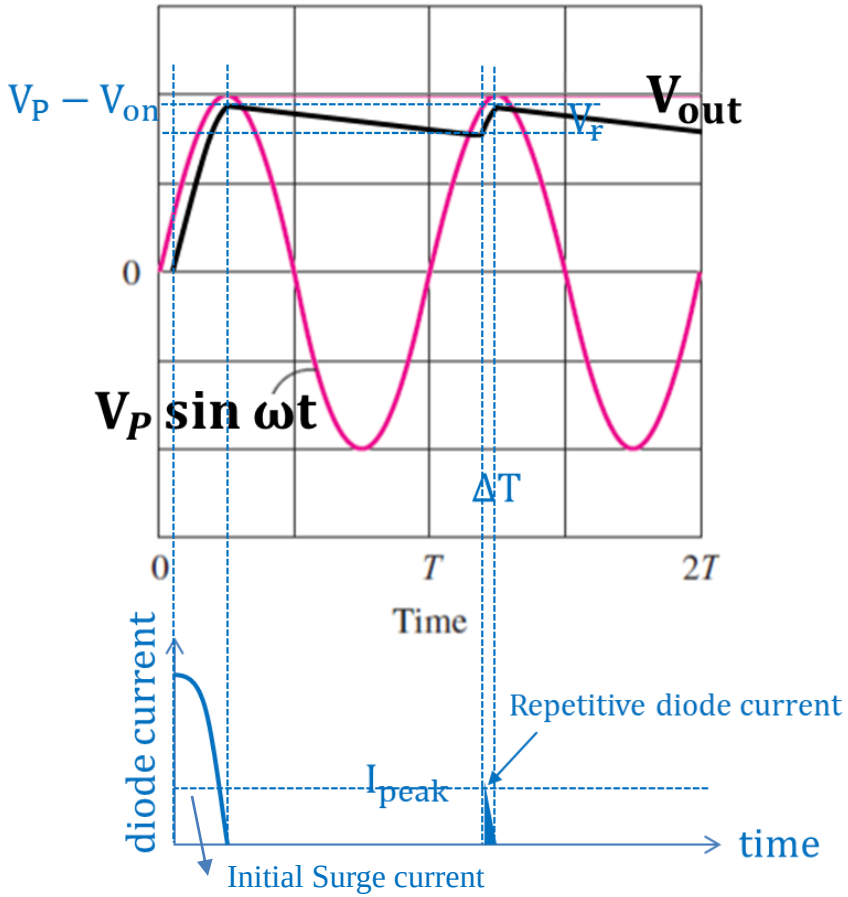
$$Q \cong \frac{I_{peak}\Delta T}{2} = I_{dc}(T - \Delta T) \cong I_{dc}T$$

$$where\ I_{dc} = \frac{V_p - V_{on}}{R}$$

$$\rightarrow \mathbf{I_{peak}} = \frac{\mathbf{2I_{dc}T}}{\mathbf{\Delta T}}$$

Surge Current

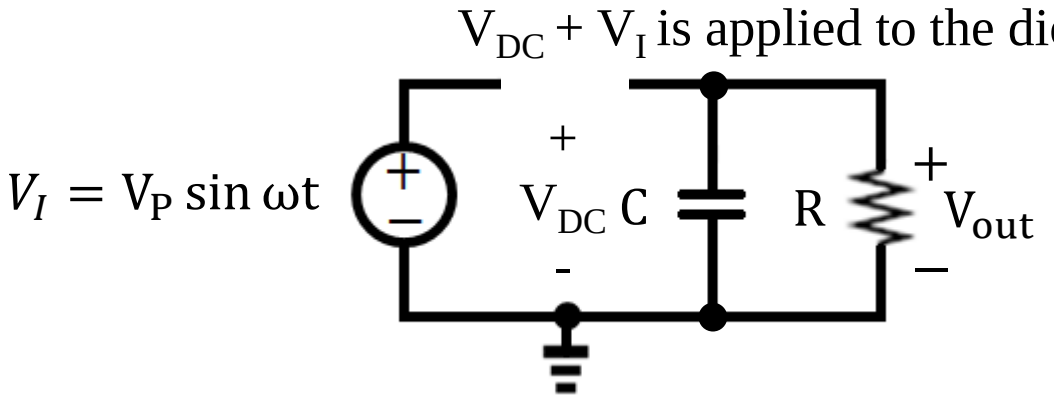
At the first cycle, the capacitor is completely discharged (as we assumed), and therefore, there will be a larger current through the diode. During charging period (ΔT), almost all diode current goes to C.

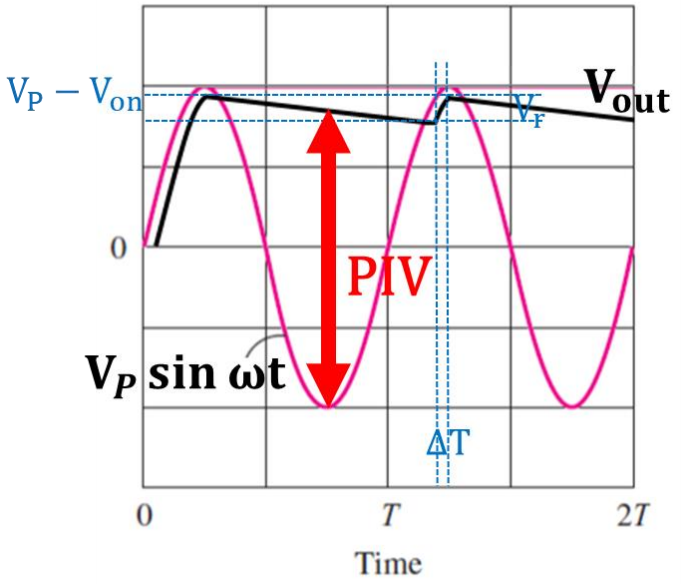


$$\boldsymbol{I_{surge}} = i_d(t) = \mathrm{C}\frac{\mathrm{d}(\mathrm{V}_P \sin \omega \mathrm{t} - \mathrm{V}_{\mathrm{on}})}{\mathrm{dt}} = \boldsymbol{\omega C V_P \cos \omega t}$$

Peak Inverse Voltage (PIV)

The breakdown voltage rating of the diodes is called the peak-inverse-voltage (VIP). If V_r is very small, the diode must be able to withstand a large negative peak voltage.

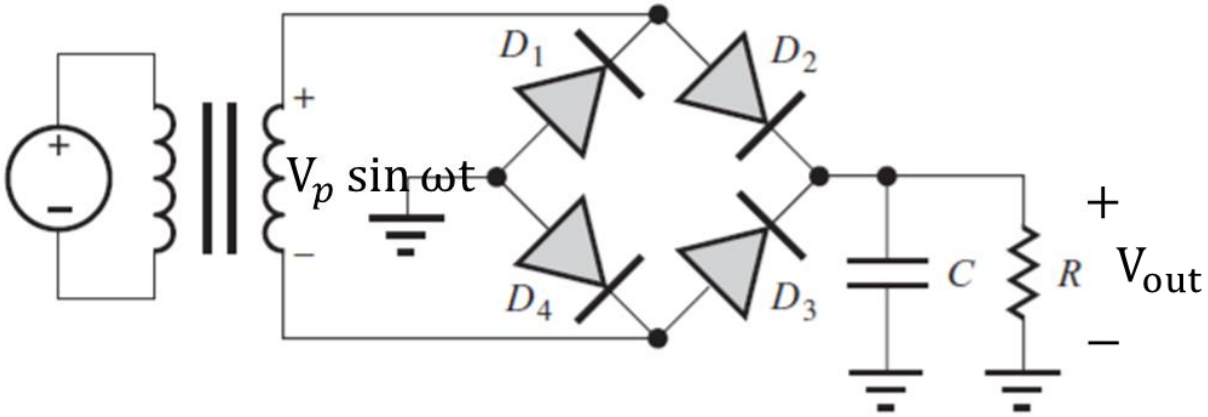


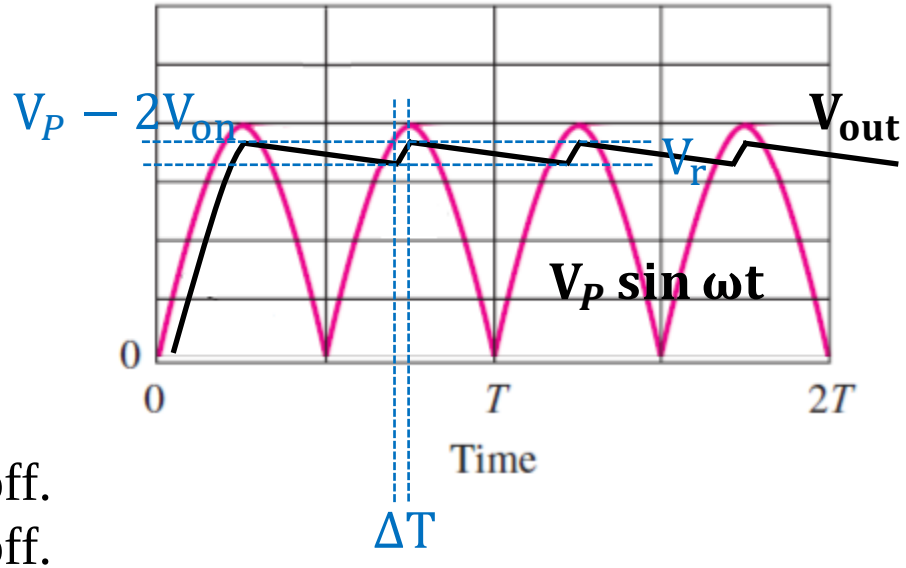


Peak-inverse-voltage (PIV) $\geq V_{DC} + V_I = V_P - V_{on} + V_P \cong 2V_P - V_{on}$

If the diode PIV is smaller than $2V_P - V_{on}$, the diode breaks down.

Full-Wave Bridge Rectifier





For $v_I > 0$, D_2 and D_4 will be on and D_1 and D_3 will be off.
For $v_I < 0$, D_1 and D_3 will be on and D_2 and D_4 will be off.

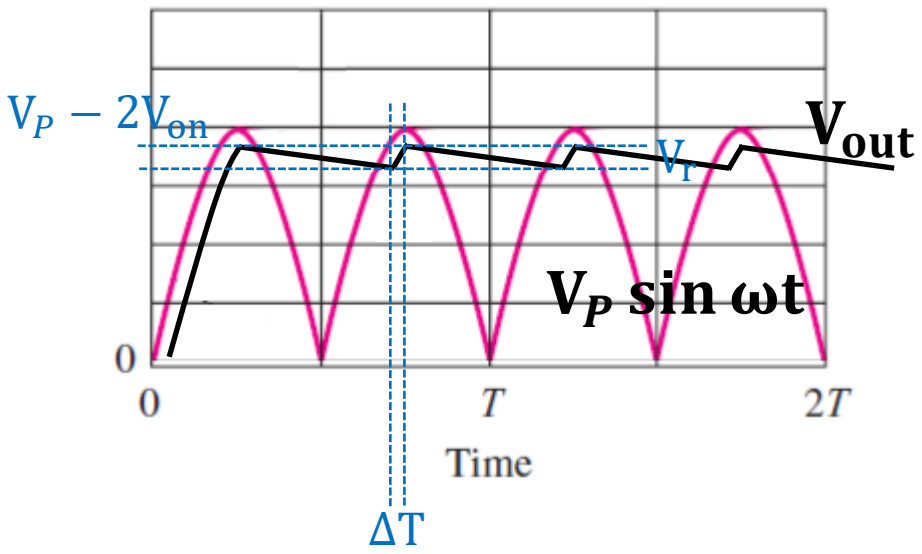
$$V_{dc} = \mathbf{V_P - 2V_{on}}$$

$$I_{dc} = \frac{V_{dc}}{R}$$

$$\mathbf{V_r} = (V_P - 2V_{on})\left(1 - e^{-\frac{T/2-\Delta T}{RC}}\right) \cong (V_P - 2V_{on})\left(\frac{T/2 - \Delta T}{RC}\right) \quad if \left(\frac{T}{2} - \Delta T\right) \ll RC$$

$$\cong (\mathbf{V_P - 2V_{on}})\left(\frac{\mathbf{T}}{\mathbf{2RC}}\right) \quad if\ \Delta T \ll \frac{T}{2}$$

Conduction angle and interval



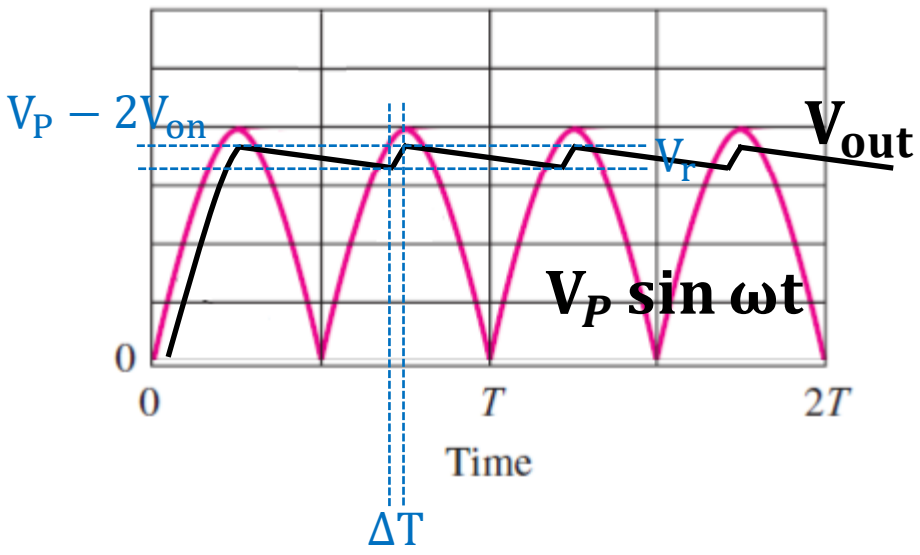
$$-V_P \sin\left[\omega\left(\frac{3T}{4} - \Delta T\right)\right] - 2V_{on} = (V_P - 2V_{on}) - V_r$$

$$-V_P \sin\left(\frac{3\pi}{2} - \theta_c\right) - 2V_{on} = (V_P - 2V_{on}) - V_r$$

$$V_P \cos\theta_c = V_s - V_r$$

$$\cos\theta_c = \frac{V_P - V_r}{V_s} \cong 1 - \frac{{\theta_c}^2}{2} \quad \textit{if } \theta_c \textit{ very small}$$

$$\boldsymbol{\theta_c = \sqrt{\frac{2V_r}{V_P}}} \qquad \boldsymbol{\Delta T = \frac{\theta_c}{\omega} = \frac{1}{\omega}\sqrt{\frac{2V_r}{V_P}}}$$

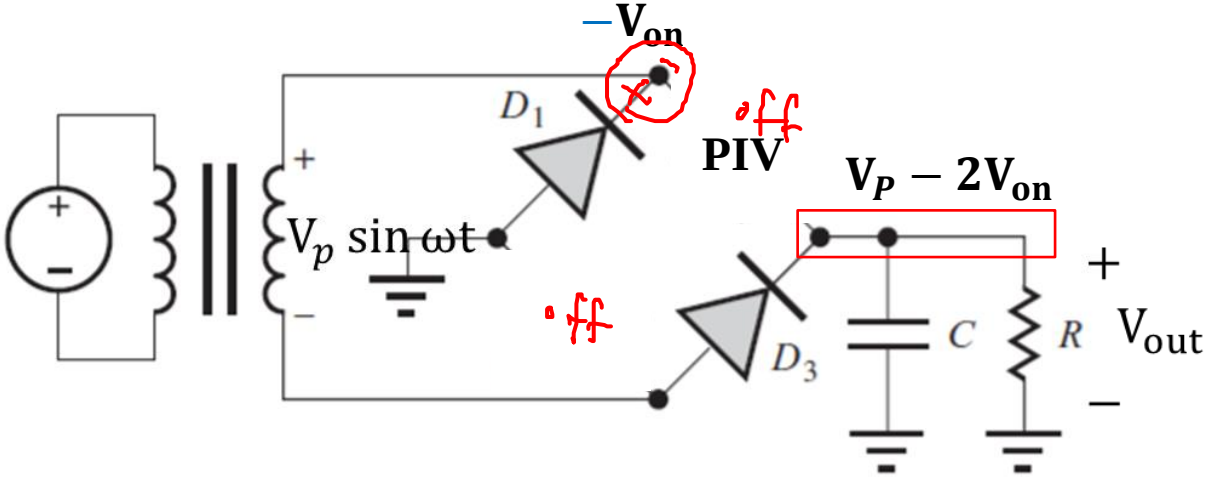


$$Q \cong \frac{I_{peak}\Delta T}{2} = I_{dc}\left(\frac{T}{2} - \Delta T\right) \cong I_{dc}\frac{T}{2}$$

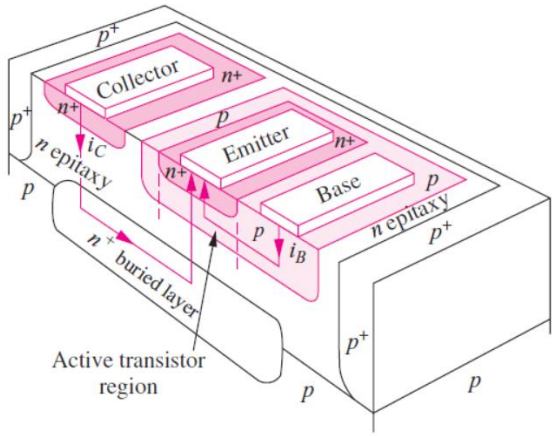
$$\mathbf{I_{peak} = \frac{I_{dc}T}{\Delta T}}$$

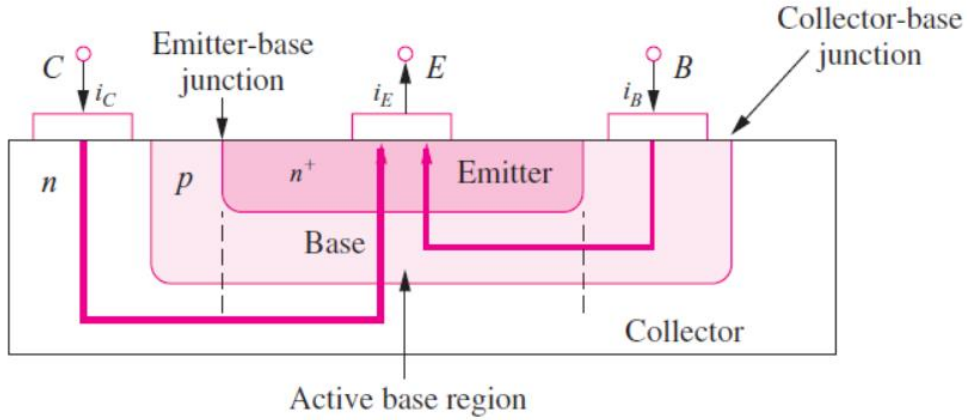
$$\mathbf{I_{surge} = \omega C V_P \ (at\ t = 0)}$$

$$\mathbf{PIV = V_P - V_{on} \cong V_P}$$



Device Schematics





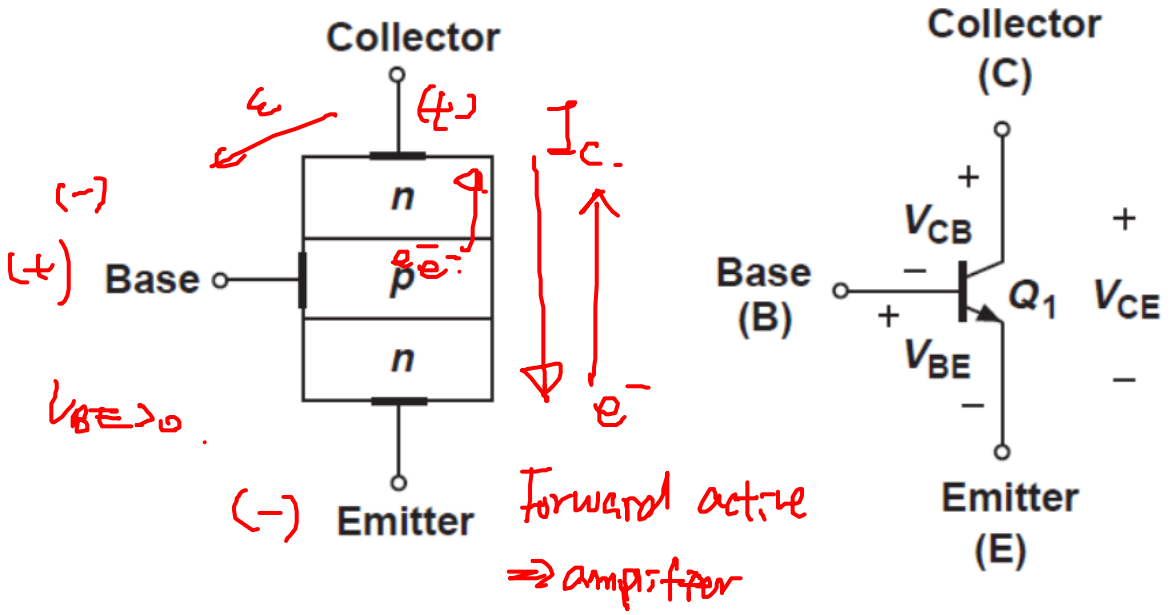
BJT has **n^+-p-n** or **p^+-n-p** structure.

e.g. n^+-p-n structure

- Emitter: heavily doped n−type
- Base: p-region
- Collector: lower n-region
- Electron diffusion length (L_n) in base $\gg W_b$
- Emitter doping $N_{de} \gg$ base doping N_{ab} ($I_n \approx I$)

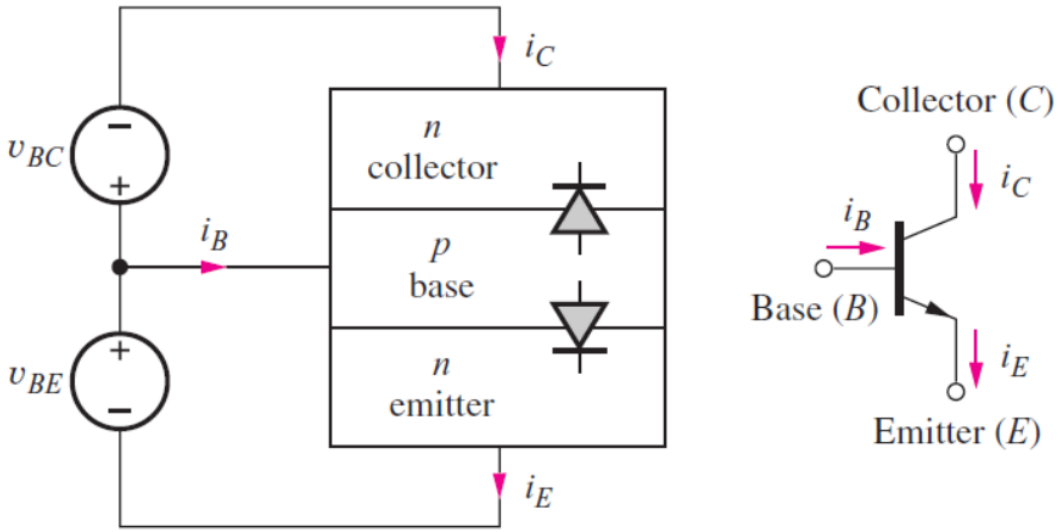
Structure of BJT

The BJT consists of three doped regions forming a sandwich. Below is an example comprising of a *p* layer sandwiched between two *n* regions and called an ***npn* BJT.**



There are three terminal voltages V_E, V_B, and V_C, and consequently the voltage differences between terminals V_{BE}, V_{CB}, and V_{CE}. Among various biasing conditions, **for amplification of BJT**, there is **only one biasing condition**.

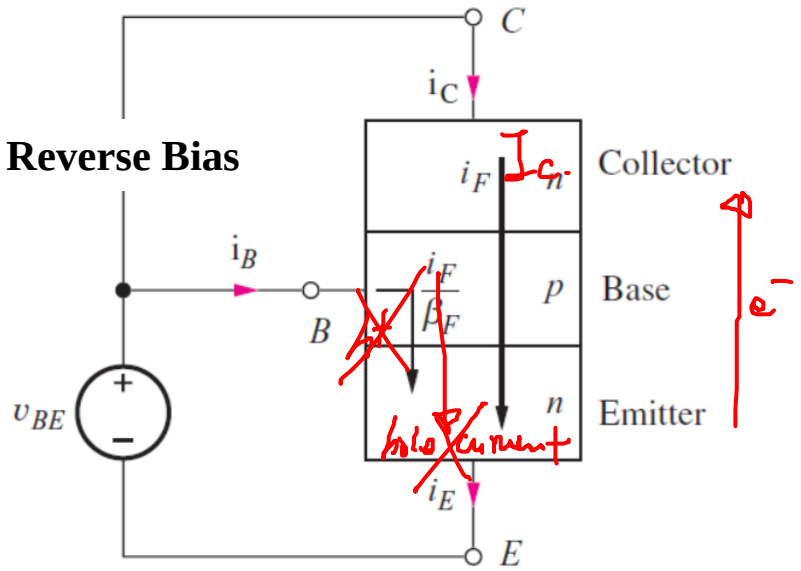
Transport Model for NPN BJT

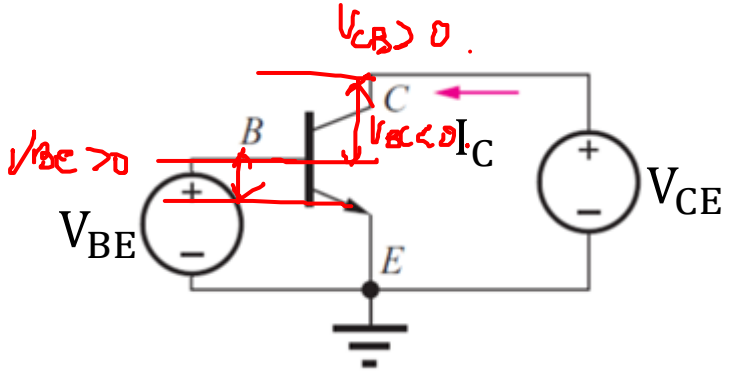


There are also three terminal currents, **collector current i_C, emitter current i_E,** and **base current i_B.** The base-emitter voltage v_{BE} and the base-collector voltage v_{BC} applied to the two *pn* junctions **determine the magnitude of these three currents in the BJT** and are defined as **positive when they forward-bias** their respective *pn* junctions.

The bias condition for the Forward active mode of BJT (a normal BJT operation mode) is $\mathbf{v_{BE} > 0}$ **and** $\mathbf{v_{BC} < 0}$.

Forward bias
Barrier ↓ and charges flow





$V_{CE} \geq V_{BE}$
$\Rightarrow$ **Forward − Active**

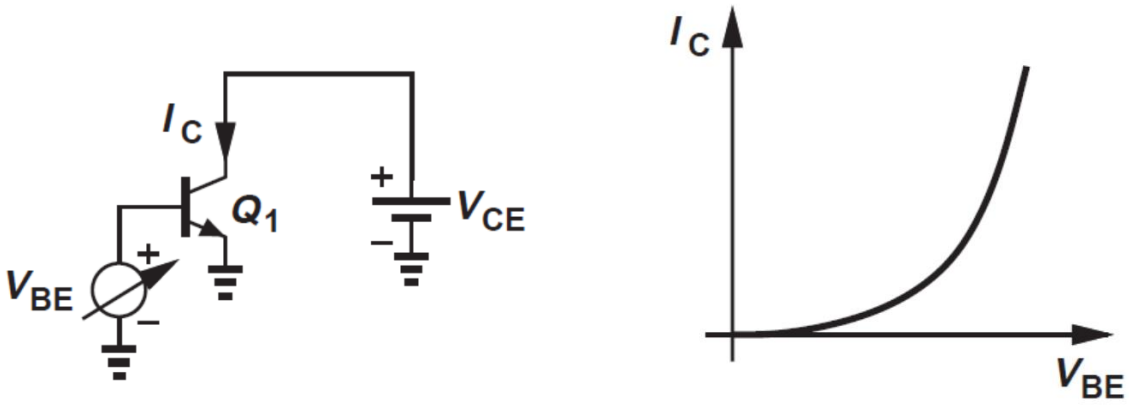
$$\mathbf{i_C = i_F = I_S}\left[e^{v_{BE}/V_T} - 1\right]$$

$$i_B = {}^{i_F}/_{\beta_F} = {}^{I_S}/_{\beta_F}\left[e^{v_{BE}/V_T} - 1\right]$$

$$i_E = I_S\left[e^{v_{BE}/V_T} - 1\right] + {}^{I_S}/_{\beta_F}\left[e^{v_{BE}/V_T} - 1\right] = \left(I_S + \frac{I_S}{\beta_F}\right)\left[e^{v_{BE}/V_T} - 1\right]$$

Large-Signal Model

IV characteristics – Transfer characteristic

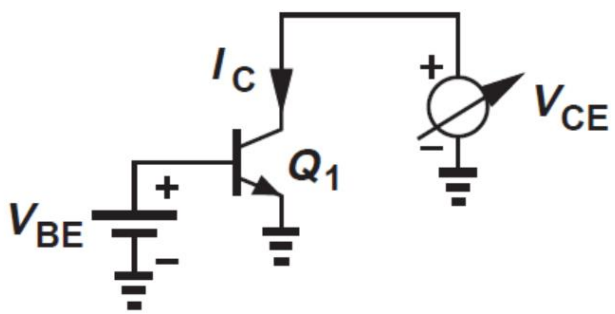


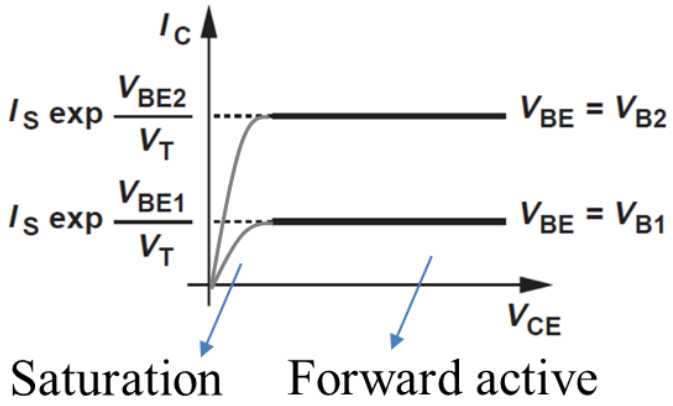
Transfer characteristic plots I_C vs V_{BE} with the assumption that the **V_{CE} is constant and no lower than the V_{BE}**, i.e. $V_{CE} > V_{BE}$. Thus, the BJT is in the forward active mode.

I_C is independent of V_{CE}; thus, different values of V_{CE} do not alter the characteristic.

$i_C = I_S[e^{v_{BE}/V_T} - 1]$

IV characteristics – Output characteristic





Output characteristic shows **I_C for a given V_{BE} but with V_{CE} varying**.

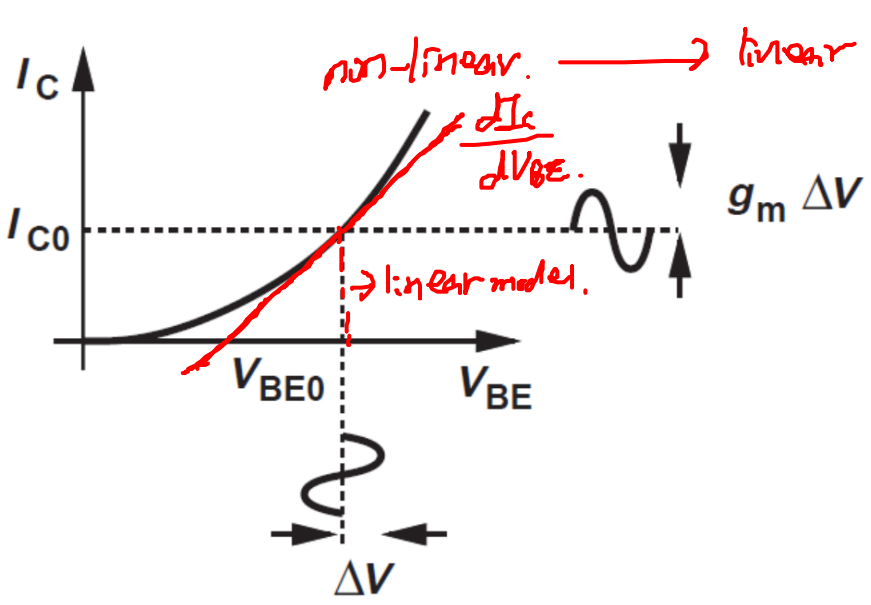
V_{CE} < V_{BE}, Both diodes (B-E and C-B) are on and thus the BJT is in a saturation.

V_{CE} > V_{BE}, BJT is in a forward active. V_{BE} increases I_C increases as $i_C = I_S[e^{v_{BE}/V_T} - 1]$

Transconductance

In the **forward active region**, the transistor becomes **a better amplifying device** by producing larger changes in I_C in response to a given signal level (V_{BE}) applied (I_C/V_{BE}).

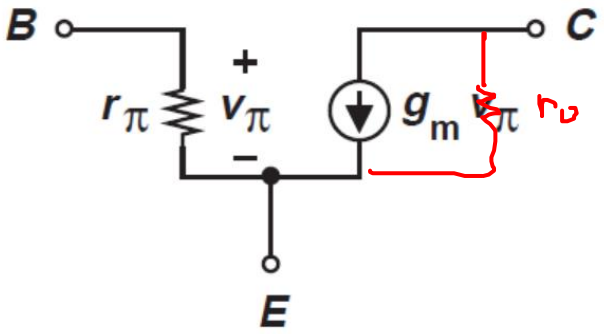
$g_m = dI_C/dV_{BE}$ represents the slope of I_C–V_{BE} characteristic at a given I_{C0}, and the corresponding V_{BE0}. In other words, **if V_{BE} experiences a small perturbation $\pm\Delta V$ around V_{BE0}, then the I_C displays a change of $\pm g_m \Delta V$ around I_{C0}.**



$$g_m = \frac{dI_C}{dV_{BE}} = \frac{d}{dV_{BE}}\left(I_S exp\frac{V_{BE}}{V_T}\right)$$
$$= \frac{1}{V_T} I_S exp\frac{V_{BE}}{V_T} = \frac{I_C}{V_T}$$

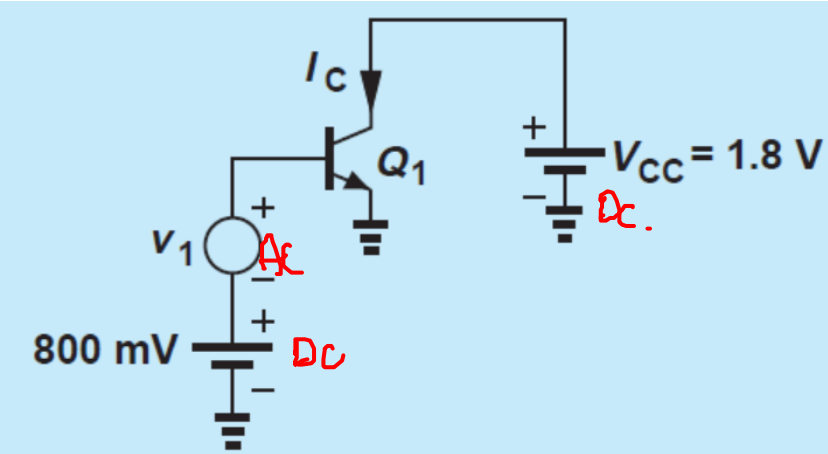
Small-Signal Model

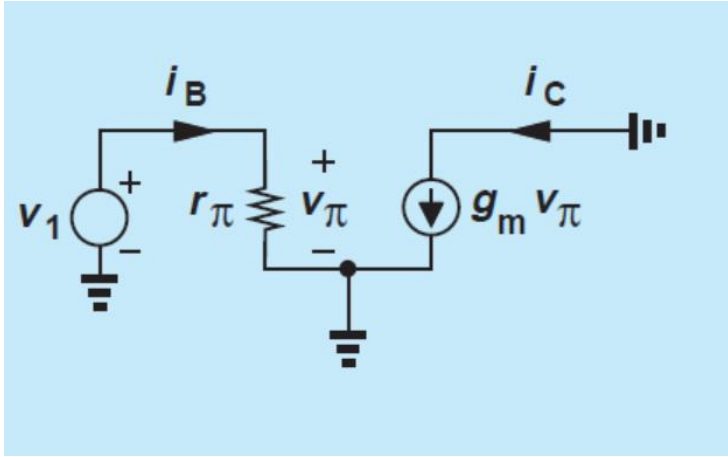
Without Early Effect



$$g_m = \frac{dI_C}{dV_{BE}} = \frac{I_C}{V_T}$$

$$r_\pi = \frac{\Delta V_{BE}}{\Delta I_B} = \frac{\beta}{g_m}$$

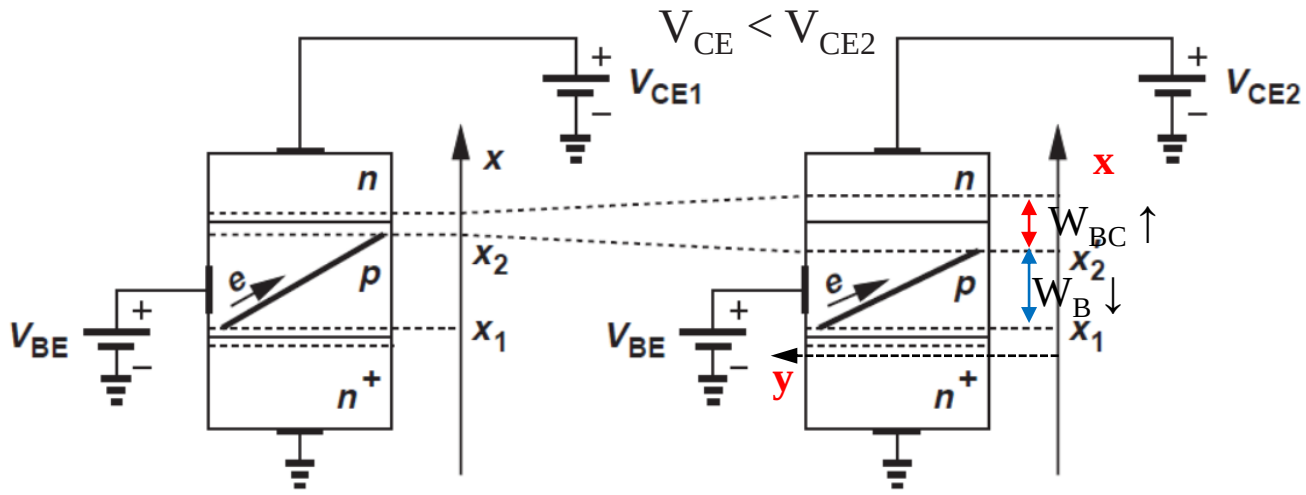




Ground all constant voltage sources and open all constant current sources while constructing the small-signal equivalent circuit

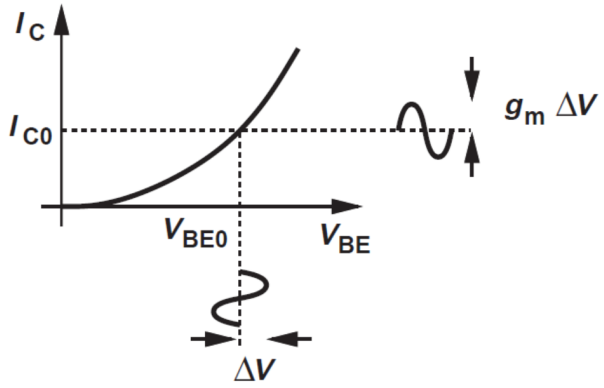
Early Effect

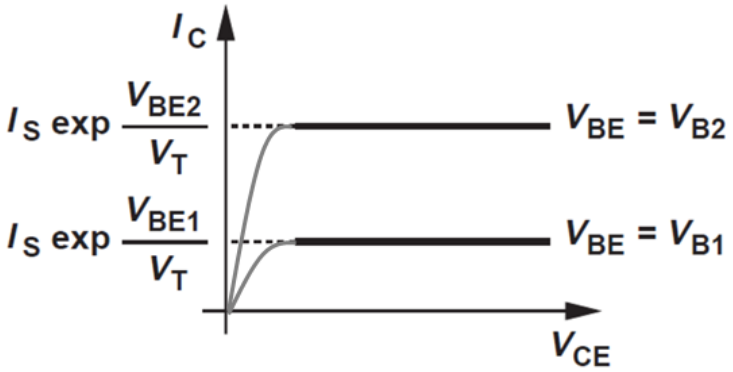
As $V_{CE} < V_{CE2}$, the depletion region in C-B areas increases, and thus **the slope of the profile increases.** Equivalently, the effective **W_B decreases**, thereby **increasing I_C. Early effect indicates that the V_{CE} does affect the I_C.**



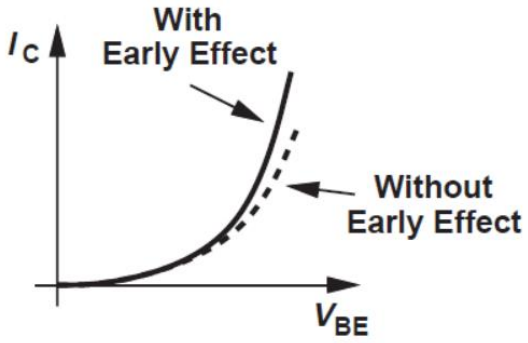
With the Early effect, $I_C \approx \left(I_S exp \frac{V_{BE}}{V_T}\right)\left(1 + \frac{V_{CE}}{V_A}\right)$ V_A = Early voltage

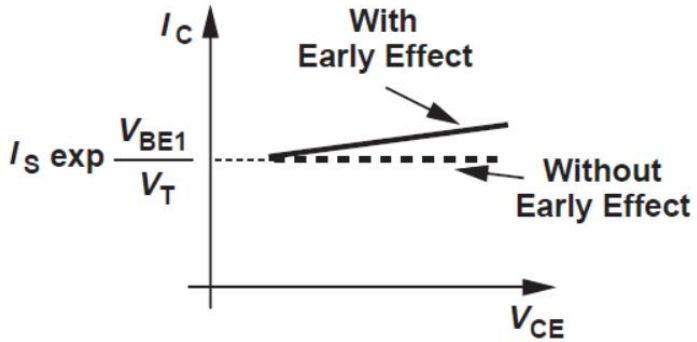
Without the Early effect, $i_C = I_S[e^{v_{BE}/V_T} - 1]$



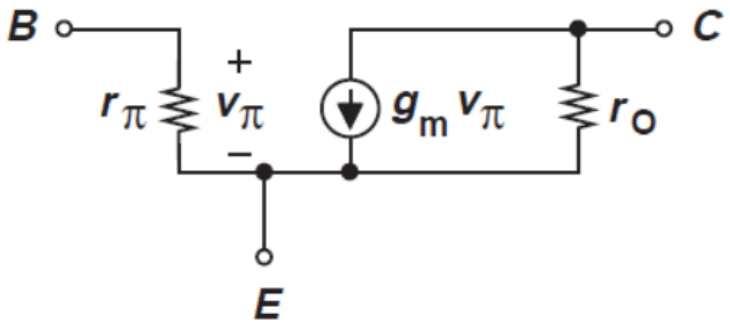


With the Early effect, $I_C \approx \left(I_S exp \frac{V_{BE}}{V_T}\right)\left(1 + \frac{V_{CE}}{V_A}\right)$





Small-signal model with Early effect



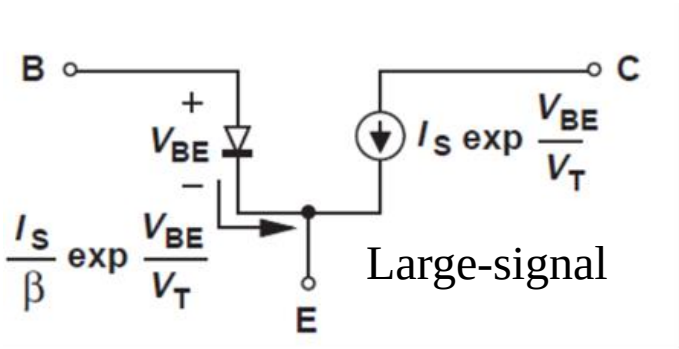
$$g_m = \frac{I_C}{V_T}$$

$$r_\pi = \frac{\beta}{g_m}$$

$$r_O \approx \frac{V_A}{I_C}$$

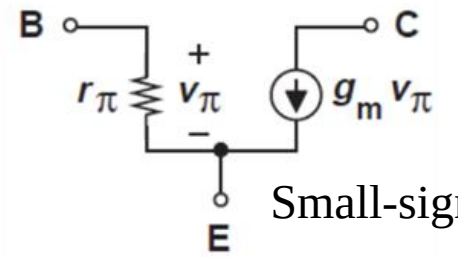
The small-signal model contains **only one extra element r_O to represent the Early effect**. This **output resistance r_O** plays a critical role in high gain amplifiers

Summary

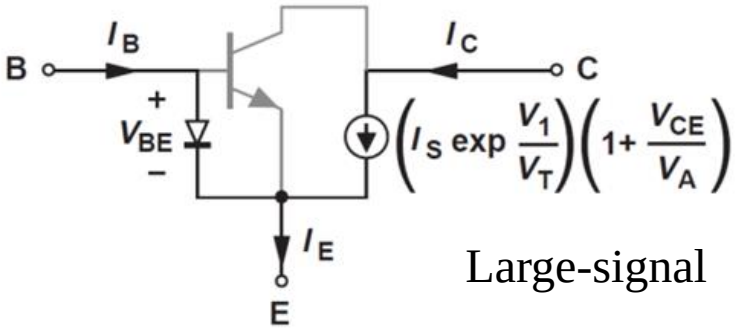


Large-signal

Without Early Effect

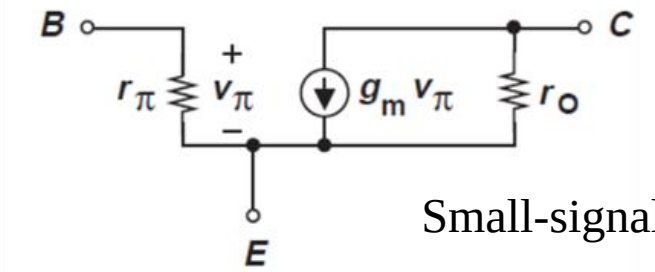


Small-signal



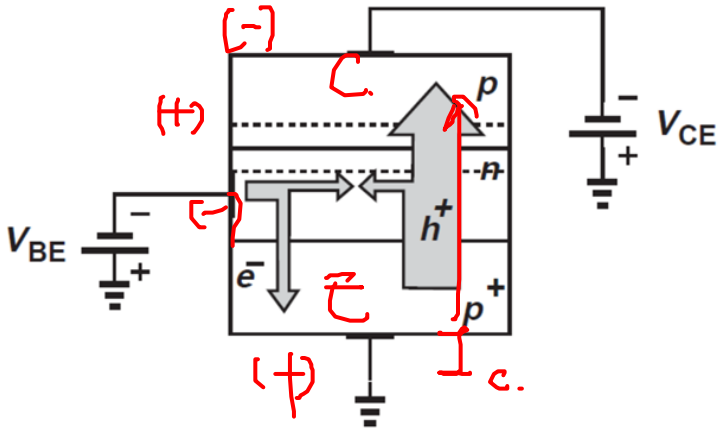
Large-signal

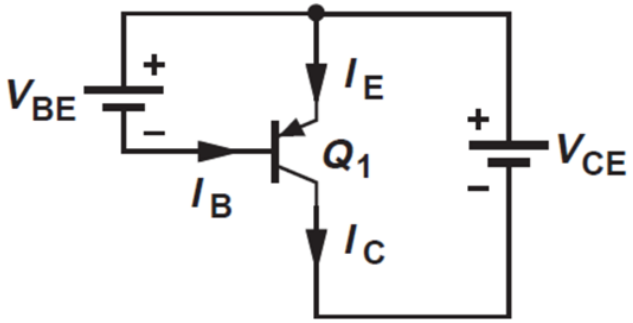
With Early Effect



Small-signal

PNP BJT





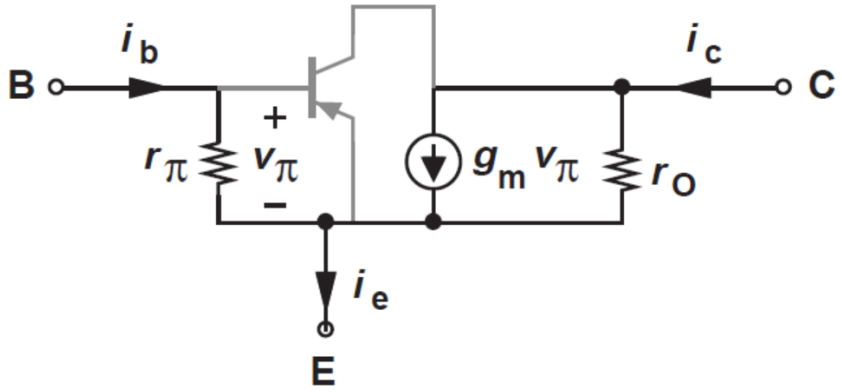
$$i_C = i_F = I_S\left[e^{v_{EB}/V_T} - 1\right]$$

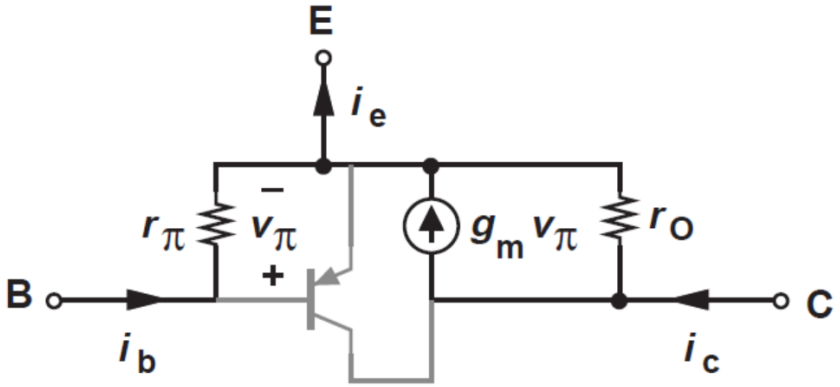
$$i_B = {}^{i_F}/_{\beta_F} = {}^{I_S}/_{\beta_F}\left[e^{v_{EB}/V_T} - 1\right]$$

$$i_E = \left(I_S + \frac{I_S}{\beta_F}\right)\left[e^{v_{EB}/V_T} - 1\right]$$

Operation of PNP in the active region requires forward biasing the base-emitter junction and reverse-biasing the collector junction. Thus, $\mathbf{V_{BE} < 0}$ **(Forward) and** $\mathbf{V_{BC} > 0}$ **(Reverse)**. All of the operation principles and equations described for npn transistors apply to pnp devices as well.

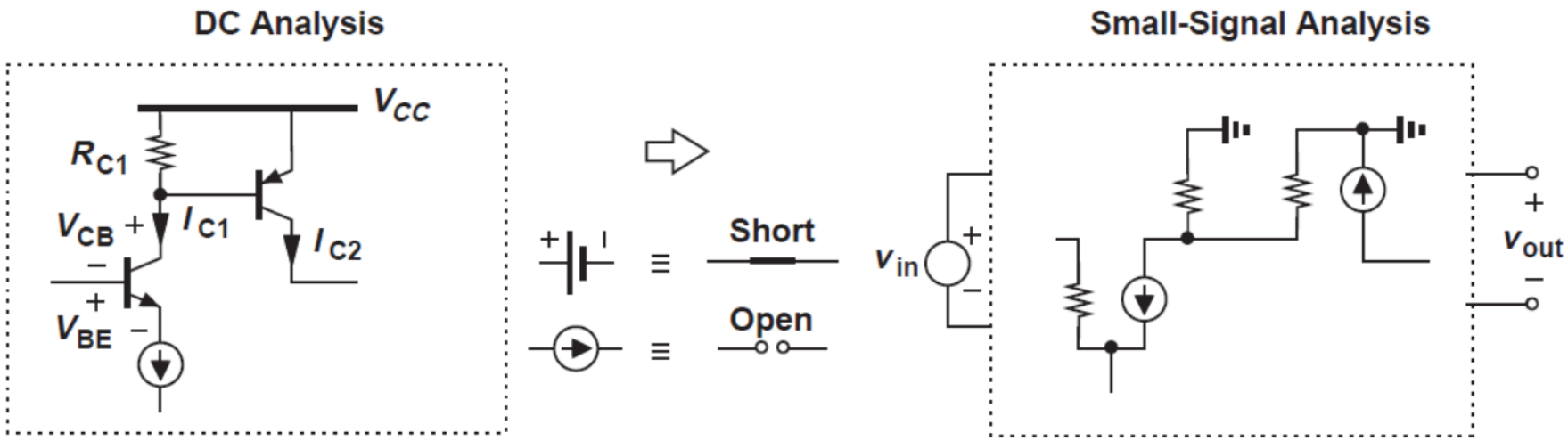
PNP BJT Small Signal model





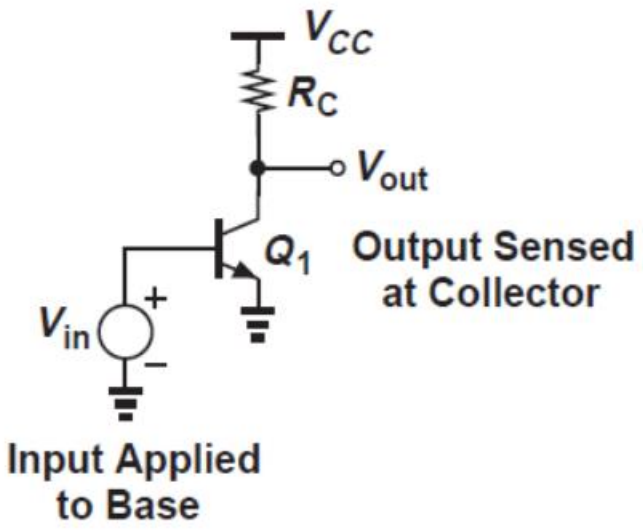
Since the small-signal model represents changes in the voltages and currents, we expect npn and pnp transistors to have similar models. **The small signal model of the pnp transistor is indeed identical to that of the npn device.**

DC and Small-Signal Analysis



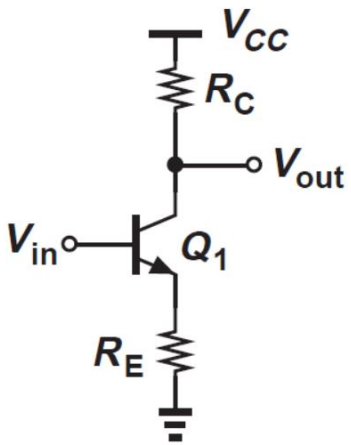
How to analyze a BJT circuit? (1) we determine the **effect of constant voltages and currents while signal sources are set to zero**; (2) we analyze the response to signal sources while **constant sources are set to zero**.

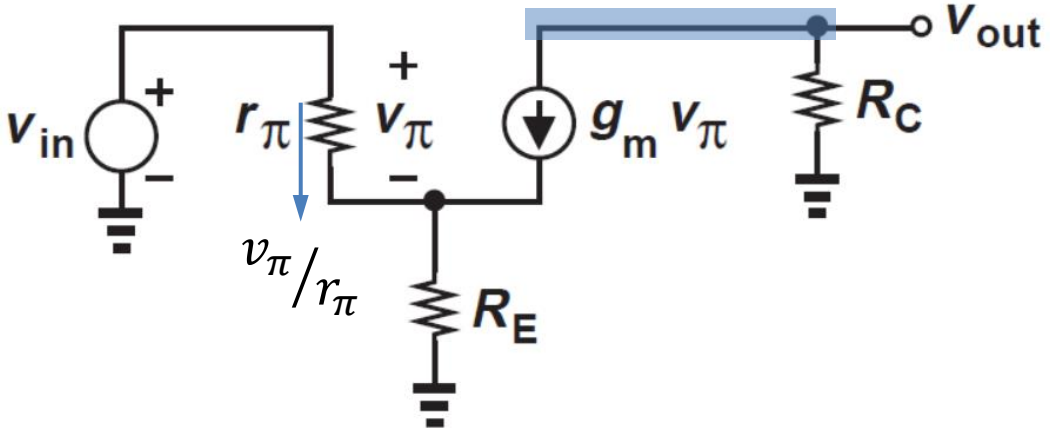
Common-Emitter (C-E) Amplifier



If the input signal is applied to base (B) and the output signal is sensed at the collector (C), the circuit is called a **common-emitter (C-E) stage, i.e. emitter (E) is grounded and appears in common to the input and output.**

CE Stage With Emitter Degeneration (Without Early Effect)





By KCL, $-g_m v_\pi = {}^{v_{out}}/_{R_C} \rightarrow v_\pi = -{}^{v_{out}}/_{g_m R_C}$

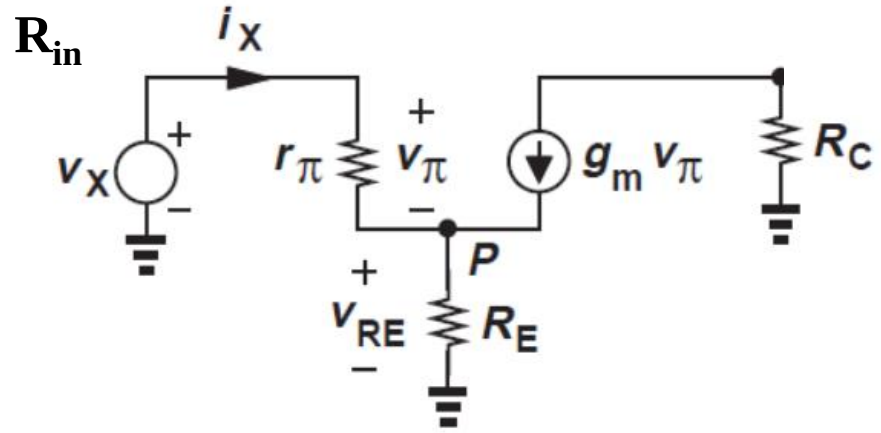
Current through $R_E = {}^{v_\pi}/_{r_\pi} + g_m v_\pi$

By KVL: $-v_{in} + v_\pi + v_{R_E} = 0 \; where \; v_{R_E} = ({}^{v_\pi}/_{r_\pi} + g_m v_\pi) R_E$

Thus, $v_{in} = v_\pi + ({}^{v_\pi}/_{r_\pi} + g_m v_\pi) R_E = v_\pi [1 + ({}^{1}/_{r_\pi} + g_m) R_E]$

$$\frac{v_{out}}{v_{in}} = -\frac{g_m R_C}{1 + \left({}^{1}/_{r_\pi} + g_m\right) R_E} \approx -\frac{g_m R_C}{1 + g_m R_E}$$

CE Stage With Emitter Degeneration-Input and Output Impedance

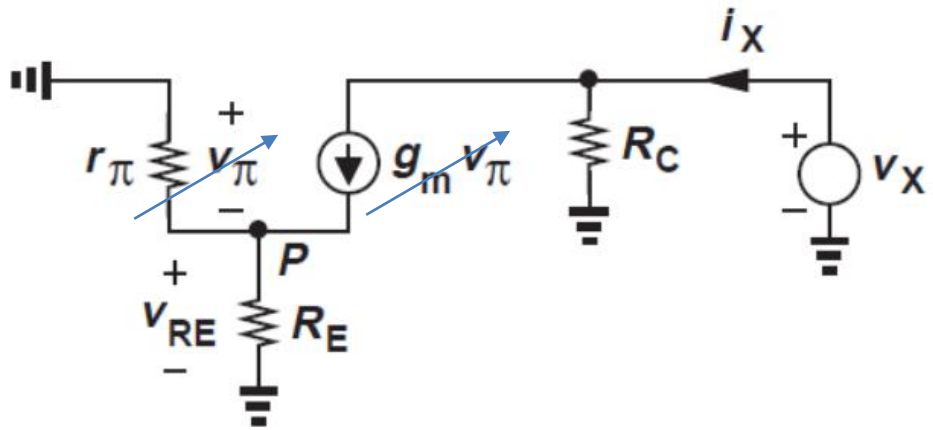


$v_\pi = r_\pi i_x$

Current through $\mathbf{R_E}$ is $i_x + g_m v_\pi = i_x + g_m r_\pi i_x = (\mathbf{1} + \boldsymbol{\beta})\boldsymbol{i_X}$ as $r_\pi = {}^{\beta}/_{g_m}$

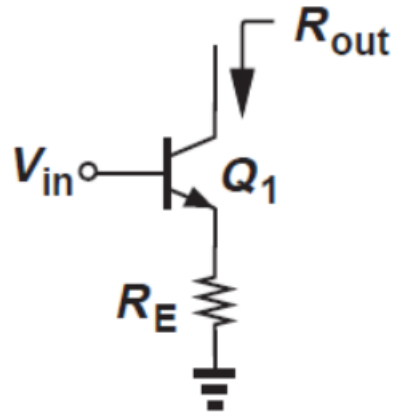
$v_x = r_\pi i_x + R_E(1 + \beta) i_X$ and thus $\boldsymbol{R_{in}} = {}^{v_x}/_{i_x} = \boldsymbol{r_\pi} + (\boldsymbol{\beta} + \mathbf{1})\boldsymbol{R_E}$

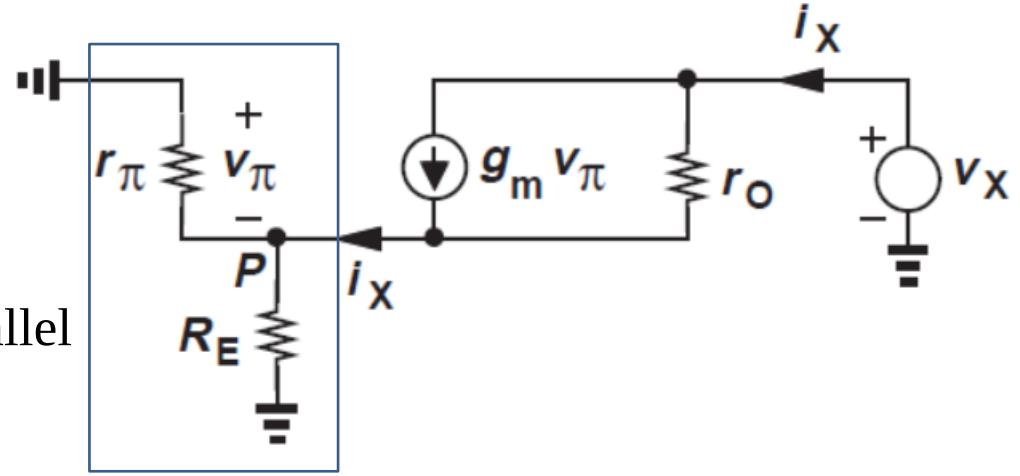
R_{out}



$v_\pi = 0$, all i_X flows through R_C and thus $R_{out} = R_C$

Effect of Transistor Output Resistance with Early Effect





Parallel

$v_\pi = -i_x(R_E \| r_\pi)$

A current through r_O is $i_X - g_m v_\pi$

By KVL: $-v_X + r_O(i_X - g_m v_\pi) - v_\pi = 0 \rightarrow \boldsymbol{v_X = r_O[i_X + g_m i_x(R_E \| r_\pi)] + i_x(R_E \| r_\pi)}$

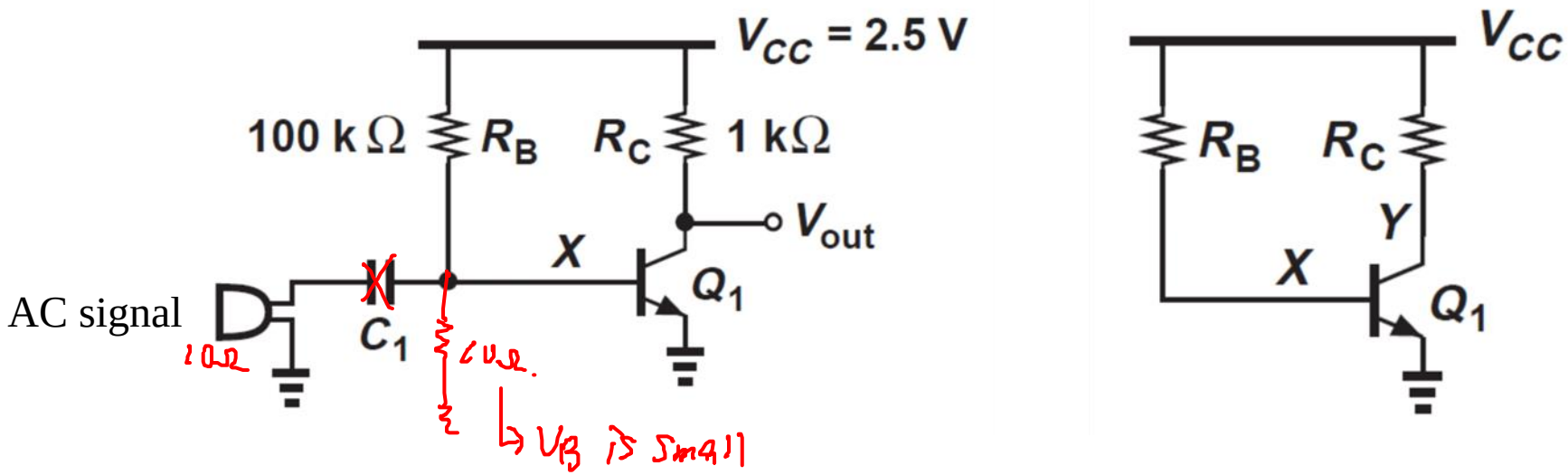
$\boldsymbol{R_{out}} = {}^{v_X}/_{i_X} = r_O[1 + g_m(R_E \| r_\pi)] + (R_E \| r_\pi) \rightarrow \boldsymbol{r_O + (g_m r_O + 1)(R_E \| r_\pi)}$

$\boldsymbol{R_{out} \approx r_O[1 + g_m(R_E \| r_\pi)]}$ **as** $\boldsymbol{g_m r_O \gg 1}$ $\boldsymbol{(intrinsic\ gain)}$

Increase in the output impedance r_O produces amplifiers with a higher gain.

Coupling capacitor

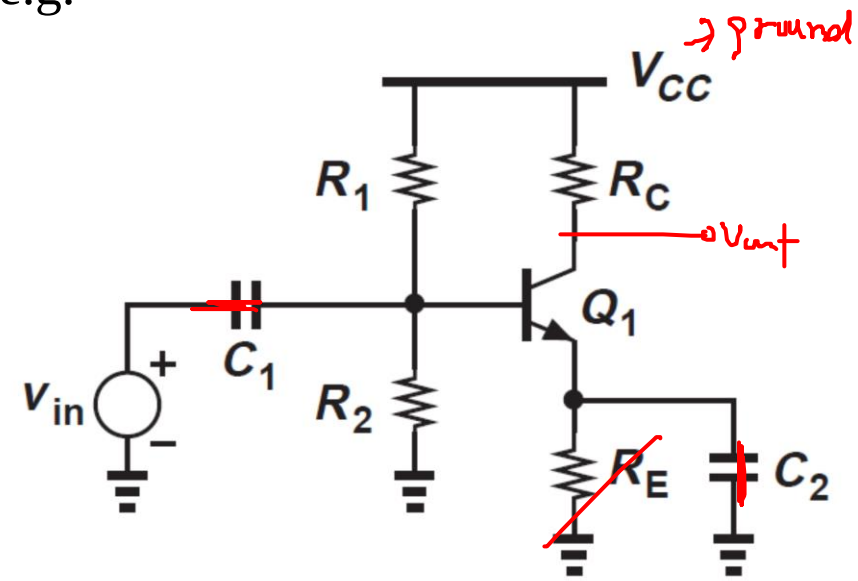
↳ Separate DC and AC signal.

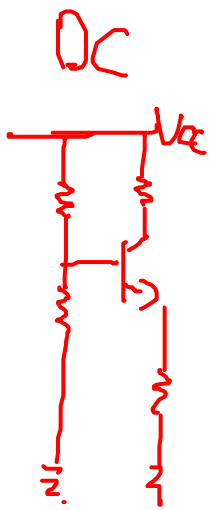


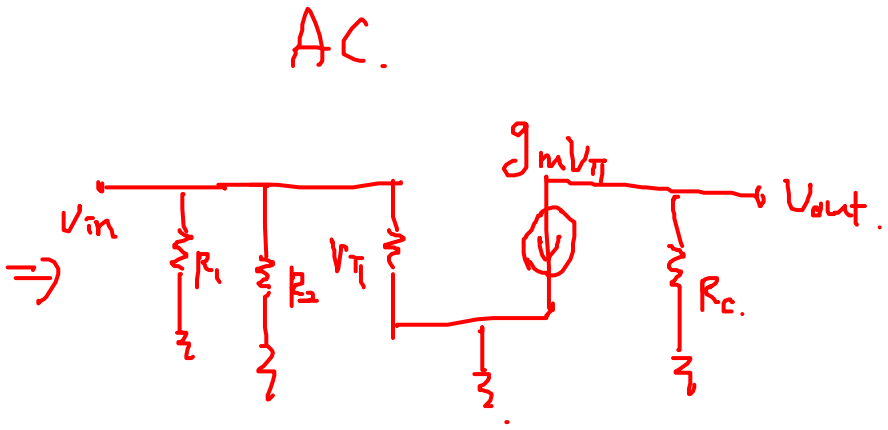
A series capacitor can be inserted to **isolate the dc biasing of the amplifier from the AC signal.**

The bias point of Q_1 remains independent of the resistance of the microphone (AC signal) because **C_1 carries no bias current (DC Open)**. The value of C_1 is chosen so that it provides a relatively low impedance for the frequencies of interest **(AC Short)**. C_1 is a **coupling capacitor** and the input of this stage is **ac-coupled** or **capacitively coupled**.

e.g.





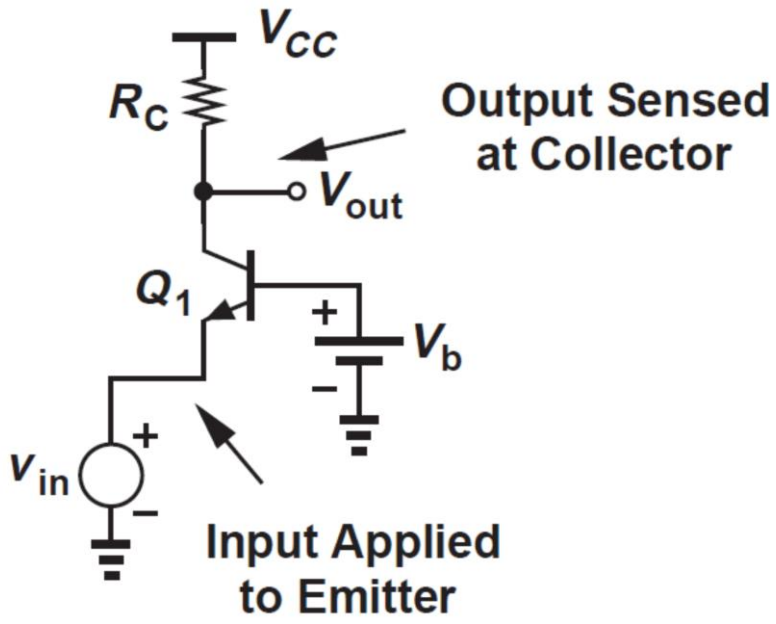


$$\frac{v_{out}}{v_{in}} = -g_m R_C$$

$$\mathrm{R_{in}} = r_\pi \| R_1 \| R_2$$

$$\mathrm{R_{out}} = R_C$$

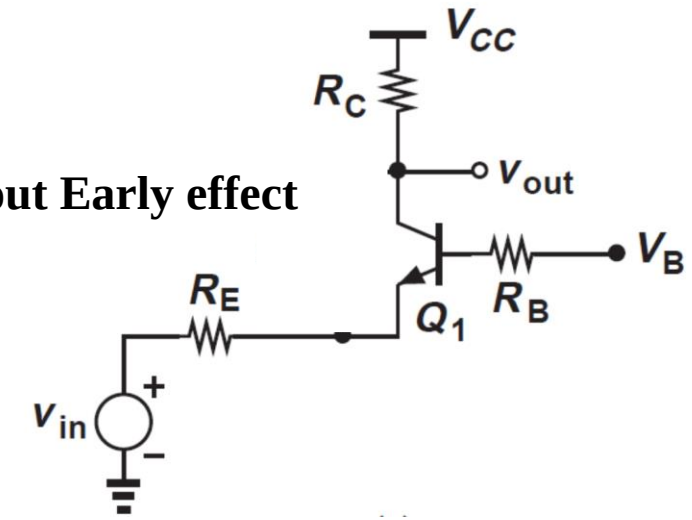
Common-Base (CB) Topology

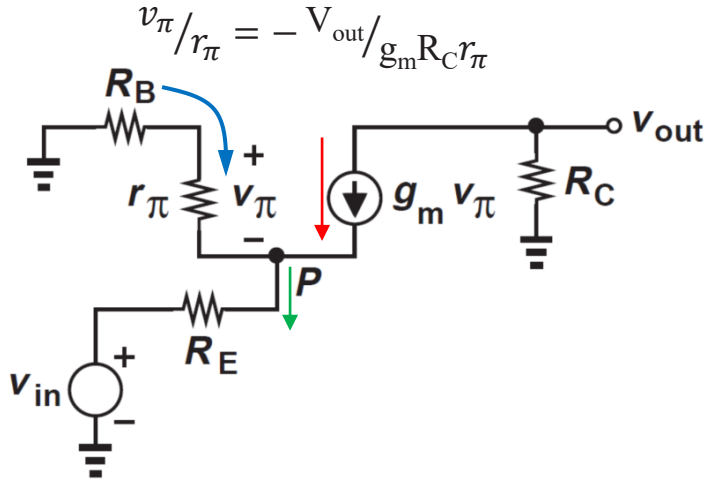


The input is applied to the emitter and the output is sensed at the collector. Biased at a proper voltage, **the base acts as ac ground** and hence as a node "common" to the input and output ports.

General case of the CB topology

Without Early effect



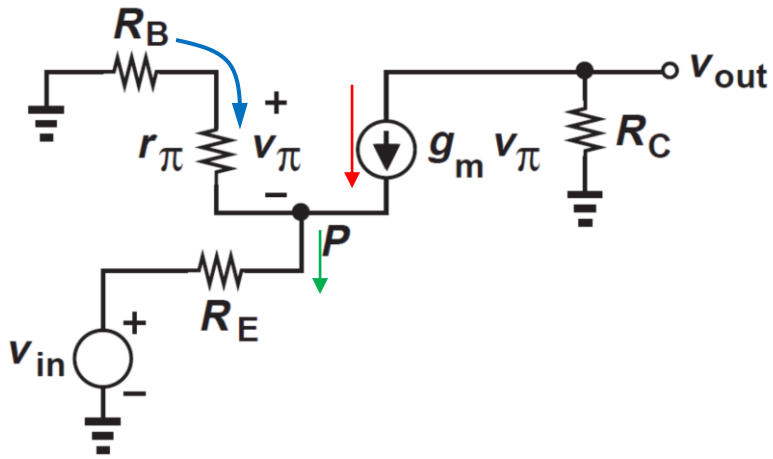


$v_{out} = -g_m v_\pi R_C \rightarrow v_\pi = -v_{out}/g_m R_C$

The current through the v_π node is $v_\pi/r_\pi = -v_{out}/g_m R_C r_\pi$

Therefore, voltage at node p is $v_p = v_{out}/g_m R_C r_\pi (R_B + r_\pi) = v_{out}/\beta R_C (R_B + r_\pi)$ $\quad *\boldsymbol{r_\pi = \frac{\beta}{g_m}}$

KCL at node P, we get $\frac{v_\pi}{r_\pi} + g_m v_\pi = \frac{v_p - v_{in}}{R_E}$



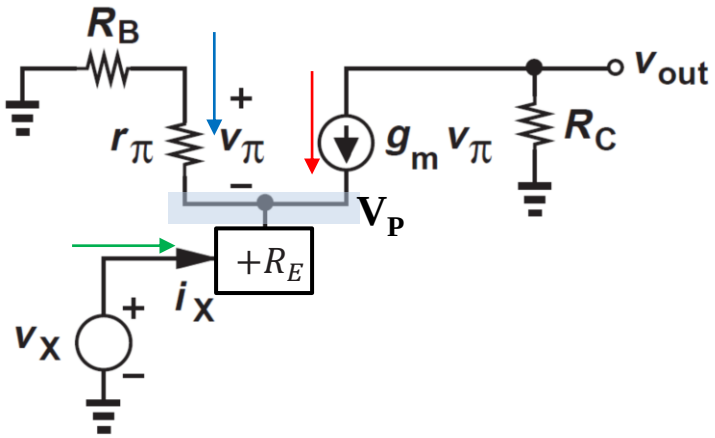
KCL at node P, we get $\frac{v_\pi}{r_\pi} + g_m v_\pi = \frac{v_p - v_{in}}{R_E}$(1)

where $v_\pi = -{}^{V_{out}}/_{g_m R_C}$ and $v_p = -{}^{V_{out}}/_{\beta R_C}\,(R_B + r_\pi)$.

Put v_π and v_p into the equation (1) and rearrange terms, we get

$$\frac{v_{out}}{v_{in}} = \frac{\beta R_C}{(\beta+1)R_E + R_B + r_\pi} \; or \; \approx \frac{R_C}{R_E + \frac{R_B}{\beta+1} + \frac{1}{g_m}}$$

Input Resistance of General CB Topology



$-v_\pi = \frac{r_\pi}{R_B + r_\pi} v_p, v_p = v_x - R_E i_x$

KCL at node P gives $\frac{v_\pi}{r_\pi} + i_x + g_m v_\pi = 0$

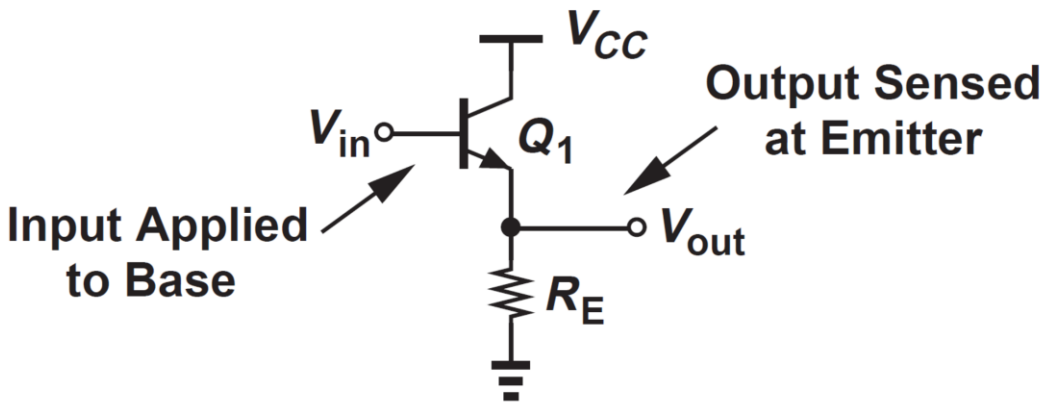
This results in $\left(\frac{1}{r_\pi} + g_m\right) v_\pi + i_x = 0$ where $-v_\pi = \frac{r_\pi}{R_B + r_\pi}(v_x - R_E i_x)$

$\left(\frac{1}{r_\pi} + g_m\right) \frac{r_\pi}{R_B + r_\pi}(v_x - R_E i_x) = i_x$ $\quad *\boldsymbol{r_\pi = \frac{\beta}{g_m}}$

$= 1+\beta$

Rearrange terms we get $\frac{v_x}{i_x} = \boldsymbol{R_E + \frac{R_B + r_\pi}{\beta + 1}}$ or without R_E (series R) $\frac{v_x}{i_x} = \frac{R_B}{\beta + 1} + \frac{1}{g_m}$

Emitter Follower

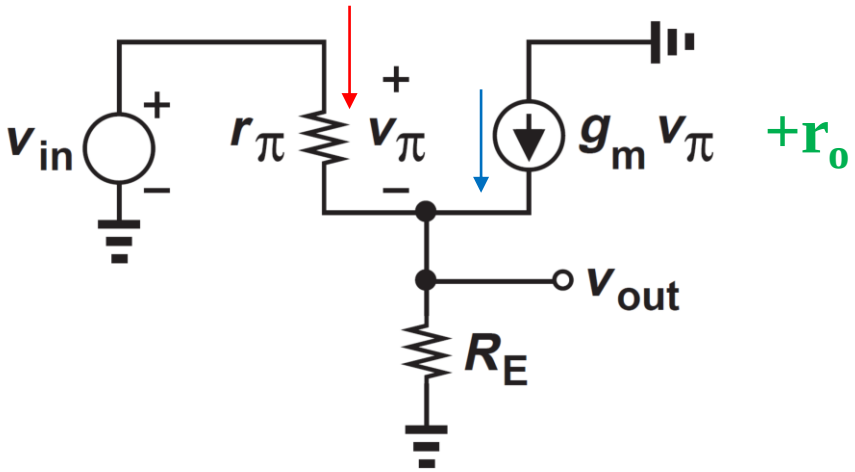


In an emitter follow circuit, V_{out} is always lower than V_{in} by an amount equal to V_{BE}, and the circuit is said to provide **level shift** and a **voltage gain less than unity**.

Even though the voltage gain is less than unity, the **input and output impedances** of the emitter follower make it a particularly useful circuit for some applications.

With Early effect

(1) Gain



By small signal analysis, the equivalent circuit yields

$$\frac{v_\pi}{r_\pi} + g_m v_\pi = \frac{v_{out}}{R_E} + \frac{v_{out}}{r_o}$$

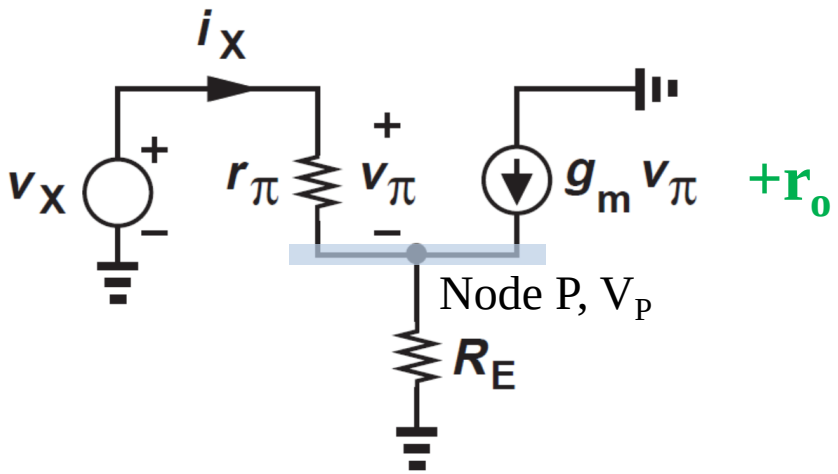
$$v_\pi = \frac{r_\pi}{\beta+1} \cdot \frac{v_{out}}{R_E \| r_o}$$

$$v_{in} = v_\pi + v_{out}$$

$$\frac{v_{out}}{v_{in}} = \frac{1}{1+\frac{r_\pi}{\beta+1}\cdot\frac{1}{R_E \| r_o}} \approx \frac{R_E \| r_o}{R_E \| r_o + \frac{1}{g_m}}$$

With Early effect

(2) Input Impedances



From the circuit above, we can derive

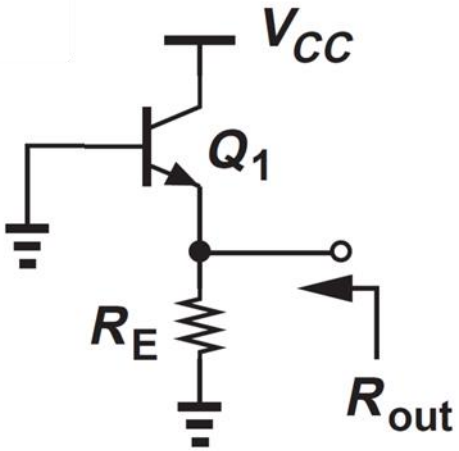
$v_\pi = i_X r_\pi$; $V_P = v_x - v_\pi = v_x - i_X r_\pi$

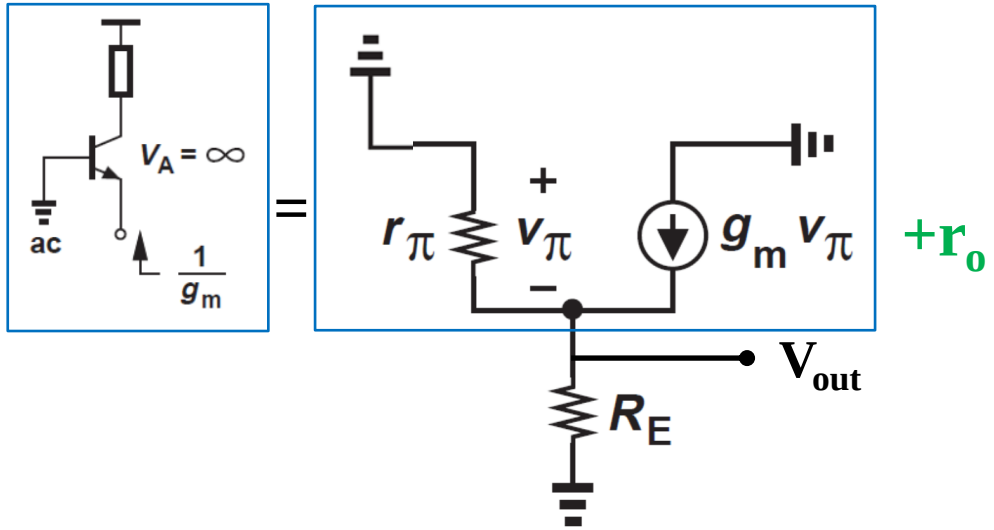
By KCL at node P, $i_X + g_m v_\pi = \frac{V_P}{R_E} + \frac{V_P}{r_o}$ where $\frac{1}{R_E} + \frac{1}{r_o} = \frac{1}{R_E \| r_o}$

$\rightarrow \boldsymbol{R_{in} = \frac{v_X}{i_X} = (1 + g_m r_\pi)(R_E \| r_o) + r_\pi = (1 + \beta)(R_E \| r_o) + r_\pi}$

With Early effect

(3) Output Impedances

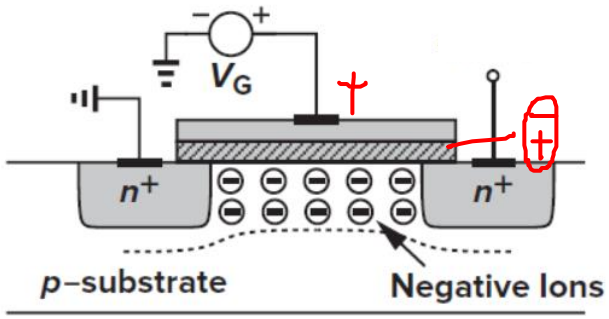


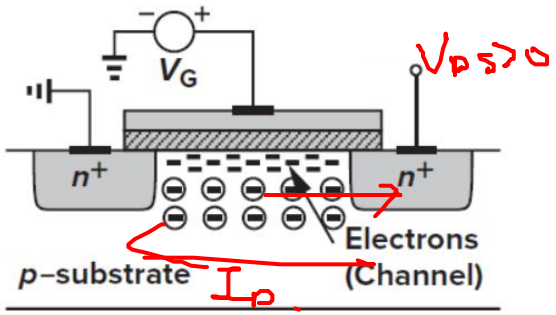


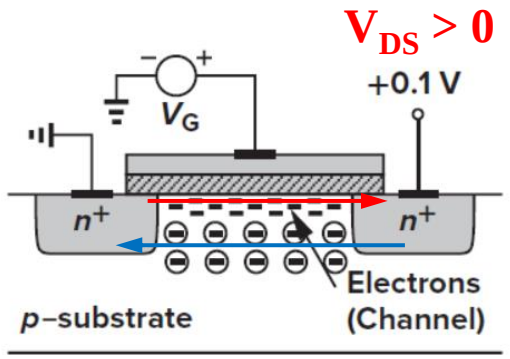
$$\boldsymbol{R_{out}} = \frac{1}{g_m} \| R_E \| \boldsymbol{r_o}$$

MOS I/V Characteristics

Assume we change V_G from negative to positive





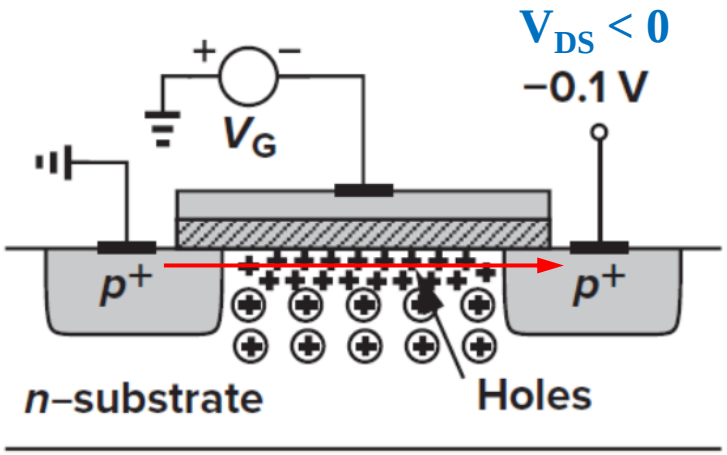


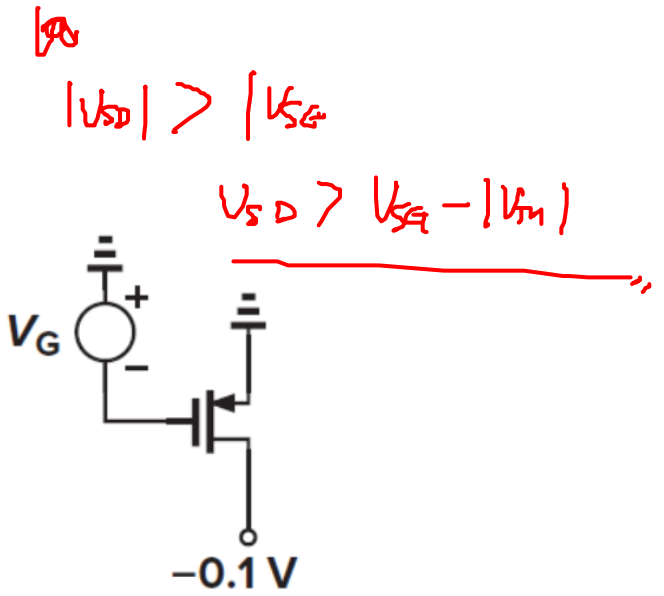
Electron direction

Drain current (I_D) direction

- By applying **positive V_{GS}**, electrons are induced in the channel, or holes are repelled from the channel, forming a **depletion region** at the interface between oxide and Si.
- When V_{GS} (> 0) is large enough, **a channel of electrons (inversion layer)** is formed at the interface.
- The value of V_{GS} at which the inversion layer forms is the **threshold voltage (V_{TH})**. The device turns on abruptly for $V_{GS} \geq V_{TH}$.
- **With the bias of V_{DS}**, electrons flow **from source to drain.**

Threshold Voltage (PMOS)



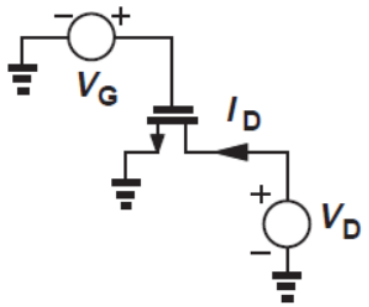


Hole and drain current (I_D) direction

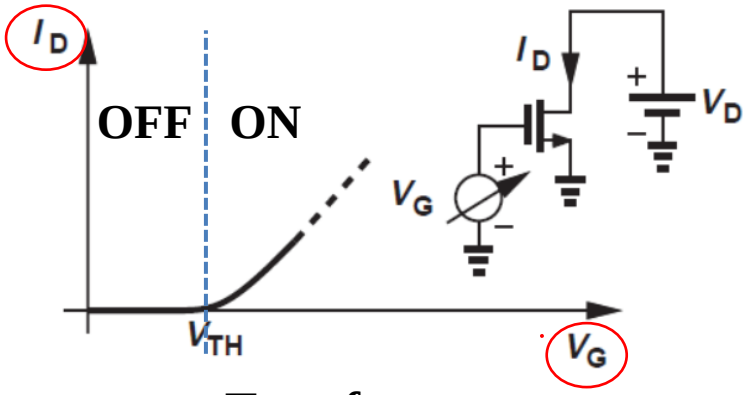
The turn-on phenomenon in a PMOS device is similar to that of NFETs, but with all the polarities reversed. If the $\mathbf{V_{GS}}$ **becomes sufficiently *negative***, an inversion layer consisting of holes is formed at the oxide-silicon interface, providing a conduction path between the source and the drain. $\mathbf{V_{TH}}$ **of PMOS < 0.**

Modes of MOSFET

(1) $V_{GS} < V_{TH}$: No channel exists, the **device is off**, and $I_D = 0$ regardless of the value of V_{DS}.
(2) $V_{GS} > V_{TH}$: The channel is formed. With $V_{DS} > 0$, the **device is on** and there is $I_D > 0$.

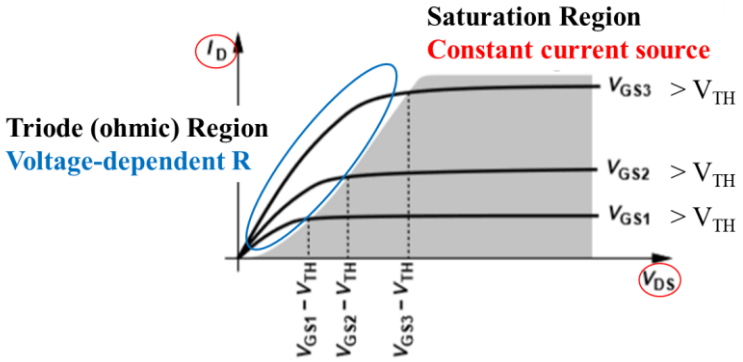


MOSFET Bias: V_{GS} and V_{DS}



Transfer curve

By varying V_{GS} at fixed V_{DS}

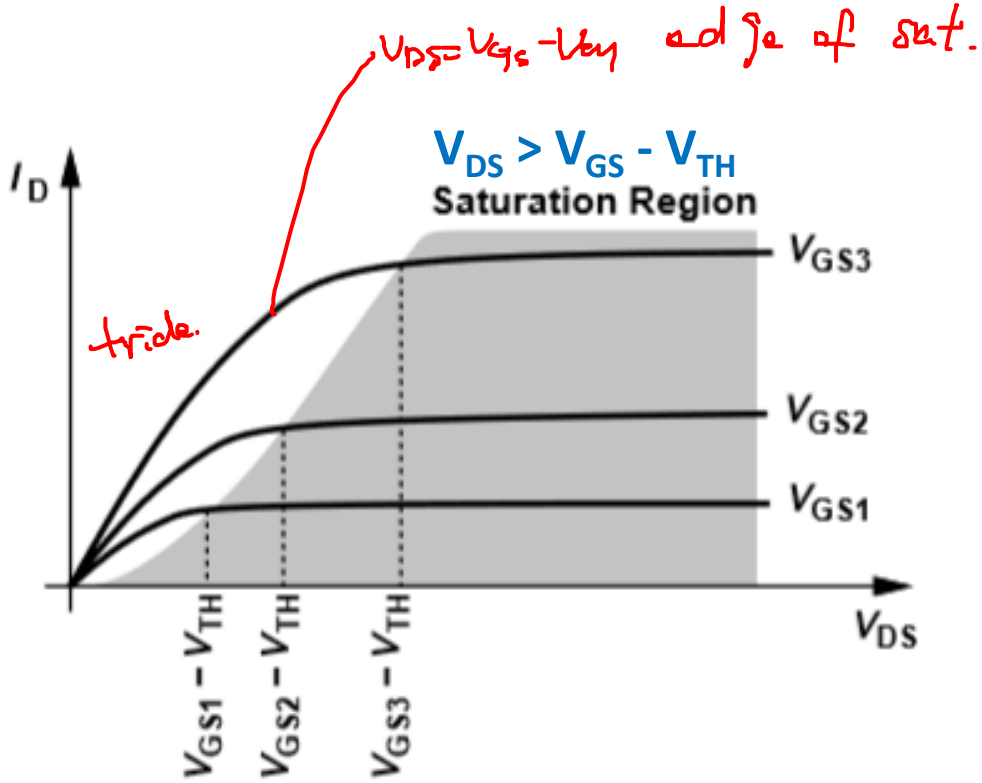


Output curve

By varying V_{DS} at fixed V_{GS}

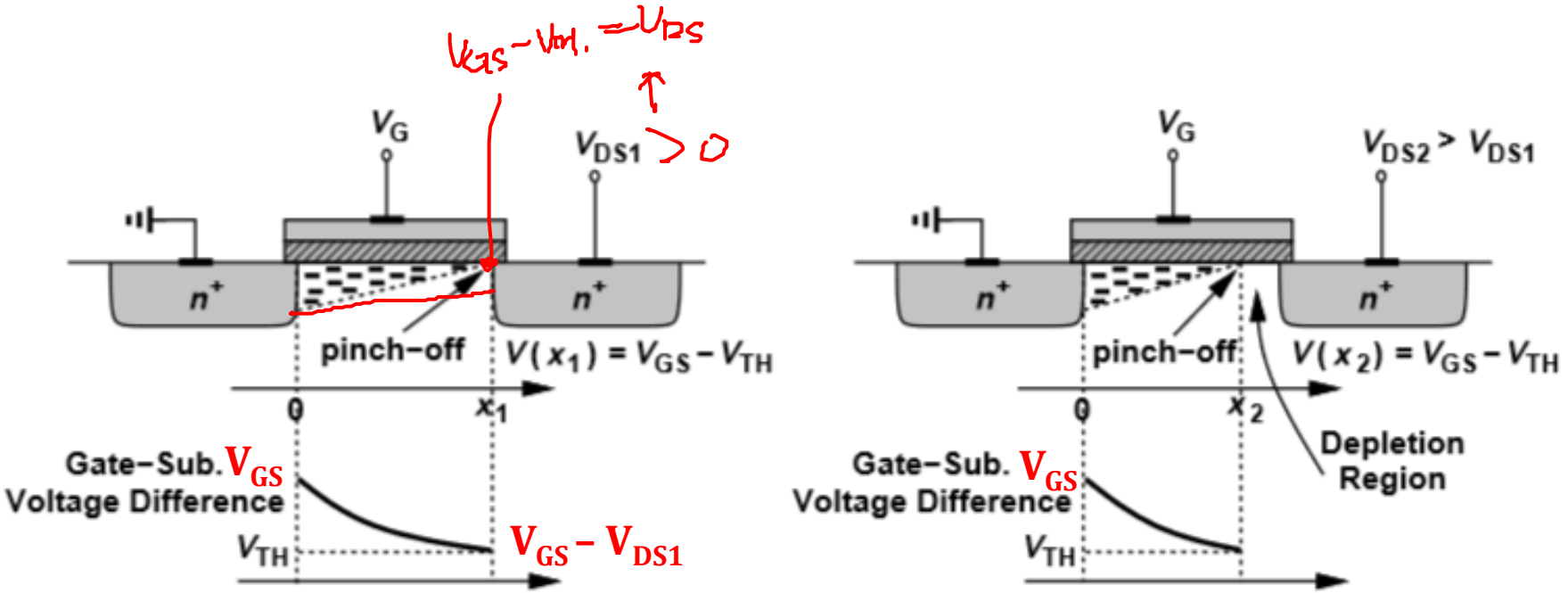
In an output curve of MOSFET, we can determine two modes (regions): **(1) Triode or ohmic region and (2) saturation region.**

Saturation Region

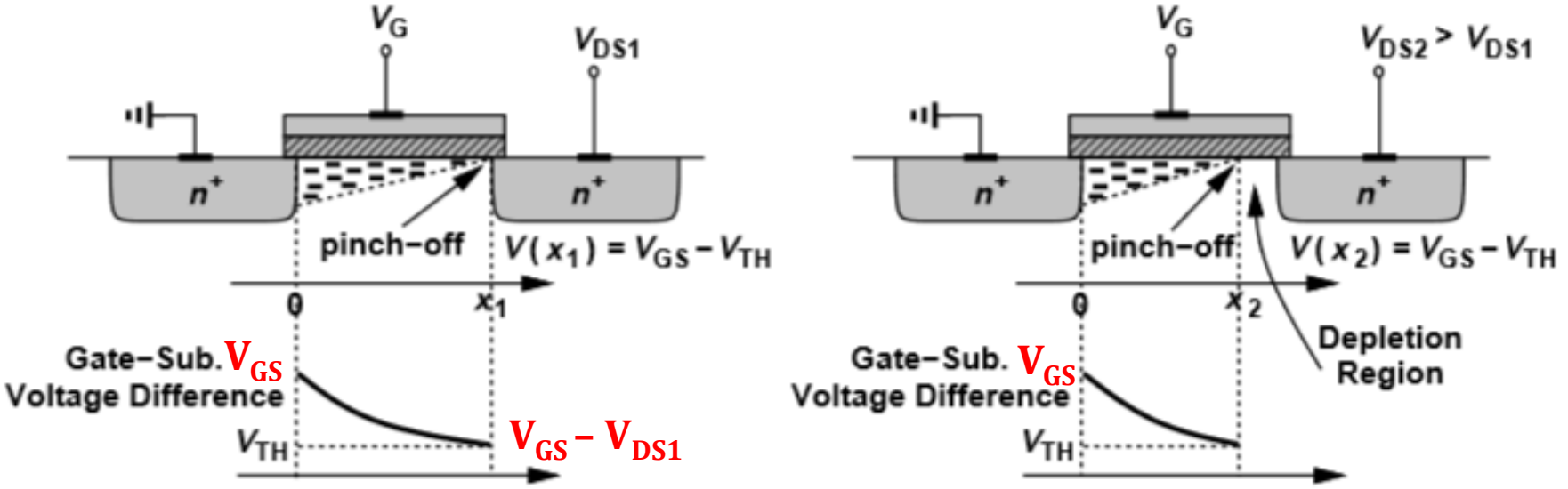


When the $V_{DS} > V_{GS} - V_{TH}$, the drain current does not follow the parabolic behavior. In fact, I_D becomes relatively constant and the device operates in the **saturation region**.

$V_{DS} = V_{GS} - V_{TH}$ is the minimum value for the NMOS to operate in saturation region.
For **$V_{DS} > V_{GS} - V_{TH}$**, I_D becomes relatively constant.



The local density of the inversion-layer charge is proportional to $V_{GS} - V(x) - V_{TH}$. Thus, if V(x) approaches $V_{GS} - V_{TH}$, then $Q_d(x)$ drops to zero. In other words, if V_{DS} is slightly greater than $V_{GS} - V_{TH}$, then the inversion layer stops at $x \leq L$, and the channel is **pinched off**. As V_{DS} increases further, **the point at which Q_d equals zero gradually moves toward the source**.

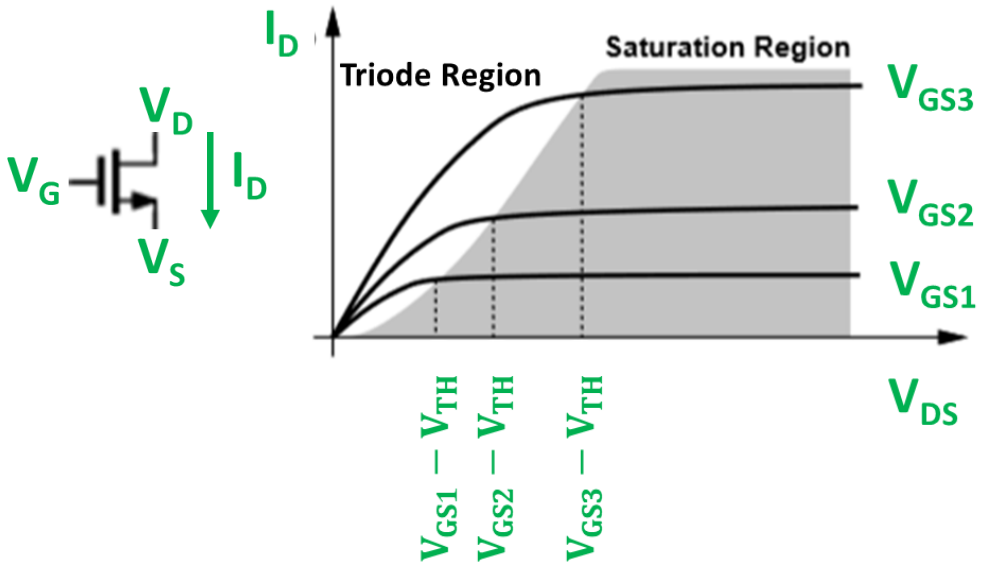


When $V_{DS} = V_{GS} - V_{TH}$, the saturation occurs. Thus, substitute V_{DS} with $V_{GS} - V_{TH}$ then

$$I_D = \mu_n C_{ox} \frac{W}{L_{eff}} \left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right] \rightarrow I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L'}(V_{GS} - V_{TH})^2$$

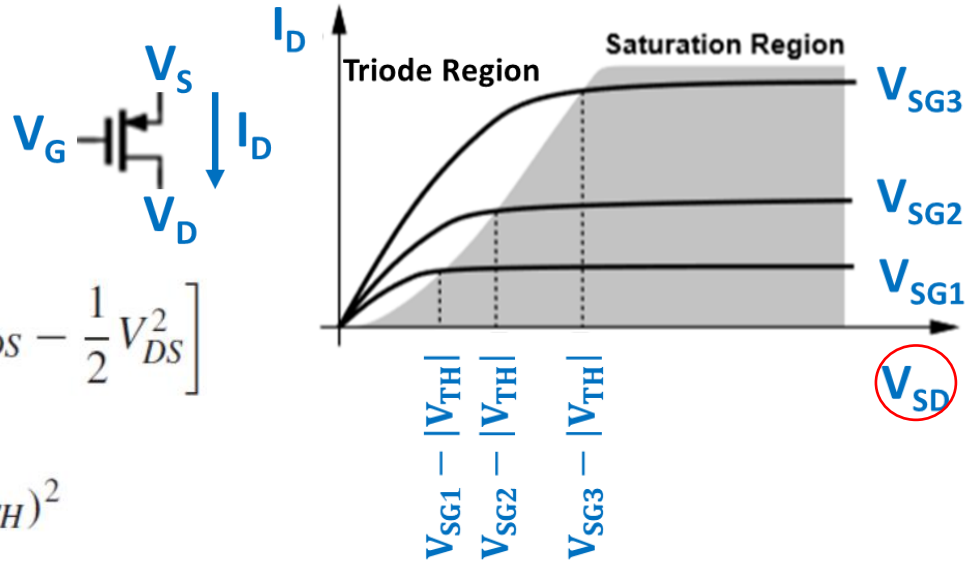
L': the point at which Q_d drops to zero

NMOS *vs* PMOS



Triode region: $I_D = \mu_n C_{ox} \frac{W}{L_{eff}} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} {V_{DS}}^2 \right]$

Saturation region: $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L'} (V_{GS} - V_{TH})^2$

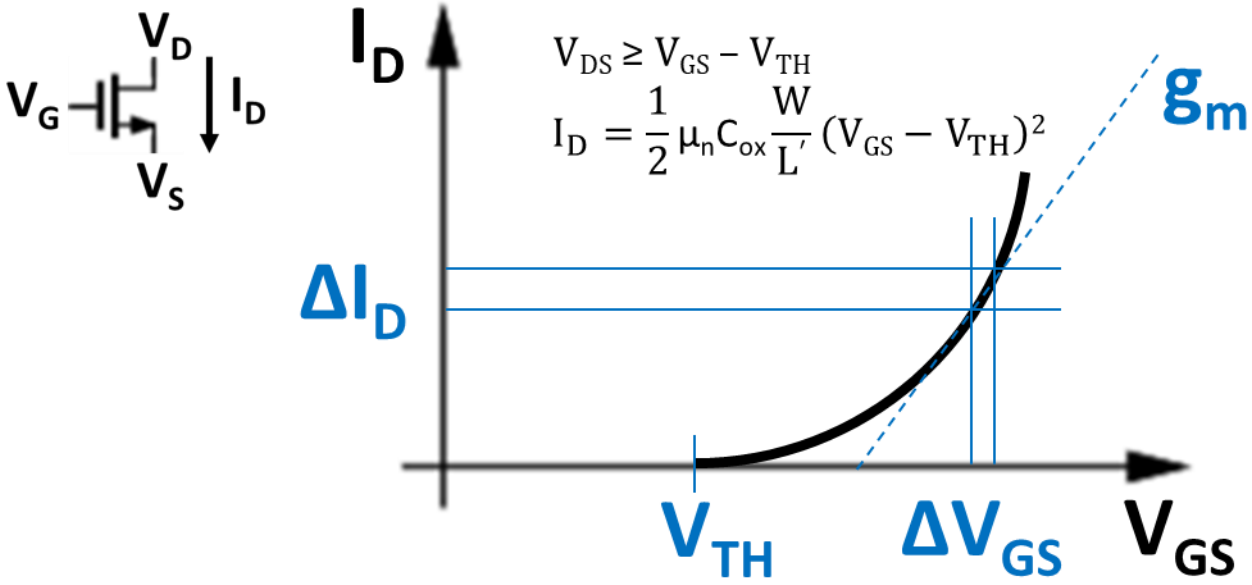


Triode region: $I_D = -\mu_p C_{ox} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$

Saturation region: $I_D = -\frac{1}{2} \mu_p C_{ox} \frac{W}{L'} (V_{GS} - V_{TH})^2$

Transconductance

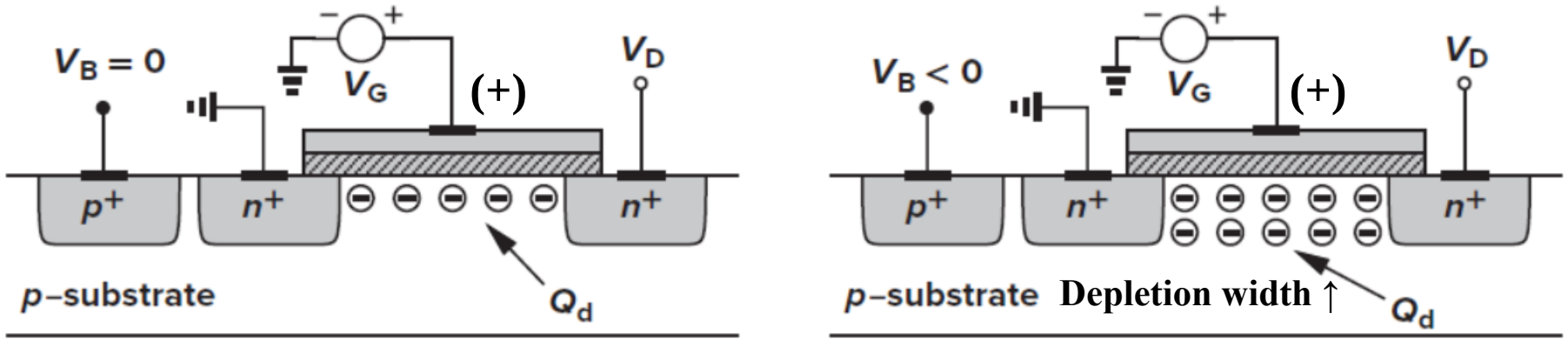
Transconductance (g_m) indicates how well a device converts a voltage to a current. Transconductance is usually defined in the saturation region.



$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox}\frac{W}{L'}(V_{GS} - V_{TH}) = \sqrt{2\mu_n C_{ox}\frac{W}{L'}I_D} = \frac{2I_D}{V_{GS} - V_{TH}}$$

Second-Order Effects

Body Effect



$$V_{TH} = V_{TH0} + \gamma(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|})$$

As V_B **or** V_{BS} **becomes more negative (**$V_{SB} > 0$**)**, more holes are attracted to the substrate connection, **leaving a larger negative charge behind**. the depletion region becomes wider.

More depletion charge (bound charge) $Q_d \uparrow \rightarrow$ V_{TH} **increases**

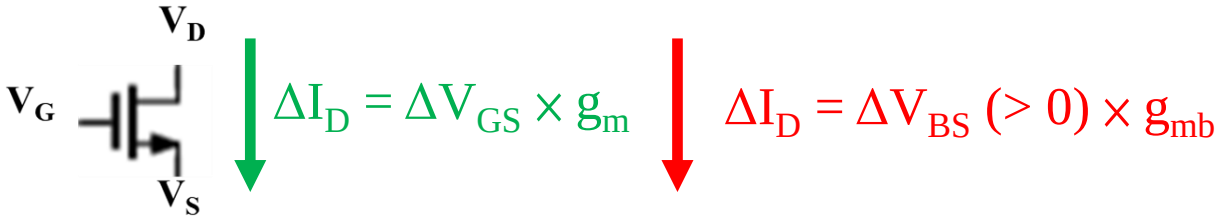
$$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}}$$

For the transconductance,

$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} \left(= -\frac{\partial I_D}{\partial V_{SB}}\right) = \frac{\partial I_D}{\partial V_{TH}} \cdot \frac{\partial V_{TH}}{\partial V_{BS}}$$

$$= -\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) \cdot \frac{\partial V_{TH}}{\partial V_{BS}}$$

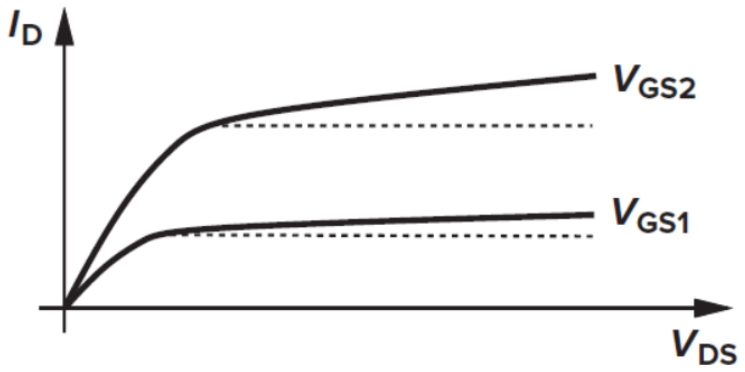
$$= \mathbf{g_m \cdot \eta}$$



- V_{GS} positively increases, I_D increases.
- V_{BS} positively increases, i.e. V_{SB} negatively increases, V_{TH} decreases and thus I_D increases.

Channel-Length Modulation

The actual length of the channel gradually decreases as the potential difference between the gate and the drain decreases. L is in fact a function of V_{DS}.



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}(V_{GS} - V_{TH})^2$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS} - V_{TH})^2\left(1 + \frac{\Delta L}{L_{eff}}\right)$$

$$= \boldsymbol{\frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})}$$

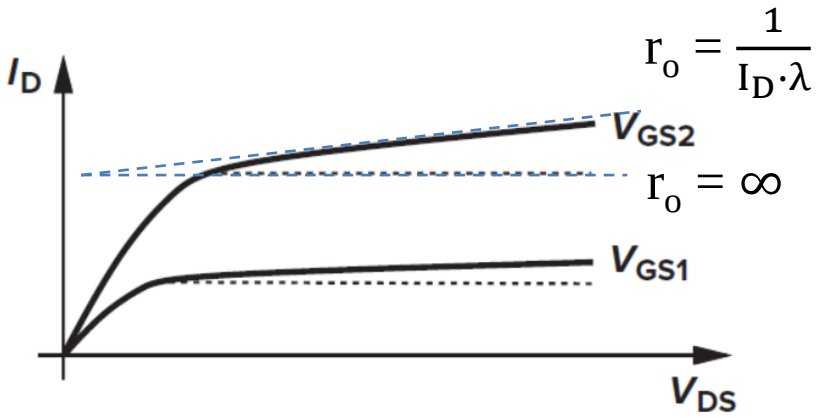
With the channel-length modulation,

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})$$

$$\mathbf{g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS} - V_{TH})(1 + \lambda V_{DS})}$$

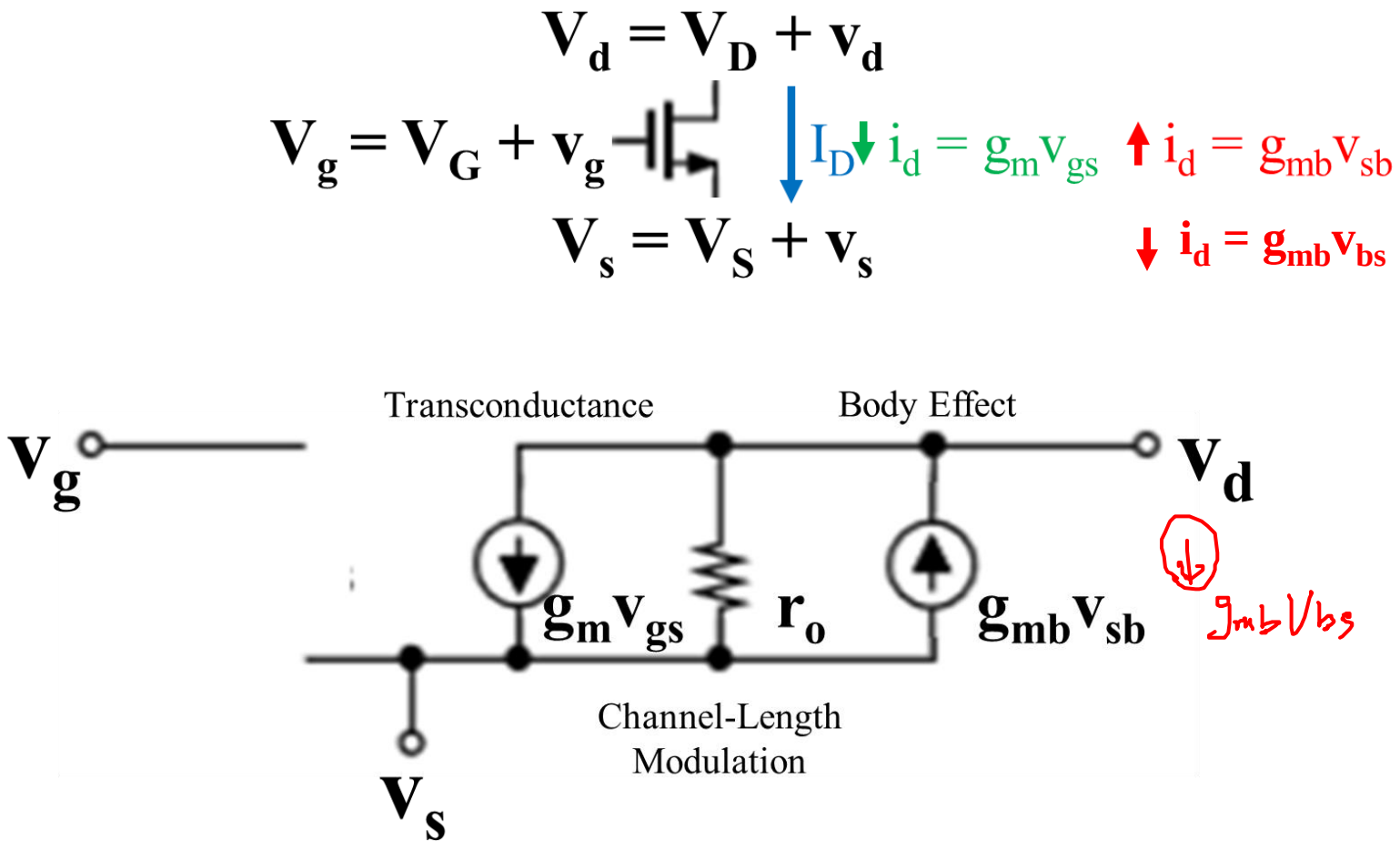
$$\mathbf{r_o} = \frac{\partial V_{DS}}{\partial I_D} = 1/\frac{\partial I_D}{\partial V_{DS}} = \frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \cdot \lambda}$$

$$\approx \mathbf{\frac{1}{I_D \cdot \lambda}}$$



Channel-length modulation is reflected in g_m and r_o by λ

Small-Signal Model for NMOS



Small-Signal Model for PMOS

$$V_s = V_S + v_s$$

$$V_g = V_G + v_g$$

$$V_d = V_D + v_d$$