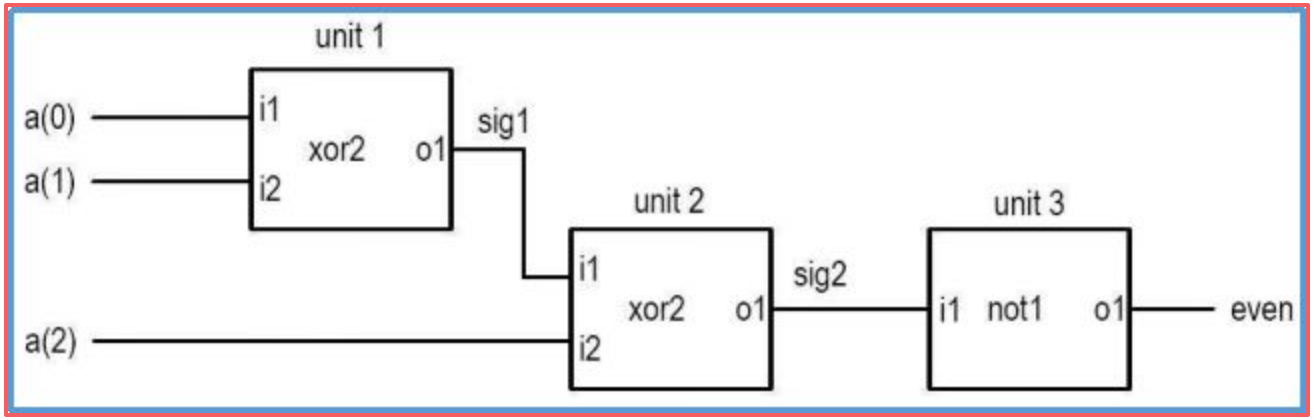
VHDL Basics

Δαδαλιάρης Αντώνιος
dadaliaris@cs.uth.gr

VHDL: Structural Description



VHDL: Structural Description (cont.)

test.vhd

```
1  LIBRARY ieee;
2  USE ieee.std_logic_1164.ALL;
3
4  ENTITY xor2 IS
5  PORT(
6     i1, i2: IN STD_LOGIC;
7     o1: OUT STD_LOGIC
8  );
9  END xor2;
10
11 ARCHITECTURE arch OF xor2 IS
12 BEGIN
13    o1 <= i1 xor i2;
14 END arch;
15
```

test2.vhd

```
1  LIBRARY ieee;
2  USE std_logic_1164.ALL;
3
4  ENTITY not1 IS
5  PORT(
6     i1: IN STD_LOGIC;
7     o1: OUT STD_LOGIC
8  );
9  END not1;
10
11 ARCHITECTURE arch OF not1 IS
12 BEGIN
13    o1 <= NOT i1;
14 END arch;
15
```

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VHDL: Structural Description (cont.)

test.vhd

```
1   LIBRARY ieee;
2   USE ieee.std_logic_1164.ALL;
3
4   ENTITY circ IS
5   PORT(
6      a0, a1, a2: IN STD_LOGIC;
7      o1: OUT STD_LOGIC
8   );
9   END circ;
10
11  ARCHITECTURE str_arch OF circ IS
12  COMPONENT xor2
13  PORT(
14     i1, i2: IN STD_LOGIC;
15     o1: OUT STD_LOGIC
16  );
```

test.vhd

```
18
19  COMPONENT not1
20  PORT(
21     i1: IN STD_LOGIC;
22     o1: OUT STD_LOGIC
23  );
24  END COMPONENT;
25
26  SIGNAL sig1, sig2: STD_LOGIC;
27
28  BEGIN
29  unit1: xor2 PORT MAP(a0, a1, sig1);
30  unit2: xor2 PORT MAP(a2, sig1, sig2);
31  unit3: not1 PORT MAP(sig2, o1);
32  END str_arch;
33
```

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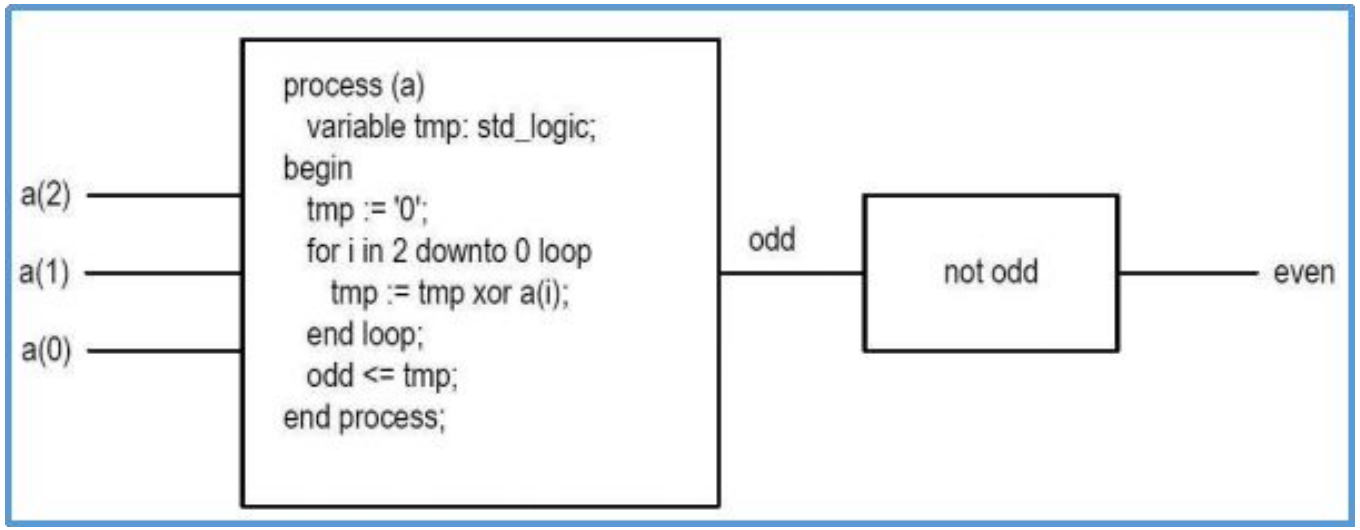
VHDL: Behvioral Description



VHDL: Behavioral Description (cont.)

test.vhd

```
1   LIBRARY ieee;
2   USE ieee.std_logic_1164.ALL;
3
4   ENTITY circ IS
5   PORT(
6      a: IN STD_LOGIC_VECTOR(2 DOWNTO 0);
7      o1: OUT STD_LOGIC
8   );
9   END circ;
10
11  ARCHITECTURE beh_arch OF circ IS
12  SIGNAL odd: STD_LOGIC;
13  BEGIN
14     o1 <= NOT odd;
15     PROCESS(a)
16        VARIABLE temp:= '0';
```

test.vhd

```
11  ARCHITECTURE beh_arch OF circ IS
12  SIGNAL odd: STD_LOGIC;
13  BEGIN
14     o1 <= NOT odd;
15     PROCESS(a)
16        VARIABLE temp:= '0';
17        BEGIN
18        tmp:= '0';
19        FOR i IN 2 DOWNTO 0 LOOP
20           tmp:= tmp XOR a(i);
21        END LOOP;
22
23        odd <= tmp;
24     END PROCESS;
25  END beh_arch;
26
```

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VHDL: Simulating a Design using ModelSim

- **CAD Tool:**
  - www.altera.com
  - MoselSim Altera Starter Edition / Student Edition

VHDL: Simulating a Design using ModelSim

- **Overall Process:**
  - Change Directory
  - Library Declaration
  - Library Mapping
  - Compilation
  - Simulation
  - Waveform Generation

VHDL: Simulating a Design using ModelSim (cont.)

- **Overall Process:**
  - Change Directory
    - *Console Command: cd:/path/*
  - Library Declaration
  - Library Mapping
  - Compilation
  - Simulation
  - Waveform Generation

VHDL: Simulating a Design using ModelSim

- **Overall Process:**
  - Change Directory
  - Library Declaration
    - *Console Command: vlib work*
  - Library Mapping
  - Compilation
  - Simulation
  - Waveform Generation

VHDL: Simulating a Design using ModelSim

- **Overall Process:**
  - Change Directory
  - Library Declaration
  - Library Mapping
    - *Console Command: vmap work work*
  - Compilation
  - Simulation
  - Waveform Generation

VHDL: Simulating a Design using ModelSim

- **Overall Process:**
  - Change Directory
  - Library Declaration
  - Library Mapping
  - Compilation
    - *Console Command: vcom file_name.vhd*
  - Simulation
  - Waveform Generation

VHDL: Simulating a Design using ModelSim

- **Overall Process:**
  - Change Directory
  - Library Declaration
  - Library Mapping
  - Compilation
  - Simulation
    - *Console Command: vsim entity_name*
  - Waveform Generation

VHDL: Simulating a Design using ModelSim

- **Overall Process:**
  - Change Directory
  - Library Declaration
  - Library Mapping
  - Compilation
  - Simulation
  - Waveform Generation
    - *Console Command: add wave **
    - *Console Command: force input_name value*
    - *Console Command: run time*