

VHDL Basics

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Introduction

- VHDL is a language used to describe digital circuits.
- VHDL stands for: Very High Speed Integrated Circuit Hardware Description Language
- Designs described in VHDL can be compiled, simulated and translated to a format suitable for hardware implementation.

Terminology

- Simulation
- Synthesis
- Field Programmable Gate Arrays (FPGAs)
- Application Specific Integrated Circuits (ASICs)

Terminology (cont.)

- Simulation
 - Predict the behavior of a design
 - Functional Simulation
 - Approximate behavior
 - Timing Simulation
 - Exact behavior

Terminology (cont.)

- Synthesis
 - Generation of a netlist file that describes the structure of a digital design.
 - VHDL is used at a previous state of the overall design flow
 - Not all VHDL statements are synthesizable.

Terminology (cont.)

- Field Programmable Gate Arrays (FPGAs)
 - Programmable devices
 - Rapid prototyping for almost any digital design
 - Creation of designs whose purpose is the generation of an input bitstream file that configures other devices

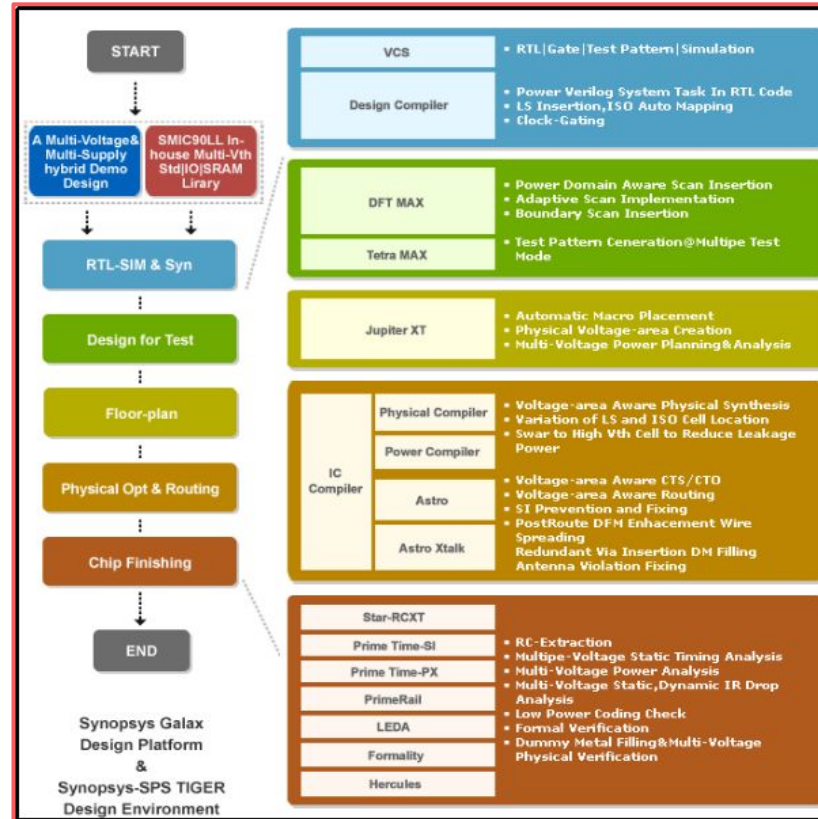
Terminology (cont.)

- Application Specific Integrated Circuits (ASICs)
 - Custom designs that implement a specific application
 - Custom capability
 - Lower unit cost
 - Smaller size

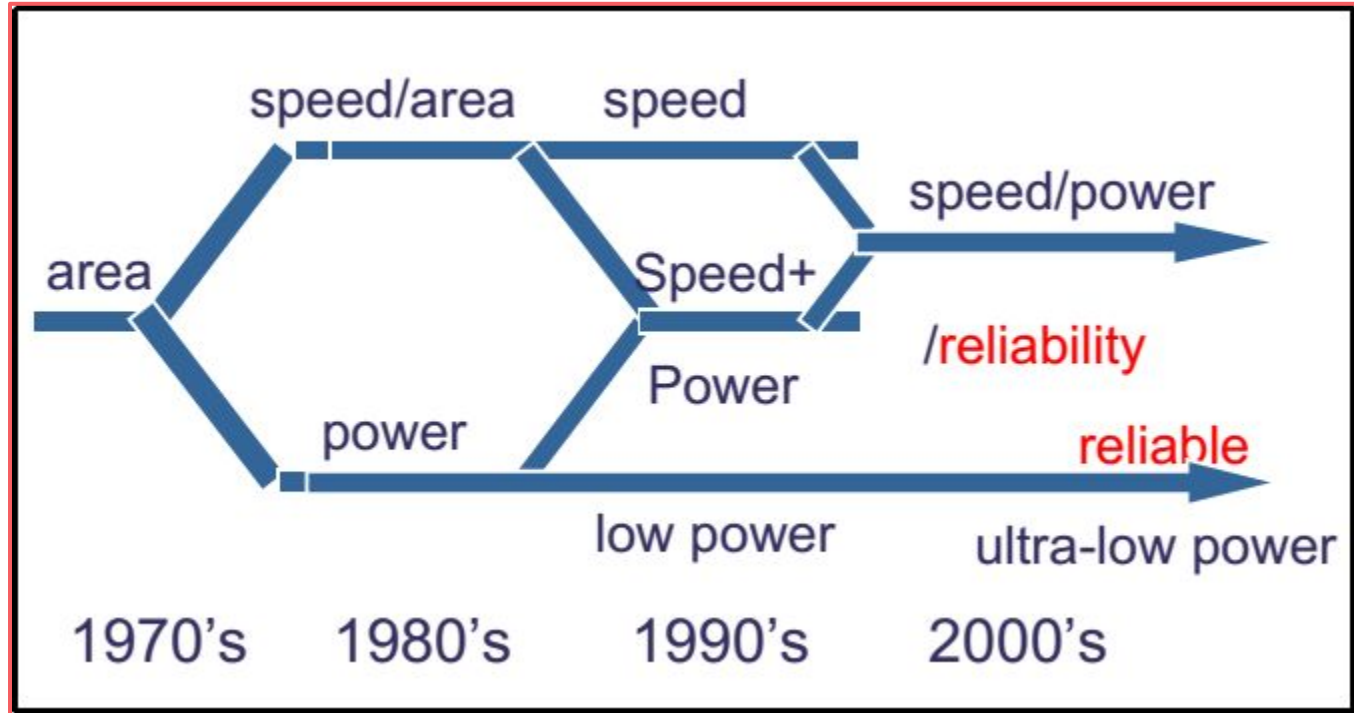
ASIC Design Flow

1. Design Specification
2. HDL Coding
3. Simulation
4. Synthesis (Design for Testability, Timing Analysis, Power Analysis, Equivalency Checking)
5. Post-Synthesis Simulation
6. Place & Route (Timing Analysis, Power Analysis, Equivalence Checking)
7. Post-Place & Route Simulation
8. Chip-Finishing / Tapeout

ASIC Design Flow (cont.)



Design Goals



Hardware Description Languages (HDLs)

- Most used HDLs: VHDL & Verilog
 - Different Syntax
 - Similar Capabilities
 - Supported by every industrial design tool
- Advantages:
 - Portability
 - Reusability
 - Standard Language - Structured Language
 - Technology Independent

VHDL References

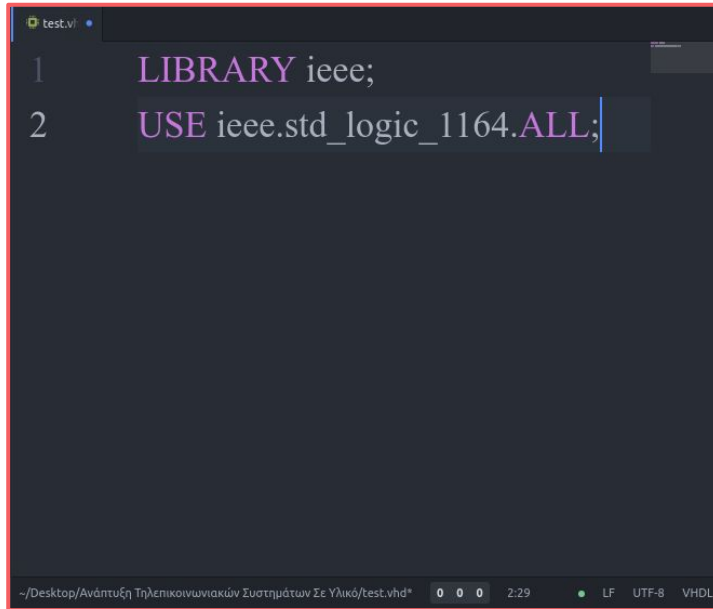
- Books:
 - Douglas Perry, “VHDL”, McGraw Hill
 - Peter J. Ashenden, “The Designer’s Guide to VHDL”, Morgan Kaufmann Publishers
 - Stephen Brown & Svonko Vranesic, “Fundamentals of Digital Logic with VHDL”, McGraw Hill

VHDL: Libraries & Packages

- Libraries:
 - Packages
 - Components
 - Functions
 - Procedures
- Packages:
 - Mainly data types

VHDL: Libraries & Packages cont.

- Libraries and packages are the first declarations that we include in any VHDL code.

A screenshot of a code editor window titled 'test.vi'. The editor has a dark background with light-colored text. Two lines of VHDL code are visible: '1 LIBRARY ieee;' and '2 USE ieee.std_logic_1164.ALL;'. The code is syntax-highlighted, with 'LIBRARY' and 'USE' in purple, 'ieee' in blue, and 'std_logic_1164.ALL' in green. A blue cursor is positioned at the end of the second line. The status bar at the bottom shows the file path '~/.Desktop/Ανάπτυξη Τηλεπικοινωνιακών Συστημάτων Σε Υλικό/test.vhd*', three zeros, the time '2:29', and encoding details 'LF UTF-8 VHDL'.

```
1 LIBRARY ieee;
2 USE ieee.std_logic_1164.ALL;
```

VHDL: Entities, Architectures & Configurations

- All VHDL designs provide an external interface and an internal implementation.
- Any VHDL design consists of an entity, one or more architectures and zero or one configuration.

VHDL: Entities

- The entity of a VHDL design is practically its external interface.
- Entity declarations specify the following:
 - Name of the entity
 - Port declarations (practically the inputs and output of the design)
- It must be noted that generic declarations can be used but are optional.

VHDL: Entities (cont.)

```
test.vhdl
1  ENTITY entity_name IS
2  GENERIC(
3      generic_1_name : generic_1_type;
4      generic_2_name : generic_2_type;
5      generic_n_name : generic_n_type
6  );
7  PORT(
8      port_1_name : port_1_dir port_1_type;
9      port_2_name : port_2_dir port_2_type;
10     port_n_name : port_n_dir port_n_type
11 );
12 END entity_name;
```

~/Desktop/Ανάπτυξη Τηλεπικοινωνιακών Συστημάτων Σε Υλικό/test.vhd* 0 0 0 12:17 LF UTF-8 VHDL

VHDL: Entities (cont.)

```
test.vhd
1  --AND GATE ENTITY DECLARATION
2  ENTITY and_gate IS
3  PORT(
4    inp1: IN STD_LOGIC;
5    inp2: IN STD_LOGIC;
6    out1: OUT STD_LOGIC
7  );
8  END and_gate;
9
```

~/Desktop/Ανάπτυξη Τηλεπικοινωνιακών Συστημάτων Σε Υλικό/test.vhd 0 0 0 9:1 LF UTF-8 VHDL

VHDL: Ports

- Port names:
 - Letters, digits and/or underscores
 - All port names must start with a letter
 - Case insensitive
- Port types:
 - IN
 - OUT
 - INOUT
 - BUFFER