VHDL Basics

Δαδαλιάρης Αντώνιος
dadaliaris@cs.uth.gr

Introduction

- VHDL is a language used to describe digital circuits.
- VHDL stands for: Very High Speed Integrated Circuit Hardware Description Language
- Designs described in VHDL can be compiled, simulated and translated to a format suitable for hardware implementation.

Terminology

- Simulation
- Synthesis
- Field Programmable Gate Arrays (FPGAs)
- Application Specific Integrated Circuits (ASICs)

Terminology (cont.)

- Simulation
  - Predict the behavior of a design
  - Functional Simulation
    - Approximate behavior
  - Timing Simulation
    - Exact behavior

Terminology (cont.)

- Synthesis
  - Generation of a netlist file that describes the structure of a digital design.
    - VHDL is used at a previous state of the overall design flow
    - Not all VDHL statements are synthesizable.

Terminology (cont.)

- Field Programmable Gate Arrays (FPGAs)
  - Programmable devices
  - Rapid prototyping for almost any digital design
  - Creation of designs whose purpose is the generation of an input bitstream file that configures other devices

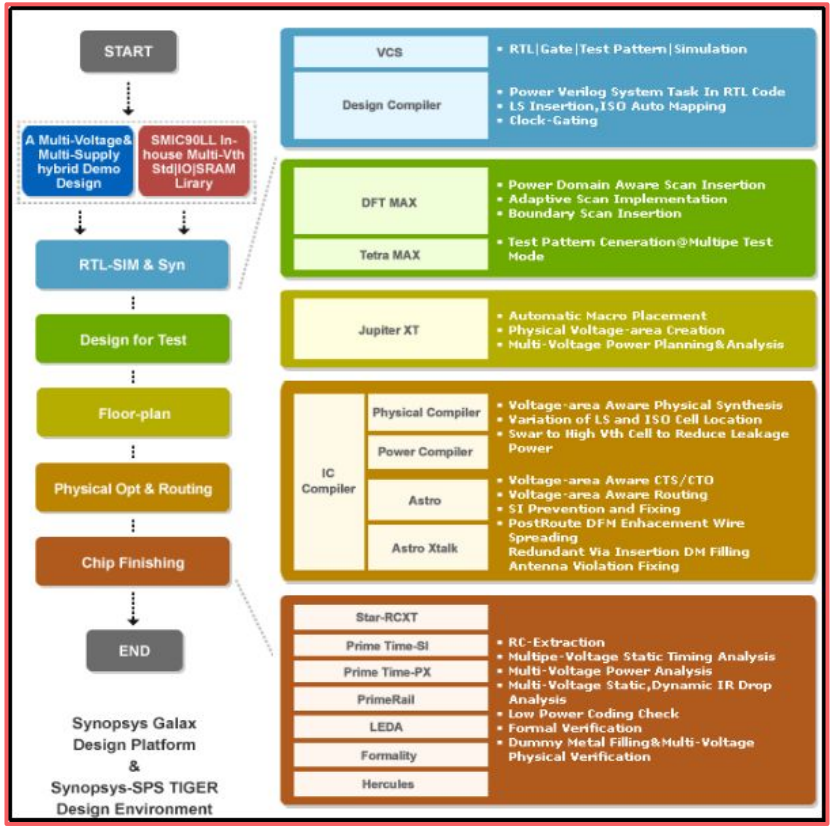
Terminology (cont.)

- Application Specific Integrated Circuits (ASICs)
  - Custom designs that implement a specific application
  - Custom capability
  - Lower unit cost
  - Smaller size

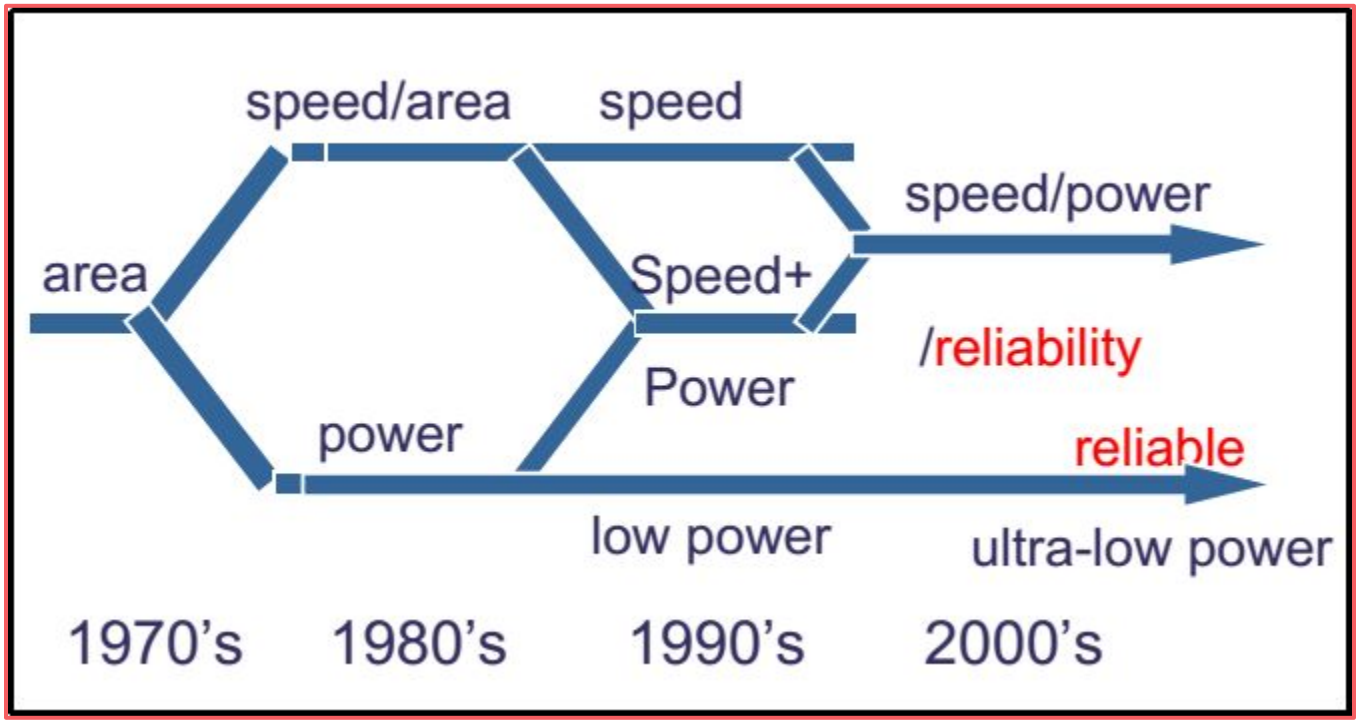
ASIC Design Flow

1. Design Specification
2. HDL Coding
3. Simulation
4. Synthesis (Design for Testability, Timing Analysis, Power Analysis, Equivalency Checking)
5. Post-Synthesis Simulation
6. Place & Route (Timing Analysis, Power Analysis, Equivalence Checking)
7. Post-Place & Route Simulation
8. Chip-Finishing / Tapeout

ASIC Design Flow (cont.)



Design Goals



Hardware Description Languages (HDLs)

- Most used HDLs: VHDL & Verilog
  - Different Syntax
  - Similar Capabilities
  - Supported by every industrial design tool
- Advantages:
  - Portability
  - Reusability
  - Standard Language - Structured Language
  - Technology Independent

VHDL References

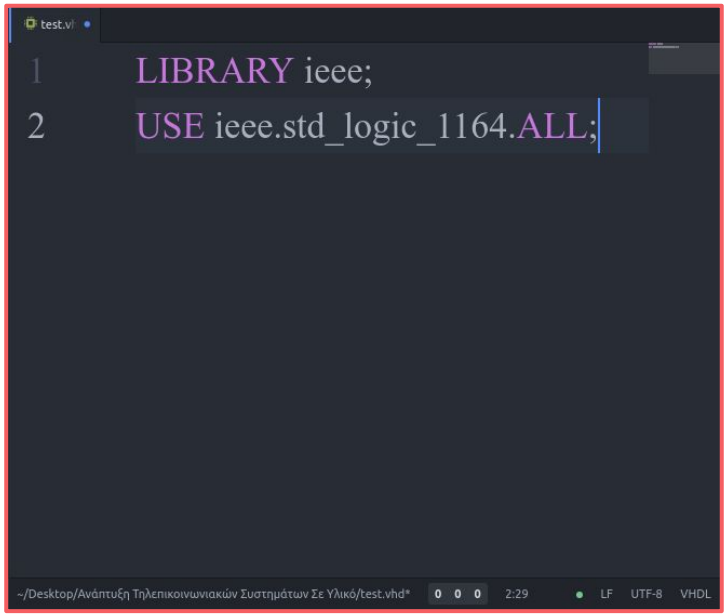
- Books:
  - Douglas Perry, “VHDL”, McGraw Hill
  - Peter J. Ashenden, “The Designer’s Guide to VHDL”, Morgan Kaufmann Publishers
  - Stephen Brown & Svonko Vranesic, “Fundamentals of Digital Logic with VHDL”, McGraw Hill

VHDL: Libraries & Packages

- Libraries:
  - Packages
  - Components
  - Functions
  - Procedures
- Packages:
  - Mainly data types

VHDL: Libraries & Packages cont.

- Libraries and packages are the first declarations that we include in any VHDL code.



VHDL: Entities, Architectures & Configurations

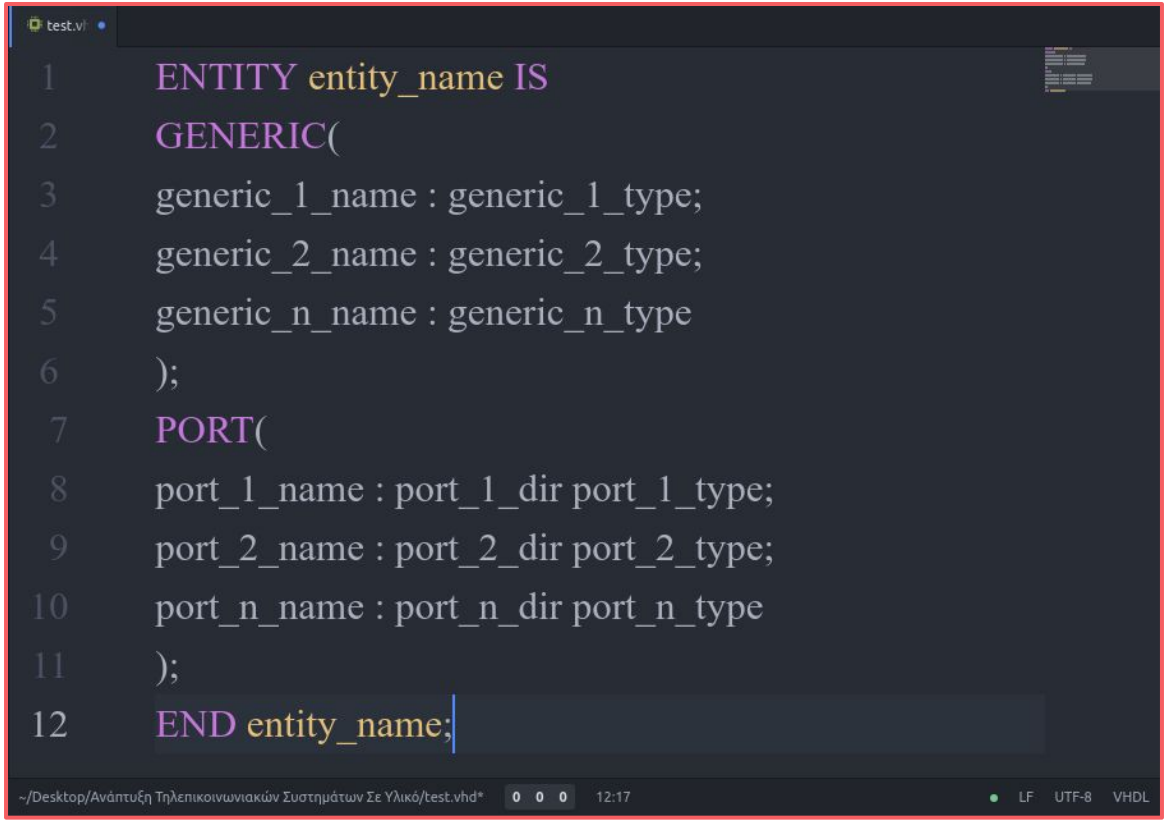
- All VHDL designs provide an external interface and an internal implementation.

- Any VHDL design consists of an entity, one or more architectures and zero or one configuration.

VHDL: Entities

- The entity of a VHDL design is practically its external interface.
- Entity declarations specify the following:
  - Name of the entity
  - Port declarations (practically the inputs and output of the design)
- It must be noted that generic declarations can be used but are optional.

VHDL: Entities (cont.)



VHDL: Entities (cont.)

VHDL: Ports

- Port names:
  - Letters, digits and/or underscores
  - All port names must start with a letter
  - Case insensitive
- Port types:
  - IN
  - OUT
  - INOUT
  - BUFFER