



## DE2-115 Control Panel - Part II

數位電路實驗

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#### **Outline**

- SDRAM/SRAM/EEPROM/Flash Controller and Programmer
- VGA
- IR Receiver
- Others
  - USB, PS/2, SD Card, RS232, and HSMC
- Over all Structure of the DE2-115 Control Panel







# SDRAM/SRAM/EEPROM/ Flash Controller and Programmer





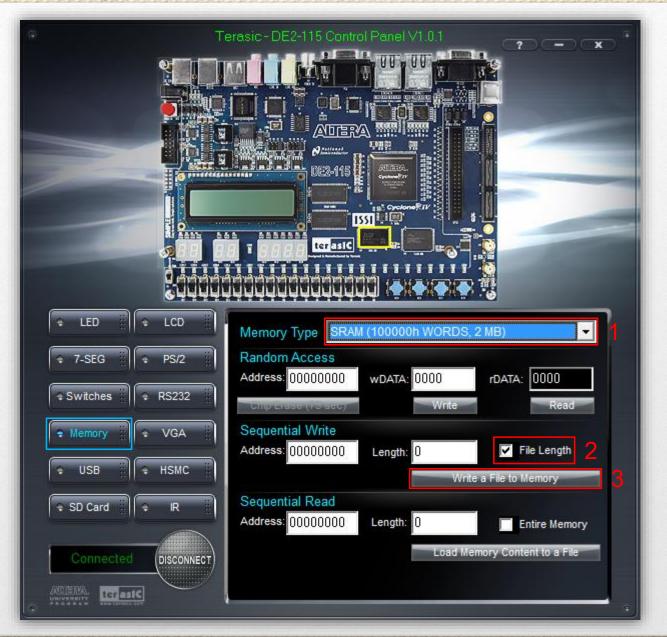


# Memory Controller and Programmer

- The Control Panel can be used to write/read data to/from the SRAM, SDRAM, EEPROM, and Flash chips on the DE2-115 board.
- As an example, we will describe how the SRAM may be accessed; the same approach is used to access the SDRAM, EEPROM, and Flash.





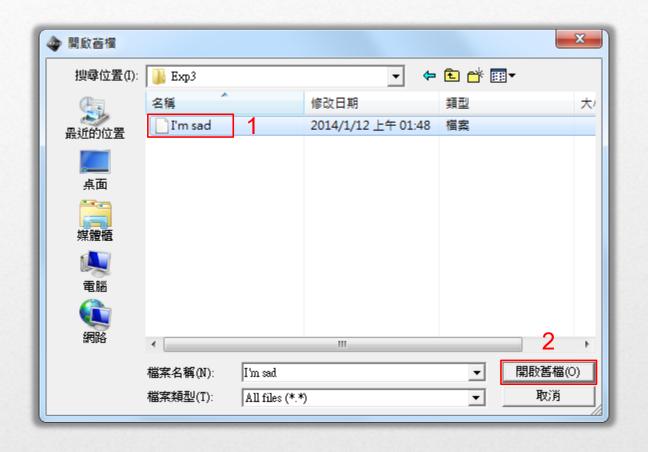


































## **VGA**





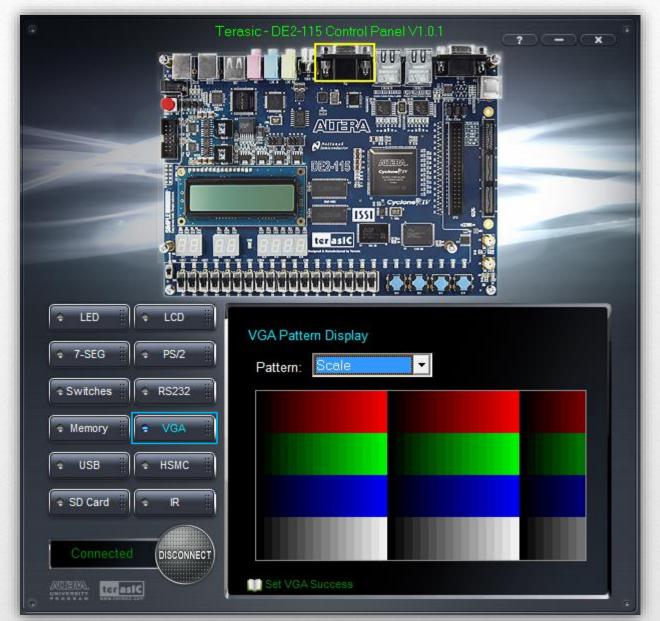


#### VGA Controller

- DE2-115 Control Panel provides VGA pattern function that allows users to output color pattern to LCD/CRT monitor using the DE2-115 board.
- Remember to plug a D-sub cable to VGA connector of the DE2-115 before using the Control Panel.































## IR Receiver







#### IR Receiver

- From the control panel, we can test the IR receiver on the DE2-115 by sending scan code from a remote controller.
- When the scan code is received, the information will be displayed on the Receiver window represented in hexadecimal.
- Also, the pressed button on the remote controller will be indicated on the graphic of remote controller on the IR receiver window.

















#### Others

USB, PS/2, SD Card, RS232, and HSMC

























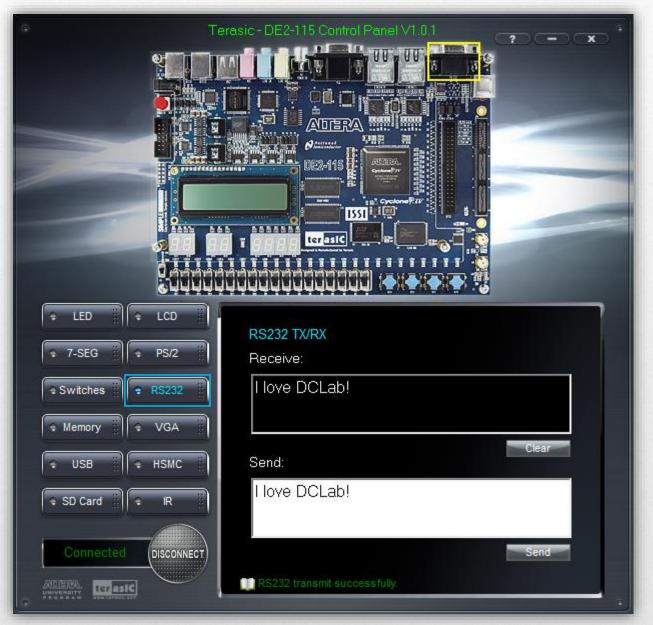


























# Over all Structure of the DE2-115 Control Panel







### Overall Structure (1/2)

- The DE2-115 Control Panel is based on a Nios II SOPC system instantiated in the Cyclone IV E FPGA with software running on the on-chip memory.
- The software part is implemented in C code; the hardware part is implemented in Verilog HDL code with SOPC builder.
  - The source code is not available on the DE2\_115 System CD.







### Overall Structure (2/2)

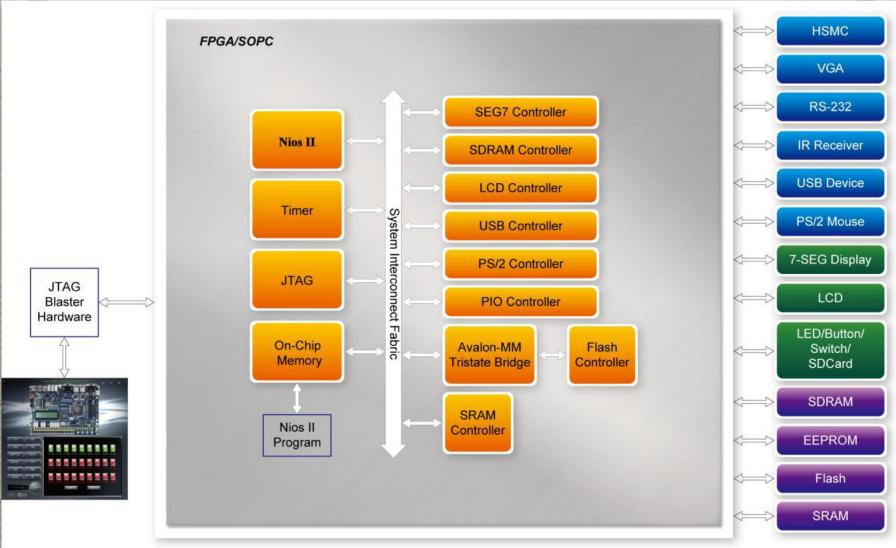
- Each input/output device is controlled by the Nios II Processor instantiated in the FPGA chip.
- The communication with the PC is done via the USB Blaster link.
- The Nios II interprets the commands set from the PC and performs the corresponding actions.





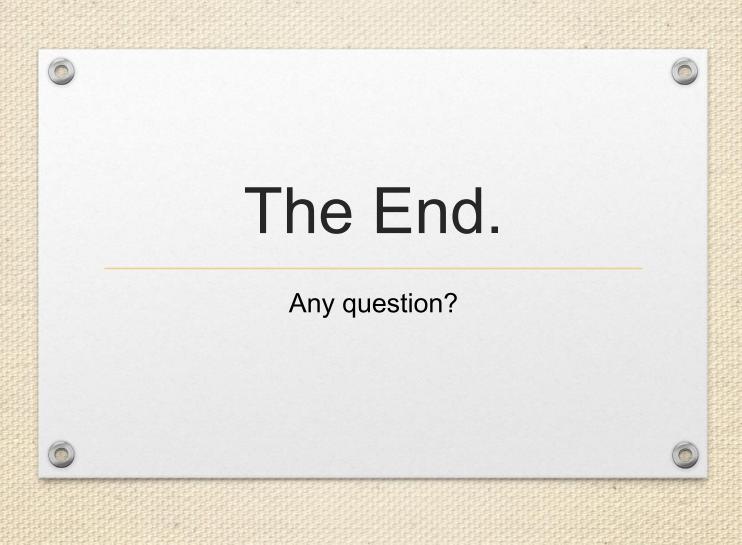














#### Reference

1. "DE2-115 User Manual" by Terasic Technologies Inc.

