Memory Devices on DE2-115

數位電路實驗
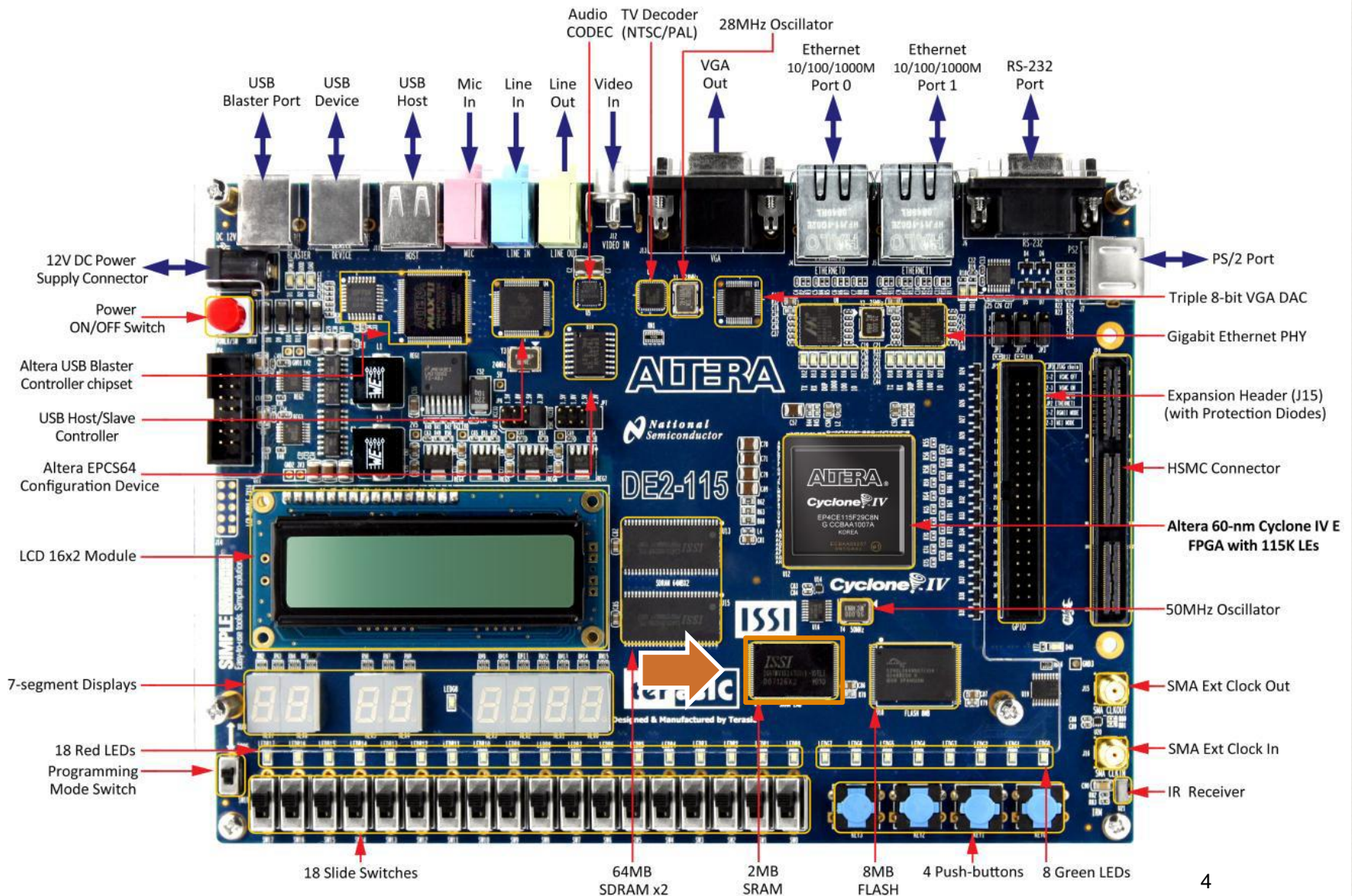
TA: 吳柏辰

Author: Trumen

Outline

- SRAM

- SDRAM

- FLASH

- EEPROM

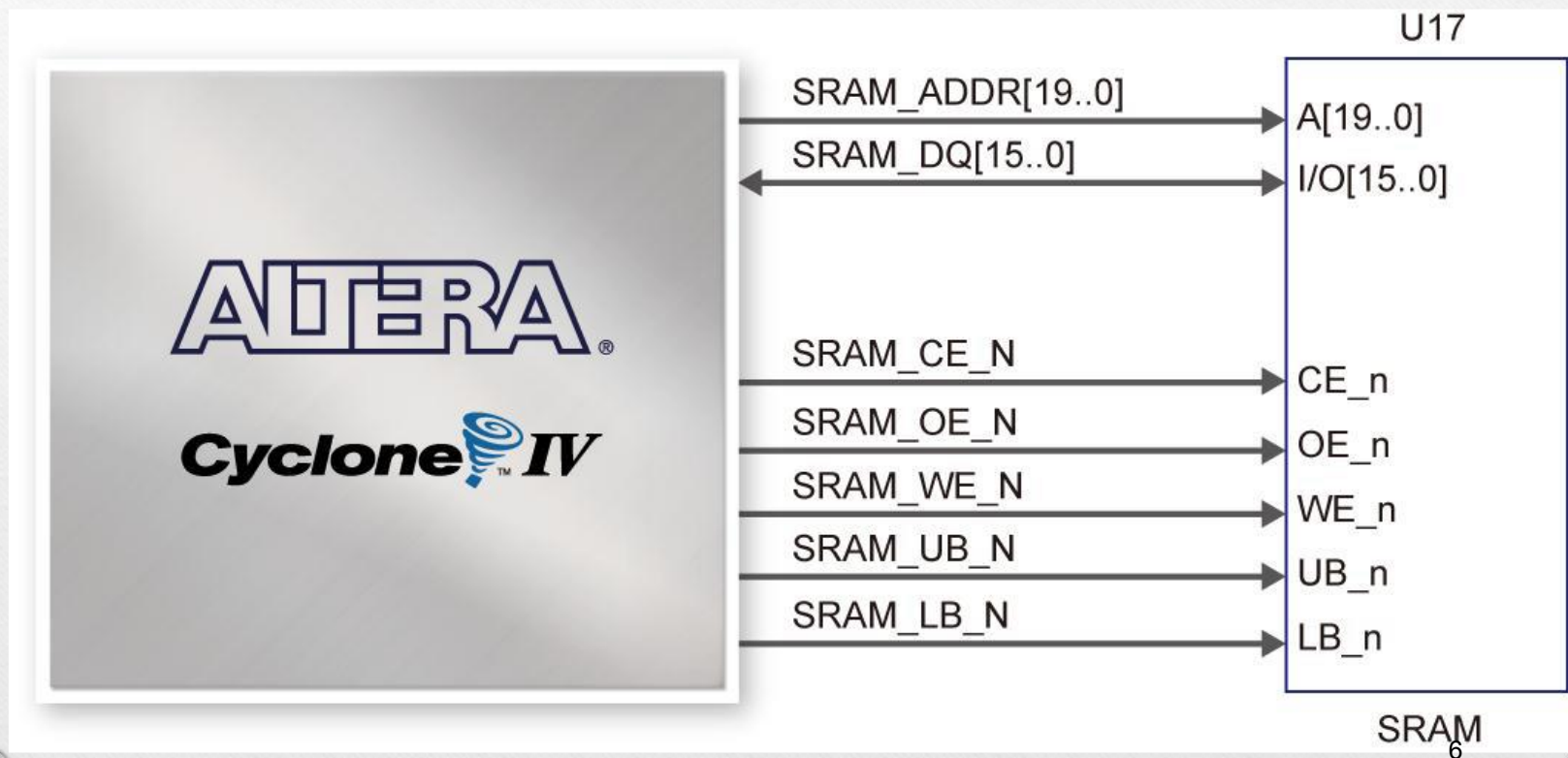- SD Card

SRAM

Altera DE2-115 Development and Education Board

Features

- 16M-bit (2MB) static RAMs organized as 1024K words by 16 bits.

  # of addresses

- High-speed access times:
  - speed = 20ns for VDD 1.65V to 2.2V
  - speed = 10ns for VDD 2.4V to 3.6V
  - speed = 8ns for VDD 3.3V + 5%
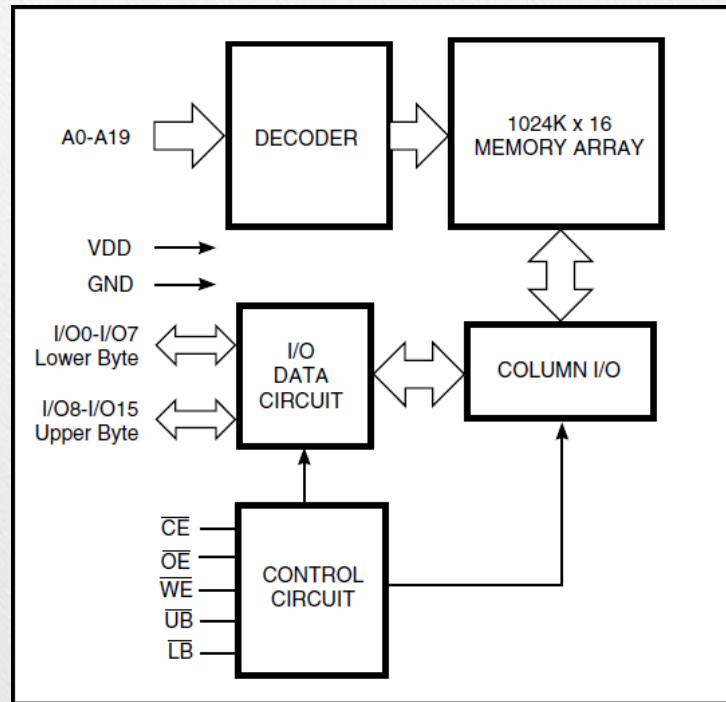
  Maximum performance frequency: 125MHz

Schematic Diagram

SRAM Pin Assignments

Signal Name	FPGA Pin No.	Description
SRAM_ADDR[0]~	PIN_AB7~	SRAM Address[0]~
SRAM_DQ[0]~	PIN_AH3~	SRAM Data[0]~
SRAM_OE	PIN_AD5	SRAM Output Enable
SRAM_WE	PIN_AE8	SRAM Write Enable
SRAM_CE	PIN_AF8	SRAM Chip Enable
SRAM_LB	PIN_AD4	SRAM Lower Byte Control
SRAM_UB	PIN_AC4	SRAM Upper Byte Control

SRAM Block Diagram

SRAM Pin Configuration

- 48-pin TSOP-1 (12mm x 20mm)

Pin	Signal		Pin	Signal
1	A4		48	A5
2	A3		47	A6
3	A2		46	A7
4	A1		45	A8
5	A0		44	$\overline{OE}$
6	NC		43	$\overline{UB}$
7	$\overline{CE}$		42	$\overline{LB}$
8	I/O0		41	I/O15
9	I/O1		40	I/O14
10	I/O2		39	I/O13
11	I/O3		38	I/O12
12	VDD		37	GND
13	GND		36	VDD
14	I/O4		35	I/O11
15	I/O5		34	I/O10
16	I/O6		33	I/O9
17	I/O7		32	I/O8
18	$\overline{WE}$		31	NC
19	NC		30	A9
20	A19		29	A10
21	A18		28	A11
22	A17		27	A12
23	A16		26	A13
24	A15		25	A14
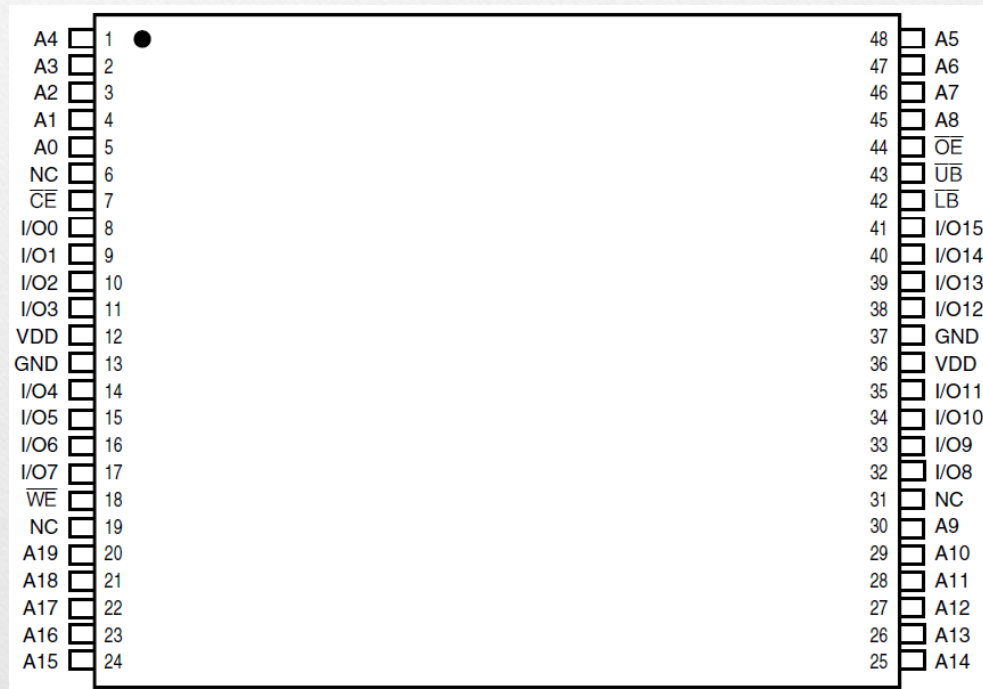
Truth Table

Mode	WE	CE	OE	LB	UB	I/O PIN I/O0-I/O7	I/O8-I/O15	V_DD Current
Not Selected	X	H	X	X	X	High-Z	High-Z	I_{SB1}, I_{SB2}
Output Disabled	H	L	H	X	X	High-Z	High-Z	I_{CC}
	X	L	X	H	H	High-Z	High-Z	
Read	H	L	L	L	H	D_{OUT}	High-Z	I_{CC}
	H	L	L	H	L	High-Z	D_{OUT}	
	H	L	L	L	L	D_{OUT}	D_{OUT}	
Write	L	L	X	L	H	D_{IN}	High-Z	I_{CC}
	L	L	X	H	L	High-Z	D_{IN}	
	L	L	X	L	L	D_{IN}	D_{IN}	

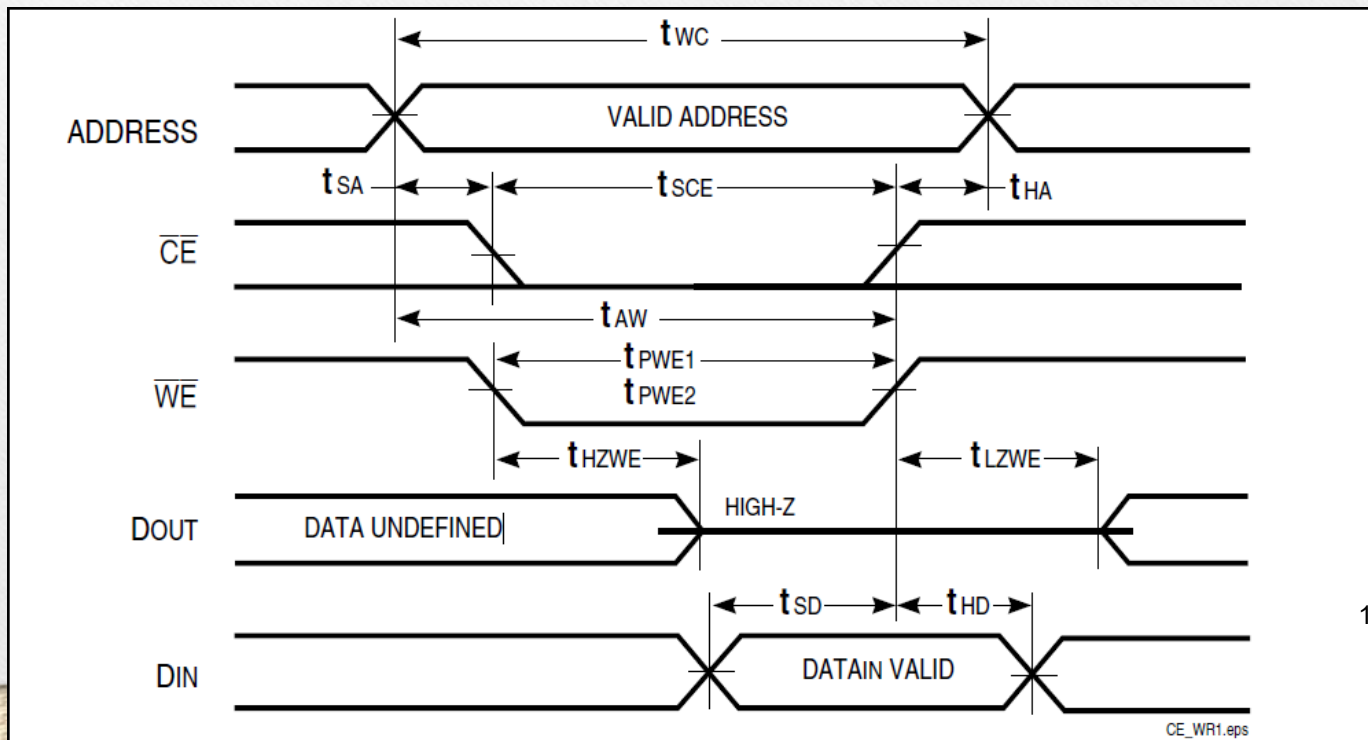# Read Cycle

- Min. read cycle time t_{RC} = 8ns
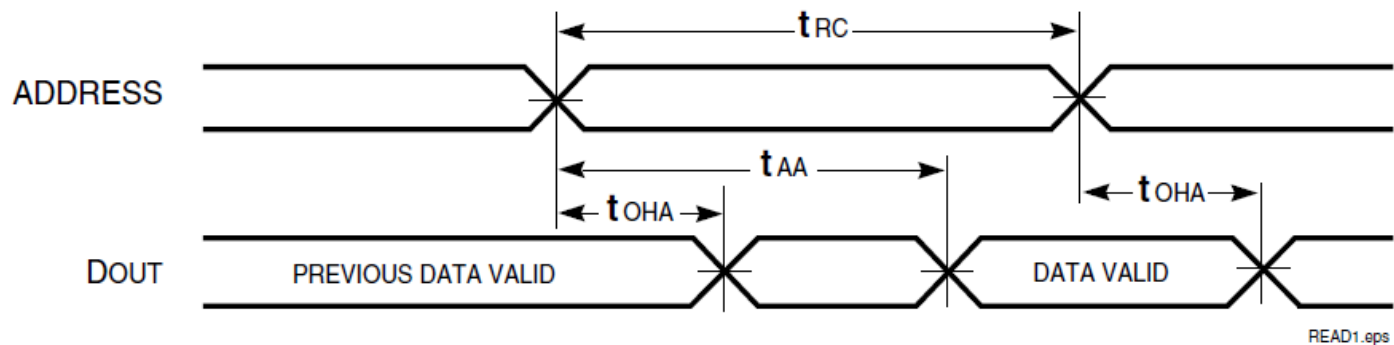
Write Cycle

- Min. write cycle time t_{WC} = 8ns

The End.

Any question?

Reference

1. "DE2-115 User Manual" by Terasic.
2. "DE2-115_MB.pdf" by Terasic.
3. "61WV102416ALL(ISSI_1M x 16_SRAM).pdf" by ISSI.