16x2 LCD Module on DE2-115

數位電路實驗

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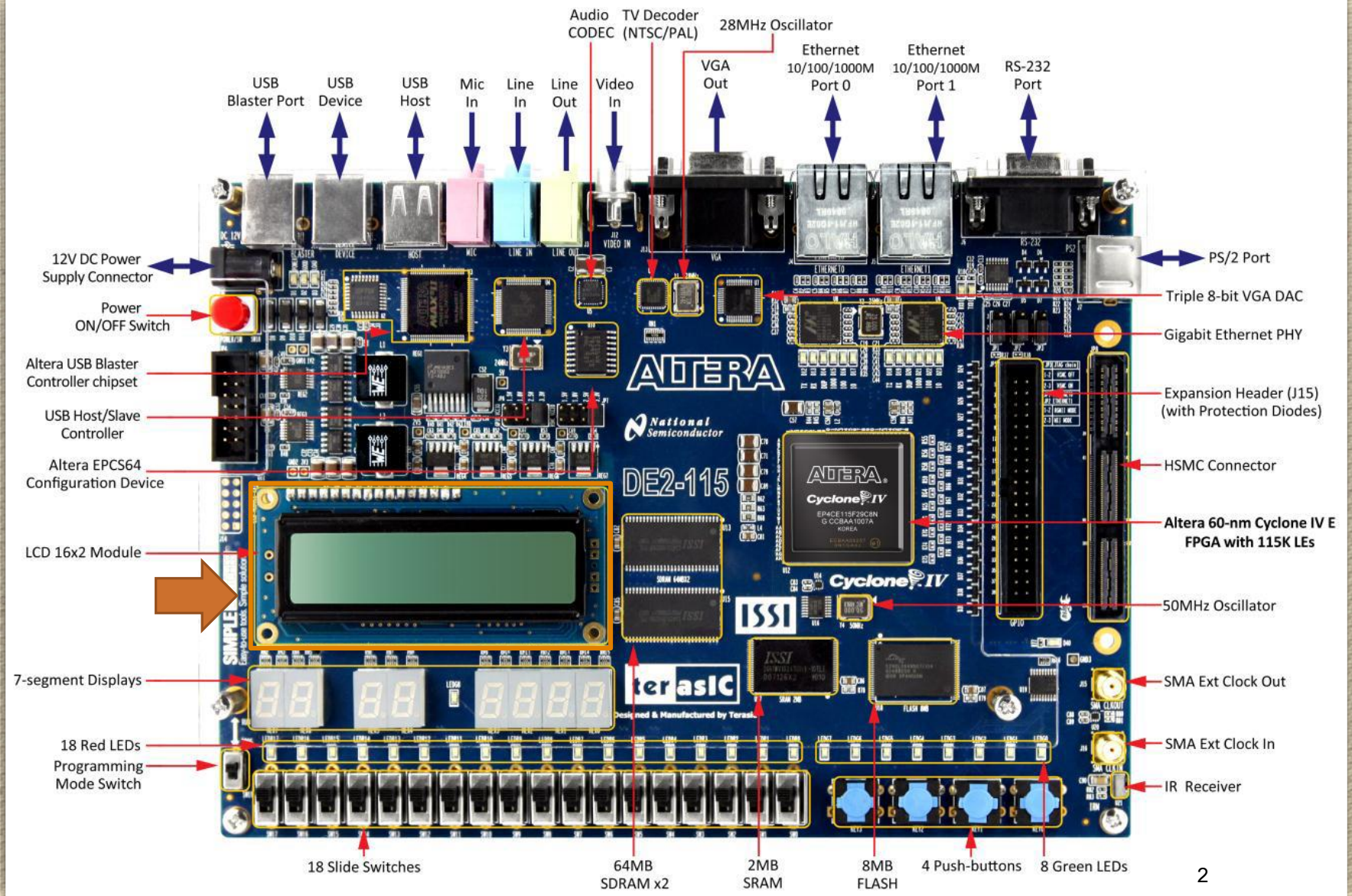
Author: Trumen

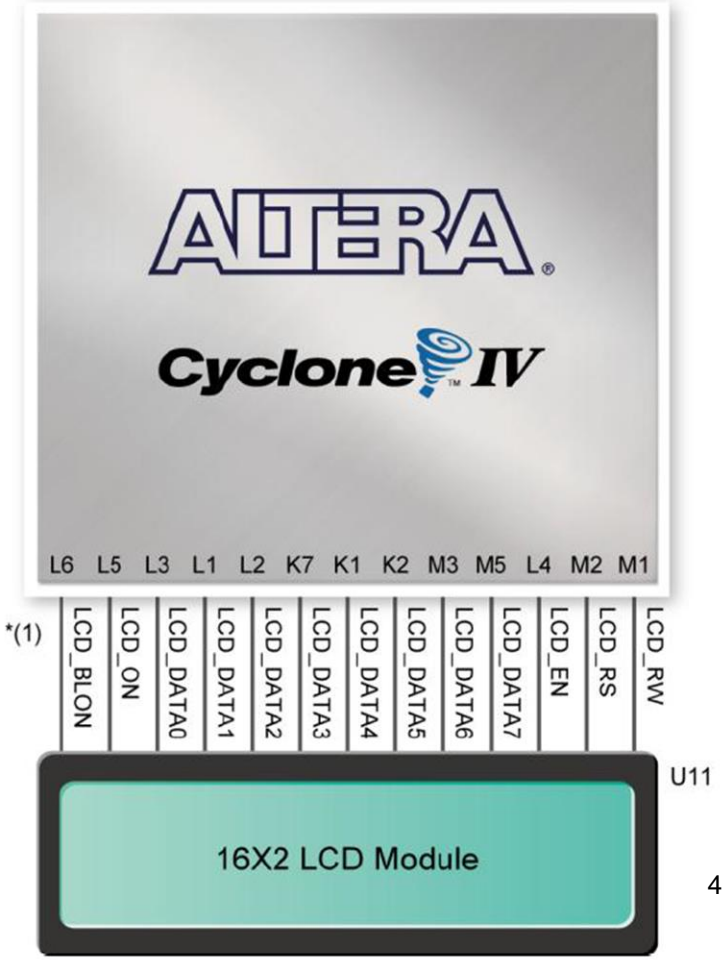

Audio CODEC
TV Decoder (NTSC/PAL)
28MHz Oscillator
VGA Out
Ethernet 10/100/1000M Port 0
Ethernet 10/100/1000M Port 1
RS-232 Port
USB Blaster Port
USB Device
USB Host
Mic In
Line In
Line Out
Video In
12V DC Power Supply Connector
Power ON/OFF Switch
Altera USB Blaster Controller chipset
USB Host/Slave Controller
Altera EPCS64 Configuration Device
LCD 16x2 Module
7-segment Displays
18 Red LEDs
Programming Mode Switch
18 Slide Switches
64MB SDRAM x2
2MB SRAM
8MB FLASH
4 Push-buttons
8 Green LEDs
PS/2 Port
Triple 8-bit VGA DAC
Gigabit Ethernet PHY
Expansion Header (J15) (with Protection Diodes)
HSMC Connector
Altera 60-nm Cyclone IV E FPGA with 115K LEs
50MHz Oscillator
SMA Ext Clock Out
SMA Ext Clock In
IR Receiver
ALTERA
National Semiconductor
DE2-115
Cyclone IV
ISSI
terasIC

Features

- Display Type:
  - Character Type
- Display's logical dimensions:
  - 16 columns by 02 lines
- View direction:
  - 6 o'clock

Schematic Diagram

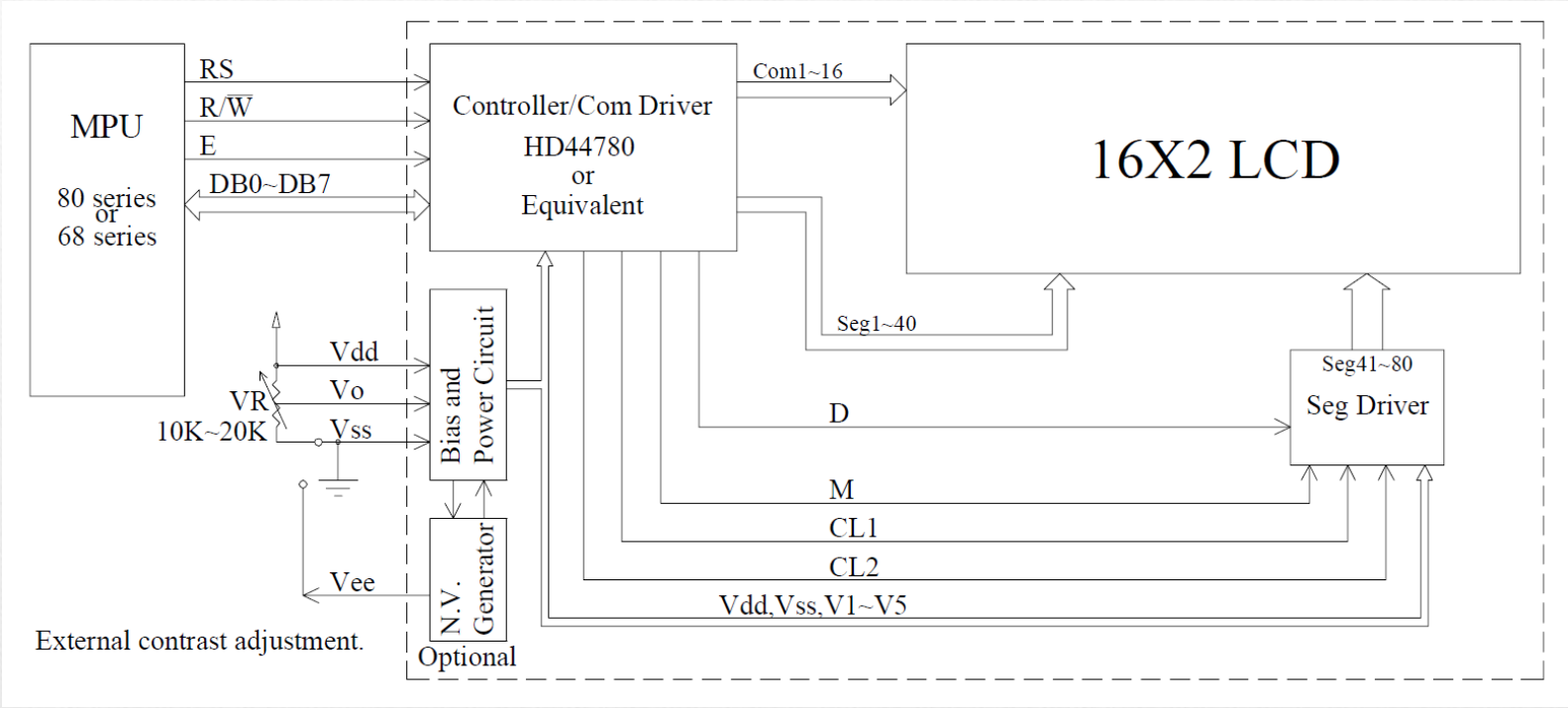
*(1): Note the current LCD modules used on DE2-115 boards do not have backlight. Therefore the LCD_BLON signals should not be used in user's design project.



LCD Module Pin Assignments

Signal Name	FPGA Pin No.	Description
LCD_DATA[0]~[7]	PIN_L3~M5	LCD Data[0]~[7]
LCD_EN	PIN_L4	LCD Enable (level sensitive: 1; edge sensitive: 1→0)
LCD_RW	PIN_M1	LCD Read/Write Select (0:write 1:read)
LCD_RS	PIN_M2	LCD Command Select (0:command 1:data)
LCD_ON	PIN_L5	Power ON/OFF
LCD_BLON	PIN_L6	LCD Back Light ON/OFF

LCD Block Diagram



Function Description (1/2)

- The LCD display Module is built in a LSI controller.
  - The controller has two 8-bit registers, an instruction register (IR) and a data register (DR).
  - The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM).
  - The DR temporarily stores data to be written or read from DDRAM or CGRAM.

Function Description (2/2)

0:command
1:data

0:write
1:read

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB6)
1	0	Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM)
1	1	Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR)

Busy Flag (BF)

- When the busy flag is 1, the controller LSI is in the internal operation mode, and the next instruction will not be accepted.
- When RS=0 and R/W=1, the busy flag is output to DB7.
- The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

- The address counter (AC) assigns addresses to both DDRAM and CGRAM.

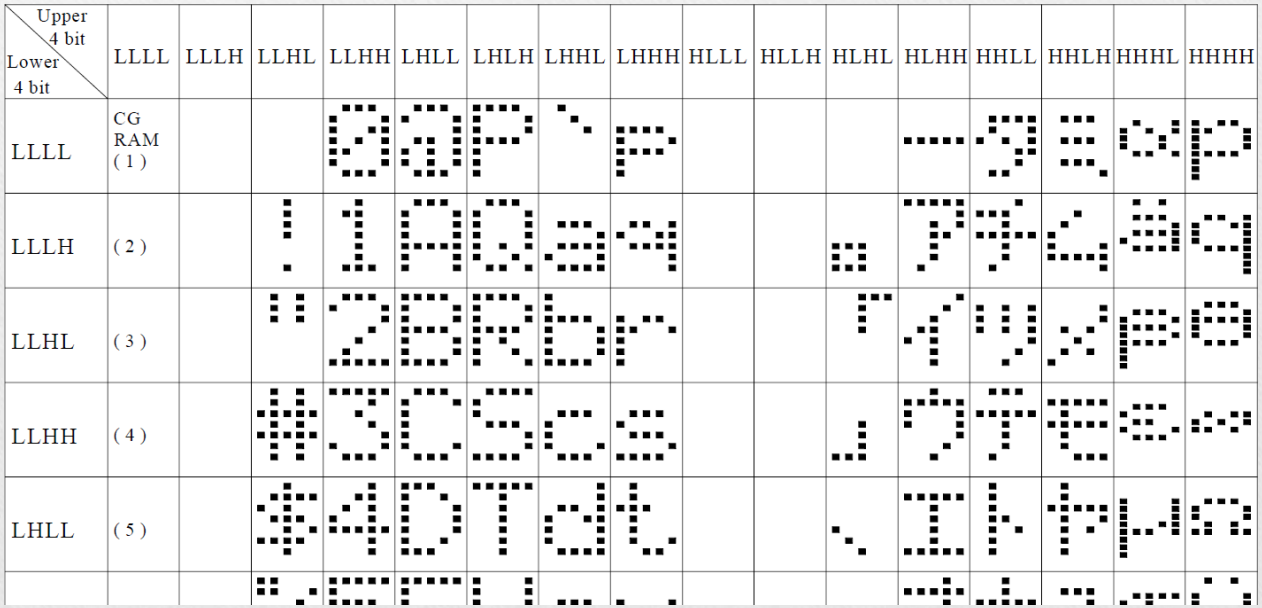
Display Data RAM (DDRAM)

- This DDRAM is used to store the display data represented in 8-bit character codes.
  - Its extended capacity is 80×8 bits or 80 characters.
  - Below figure is the relationships between DDRAM addresses and positions on the liquid crystal display.

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

Character Generator ROM (CGROM)

- The CGROM generate 5×8 dot or 5×10 dot character patterns from 8-bit character codes.



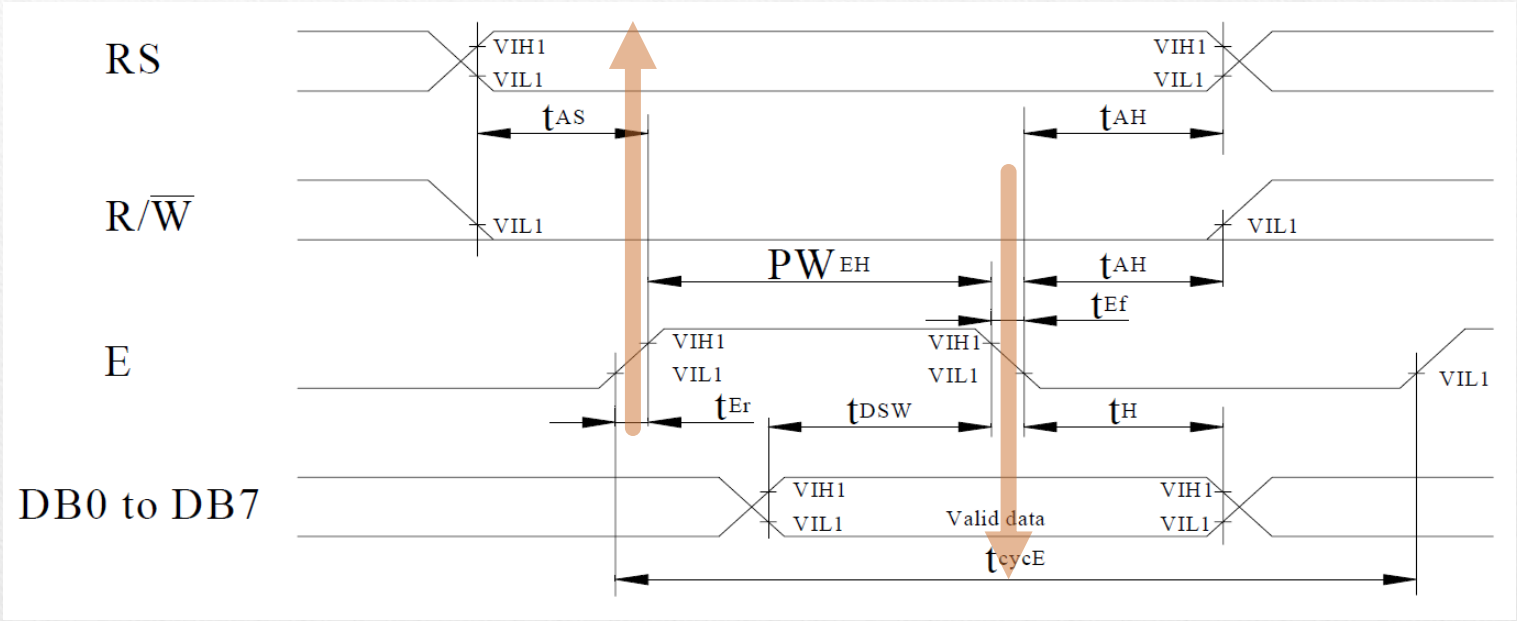
Instruction Table (1/2)

Instruction	Instruction Code										Description	Execution time (fosc=270Khz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "00H" to DDRAM and set DDRAM address to "00H" from AC	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display.	39 μ s
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit.	39 μ s
Function Set	0	0	0	0	1	DL	N	F	—	—	Set interface data length (DL:8-bit/4-bit), numbers of display line (N:2-line/1-line)and, display font type (F:5×11 dots/5×8 dots)	39 μ s

Instruction Table (2/2)

Instruction	Instruction Code										Description	Execution time (fosc=270Khz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39 μ s
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43 μ s

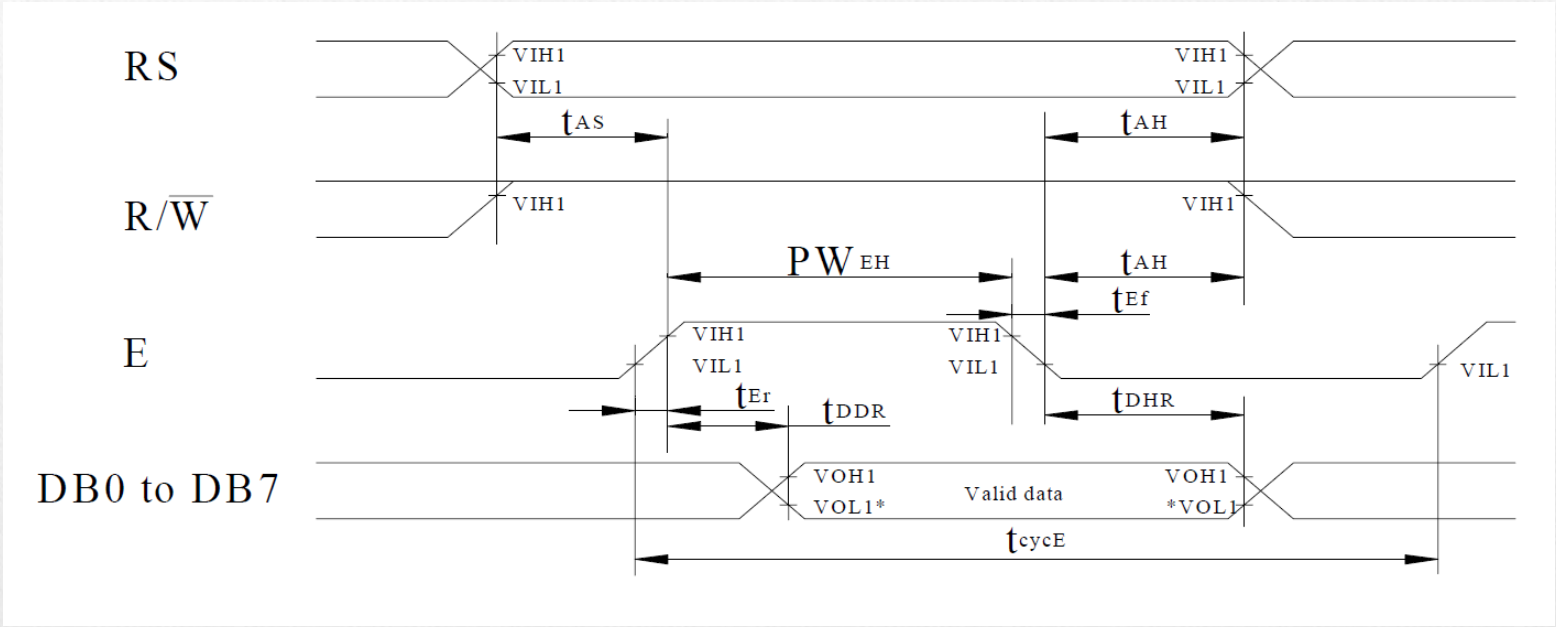
Write Operation (1/2)



Write Operation (2/2)

Item	Symbol	Min	Typ	Max	Unit
Enable cycle time	t_{cycE}	500	—	—	ns
Enable pulse width (high level)	PW_{EH}	230	—	—	ns
Enable rise/fall time	t_{Er},t_{Ef}	—	—	20	ns
Address set-up time (RS, R/W to E)	t_{AS}	40	—	—	ns
Address hold time	t_{AH}	10	—	—	ns
Data set-up time	t_{DSW}	80	—	—	ns
Data hold time	t_{H}	10	—	—	ns

Read Operation (1/2)



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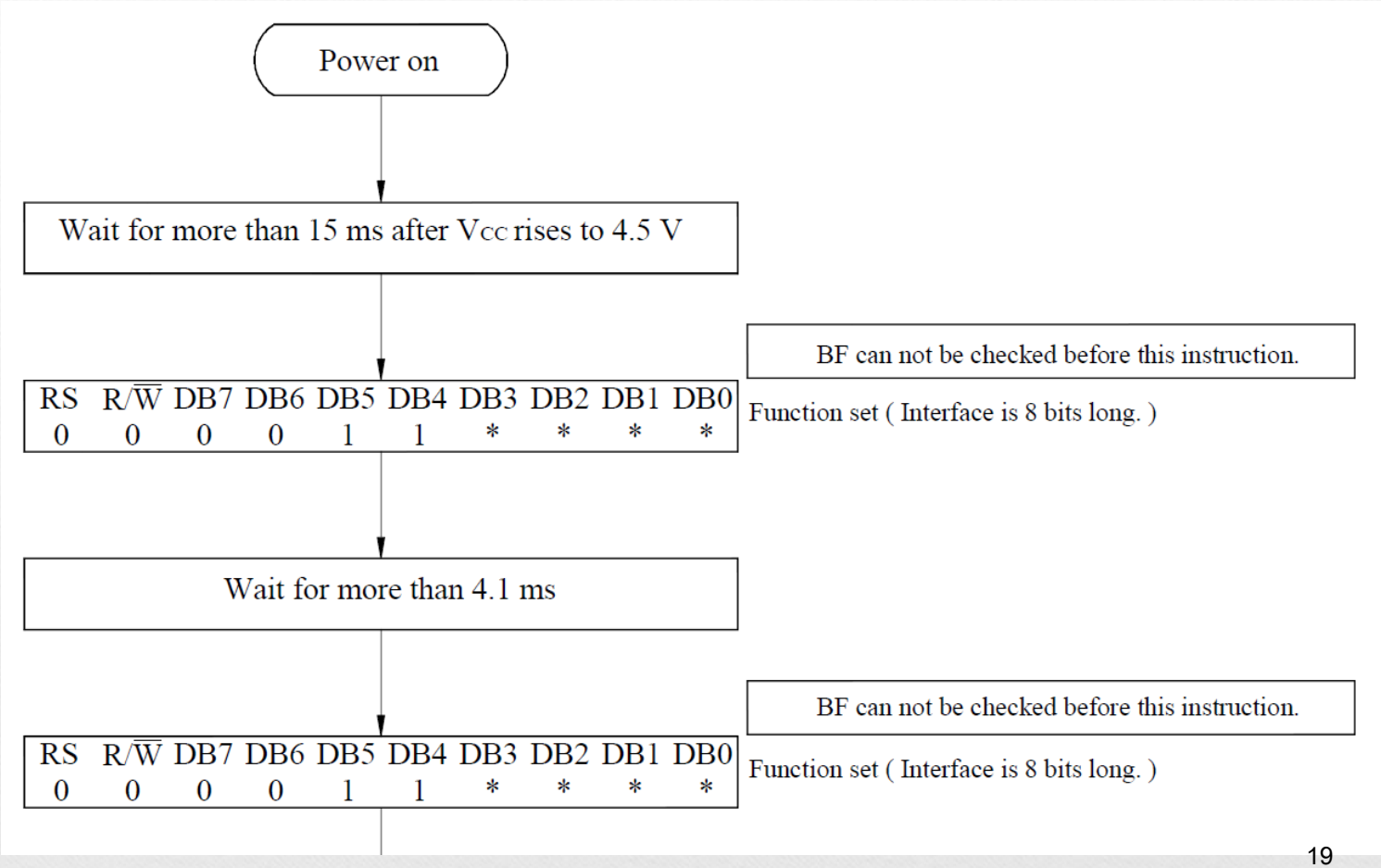
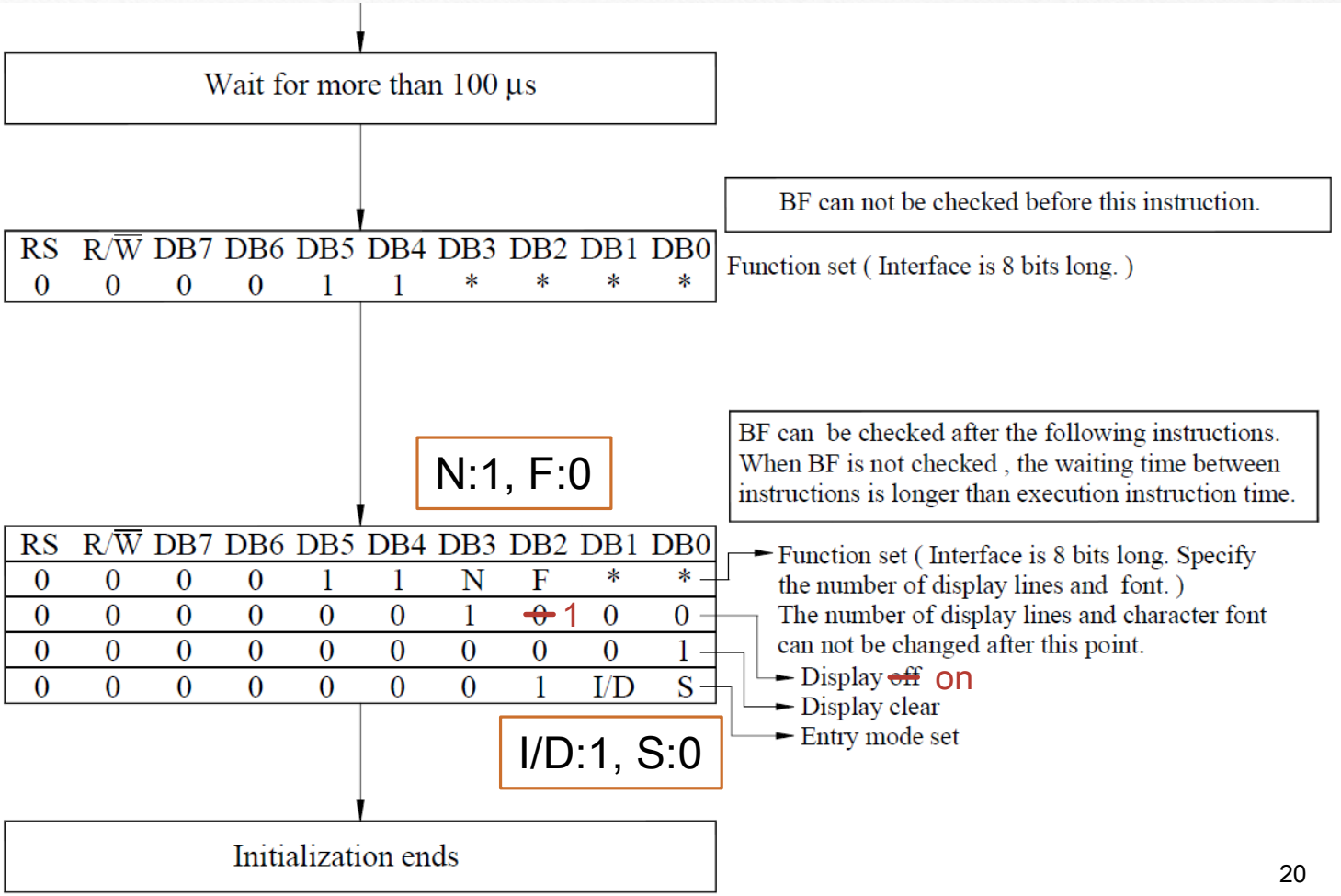
Enable cycle time	t_{cycE}	500	—	—	ns
Enable pulse width (high level)	PW_{EH}	230	—	—	ns
Enable rise/fall time	t_{Er},t_{Ef}	—	—	20	ns
Address set-up time (RS, R/W to E)	t_{AS}	40	—	—	ns
Address hold time	t_{AH}	10	—	—	ns
Data delay time	t_{DDR}	—	—	160	ns
Data hold time	t_{DHR}	5	—	—	ns

Initializing of LCM (1/2)



Initializing of LCM (2/2)



The End.

Any question?

Reference

1. "DE2-115 User Manual" by Terasic.
2. "DE2-115_MB.pdf" by Terasic.
3. "CFAH1602BTMCJP.pdf" by *Crystalfontz America*, Inc..