

VLSI Project Report

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Proposed Designs:

D1 : 13 States Mono

Rather than checking the sensors on each cycle based on their priority, we check the sensors on 13 cycles, with each sensor having a higher weight based on its priority, so:

the front sensor has 4 cycles weight

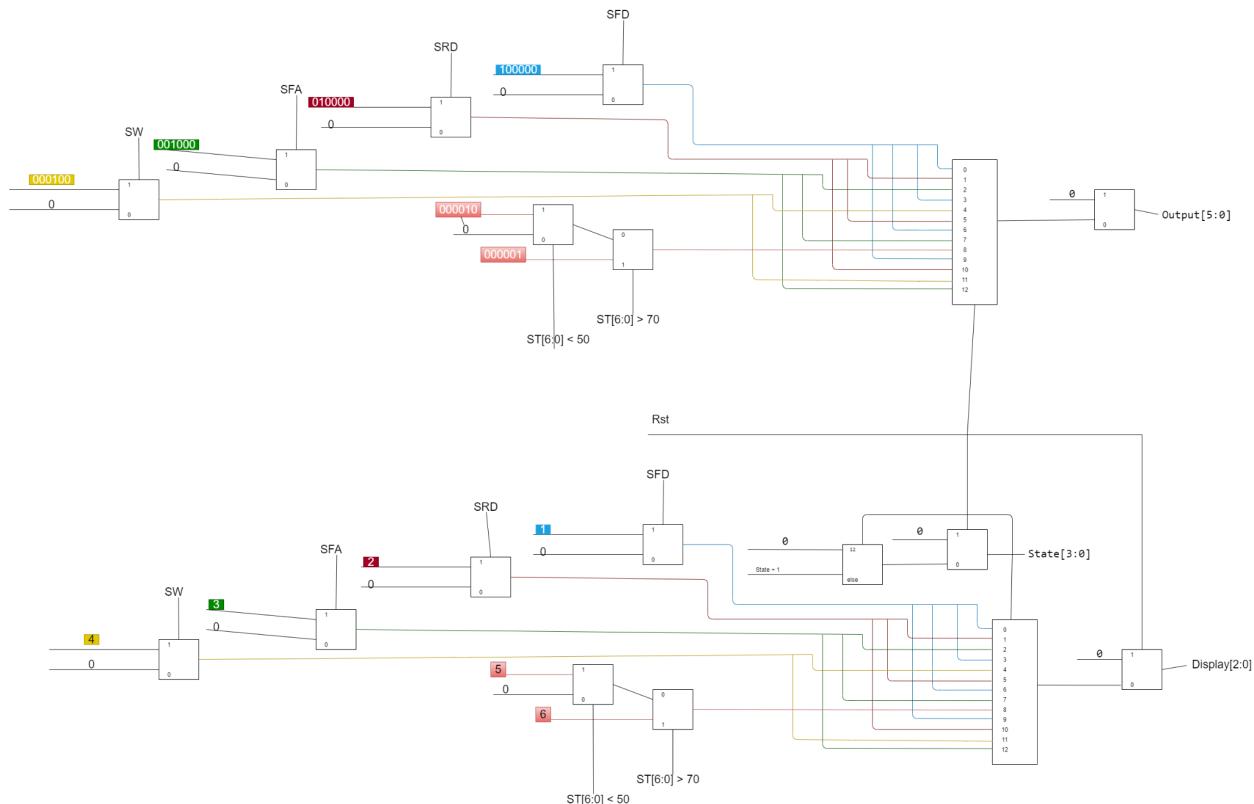
rear sensor have 3 cycles weight

fire sensor have 3 cycles weight

window sensor have 2 cycles weight

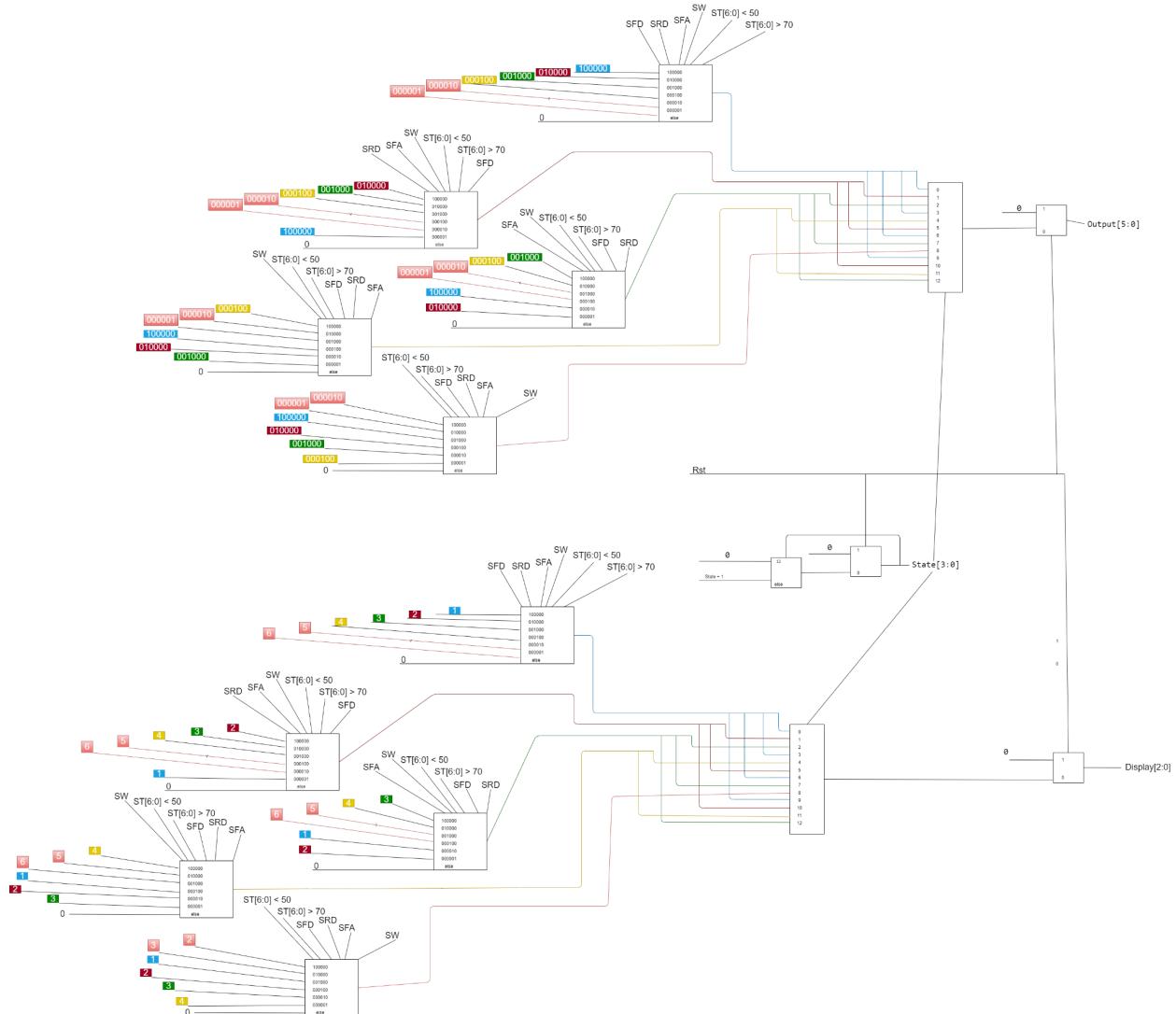
temperature sensor have 1 cycles weight

This means that the front door sensor is checked four times for every 13 clock cycles, while the rear door and fire alarm sensors are checked three times for every 13 clock cycles, and so on.



D2 : 13 States Multi

The goal of this design is to make the 13 States Mono more effective by not just checking one sensor on each clock cycle based on its weight, but also monitoring the other sensors if a sensor's reading is low on his turn.



D3 : Design 14253

This design utilizes two loops, the inner one loops every single cycle on all sensors until it finds a HIGH signal to process, while the other one decides the beginning of the inner loop, i.e.: the inner loop can be one of 5:

1 2 3 4 5

2 3 4 5 1

3 4 5 1 2

4 5 1 2 3

5 1 2 3 4,

the outer loop decides which one.

In another way, the outer loop selects where to start checking, then the inner loop stops when it finds a HIGH signal or outputs ZERO if none is found.

The trick is, the START of checking is 1, 4, 2, 5, 3 instead of the usual 1, 2, 3, 4, 5.

This distributes the checked signals more evenly compared to the naive way.

In a third way, this design checks signals like this:

1-first cycle: 1->2->3->4->5

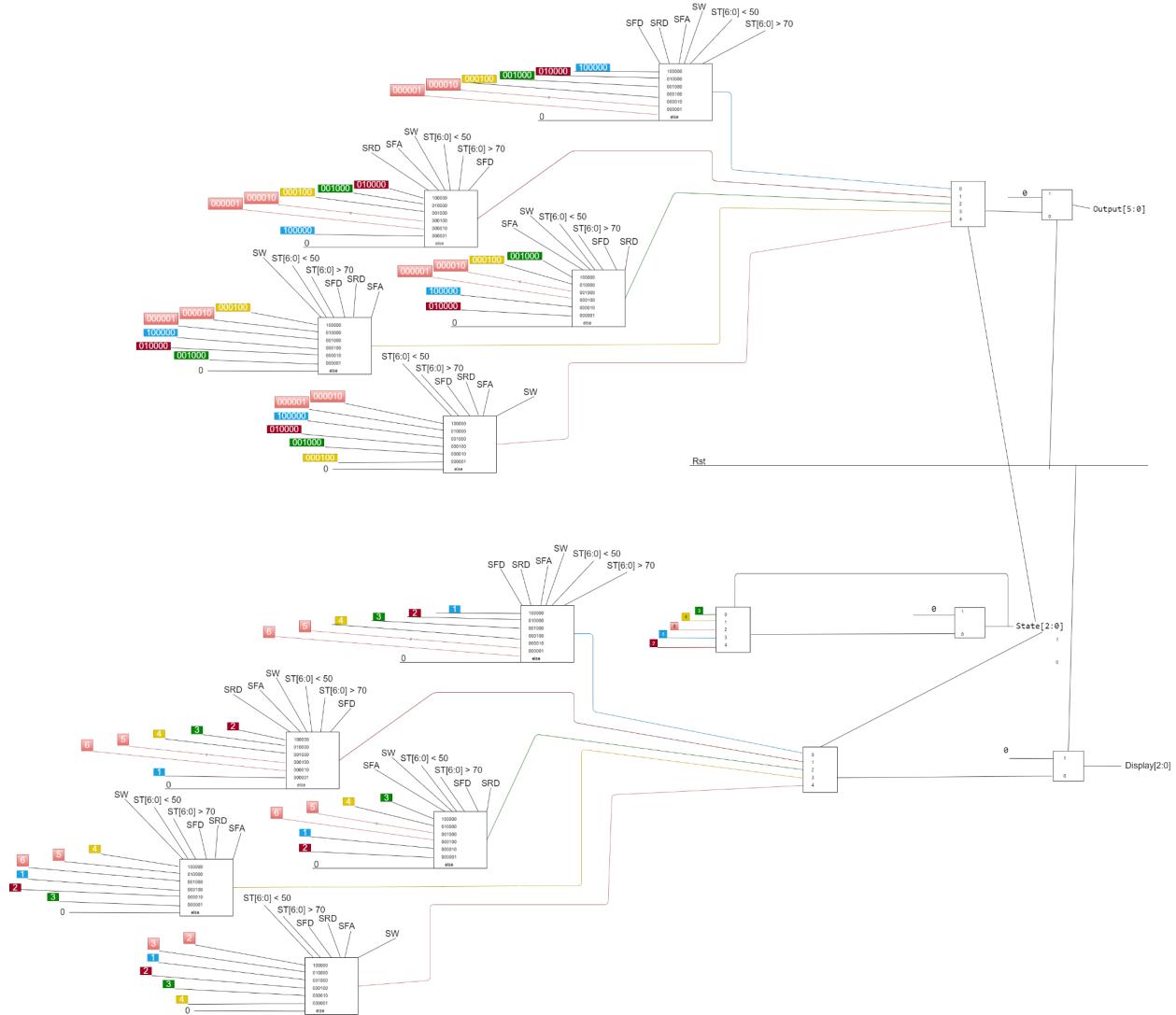
2-next: 4->5->1->2->3

3-next: 2->.....

4-next 5...

5-next 3....

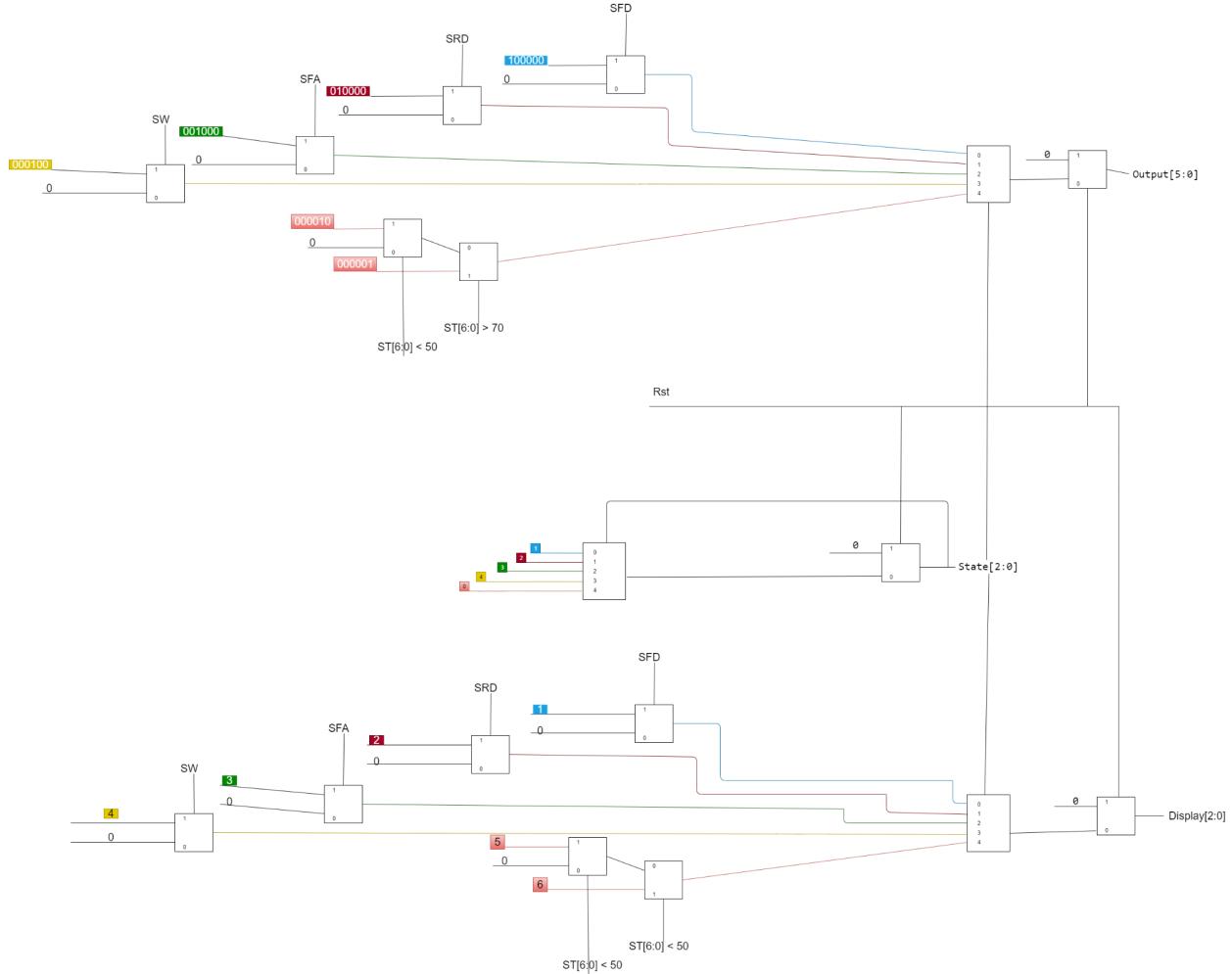
6-go back to 1



D4 : Seq mono check

We examine the reading of one sensor every clock cycle, starting with the greatest priority and working our way down, therefore we need 6 clock cycles to check the full system design.

When it's time to check a sensor with a lower priority than the previous one and a high value, we ignore the previous one and update the display with the current condition, despite the lower priority.



Synthesize Results Summary:

D1: 13 States Mono, D2: 13 States Multi, D3: 14253 Design, D4: Seq Mono Check

D1:

Report Path Groups:				
	Path Group	Weight	Critical Range(ps)	Worst Slack(ps)
1	1 default	1.000	0.0 1060.9	
2	2 I2R	1.000	0.0 517.6	
3	3 I2O	1.000	0.0 <ill>	
4	4 R2O	1.000	0.0 935.3	
10				

1	warning: No library characterized for (process = 1.00 voltage = 0.85 temperature = 25.00) can be found i			
Report Power (instances with prefix '*' are included in total) :				
Instance	Internal Power(uw)	Switching Power(uw)	Leakage Power(uw)	Total Power(uw)
1 *display_reg[2]	1.356428	1.421292	0.079112	2.856833
2 *display_reg[1]	1.562515	1.638362	0.079112	3.279990
3 *display_reg[0]	1.459398	1.529186	0.079112	3.067696
4 *out_reg[5]	0.642533	0.674881	0.079112	1.396526
5 *out_reg[4]	0.714939	0.751449	0.079112	1.545500
6 *out_reg[3]	0.498195	0.522670	0.079112	1.099977
7 *out_reg[2]	0.339191	0.355610	0.079112	0.773913
8 *out_reg[1]	0.575120	0.603323	0.079112	1.257555
9 *out_reg[0]	0.650463	0.682830	0.079112	1.412406
10 *State_reg[3]	2.120022	5.770236	0.079112	7.969371
11 *State_reg[2]	2.044384	6.063344	0.079112	8.186840
12 *State_reg[1]	2.044501	6.951147	0.079112	9.074760
13 *State_reg[0]	2.044163	4.383632	0.079112	6.506907
14 *i_0_0_0	1.338442	5.016623	0.061230	6.416295
15 *i_0_0_1	1.117229	4.387444	0.061230	5.565903
16 *i_0_0_2	0.445302	0.336739	0.021200	0.803240
17 *i_0_0_3	0.269597	0.209722	0.021200	0.500519
18 *i_0_0_4	0.212511	0.162594	0.021200	0.396304
19 *i_0_0_5	0.798689	0.303081	0.041741	1.143512
20 *i_0_0_6	0.641976	3.604043	0.022619	4.268639
21 *i_0_0_7	0.406539	0.160341	0.024415	0.591295
22 *i_0_0_8	0.196655	0.182526	0.025066	0.404247
23 *i_0_0_9	0.410118	0.223940	0.043178	0.677236
24 *i_0_0_10	0.374232	0.149857	0.024415	0.548504
25 *i_0_0_11	0.057888	0.134436	0.014353	0.206677
26 *i_0_0_12	0.103901	0.755340	0.022039	0.881280
27 *i_0_0_13	0.567537	0.885329	0.022619	1.475485
28 *i_0_0_14	0.844723	1.540357	0.022695	2.407774
29 *i_0_0_15	0.492982	1.322901	0.018105	1.833988
30 *i_0_0_16	0.121693	0.178349	0.025066	0.325109

36	31	*i_0_0_17		0.158417	0.136578	0.034026	0.329022
37	32	*i_0_0_18		0.193252	0.522290	0.018105	0.733647
38	33	*i_0_0_19		0.290366	0.885656	0.014353	1.190375
39	34	*i_0_0_20		0.932183	5.447109	0.036164	6.415455
40	35	*i_0_0_21		0.303668	0.119574	0.024415	0.447656
41	36	*i_0_0_22		0.109239	0.100871	0.025066	0.235176
42	37	*i_0_0_23		0.172069	0.125050	0.034026	0.331145
43	38	*i_0_0_24		0.418741	0.904905	0.017393	1.341039
44	39	*i_0_0_25		0.044417	0.093210	0.018127	0.155754
45	40	*i_0_0_26		0.090703	0.175372	0.032601	0.298676
46	41	*i_0_0_27		1.103387	0.951933	0.026481	2.081801
47	42	*i_0_0_28		0.704206	0.396736	0.024415	1.125357
48	43	*i_0_0_29		0.092419	0.198864	0.032601	0.323884
49	44	*i_0_0_30		0.195354	1.663878	0.017393	1.876626
50	45	*i_0_0_31		0.596786	1.810558	0.022619	2.429964
51	46	*i_0_0_32		0.222644	1.832890	0.017393	2.072927
52	47	*i_0_0_33		0.443372	1.811803	0.021200	2.276373
53	48	*i_0_0_34		0.495383	0.549449	0.032601	1.077434
54	49	*i_0_0_35		0.726402	0.609237	0.026481	1.362120
55	50	*i_0_0_36		0.697208	0.754494	0.014353	1.466055
56	51	*i_0_0_37		0.016072	0.032180	0.014353	0.062605
57	52	*i_0_0_38		0.826495	0.894405	0.014353	1.735252
58	53	*i_0_0_39		1.028024	1.472222	0.014353	2.514599
59	54	*i_0_0_40		0.227495	1.432950	0.014353	1.674799
60	55	*i_0_0_41		0.227522	1.216987	0.014353	1.458863
61	56	*i_0_0_42		0.235515	3.373861	0.014353	3.623729
62	57	*i_0_0_43		0.499730	8.184460	0.014353	8.698543
63	58						
64	59	*TOTAL		35.502941	86.599121	2.111117	124.213181
65		-----+-----+-----+-----+-----+-----+-----+-----					

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1 Report Physical info:
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			Area (squm)	Leakage (uW)
5 Design Name	integ			
6 Total Instances		57	107	2.111
7 Macros		0	0	0.000
8 Pads		0	0	0.000
9 Phys		0	0	0.000
10 Blackboxes		0	0	0.000
11 Cells		57	107	2.111
12 Buffers		0	0	0.000
13 Inverters		10	5	0.144
14 Clock-Gates		0	0	0.000
15 Combinational		34	43	0.939
16 Latches		0	0	0.000
17 FlipFlops		13	59	1.028
18 Single-Bit FF		13	59	1.028
19 Multi-Bit FF		0	0	0.000
20 Clock-Gated		0		
21 Bits		13	59	1.028
22 Load-Enabled		0		
23 Clock-Gated		0		
24 Tristate Pin Count		0		
25 Physical Info	Placed			
26 Chip Size (mm x mm)	0.073 x 0.073		5382	
27 Fixed Cell Area			0	
28 Phys Only		0	0	
29 Placeable Area			168	
30 Movable Cell Area			107	
31 Utilization (%)		63		
32 Chip Utilization (%)		63		
33 Total Wire Length (mm)	0.813			
34 Longest Wire (mm)	0.037			
35 Average Wire (mm)	0.037			
36				

D2:

```
1 Report Path Groups:  
2 -----+-----+-----+-----  
3 | Path | Weight|Critical |Worst  
4 | Group |       |Range(ps)|Slack(ps)  
5 -----+-----+-----+-----  
6 1 |default| 1.000|      0.0| 963.9  
7 2 |I2R    | 1.000|      0.0| 450.6  
8 3 |I2O    | 1.000|      0.0|<ill>  
9 4 |R2O    | 1.000|      0.0| 935.0  
10 -----+-----+-----+-----  
  
1 Report Physical info:  
2 -----+-----+-----+-----  
3 |           |          |Area (squm)|Leakage (uW)  
4 -----+-----+-----+-----  
5 Design Name           |integ   |      |  
6 Total Instances        |         93| 139| 2.882  
7 Macros                |         0| 0| 0.000  
8 Pads                  |         0| 0| 0.000  
9 Phys                  |         0| 0| 0.000  
10 Blackboxes            |         0| 0| 0.000  
11 Cells                 |         93| 139| 2.882  
12 Buffers               |         0| 0| 0.000  
13 Inverters              |         21| 11| 0.301  
14 Clock-Gates            |         0| 0| 0.000  
15 Combinational          |         59| 69| 1.552  
16 Latches                |         0| 0| 0.000  
17 FlipFlops              |         13| 59| 1.028  
18 Single-Bit FF           |         13| 59| 1.028  
19 Multi-Bit FF            |         0| 0| 0.000  
20 Clock-Gated             |         0| 0| 0.000  
21 Bits                   |         13| 59| 1.028  
22 Load-Enabled            |         0| 0| 0.000  
23 Clock-Gated             |         0| 0| 0.000  
24 Tristate Pin Count      |         0| 0| 0.000  
25 Physical Info           |Placed   |      |  
26 Chip Size (mm x mm)    |0.076 x 0.076| 5775|  
27 Fixed Cell Area         |         0| 0| 0.000  
28 Phys Only               |         0| 0| 0.000  
29 Placeable Area          |         0| 246|  
30 Movable Cell Area       |         0| 139|  
31 Utilization (%)         |         56| 0|  
32 Chip Utilization (%)    |         56| 0|  
33 Total Wire Length (mm)  |         0.842| 0|  
34 Longest Wire (mm)        |         0.039| 0|  
35 Average Wire (mm)       |         0.038| 0|  
36 -----+-----+-----+-----
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1 warning: No library characterized for (process = 1.00 voltage = 0.85 temperature = 25.00) can be found
2 Report Power (instances with prefix '*' are included in total) :
3 -----
4 | Instance      | Internal Power(uw) | Switching Power(uw) | Leakage Power(uw) | Total Power(uw)
5 -----
6 1  | *display_reg[2] | 2.167321 | 2.295109 | 0.079112 | 4.541543
7 2  | *display_reg[1] | 2.316711 | 2.453099 | 0.079112 | 4.848923
8 3  | *display_reg[0] | 2.060424 | 2.183211 | 0.079112 | 4.322748
9 4  | *out_reg[5]    | 1.044252 | 1.109120 | 0.079112 | 2.232484
10 5 | *out_reg[4]    | 1.030298 | 1.094623 | 0.079112 | 2.204032
11 6 | *out_reg[3]    | 0.886559 | 0.941909 | 0.079112 | 1.907580
12 7 | *out_reg[2]    | 0.894354 | 0.949546 | 0.079112 | 1.923011
13 8 | *out_reg[1]    | 0.354241 | 0.375766 | 0.079112 | 0.809120
14 9 | *out_reg[0]    | 0.401960 | 0.426765 | 0.079112 | 0.907837
15 10 | *State_reg[3]  | 2.120026 | 5.800629 | 0.079112 | 7.999767
16 11 | *State_reg[2]  | 2.044492 | 6.878209 | 0.079112 | 9.001812
17 12 | *State_reg[1]  | 2.044341 | 5.730345 | 0.079112 | 7.853798
18 13 | *State_reg[0]  | 2.044537 | 7.219379 | 0.079112 | 9.343028
19 14 | *i_0_0_0       | 1.326267 | 0.679288 | 0.061230 | 2.066786
20 15 | *i_0_0_1       | 1.114165 | 0.728592 | 0.061230 | 1.903987
21 16 | *i_0_0_2       | 0.425878 | 0.336739 | 0.021200 | 0.783817
22 17 | *i_0_0_3       | 0.466488 | 0.204788 | 0.025066 | 0.696342
23 18 | *i_0_0_4       | 0.361679 | 0.158470 | 0.025066 | 0.545216
24 19 | *i_0_0_5       | 0.545638 | 0.208714 | 0.041741 | 0.796093
25 20 | *i_0_0_6       | 0.315828 | 1.144227 | 0.014353 | 1.474408
26 21 | *i_0_0_7       | 0.402715 | 6.903829 | 0.017393 | 7.323937
27 22 | *i_0_0_8       | 0.077928 | 0.035021 | 0.025066 | 0.138014
28 23 | *i_0_0_9       | 0.062000 | 0.038670 | 0.034566 | 0.135235
29 24 | *i_0_0_10      | 0.198579 | 0.176107 | 0.014353 | 0.389039
30 25 | *i_0_0_11      | 0.290363 | 2.560898 | 0.022619 | 2.873880
31 26 | *i_0_0_12      | 0.126025 | 0.224806 | 0.027858 | 0.378690
32 27 | *i_0_0_13      | 0.114487 | 0.108909 | 0.024415 | 0.247811
33 28 | *i_0_0_14      | 0.316642 | 0.267326 | 0.014353 | 0.598321
34 29 | *i_0_0_15      | 0.425793 | 3.887386 | 0.027858 | 4.341038
35 30 | *i_0_0_16      | 0.813175 | 1.063097 | 0.022039 | 1.898311
36 31 | *i_0_0_17      | 0.314073 | 0.699261 | 0.014353 | 1.027687
37 32 | *i_0_0_18      | 0.613535 | 3.915309 | 0.032612 | 4.561457
38 33 | *i_0_0_19      | 1.147577 | 1.221801 | 0.033938 | 2.403316
39 34 | *i_0_0_20      | 0.136723 | 0.233703 | 0.027858 | 0.398284

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40	35	*i_0_0_21		0.563770	0.927679	0.018105	1.509554
41	36	*i_0_0_22		0.226775	0.605741	0.027858	0.860374
42	37	*i_0_0_23		0.737349	0.301276	0.024415	1.063040
43	38	*i_0_0_24		0.175364	0.449288	0.021200	0.645851
44	39	*i_0_0_25		0.435699	1.221714	0.027858	1.685271
45	40	*i_0_0_26		0.195196	0.346499	0.027858	0.569554
46	41	*i_0_0_27		0.012669	0.015242	0.018127	0.046038
47	42	*i_0_0_28		0.236981	0.268648	0.041741	0.547370
48	43	*i_0_0_29		0.371838	0.975459	0.027858	1.375156
49	44	*i_0_0_30		0.158578	1.461295	0.014353	1.634226
50	45	*i_0_0_31		0.288330	3.111124	0.027858	3.427312
51	46	*i_0_0_32		0.320659	0.270718	0.014353	0.605731
52	47	*i_0_0_33		0.448249	3.936711	0.027858	4.412818
53	48	*i_0_0_34		0.309577	1.055745	0.017393	1.382715
54	49	*i_0_0_35		0.230939	0.547770	0.027858	0.806568
55	50	*i_0_0_36		0.008627	0.011451	0.018127	0.038205
56	51	*i_0_0_37		0.079904	0.467678	0.014353	0.561935
57	52	*i_0_0_38		0.198607	1.733287	0.018127	1.950021
58	53	*i_0_0_39		0.382885	2.328013	0.021200	2.732097
59	54	*i_0_0_40		0.612925	2.514030	0.017393	3.144348
60	55	*i_0_0_41		0.580616	2.527671	0.017393	3.125681
61	56	*i_0_0_42		0.644437	4.937069	0.017393	5.598900
62	57	*i_0_0_43		0.800447	0.951313	0.018105	1.769864
63	58	*i_0_0_44		0.704714	0.679007	0.024415	1.408136
64	59	*i_0_0_45		0.469214	5.688364	0.014353	6.171930
65	60	*i_0_0_46		1.084002	9.250976	0.027858	10.362836
66	61	*i_0_0_47		0.501429	0.652065	0.026832	1.180326
67	62	*i_0_0_48		0.550743	0.629289	0.018105	1.198137
68	63	*i_0_0_49		0.439862	1.797003	0.027858	2.264724
69	64	*i_0_0_50		0.605375	0.787701	0.027858	1.420934
70	65	*i_0_0_51		0.338075	1.387970	0.017393	1.743438
71	66	*i_0_0_52		0.168042	0.486794	0.014353	0.669189
72	67	*i_0_0_53		0.302822	3.292641	0.027858	3.623322
73	68	*i_0_0_54		0.105800	0.366926	0.027858	0.500585
74	69	*i_0_0_55		0.050007	0.052391	0.024415	0.126903
75	70	*i_0_0_56		0.395106	0.978399	0.022619	1.396124
76	71	*i_0_0_57		0.103846	0.983824	0.014353	1.102023
77	72	*i_0_0_58		0.215771	2.318973	0.027858	2.562603
78	73	*i_0_0_59		0.247340	0.531184	0.017393	0.795917
79	74	*i_0_0_60		0.074645	0.161775	0.022695	0.259115
80	75	*i_0_0_61		0.199954	0.496689	0.018105	0.714748
81	76	*i_0_0_62		0.501586	2.039875	0.034566	2.576026
82	77	*i_0_0_63		0.717567	0.666901	0.022039	1.406507
83	78	*i_0_0_64		0.196807	0.627309	0.018105	0.842221
84	79	*i_0_0_65		0.408447	1.052837	0.027858	1.489142
85	80	*i_0_0_66		0.564669	1.082873	0.026481	1.674024
86	81	*i_0_0_67		0.728837	0.580899	0.034026	1.343762
87	82	*i_0_0_68		0.582968	1.650301	0.034026	2.267296
88	83	*i_0_0_69		0.016072	0.032180	0.014353	0.062605
89	84	*i_0_0_70		0.941932	2.698965	0.014353	3.655250
90	85	*i_0_0_71		0.858899	4.132402	0.014353	5.005653
91	86	*i_0_0_72		0.808265	5.245085	0.014353	6.067703
92	87	*i_0_0_73		0.741922	7.032764	0.014353	7.789039
93	88	*i_0_0_74		0.718389	7.666884	0.014353	8.399626
94	89	*i_0_0_75		0.227407	2.143910	0.014353	2.385671
95	90	*i_0_0_76		0.227087	3.321438	0.014353	3.562878
96	91	*i_0_0_77		0.227503	1.369737	0.014353	1.611593
97	92	*i_0_0_78		0.235303	4.134295	0.014353	4.383952
98	93	*i_0_0_79		0.485926	4.964245	0.014353	5.464524
99	94						
100	95	*TOTAL		52.771923	174.204941	2.881584	229.858444

101

D3:

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1 Report Path Groups:
2 -----
3 | Path  |Weight|Critical |Worst
4 | Group |      |Range(ps)|Slack(ps)
5 -----
6 1 |default| 1.000|    0.0| 1044.3
7 2 |I2R    | 1.000|    0.0| 397.7
8 3 |I2O    | 1.000|    0.0|<ill>
9 4 |R2O    | 1.000|    0.0| 934.8
10 -----
1 warning: No library characterized for (process = 1.00 voltage = 0.85 temperature = 25.00) can be found in the
2 Report Power (instances with prefix '*' are included in total) :
3 -----
4 | Instance          | Internal Power(uw) | Switching Power(uw) | Leakage Power(uw) | Total Power(uw)
5 -----
6 1 |*display_reg[2]   | 2.444616| 2.604738| 0.079112| 5.128467
7 2 |*display_reg[1]   | 2.444283| 2.575281| 0.079112| 5.098677
8 3 |*display_reg[0]   | 2.444263| 2.573496| 0.079112| 5.096871
9 4 |*out_reg[5]       | 2.444354| 2.581530| 0.079112| 5.104996
10 5 |*out_reg[4]      | 2.444334| 2.579745| 0.079112| 5.103190
11 6 |*out_reg[3]      | 2.444277| 2.574725| 0.079112| 5.098115
12 7 |*out_reg[2]      | 2.444610| 2.604182| 0.079112| 5.127904
13 8 |*out_reg[1]      | 2.444648| 2.607530| 0.079112| 5.131290
14 9 |*out_reg[0]      | 2.444628| 2.605745| 0.079112| 5.129485
15 10 |*State_reg[2]    | 0.953645| 2.090782| 0.079112| 3.123539
16 11 |*State_reg[1]    | 1.246195| 4.413481| 0.079112| 5.738789
17 12 |*State_reg[0]    | 2.447663| 6.988895| 0.079112| 9.515670
18 13 |*i_0_0_0         | 0.014158| 0.010014| 0.026832| 0.051004
19 14 |*i_0_0_1         | 0.018111| 0.009062| 0.032601| 0.059774
20 15 |*i_0_0_2         | 0.086332| 0.076562| 0.014353| 0.177247
21 16 |*i_0_0_3         | 0.120102| 1.113346| 0.022619| 1.256068
22 17 |*i_0_0_4         | 0.029980| 0.035603| 0.032601| 0.098184
23 18 |*i_0_0_5         | 0.145887| 0.090288| 0.022619| 0.258794
24 19 |*i_0_0_6         | 0.387516| 1.583037| 0.017393| 1.987947
25 20 |*i_0_0_7         | 0.192333| 0.134386| 0.027858| 0.354578
26 21 |*i_0_0_8         | 0.083897| 0.149133| 0.018105| 0.251134
27 22 |*i_0_0_9         | 0.028045| 0.031306| 0.014353| 0.073704
28 23 |*i_0_0_10        | 0.070111| 0.457157| 0.033938| 0.561206
29 24 |*i_0_0_11        | 0.262128| 0.232465| 0.014353| 0.508946
30 25 |*i_0_0_12        | 0.445771| 3.380439| 0.022619| 3.848829
31 26 |*i_0_0_13        | 0.231804| 0.145048| 0.026832| 0.403683
32 27 |*i_0_0_14        | 0.108280| 0.037024| 0.024415| 0.169719
33 28 |*i_0_0_15        | 0.543320| 0.298901| 0.022039| 0.864260
34 29 |*i_0_0_16        | 0.233680| 0.482171| 0.021200| 0.737051
35 30 |*i_0_0_17        | 0.152990| 0.559141| 0.021200| 0.733330
36 31 |*i_0_0_18        | 0.064816| 0.189814| 0.014353| 0.268983
37 32 |*i_0_0_19        | 0.122852| 1.282784| 0.022619| 1.428255
38 33 |*i_0_0_20        | 0.152131| 0.206972| 0.022619| 0.381722
39 34 |*i_0_0_21        | 0.308705| 0.615181| 0.021200| 0.945086
40 35 |*i_0_0_22        | 0.173568| 0.768546| 0.014353| 0.956467
41 36 |*i_0_0_23        | 0.293421| 2.455544| 0.022619| 2.771585
42 37 |*i_0_0_24        | 0.330807| 0.846003| 0.034566| 1.213655
43 38 |*i_0_0_25        | 0.091504| 0.272271| 0.014353| 0.378128
44 39 |*i_0_0_26        | 0.131091| 1.805071| 0.021200| 1.957362
45 40 |*i_0_0_27        | 0.647328| 2.153851| 0.017393| 2.818572

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46	41	*i_0_0_28		0.514952	0.281074	0.022039	0.818065
47	42	*i_0_0_29		0.230455	1.188758	0.027858	1.447071
48	43	*i_0_0_30		0.046450	0.160775	0.018127	0.225352
49	44	*i_0_0_31		0.430749	0.597080	0.034026	1.061855
50	45	*i_0_0_32		0.228236	0.698710	0.026832	0.953778
51	46	*i_0_0_33		0.388185	1.610158	0.021200	2.019543
52	47	*i_0_0_34		0.397642	1.340988	0.021200	1.759829
53	48	*i_0_0_35		0.173076	0.527906	0.014353	0.715335
54	49	*i_0_0_36		0.411890	3.930947	0.022039	4.364875
55	50	*i_0_0_37		0.177317	0.120743	0.027858	0.325919
56	51	*i_0_0_38		0.263571	0.403823	0.017393	0.684788
57	52	*i_0_0_39		0.630354	3.359815	0.021200	4.011368
58	53	*i_0_0_40		0.469749	2.815580	0.014353	3.299683
59	54	*i_0_0_41		1.117174	12.045470	0.022619	13.185263
60	55	*i_0_0_42		0.704587	0.630440	0.024415	1.359441
61	56	*i_0_0_43		0.727183	0.626554	0.026481	1.380219
62	57	*i_0_0_44		0.796067	4.044455	0.021200	4.861721
63	58	*i_0_0_45		1.136616	1.977480	0.026481	3.140578
64	59	*i_0_0_46		0.704206	0.396736	0.024415	1.125357
65	60	*i_0_0_47		0.177404	1.206377	0.021200	1.404980
66	61	*i_0_0_48		0.044894	0.255460	0.021200	0.321554
67	62	*i_0_0_49		0.208140	1.242261	0.014353	1.464754
68	63	*i_0_0_50		0.438203	5.404646	0.026832	5.869680
69	64	*i_0_0_51		0.165754	0.714554	0.021200	0.901507
70	65	*i_0_0_52		0.224980	0.648603	0.014353	0.887936
71	66	*i_0_0_53		0.507071	4.455115	0.022039	4.984225
72	67	*i_0_0_54		0.376971	1.891098	0.017393	2.285462
73	68	*i_0_0_55		0.425672	2.143666	0.021200	2.590537
74	69	*i_0_0_56		0.739053	1.674047	0.022619	2.435719
75	70	*i_0_0_57		0.111985	0.218859	0.021200	0.352044
76	71	*i_0_0_58		0.308288	4.401180	0.014353	4.723821
77	72	*i_0_0_59		0.515412	7.909902	0.021200	8.446514
78	73	*i_0_0_60		0.272094	3.229532	0.014353	3.515979
79	74	*i_0_0_61		0.138544	1.559893	0.014353	1.712791
80	75	*i_0_0_62		0.106149	0.517845	0.014353	0.638347
81	76	*i_0_0_63		0.940043	2.731588	0.014353	3.685984
82	77	*i_0_0_64		0.859421	4.123376	0.014353	4.997150
83	78	*clk_gate_display_reg		1.402187	0.000000	0.059138	1.461324
84	79						
85	80	*TOTAL		49.631187	137.306763	2.394687	189.332642
86		-----+-----+-----+-----+-----+-----+-----+-----					

1 Report Physical info:

			Area (squm)	Leakage (uW)
5	Design Name	integ		
6	Total Instances	78	118	2.395
7	Macros	0	0	0.000
8	Pads	0	0	0.000
9	Phys	0	0	0.000
10	Blackboxes	0	0	0.000
11	Cells	78	118	2.395
12	Buffers	0	0	0.000
13	Inverters	16	9	0.230
14	Clock-Gates	1	4	0.059
15	Combinational	49	52	1.157
16	Latches	0	0	0.000
17	FlipFlops	12	54	0.949
18	Single-Bit FF	12	54	0.949
19	Multi-Bit FF	0	0	0.000
20	Clock-Gated	12		
21	Bits	12	54	0.949
22	Load-Enabled	0		
23	Clock-Gated	12		
24	Tristate Pin Count	0		
25	Physical Info	Placed		
26	Chip Size (mm x mm)	0.076 x 0.076	5745	
27	Fixed Cell Area		0	
28	Phys Only	0	0	
29	Placeable Area		243	
30	Movable Cell Area		118	
31	Utilization (%)	48		
32	Chip Utilization (%)	48		
33	Total Wire Length (mm)	0.838		
34	Longest Wire (mm)	0.039		
35	Average Wire (mm)	0.038		

D4:

```
1 Report Path Groups:
2 -----
3 | Path  |Weight|Critical |Worst
4 | Group |      |Range(ps)|Slack(ps)
5 -----
6 1 |default| 1.000|    0.0| 1164.9
7 2 |I2R    | 1.000|    0.0| 571.0
8 3 |I2O    | 1.000| 0.0|<ill>
9 4 |R2O    | 1.000|    0.0| 935.6
10 -----
1 Report Physical info:
2 -----
3 |          |          |Area (squm)|Leakage (uW)
4 -----
5 Design Name |integ   |          |
6 Total Instances | 37| 84| 1.570
7 Macros | 0| 0| 0.000
8 Pads | 0| 0| 0.000
9 Phys | 0| 0| 0.000
10 Blackboxes | 0| 0| 0.000
11 Cells | 37| 84| 1.570
12 Buffers | 0| 0| 0.000
13 Inverters | 3| 2| 0.043
14 Clock-Gates | 1| 4| 0.059
15 Combinational | 21| 24| 0.519
16 Latches | 0| 0| 0.000
17 FlipFlops | 12| 54| 0.949
18 Single-Bit FF | 12| 54| 0.949
19 Multi-Bit FF | 0| 0| 0.000
20 Clock-Gated | 12| | |
21 Bits | 12| 54| 0.949
22 Load-Enabled | 0| | |
23 Clock-Gated | 12| | |
24 Tristate Pin Count | 0| | |
25 Physical Info |Placed   |          |
26 Chip Size (mm x mm) | 0.072 x 0.072| 5162|
27 Fixed Cell Area | | 0|
28 Phys Only | 0| 0|
29 Placeable Area | | 132|
30 Movable Cell Area | | 84|
31 Utilization (%) | 63| |
32 Chip Utilization (%) | 63| |
33 Total Wire Length (mm) | 0.797| |
34 Longest Wire (mm) | 0.037| |
35 Average Wire (mm) | 0.036| |
36 -----
```

```

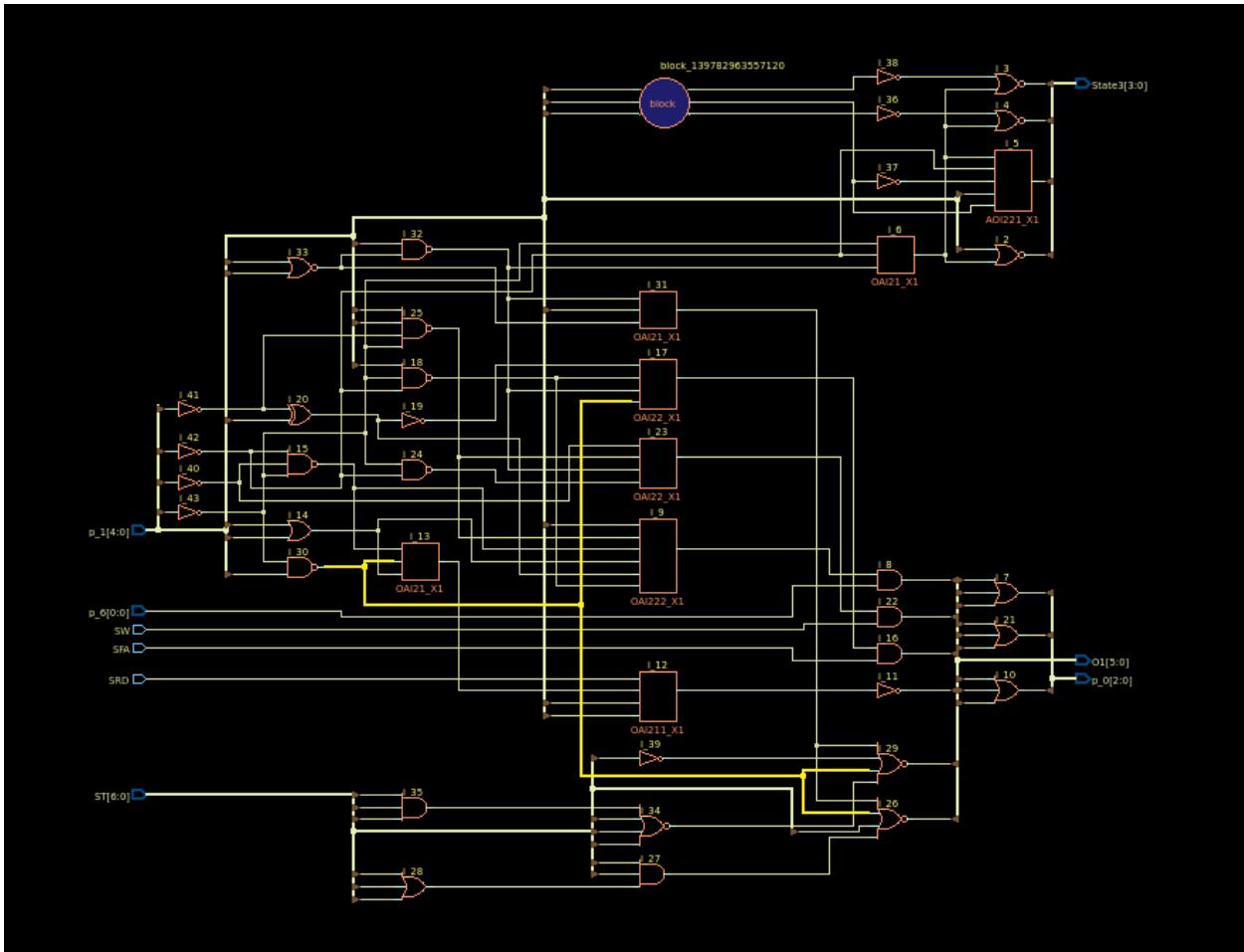
1 warning: No library characterized for (process = 1.00 voltage = 0.85 temperature = 25.00) can be found in the
2 Report Power (instances with prefix '*' are included in total) :
3 -----
4 | Instance | Internal Power(uw) | Switching Power(uw) | Leakage Power(uw) | Total Power(uw)
5 -----
6 1  /*display_reg[2] | 0.119279 | 0.124111 | 0.079112 | 0.322502
7 2  /*display_reg[1] | 2.831355 | 2.947846 | 0.079112 | 5.858314
8 3  /*display_reg[0] | 2.831311 | 2.943968 | 0.079112 | 5.854391
9 4  /*out_reg[5] | 0.588080 | 0.612965 | 0.079112 | 1.280157
10 5  /*out_reg[4] | 0.171519 | 0.178885 | 0.079112 | 0.429517
11 6  /*out_reg[3] | 0.344382 | 0.359359 | 0.079112 | 0.782853
12 7  /*out_reg[2] | 0.088178 | 0.092013 | 0.079112 | 0.259304
13 8  /*out_reg[1] | 0.015101 | 0.015747 | 0.079112 | 0.109960
14 9  /*out_reg[0] | 0.017212 | 0.017948 | 0.079112 | 0.114273
15 10 /*State_reg[2] | 0.175141 | 0.301720 | 0.079112 | 0.555974
16 11 /*State_reg[1] | 1.346454 | 1.027794 | 0.079112 | 2.453360
17 12 /*State_reg[0] | 1.244668 | 1.358831 | 0.079112 | 2.682612
18 13 /*i_0_0_0 | 0.407421 | 1.075530 | 0.021200 | 1.504151
19 14 /*i_0_0_1 | 0.033273 | 0.064302 | 0.026481 | 0.124056
20 15 /*i_0_0_2 | 0.617268 | 1.091025 | 0.026832 | 1.735125
21 16 /*i_0_0_3 | 0.335126 | 4.995475 | 0.021200 | 5.351800
22 17 /*i_0_0_4 | 0.234715 | 1.110965 | 0.014353 | 1.360033
23 18 /*i_0_0_5 | 0.349846 | 0.153572 | 0.025066 | 0.528484
24 19 /*i_0_0_6 | 0.496761 | 2.990985 | 0.014353 | 3.502100
25 20 /*i_0_0_7 | 0.004342 | 0.002493 | 0.018105 | 0.024939
26 21 /*i_0_0_8 | 0.530426 | 0.907809 | 0.026832 | 1.465067
27 22 /*i_0_0_9 | 0.704191 | 0.358240 | 0.024415 | 1.086846
28 23 /*i_0_0_10 | 1.112299 | 1.006695 | 0.026481 | 2.145476
29 24 /*i_0_0_11 | 0.013532 | 0.037448 | 0.018105 | 0.069085
30 25 /*i_0_0_12 | 0.005585 | 0.014183 | 0.026832 | 0.046599
31 26 /*i_0_0_13 | 0.120216 | 0.178174 | 0.026481 | 0.324872
32 27 /*i_0_0_14 | 0.610272 | 0.580041 | 0.026481 | 1.216795
33 28 /*i_0_0_15 | 0.662401 | 0.251458 | 0.024415 | 0.938274
34 29 /*i_0_0_16 | 1.080399 | 0.927756 | 0.014353 | 2.022508
35 30 /*i_0_0_17 | 0.509867 | 0.422040 | 0.026832 | 0.958739
36 31 /*i_0_0_18 | 0.561596 | 0.442590 | 0.018105 | 1.022291
37 32 /*i_0_0_19 | 0.006302 | 0.016309 | 0.034566 | 0.057177
38 33 /*i_0_0_20 | 0.119333 | 0.112948 | 0.026481 | 0.258763
39 34 /*i_0_0_21 | 0.162132 | 0.066550 | 0.024415 | 0.253097
40 35 /*i_0_0_22 | 0.017887 | 0.016008 | 0.025066 | 0.058961
41 36 /*i_0_0_23 | 0.034971 | 0.013710 | 0.024415 | 0.073096
42 37 /*clk_gate_display_reg | 1.355973 | 0.000000 | 0.059138 | 1.415111
43 38 | | | | |
44 39 /*TOTAL | 19.858812 | 26.817493 | 1.570349 | 48.246651
45 -----

```

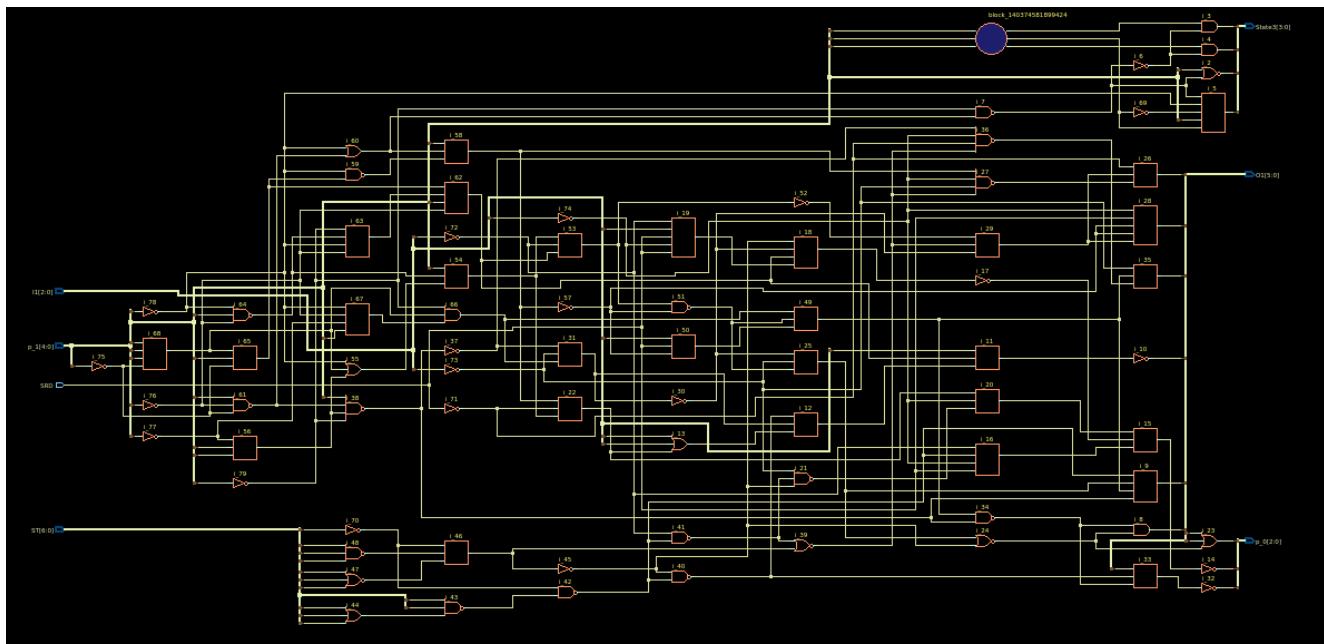
Resulting Schema from Synthesis:

D1: 13 States Mono, D2: 13 States Multi, D3: 14253 Design, D4: Seq Mono Check

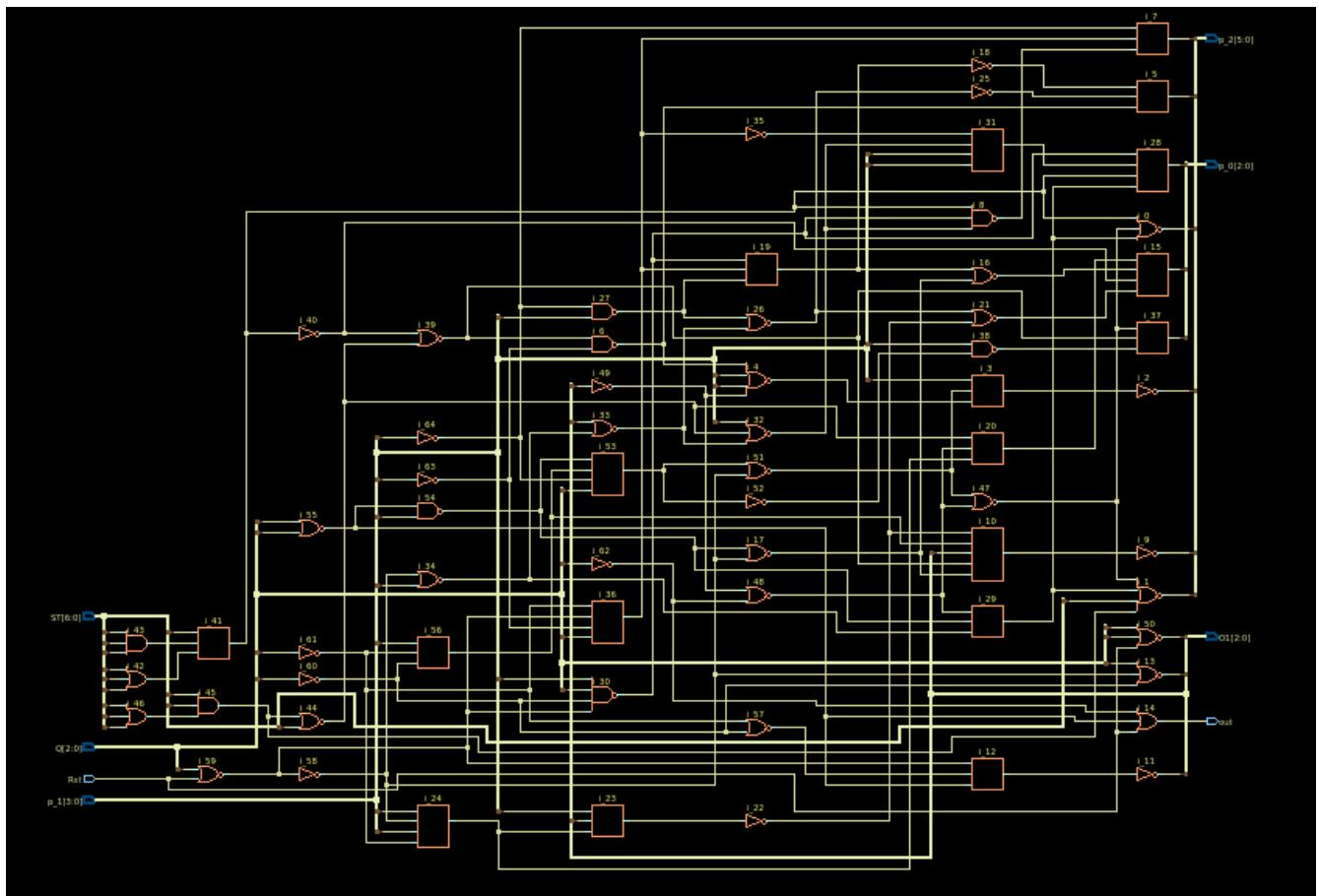
D1:



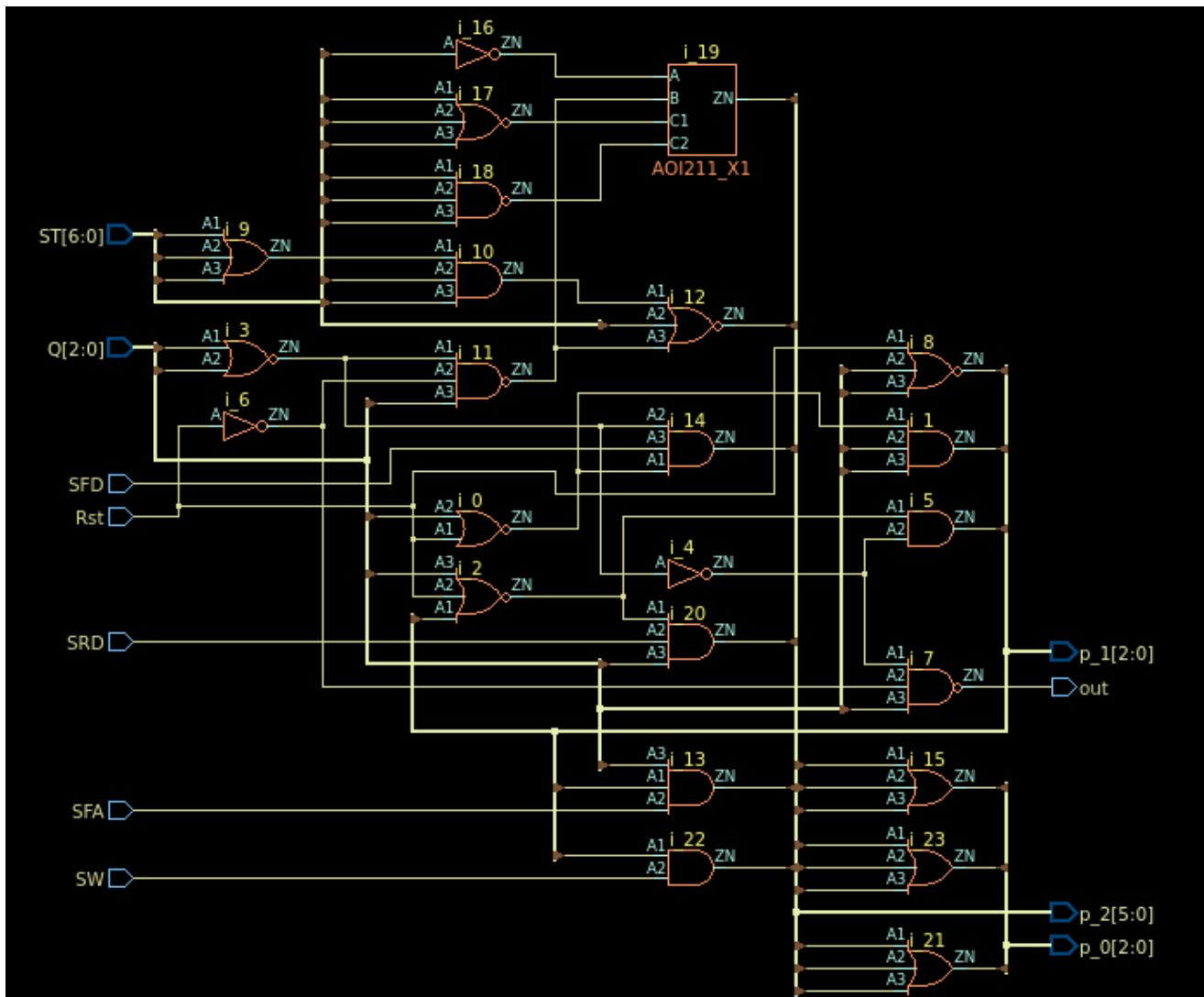
D2:



D3:

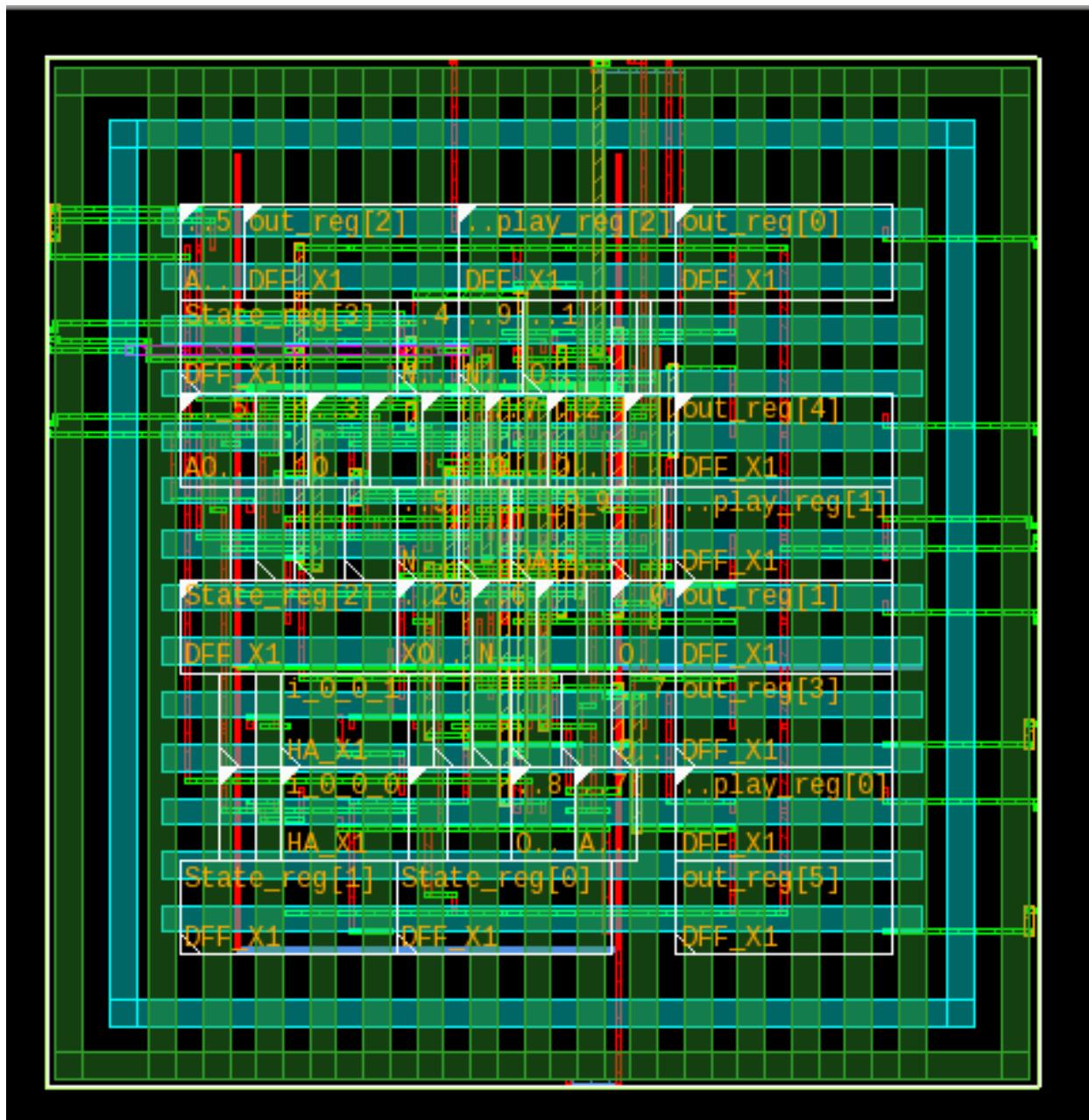


D4:

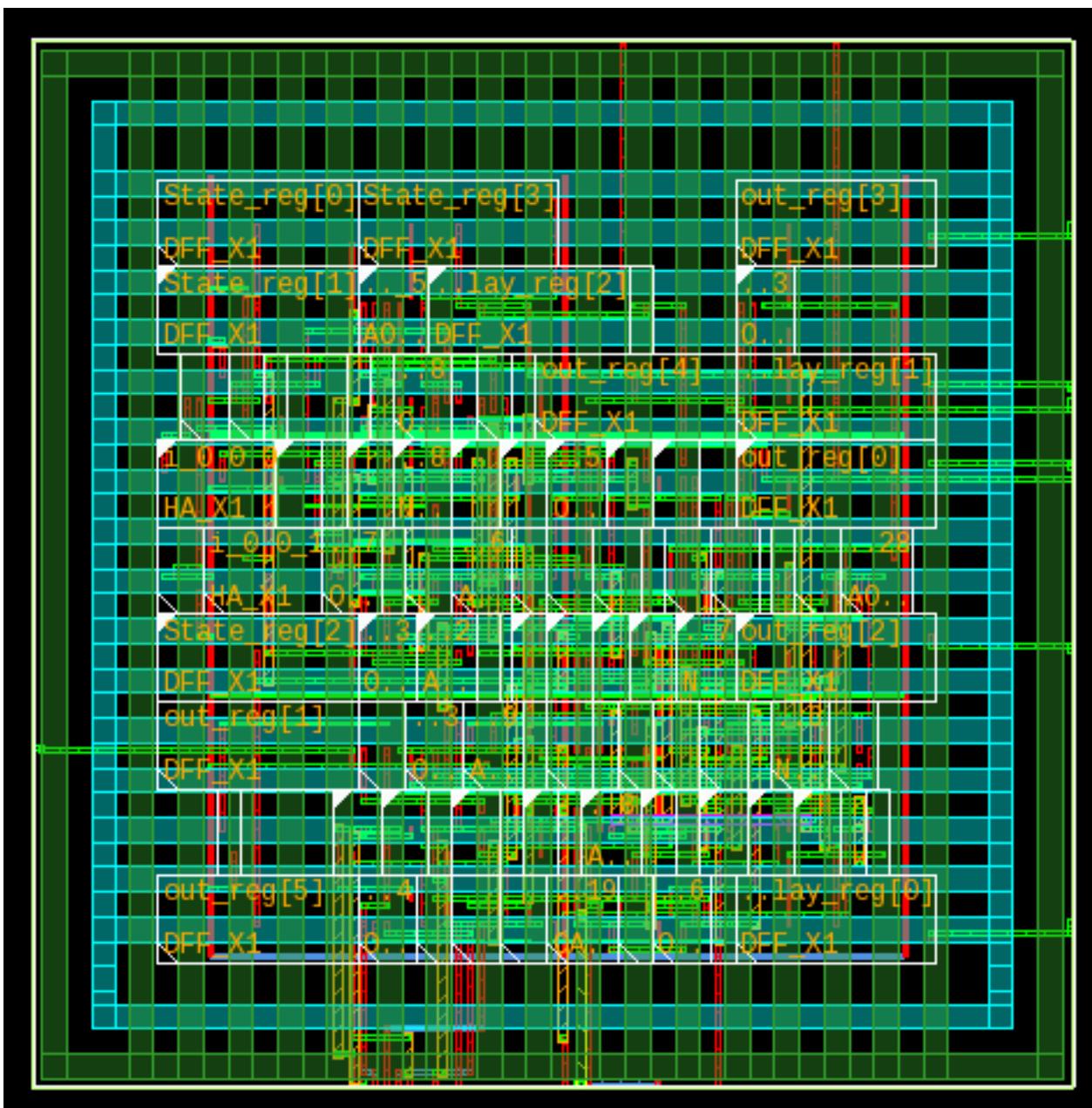


Resulting Chip Schematic from Floor Planning:

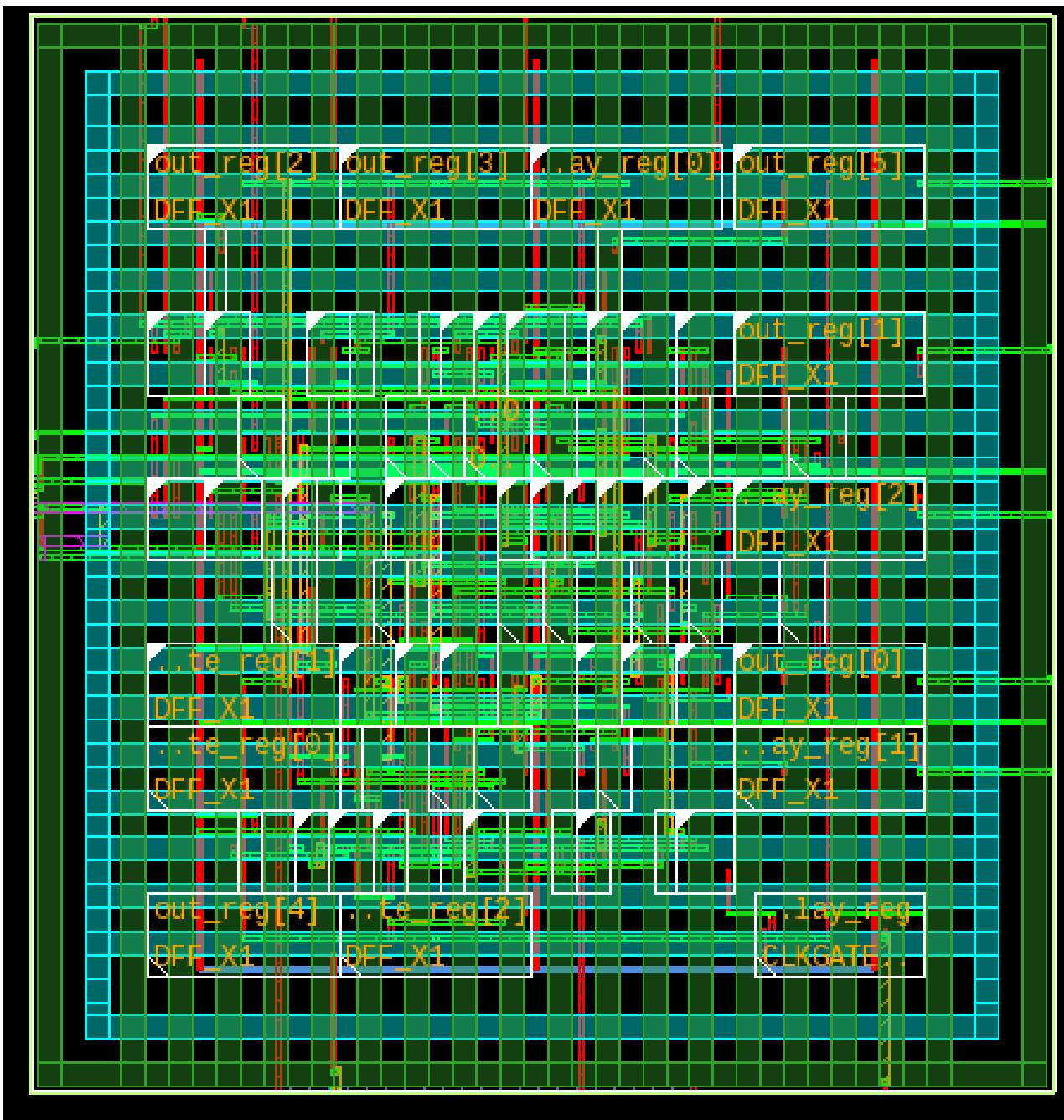
D1:



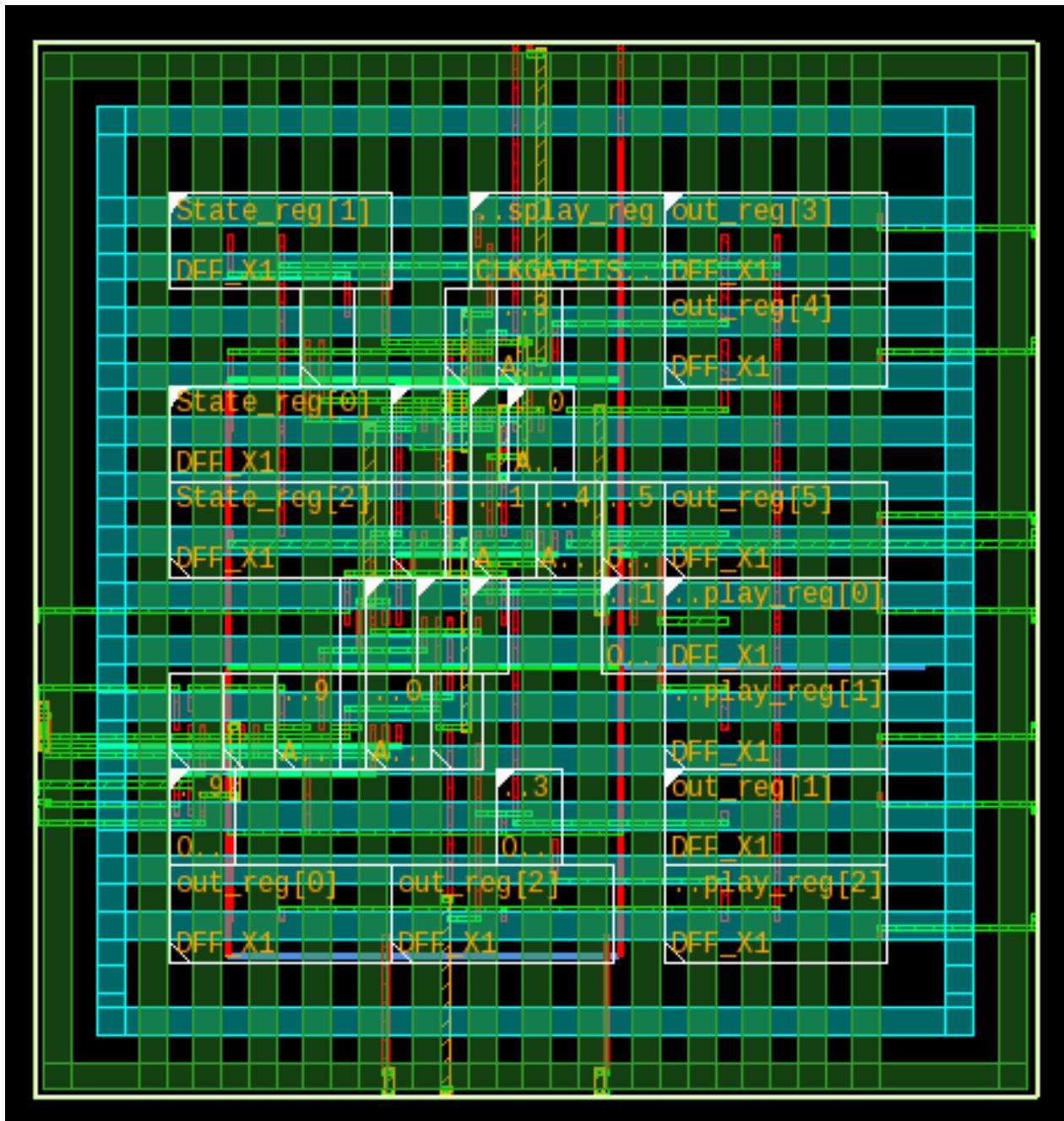
D2:



D3:



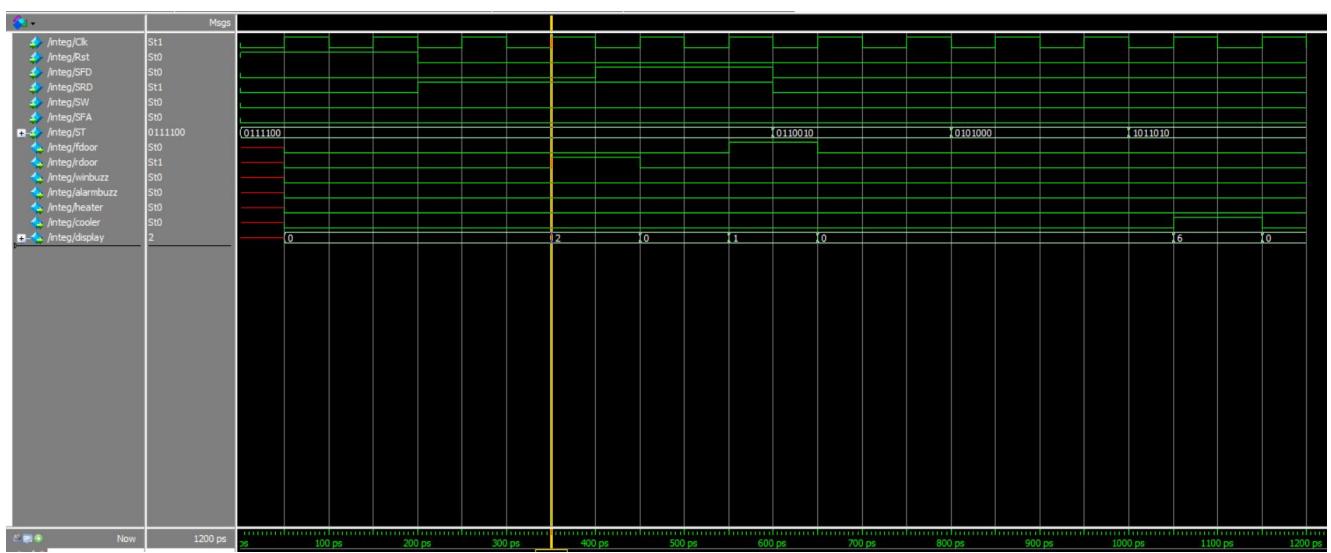
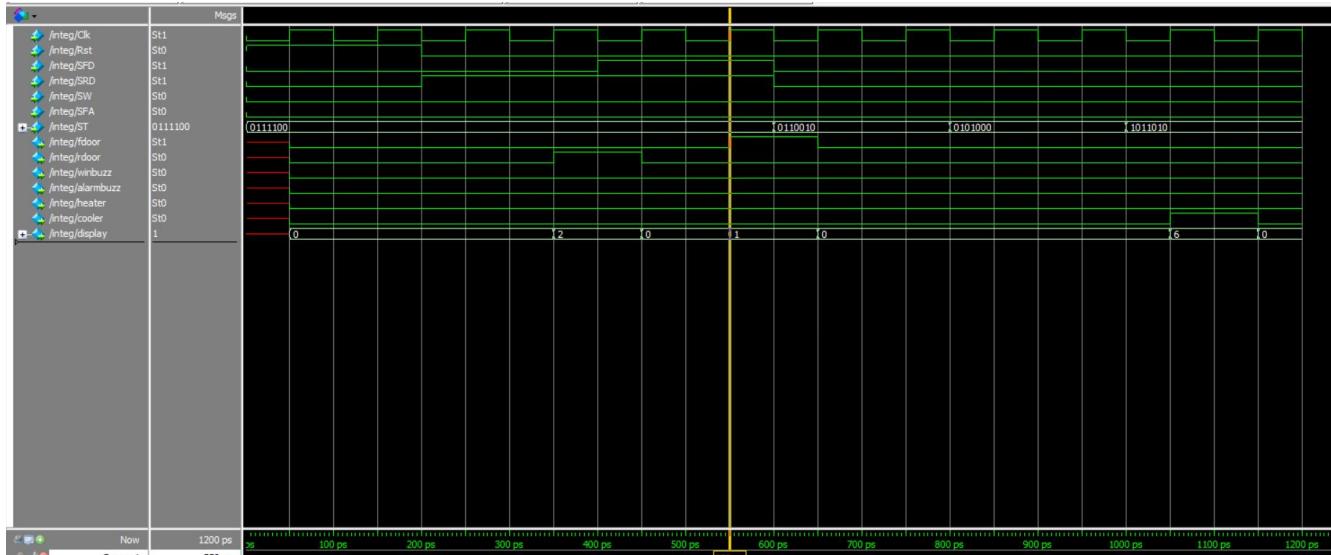
D4:



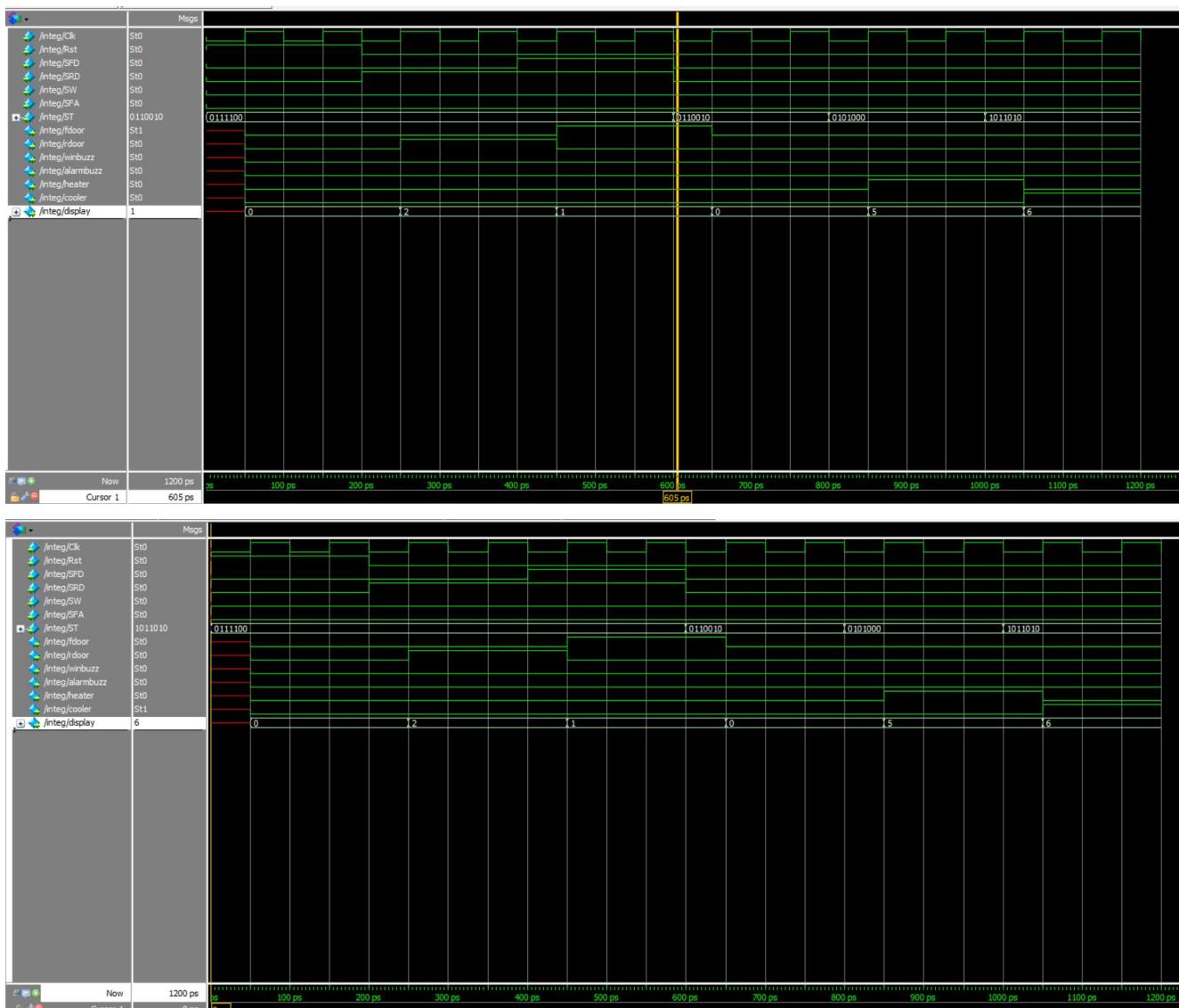
Pre & Post Synth. Simulation:

D1: 13 States Mono, D2: 13 States Multi, D3: 14253 Design, D4: Seq Mono Check

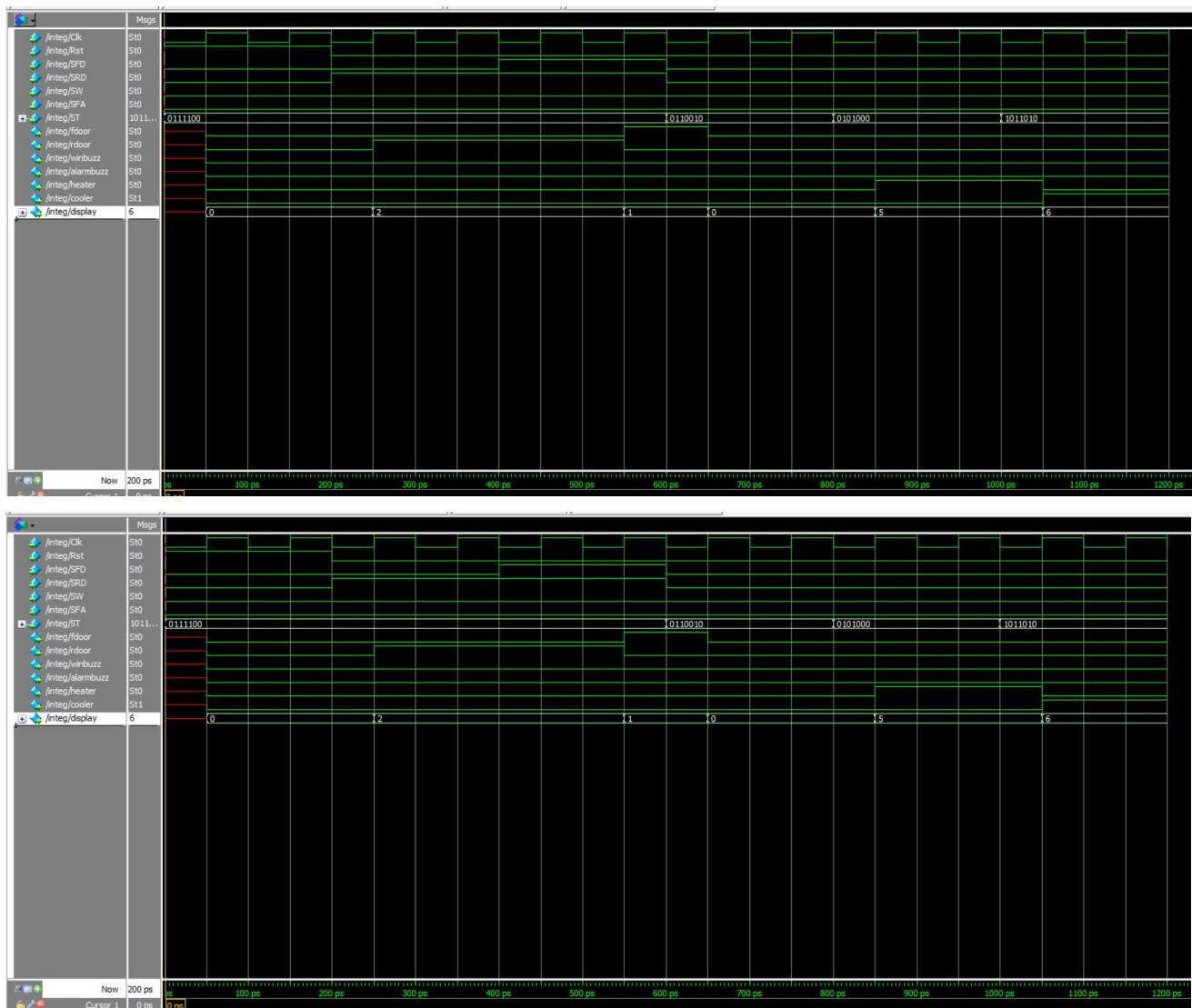
D1:



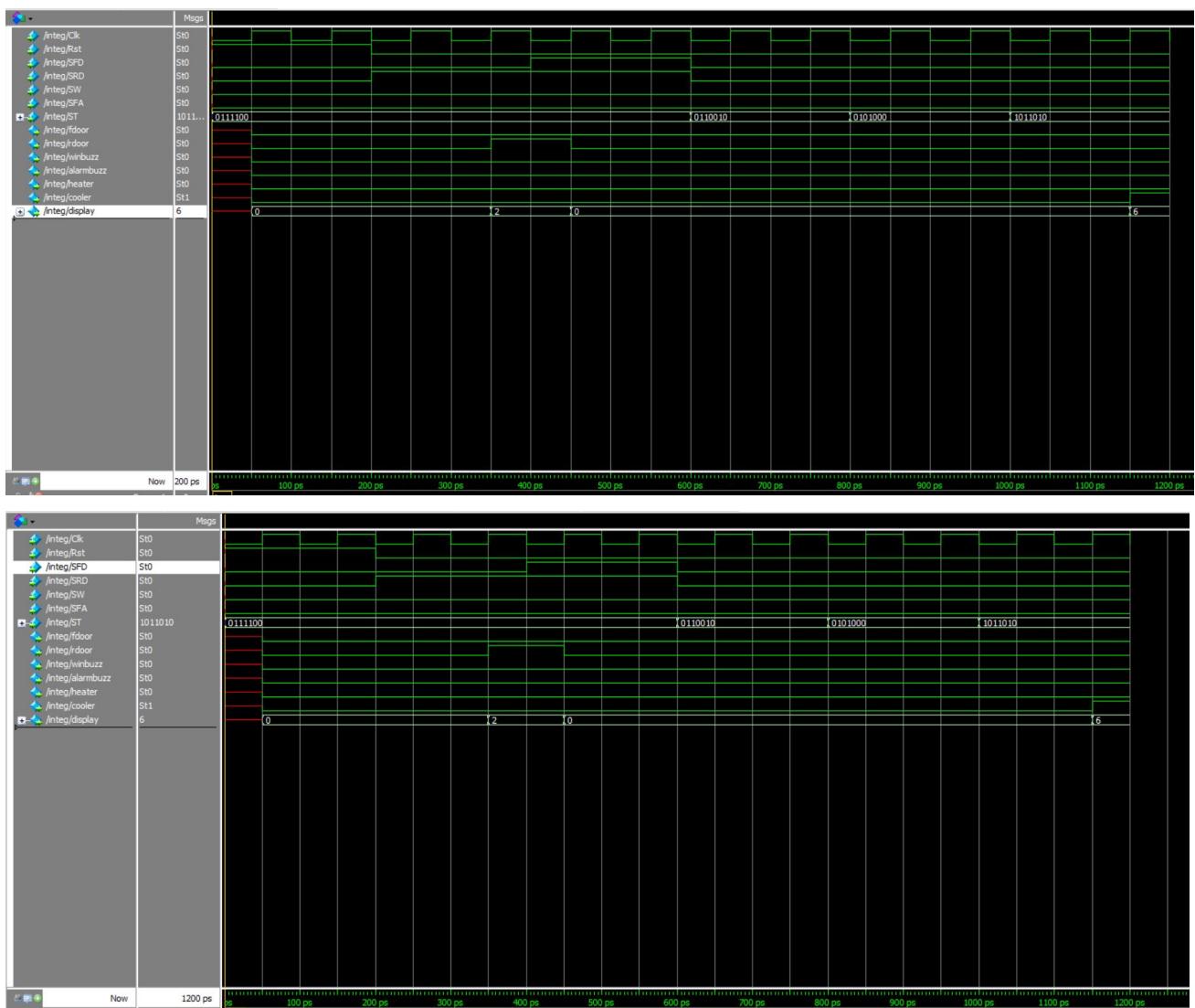
D2:



D3:



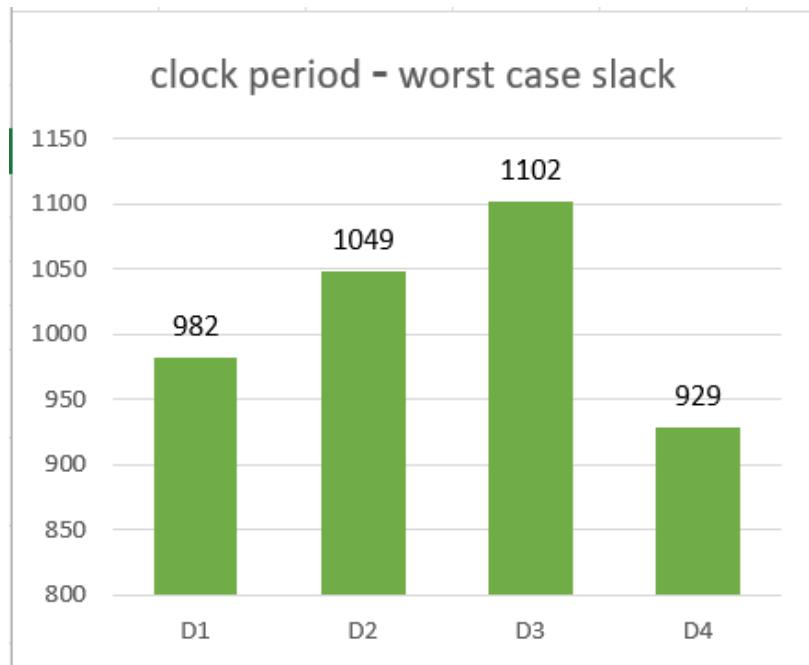
D4:



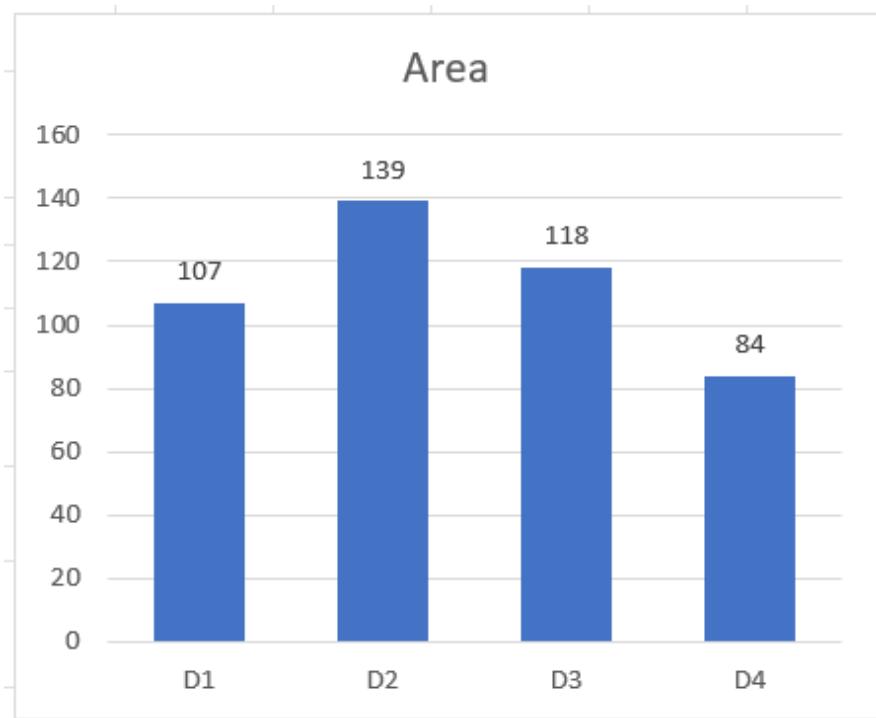
Comparing Proposed Designs by Metrics:

D1: 13 States Mono, D2: 13 States Multi, D3: 14253 Design, D4: Seq Mono Check

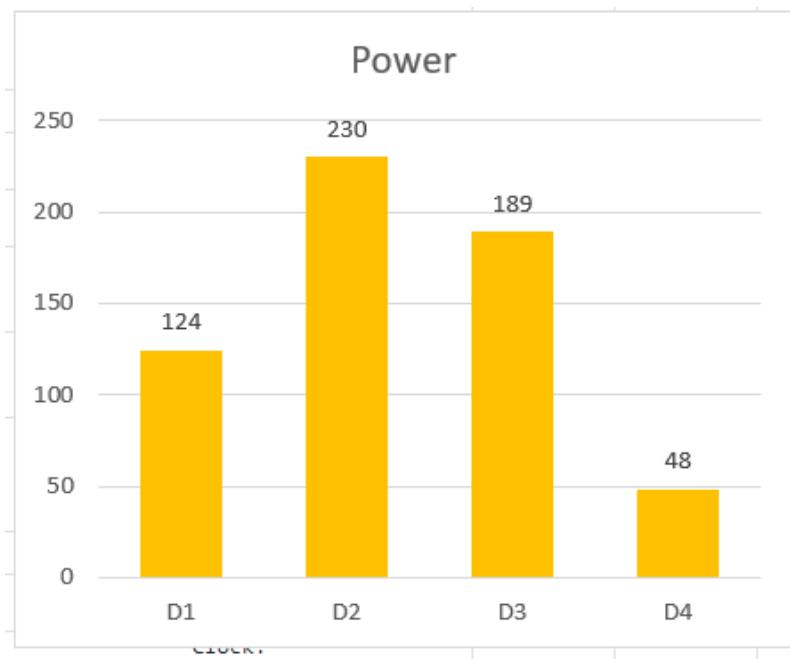
By (Cycle Period - Worst Slack Time):



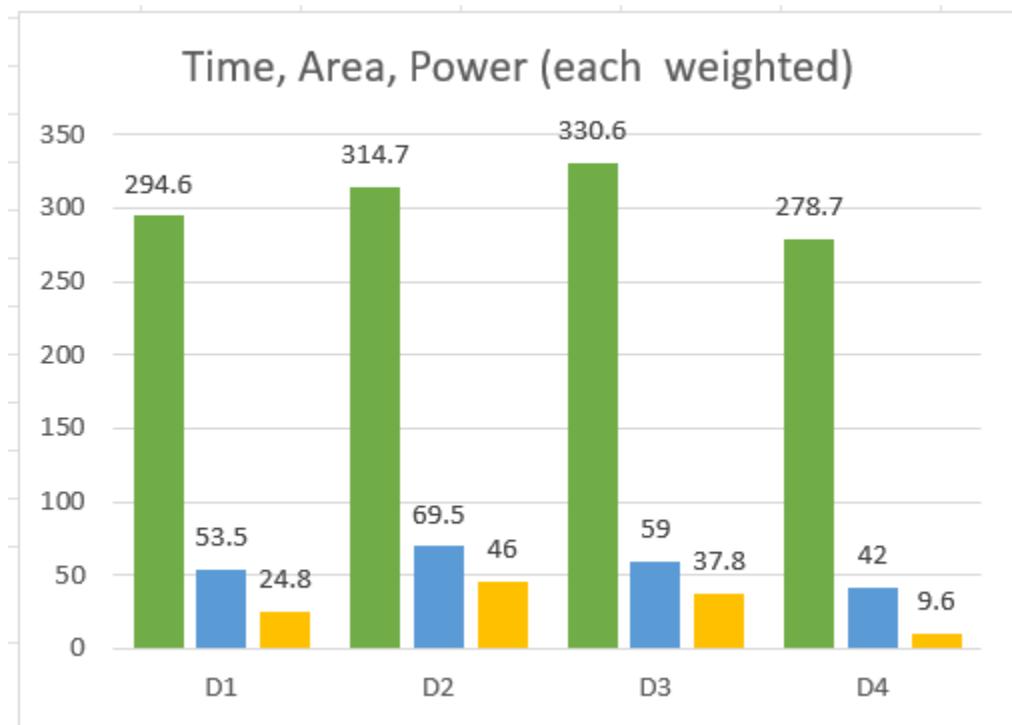
By Area:



By Power:

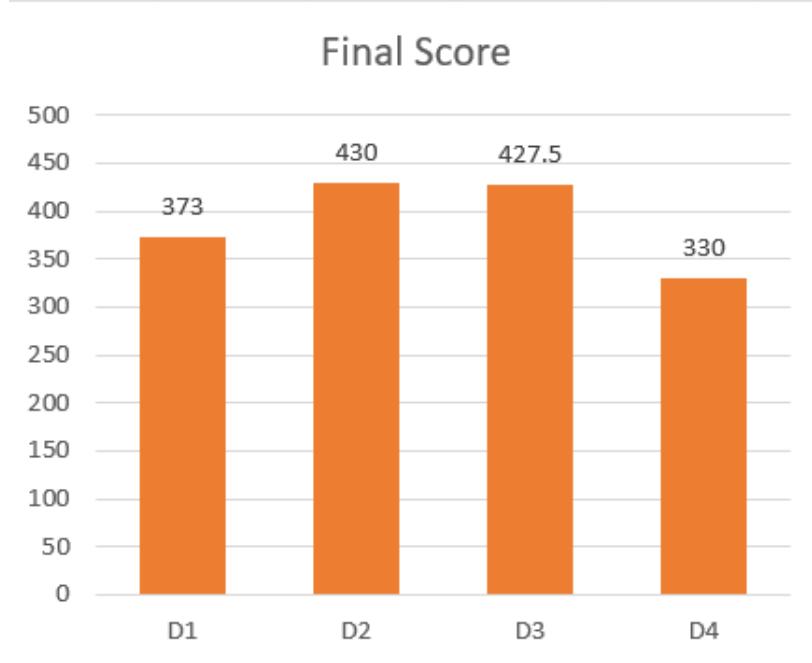


Collective Comparison (side by side):



(note time was divided by 10 to have a suitable visualization)

By Weighted Score:



From These Graphs We considered optimizing “D4: Seq Mono Check”, Since it clearly has better metrics than the other designs, “D1: 13 States Mono” also was good in some metrics, we tried making some optimizations and got a score of 362. So, D4 made more sense to work on.

Comparing Optimizations on Design 4 by Metrics:

We tried optimizing the design itself multiple times. While that did have some effects, they were very minor. On the other hand, we changed the input delay to reach the bottleneck of the minimum slack, we found that anything below 0.3ns input delay had no effects on the minimum slack. So we used 0.3ns instead of the initial 0.7ns. Below we compare the results:

Design	Area	Power	Clock Period - Min Slack	Score
Old Results	84	48.246651	971.0	330.5
After Optimization	84	48.246651	935.6	220.97

Score Ratio vs Other Designs	D1	D2	D3	Old D4
Optimized D4	%59.24	%51.39	%51.69	%66.86