2Pai Semi

Enhanced ESD, 3.0 kV rms/5.0 kV rms 150Kbps Triple-Channel Digital Isolators

Data Sheet **π130U/π131U**

FEATURES

- **Ultra-low power consumption (150Kbps): 0.62mA/Channel**
- **High data rate: 150kbps**
- **High common-mode transient immunity: 250 kV/μs**
- **High robustness to radiated and conducted noise**
- **Isolation voltages:**
  - **π13xx3x: AC 3000Vrms**
  - **π13xx6x: AC 5000Vrms**
- **High ESD rating:**
  - **ESDA/JEDEC JS-001-2017**
  - **Human body model (HBM) ±8kV**
- **Safety and regulatory approvals：**
  - **UL certificate number: E494497**
    - **3000Vrms/5000Vrms for 1 minute per UL 1577**
  - **CSA Component Acceptance Notice 5A**
  - **VDE certificate number: 40053041/40052896**
    - **DIN VDE V 0884-11:2017-01**
    - **V_{IORM} =565V peak/1200V peak**
  - **CQC certification per GB4943.1-2011**
- **3 V to 5.5 V level translation**
- **Wide temperature range: -40°C to 125°C**
- **RoHS-compliant, NB SOIC-16, WB SOIC-16 and SSOP16 package**

APPLICATIONS

- **General-purpose multichannel isolation**
- **Industrial field bus isolation**
- **Isolation Industrial automation systems**
- **Isolated switch mode supplies**
- **Isolated ADC, DAC**
- **Motor control**

GENERAL DESCRIPTION

The π1xxxxx is a 2PaiSemi digital isolators product family that includes over hundreds of digital isolator products. By using maturated standard semiconductor CMOS technology and 2PaiSemi ***iDivider®*** technology, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators.

Intelligent voltage divider technology (***iDivider®*** technology) is a new generation digital isolator technology invented by 2PaiSemi. It uses the principle of capacitor voltage divider to transmit voltage signal directly cross the isolator capacitor without signal modulation and demodulation.

The π1xxxxx isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 1.5 kV rms to 5.0 kV rms and the data rate from DC up to 600Mbps (see the Ordering Guide). The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier. The fail-safe state is available in which the outputs transition to a preset state when the input power supply is not applied.

FUNCTIONAL BLOCK DIAGRAMS

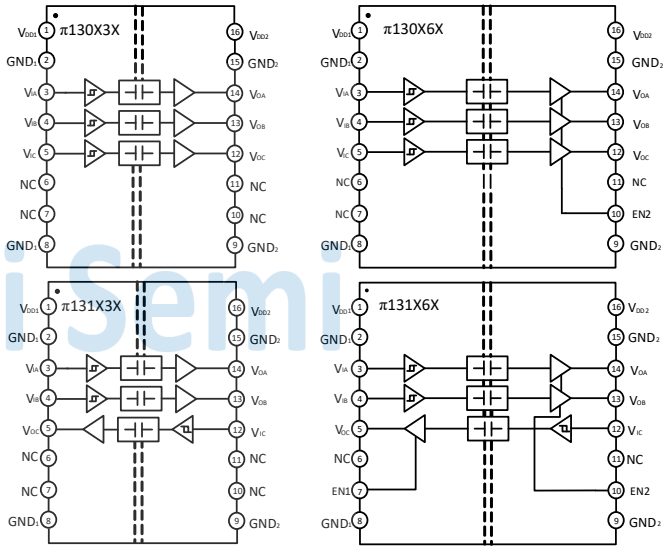


Figure 1.π130xxx/π131xxx functional Block Diagram

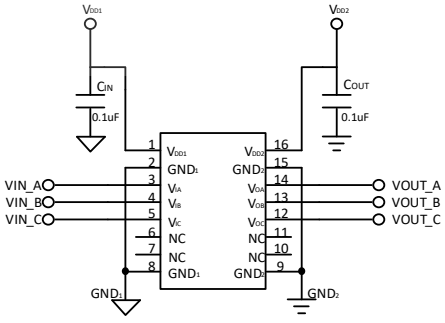


Figure 2.π130x3x Typical Application Circuit

Room 307-309, No.22, Boxia Road, Pudong New District, Shanghai, 201203, China
021-50850681

http://www.rpsemi.com/

PIN CONFIGURATIONS AND FUNCTIONS

Table 1.π130Uxx Pin Function Descriptions

Pin No.	Name	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	NC	No connect.
7	NC	No connect.
8	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
9	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC/EN2	No connect for π130U3X. Output enable for π130U6X. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
11	NC	No connect.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
16	V_{DD2}	Supply Voltage for Isolator Side 2.

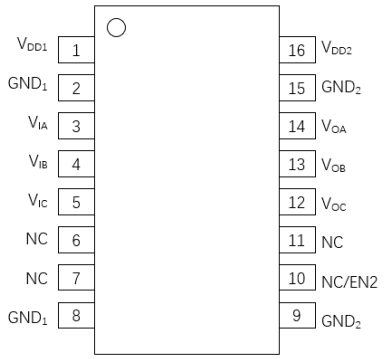


Figure 3.π130Uxx Pin Configuration

Table 2.π131Uxx Pin Function Descriptions

Pin No.	Name	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{OC}	Logic Output C.
6	NC	No connect.
7	NC/EN1	No connect for π131U3X. Output enable for π131U6X. Output pins on side 1 are enabled when EN1 is high or open and in high-impedance state when EN1 is low.
8	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
9	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC/EN2	No connect for π131U3X. Output enable for π131U6X. Output pins on side 2 are enabled when EN2 is high or open and in high-impedance state when EN2 is low.
11	NC	No connect.
12	V_{IC}	Logic Input C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
15	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
16	V_{DD2}	Supply Voltage for Isolator Side 2.

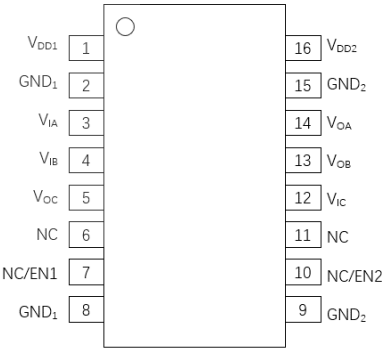


Figure 4.π131Uxx Pin Configuration

ABSOLUTE MAXIMUM RATINGS

Table 3.Absolute Maximum Ratings[4]
TA = 25°C, unless otherwise noted.

Parameter	Rating
Supply Voltages (V_{DD1}-GND_1, V_{DD2}-GND_2)	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB})[1]	−0.5 V to V_{DDx} + 0.5 V
Output Voltages (V_{OA}, V_{OB})[1]	−0.5 V to V_{DDx} + 0.5 V
Average Output Current per Pin[2] Side 1 Output Current (I_{O1})	−10 mA to +10 mA
Average Output Current per Pin[2] Side 2 Output Current (I_{O2})	−10 mA to +10 mA
Common-Mode Transients Immunity[3]	−300 kV/µs to +300 kV/µs
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +125°C

Notes:
[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.
[2] See Figure 5 for the maximum rated current values for various temperatures.
[3] See Figure 16 for Common-mode transient immunity (CMTI) measurement.
[4] Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

RECOMMENDED OPERATING CONDITIONS

Table 4.Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DDx} [1]	3		5.5	V
High Level Input Signal Voltage	V_{IH}	0.7*V_{DDx}[1]		V_{DDx}[1]	V
Low Level Input Signal Voltage	V_{IL}	0		0.3*V_{DDx}[1]	V
High Level Output Current	I_{OH}	-6			mA
Low Level Output Current	I_{OL}			6	mA
Data Rate		0		150	Kbps
Junction Temperature	T_J	-40		150	°C
Ambient Operating Temperature	T_A	-40		125	°C

Notes:
[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

Truth Tables

Table 5.π130U3x/π131U3x Truth Table

V_{Ix} Input[1]	V_{DDI} State[1]	V_{DDO} State[1]	Default Low V_{Ox} Output[1]	Default High V_{Ox} Output[1]	Test Conditions /Comments
Low	Powered[2]	Powered[2]	Low	Low	Normal operation
High	Powered[2]	Powered[2]	High	High	Normal operation
Open	Powered[2]	Powered[2]	Low	High	Default output
Don't Care[4]	Unpowered[3]	Powered[2]	Low	High	Default output[5]
Don't Care[4]	Powered[2]	Unpowered[3]	High Impedance	High Impedance	

Notes:
[1] V_{Ix}/V_{Ox} are the input/output signals of a given channel (A or B). V_{DDI}/V_{DDO} are the supply voltages on the input/output signal sides of this given channel.
[2] Powered means V_{DDx}≥ 2.95V
[3] Unpowered means V_{DDx} < 2.30V
[4] Input signal (V_{Ix}) must be in a low state to avoid powering the given V_{DDI}[1] through its ESD protection circuitry.
[5] If the V_{DDI} goes into unpowered status, the channel outputs the default logic signal after around 1us. If the V_{DDI} goes into powered status, the channel outputs the input status logic signal after around 3us.

Table 6.π130U6x/π131U6x Truth Table

V_{Ix} Input[1]	EN1/2 State	V_{DDI} State[1]	V_{DDO} State[1]	Default Low V_{Ox} Output[1]	Default High V_{Ox} Output[1]	Test Conditions /Comments
Low	High or NC	Powered[2]	Powered[2]	Low	Low	Normal operation
High	High or NC	Powered[2]	Powered[2]	High	High	Normal operation
Don't Care[4]	L	Powered[2]	Powered[2]	High Impedance	High Impedance	Disabled
Open	High or NC	Powered[2]	Powered[2]	Low	High	Default output[5]
Don't Care[4]	High or NC	Unpowered[3]	Powered[2]	Low	High	Default output[5]
Don't Care[4]	L	Unpowered[3]	Powered[2]	High Impedance	High Impedance	
Don't Care[4]	Don't Care[4]	Powered[2]	Unpowered[3]	High Impedance	High Impedance	

Notes:

[1] V_{Ix}/V_{Ox} are the input/output signals of a given channel (A or B). V_{DDI}/V_{DDO} are the supply voltages on the input/output signal sides of this given channel.

[2] Powered means $V_{DDx} \geq 2.95V$

[3] Unpowered means $V_{DDx} < 2.30V$

[4] Input signal (V_{Ix}) must be in a low state to avoid powering the given V_{DDI}[1] through its ESD protection circuitry.

[5] If the V_{DDI} goes into unpowered status, the channel outputs the default logic signal after around 1us. If the V_{DDI} goes into powered status, the channel outputs the input status logic signal after around 3us.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Table 7.π13xU3x Switching Specifications

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Minimum Pulse Width	PW			6.5	us	Within pulse width distortion (PWD) limit
Maximum Data Rate		150			Kbps	Within pulse width distortion (PWD) limit
Propagation Delay Time[1]	t_{pHL}, t_{pLH}		3.0	4.5	us	@ 5V_{DC} supply
			3.2	4.8	us	@ 3.3V_{DC} supply
Pulse Width Distortion	PWD	0	0.02	0.2	us	The max different time between t_{pHL} and t_{pLH}@ 5V_{DC} supply. And The value is | t_{pHL} - t_{pLH} |
		0	0.02	0.2	us	The max different time between t_{pHL} and t_{pLH}@ 3.3V_{DC} supply. And The value is | t_{pHL} - t_{pLH} |
Output Signal Rise/Fall Time[4]	t_r/t_f		1.5		ns	See Figure 9.
Common-Mode Transient Immunity[3]	CMTI	250			kV/μs	V_{IN} = V_{DDx}[2] or 0V, V_{CM} = 1000 V
ESD (HBM - Human body model)	ESD		±8		kV	

Notes:

[1] t_{pLH} = low-to-high propagation delay time, t_{pHL} = high-to-low propagation delay time. See Figure 10.

[2] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

[3] See Figure 16 for Common-mode transient immunity (CMTI) measurement.

[4] t_r means is the time from 10% amplitude to 90% amplitude of the rising edge of the signal, t_f means is the time from 90% amplitude to 10% amplitude of the falling edge of the signal.

Table 8.π13XU6x Switching Specifications

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Minimum Pulse Width	PW			6.5	us	Within pulse width distortion (PWD) limit
Maximum Data Rate		150			Kbps	Within pulse width distortion (PWD) limit
Propagation Delay Time[1]	t_{pHL}, t_{pLH}		2.5	4.5	us	@ 5V_{DC} supply
			2.7	4.8	us	@ 3.3V_{DC} supply
Pulse Width Distortion	PWD	0	0.02	0.2	us	The max different time between t_{pHL} and t_{pLH}@ 5V_{DC} supply. And The value is | t_{pHL} - t_{pLH} |
		0	0.02	0.2	us	The max different time between t_{pHL} and t_{pLH}@ 3.3V_{DC} supply. And The value is | t_{pHL} - t_{pLH} |
Output Signal Rise/Fall Time[4]	t_r/t_f		1.5		ns	See Figure 9.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Disable propagation delay, high-to-high impedance output[5]	t_{PHZ}		23	47	ns	@ $5V_{DC}$ supply
			28	58	ns	@ $3.3V_{DC}$ supply
Disable propagation delay, low-to-high impedance output	t_{PLZ}		23	47	ns	@ $5V_{DC}$ supply
			28	58	ns	@ $3.3V_{DC}$ supply
Enable propagation delay, high impedance-to-high output	t_{PZH}		13	27	ns	@ $5V_{DC}$ supply, for π13xU61
			17	35	ns	@ $3.3V_{DC}$ supply, for π13xU61
			3.5	12	us	@ $5V_{DC}$ supply, for π13xU60
			3.3	11	us	@ $3.3V_{DC}$ supply, for π13xU60
Enable propagation delay, high impedance-to-low output	t_{PZL}		3.5	12	us	@ $5V_{DC}$ supply, for π13xU61
			3.3	11	us	@ $3.3V_{DC}$ supply, for π13xU61
			13	27	ns	@ $5V_{DC}$ supply, for π13xU60
			17	35	ns	@ $3.3V_{DC}$ supply, for π13xU60
Common-Mode Transient Immunity[3]	CMTI	250			kV/μs	V_{IN} = V_{DDx}[2] or 0V, V_{CM} = 1000 V
ESD (HBM - Human body model)	ESD		±8		kV	

Notes:

[1] t_{pLH} = low-to-high propagation delay time, t_{pHL} = high-to-low propagation delay time. See Figure 10.

[2] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

[3] See Figure 16 for Common-mode transient immunity (CMTI) measurement.

[4] t_r means is the time from 10% amplitude to 90% amplitude of the rising edge of the signal, t_f means is the time from 90% amplitude to 10% amplitude of the falling edge of the signal.

[5] See Figure 11, Figure 12 for t_{PLZ}, t_{PZL} measurement, see Figure 13, Figure 14 for t_{PHZ}, t_{PZH} measurement.

Table 9.DC Specifications

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = $3.3V_{DC}$±10% or $5V_{DC}$±10%, T_A=25°C, unless otherwise noted.

	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Rising Input Signal Voltage Threshold	V_{IT+}		0.6*V_{DDx}[1]	0.7*V_{DDx}[1]	V	
Falling Input Signal Voltage Threshold	V_{IT-}	0.3* V_{DDx}[1]	0.4* V_{DDx}[1]		V	
High Level Output Voltage	V_{OH} [1]	V_{DDx} – 0.1	V_{DDx}		V	−20 μA output current
		V_{DDx} – 0.2	V_{DDx} – 0.1		V	−2 mA output current
Low Level Output Voltage	V_{OL}		0	0.1	V	20 μA output current
			0.1	0.2	V	2 mA output current
Input Current per Signal Channel	I_{IN}	−10	0.5	10	μA	0 V ≤ Signal voltage ≤ V_{DDx}[1]
V_{DDx}[1] Undervoltage Rising Threshold	V_{DDxUV+}	2.45	2.75	2.95	V	
V_{DDx}[1] Undervoltage Falling Threshold	V_{DDxUV-}	2.30	2.60	2.75	V	
V_{DDx}[1] Hysteresis	V_{DDxUVH}		0.15		V	

Notes:

[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

Table 10.Quiescent Supply Current

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = $3.3V_{DC}$±10% or $5V_{DC}$±10%, T_A=25°C, C_L = 0 pF, unless otherwise noted.

Part	Symbol	Min	Typ	Max	Unit	Test Conditions	
						Supply voltage	Input signal
π130U3x	$I_{DD1 (Q)}$	0.28	0.35	0.45	mA	$5V_{DC}$	VI=0V for π13xUx1
	$I_{DD2 (Q)}$	1.12	1.40	1.83	mA		VI=5V for π13xUx0
	$I_{DD1 (Q)}$	0.11	0.14	0.18	mA		VI=5V for π13xUx1
	$I_{DD2 (Q)}$	1.21	1.51	1.96	mA		VI=0V for π13xUx0
	$I_{DD1 (Q)}$	0.21	0.27	0.35	mA	$3.3V_{DC}$	VI=0V for π13xUx1
	$I_{DD2 (Q)}$	1.10	1.38	1.79	mA		VI=3.3V for π13xUx0
	$I_{DD1 (Q)}$	0.10	0.13	0.17	mA		VI=3.3V for π13xUx1

Part	Symbol	Min	Typ	Max	Unit	Test Conditions	
						Supply voltage	Input signal
	$I_{DD2\,(Q)}$	1.19	1.49	1.94	mA		VI=0V for π13xUx0
π131U3x	$I_{DD1\,(Q)}$	0.56	0.70	0.90	mA	$5V_{DC}$	VI=0V for π13xUx1
	$I_{DD2\,(Q)}$	0.85	1.06	1.38	mA		VI=5V for π13xUx0
	$I_{DD1\,(Q)}$	0.49	0.61	0.79	mA		VI=5V for π13xUx1
	$I_{DD2\,(Q)}$	0.85	1.07	1.39	mA		VI=0V for π13xUx0
	$I_{DD1\,(Q)}$	0.51	0.63	0.82	mA	$3.3V_{DC}$	VI=0V for π13xUx1
	$I_{DD2\,(Q)}$	0.81	1.01	1.32	mA		VI=3.3V for π13xUx0
	$I_{DD1\,(Q)}$	0.48	0.61	0.79	mA		VI=3.3V for π13xUx1
	$I_{DD2\,(Q)}$	0.84	1.05	1.37	mA		VI=0V for π13xUx0
π130U6x	$I_{DD1\,(Q)}$	0.28	0.47	0.59	mA	$5V_{DC}$	VI=0V for π13xUx1
	$I_{DD2\,(Q)}$	1.12	1.59	2.06	mA		VI=5V for π13xUx0
	$I_{DD1\,(Q)}$	0.10	0.13	0.16	mA		VI=5V for π13xUx1
	$I_{DD2\,(Q)}$	1.21	1.71	2.22	mA		VI=0V for π13xUx0
	$I_{DD1\,(Q)}$	0.21	0.30	0.40	mA	$3.3V_{DC}$	VI=0V for π13xUx1
	$I_{DD2\,(Q)}$	1.10	1.53	1.99	mA		VI=3.3V for π13xUx0
	$I_{DD1\,(Q)}$	0.09	0.11	0.14	mA		VI=3.3V for π13xUx1
	$I_{DD2\,(Q)}$	1.19	1.66	2.15	mA		VI=0V for π13xUx0
π131U6x	$I_{DD1\,(Q)}$	0.56	0.81	1.05	mA	$5V_{DC}$	VI=0V for π13xUx1
	$I_{DD2\,(Q)}$	0.85	1.14	1.47	mA		VI=5V for π13xUx0
	$I_{DD1\,(Q)}$	0.49	0.63	0.81	mA		VI=5V for π13xUx1
	$I_{DD2\,(Q)}$	0.85	1.11	1.44	mA		VI=0V for π13xUx0
	$I_{DD1\,(Q)}$	0.51	0.68	0.89	mA	$3.3V_{DC}$	VI=0V for π13xUx1
	$I_{DD2\,(Q)}$	0.81	1.05	1.36	mA		VI=3.3V for π13xUx0
	$I_{DD1\,(Q)}$	0.48	0.60	0.78	mA		VI=3.3V for π13xUx1
	$I_{DD2\,(Q)}$	0.84	1.08	1.40	mA		VI=0V for π13xUx0

Table 11.Total Supply Current vs. Data Throughput (CL = 0 pF)

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = $3.3V_{DC}$±10% or $5V_{DC}$±10%, T_A=25°C, C_L = 0 pF, unless otherwise noted.

Part	Symbol	2 Kbps			50Kbps			150Kbps			Unit	Supply voltage
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
π130U3x	I_{DD1}		0.24	0.36		0.24	0.36		0.25	0.38	mA	$5V_{DC}$
	I_{DD2}		1.45	2.18		1.47	2.21		1.49	2.24		
	I_{DD1}		0.18	0.27		0.18	0.27		0.18	0.27	mA	$3.3V_{DC}$
	I_{DD2}		1.41	2.12		1.42	2.13		1.43	2.15		
π131U3x	I_{DD1}		0.60	0.90		0.61	0.92		0.62	0.93	mA	$5V_{DC}$
	I_{DD2}		1.05	1.58		1.07	1.61		1.09	1.64		
	I_{DD1}		0.55	0.83		0.56	0.84		0.57	0.86	mA	$3.3V_{DC}$
	I_{DD2}		1.03	1.55		1.05	1.58		1.07	1.61		
π130U6x	I_{DD1}		0.28	0.42		0.28	0.42		0.29	0.43	mA	$5V_{DC}$
	I_{DD2}		1.58	2.37		1.58	2.37		1.60	2.39		
	I_{DD1}		0.19	0.29		0.20	0.29		0.20	0.30	mA	$3.3V_{DC}$
	I_{DD2}		1.53	2.30		1.54	2.31		1.55	2.32		
π131U6x	I_{DD1}		0.71	1.07		0.72	1.08		0.73	1.09	mA	$5V_{DC}$
	I_{DD2}		1.13	1.69		1.13	1.70		1.14	1.71		
	I_{DD1}		0.64	0.96		0.64	0.96		0.65	0.97	mA	$3.3V_{DC}$
	I_{DD2}		1.07	1.60		1.07	1.60		1.08	1.61		

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 12.Insulation Specifications

Parameter	Symbol	Value		Unit	Test Conditions/Comments
		π13xU3x	π13xU6x		
Rated Dielectric Insulation Voltage		3000	5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (CLR)	4	8	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (CRP)	4	8	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		11	21	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	>400	V	DIN EN 60112 (VDE 0303-11):2010-05
Material Group		II	II		IEC 60112:2003 + A1:2009

PACKAGE CHARACTERISTICS

Table 13.Package Characteristics

Parameter	Symbol	Typical Value		Unit	Test Conditions/Comments
		π13xU3x	π13xU6x		
Resistance (Input to Output)[1]	R_{IO}	10^{11}	10^{11}	Ω	
Capacitance (Input to Output)[1]	C_{IO}	1.5	1.5	pF	@1MHz
Input Capacitance[2]	C_I	3	3	pF	@1MHz
IC Junction to Ambient Thermal Resistance	θ_{JA}	100	45	°C/W	Thermocouple located at center of package underside

Notes:

[1]The device is considered a 2-terminal device; Short-circuit all terminals on the VDD1 side as one terminal, and short-circuit all terminals on the VDD2 side as the other terminal.

[2]Testing from the input signal pin to ground.

REGULATORY INFORMATION

See Table 14 for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Table 14.Regulatory

Regulatory	π13xU3x	π13xU6x
UL	Recognized under UL 1577 Component Recognition Program[1] Single Protection, 3000 V rms Isolation Voltage File (E494497)	Recognized under UL 1577 Component Recognition Program[1] Single Protection, 5000 V rms Isolation Voltage File (E494497)
VDE	DIN VDE V 0884-11:2017-01[2] Basic insulation, V_{IORM} = 565V peak, V_{IOSM} = 3615 V peak File (40053041)	DIN VDE V 0884-11:2017-01[2] Basic insulation, V_{IORM} = 1200 V peak, V_{IOSM} = 5000 V peak File (40052896)
CQC	Certified under CQC11-471543-2012 and GB4943.1-2011 Basic insulation at 500 V rms (707 V peak) working voltage Reinforced insulation at 250 V rms (353 V peak) NB SOIC-16 File (CQC20001260212) SSOP16 File (CQC20001260213)	Certified under CQC11-471543-2012 and GB4943.1-2011 Basic insulation at 845 V rms (1200 V peak) working voltage Reinforced insulation at 422 V rms (600 V peak) WB SOIC-16 File (CQC20001260258)

Notes:

[1] In accordance with UL 1577, each π130U3X/π131U3X is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 sec; each π130U6X/π131U6X is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec

[2] In accordance with DIN V VDE V 0884-11, each π130U3X/π131U3X is proof tested by applying an insulation test voltage ≥ 848 V peak for 1 sec (partial discharge detection limit = 5 pC); each π130U6X/π131U6X is proof tested by ≥ 1800V peak for 1 sec.

DIN V VDE V 0884-11 (VDE V 0884-11) INSULATION CHARACTERISTICS

Table 15.VDE Insulation Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic		Unit
			π13xU3x	π13xU6x	
Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms			 I to IV I to III I to III	 I to IV I to III I to III	
Climatic Classification			40/105/21	40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	2	
Maximum repetitive peak isolation voltage		V_{IORM}	565	1200	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	848	1800	V peak
Input to Output Test Voltage, Method A					
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.3 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	735	1560	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	678	1440	V peak
Highest Allowable Overvoltage		V_{IOTM}	4200	7071	V peak
Surge Isolation Voltage Basic	Basic insulation, 1.2/50 µs combination wave, VTEST = 1.3 × VIOSM (qualification)[1]	V_{IOSM}	3615	5000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see *Figure 5*)				
Maximum safety Temperature		T_S	150	150	°C
Maximum Power Dissipation at 25°C		P_S	1.67	2.78	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	$>10^9$	Ω

Notes:

[1]In accordance with DIN V VDE V 0884-11, π1xxx3x is proof tested by applying a surge isolation voltage 4700 V, π1xxx6x is proof tested by applying a surge isolation voltage 6500 V.

Typical Thermal Characteristic

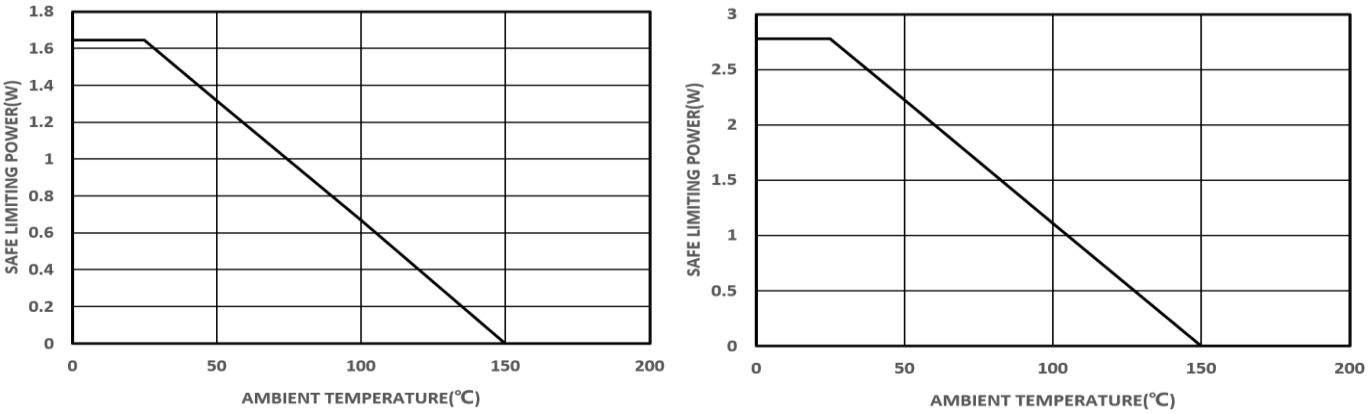


Figure 5.Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per VDE (left: π13xU3x; right: π13xU6x)

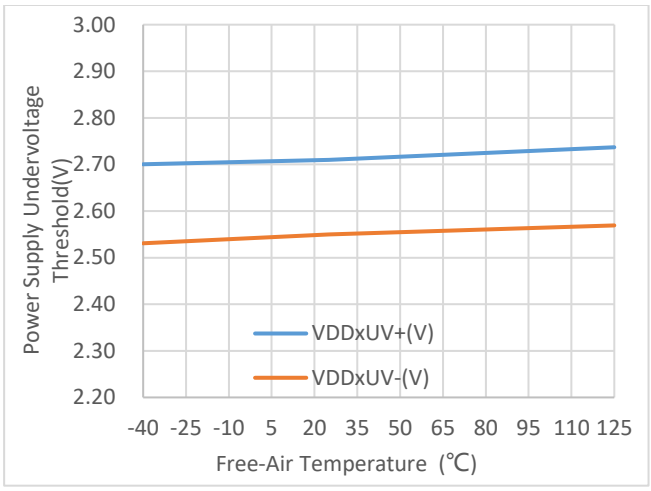


Figure 6.UVLO vs. Free-Air Temperature

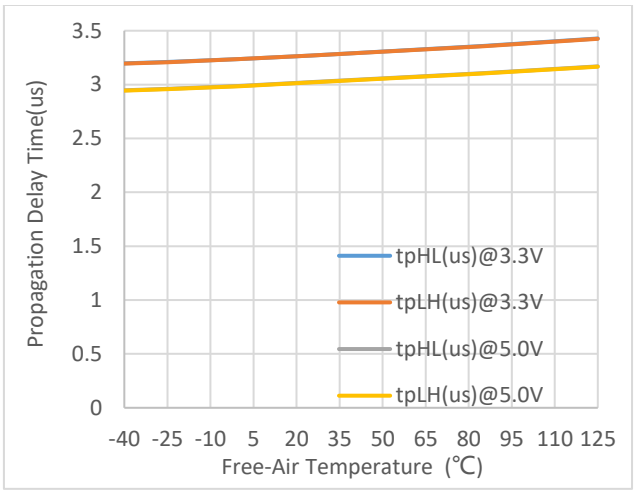


Figure 7.π13xU3x Propagation Delay Time vs. Free-Air Temperature

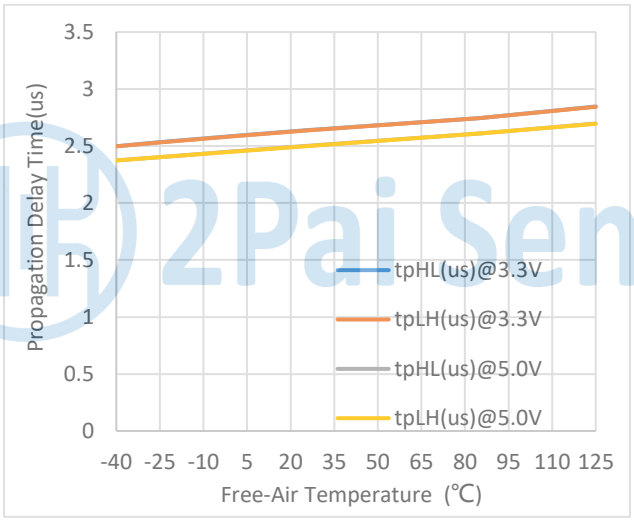


Figure 8.π13xU6x Propagation Delay Time vs. Free-Air Temperature

Timing test information

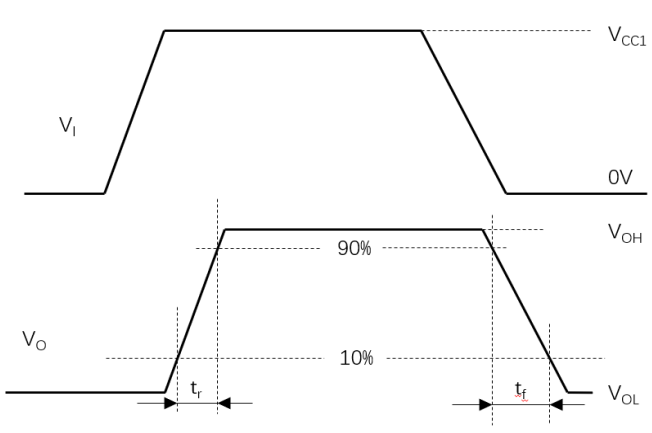


Figure 9.Transition time waveform measurement

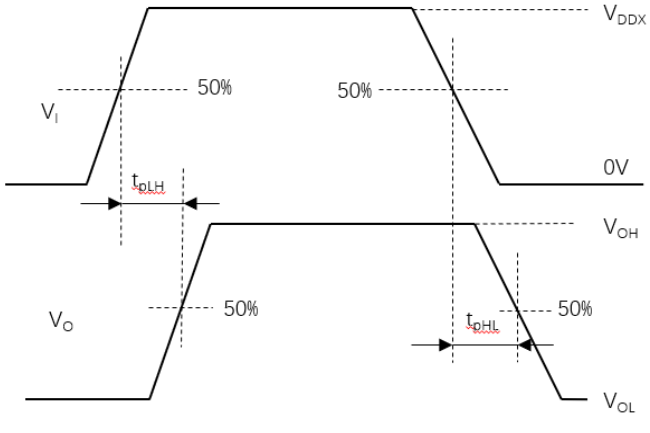


Figure 10.Propagation delay time waveform measurement

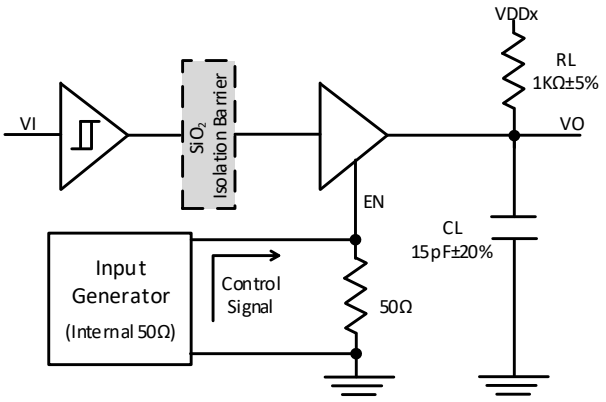


Figure 11.t_{PZL}/t_{PLZ} test circuit

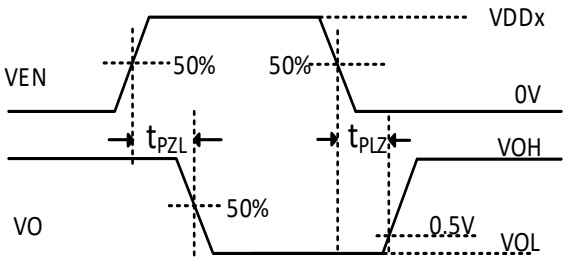


Figure 12. t_{PZL}/t_{PLZ} measurement waveform

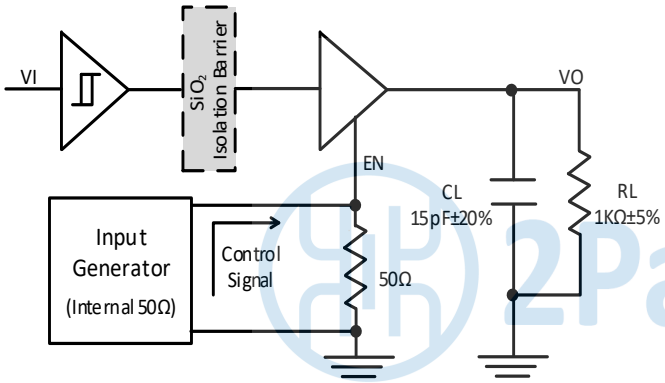


Figure 13. t_{PZH}/t_{PHZ} test circuit

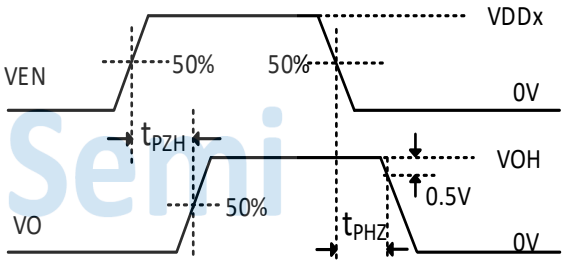


Figure 14. t_{PZH}/t_{PHZ} measurement waveform

APPLICATIONS INFORMATION

OVERVIEW

The π1xxxxx are 2PaiSemi digital isolators product family based on 2PaiSemi unique ***iDivider®*** technology. Intelligent voltage **Divider** technology (***iDivider®*** technology) is a new generation digital isolator technology invented by 2PaiSemi. It uses the principle of capacitor voltage divider to transmit signal directly cross the isolator capacitor without signal modulation and demodulation. Compare to the traditional Opto-couple technology, icoupler technology, OOK technology, ***iDivider®*** is a more essential and concise isolation signal transmit technology which leads to greatly simplification on circuit design and therefore significantly improves device performance, such as lower power consumption, faster speed, enhanced anti-interference ability, lower noise.

By using maturated standard semiconductor CMOS technology and the innovative ***iDivider®*** design, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators. The π1xxxxx isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 1.5 kV rms to 5.0 kV rms and the data rate from DC up to 600Mbps (see the Ordering Guide).

The π130Uxx/π131Uxx are the outstanding 150Kbps Triple-channel digital isolators with the enhanced ESD capability. the devices transmit data across an isolation barrier by layers of silicon dioxide isolation.

The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, offering voltage translation of 3.3 V, and 5 V logic. The π130Uxx/π131Uxx have very low propagation delay and high speed. The input/output design techniques allow logic and supply voltages over a wide range from 3.0 V to 5.5 V, offering voltage translation of 3.3 V and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference.

See the Ordering Guide for the model numbers that have the fail-safe output state of low or high.

PCB LAYOUT

The low-ESR ceramic bypass capacitors must be connected between V_{DD1} and GND_1 and between V_{DD2} and GND_2. The bypass capacitors are placed on the PCB as close to the isolator device as possible. The recommended bypass capacitor value is between 0.1 µF and 10 µF. The user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy, or in order to enhance the anti ESD ability of the system.

Avoid reducing the isolation capability, Keep the space underneath the isolator device free from metal such as planes, pads, traces and vias.

To minimize the impedance of the signal return loop, keep the solid ground plane directly underneath the high-speed signal path, the closer the better. The return path will couple between the nearest ground plane to the signal path. Keep suitable trace width for controlled impedance transmission lines interconnect.

To reduce the rise time degradation, keep the length of input/output signal traces as short as possible, and route low inductance loop for the signal path and It's return path.

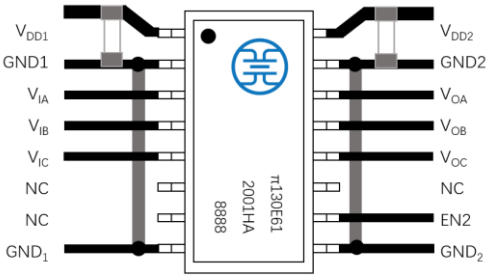


Figure 15.Recommended Printed Circuit Board Layout

CMTI MEASUREMENT

To measure the Common-Mode Transient Immunity (CMTI) of π1xxxxx isolator under specified common-mode pulse magnitude (VCM) and specified slew rate of the common-mode pulse (dVCM/dt) and other specified test or ambient conditions, The common-mode pulse generator (G1) will be capable of providing fast rise and fall pulses of specified magnitude and duration of the common-mode pulse (VCM),such that the maximum common-mode slew rates (dVCM/dt) can be applied to π1xxxxx isolator coupler under measurement. The common-mode pulse is applied between one side ground GND1 and the other side ground GND2 of π1xxxxx isolator, and shall be capable of providing positive transients as well as negative transients.

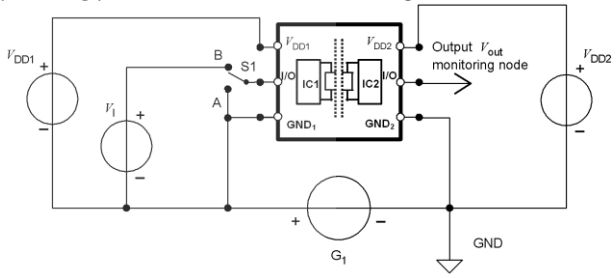


Figure 16.Common-mode transient immunity (CMTI) measurement

OUTLINE DIMENSIONS

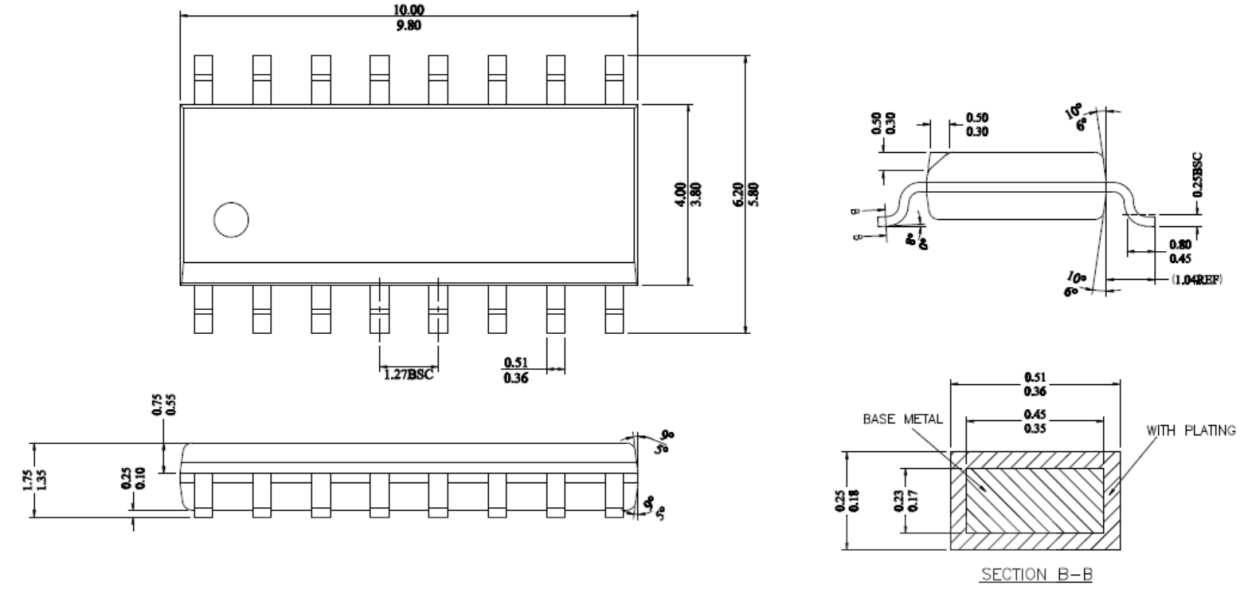


Figure 17. 16-Lead Narrow Body SOIC [NB SOIC-16] Outline Package

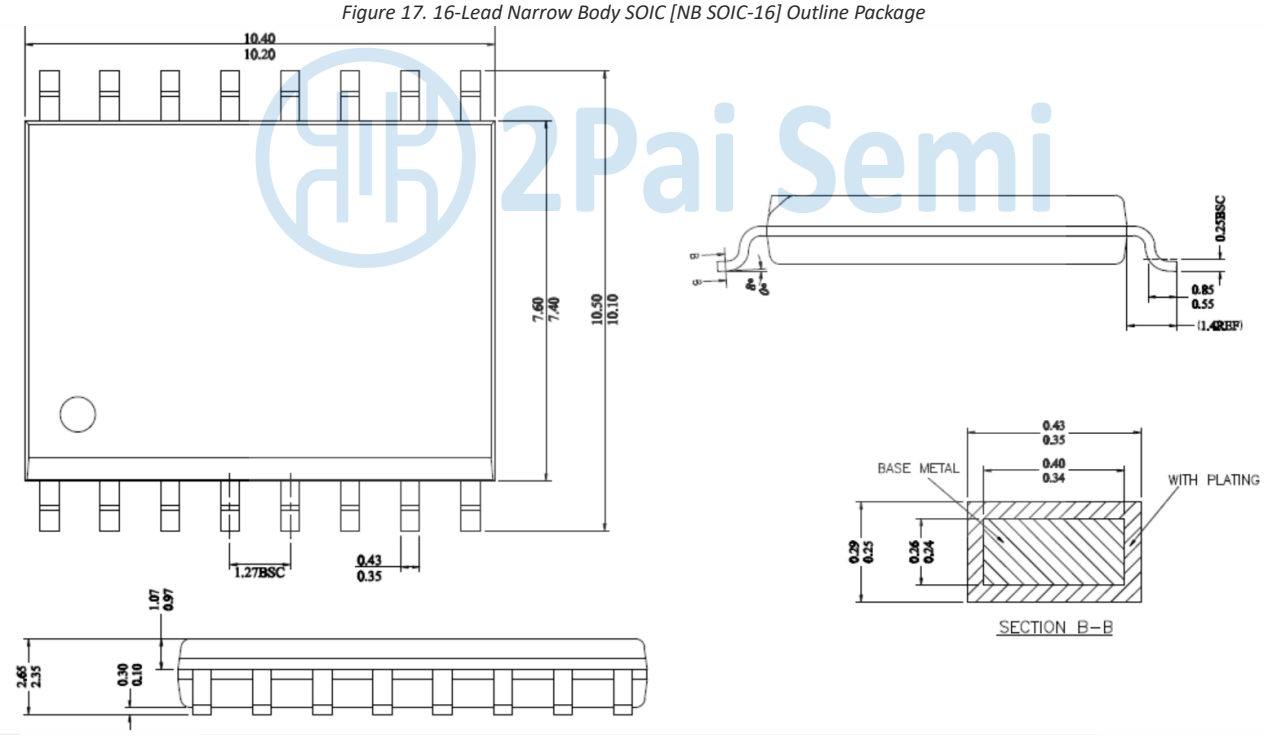
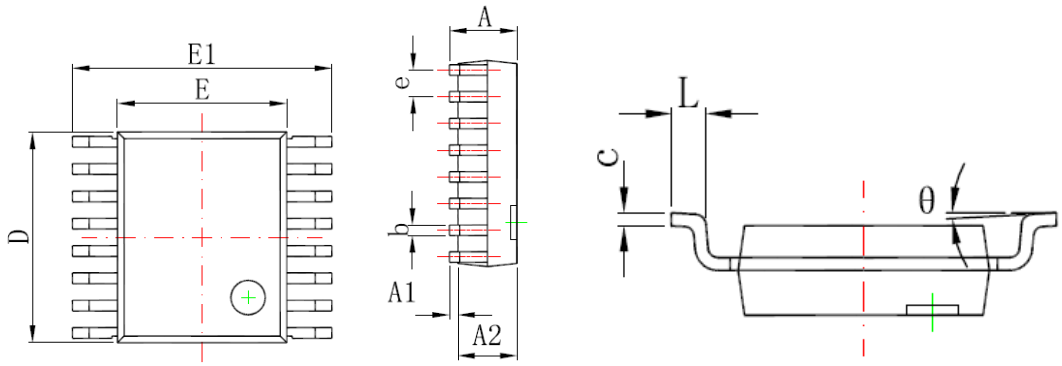


Figure 18.16-Lead Wide Body Outline Package [WB SOIC-16]



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.200	0.300	0.008	0.012
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	0.635(BSC)		0.025(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Figure 19.16-Lead SSOP Outline Package [SSOP16]

Land Patterns

16-Lead Narrow Body SOIC [NB SOIC-16]

The figure below illustrates the recommended land pattern details for the π1xxxxx in a 16-pin narrow-body SOIC. The table below lists the values for the dimensions shown in the illustration.

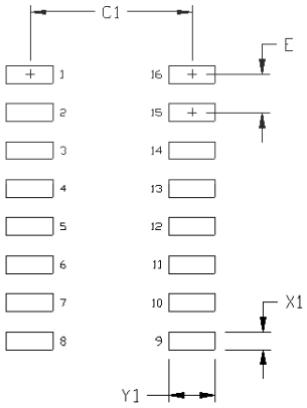


Figure 20.16-Lead Narrow Body SOIC [NB SOIC-16] Land Pattern

Table 16.16-Lead Narrow Body SOIC [NB SOIC-16] Land Pattern Dimensions

Dimension	Feature	Parameter	Unit
C1	Pad column spacing	5.40	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	1.55	mm

Note:

1.This land pattern design is based on IPC -7351

2.All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

16-Lead Wide Body SOIC [WB SOIC-16]

The figure below illustrates the recommended land pattern details for the π1xxxxx in a 16-pin wide-body SOIC package. The table lists the values for the dimensions shown in the illustration.

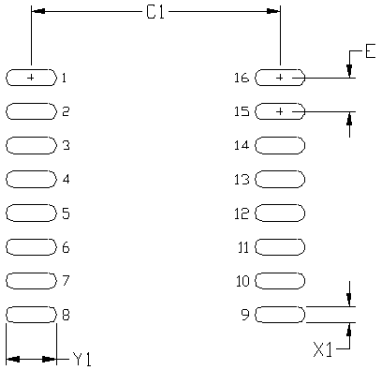


Figure 21. 16-Lead Wide Body SOIC [WB SOIC-16] Land Pattern

Table 17. 16-Lead Wide Body SOIC [WB SOIC-16] Land Pattern Dimensions

Dimension	Feature	Parameter	Unit
C1	Pad column spacing	9.40	mm
E	Pad row pitch	1.27	mm
X1	Pad width	0.60	mm
Y1	Pad length	1.90	mm

Note:

1.This land pattern design is based on IPC -7351

2.All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

16-Lead SSOP

The figure below illustrates the recommended land pattern details for the π1xxxxx in a *16-Lead SSOP* package. The table lists the values for the dimensions shown in the illustration.

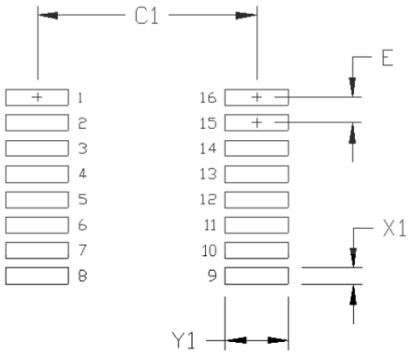


Figure 22. 16-Lead SSOP Land Pattern

Table 18. 16-Lead SSOP Land Pattern Dimensions

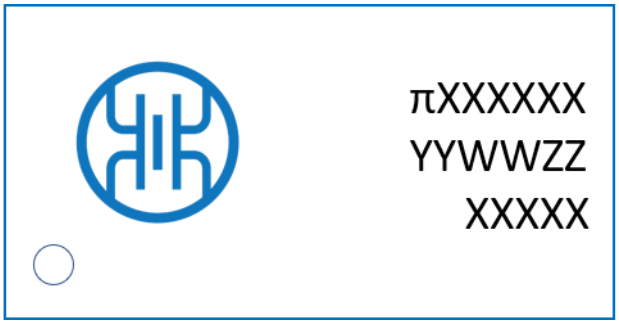
Dimension	Feature	Parameter	Unit
C1	Pad column spacing	5.40	mm
E	Pad row pitch	0.635	mm
X1	Pad width	0.40	mm
Y1	Pad length	1.55	mm

Note:

1.This land pattern design is based on IPC -7351

2.All feature sizes shown are at maximum material condition and a card fabrication tolerance of 0.05 mm is assumed.

Top Marking

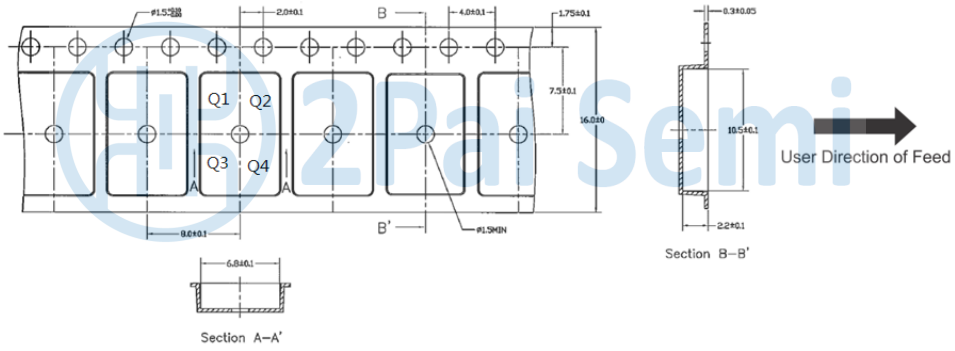


Line 1	πXXXXXX=Product name
Line 2	YY = Work Year WW = Work Week ZZ=Manufacturing code from assembly house
Line 3	XXXXX, no special meaning

Figure 23. Top Marking

REEL INFORMATION

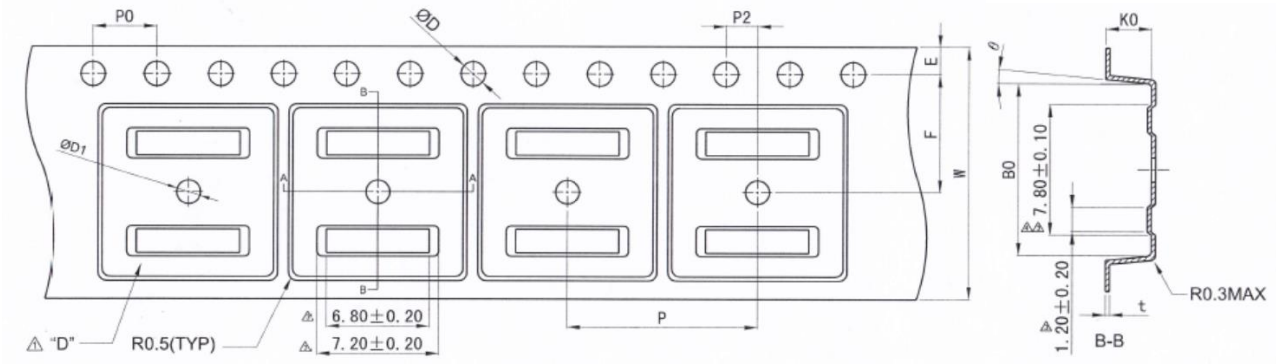
16-Lead Narrow Body SOIC [NB SOIC-16]

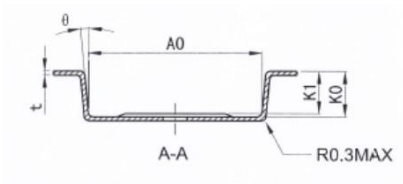


Note： The Pin 1 of the chip is in the quadrant Q1

Figure 24. 16-Lead Narrow Body SOIC [NB SOIC-16] Reel Information

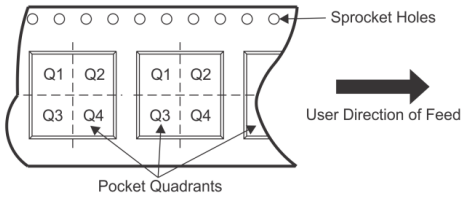
16-Lead Wide Body SOIC [WB SOIC-16]





Items	Size(mm)
E	1.75±0.10
F	7.50±0.05
P2	2.00±0.05
D	1.55±0.05
D1	1.5±0.10
P0	4.00±0.10
10P0	40.00±0.20

Items	Size(mm)
W	16.00±0.30
P	12.00±0.10
A0	10.90±0.10
B0	10.80±0.10
K0	3.00±0.10
t	0.30±0.05
K1	2.70±0.10
θ	5° TYP



Note：The Pin 1of the chip is in the quadrant Q1

Figure 25. 16-Lead Wide Body SOIC [WB SOIC-16] Reel Information

16-Lead SSOP

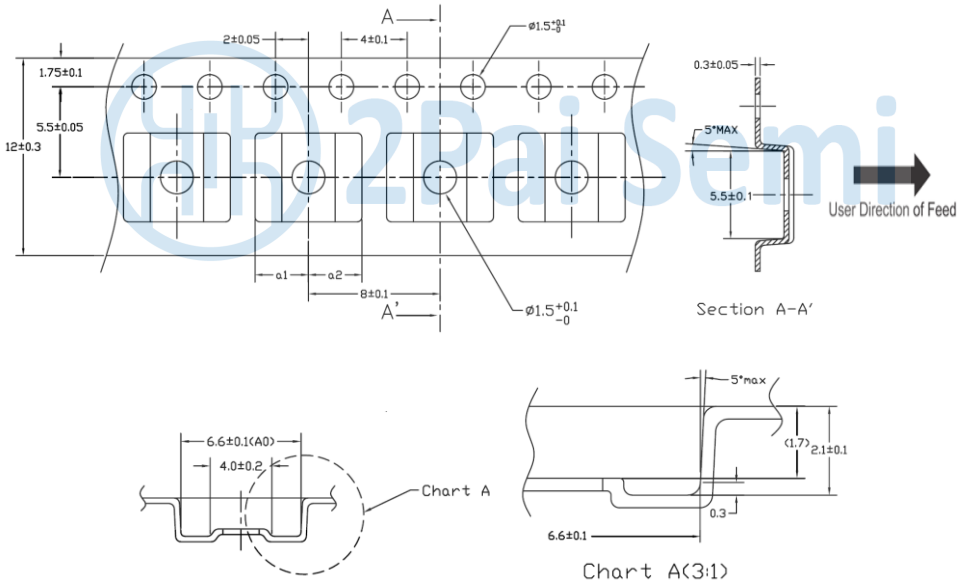


Figure 26. 16-Lead SSOP Reel Information

ORDERING GUIDE

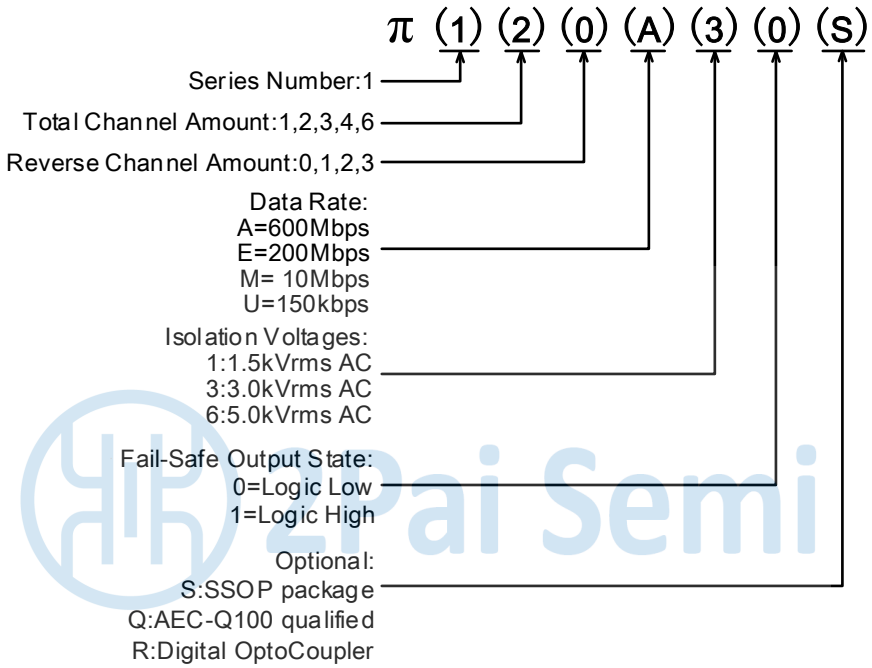
Table 19. Ordering Guide

Model Name [1]	Temperature Range	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Isolation Rating (kV rms)	Fail-Safe Output State	Package	MSL Peak Temp [2]	MOQ/ Quantity per reel[3]
π130U31	−40~125°C	3	0	3	High	NB SOIC-16	Level-2-260C-1 YEAR	2500
π130U30	−40~125°C	3	0	3	Low	NB SOIC-16	Level-2-260C-1 YEAR	2500
π131U31	−40~125°C	2	1	3	High	NB SOIC-16	Level-2-260C-1 YEAR	2500
π131U30	−40~125°C	2	1	3	Low	NB SOIC-16	Level-2-260C-1 YEAR	2500
π130U61	−40~125°C	3	0	5	High	WB SOIC-16	Level-2-260C-1 YEAR	1500
π130U60	−40~125°C	3	0	5	Low	WB SOIC-16	Level-2-260C-1 YEAR	1500
π131U61	−40~125°C	2	1	5	High	WB SOIC-16	Level-2-260C-1 YEAR	1500
π131U60	−40~125°C	2	1	5	Low	WB SOIC-16	Level-2-260C-1 YEAR	1500
π130U31S	−40~125°C	3	0	3	High	16-Lead SSOP	Level-3-260C-168 HR	4000
π130U30S	−40~125°C	3	0	3	Low	16-Lead SSOP	Level-3-260C-168 HR	4000

Model Name [1]	Temperature Range	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Isolation Rating (kV rms)	Fail-Safe Output State	Package	MSL Peak Temp [2]	MOQ/ Quantity per reel[3]
π131U31S	−40~125°C	2	1	3	High	16-Lead SSOP	Level-3-260C-168 HR	4000
π131U30S	−40~125°C	2	1	3	Low	16-Lead SSOP	Level-3-260C-168 HR	4000

[1] Pai1xxxxx is equals to π1xxxxx in the customer BOM.
[2] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
[3] MOQ, minimum ordering quantity.

PART NUMBER NAMED RULE



Notes:
Pai1xxxxx is equals to π1xxxxx in the customer BOM

Figure 27. Part Number Named Rule

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Room 307-309, No.22, Boxia Road, Pudong New District, Shanghai, 201203, China 021-50850681

http://www.rpsemi.com/

REVISION HISTORY

Revision	Date	Page	Change Record
1.0	2018/09/17	All	Initial version
1.1	2018/11/28	P11	Changed the recommended bypass capacitor value.
1.2	2019/09/08	Page1	Changed the contact address. Add *iDivider* technology description in General Description. Changed propagation delay time, CMTI and HBM ESD. Added WB SOIC-16 Lead information.
1.3	2019/12/20	Page1,11,14	Changed description of π1xxx6x.
1.4	2020/02/16	Page1	Changed propagation delay time.
1.5	2020/02/25	Page5	Changed Pulse Width Distortion.
1.6	2020/03/16	Page6	Changed VDDx Undervoltage Threshold and Regulatory Information. Added information of Land Patterns and Top Marking
1.7	2020/04/16	Page12	Optimize description and format to make it consistent with the Chinese version.
1.8	2021/05/17	Page 1,5~10	Changed Regulatory Information. Added propagation delay time and supply current of π1xxU6x.
1.9	2021/12/06	Page5,10,15, 16,17	Added Enable and Disable propagation delay time. Changed Top Marking Information. Changed MSL Peak Temp.