Analog Circuit Implementation of Fractional-Order Memristor: Arbitrary-Order Lattice Scaling Fracmemristor

Yi-Fei Pu, Xiao Yuan, and Bo Yu

***Abstract*— In this paper, based on fractional calculus, the fractional-order memristor, an arbitrary-order fracmemristor, is proposed to be implemented in the form of a lattice scaling analog circuit. Since the concept of the memristor is generalized from the classic integer-order memristor to that of the fractional-order memristor, fracmemristor, it is natural to ponder a challenging theoretical problem to propose a circuit theoretic methodology to achieve an arbitrary-order memristor by using the ordinary memristor and capacitor or inductor in the form of an analog circuit. Motivated by this need, in this paper, we propose an interesting analog circuit implementation method of an arbitrary-order memristor. The first step is the proposal for a novel feasible analog circuit implementation of an arbitrary-order lattice scaling fracmemristor. In particular, the hardware achievement of this arbitrary-order lattice scaling fracmemristor is mathematically derived and analyzed in detail. Second, the approximation performance, electrical characteristics, especially fingerprints, and analog circuit achievement of an arbitrary-order fracmemristor are experimentally analyzed in detail, respectively. The main contribution of this paper is the first proposal for the preliminary attempt of a feasible hardware achievement of an arbitrary-order fracmemristor and for the recognition of the fingerprints of fracmemristor.**

***Index Terms*— Fractional calculus, fractional-order memristor, three-port mirror memristor, fingerprints of fracmemristor, fracmemristance.**

I. Introduction

THE memristor was originally envisioned [1] and was generalized to memristive systems [2] by circuit theorist Chua as a missing nonlinear passive two-terminal electrical component [3], which has non-volatility property [4]–[10]. A broader definition of the memristor was argued that it could cover all forms of two-terminal non-volatile memory devices based on resistance switching effects [4]–[8], [11]. A solely current-controlled memristor with the so-called non-volatility property [5]–[8] cannot enable such a memristor system to erratically change its state just under the influence of white current noise [12], [13], whose dynamic state equations allow the violation of Landauer's principle of the minimum amount of energy [12], [14]. The pinched hysteresis effect of the memristors and memristive systems [15], [16], the nonlinear ionic drift models of the memristors [17] and Strukov's initial memristor modeling equations [18] were further studied, respectively. Moreover, the memristors can be generally classified into five categories: the titanium dioxide memristor [9], [10], [19], [20], the polymeric memristor [21], [22], the layered memristor [23], the ferroelectric memristor [24] and the spin memristive systems [25]–[30], respectively. The electrical properties of the aforementioned memristors and memristive systems are of the classic integer-order.

Fractional calculus has become an important novel branch of mathematical analyses [31], [32]. For physical scientists and engineering technicians, fractional calculus is now a novel useful mathematical method mainly because of its inherent strength of long-term memory, non-locality and weak singularity. Many scientific fields such as the fractional diffusion processes [33], [34], fractional viscoelasticity [35], fractal dynamics [36], fractional control [37], fractional image processing [38], fractional signal processing [39], fractional neural networks [40], [41], fractional circuits and systems [42]–[45], etc., presently use fractional calculus and has obtained some promising results. However, the application of fractional calculus to analyzing the memristor is an emerging discipline of study in which few studies have been performed [46]–[55]. From the Chua's axiomatic element system [1]–[6] and according to constitutive relation, logical consistency, axiomatic completeness and formal symmetry, we can assume that there should be a capacitive fractional-order memristor and an inductive fractional-order memristor corresponding to the capacitive fractor and inductive fractor, respectively. The concept of the memristor was generalized preliminarily from the classic integer-order memristor to that of the fractional-order one [46]–[55]. In particular, Pu [55] firstly derived the generic fractional-order driving-point impedance functions of an arbitrary-order capacitive fracmemristor and inductive one in their natural implementations, respectively. There are two types of the fractional-order memristor: the capacitive fractional-order memristor and the inductive fractional-order memristor [55]. The terms "fracmemristor" and "fracmemristance" are two portmanteaus of "the fractional-order memristor" and "the fractional-order memristance," respectively [55]. The dynamic characteristics of the frammeristor based chaotic systems depend on not only its circuit parameters but also its initial state as well as its fractional-order. The frammeristor based chaotic behavior is a promising scope of study.

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Y.-F. Pu is with the College of Computer Science, Sichuan University, Chengdu 610065, China (e-mail: puyifei@scu.edu.cn; puyifei_007@163.com).

X. Yuan is with the College of Electronics and Information Engineering, Sichuan University, Chengdu 610065, China (e-mail: 653381180@qq.com).

B. Yu is with the College of Physics and Engineering, Chengdu Normal University, Chengdu 611130, China (e-mail: analogyb@foxmail.com).

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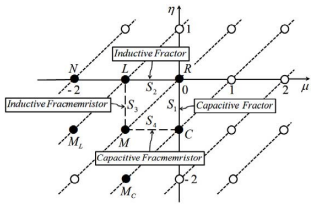


Fig. 1. Chua's periodic table of all two-terminal circuit elements.

Therefore, based on the aforementioned previous researches of the fractional-order memristor [46]–[55], it is natural to ponder a challenging theoretical problem to propose a circuit theoretic methodology to implement a fractional-order memristor by using the ordinary memristor and capacitor or inductor in the form of an analog circuit. Motivated by this need, in this paper, we used fractional calculus to propose an interesting analog circuit implementation method of an arbitrary-order memristor. Pu [55] only derived the generic fractional-order driving-point impedance functions of an arbitrary-order capacitive fracmemristor and inductive one in their natural implementations, respectively. Comparing to the previous work of fracmemristor [46]–[55], the main contribution of this paper is the first proposal for the preliminary attempt of a feasible hardware achievement of an arbitrary-order fracmemristor and for the recognition of the fingerprints of fracmemristor. The major advantage of the proposed lattice scaling approach is that we can use ordinary memristor and capacitor or inductor to easily achieve an arbitrary-order fracmemristor.

The remainder of this paper is organized as follows: Section 2 recalls some preliminary concepts of the fractor and the fracmemristor. In Section 3, at first, the circuit configurations of an arbitrary-order capacitive lattice scaling fracmemristor is proposed and mathematically derived. The second step is the proposal for an arbitrary-order compensatory capacitive lattice scaling fracmemristor. In Section 4, the approximation performance, electrical characteristics and analog circuit achievement of an arbitrary-order fracmemristor are experimentally analyzed in detail, respectively. In Section 5, the conclusions of this manuscript are presented.

II. Related Work

This section presents a brief introduction to the necessary electrical background of the fractor and the fracmemristor.

The memristor, M, completes the set of relations with [1]:

$$\varphi[q(t)] = M[q(t)]q(t), \tag{1}$$

where φ, q and t denote the magnetic flux, quantity of electric charge and time variable, respectively. The slope of this function is called the memristance being similar to variable resistance [1], given as:

$$\begin{aligned} V_i(t) &= d\varphi(q)/dq\, I_i(t) = [M(q) + qdM(q)/dq]\, I_i(t) \\ &= R\,[q(t)]\, I_i(t) = H\,[q(t)] * I_i(t), \end{aligned} \tag{2}$$

where $V_i(t)$ and $I_i(t)$ denote the instantaneous value of the input voltage and input current of a memristor, respectively. The symbol $*$ denotes convolution, $R\,[q(t)] = [M(q) + qdM(q)/dq]$ and $H\,[q(t)]$ denote the memristance and transmission function of a memristor, respectively. Note that in the time-invariant case, the constitutive relation of a memristor can be simply expressed as a set of points in the $\varphi - q$ plane. We can regard this relationship as a generalized Ohm's law [3]. Moreover, Chua's periodic table of all two-terminal circuit elements [4]–[8] can be shown as given in Fig. 1.

In Fig. 1, μ and η denote the voltage exponent and current exponent, which are equal to the order of the time derivative of $V_i(t)$ and $I_i(t)$, respectively. (μ, η) is referred to the Chua's plane of the Chua's axiomatic element system. C, R, L, M, M_L and M_C denote the capacitor, resistor, inductor, memristor, meminductor and memcapacitor, respectively. O denotes the other postulated elements of the Chua's axiomatic element system. Note that at first, small-signal behavior method is an efficient approach to study a resistive nonlinear network [56]–[58]. To give some physical meaning to each Chua's axiomatic element in Fig. 1 (including memristor), it is convenient to examine its small-signal behavior about an operating point Q on its associated $V_i^{(\mu)} - I_i^{(\eta)}$ curve. Assuming that a Chua's axiomatic element is characterized by $V_i^{(\mu)} = f\left(I_i^{(\eta)}\right)$ and its small-signal behavior about Q by described $V_i^{(\mu)}(t) = m_Q I_i^{(\eta)}(t)$, where m_Q denotes the slope $f'\left[I_i^{(\eta)}\right]$ at Q. Therefore, the small-signal reactance of this Chua's axiomatic element can be defined by taking Laplace transform of $\delta V_i^{(\mu)}(t) = m_Q \delta I_i^{(\eta)}(t)$. Thus, we obtain $L\{V_i(t)\} = Z(s)\, L\{I_i(t)\}$, where $Z(s) = s^{\eta-\mu} m_Q$, $L\{\}$ denotes Laplace transform and s denotes a complex variable of the Laplace transform. We can interpret the small-signal reactance $Z(s) = s^{\eta-\mu} m_Q$ as the impedance of an associated linearized element about Q [2]–[4]. For instance, based on certain algebraic properties of the Laplace operator, nonlinear n-port decomposition is achieved [59]. Finite-time synchronization of fractional-order memristor-based neural networks with time delays was considered by using Laplace transform, such as the generalized Gronwall inequality and Mittag-Leffler functions [60]. Secondly, (2) shows that in the case of small-signal behavior about Q, the Laplace transform of $V_i(t) = R\,[q(t)]\, I_i(t)$ is equal to $V_i(s) = 1/2\pi L\{R\,[q(t)]\} * I_i(s)$, which implements a convolution in Laplace transform domain and is sometimes too difficult to be calculated. For the convenience of analysis, let's assume that the transmission function of a memristor, $H\,[q(t)]$, satisfies $V_i(t) = R\,[q(t)]\, I_i(t) = H\,[q(t)] * I_i(t)$ (i.e.$R\,[q(t)] = \{H\,[q(t)] * I_i(t)\}/I_i(t)$). Thus, the Laplace transform of $V_i(t) = H\,[q(t)] * I_i(t)$, $V_i(s) = r[q(s)] I_i(s)$, implements a multiplication in Laplace transform domain, where $r[q(s)] = L\{H\,[q(t)]\}$ is the reactance of this memristor. In addition, Fig. 1 shows that at first, the capacitive fracmemristor is lying on the line segment, S_4, between C and M. The electrical properties of the capacitive fracmemristor fall in between those of the capacitor and those of the memristor [55]. Secondly, the inductive fracmemristor is lying on the line segment, S_3, between L and M. The electrical properties of the inductive fracmemristor fall in between those of the inductor and those of the memristor [55]. Furthermore, Pu derived the generic fractional-order driving-point impedance functions of an arbitrary-order capacitive fractor [44], [45], inductive fractor [44], [45], capacitive fracmemristor [55] and inductive fracmemristor [55] in their natural implementations, respectively, given as:

$$F_{-\upsilon}^{c} = F_{-(\eta+p)}^{c} = V_i(s)/I_i(s) = c^{-\upsilon} r^{1-p} s^{-\upsilon}, \tag{3}$$

$$F_{\upsilon}^{l} = F_{\eta+p}^{l} = V_i(s)/I_i(s) = l^{\upsilon} r^{1-p} s^{\upsilon}, \tag{4}$$

$$FM_{-\upsilon}^{c} = FM_{-(\eta+p)}^{c} = V_i(s)/I_i(s) = c^{-\upsilon} \{r[q(s)]\}^{1-p} s^{-\upsilon}, \tag{5}$$

$$FM_{\upsilon}^{l} = FM_{\eta+p}^{l} = V_i(s)/I_i(s) = l^{\upsilon} \{r[q(s)]\}^{1-p} s^{\upsilon}, \tag{6}$$

where $\upsilon = \eta + p$ is a non-negative real number, η is a non-negative integer and $0 \le p \le 1$. Note that at first, if $\upsilon = 0$, then $\eta = 0$ and $p = 0$. Equations (3)-(6) identically degenerate to the driving-point impedance function of R in Fig. 1. Secondly, if υ is a positive integer, then $\eta = \upsilon - 1$ and $p = 1$. Equations (3)-(6) degenerate to the driving-point impedance functions of C, L, C and L in Fig. 1, respectively. Thirdly, if $0 < \upsilon < 1$, then $\eta = 0$ and $0 < p < 1$. Equations (3)-(6) denote the $0 < \upsilon < 1$ order driving-point impedance functions of the capacitive fractor, inductive fractor, capacitive fracmemristor and inductive fracmemristor in Fig. 1, respectively. Fourthly, if $\upsilon > 1$ is a positive fraction, then $\eta = [\upsilon]$ and $0 < p < 1$, where [] denotes rounding operation. Equations (3)-(6) denote the corresponding $\upsilon > 1$ order driving-point impedance functions. $F^c_{-\upsilon}$, F^l_{υ}, $FM^c_{-\upsilon}$ and FM^l_{υ} denote the fractional-order driving-point impedance function of a purely ideal υ-order capacitive fractor, inductive fractor, capacitive fracmemristor and inductive fracmemristor, respectively. c, l and r denote the capacitance, inductance and resistance, respectively. $c^{\upsilon} r^{1-p}$, $l^{\upsilon} r^{1-p}$, $c^{\upsilon} L^{-1}\left\{[r(q)]^{1-p}\right\}$ and $l^{\upsilon} L^{-1}\left\{[r(q)]^{1-p}\right\}$ denote the capacitive fractance, inductive fractance, capacitive fracmemristance, inductive fracmemristance, respectively, where $L^{-1}\{\}$ denotes inverse Laplace transform. For instance, with regard to a nonlinear time dependent current-controlled memristor, let's assume that $I_i(t) = \sin(at)\,u(t)$ in (2), where a is frequency and $u(t)$ is a Heaviside function. Then, $I_i(s) = a/\left(s^2 + a^2\right)$ and $q(t) = D_t^{-1} I_i(t) = -(1/a)\cos(at)\,u(t)$. And supposing that $M[q(t)] = q(t)/2 + 1/a$. Thus, $R[q(t)] = [-(1/a)\cos(at) + 1/a]\,u(t)$ and $V_i(t) = [-\sin(2at)/(2a) + \sin(at)/a]\,u(t)$. And assuming the initial state of this memristor is zero, thus $V_i(s) = r[q(s)]I_i(s) = 3a^2/\left[\left(s^2 + 4a^2\right)\left(s^2 + a^2\right)\right]$. Then, we have $r[q(s)] = V_i(s)/I_i(s) = 3a/\left(s^2 + 4a^2\right)$. Therefore, $H[q(t)] = L^{-1}\{r[q(s)]\} = (3/2)\sin(2at)\,u(t)$, where $L^{-1}\{\}$ denotes inverse Laplace transform. Let's assume that $\upsilon = \eta + 2/3$, thus η is a positive integer and $p = 2/3$. Then, in (5) and (6), $L^{-1}\left\{[r(q)]^{1-p}\right\} = L^{-1}\left\{[r(q)]^{1/3}\right\} = (3a)^{1/3}\sqrt{\pi}/\Gamma(1/3)\,[t/(4a)]^{-1/6} J_{-1/6}(2at)u(t)$, where $J_{-1/6}(t)$ is a Bessel function of the first kind extended to non-integer orders by one of Schläfli's integrals. From aforementioned discussion, in the case of small-signal behavior about Q, we can approximately apply Laplace transform to analyze a circuit consisted of the memristor [2]–[4]. The generic fractional-order driving-point impedance functions of an arbitrary-order capacitive fracmemristor and inductive one in their natural implementations can be described as (5) and (6), respectively [55]. The measurement units and physical dimensions of the fracmemristance are the same as those of the fractance [44], [45], [55].

III. Analog Circuit Implementation of Arbitrary-Order Lattice Scaling Fracmemristor

This section is the proposal for a novel feasible analog circuit implementation of an arbitrary-order lattice scaling fracmemristor.

According to the characteristics of fractional calculus and Laplace transform, provided the transmission function of the memristor $H[q(t)]$ is a causal function and its fractional primitives are zero, we can simplify the inverse Laplace transforms of (5) and (6), given as:

$$V_i(t) = c^{-\upsilon} L^{-1}\left\{[r(q)]^{1-p}\right\} * [D_t^{-\upsilon} I_i(t)], \tag{7}$$

$$V_i(t) = l^{\upsilon} L^{-1}\left\{[r(q)]^{1-p}\right\} * [D_t^{\upsilon} I_i(t)], \tag{8}$$

where $D_t^{-\upsilon}$ denotes the υ-order integral with respect to t, and D_t^{υ} denotes the υ-order differential with respect to t. Equations (7) and (8) show that since the transmission function of a memristor $H[q(t)]$ can be arbitrary [1]–[8], $r[q(s)]$ is correspondingly arbitrary. Thus, in (5)-(8), the approximate implementation of $\{r[q(s)]\}^{1-p}$ and $L^{-1}\left\{[r(q)]^{1-p}\right\}$ are very difficult. The hardware achievement method of an arbitrary-order fracmemristor cannot directly employ that of an arbitrary-order fractor [42]–[45]. For conciseness, in this paper, we only discuss a novel feasible analog circuit implementation of an arbitrary-order capacitive lattice scaling fracmemristor in detail. An arbitrary-order inductive lattice scaling fracmemristor can be achieved in a similar way.

The circuit configurations of a υ-order capacitive lattice scaling fracmemristor can be shown in Fig. 2.

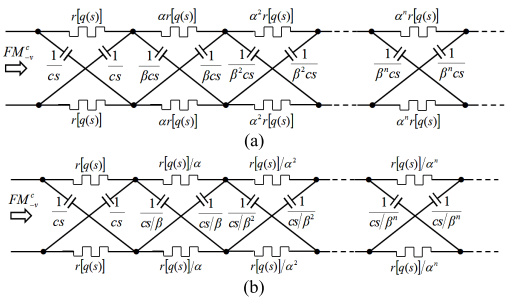


Fig. 2. Circuit configurations of υ-order capacitive lattice scaling fracmemristor: (a) υ-order low-pass filtering capacitive lattice scaling fracmemristor; (b) υ-order high-pass filtering capacitive lattice scaling fracmemristor.

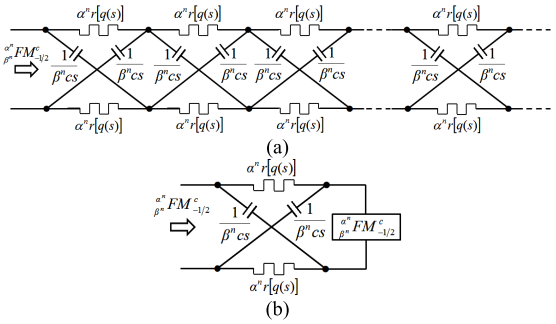


Fig. 3. Circuit configuration of a 1/2-order low-pass filtering capacitive lattice scaling fracmemristor: (a) Circuit configuration; (b) (f) Equivalent circuit.

In Fig. 2, $0 < \upsilon < 1$ is an arbitrary positive rational number, the symbol of ⎍⎍⎍ denotes the memristor, and α and β represent two positive scaling factors, respectively. Note that in physics, these so-called scaling factors are often referred to as two progressive ratios, and their product is then referred to scaling factor. The amount of memristors or capacitors the υ-order capacitive lattice scaling fracmemristor is equal to the double amount of layers. Figure 2 shows that the υ-order capacitive lattice scaling fracmemristor has a cascade circuit with a series connection of infinitely repeated lattice structures.

To simplify discussion, we use iterative solution method to analyze the fractional-order reactance of the υ-order low-pass filtering capacitive lattice scaling fracmemristor. The circuit configuration of a 1/2-order low-pass filtering capacitive lattice scaling fracmemristor can be shown in Fig. 3.

Figure 3 shows that the positive scaling factor of the reactance of a memristor and that of the capacitance of its

every series circuit, α^n and β^n, are identical, respectively. The every series circuit of the 1/2-order low-pass filtering capacitive lattice scaling fracmemristor in Fig. 3(a) has the same circuit configuration as that of the $(n+1)\,th$ series circuit of the υ-order one in Fig. 2(a). Provided the number of the series circuit is infinite, ${}^{\alpha^n}_{\beta^n}FM^c_{-1/2}$ is the 1/2-order capacitive reactance of the 1/2-order low-pass filtering capacitive lattice scaling fracmemristor in Fig. 3. As we know, Kirchhoff's Current Law (KCL) and Kirchhoff's Voltage Law (KVL) describe the topological constraints, which construct the basic theory of circuits and systems [61], [62]. KCL (the algebraic sum of currents in a circuit meeting at a point is zero) and KVL (the algebraic sum of the voltage around any closed network is zero) can be described as two constraint algebraic equations, which merely depend on the topological structure and have nothing to do with the electrical characteristics of the circuit devices in a circuit. Since the memristor is a nonlinear circuit element, a circuit consisted of the memristor is also a nonlinear circuit. In classic theory of circuits and systems, the model of a nonlinear circuit can be described as a constraint equation $f(q,\varphi,I,V,t)=0$. Since a nonlinear circuit consisted of memristor still satisfies the law of conservation of charge and the law of conservation of energy, $f(q,\varphi,I,V,t)$ conforms to KCL and KVL [2]–[4], [61], [62]. With regard to the four circuit variables in $f(q,\varphi,I,V,t)$, there are two differential mapping relationships, $c/dt = I$ and $d\varphi/dt = V$, between (q and φ) and (I and V), respectively. From (1), (2) and Fig. 1, we can observe that in the Chua's axiomatic element system, the resistor, capacitor, inductor and memristor satisfy $(\mu=0,\eta=0)$, $(\mu=0,\eta=-1)$, $(\mu=-1,\eta=0)$ and $(\mu=-1,\eta=-1)$, respectively [2]–[4]. A memristor in the small-signal behavior about Q can be described as $V_i^{(-1)}(t) = m_Q I_i^{(-1)}(t)$, thus its small-signal reactance $Z(s)=m_Q$ can be interpreted as the impedance of an associated linearized element about Q [2]–[4]. Therefore, in the case of small-signal behavior about Q, the electrical characteristics of a circuit consisted of the memristor can be analyzed according to KCL and KVL [2]–[4], [61], [62].

In Fig. 3(b), let's assume that $i_r(s)$ and $i_c(s)$ are the currents of $\alpha^n r[q(s)]$ and $1/(\beta^n cs)$, respectively. $V_i(s)$ and $I_i(s) = i_r(s) + i_c(s)$ denote the input voltage and input current of ${}^{\alpha^n}_{\beta^n}FM^c_{-1/2}$, respectively. Therefore, in the case of small-signal behavior about Q, according to KCL and KVL, we obtain from Fig. 3 the following relationship:

$$\begin{cases} \alpha^n r\,[q(s)]\,i_r(s) + \left[1/(\beta^n cs)\right] i_c(s) - V_i(s) = 0 \\ \left\{\alpha^n r\,[q(s)] + {}^{\alpha^n}_{\beta^n}FM^c_{-1/2}\right\} i_r(s) \\ \quad - \left[{}^{\alpha^n}_{\beta^n}FM^c_{-1/2} + 1/(\beta^n cs)\right] i_c(s) = 0. \end{cases} \tag{9}$$

Thus, according to the Cramer's rule of linear algebra, from (9), we get:

$$\begin{cases} i_r(s) = \dfrac{\left[1/(\beta^n cs) + {}^{\alpha^n}_{\beta^n}FM^c_{-1/2}\right] V_i(s)}{\begin{vmatrix} \alpha^n r[q(s)] + {}^{\alpha^n}_{\beta^n}FM^c_{-1/2} & -\left[{}^{\alpha^n}_{\beta^n}FM^c_{-1/2} + 1/(\beta^n cs)\right] \\ \alpha^n r\,[q(s)] & 1/(\beta^n cs) \end{vmatrix}} \\ i_c(s) = \dfrac{\left[\alpha^n r\,[q(s)] + {}^{\alpha^n}_{\beta^n}FM^c_{-1/2}\right] V_i(s)}{\begin{vmatrix} \alpha^n r\,[q(s)] + {}^{\alpha^n}_{\beta^n}FM^c_{-1/2} & -\left[{}^{\alpha^n}_{\beta^n}FM^c_{-1/2} + 1/(\beta^n cs)\right] \\ \alpha^n r\,[q(s)] & 1/(\beta^n cs) \end{vmatrix}}. \end{cases} \tag{10}$$

Then, from (10), ${}^{\alpha^n}_{\beta^n}FM^c_{-1/2}$ can be derived as:

$$\begin{aligned} &{}^{\alpha^n}_{\beta^n}FM^c_{-1/2} \\ &= \frac{V_i(s)}{I_i(s)} \\ &= \frac{2\alpha^n r[q(s)]\left[1/(\beta^n cs)\right] + {}^{\alpha^n}_{\beta^n}FM^c_{-1/2}\{\alpha^n r\,[q(s)] + 1/(\beta^n cs)\}}{2{}^{\alpha^n}_{\beta^n}FM^c_{-1/2} + \alpha^n r\,[q(s)] + 1/(\beta^n cs)}. \end{aligned} \tag{11}$$

Thus, from (11), the following can be obtained:

$${}^{\alpha^n}_{\beta^n}FM^c_{-1/2} = V_i(s)/I_i(s) = \left(\beta^n c\right)^{-1/2}\left\{\alpha^n r[q(s)]\right\}^{1/2} s^{-1/2}. \tag{12}$$

From (12), we can observed that at first, there is a negative 1/2-order complex variable of the Laplace transform $s^{-1/2}$ (a 1/2-order integral capacitive operator), however, there is also a $\{r\,[q\,(s)]\}^{-1/2}$ in the formula of ${}^{\alpha^n}_{\beta^n}FM^c_{-1/2}$. Thus, being more complex than a pure fractional-element (ideal capacitive fractor), the cascade circuit with a series connection of infinitely repeated lattice scaling structures (when $m \to \infty$) in Fig. 3 achieves a 1/2-order low-pass filtering nonlinear capacitive operation. Secondly, as subsequent mathematically derivation, provided the number of the series circuit is infinite, the fractional-order $\upsilon = 1/2$ of a 1/2-order low-pass filtering capacitive lattice scaling fracmemristor can be also solely derived from (25). Thirdly, as subsequent further demonstration in following Example 1, in a certain passband, both the magnitude and the phase of the 1/2-order capacitive reactance of the 1/2-order capacitive lattice scaling fracmemristor with m series circuits, ${}^{\alpha^n}_{\beta^n}FM^c_{-1/2}$, can approach those of the ideal 1/2-order capacitive fracmemristor with a high degree of accuracy. The larger m is, the wider the passband of the 1/2-order capacitive lattice scaling fracmemristor is. From aforementioned discussion, in the case of small-signal behavior about Q, according to KCL and KVL, the electrical characteristics of a 1/2-order low-pass filtering capacitive lattice scaling fracmemristor can be derived as (12).

Furthermore, the infinitely iterative circuit configurations of the υ-order low-pass filtering capacitive lattice scaling fracmemristor can be shown in Fig. 4.

In Fig. 4, Z^0, Z^1, Z^2 and Z^{n-1} denote the driving-point capacitive impedance function of the first, the second, the third, and the nth iterative circuit of the υ-order low-pass filtering capacitive lattice scaling fracmemristor, respectively. In Fig. 4(e), let's assume that $i_r(s)$ and $i_c(s)$ are the currents of $r[q(s)]$ and c, respectively. $V_i(s)$ and $I_i(s)$ are the input voltage and the input current of Z^0, respectively. Thus, from Fig. 4(e), according to KCL and KVL, we obtain:

$$\begin{cases} r[q(s)]i_r(s) + [1/(cs)]\,i_c(s) - V_i(s) = 0 \\ \left(r[q(s)] + {}^{\alpha}_{\beta}FM^c_{-1/2}\right) i_r(s) \\ \quad - \left\{{}^{\alpha}_{\beta}FM^c_{-1/2} + [1/(cs)]\right\} i_c(s) = 0. \end{cases} \tag{13}$$

Then, according to the Cramer's rule of linear algebra, from (13), we have:

$$\begin{cases} i_r(s) = \dfrac{\left\{[1/(cs)] + {}^{\alpha}_{\beta}FM^c_{-1/2}\right\} V_i(s)}{\begin{vmatrix} r[q(s)] + {}^{\alpha}_{\beta}FM^c_{-1/2} & -\left\{[1/(cs)] + {}^{\alpha}_{\beta}FM^c_{-1/2}\right\} \\ r[q(s)] & [1/(cs)] \end{vmatrix}} \\ i_c(s) = \dfrac{\left\{r[q(s)] + {}^{\alpha}_{\beta}FM^c_{-1/2}\right\} V_i(s)}{\begin{vmatrix} r[q(s)] + {}^{\alpha}_{\beta}FM^c_{-1/2} & -\left\{[1/(cs)] + {}^{\alpha}_{\beta}FM^c_{-1/2}\right\} \\ r[q(s)] & [1/(cs)] \end{vmatrix}}. \end{cases} \tag{14}$$

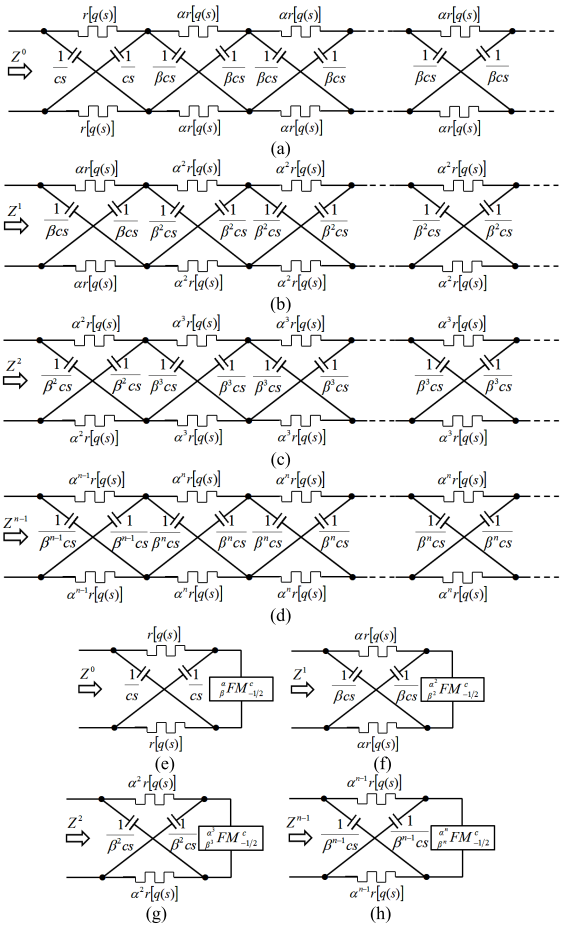


Fig. 4. Infinitely iterative circuit configurations of υ-order low-pass filtering capacitive lattice scaling fracmemristor: (a) First iterative circuit; (b) Second iterative circuit; (c) Third iterative circuit; (d) nth iterative circuit; (e) Equivalent circuit of first iterative circuit; (f) Equivalent circuit of second iterative circuit; (g) Equivalent circuit of third iterative circuit; (h) Equivalent circuit of nth iterative circuit.

Then, (14) can be rewritten as:

$$Z^0(s) = \frac{V_i(s)}{I_i(s)} = \frac{V_i(s)}{i_r(s) + i_c(s)} = \frac{2r[q(s)]\,(1/cs) + \frac{\alpha}{\beta}FM^c_{-1/2}\{r[q(s)] + 1/cs\}}{2\frac{\alpha}{\beta}FM^c_{-1/2} + r[q(s)] + 1/cs}. \quad (15)$$

Substituting (12) into (15), we obtain:

$$Z^0(s) = \frac{2r[q(s)]/(cs) + \sqrt{\alpha r[q(s)]/(\beta cs)}\{r[q(s)] + 1/(cs)\}}{2\sqrt{\alpha r[q(s)]/(\beta cs)} + r[q(s)] + 1/(cs)}. \quad (16)$$

Further, from Figs. 4(b), 4(c), 4(b) and 4(c), we get $Z^1(s) = \alpha Z^0(\alpha\beta s)$ and $Z^2(s) = \alpha Z^1(\alpha\beta s)$, respectively. In a similar way, from Figs. 4(d) and 4(h), we obtain (17), as shown at the bottom of this page. Equations (16) and (17) show that the υ-order low-pass filtering capacitive lattice scaling fracmemristor shown in Fig. 2 (a) can be treated as an infinitely successively nested structure of the first, the second, the third, $\cdots$ and the nth iterative circuit ($n \to \infty$) shown in Fig. 4. Thus, provided $n \to \infty$, the υ-order capacitive reactance of the υ-order low-pass filtering capacitive lattice scaling fracmemristor is equal to the limiting value of the recursion equation of successively nested $Z^0(s)$, $Z^1(s)$, $Z^2(s)$, $\cdots$ and $Z^{n-1}(s)$. Hence, from (16) and (17), if $n \to \infty$, the υ-order iterative capacitive reactance of the υ-order low-pass filtering capacitive lattice scaling fracmemristor can be derived as:

$$FM^{nc}_{-\upsilon}(s) = \frac{2r[q(s)]/(cs) + \alpha FM^{(n-1)c}_{-\upsilon}(\alpha\beta s)\{r[q(s)] + 1/(cs)\}}{2\alpha FM^{(n-1)c}_{-\upsilon}(\alpha\beta s) + r[q(s)] + 1/(cs)}, \quad (18)$$

where $FM^{nc}_{-\upsilon}(s)$ and $FM^{(n-1)c}_{-\upsilon}(s)$ are the driving-point capacitive impedance functions of the υ-order low-pass filtering capacitive lattice scaling fracmemristor with n series circuits and that with $(n-1)$ series circuits, respectively. Equation (18) is essentially a specific continued fraction expansion. Therefore, from Figs. 2 and 4, provided $n \to \infty$, it follows that:

$$FM^{c}_{-\upsilon}(s) = \lim_{n\to\infty} FM^{nc}_{-\upsilon}(s) = \lim_{n\to\infty} FM^{(n-1)c}_{-\upsilon}(s). \quad (19)$$

Then, from (19), (18) can be rewritten as:

$$FM^{c}_{-\upsilon}(s) = \frac{2r[q(s)]/(cs) + \alpha FM^{c}_{-\upsilon}(\alpha\beta s)\{r[q(s)] + 1/(cs)\}}{2\alpha FM^{c}_{-\upsilon}(\alpha\beta s) + r[q(s)] + 1/(cs)}. \quad (20)$$

In (20), $\alpha\beta$ is actually the fractal scaling factor of the υ-order low-pass filtering capacitive lattice scaling fracmemristor. Equation (20) is the irregular iterative scaling equation of the υ-order low-pass filtering capacitive lattice scaling fracmemristor, which accords with standard dynamical scaling law [63]–[67]. Hence, the solution of (20) can be given as:

$$FM^{c}_{-\upsilon}(s) = \kappa(s)\, s^{-\upsilon}, \quad (21)$$

where $\kappa(s)$ is a scalar factor. Although the irregular iterative scaling equation maybe has multiple solutions in pure mathematics, the true solution of (20) must accord with the actual circuit of the υ-order low-pass filtering capacitive lattice scaling fracmemristor shown in Fig. 2(a). All other multiple solutions of (20) are spurious solutions. From Fig. 2(a), by means of nested iterations, the generic fractional-order driving-point impedance functions of an arbitrary-order capacitive fracmemristor in their natural implementations can be derived as (5) [55]. Thus, with regard to the υ-order low-pass filtering capacitive lattice scaling fracmemristor, substituting (16) into (17) recursively, by means of mathematical

$$\begin{aligned} Z^{n-1}(s) &= \frac{2\alpha^{n-1}r[q(s)]/\left(\beta^{n-1}cs\right) + \sqrt{\alpha^n r[q(s)]/(\beta^n cs)}\left\{\alpha^{n-1}r[q(s)] + 1/\left(\beta^{n-1}cs\right)\right\}}{2\sqrt{\alpha^n r[q(s)]/(\beta^n cs)} + \alpha^{n-1}r[q(s)] + 1/\left(\beta^{n-1}cs\right)} \\ &= \alpha\frac{2\alpha^{n-2}r[q(s)]/\left[\beta^{n-2}c\,(\alpha\beta s)\right] + \sqrt{\alpha^{n-1}r[q(s)]/\left[\beta^{n-1}c\,(\alpha\beta s)\right]}\left\{\alpha^{n-2}r[q(s)] + 1/\left[\beta^{n-2}c\,(\alpha\beta s)\right]\right\}}{2\sqrt{\alpha^{n-1}r[q(s)]/\left[\beta^{n-1}c\,(\alpha\beta s)\right]} + \alpha^{n-2}r[q(s)] + 1/\beta^{n-2}c\,(\alpha\beta s)} \\ &= \alpha Z^{n-2}(\alpha\beta s). \end{aligned} \quad (17)$$

induction, we can obtain the limiting value of $\kappa(s)$ when $n \to \infty$:

$$\kappa(s) \overset{n\to\infty}{\approx} c^{-\upsilon}\{r[q(s)]\}^{1-p}, \tag{22}$$

where $\upsilon = \eta + p$ that is the same as that of (5) and (6). Equations (21) and (22) are consistent with (5). Further, substituting (21) into (20) results in:

$$\begin{aligned}\kappa s^{-\upsilon} &= \frac{2r[q(s)]/(cs) + \alpha\kappa(\alpha\beta s)^{-\upsilon}\{r[q(s)] + 1/(cs)\}}{2\alpha\kappa(\alpha\beta s)^{-\upsilon} + r[q(s)] + 1/(cs)} \\ &= \frac{2r[q(s)] + \alpha\kappa(\alpha\beta s)^{-\upsilon}(r[q(s)]cs + 1)}{2\alpha\kappa(\alpha\beta s)^{-\upsilon} cs + r[q(s)]cs + 1}.\end{aligned} \tag{23}$$

Since $0 < \upsilon < 1$, when $s \to 0$, we have $s^{-\upsilon}s \to 0$ and $\kappa(s) \overset{s\to 0}{\approx} \kappa(\alpha\beta s)$. Then, when $s \to 0$ (low-pass filtering), (23) can be simplified as:

$$\begin{aligned}\kappa s^{-\upsilon} &= \frac{2r[q(s)] + \alpha\kappa(\alpha\beta s)^{-\upsilon}(r[q(s)]cs + 1)}{2\alpha\kappa(\alpha\beta s)^{-\upsilon} cs + r[q(s)]cs + 1} \\ &\overset{s\to 0}{\approx} \frac{\alpha\kappa(\alpha\beta s)^{-\upsilon}(r[q(s)]cs + 1)}{r[q(s)]cs + 1} = \alpha\kappa(\alpha\beta s)^{-\upsilon}.\end{aligned} \tag{24}$$

Therefore, when $s \to 0$ (low-pass filtering), the solution of (24) can be derived as:

$$\upsilon = \log(\alpha)/\big[\log(\alpha) + \log(\beta)\big], \tag{25}$$

where $\log()$ is a logarithm. Equation (25) shows that the fractional-order of the υ-order low-pass filtering capacitive lattice scaling fracmemristor shown in Fig. 2 merely essentially depends on its two positive scaling factors (α and β), but has nothing to do with its reactance of a memristor and capacitance ($r[q(s)]$ and c). Note that if the fractional order v>1, active element should be also applied to the analog circuit implementation of fracmemristor. In particular, with regard to Fig.4, the positive scaling factor of the reactance of a memristor and that of the capacitance of its every series circuit, α^n and β^n, are identical, respectively. Then, comparing Fig. 2(a) with Fig. 3, we can observe that if we substitute $\alpha^n r[q(s)]$ and $1/(\beta^n cs)$ for $r[q(s)]$ and $1/(cs)$ in Fig. 2(a), respectively, Fig. 3 is equivalent to Fig. 2(a) with two positive scaling factors $\alpha = 1$ and $\beta = 1$. Thus, from (25), provided $\alpha \to 1$ and $\beta \to 1$, we can derive that $\lim_{\alpha\to 1,\beta\to 1} \upsilon = 1/2$, which is consistent with the derivation of (12). Substituting $\alpha = 1$ and $\beta = 1$ and $\upsilon = 1/2$ into (21), (22) and (23) gives:

$$\begin{aligned}FM^{c}_{-\upsilon}(s) &\overset{\alpha=1,\beta=1}{=} FM^{c}_{-1/2}(s) = \kappa s^{-1/2} \\ &= c^{-1/2}\{r[q(s)]\}^{1/2} s^{-1/2}.\end{aligned} \tag{26}$$

Equation (26) shows that if $\alpha = 1$ and $\beta = 1$, (24) can be accurately simplified as $\kappa s^{-\upsilon} \overset{s\to 0}{=} \alpha\kappa(\alpha\beta s)^{-\upsilon}\big|_{\alpha=1,\beta=1,\upsilon=1/2}$. The 1/2-order low-pass filtering capacitive lattice scaling fracmemristor is a special case of the purely ideal υ-order capacitive fracmemristor [55]. From aforementioned discussion, in the case of small-signal behavior about Q, according to KCL and KVL, the fractional-order υ of an arbitrary-order low-pass filtering capacitive lattice scaling fracmemristor can be determined by means of altering its two positive scaling factors (α and β) in (25).

In addition, (24) further shows that to improve its approximation accuracy, an impedance, $-2r[q(s)]/\{r[q(s)]cs + 1\}$, should be compensatory in the first series circuit of the υ-order low-pass filtering capacitive lattice scaling fracmemristor shown in Fig. 2(a), as illustrated in Fig. 5.

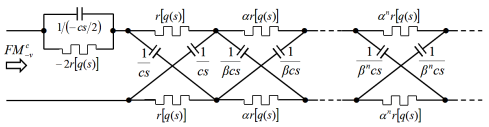


Fig. 5. Circuit configuration of υ-order compensatory low-pass filtering capacitive lattice scaling fracmemristor.

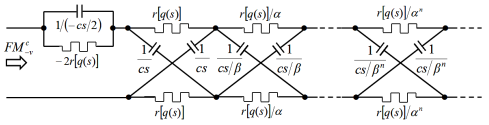


Fig. 6. Circuit configuration of υ-order compensatory high-pass filtering capacitive lattice scaling fracmemristor.

In Fig. 5, negative reactance of a memristor and negative capacitance can be achieved by negative impedance converter. Thus, from Fig. 5, the fractional-order driving-point impedance function of the υ-order compensatory low-pass filtering capacitive lattice scaling fracmemristor can be derived as $\kappa s^{-\upsilon} = \frac{2r[q(s)]+\alpha\kappa(\alpha\beta s)^{-\upsilon}(r[q(s)]cs+1)}{2\alpha\kappa(\alpha\beta s)^{-\upsilon}cs+r[q(s)]cs+1} - \frac{2r[q(s)]}{r[q(s)]cs+1} \overset{s\to 0}{=} \alpha\kappa(\alpha\beta s)^{-\upsilon}$. Thus, by adding the first compensatory series circuit of the υ-order low-pass filtering capacitive lattice scaling fracmemristor, (25) can be accurately derived.

In a similar way, with respect to the υ-order high-pass filtering capacitive lattice scaling fracmemristor shown in Fig. 2(b), $FM^{c}_{-\upsilon}(s) = \frac{2r[q(s)]/(cs)+(1/\alpha)FM^{c}_{-\upsilon}[s/(\alpha\beta)]\{r[q(s)]+1/(cs)\}}{2(1/\alpha)FM^{c}_{-\upsilon}[s/(\alpha\beta)]+r[q(s)]+1/(cs)}$ and $FM^{c}_{-\upsilon}(s) = \kappa(s)s^{-\upsilon}$ can be derived. Since $0 < \upsilon < 1$, when $s \to \infty$, we have $s^{-\upsilon} \to 0$ $\kappa(s) \overset{s\to\infty}{\approx} \kappa(\alpha\beta s)$. Thus, when $s \to \infty$ (high-pass filtering), we have:

$$\begin{aligned}&\kappa s^{-\upsilon} \\ &= \frac{2r[q(s)]/(cs) + (1/\alpha)\kappa[s/(\alpha\beta)]^{-\upsilon}\{r[q(s)] + 1/(cs)\}}{2(1/\alpha)\kappa[s/(\alpha\beta)]^{-\upsilon} + r[q(s)] + 1/(cs)} \\ &\overset{s\to\infty}{\approx} \frac{(1/\alpha)\kappa[s/(\alpha\beta)]^{-\upsilon}(r[q(s)]cs + 1)}{r[q(s)]cs + 1} \\ &= (1/\alpha)\kappa[s/(\alpha\beta)]^{-\upsilon}.\end{aligned} \tag{27}$$

Then, when $s \to \infty$ (high-pass filtering), the solution of (27) can be derived as $\upsilon = \lg(\alpha)/\big[\lg(\alpha) + \lg(\beta)\big]$. In particular, if $\alpha = 1$ and $\beta = 1$, $\kappa s^{-\upsilon} \overset{s\to\infty}{=} (1/\alpha)\kappa[s/(\alpha\beta)]^{-\upsilon}\big|_{\alpha=1,\beta=1,\upsilon=1/2}$. The classical 1/2-order high-pass filtering capacitive lattice scaling fracmemristor is a special case of the purely ideal υ-order capacitive fracmemristor [55]. In addition, (27) further shows that to improve its approximation accuracy, an impedance, $-2r[q(s)]/\{r[q(s)]cs + 1\}$, should be compensatory in the first series circuit of the υ-order high-pass filtering capacitive lattice scaling fracmemristor shown in Fig. 2(b), as illustrated in Fig. 6.

Comparing Fig. 6 with Fig. 5, we can see that the first compensatory series circuit of the υ-order compensatory high-pass filtering capacitive lattice scaling fracmemristor is the same as that of the υ-order compensatory low-pass filtering one.

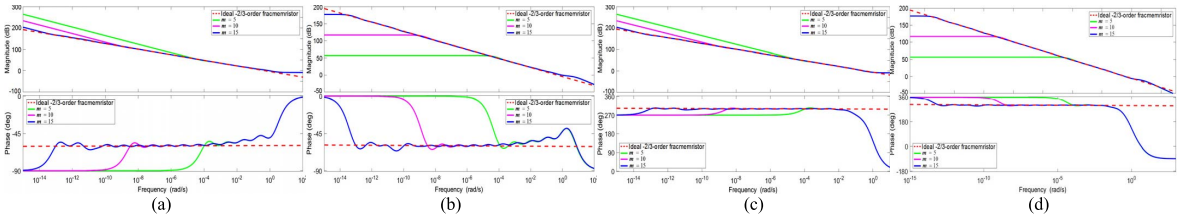


Fig. 7. Bode diagrams of fractional-order capacitive reactances of a 2/3-order low-pass filtering capacitive lattice scaling fracmemristor with m series circuits and corresponding 2/3-order compensatory one: (a) Open-circuit capacitive reactance $Z^{om}_{-2/3}$; (b) Short-circuit capacitive reactance $Z^{sm}_{-2/3}$; (c) Compensatory open-circuit capacitive reactance $Z^{om}_{-2/3}$; (d) Compensatory short-circuit capacitive reactance $Z^{sm}_{-2/3}$.

IV. Experiment and Analysis

A. Approximation Performance of Arbitrary-Order Capacitive Lattice Scaling Fracmemristor

In this subsection, the effect of the number of series circuits on the approximation performance of an arbitrary-order low-pass filtering capacitive lattice scaling fracmemristor is analyzed, which is similar to that of an arbitrary-order high-pass filtering one.

Example 1: Without loss of generality, the approximate implementation of a 2/3-order low-pass filtering capacitive lattice scaling fracmemristor is illustrated. In particular, from (25), let's set $\alpha = 4$ and $\beta = 2$, we obtain $\upsilon = 2/3$. Suppose the capacitance $c = 1$. Equation (2) shows that the memristance $R[q(t)]$ and transmission function $H[q(t)]$ change with the input current $I_i(t)$ of a memristor. For the convenience of illustration, let's set the transmission function of a memristor $H[q(t)] = \delta(t)$, where $\delta(t)$ is an impulse signal. Thus, the reactance of this memristor $r[q(s)] = L\{H[q(t)]\} = 1$. Thus, from Fig. 2(a), the Bode diagrams of the fractional-order capacitive reactances of this 2/3-order low-pass filtering capacitive lattice scaling fracmemristor with m series circuits and the corresponding 2/3-order compensatory one can be shown as given in Fig. 7, respectively.

Figure 7 shows that at first, the optimum value of m is closely related to the pass-band of actually design. Both the magnitude and the phase of $Z^{om}_{-2/3}$ and $Z^{sm}_{-2/3}$ of the 2/3-order low-pass filtering capacitive lattice scaling fracmemristor with m series circuits and those of the corresponding 2/3-order compensatory one can approach those of the ideal 2/3-order capacitive fracmemristor with a high degree of accuracy in a certain pass-band. The larger m is, the wider the pass-band of the 2/3-order low-pass filtering capacitive lattice scaling fracmemristor is. When $m = 15$, the pass-band is [10^{-13} rad/sec, 10^{0} rad/sec]. Secondly, the approximation performance of the 2/3-order compensatory low-pass filtering capacitive lattice scaling fracmemristor is more precise and smoother than that of the corresponding 2/3-order low-pass filtering one. As shown in Fig. 5 and Fig. 7, (24) converts to the regularized iterative scaling equation of a υ-order compensatory low-pass filtering capacitive lattice scaling fracmemristor, which can be more accurately simplified as $ks^{-\upsilon} = \alpha k(\alpha\beta s)^{-\upsilon}$ when $s \to 0$. The intrinsic effect of the compensatory circuit in the first series circuit is to change the pole-zero location of the υ-order low-pass filtering capacitive lattice scaling fracmemristor by means of zero pole cancellation. From aforementioned discussion, the larger m is, the wider the pass-band of the fractional-order capacitive lattice scaling fracmemristor is.

B. Electrical Characteristics of Fracmemristor

In this subsection, to recognize whether a circuit element is fracmemristor or not, the electrical characteristics of the fracmemristor, especially the fingerprints of a fracmemristor, are studied.

Example 2: Without loss of generality, let's take a current-controlled capacitive fracmemristor as an example to analyze the electrical characteristics of the fracmemristor. Let's assume that the input causal current sources $I_i(t) = sin(at)\,u(t)$ applied across a memristor and a fracmemristor are identical, where a is frequency and $u(t)$ is a Heaviside function. Thus, $I_i(s) = a/(s^2 + a^2)$ and the corresponding quantity of electric charge $q(t) = D_t^{-1} I_i(t) = -(1/a)\cos(at)\,u(t)$. And assuming that $M[q(t)] = q(t)/2 + 1/a$. Thus, from (2), we have:

$$\begin{aligned} R[q(t)] &= [M(q) + qdM(q)/dq] \\ &= [-(1/a)\cos(at) + 1/a]\,u(t). \end{aligned} \tag{28}$$

Then, from (2) and (28), the instantaneous value of the input voltage of a memristor can be derived as:

$$\begin{aligned} V_i(t) &= R[q(t)]\,I_i(t) = H[q(t)] * I_i(t) \\ &= [-[1/(2a)]\sin(2at) + (1/a)\sin(at)]\,u(t), \end{aligned} \tag{29}$$

where $R[q(t)] = \{H[q(t)] * I_i(t)\}/I_i(t)$. And assuming the initial state of this memristor is zero, thus the Laplace transform of (29) is as follows:

$$V_i(s) = r[q(s)]I_i(s) = 3a^2/\left[\left(s^2 + 4a^2\right)\left(s^2 + a^2\right)\right], \tag{30}$$

where the reactance of this memristor $r[q(s)] = L\{H[q(t)]\}$. For $I_i(s) = a/(s^2 + a^2)$, form (30), we have:

$$r[q(s)] = 3a/\left(s^2 + 4a^2\right). \tag{31}$$

The inverse Laplace transform of (31) is the transmission function $L^{-1}\{r[q(s)]\} = H[q(t)] = (3/2)\,sin(2at)\,u(t)$ of a memristor. Further, in (5) and (7), for $\upsilon = \eta + p$, from (31), we obtain:

$$\begin{aligned} L^{-1}\left\{[r(q)]^{1-p}\right\} &= (3a)^{1-p}\sqrt{\pi}/\Gamma(1-p) \\ &\quad \times [t/(4a)]^{(1/2-p)}\,J_{(1/2-p)}(2at)u(t), \end{aligned} \tag{32}$$

where $J_{(1/2-p)}(t)$ is a Bessel function of the first kind extended to non-integer orders by one of Schläfli's integrals. Then, substituting (32) into (7), the voltage-current relation equation of a υ-order capacitive fracmemristor can be derived.

Therefore, from (2), (5), (7), (29) and (32), the constitutive relation of a fracmemristor can be analyzed in the V_i-I_i plane. At first, let's illustrate the effect of the fractional-order υ on the electrical characteristics of a fracmemristor. Let's set the frequency $a = 1$ rad/s and the time duration of $I_i(t)$ be equal to 6π. To illustrate the $V_i(t)$ curves of the memristor and the fracmemristor in the same plot, the experimental values of

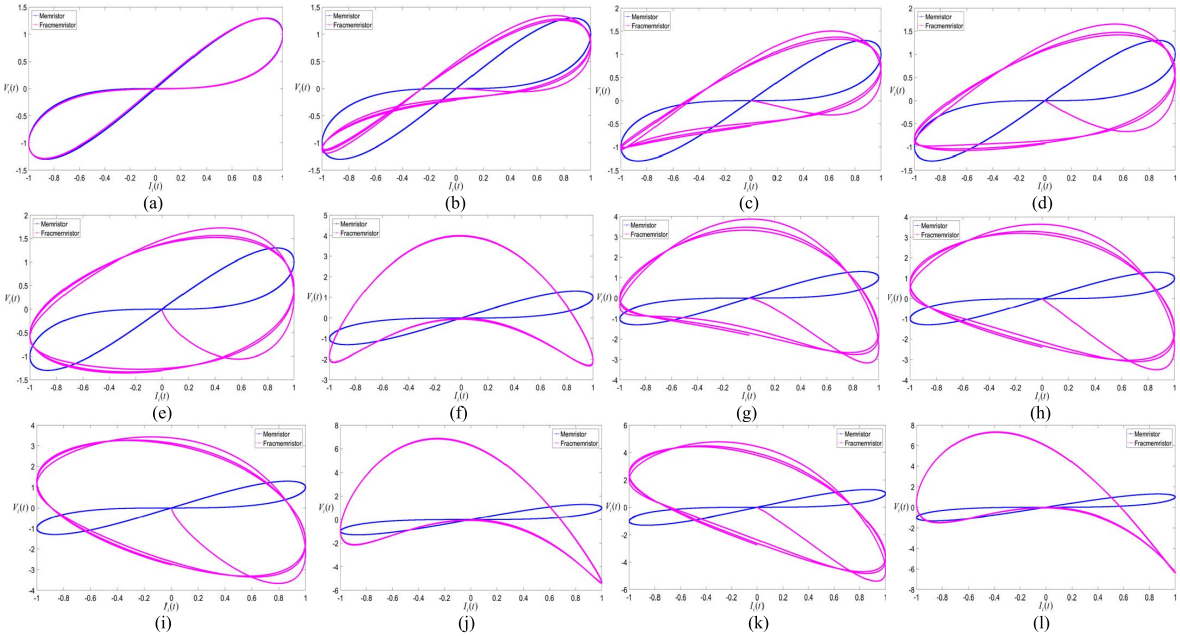


Fig. 8. V_i-I_i curve of ideal υ-order capacitive fracmemristors: (a) 0.001-order one; (b) 1/6-order one; (c) 1/3-order one; (d) 1/2-order one; (e) 2/3-order one; (f) 1-order one; (g) 4/3-order one; (h) 3/2-order one; (i) 5/3-order one; (j) 2-order one; (k) 5/2-order one; (l) 3-order one.

the fracmemristor are divided by 1000. To avoid completely overlapping the V_i-I_i curve of a fracmemristor with that of a memristor and inconvenience of demonstration, let's set $\upsilon = 0.001$ when $\upsilon = 0$. Thus, the V_i-I_i curve of the ideal υ-order capacitive fracmemristor can be shown in Fig. 8.

From Fig. 8, (3), (5), (7) and (32), we can observe that if the initial state of an ideal capacitive fracmemristor is zero and it is stimulated by a bipolar periodic signal with zero starting value, at first, when the fractional-order $\upsilon \to 0$, from (7) and (32), an ideal capacitive fracmemristor degenerates to an ideal memristor, which is lying on the point of M in Fig. 1. Thus, in Fig. 8(a), the V_i-I_i curve of an ideal 0.001-order capacitive fracmemristor almost overlaps that of an ideal memristor, which has multiple-valued Lissajous curves for all $I_i(t)$ except when it passes through the pinched point $(0, 0)$. Secondly, when $0 < \upsilon$ is not a positive integer, from (7) and (32), the electrical properties of a capacitive fracmemristor fall in between those of the capacitor and those of the memristor [55]. The capacitive fracmemristor is lying on the line segment, S_4, between C and M in Fig. 1. In particular, on the one hand, when $0 < \upsilon < \upsilon_{th}$, the effect of memristor on the electrical properties of a capacitive fracmemristor is larger than that of capacitor, where υ_{th} is a critical order that nonlinearly depends on the fractional-order υ, the system parameter and original state of a capacitive fracmemristor as well as the amplitude and frequency of $I_i(t)$. Then, in Fig. 8(b), the V_i-I_i curve of an ideal 1/6-order capacitive fracmemristor has also a pinched hysteresis loop start from the original point of $(0, 0)$. However, the pinched point of the multiple-valued Lissajous curves is no longer fixed at the point of $(0, 0)$, but continuously drifts from the original point $(0, 0)$ to the top of one side lobe of the V_i-I_i curve along with the increasing of υ. In Fig. 8(c), when $\upsilon \to \upsilon_{th} \approx 1/3$, the pinched point disappears. On the other hand, when $\upsilon_{th} \leq \upsilon$, the effect of capacitor on the electrical properties of a capacitive fracmemristor is larger than that of memristor. Therefore, in Figs. 8(d), 8(e), 8(g), 8(h), 8(i) and 8(k), the V_i-I_i curve of an ideal υ-order capacitive fracmemristor is a nonlinear elliptic hysteresis loop, which has multiple-valued twisted ellipse curves for all $I_i(t)$ start from the original point of $(0, 0)$. Thirdly, when υ is a positive integer, from (5), (7) and (32), an ideal υ-order capacitive fracmemristor degenerates to an integer-order integrator, whose electrical properties merely possess those of the integer-order integral [55]. The capacitive fracmemristor is lying on the point of C in Fig. 1. Then, we certainly obtain $V_i(t + T) = 0$ and $V_i(t + T/2) \neq 0$, where T is the period of the bipolar periodic signal. Thus, in Figs. 8(f), 8(j) and 8(l), the V_i-I_i curve of an ideal υ-order capacitive fracmemristor is a nonlinear multiple-valued twisted elliptic hysteresis loop, which certainly passes through the point of $(0, 0)$.

Secondly, let's illustrate the effect of the frequency a of the input causal current sources $I_i(t)$ on the electrical characteristics of a fracmemristor. Thus, keeping the aforementioned parameter settings unchanged, the electrical characteristics of an ideal 2/3-order capacitive fracmemristor with $a = 2$ rad/s, $a = 3$ rad/s, $a = 4$ rad/s and $a = 100$ rad/s, can be shown in Fig. 9.

From Fig. 8(e), Fig. 9, (3), (5), (7) and (32), we can observe that at first, the input voltage of a capacitive fracmemristor nonlinearly consists of both the fundamental component and other harmonic component of $I_i(t)$, whose weight nonlinearly depends on the fractional-order υ, the system parameter and original state of a capacitive fracmemristor as well as the amplitude and frequency of $I_i(t)$. Therefore, the responses of the fracmemristor are nonlinearly periodic. In pure mathematical computations, the time duration of $s_1(t) * s_2(t)$ should be equal to the summation of the time duration of $s_1(t)$ and that of $s_2(t)$, where $s_1(t)$ and $s_2(t)$ are two analytic functions. However, for real causal circuits and systems, if we ignore the discharge process of the capacitor in a fracmemristor, when $I_i(t)$ has been powered off, a fracmemristor should not continue to run and its fracmemristance should remain unchanged. Therefore, although (7) has a mathematical computation of convolution, the time duration of $V_i(t)$ across a fracmemristor should be equal to the time duration of $I_i(t)$.

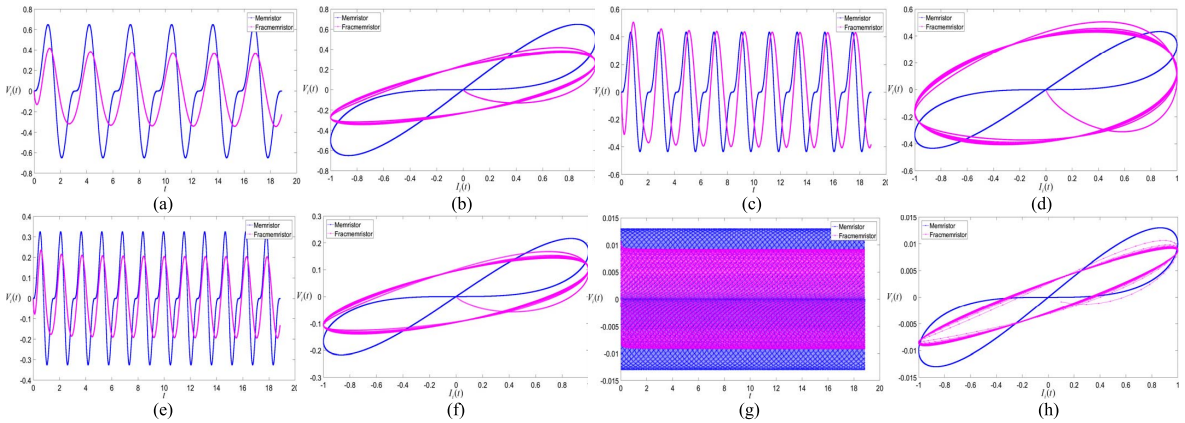


Fig. 9. Electrical characteristics of an ideal 2/3-order capacitive fracmemristors: (a) V_i-t curve with $a = 2$ rad/s; (b) V_i-I_i curve with $a = 2$ rad/s; (c) V_i-t curve with $a = 3$ rad/s; (d) V_i-I_i curve with $a = 3$ rad/s; (e) V_i-t curve with $a = 4$ rad/s; (f) V_i-I_i curve with $a = 4$ rad/s; (c) V_i-t curve with $a = 100$ rad/s; (d) V_i-I_i curve with $a = 100$ rad/s.

Thus, in Fig. 9, the curve of $V_i(t)$ across a fracmemristor persists for the time of $t = 6\pi$. Secondly, in (7) and (32), the weight of each harmonic component of $I_i(t)$ nonlinearly is in inverse proportion to the frequency a of $I_i(t)$. The corresponding lobe area of the nonlinear elliptic hysteresis loop in the V_i -I_i plane can be calculated by $\int V_i dI_i$. Thus, in Figs. 9(a), 9(c), 9(e) and 9(g), the amplitude of the V_i-t curve of a fracmemristor decreases with the increasing of the frequency a of $I_i(t)$. Meanwhile, in Figs. 9(b), 9(d), 9(f) and 9(h), the corresponding lobe area of the nonlinear elliptic hysteresis loop in the V_i-I_i plane decreases with the increasing of the frequency a of $I_i(t)$. In particular, when $a \to \infty$, the nonlinear elliptic hysteresis loop of a fracmemristor in the V_i-I_i plane shrinks to a straight line segment.

Therefore, from aforementioned discussion, the fingerprints of a fracmemristor can be summarized as four points: if the initial state of an ideal capacitive fracmemristor is zero and it is stimulated by a bipolar periodic signal with zero starting value, at first, if the fractional-order υ is equal to zero, it degenerates to a memristor. Its V_i-I_i curve is a pinched hysteresis loop, which is the same as that of the corresponding memristor. Secondly, if υ is a positive fraction, when $0 < \upsilon < \upsilon_{th}$, its V_i-I_i curve is also a pinched hysteresis loop, however, whose pinched point continuously drifts from the original point $(0, 0)$ to the top of one side lobe with the increasing of υ; Moreover, when $\upsilon_{th} \leq \upsilon$, the pinched point disappears, its V_i-I_i curve is a nonlinear elliptic hysteresis loop started from the original point of $(0, 0)$. Thirdly, if υ is a positive integer, it degenerates to an integer-order integrator. Its V_i-I_i curve is a nonlinear multiple-valued twisted elliptic hysteresis loop, which certainly passes through the point of $(0, 0)$. Fourthly, the corresponding lobe area of its nonlinear elliptic hysteresis loop in the V_i-I_i plane decreases with the increasing of the frequency a of $I_i(t)$. When $a \to \infty$, the nonlinear elliptic hysteresis loop of a fracmemristor in the V_i-I_i plane shrinks to a straight line segment.

C. Analog Circuit Achievement of an Arbitrary-Order Fracmemristor

In this subsection, without loss of generality, a 2/3-order high-pass filtering capacitive lattice scaling fracmemristor is implemented in the form of analog circuit.

Example 3: For the verification of the actual existence of a fracmemristor, we implement a fracmemristor in the form of analog circuit, which satisfied its corresponding electrical characteristics in Example 2, respectively. From (25), when $\alpha = 4$ and $\beta = 2$, we obtain $\upsilon = 2/3$. Let's suppose that the memristance and capacitance in Fig. 6 are $R[q(t)]$ and $c = 16\mu F$, respectively. Since $R[q(t)] = \{H[q(t)] * I_i(t)\}/I_i(t)$ and $r[q(s)] = L\{H[q(t)]\}$ in (2), the memristance $R[q(t)]$ keeps up the same multiple growths as the reactance $r[q(s)]$ of a memristor. Thus, from Fig. 2(b) and Fig. 6, we can implement a 2/3-order high-pass filtering capacitive lattice scaling fracmemristor with 5 open-circuit series circuits and a 2/3-order compensatory one, as shown in Fig. 10.

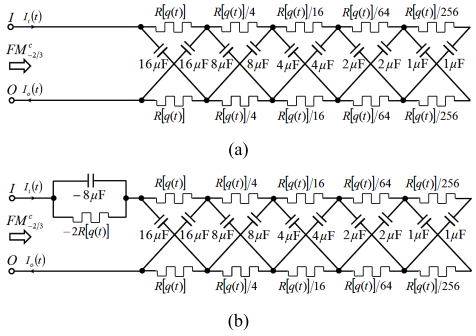


Fig. 10. Analog series circuit of a 2/3-order high-pass filtering capacitive lattice scaling fracmemristor: (a) 2/3-order one; (b) 2/3-order compensatory one.

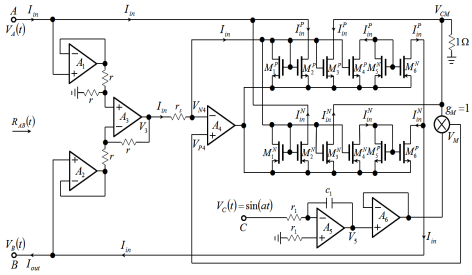


Fig. 11. A floating voltage-controlled memristor.

In Fig. 10, I and O are the input port and the output port of the analog series circuit of a 2/3-order high-pass filtering capacitive lattice scaling fracmemristor, respectively. Figure 10 shows that at first, in Fig. 10(b), the negative memristance and the negative capacitance can be achieved by negative impedance converter. Secondly, a key technical problem of the analog circuit implementation of a 2/3-order high-pass filtering capacitive lattice scaling fracmemristor is

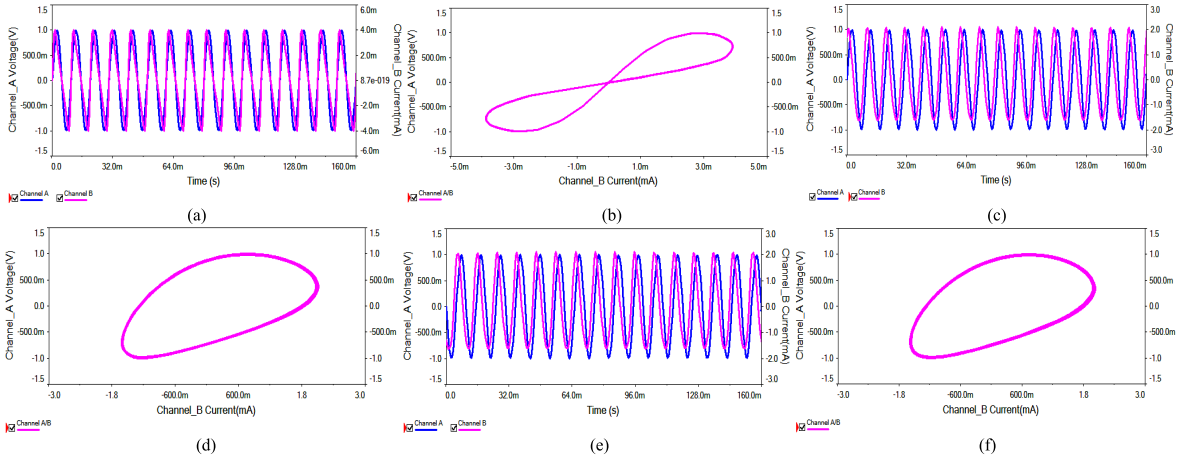


Fig. 12. Electrical characteristics of actual analog series circuits of a 2/3-order high-pass filtering capacitive lattice scaling fracmemristors: (a) V_i-t curve of memristor in 2/3-order capacitive fracmemristor; (b) V_i-I_i curve of memristor in 2/3-order capacitive fracmemristor; (c) V_i-t curve of 2/3-order capacitive fracmemristor; (d) V_i-I_i curve of 2/3-order capacitive fracmemristor; (e) V_i-t curve of 2/3-order compensatory capacitive fracmemristor; (f) V_i-I_i curve of 2/3-order compensatory capacitive fracmemristor.

to synchronously achieve the scaling memristance $R\left[q\left(t\right)\right]/\alpha^n$ without being affected by the branch-current or branch-voltage of its $(n+1)\,th$ series circuit. Thus, we should implement a floating voltage-controlled memristor that implements $R\left[q\left(t\right)\right] = \left[-\left(1/a\right)\cos\left(at\right)+1/a\right]u\left(t\right)$ in (28), as shown in Fig. 11.

In Fig. 11, A, B and C are the input port, the output port and the control voltage source input port of a floating voltage-controlled memristor, respectively. A_1, A_2 and A_6 are three voltage followers, A_3 is a subtracter, A_4 is a voltage-current converter and A_5 is a phase-reversing integrator. $V_A\left(t\right)$, $V_B\left(t\right)$, $V_C\left(t\right)$, I_{in} and I_{out} are the input voltage source, output voltage source, control voltage source, input current and output current of a floating voltage-controlled memristor, respectively. M_1^P, M_2^P, M_3^P, M_4^P, M_5^N and M_6^N are a multichannel positive Current Mirror (CM) copies the positive part of I_{in}. M_1^N, M_2^N, M_3^N, M_4^N, M_5^P and M_6^P are a multichannel negative CM copies the negative part of I_{in}. Thus, we obtain $I_{in} = I_{out}$. Let's set $r_s = 1/a$, $r_1c_1 = 1$ and multiplier gain $g_M = 1$. Thus, according to the virtual short and virtual off electrical characteristics of an operational amplifier, we can derive that $V_3 = V_A - V_B$, $V_5 = -1/\left(r_1c_1\right)\int\sin\left(at\right)dt = 1/a\cos\left(at\right)u\left(t\right)$, $V_{CM} = -I_{in}$, $V_{N4} = V_{P4} = V_M = g_MV_{CM}V_5 = -1/a\cos\left(at\right)I_{in}u\left(t\right)$ and $I_{in} = \left(V_3 - V_{N4}\right)/r_s$. Thus, we have:

$$V_3 = V_A - V_B = \left[-1/a\cos\left(at\right)+1/a\right]I_{in}u\left(t\right). \quad (33)$$

Thus, from (33), we obtain $R_{AB}\left(t\right) = R\left[q\left(t\right)\right] = \left[-\left(1/a\right)\cos\left(at\right)+1/a\right]u\left(t\right)$. Note that for the convenience of actual implementation, we can also use a programmable voltage-controlled resistance to achieve $R_{AB}\left(t\right) = R\left[q\left(t\right)\right] = \left[-\left(1/a\right)\cos\left(at\right)+1/a\right]u\left(t\right)$ directly.

Thus, in Fig. 11, let's set $a = 100\text{Hz}$, $r = 1\Omega$, $r_s = 0.01\Omega$, $r_1 = 1\text{M}\Omega$, $c = c_1 = 1\mu\text{F}$ and $I_i\left(t\right) = I_o\left(t\right) = \sin\left(at\right)u\left(t\right)$. Let's select the type of the operational amplifiers $A_1 - A_6$, N-type MOSFET $M_1^P - M_6^P$, P-type MOSFET $M_1^N - M_6^N$ and multiplier are OP37G, ALD1116PAL, ALD1117PAL and AD633ANZ, respectively. Therefore, from Fig. 10 and Fig. 11, using commonly used PCB design software of Multisim13, we can simulate the actual analog series circuits of a 2/3-order high-pass filtering capacitive lattice scaling fracmemristor and a 2/3-order compensatory one, whose electrical characteristics can be shown in Fig. 12.

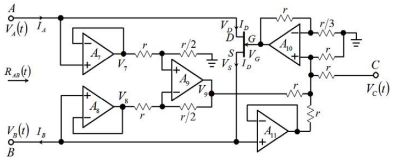


Fig. 13. A floating voltage-controlled linear resistor achieved by JFET.

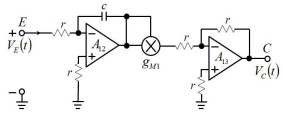


Fig. 14. A control voltage source $V_C\left(t\right)$.

In Fig. 12(a), Channel_A is the input voltage $\left[V_A\left(t\right) - V_B\left(t\right)\right]$ and Channel_B is the input current $I_{in}\left(t\right)$ in Fig. 11. In Fig. 12(b), Channel_B is the input current $I_{in}\left(t\right)$ and Channel_A is the input voltage $\left[V_A\left(t\right) - V_B\left(t\right)\right]$ in Fig. 11. In Figs. 12(c) and 12(e), Channel_A is the input voltage $\left[V_I\left(t\right) - V_O\left(t\right)\right]$ and Channel_B is the input current $I_{in}\left(t\right)$ in Fig. 10. In Figs. 12(d) and 12(f), Channel_B is the input current $I_{in}\left(t\right)$ and Channel_A is the input voltage $\left[V_I\left(t\right) - V_O\left(t\right)\right]$ in Fig. 10. Comparing Fig. 12 with Fig. 8(e) and Fig. 9, we can observe that at first, the electrical characteristics of a floating voltage-controlled memristor in Fig. 11 is approximately identical to those of the memristor in (28). The V_i-t curves and V_i-I_i curves of an actual 2/3-order capacitive fracmemristor accord with those of a theoretical ideal one. Secondly, the electrical characteristics of actual analog series circuits of a 2/3-order high-pass filtering capacitive lattice scaling fracmemristor in Fig. 10 are approximately identical to those of a corresponding ideal 2/3-order capacitive fracmemristor in (7) and (32). For the memristor in a 2/3-order capacitive fracmemristor, there is a pinched hysteresis loop in the V_i-I_i plane, which passes through the pinched point $(0, 0)$. For the corresponding 2/3-order capacitive fracmemristor, there is a nonlinear twisted ellipse curve in the V_i-I_i plane. Note that since we let Multisim13 doesn't begin to illustrate

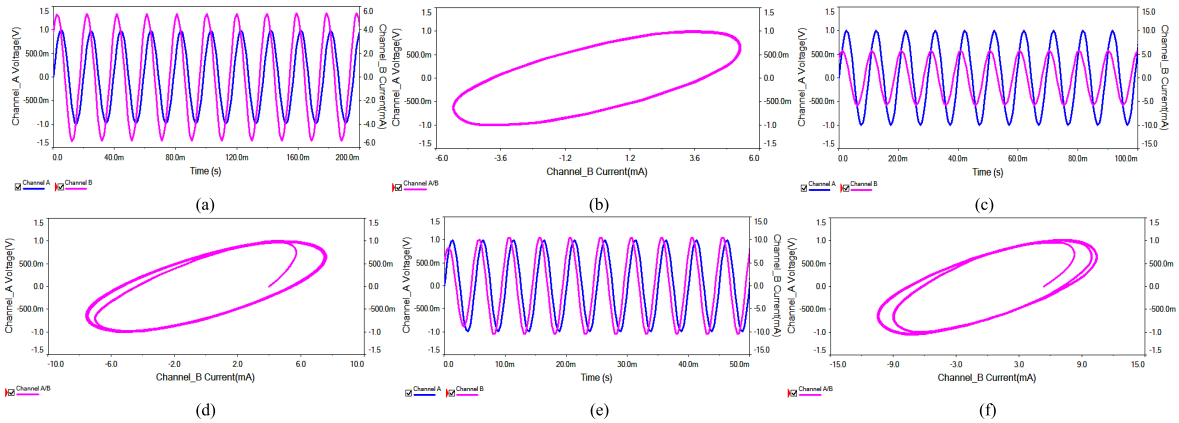


Fig. 15. Electrical characteristics of actual analog series circuits of a 1/2-order compensatory high-pass filtering capacitive lattice scaling fracmemristor: (a) V_i-t curve when $a = 50Hz$; (b) V_i-I_i curve when $a = 50Hz$; (c) V_i-I_i curve when $a = 100Hz$; (d) V_i-t curve when $a = 100Hz$; (e) V_i-I_i curve when $a = 200Hz$; (f) V_i-I_i curve when $a = 200Hz$.

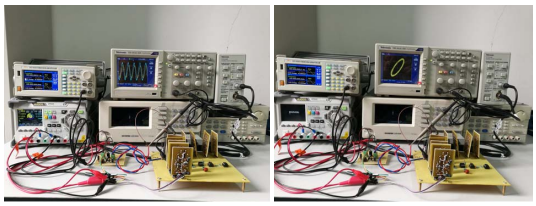
until circuits perform stably, the nonlinear twisted ellipse curves in Figs. 12(d) and 12(f) don't start from the point of $(0, 0)$. Thirdly, in comparison with an ideal 2/3-order capacitive fracmemristor, the approximation performance of the 2/3-order compensatory high-pass filtering capacitive lattice scaling fracmemristor is more precise and smoother than that of the corresponding 2/3-order high-pass filtering one. Therefore, the simulation results of Example 3 effectively verify the actual existence of a fracmemristor.

Example 4: For further analysis the electrical characteristics of an arbitrary-order capacitive fracmemristor, we should firstly achieve a versatile floating equivalent circuit of memristor achieved by a voltage-controlled linear resistor. A floating voltage-controlled linear resistor can be achieved by Junction Field Effect Transistor (JFET), as shown in Fig. 13.

In Fig. 13, A, B and C are the input port, the output port and the control voltage source input port of a floating voltage-controlled mirror linear resistor achieved by JFET, respectively. A_7, A_8 and A_{11} are three voltage followers, A_9 is a subtracter, A_{10} is a phase-identical adder, $V_C(t)$ is a control voltage source and I_D is the drain current of a JFET. Thus, according to the virtual short and virtual off electrical characteristics of an operational amplifier, we can derive that $V_7 = V_A$, $V_8 = V_B$, $V_D = V_A$, $V_S = V_B$, $V_9 = (V_A - V_B)/2$, $V_G = (V_A + V_B)/2 + V_B + V_C$, and $I_A = I_D = I_B$. Thus, $V_{GS} = (V_A - V_B)/2 + V_C = V_{DS}/2 + V_C$. Further, for a N-channel JFET, it should satisfy $V_{DS} > 0$. When $0 < V_{GS} < V_P$ and $|V_{DS} - V_{GS}| < V_P$, it works in variable resistance region (triode region), in which its drain-source current can be expressed as $I_D = \left\{2I_{DSS}\left[(V_{GS} - V_P)\, V_{DS} - V_{DS}^2/2\right]\right\}/V_P^2$, where I_{DSS} is the saturation current at zero gate-source voltage and V_P is the pinch-off voltage of a JFET. Then, we obtain:

$$\begin{aligned} R_{AB}(t) &= R_{DS}(t) = V_{DS}/I_{DS} \\ &= V_P^2/[2I_{DSS}(V_{GS} - V_P - V_{DS}/2)] \\ &= V_P^2/[2I_{DSS}(V_C - V_P)]. \end{aligned} \tag{34}$$

Equation (34) shows that a floating voltage-controlled linear resistor achieved by JFET in Fig. 13 is linearly controlled by $V_C(t)$. In theory, the control voltage source of a floating voltage-controlled linear resistor, $V_C(t)$, can be arbitrary in the variable resistance region of a JFET except for $V_C = V_P$. Note that with regard to a N-channel JFET, since $V_{DS} > 0$, $0 < V_{GS} < V_P$ and $|V_{GD}| = |V_{GS} - V_{DS}| < V_P$, from (34), V_A, V_B and V_C should satisfy $V_A > V_B$, $-(V_A - V_B)/2 < V_C < V_P - (V_A - V_B)/2$ and $|V_C - (V_A - V_B)/2| < V_P$. Note that since the control voltage source $V_C(t)$ is generated by an equivalent circuit of the memristor, the memristance $R[q(t)]$ of a floating voltage-controlled linear resistor achieved by JFET cannot be controlled by its input potential difference $(V_A - V_B)$. No matter what $(V_A - V_B)$, the memristance $R[q(t)]$ of a floating voltage-controlled linear resistor achieved by JFET is always controlled by $V_C(t)$. Thus, in this case, the floating voltage-controlled linear resistor achieved by JFET is actually a three-port mirror memristor.



(a) (b)

Fig. 16. Physical realization of a 1/2-order high-pass filtering capacitive lattice scaling fracmemristor: (a) V_i-t curve; (b) V_i-I_i curve.

Further, using the aforementioned floating voltage-controlled linear resistor, we can achieve a versatile floating equivalent circuit of memristor. Then, $R_{AB}(t) = R[q(t)]$. Without loss of generality, let's choose a control voltage source $V_C(t)$ achieved by operational amplifier and multiplier, as shown in Fig. 14.

In Fig. 14, E are the input port of a control voltage source. The port C in Fig. 14 is identical with the port C in Fig. 12. A_{12} is a phase-reversing integrator and A_{13} is a phase-reversing proportioner. g_M is the multiplier gain of a multiplier. Thus, we have:

$$V_C(t) = -g_M\left[-1/(rc)\int V_E(t)\,dt\right]^2 u(t). \tag{35}$$

To further analyze the electrical characteristics of the fractional-order capacitive fracmemristor, let's construct a 1/2-order compensatory high-pass filtering capacitive lattice scaling fracmemristor. In (25), let's set $\alpha = 2$ and $\beta = 2$. Then, we obtain $\upsilon = 1/2$. In (34), let's set $V_E(t) = \sin(at)\,u(t)$, $g_M = 1$, $r = 1\Omega$ and $c = 100\mu$F. Thus, from Fig. 6, Fig. 13 and Fig.15, using Multisim13, we can simulate

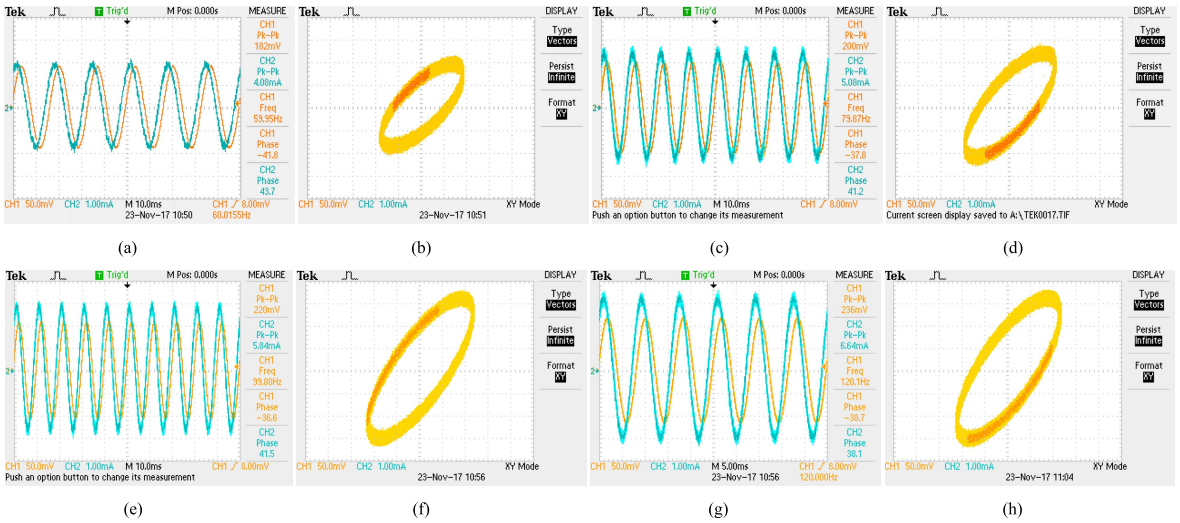


Fig. 17. Actual electrical characteristics of physical realization of a 1/2-order high-pass filtering capacitive lattice scaling fracmemristor: (a) V_i-t curve when $a = 60Hz$; (b) V_i-I_i curve when $a = 60Hz$; (c) V_i-I_i curve when $a = 80Hz$; (d) V_i-t curve when $a = 80Hz$; (e) V_i-I_i curve when $a = 100Hz$; (f) V_i-t curve when $a = 100Hz$; (g) V_i-I_i curve when $a = 80Hz$; (h) V_i-t curve when $a = 80Hz$.

the actual analog series circuits of a 1/2-order compensatory high-pass filtering capacitive lattice scaling fracmemristor, whose electrical characteristics can be shown in Fig. 15.

In Figs. 15(a), 15(c) and 15(e), Channel_A is the input voltage $[V_I(t) - V_O(t)]$ and Channel_B is the input current $I_{in}(t)$ in Fig. 6. In Figs. 15(b), 15(d) and 15(f), Channel_B is the input current $I_{in}(t)$ and Channel_A is the input voltage $[V_I(t) - V_O(t)]$ in Fig. 6. Example 4 shows that at first, the responses of a 1/2-order capacitive fracmemristor are nonlinearly periodic which vary with different driving frequency. From Fig. 1 and Fig. 6, we can see that a 1/2-order compensatory high-pass filtering capacitive lattice scaling fracmemristor can be considered in a certain way as a nonlinear interpolation of the memristor and capacitor. Equation (7) shows that the υ-order capacitive fracmemristor implements the convolution of $L^{-1}\left\{[r(q)]^{1-p}\right\}$ and $D_t^{-\upsilon} I_i(t)$. Thus, in Figs. 15(a), 15(c) and 15(e), the time variations of the voltage across a 1/2-order capacitive fracmemristor depend on the convolution of its input current history and its fractional calculus. Further, according to the theory of fractional calculus, the fractional integral of the input current across a 1/2-order compensatory capacitive fracmemristor, $D_t^{-1/2} I_i(t)$, suppresses its high frequency singular noise. From (5) and (7), we can see that the electrical characteristics of a capacitive fractor provide a physical mechanism of the fractional-order smoothness, which enables a capacitive fracmemristor to protect its memory states under the influence of noise. Secondly, the V_i-t curves and V_i-I_i curves of an actual 1/2-order capacitive fracmemristor accord with those of a theoretical ideal one. Comparing with Fig. 8(d) and Figs. 15(d) and 15(f), we can see that with regard to a 1/2-order compensatory capacitive fracmemristor, there should be a nonlinear twisted ellipse curve in the V_i-I_i plane, which start from the point of $(0, 0)$. Note that since we let Multisim13 doesn't begin to illustrate until circuits perform stably, the nonlinear twisted ellipse curves in Figs. 15(b), 15(d) and 15(f) don't start from the point of $(0, 0)$. Therefore, the simulation results of Example 4 effectively verify the actual existence of a fracmemristor.

Example 5: For further discussion, from Fig. 6, Fig. 13 and Fig.15, keeping the parameter settings of Example 4 unchanged, let's use Tektronix oscilloscope TDS 1012C-EDU to demonstrate, the physical realization of a 1/2-order high-pass filtering capacitive lattice scaling fracmemristor can be achieved, as shown in Fig. 16.

Therefore, from Fig. 16, the actual characteristics of the physical realization of a 1/2-order high-pass filtering capacitive lattice scaling fracmemristor can be tested, as shown in Fig. 17.

Note that to obtain the enough number of points of the experimental results in Fig. 17, let's set the time persist of display to be infinite. Comparing Fig. 17 with Fig. 15, we can see that the actual characteristics of the physical realization of a 1/2-order high-pass filtering capacitive lattice scaling fracmemristor perfectly consistent with those of its theoretical results. These physical realization experimental results of Example 5 also effectively verify the actual existence of a fracmemristor.

V. Conclusions and Discussion

From aforementioned mathematical derivation, experimental and analysis, we can observe that at first, the proposed arbitrary-order lattice scaling fracmemristor is a feasible hardware achievement of an arbitrary-order memristor. In addition, there should be some other type arbitrary-order scaling fracmemristors in their natural implementations, such as an arbitrary-order tree type scaling fracmemristor, arbitrary-order two-circuit type scaling fracmemristor, arbitrary-order H type scaling fracmemristor [44], [45], and so on. Secondly, the electrical characteristics of an arbitrary-order fracmemristor depend on the convolution of its input current history and its fractional calculus. Thus, a capacitive fracmemristor and inductive fracmemristor can be considered in a certain way as a nonlinear interpolation of the memristor and capacitor and that of the memristor and inductor, respectively. Thus, the fingerprints of an arbitrary-order fracmemristor is different from that of a memristor. Thirdly, from the mathematical analysis of the relationship between the memristance and transmission function of a memristor, $R[q(t)]$ and $H[q(t)]$, in (2), we can further see that since authors' clerical mistake, the reactance of a memristor $r[q(s)]$ is the Laplace transform of $H[q(t)]$ rather than that of $R[q(t)]$ in literature [55]. However, when $r[q(s)]$ is considered as the Laplace transform

of $H\left[q(t)\right]$ in (5) and (6), the generic fractional-order driving-point impedance functions of an arbitrary-order capacitive fracmemristor and inductive fracmemristor in their natural implementations derived in [55] are still correct. Fourthly, from the physical analysis of real causal circuits and systems in Example 2, although there is a convolution in (7) in pure mathematics, the time duration of $V_i\left(t\right)$ across a fracmemristor should be equal to the time duration of $I_i\left(t\right)$. Thus, since the insufficient understanding of authors' preliminary research, the prediction characteristics of a fracmemristor concluded in [55] are non-existent.

Fracmemristor extends the concepts of the classical memristor. Until recently, the applications of fracmemristor were mainly in the domain of physics and mathematics [46]–[55]. With respect to the state-of-the-art analog circuit implementation and application of the fracmemristor, there are many other fascinating issues else need to be further studied. For instance, at first, there should be some other circuit configurations of an arbitrary-order fracmemristors, as well as the fracmemristor based adaptive intelligence and learning systems, neural networks and weighted feedback systems, spiking-timing-dependent plasticity experimentation, chaotic systems, etc. Secondly, rules for series and parallel connections of two fracmemristors are more profound than those of two memristors [68], [69]. From (5) and (6), we can see that the fracmemristance nonlinearly changes with the instantaneous value of the reactance of the memristor contained in each fracmemristor. Further, the fractional-order of each fracmemristor could be also different. Thus, when two fracmemristors are connected in series or parallel, the electrical characteristics of the composite circuit of fracmemristor are quite complicated, which extremely depend on the fractional-order, circuit parameters, the frequency and amplitude of the input voltage or input current of a fracmemristor. Thirdly, the circuit design of the fracmemristor is also more complex than that of the memristor [62], [70]. From Fig. 2, we can observe that a υ-order capacitive lattice scaling fracmemristor is a floating two-port circuit element, which can be feasibly embedded in a fracmemristive circuit. In a similar way to the memristive circuit [62], we can deal with frequency-domain model of the fracmemristor, and achieve its steady-state analysis by means of the harmonic-balance method [62]. Since the fractional-order of a fracmemristive filter can be chosen arbitrarily, the fractional adaptive multi-scale filtering capability of a fracmemristor based filter is a major advantage that is superior to the conventional memristive filters and LTI filters. It will be further discussed in detail in our future work.

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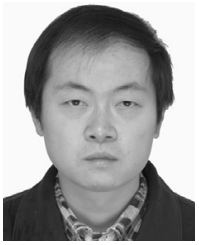
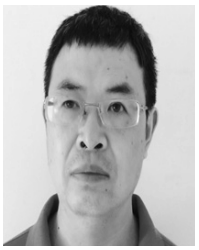


Yi-Fei Pu received the Ph.D. degree from the College of Electronics and Information Engineering, Sichuan University, in 2006.

He is currently a Full Professor and the Doctoral Supervisor with the College of Computer Science, Sichuan University, and the Chief Technology Officer with Chengdu PU Chip Science and Technology Co., Ltd. He is elected into the Thousand Talents Program of Sichuan Province as the Academic and Technical Leader of Sichuan Province. He focuses on the application of fractional calculus and fractional partial differential equation to signal analysis, signal processing, image processing, circuits and systems, and machine intelligence. He has authored with the first author's identity about 20 papers indexed by SCI in journals such as the *International Journal of Neural Systems*, the IEEE TRANSACTIONS ON IMAGE PROCESSING, the IEEE TRANSACTIONS ON NEURAL NETWORKS AND LEARNING SYSTEMS, the IEEE ACCESS, *Mathematical Methods in the Applied Sciences*, *Science in China Series F: Information Sciences*, and *Science China Information Sciences*. He holds 13 China inventive patents, as the first or single inventor. He held positions in several research projects, such as the National Nature Science Foundation of China and the Returned Overseas Chinese Scholars Project of Education Ministry of China.



Xiao Yuan received the Ph.D. degree from the School of Electronic Engineering, University of Electronic Science and Technology of China, in 1998.

He is currently an Associate Professor with the College of Electronics and Information Engineering, Sichuan University. He has authored over 40 papers which are indexed by SCI, EI or ISTP, and two books which for fractional calculus. He recently focuses on the mathematical principles of physical realization for fractional operator elements, digital implementation of fractional-order systems, fundamental theory of fractional-order circuits and systems, fractal systems and fractional-order processes and phenomena, fractional-order signal analysis and processing, theory and applications of fractional differential equations, and fractional calculus view of complexity.

Bo Yu is currently pursuing the Ph.D. degree with the College of Computer Science, Sichuan University.

He is currently a Lecturer with the College of Physics and Engineering, Chengdu Normal University. He focuses on the application of fractional circuits and systems.