Report for lab6(1 day late token)

In this lab, we need to implement conditional branches (cbz), unconditional branches (b) in the ID stage and Flush function.

The compilation order:

1. IMEM outputs the instructions corresponding to the address according to the address sent by the PC. Whether to write this instruction depends on whether a hazard is detected.

2. The IFID register transfers instructions to CPUcontrol, Hazard detector, register, and IDEX register. The address of the operation register and destination register is given to the IDEX register for subsequent forward comparison. If flush is detected, the PC address and instructions are all cleared.

3. IDEX transmits the data of the corresponding register to two multiplexers, and then selects the data input to ALU according to the signal given by forwarding. If the address of the register is the same as ALUresult, the result will be returned as the input of ALU.

4. Then store the data in the corresponding memory address, and transfer the data to be written back to the MEMWB register, and then write it back to the corresponding register.

I want to illustrate the correctness of the experiment through the following table.

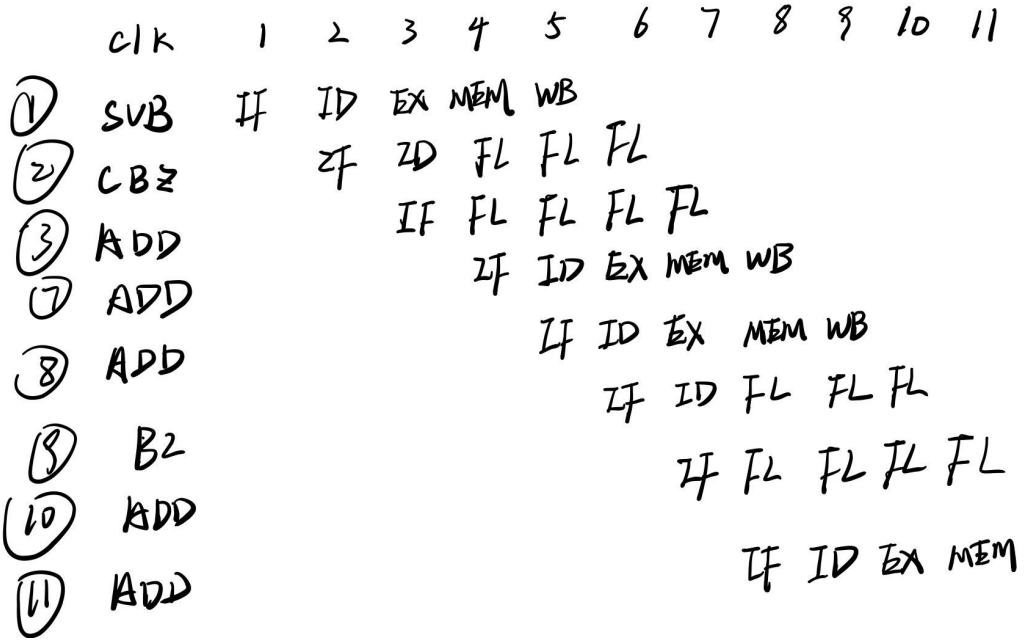

Figure 1.1 Instructions Stage Form

In the above figure, FL means flush.

It can be seen from Figure 1.1 that before the result of the first instruction is written back to the register, the conditional branch judgment is performed.

At this time, the value in X23 register is 0, so the jump instruction should be executed. Therefore, after taking the next instruction, the flush operation is directly executed.

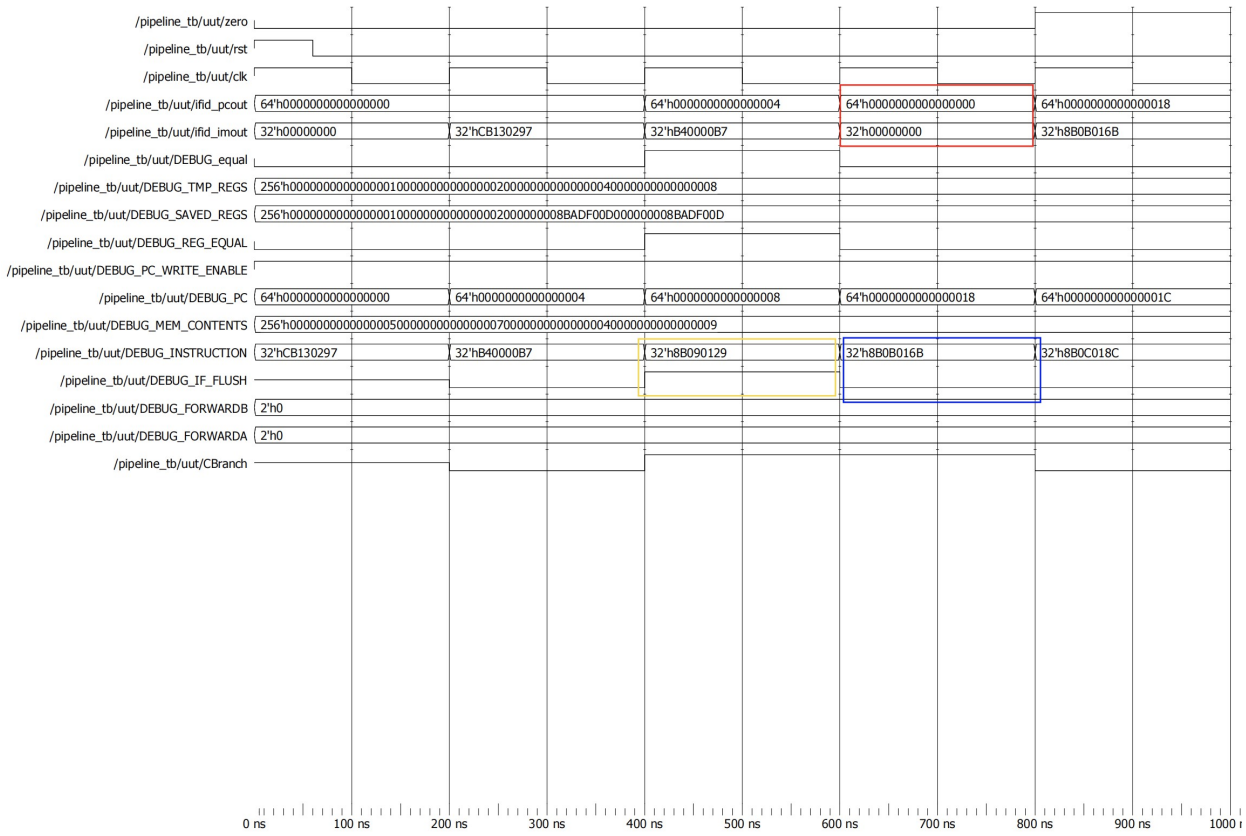

Figure 1.2 CBZ

In the third cycle where the yellow box is located, although the third instruction is read, it is not executed. At this time, the flush signal is 1, and the flush operation is executed.

The red box represents the fourth cycle. Because flush is 1, the PC output signal and the command output signal are both 0.

And the next instruction in the blue rectangle is the instruction to be read after the jump (ADD X11, X11, X11).

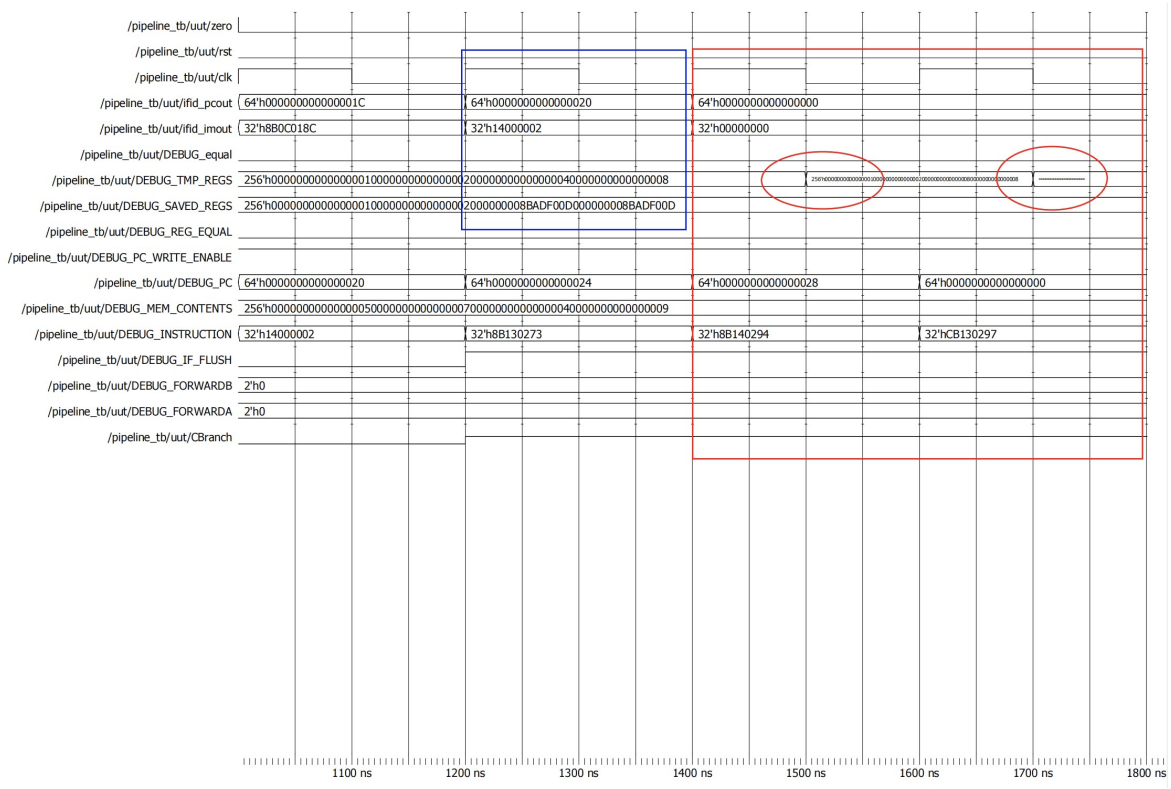

Figure 1.3 FLUSH

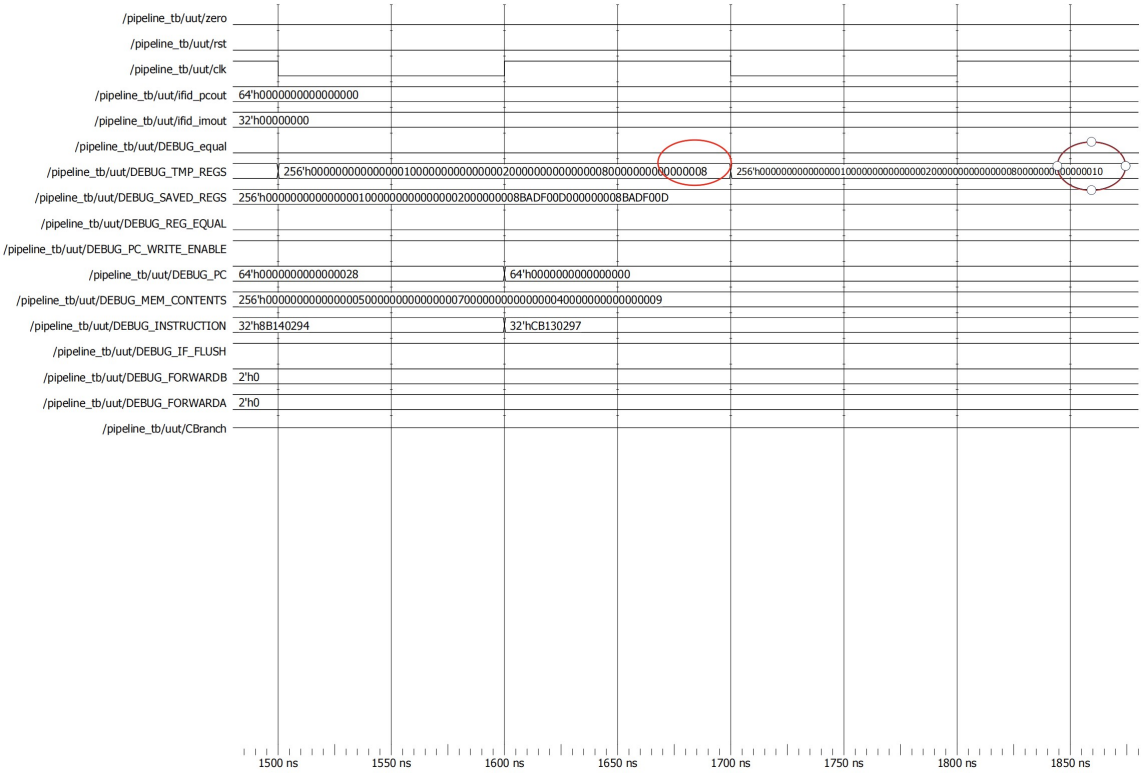

Figure 1.4 value of registers

The blue box is the waveform of the seventh cycle. It can be seen that the value in the register has not changed, which proves that the third instruction has not been executed, but has been flushed.

The red boxes are the 8th and 9th cycles. The value of the register has changed, which corresponds to the WB stages of the 8th and 9th cycles in Figure 1.1.

And as can be seen in Figure 1.4, after the instruction is successfully executed, the value of the register becomes 8 and 16.