Report for lab2 assignment(used 1 day late token)

1. Waveform with brief description for some entities.

(1) ALU：From figure 1.1, We can see that the four parts implement ‘and’, ‘or’, ‘add’ and ‘subtraction’ respectively. And when the addition operation is executed, a overflow signal 1 is generated. When the subtraction operation is executed, the zero output signal is 1.

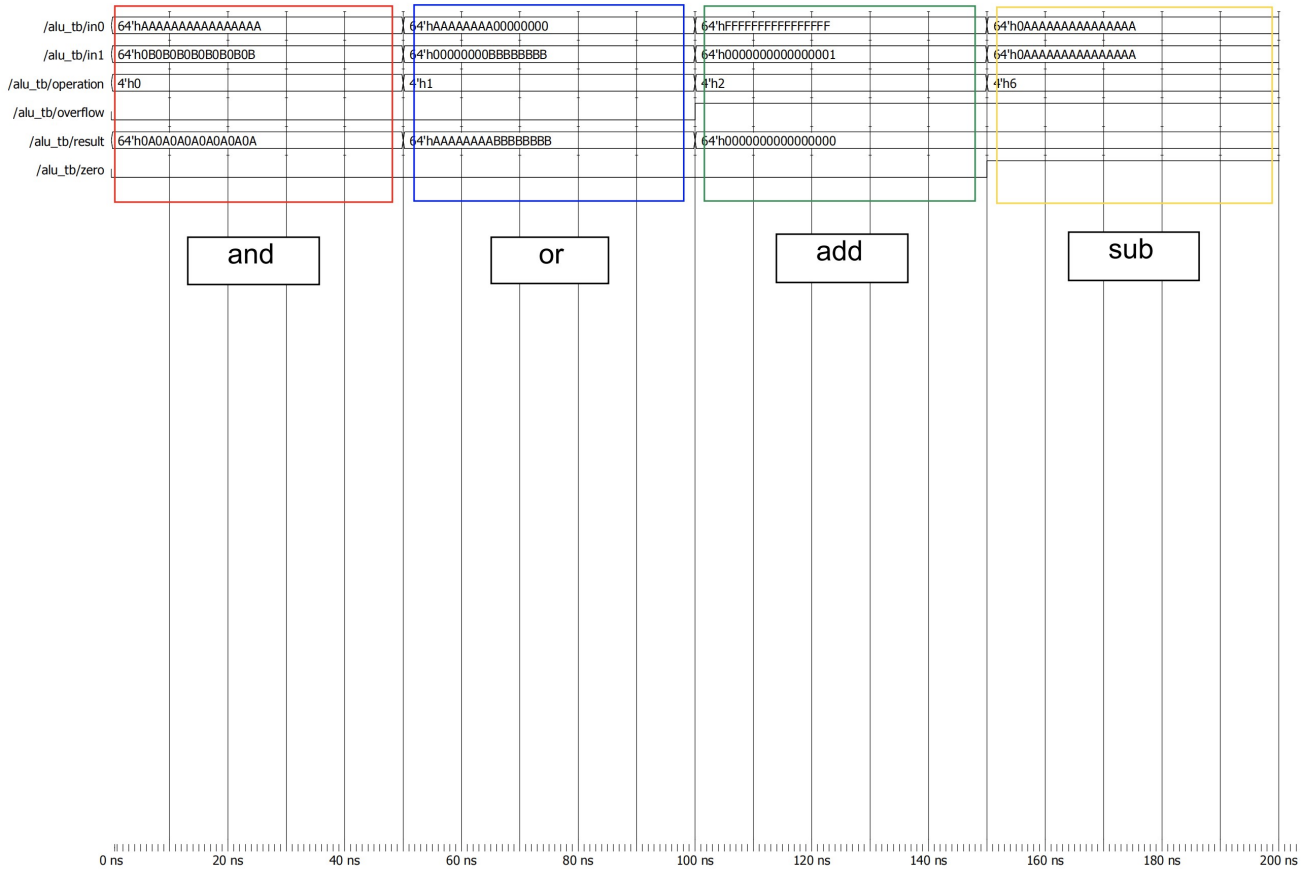

Figure 1.1 Wave of ALU testbench

(2) Registers: From figure 1.2, we can see that the three signals are successfully written at the falling edge and the writing signal is 1. In the red rectangle, it’s register X10, at first the address is x0000000000000001, then the signal xFFFFFFFF00000000 was successfully written in, and we also read the right signal. The rest two parts blue rectangle and green rectangle also implemented The corresponding write and read operations.

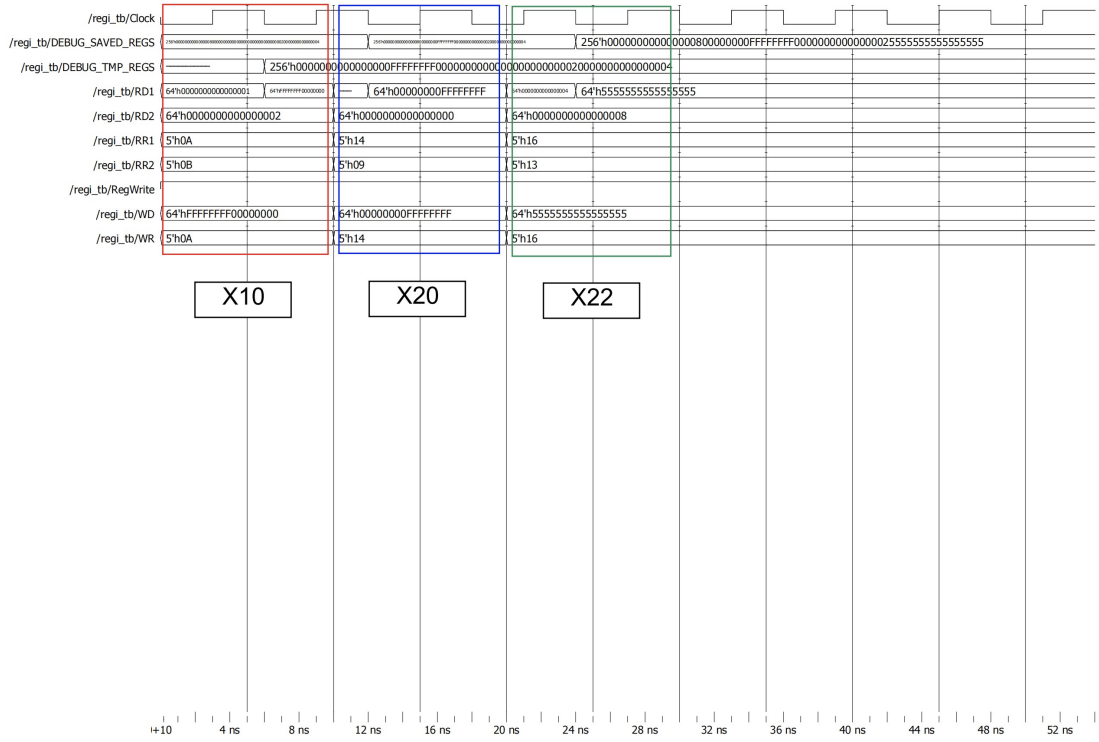

Figure 1.2 Wave of registers testbench

(3) IMEM: Receive the instruction address from the PC, and then match the corresponding instruction. Similar to the above components, first convert the 64 bit address into an integer, that is, decimal, and then find the first byte corresponding to the instruction according to the decimal number, and then output four byte 32-bit instructions. I set two 4-byte instructions, the first instruction from iemeBytes(11) -> iemeBytes(14), the second one from iemeBytes(16) -> (19). We can see that the address successfully matches the corresponding instruction.

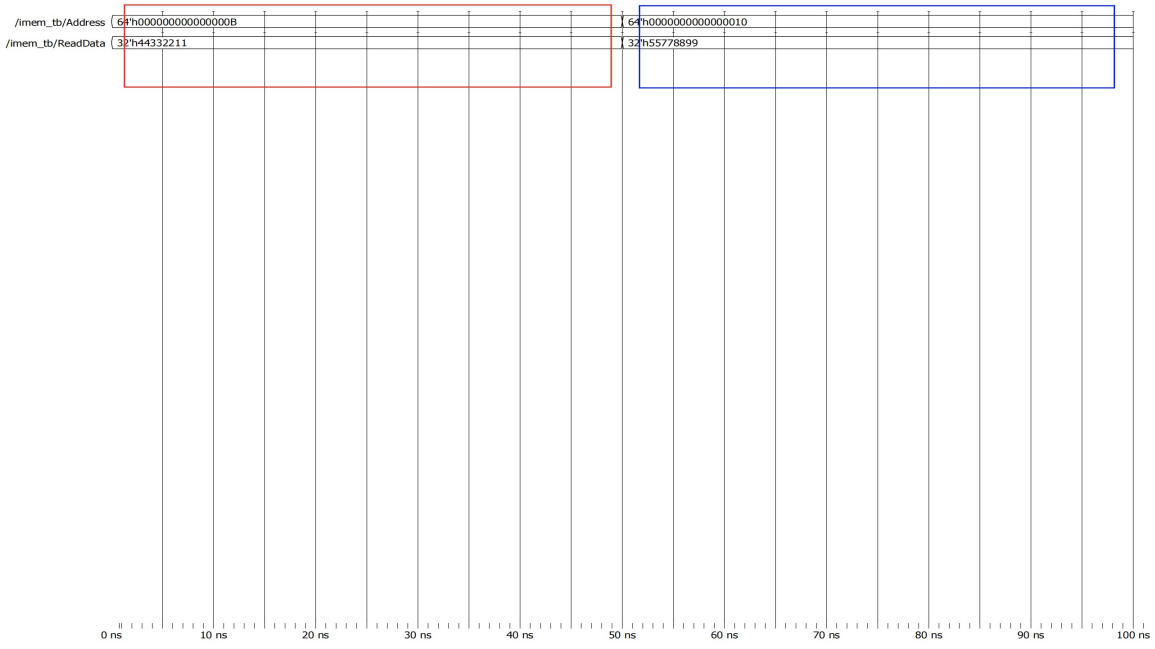

Figure 1.3 Wave of IMEM testbench

(4) DMEM: This is a 1kb data storage, from figure 1.4, when MemWrite = 1 and MemRead = 0, those two data “FFFFFFFF00000000” and “00000000FFFFFFFF” are successfully written at the rising edge, and read successfully when MemWrite = 0 and MemRead = 1;

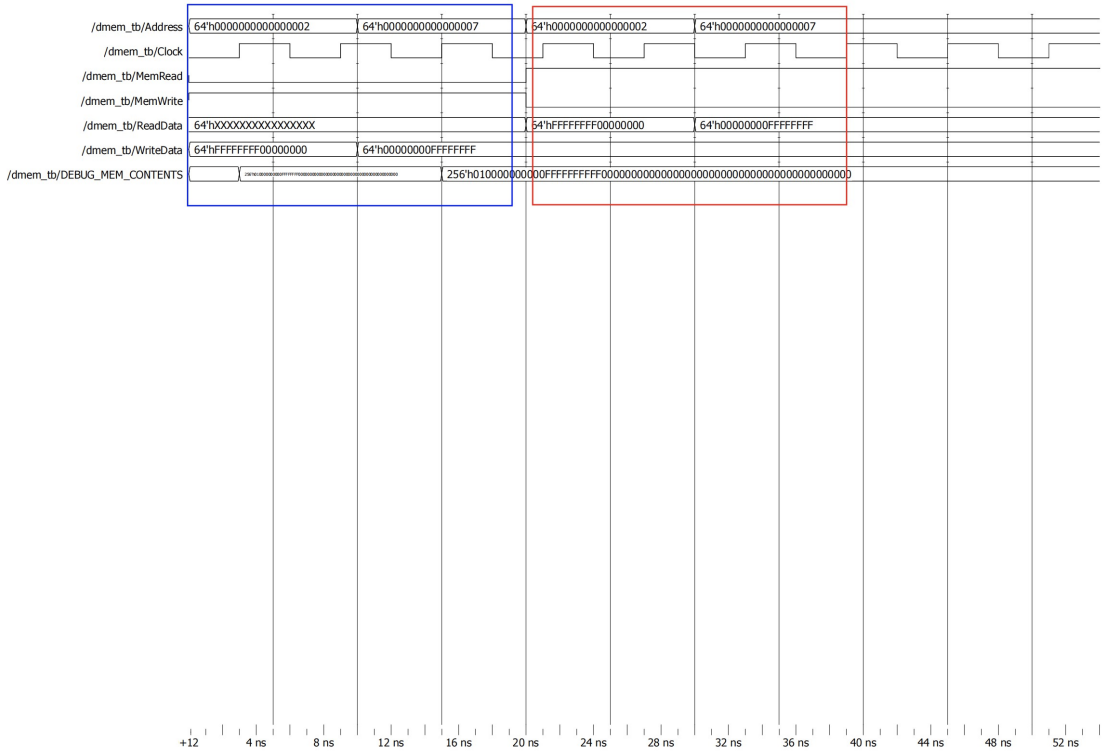

Figure 1.4 Wave of DMEM testbench