Report for lab 4

Compared with lab3, this lab has four more registers, which are used to form the pipeline cpu.

Compilation order of the processor:
1. IMEM outputs the instructions corresponding to the address according to the address sent by the PC, and then stores them in the IFID register together with the address, which is the first stage.
2. IMEM outputs the instructions corresponding to the address according to the address sent by the PC, and then stores them in the IFID register together with the address, which is the first stage.
3. At this time, in addition to the data in register 2 being directly transmitted to the EXMEM register by IDEX, the signals received by EXMEM also include the address calculated by the adder and the result of logical operation performed by ALU. ALU is controlled by ALUControl that receives the OPcode signal given by IDEX for logical operation
4. ALU is controlled by ALUControl that receives the OPcode signal given by IDEX for logical operation
5. EXMEM gives another PC address to be selected, and the AND gate composed of its output CBrank signal and ALU zero signal outputs the selection signal of PC address. The DMEM also receives the ALUresult from the EXMEM and the RD2 value to be written to the memory.

Waveforms:

In this lab, there are two data hazards, one after the second instruction and the other after the fifth instruction. Now, I will use the waveform to explain:

1. In Figure 1.1, it can be seen that the register data is read correctly, the instruction is read correctly, and the DMEM data is also the data after initialization.

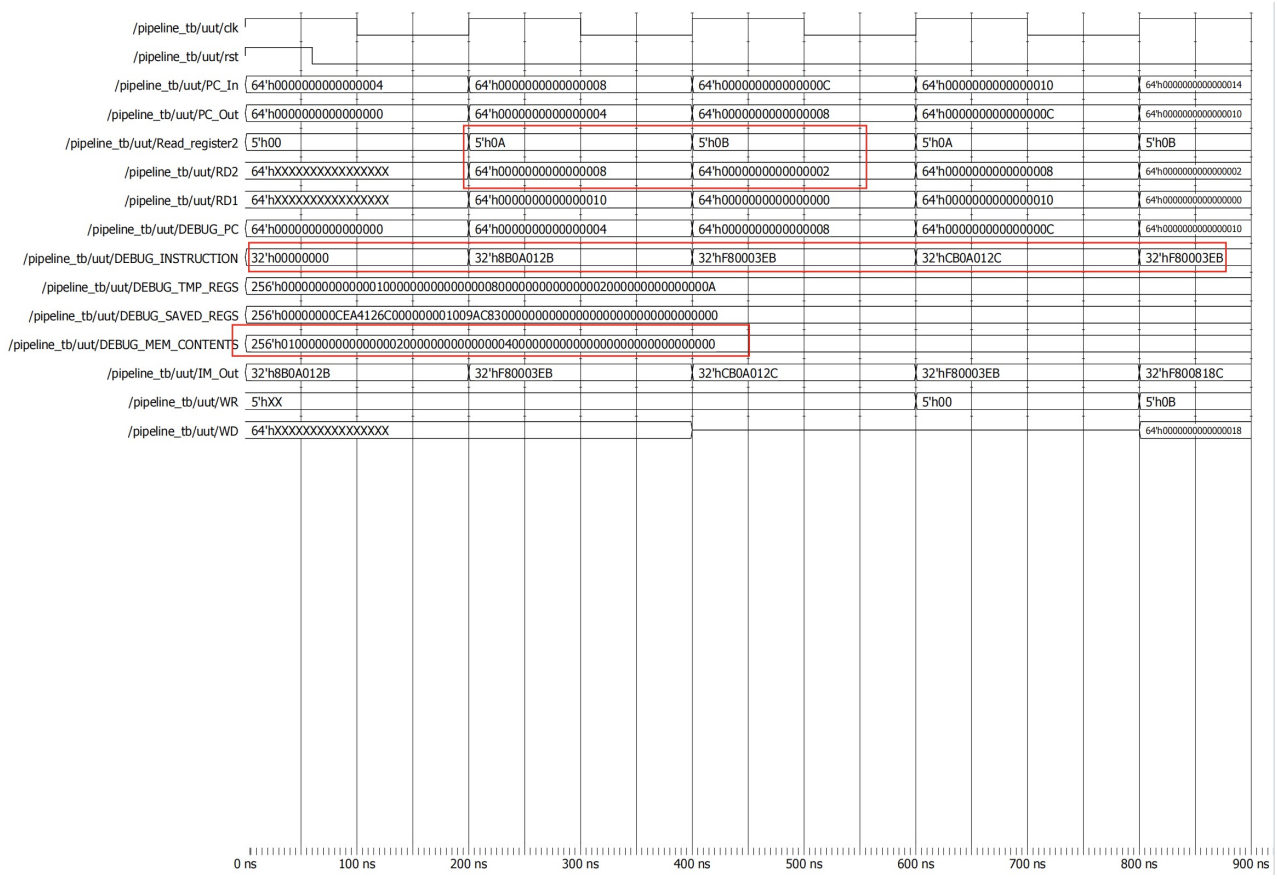

Figure 1.1 the first hazard 1

Since the pipeline processor executes an instruction within 5 clock cycles, the current instruction and the subsequent instructions are executed at each stage. It can be seen from Figure 1.2 that until the fifth clock cycle, the value of register X11 changes from 0x... 02 to 0x... 18 at the falling edge. When the STUR instruction is executed in the next clock cycle, an error occurs. Due to the data hazard, “18” was originally stored

in DMEM bit 0, but now “02” is stored, that is, the original data in the X11 register, the correct data “18” is stored after two clock cycles. That is, the correct data is stored only after the same STUR X11, XZR, 0 instructions are executed for the second time. This is the first data hazard.

Figure 1.2 the first hazard 2

2. After the fifth instruction is executed, the value of X12 should be stored in 16 bits of DMEM, that is, "08" is used instead of "04" but the initial value “0A” of X12 register is stored at 18 bits of DMEM. See Figure 2.1 for details:

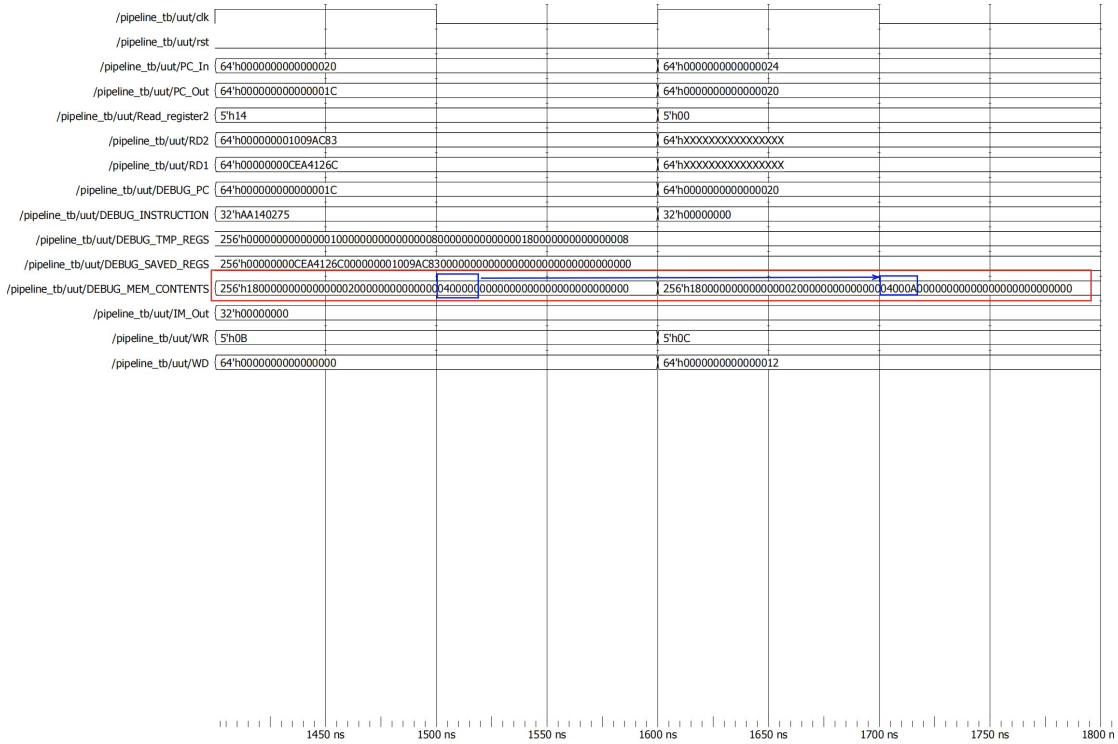

Figure 2.1 the second hazard 1

After executing the same sixth instruction, the correct X12 value "08" is obtained and stored in 16 bits of DMEM.

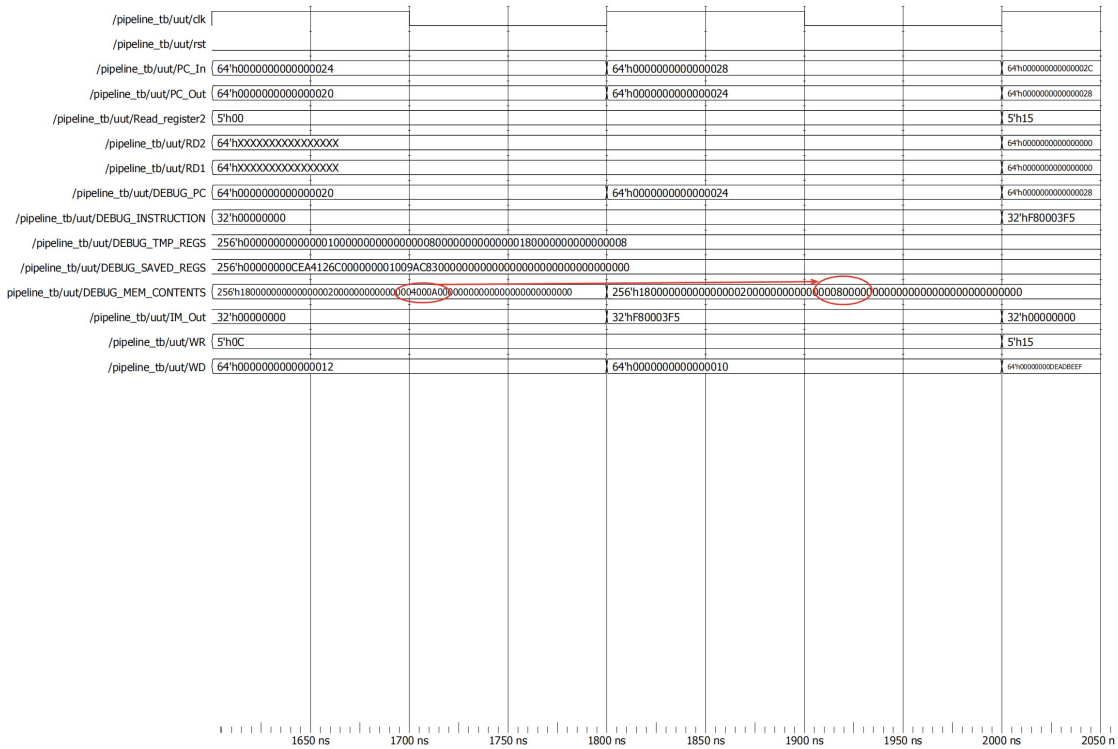

Figure2.2 the second hazard 2