

Report for lab3 assignment(use 1 day late token)

1. Waveform with brief description for the whole single cycle cpu.

Because of space, I deleted the write enable signal, which always has a value of 1.
Test program:

```
ADDI X9, X9, 1
ADD X10, X9, X11
STUR X10, [X11, 0]
LDUR X12, [X11, 0]
CBZ X9, 2
B 3
ADD X9, X10, X11
ADDI X9, X9, 1
ADD X21, X10, X9
```

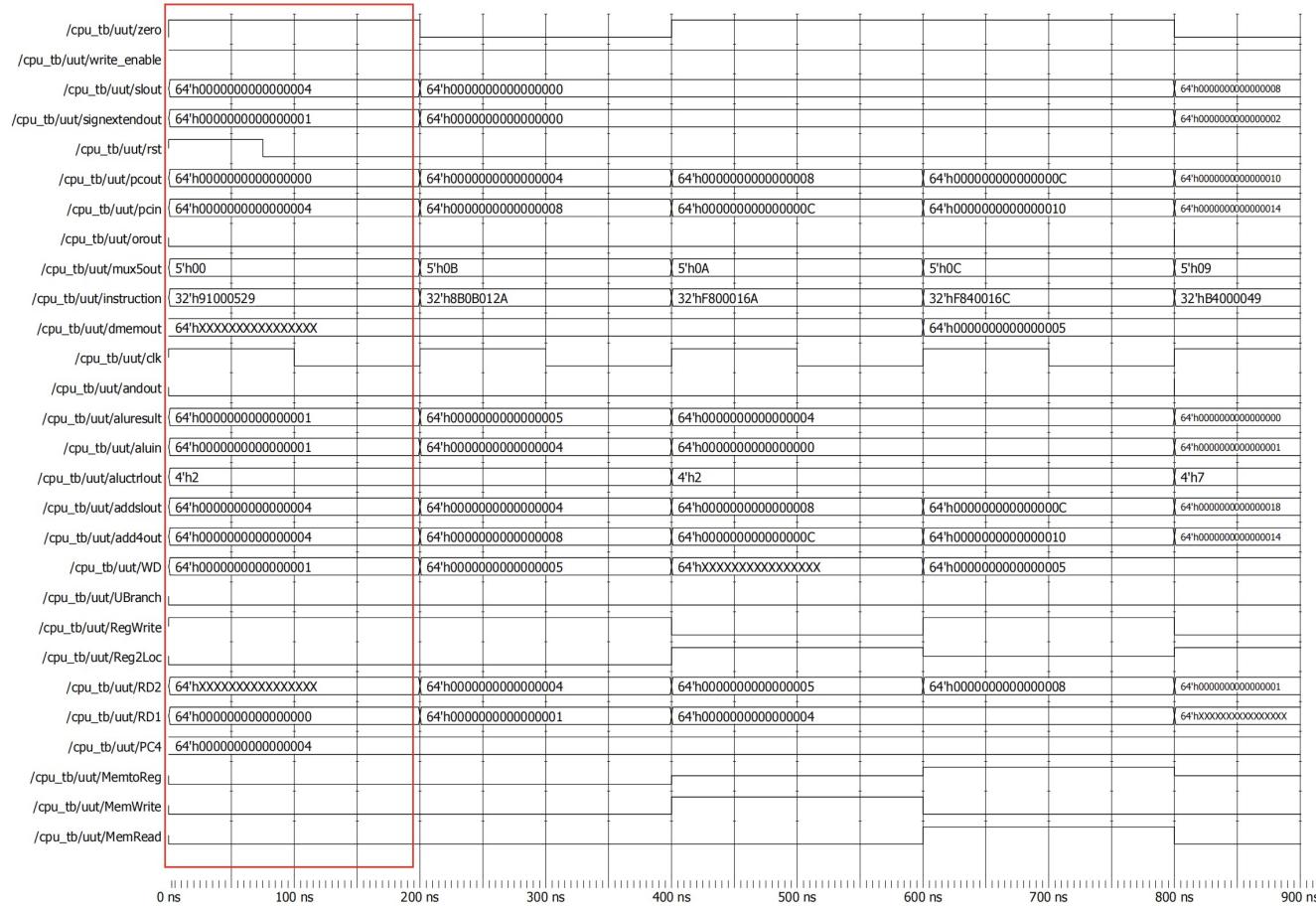
After executing the above instructions, the final value of X9 register should be 1. Because after judging that X9 is not equal to 0, the next instruction B 3 jumps to the last instruction directly, so the value of X9 remains unchanged as 1.

Answer the question: what value would be written to memory by the test program is X9 = -1?

4 should be writte to memory.

In Figure 1.1, Since the rst signal of the first half of the rectangle marked area is 1, the cpu is in the reset state and does not start executing instructions. When IMEM got PC address out 0x0, the instruction 32'h91000529 was sent to Registers, cpu control and sign-extend. Then ALU got RD1 and sign-extend signal : immediate '1' so it could eexecute addition. Finally, the DMEM sent the result back to Register, which controlled by

MemtoReg.



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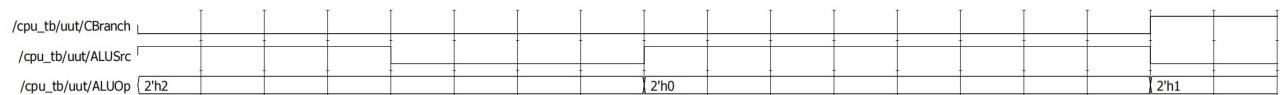
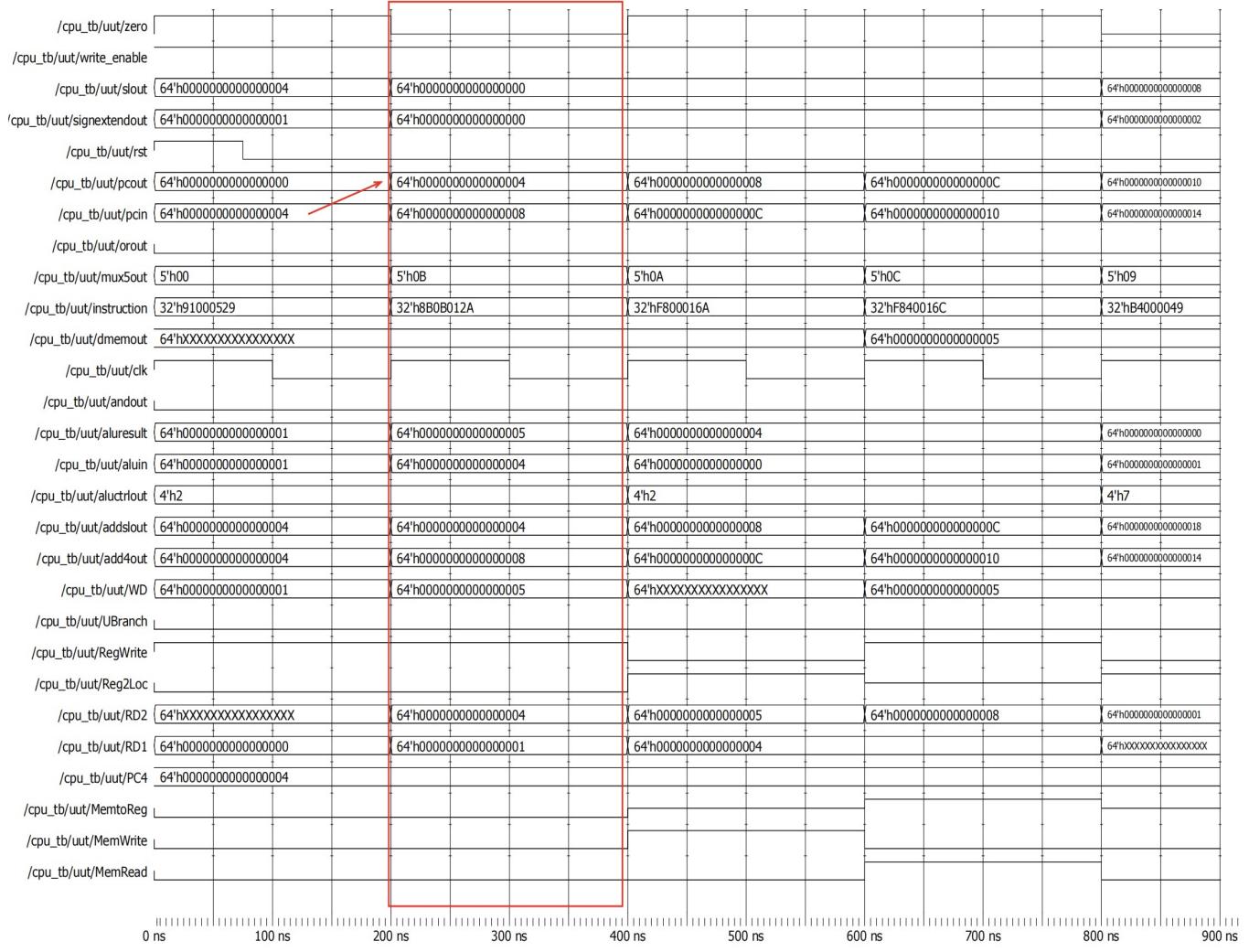


Figure 1.1 wave in first clock cycle

In Figure 1.2, we can see that the current PC address out is last clock cycle PC address in (due to the or-gate signal is 0, so the pc address in is PC + 4 after mux select in0). At this clock cycle, due to no immediate number, so the ALU executed the addition of two registers data (Since the ALUSrc is 1 in this cycle, so the mux selected in0). It means that the signextend signal didn't work, so it had to be 0x0.



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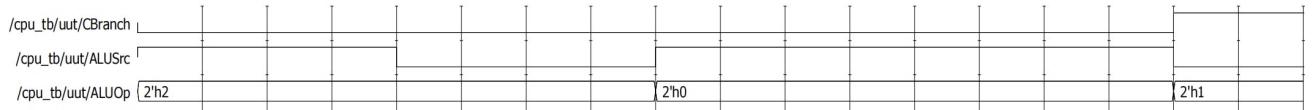
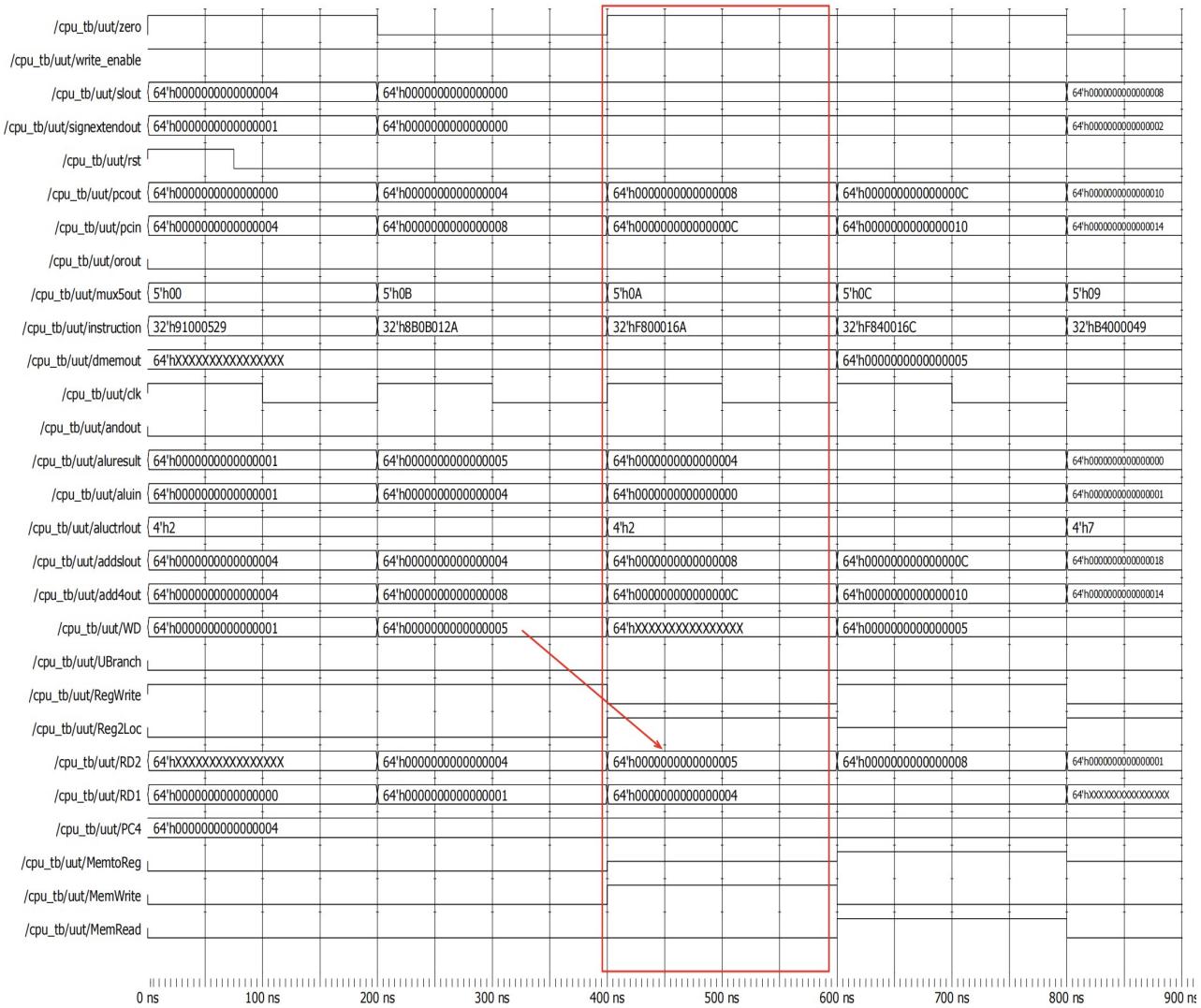


Figure 1.2 wave in second clock cycle

In Figure 1.3, the processor needs to execute STUR(store into memory) operation in this clock cycle, MemWrite is 1, so the value 5 of X10, would be saved.



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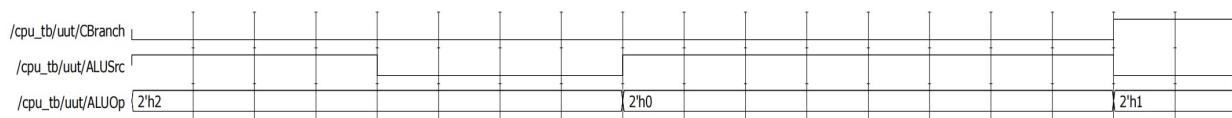


Figure 1.3 wave in third clock cycle

In the Figure 1.4, processor needs to execute load operation in this cycle, the value of MemRead and MemtoReg are 1, when IMEM got new address from pc address out, it gave LDUR instruction to registers, cpu control and sign-extend. Then DMEM received the expected address from ALU, found its data from that address and sent it back to the X12 register. The result is 0x5.

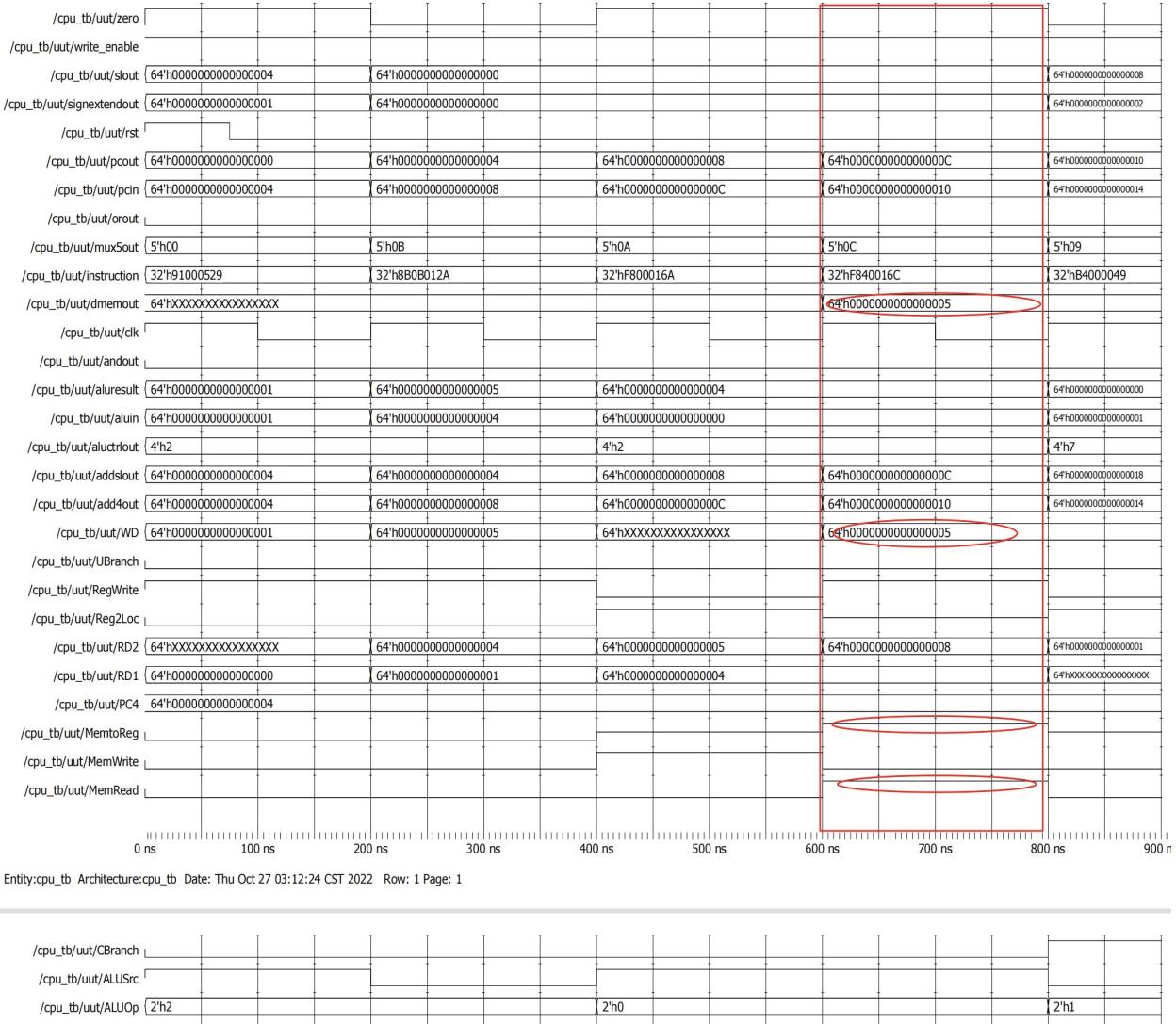
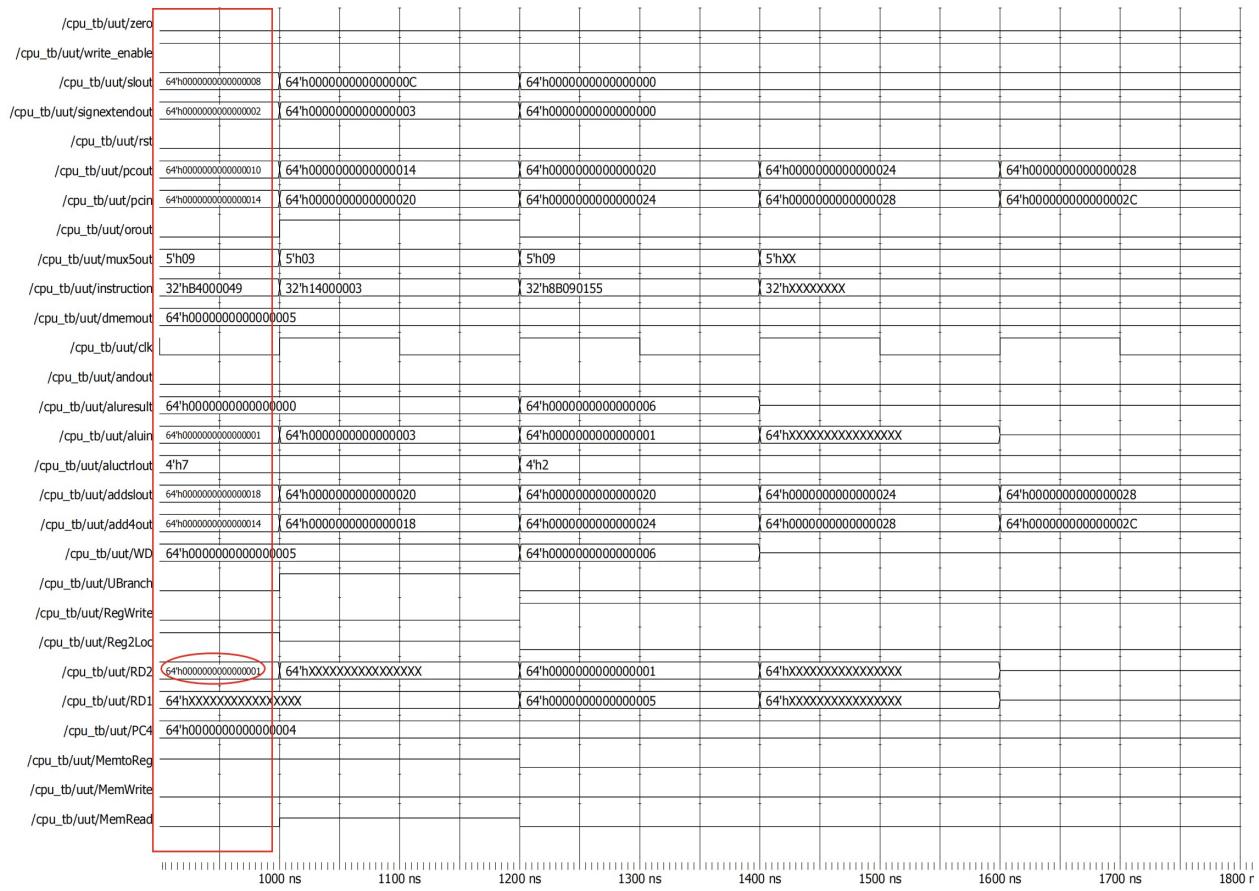


Figure 1.4 wave in 4th clock cycle

In Figure 1.5, the processor needs to execute conditional branch instruction, since the value of X9 is still 1 in red circle, executed the next instruction directly.

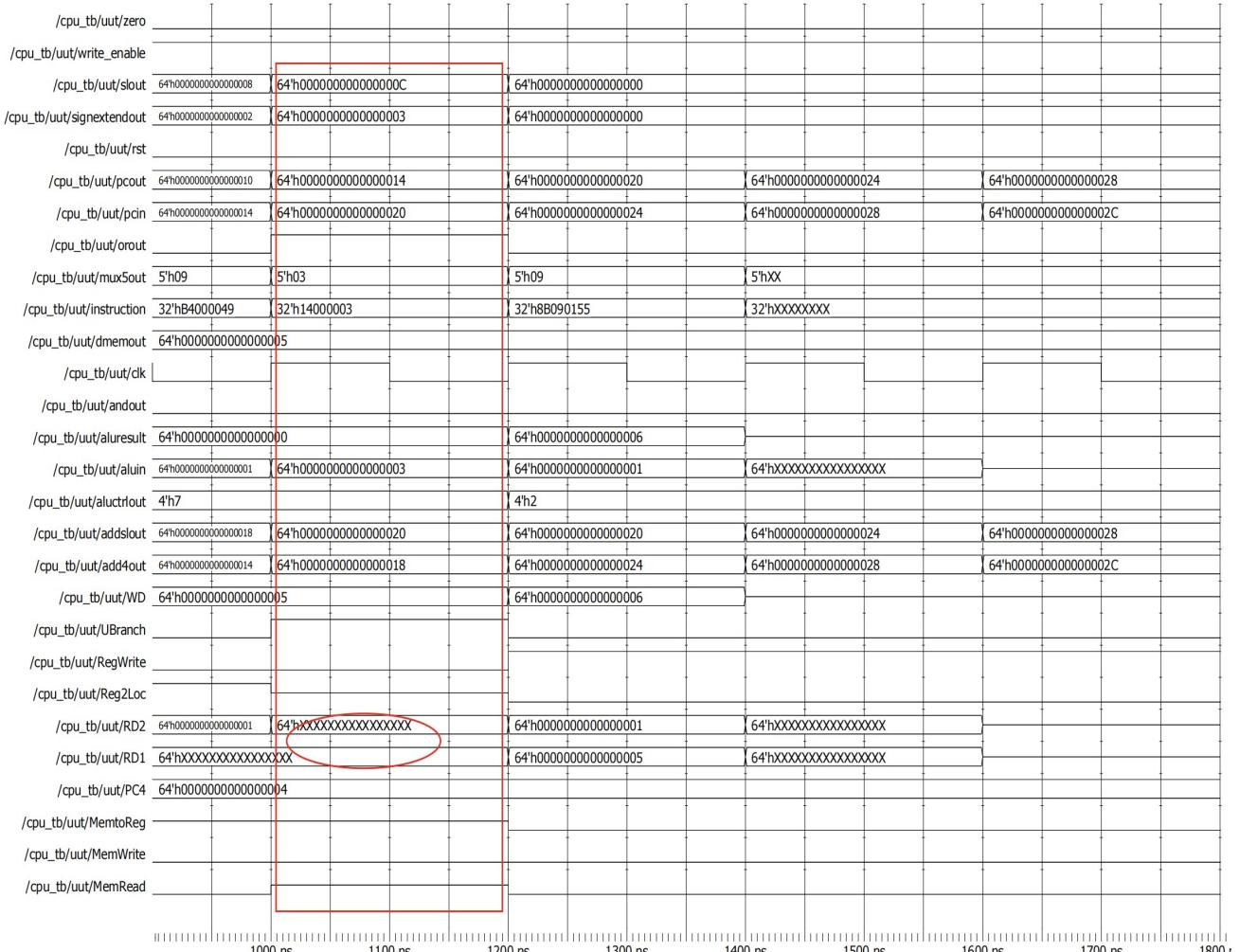


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Figure 1.5 wave in 5th clock cycle.

In Figure 1.6, processor need to execute a B type instruction B 3, it means there is no any other things happen. Just jumps to the third instruction after this instruction, that is, the last instruction. At this time, no data is read from the registers because mux5 out selected register 3, but we didn't set this register.



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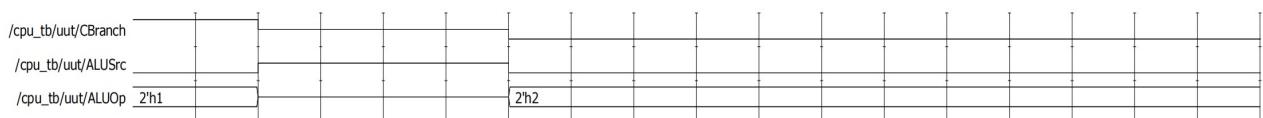
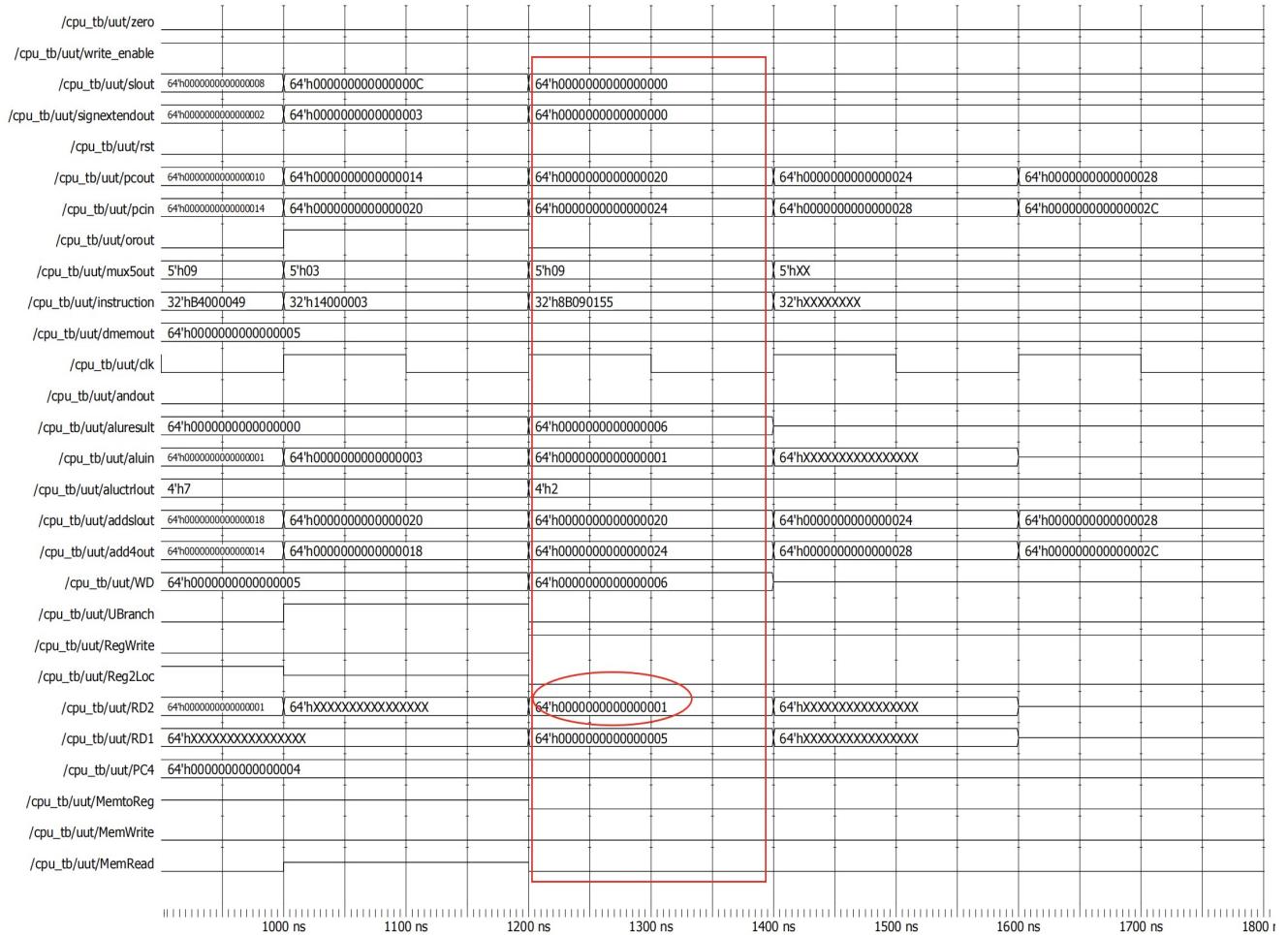


Figure 1.6 wave in 6th clock cycle

In Figure 1.7, this is the last instruction the processor need to process. Due to the direct jump from the previous instruction to the last instruction, the processor needs to add the data in two registers X10 and X9. It can be seen from the figure 1.7 that the processor did skip the two instructions in front of last instruction, so the value of register X9 does not change at this time, it is still 1.



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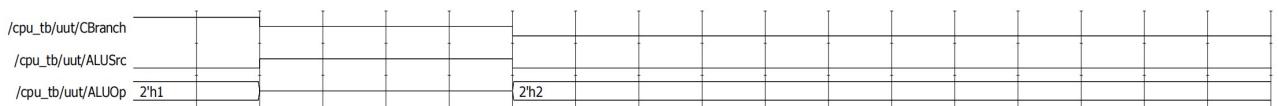


Figure 1.7 wave in 7th clock cycle