

TU, PU, PoU & KU

Revised and Updated

# Insights on **ELECTRONIC DEVICES & CIRCUITS**

THIRD EDITION

## Features

- A textbook with **INSTANT NOTES**
- Solution to large number of numericals including that of previous exams



## Authors

Er. Amit Kumar Rauniyar  
Er. Prem Chandra Roy

## Editors

Er. Rajan Lama  
Er. Kailash Khadka  
Er. Manish Mallick  
Er. Krishna Kumar Jha  
Er. Neha Karna

# CONTENTS

## Chapter: 1

### DIODES

1.1	The Ideal Diode	1
1.2	Terminal Characteristics of Junction Diodes	2
1.3	Physical Operation of Diodes	3
1.4	Analysis of Diode Circuits	5
1.5	Large Signal Model/Small Signal Model and its Application	8
1.6	Operation in the Reverse Breakdown Region - Zener Diode	17

## Chapter: 2

### BIPOLAR JUNCTION TRANSISTOR

2.1	Operation of npn-Transistor in Active Mode (Normal Mode)	45
2.2	Graphical Representation of Transistor Characteristics	46
2.3	Analysis of Transistor Circuits at DC	47
2.4	Transistor as an Amplifier	50
2.5	Small Signal Equivalent Circuit Models	53
2.6	Graphical Load Line Analysis	55
2.7	Biasing BJT for Discrete Circuit Design	57
2.8	Basic Single Stage BJT Amplifier Configurations (C-E, C-B, C-C)	68
2.9	Transistor as a Switch - Cutoff and Saturation	81
2.10	A General Large Signal Model for the BJT: The Ebers-Moll Model	85

## Chapter: 3

### FIELD- EFFECT TRANSISTOR

3.1	Structure and Physical Operation of Enhancement type MOSFET	111
3.2	Current Voltage Characteristics of E-MOSFET	115
3.3	The Depletion Type MOSFET	118
3.4	MOSFET Circuits at DC	120

# DIODES

## Introduction

The earlier course "Basic Electronics Engineering" has already covered some of the basic concepts of electronics. This chapter deals with two terminals non-linear device diode and focuses more on numerical problems.

A diode is an electronic device allowing current to move through it in one direction with far greater ease than in the other. The most common kind of diode in modern circuit design is the semiconductor diode, although other diode technologies exist. In this chapter, the prime concern is to study semiconductor diode and its important applications: rectification, clipping, clamping, switching etc.

### 1.1 The Ideal Diode

An ideal diode is a semiconductor device that produces no current when operated in reverse-biased mode and zero voltage drops when operated in forward-biased mode. Thus, a forward-biased diode acts a short circuit and reverse-biased diode acts as an open circuit.

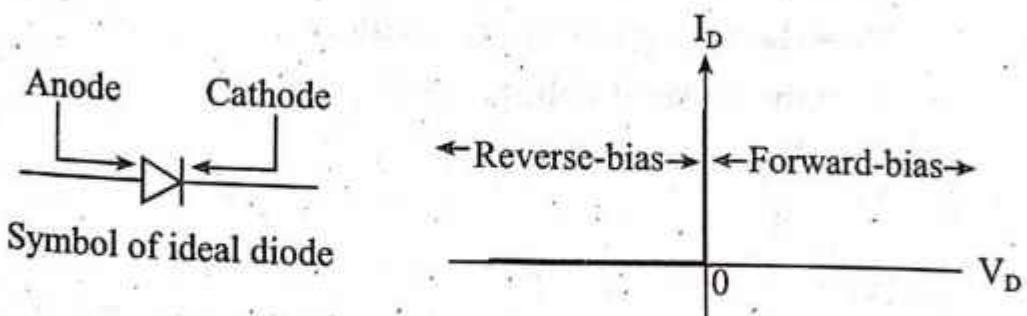


Figure: I - V characteristic curve of ideal diode

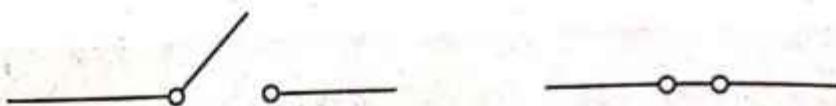
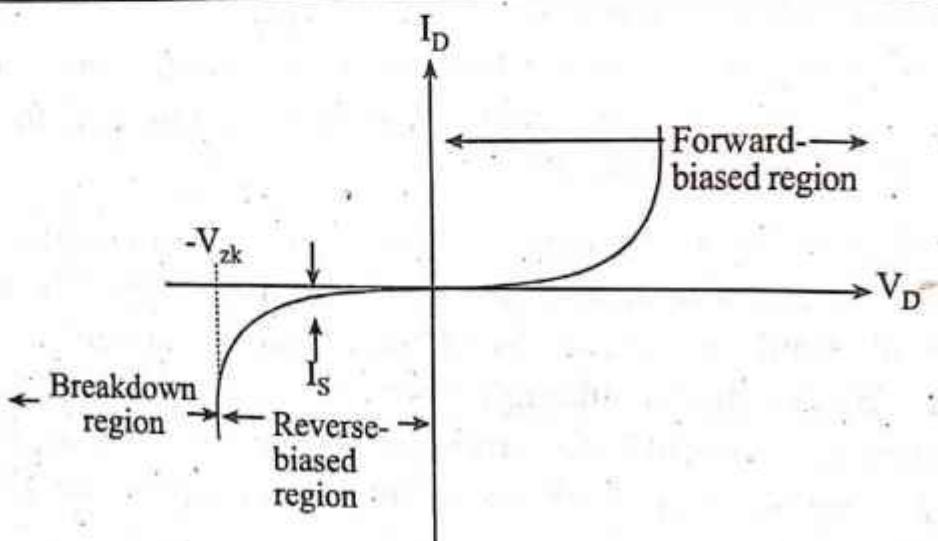


Figure: Equivalent circuit for reverse-biased ideal diode

Figure: Equivalent circuit for forward biased ideal diode

## 1.2 Terminal Characteristics of Junction Diodes



From Shockley's Diode Equation, we have,

$$I_D = I_S (e^{V_D/nV_T} - 1) \dots\dots\dots (i)$$

Where,

$I_D$  = the current flowing through diode

$I_S$  = the reverse saturation or scale current

$V_D$  = the voltage drop across diode

$V_T$  = the thermal voltage and is defined as

$$V_T = \frac{KT}{q}$$

Where,

$K$  = Boltzmann's constant =  $1.38 \times 10^{-23} \text{ JK}^{-1}$

$T$  = absolute temperature in Kelvin =  $273 + T^\circ\text{C}$

$q$  = magnitude of electronic charge =  $1.6 \times 10^{-19}\text{C}$

$\eta$  = the parameter whose value is in between 1 and 2 and depends upon the materials used and physical structure of diode.

The thermal voltage  $V_T$  has value of 25 mV at room temperature (i.e.  $T = 25^\circ\text{C}$ )

**Forward - bias (with  $V_D > 0$ ):**

We have,

$$I_D = I_S \left( e^{\frac{V_D}{\eta V_T}} - 1 \right)$$

$$\text{or, } I_{D1} \equiv I_S e^{\frac{V_{D1}}{\eta V_T}} \dots \dots \dots \text{(i)}$$

Also,

$$I_{D2} \equiv I_S e^{\frac{V_{D2}}{\eta V_T}} \dots \dots \text{(ii)}$$

Dividing equation (i) by (ii) we get,

$$\frac{I_{D2}}{I_{D1}} = e^{\frac{V_{D2}-V_{D1}}{\eta V_T}}$$

Taking natural log on both sides we get

$$\frac{V_{D2}-V_{D1}}{\eta V_T} = \ln \frac{I_{D2}}{I_{D1}}$$

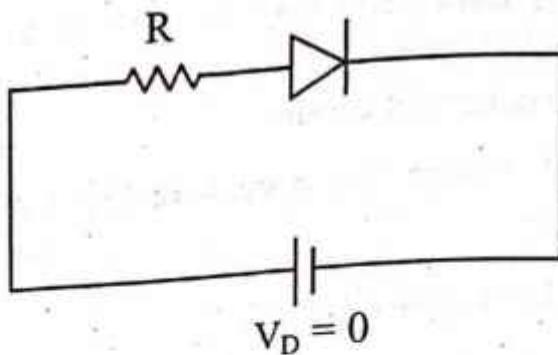
$$\text{or, } V_{D2} - V_{D1} = \eta V_T \ln \frac{I_{D2}}{I_{D1}}$$

$$\text{or, } V_{D2} - V_{D1} = 2.3 \eta V_T \log \frac{I_{D2}}{I_{D1}}$$

### 1.3 Physical Operation of Diodes

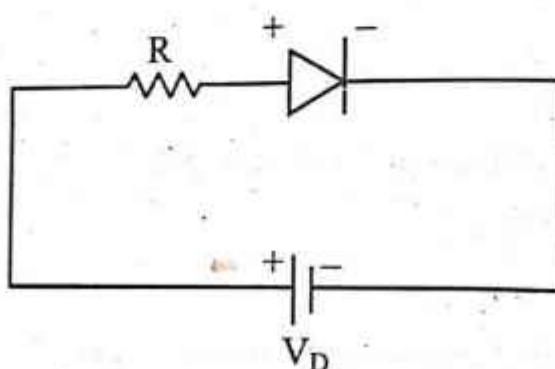
#### i. No Biasing applied ( $V_D = 0\text{V}$ )

In absence of an applied bias, the net flow of electron or holes (charges) in one direction is zero. Hence, no current flows if no biasing voltage is applied.



### ii. Forward - Bias Region:

A forward bias condition is established by applying the positive potential to the p-type material and the negative potential to n-type material as shown in the figure.



A glance at the I-V characteristics in the forward region reveals that the current is negligibly small for  $V_D$  smaller than about 0.5V. This value is usually referred as the cut-in voltage. But for a "fully conducting" diode, the voltage drop lies in a narrow range, approximately 0.6v to 0.8v.

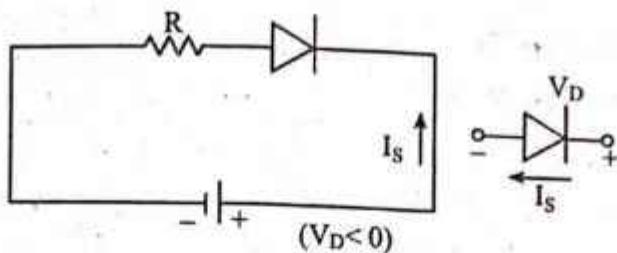
### iii. Reverse Bias Region: ( $V_D < 0$ )

The reverse- Bias region of operation is entered when the diode voltage  $V_D$  is negative.

We have,

$$I_D = I_s (e^{V_D / \eta V_T} - 1) \dots \text{(i)}$$

In equation (i) if  $V_D$  is negative and a few times larger than  $V_T$  (25mv) in magnitude, the exponential term becomes negligibly small compared to unity, and the diode current becomes:  $I_D \approx -I_s$



#### iv. Breakdown Region:

The breakdown region can be easily identified on the diode I-V characteristics (see figure). The breakdown region is entered when the magnitude of the reverse voltage exceeds a threshold value that is specific to the particular diode, is called the "breakdown voltage". This is the voltage at the "knee" of the I-V curve in figure and is denoted by  $V_{ZK}$ , where the subscript 'Z' stands for zener and 'K' denotes knee.

---

### 1.4 Analysis of Diode Circuits

---

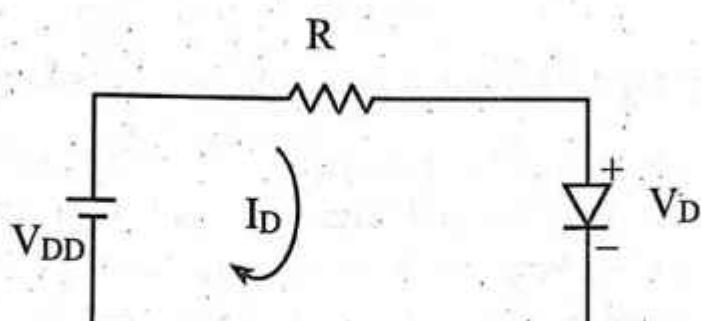
#### a. Using load line:

Load line is constructed to determine an appropriate 'Q' point for given circuit. i.e. working point for the given circuit.

In order to construct a load line of a device (diode circuits) two things are important.

- i. Volt-ampere characteristics of the device (diode) and
- ii. Current expression for the given circuit

Let us consider a diode circuit as shown below



*Fig. 1.4(a) Simple diode circuit*

From figure,

$$V_{DD} - I_D R - V_D = 0$$

$$\therefore I_D = \frac{V_{DD} - V_D}{R} \dots\dots (i)$$

Putting  $V_D = 0$  in equation (i),

We get,

$I_D$  maximum

$$\text{i.e. } I_{D\max} = \frac{V_{DD} - 0}{R} = \frac{V_{DD}}{R} \dots\dots (ii)$$

Again,

Putting  $I_D = 0$  in equation (i),

We get,  $V_{D\max}$  i.e.

$$V_{D\max} = V_{DD} \dots\dots (iii)$$

Plotting equation (ii) & (iii) in figure below

i.e. in I-V curve

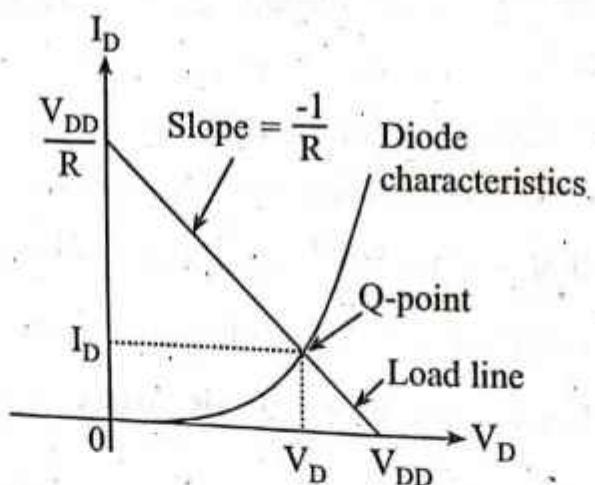
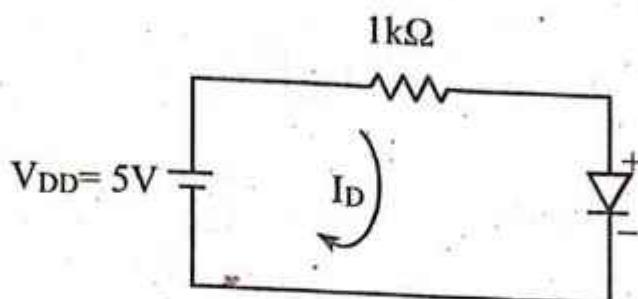


Fig.1.4 (b) Diode characteristics showing load line

Plotting these two points  $(V_{DD}/R, V_{DD})$  an intersection point is obtained. This point is known as operating point or working point or Q (quiescent) point and gives the biasing voltage  $V_D$  and the current  $I_D$ . The straight line represented by equation (i) is called load line.

**b. Using Iterative method:**

Determine the current  $I_D$  and the diode voltage  $V_D$  for the circuit in figure with  $V_{DD} = 5V$  and  $R = 1K\Omega$ . Assume that the diode has a current of 1mA at a voltage of 0.7V and that its voltage drop changes by 0.1V for every decade change in current.



**Solution:**

To begin iteration, assume  $V_D = 0.7V$  and determine current as

$$I_D = \frac{V_{DD} - V_D}{R} = \frac{5 - 0.7}{1K\Omega} = 4.3 \text{ mA}$$

For better estimation of  $V_D$ , we have,

$$\begin{aligned} V_{D2} - V_{D1} &= \eta V_T \ln \left( \frac{I_{D2}}{I_{D1}} \right) \\ &= 2.3\eta V_T \log \left( \frac{I_{D2}}{I_{D1}} \right) \dots\dots (i) \end{aligned}$$

By question,

If  $\frac{I_{D2}}{I_{D1}} = 10$ ,  $V_{D2} - V_{D1} = 0.1$ , so putting these value in equation (i) we get,

$$2.3\eta V_T = 0.1$$

Thus,

$$V_{D2} - V_{D1} = 0.1 \log \left( \frac{I_{D2}}{I_{D1}} \right)$$

$$\text{or, } V_{D2} - 0.7 = 0.1 \log \frac{4.3}{1}$$

$$\therefore V_{D2} = 0.763V$$

Again, if  $V_D = 0.763V$  and  $I_D = \frac{V_{DD} - V_D}{R}$ ,

Then

$$I_D = \frac{5 - 0.763}{1K} = 4.237mA$$

$$\text{So, } V_{D3} - V_{D2} = 0.1 \log \left( \frac{I_{D3}}{I_{D2}} \right)$$

$$\text{or, } V_{D3} - 0.763 = 0.1 \log \frac{4.237}{4.3}$$

$$\therefore V_{D3} = 0.762V$$

Thus, the second iteration yields value of  $I_D = 4.237mA$  and  $V_D = 0.762V$  which are much closer to first iteration. So, the required solution is

$$I_D = 4.237mA \text{ and}$$

$$V_D = 0.762V$$

## 1.5 Large Signal Model/Small Signal Model and its Application

The representation of any device with equivalent electric elements such as resistors, capacitors, inductors, voltage/current source (s) etc. is called **modeling** and the circuit representation of any device with equivalent electric elements without the loss of its exact functional behavior is called the "**Model of the device**". A semiconductor diode can be modeled with respect to dc signal and ac signal acting on it. A dc model or large signal model shows how a device behaves when a dc signal (voltage) is acting on it. Similarly an ac or small signal model shows how the device behaves when an ac signal is acting on it.

### Large or DC signal Model:

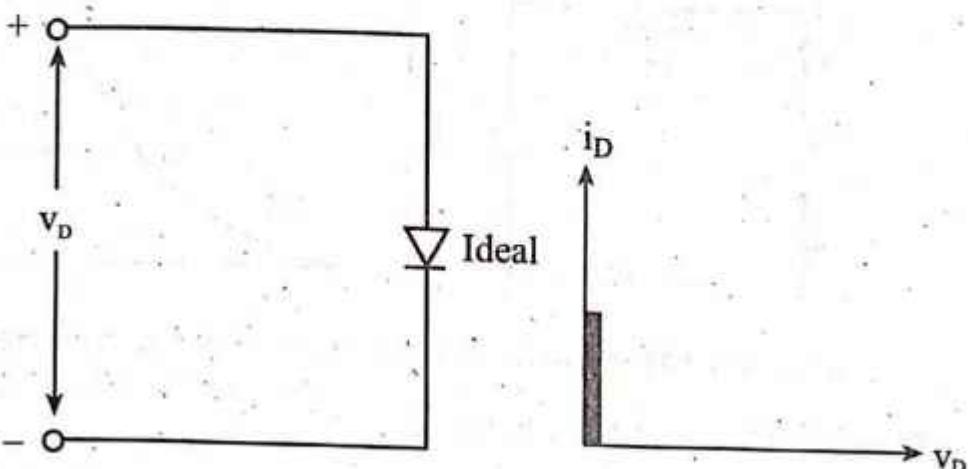
#### i. Ideal Diode Model

This model is useful for the application that involve voltages much greater than the diode voltage drop, we

may neglect the diode voltage drop altogether while calculating the diode current. This type of modeling is greatly used in determining which diodes are ON and which are OFF in a multi diode circuit (logic circuits).

The diode equation is

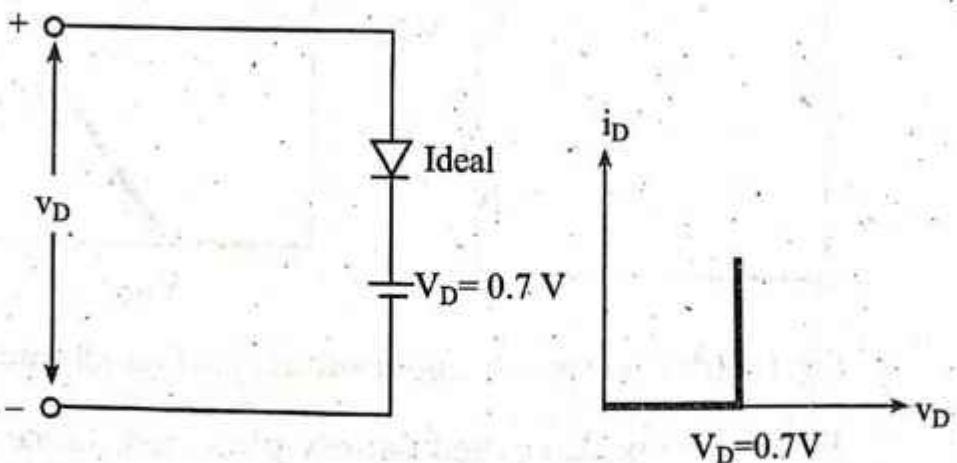
$$v_D = 0 \text{ for } i_D > 0$$



*Fig.1.5 (a) Ideal Diode Model and its characteristics curve.*

## ii. Constant voltage drop Model:

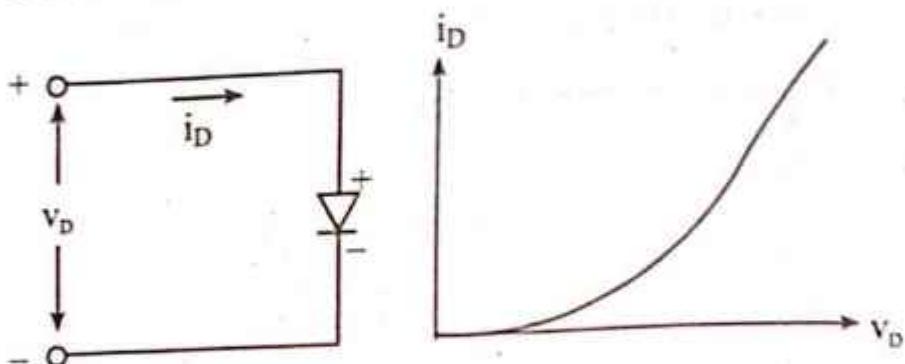
This is the simpler model of the diode forward characteristics. This uses the vertical straight line to approximate the fast-rising part of the exponential curve. This model simply says that a forward conducting diode exhibits a constant voltage drop  $V_D$ . This model is used in the initial phases of analysis and design. The equation of diode for this model is  $V_D = 0.7V$  for  $i_D > 0$



*Fig.1.5 (b) Constant voltage drop model and its characteristics curve*

### iii. Exponential Model:

The most accurate description of the diode operation in the forward region is provided by the exponential model. However, its severely non linear nature makes this model the most difficult to use.



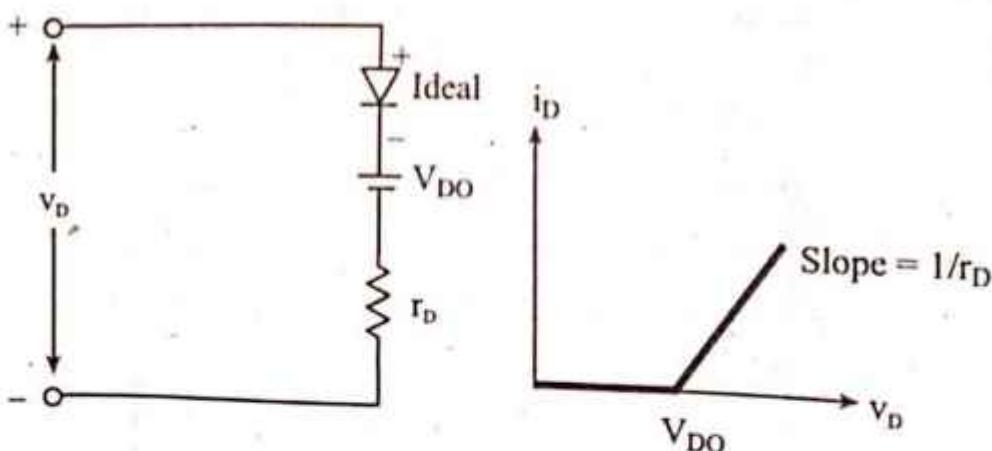
*Fig.1.5 (c) Exponential model and its characteristics curve.*

### iv. Piecewise - linear Model:

This model uses the straight line to approximate the fast rising part of exponential curve. The piecewise linear or straight line model can be described as

$$i_D = 0, v_D \leq V_{D0}$$

$$i_D = \frac{(v_D - V_{D0})}{r_D}, v_D \geq V_{D0}$$



*Fig.1.5 (d) Piecewise- linear model and its characteristics*

This model is also called battery plus - resistance model. The Model (i), (ii), (iii) and (iv) are called DC or Large signal model.

### Abbreviations:

$i_d, v_d, r_d \rightarrow$  ac quantities

$I_D, V_D, R_D \rightarrow$  dc quantities

$i_D, v_D, r_D \rightarrow$  (ac + dc) quantities i.e.  $i_D = i_d + I_D$

### Small Signal Model

For small signal operation around the dc biased point, the diode can singly be represented by a resistance equal to the inverse of slope of the tangent to exponential i-v characteristic curve at the bias point.

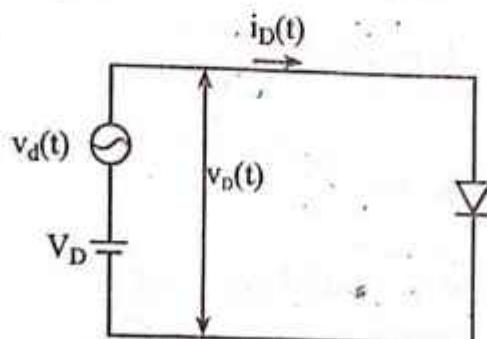


Fig.1.5(d) Circuit to Study Small Signal Model

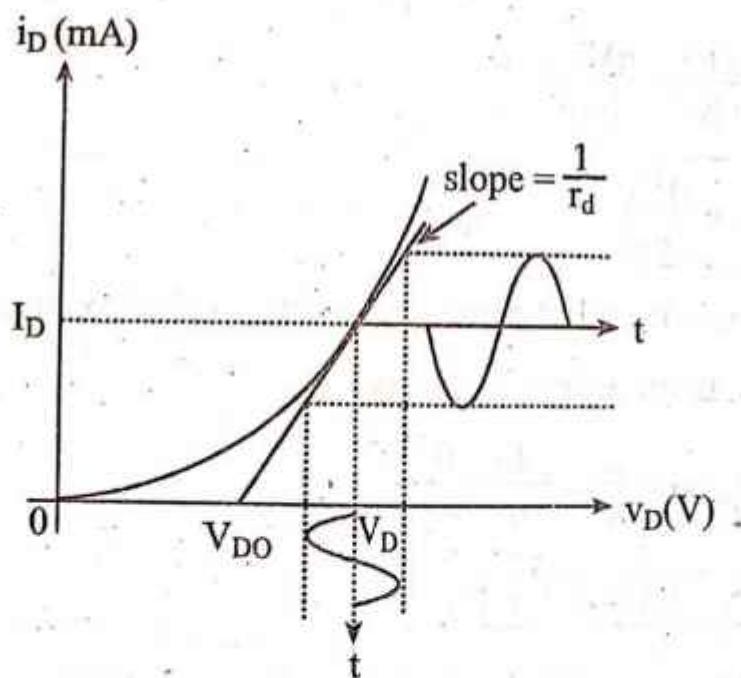


Fig: Graphical analysis of small signal model

Consider a simple circuit as shown in diagram. Now, we know that,

$$i_D(t) = I_S e^{v_D(t)/\eta V_T}$$

But,  $v_D(t) = V_D + v_d(t)$  and

$$i_D(t) = I_D + i_d(t)$$

So, the above equation can be rewritten as

$$I_D + i_d(t) = I_S e^{(V_D + v_d(t))/\eta V_T}$$

Expanding the exponential term and neglecting higher values since

$$\frac{v_d(t)}{\eta V_T} \ll 1, \text{ we get,}$$

$$I_D + i_d(t) = I_S e^{V_D/\eta V_T} \left( 1 + \frac{v_d(t)}{\eta V_T} \right)$$

$$\text{or, } I_D + i_d(t) = I_D + I_D \frac{v_d(t)}{\eta V_T}$$

Comparing ac to ac quantities we get

$$i_d(t) = I_D \frac{v_d(t)}{\eta V_T}$$

$$\text{or, } \frac{v_d(t)}{i_d(t)} = \frac{\eta V_T}{I_D}$$

$$\therefore r_d = \boxed{\frac{\eta V_T}{I_D}}$$

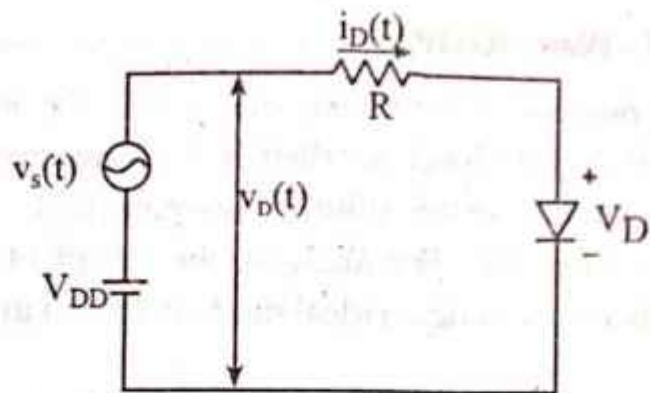
Where,  $r_d$  is called dynamic resistance or ac resistance.

Again, from graph, we have

$$\text{Slope} = \frac{1}{r_d} = \frac{I_D - 0}{V_D - V_{DO}}$$

$$\text{or, } \boxed{V_D = V_{DO} + I_D r_d} \quad \dots \dots \dots \text{(i)}$$

Now, consider a circuit as shown below:

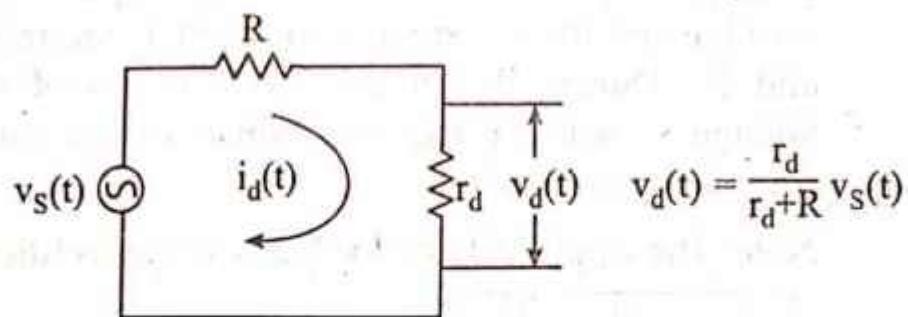
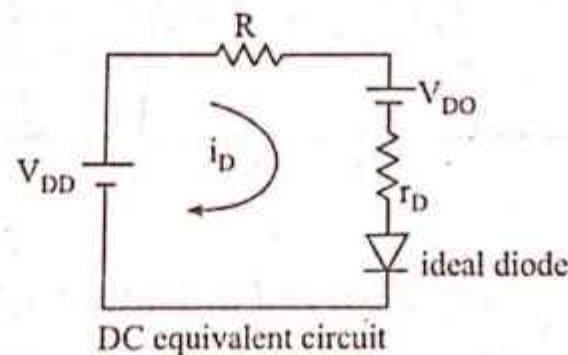


res

Now,

$$\begin{aligned}
 V_{DD} + v_s(t) &= i_D(t) R + v_D(t) \\
 &= \{I_D + i_d(t)\} R + \{V_{DO} + v_d(t)\} \\
 &= I_D R + i_d(t) R + V_{DO} + I_D r_d + i_d(t) r_d \quad [\text{From equation (i)}] \\
 &= \frac{I_D (R + r_d) + V_{DO}}{\text{DC quantity}} + \frac{i_d(t) (R + r_d)}{\text{AC quantity}}
 \end{aligned}$$

So, the diode equivalent circuit can be written as



AC equivalent circuit

### → Rectifier circuits

Rectifier is a device used for converting alternating current (AC) to direct current (DC) and the process is called rectification.

## 1. Half - Wave Rectifier:

The process of removing one - half the input signal to establish a dc level is called half - wave rectification. The half- wave rectifier utilizes alternate half - cycles, of the input sinusoid - For analysis, the circuit of a half - wave rectifier, assuming an ideal diode is shown in figure below

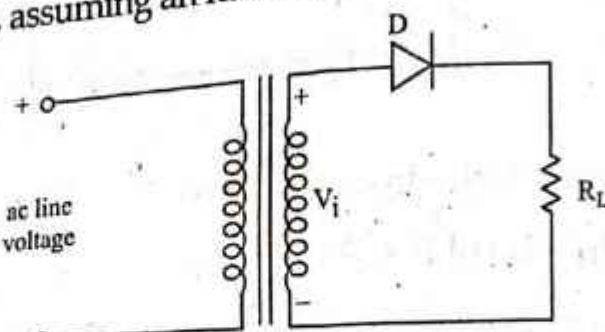


Fig: Half - wave Rectifier

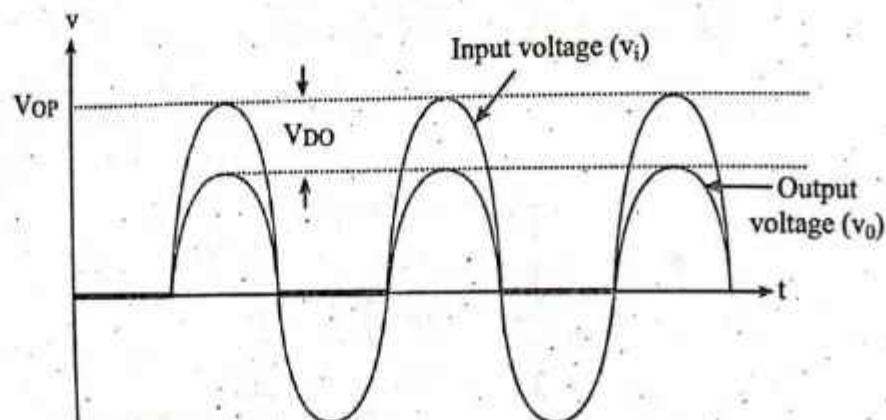


Fig. Input and Output waveforms.

During the positive half cycles of the input voltage  $v_i$  is positive and thus, current is conducted through diode D and  $R_L$ . During the negative half cycles of the input voltage  $v_i$  will be negative, which makes diode D in reverse biased condition.

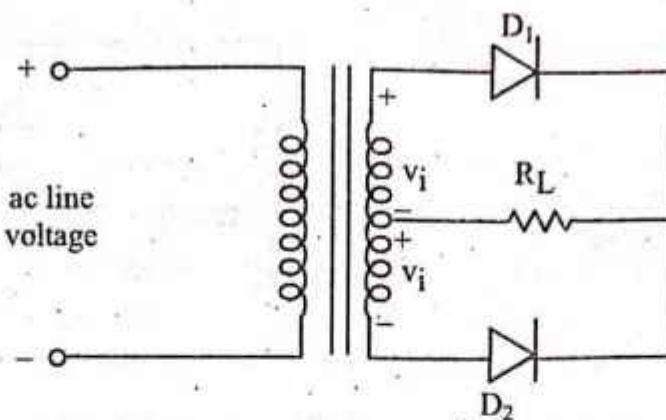
Note: The ripple voltage for half - wave rectifier is given as,

$$V_r = \frac{V_o}{fCR_L} \approx \frac{V_{OP}}{fCR_L}$$

## 2. Full - wave Rectifier:

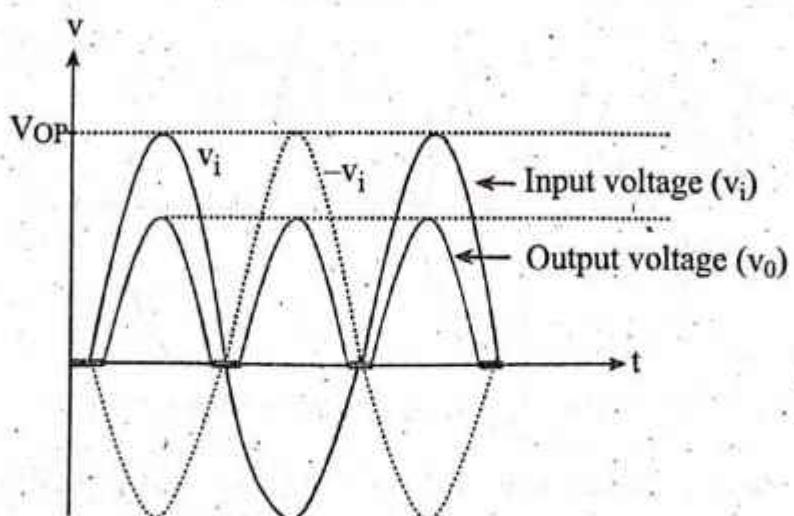
The full - wave rectifier utilizes both halves of the input sinusoid. To provide a unipolar output, it inverts the negative halves of the sine wave.

i. Center - tapped transformer full - wave rectifier:



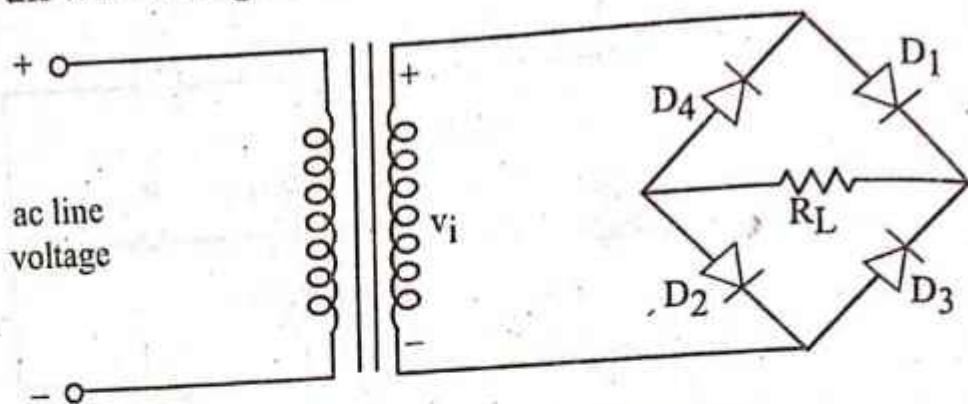
*Fig: Center - tapped transformer full - wave rectifier*

As shown in the circuit, the transformer winding is center - tapped to provide two equal voltages  $v_i$  across the two halves of the secondary winding with the polarities indicated. During the positive half - cycle of the ac line voltage (primary side), both of the signals labeled  $v_i$  will be positive. In this case,  $D_1$  will conduct and  $D_2$  will be reverse biased. The current through  $D_1$  will flow through  $R_L$  and back to the center tap of the secondary. During the negative half - cycle of the ac line voltage (primary side) both of the voltages labeled  $v_i$  will be negative. Thus  $D_1$  will be cut - off while  $D_2$  will conduct. The current conducted by  $D_2$  will flow through  $R_L$  and back to the center tap.



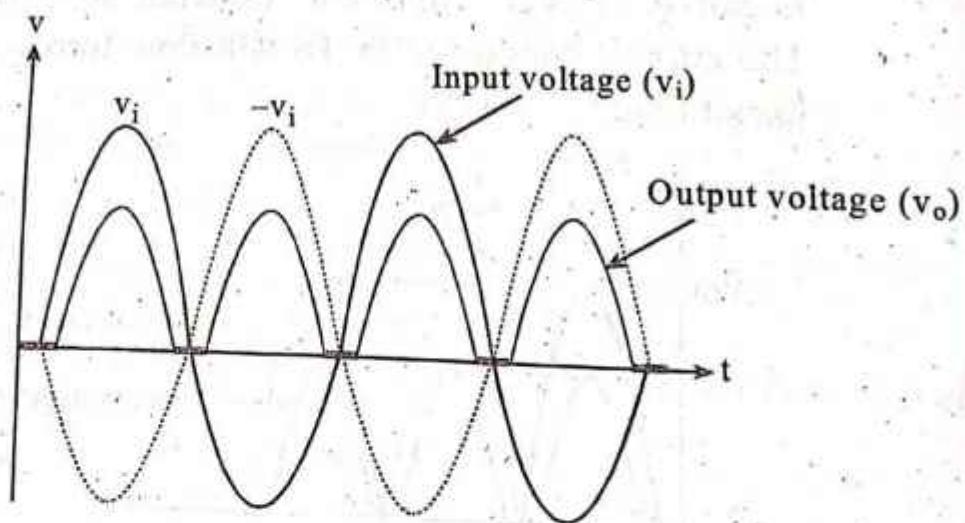
*Fig. Input and output waveforms*

## ii. Full wave bridge Rectifier:



*Fig: Full wave bridge Rectifier*

The bridge rectifier circuit operates as follows: During the positive half-cycles of the input voltage,  $v_i$  is positive, and thus, current is conducted through diode D<sub>1</sub>, resistor R<sub>L</sub> and diode D<sub>2</sub>. Meanwhile, diodes D<sub>3</sub> and D<sub>4</sub> will be reverse biased. During the negative half cycles of the input voltage,  $v_i$  will be negative, and thus -  $v_i$  will be positive, forcing current through D<sub>3</sub>, R<sub>L</sub> and D<sub>4</sub>. Meanwhile, diodes D<sub>1</sub> and D<sub>2</sub> will be reverse biased. It should be noted that, during both half-cycles of the input voltage, current flows through R<sub>L</sub> in the direction (from right to left).



*Fig: Input and output wave form*

Note: The ripple voltage for full-wave rectifier is

$$V_r = \frac{V_o}{2fCR_L} \approx \frac{V_{op}}{2fCR_L}$$

### Zener Diode

Zener diode is a special type of semi conductor diode which works in a breakdown region. It acts as a simple diode when operated in forward-bias mode but when operated in reverse breakdown, zener diodes are found to have extremely stable breakdown voltage over a wide range of current levels. Thus, the zener diodes are considered as the backbone of voltage regulators.

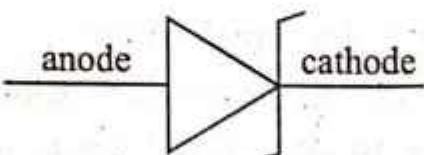


Fig1.6 (a) Symbol of Zener diode

### Breakdown phenomena:

There will always be some thermally produced electrons and holes when the zener diodes are operated in reverse biased mode. As the reverse voltage increases, the free electrons move with higher speed. Higher the reverse bias voltage, greater is the speed of electrons. But, on the increment of reverse bias voltage, the electrons gain high speed and collide with the atoms of semiconductor ejecting valence electrons. These free electrons also move with high speed and collide with atoms to produce more electrons. This phenomenon continues until high current flows in the diode. This process is called "Breakdown." Breakdown is normally of three types:

#### i. Thermal Breakdown:

In ordinary diode, when reverse biasing voltage is increased to a breakdown value, a heavy current flows through device. This will cause overheating of device that permanently destroys it. Thermal Breakdown is an irreversible process.

### ii. Zener Breakdown:

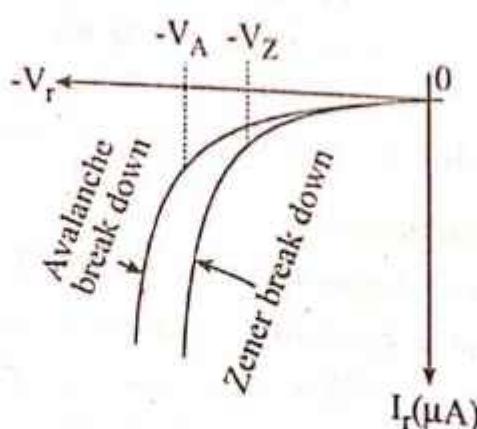
In a heavily doped pn-junction diode, zener effect occurs due to spontaneous generation of hole-electron pairs within the junction region by the effect of intense electric field across it.

The ionization is occurred due to the higher electric field, causing the bonds to break and flow of high current. This effect is negative temperature coefficient (NTC) i.e. increase in temperature causes reduction in flow of current due to more ionization and less mobility of ions. This effect occurs at low voltage.

### iii. Avalanche effect or breakdown:

In a lightly doped pn-junction diode, the high speed electrons due to large reverse bias voltage collide with valence electrons of the atoms fixed in the crystal lattice of depletion region. As a result, some electrons are liberated out of the covalent bond, thus creating further hole electron pairs. The ionization occurs due to collisions of high speed electrons with valence electrons of depletion region. It is the positive temperature coefficient (PTC) i.e. increases in temperature causes increase in flow of current. It occurs at high voltage.

Both the zener breakdown and avalanche breakdown are reversible.



Assumptions: (For ripple voltage calculation)

- Magnitude of the ripple voltage  $V_R$  is very small ( $V_R \ll V_P$ )

ii. The capacitors discharge time is approximately equal to time period of wave  $\approx T$

iii. The capacitor discharges linearly for small  $V_R$ .

When

$I_L = 0$  i.e. load is opened,

Then  $I_S = I_Z$

or,  $I_S = I_{Z\max}$

And, when load is kept at output terminal

$I_{L\max} = I_S - I_{Z\min}$

## NUMERICAL:

- Suppose,  $V_S = 24V$ ,  $V_Z = 6.2 V$ ,  $P_{\max} = 400 \text{ mW}$  and  $I_{ZK} = 1\text{mA}$ . Design a regulator circuit

*Solution:*

Here, we have,

$$I_{\max} = \frac{P_{\max}}{V_Z} = \frac{400 \text{ mW}}{6.2 \text{ V}} = 64.5 \text{ mA}$$

And,  $I_S = I_{Z\max}$  at  $I_L = 0$

So,

$$R_S = \frac{V_S - V_Z}{I_S} = \frac{24 - 6.2}{64.5} = 276 \Omega$$

The maximum load current sustainable is

$$\begin{aligned} I_{L\max} &= I_S - I_{Z\min} \\ &= (64.5 - 1) \text{ mA} \end{aligned}$$

$\therefore I_{L\max} = 63.5 \text{ mA}$

## Regulator performance

With a practical zener diode, the output voltage varies slightly whenever the input source voltage fluctuates or the output load current changes. Smaller the output voltage fluctuates, better the regulator performance is.

Thus, the regulator performance is estimated as:

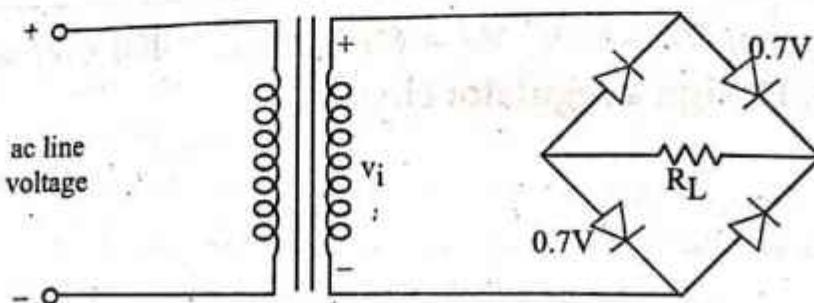
a. Regulation against input supply voltage fluctuations:

It is also called line regulation or voltage regulation to determine the line regulation performance, the equivalent diagram for voltage regulator is drawn by replacing zener diode with  $r_z$  and  $v_z$ .

- Q. Draw full wave bridge rectifier circuit with 5 ohm load resistor connected at its output. If input ac voltage is 10V, calculate the power dissipation in the load resistor (Assume diodes operate at forward voltage of 0.7V).

[069 Chaitra Regular]

Solution:



Here,

$$V_L = 10 - 0.7 \times 2 = 8.6 \text{ V}$$

The power dissipation in the load resistor is,

$$\therefore P = \frac{V_R^2}{R_L} = \frac{8.6^2}{5} = 14.79 \text{ W}$$

- Q. A diode for which  $\eta = 2$  conducts 1 mA at 0.7V. For what current is its voltage drop equal to 0.8V.

[066 Bhadra Regular]

Solution:

We have

$$\begin{aligned} I_{D2} &= I_{D1} e^{(V_2 - V_1)/\eta V_T} \\ &= 1 e^{(0.8 - 0.7)/2 \times 0.025} \\ &= 7.38 \times 10^{-3} \text{ A} \end{aligned} \quad [V_T = 25 \text{ mV}]$$

$$\therefore I_{D2} = 7.38 \text{ mA}$$

Note:  $V_{D2} - V_{D1} = \eta V_T \ln \left( \frac{I_{D2}}{I_{D1}} \right)$ .

- Q.** Find the value of dynamic resistance if voltage is in the diode is 650 mV and  $I_{RS}$  is  $10\text{pA} = (10 \times 10^{-12} \text{ A})$ . Given  $\eta = 2$  and  $V_T = 25 \text{ mV}$ . [070 Chaitra Regular]

**Solution:**

$$\text{Given, } I_{RS} = 10\text{pA} = (10 \times 10^{-12} \text{ A})$$

$$V_D = 650 \text{ mV}$$

$$V_T = 25 \text{ mV}$$

We know dynamic resistance is

$$r_d = \left( \frac{\eta V_T}{I_D} \right) \dots\dots\dots \text{(i)}$$

where,

$$I_D = I_{RS}(e^{V_D/\eta V_T} - 1) = 10 \times 10^{-12}(e^{650/2 \times 25} - 1) = 4.424 \times 10^{-6} \text{ A}$$

Then, equation (i) becomes,

$$r_d = \left( \frac{\eta V_T}{I_D} \right) = 2 \times 25 \times 10^{-3} / 4.424 \times 10^{-6} = 11301.6 \Omega = 11.301 \text{ K } \Omega$$

- Q.** A diode conducts 1 mA at  $20^\circ\text{C}$ . If it is operated at  $100^\circ\text{C}$ , what will be its current? Given data are  $\eta = 1.8$  and negative temperature coefficient value =  $-1.8 \text{ mV}/^\circ\text{C}$ .

[068 Chaitra Regular]

**Solution:**

$$\text{Given: } \left( \frac{\Delta V_D}{\Delta t} \right) = -1.8 \text{ mV}/^\circ\text{C}$$

$$\begin{aligned} \Delta V_D &= V_{D2} - V_{D1} \\ &= 1.8 \text{ mV}/^\circ\text{C} \times \Delta t \\ &= 1.8 \text{ mV}/^\circ\text{C} (100 - 20)^\circ\text{C} \\ &= -144 \text{ mV} \end{aligned}$$

We know,

$$V_{D2} - V_{D1} = 2.3\eta V_T \log\left(\frac{I_{D2}}{I_{D1}}\right)$$

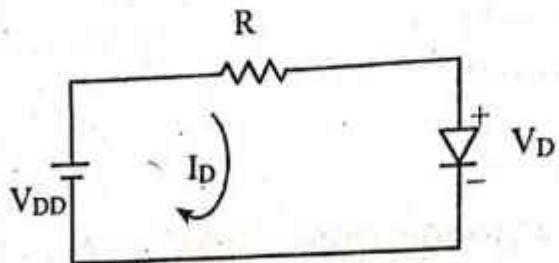
$$\text{or, } -144 = 2.3 \times 1.8 \times 25 \log\left(\frac{I_{D2}}{1}\right)$$

$$\text{or, } \frac{I_{D2}}{1\text{mA}} = 10^{\frac{144}{103.5}}$$

$$\text{or, } I_{D2} = 0.0406 \times 1\text{mA}$$

$$\therefore I_{D2} = 0.0406 \text{ mA.}$$

- Q.** In the given circuit, the diode used has its  $\eta = 1.74$  and it conducts 1 mA at forward bias voltage of 0.7 V. Find the current flow in the circuit. Given  $R = 660 \Omega$  and  $V_{DD} = 6 \text{ V}$ . [070 Ashad Back]



**Solution:**

From figure,

$$I_D = I_{D2} = \left( \frac{V_{DD} - V_{D1}}{R} \right) = \left( \frac{6 - 0.7}{660} \right) = 8.03 \text{ mA.}$$

We know,

$$V_{D2} - V_{D1} = 2.3\eta V_T \log\left(\frac{I_{D2}}{I_{D1}}\right)$$

$$\text{or, } V_{D2} = 0.7 + 2.3 \times 1.74 \times 25 \times 10^{-3} \log\left(\frac{8.03}{1}\right)$$

$$V_{D2} = 0.79 \text{ V}$$

Now,

$$I_{D3} = \left( \frac{6 - V_{D2}}{660} \right) = \left( \frac{6 - 0.79}{660} \right) = 7.89 \text{ mA}$$

Again,

$$V_{D3} - V_{D2} = 2.3\eta V_T \log\left(\frac{I_{D3}}{I_{D2}}\right)$$

$$\text{or, } V_{D3} = 0.79 + 2.3 \times 1.74 \times 25 \times 10^{-3} \log\left(\frac{7.89}{8.03}\right)$$

$$\text{or, } V_{D3} = 0.789 \text{ V}$$

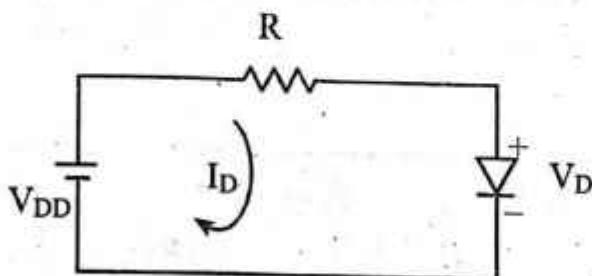
Finally,

$$I_{D4} = \left( \frac{6 - V_{D3}}{660} \right) = \left( \frac{6 - 0.789}{660} \right) = 7.89 \text{ mA}$$

Therefore the current flow in the circuit is 7.89 mA.

- Q. In the given circuit, the diode used has its  $\eta = 1.74$  and it conducts 1 mA at forward bias voltage of 0.7 V. Find the current flow in the circuit. Given  $R = 500\Omega$  and  $V_{DD} = 5V$ .

[072 Kartik Back]



*Solution:*

From figure

$$I_D = I_{D2} = \left( \frac{V_{DD} - V_{D1}}{R} \right) = \left( \frac{5 - 0.7}{500} \right) = 8.6 \text{ mA}$$

$$V_{D2} - V_{D1} = 2.3\eta V_T \log\left(\frac{I_{D2}}{I_{D1}}\right)$$

$$\text{or, } V_{D2} = 0.7 + 2.3 \times 1.74 \times 25 \times 10^{-3} \log\left(\frac{8.6}{1}\right)$$

$$V_{D2} = 0.793 \text{ V}$$

Now,

$$I_{D3} = \left( \frac{5 - V_{D2}}{500} \right) = \left( \frac{5 - 0.793}{500} \right) = 8.41 \text{ mA}$$

Again,

$$V_{D3} - V_{D2} = 2.3\eta V_T \log\left(\frac{I_{D3}}{I_{D2}}\right)$$

$$\text{or, } V_{D3} = 0.793 + 2.3 \times 1.74 \times 25 \times 10^{-3} \log\left(\frac{8.41}{8.6}\right)$$

$$\therefore V_{D3} = 0.792 \text{ V}$$

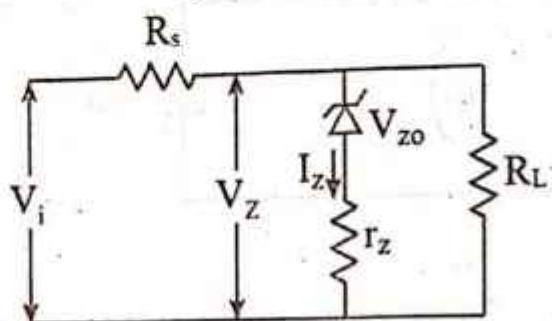
Finally,

$$I_{D4} = \left( \frac{5 - V_{D3}}{500} \right) = \left( \frac{5 - 0.792}{500} \right) = 8.41 \text{ mA}$$

Therefore the current flow in the circuit is 8.41 mA

- Q. Design DC voltage regulator for 6V output. Given data are  $V_Z = 6\text{V}$  at  $I_Z = 20\text{mA}$ ,  $I_{ZK} = 2\text{mA}$ ,  $P_{ZMAX} = 500\text{mW}$  and  $r_z = 20\Omega$ . The nominal input voltage is  $12\text{V} \pm 20\%$  DC. Find its voltage regulation factor and maximum current it can deliver to the load. (2067 Ashad Regular/ 2071 Shrawan Back)

*Solution:*



Here,

$$V_i = 12\text{V} \pm 20\% = 9.6\text{V} \text{ to } 14.4\text{V}$$

And,

$$V_z = V_{zo} + I_z r_z$$

$$\text{or, } 6 = V_{zo} + 20 \times 10^{-3} \times 20$$

$$\therefore V_{zo} = 5.6\text{V}$$

Now, for the voltage regulation to breakdown zener diode  $VR_L \geq V_z$ .

When  $V_i = 9.6\text{V}$

$$VR_L = \frac{R_L}{R_L + R_s} \times V_i$$

$$\text{or, } 6 = \frac{R_L}{R_L + R_s} \times 9.6$$

$$\text{or, } \frac{R_L}{R_L + R_s} = 0.625$$

$$\text{or, } \frac{R_L}{R_s} = 1.67$$

$$\therefore R_L \geq 1.67 R_s \dots \text{(i)}$$

Also,

When,  $V_i = 14.4V$

$$V_{RL} = \frac{R_L}{R_L + R_s} \times V_i$$

$$\text{or, } 6 = \frac{R_L}{R_L + R_s} \times 14.4$$

$$\text{or, } \frac{R_L}{R_s} = 0.714$$

$$\therefore R_L \geq 0.714 R_s \dots \text{(ii)}$$

We know,

$$I_{Z\max} = \sqrt{\frac{P_{Z\max}}{r_Z}} = \sqrt{\frac{500}{20 \times 10^{-3}}} = 158 \text{ mA}$$

### Calculation of $R_s$ at worst condition

- a. When  $V_i = 9.6V$ , in that case also the zener diode should be at breakdown reason and if load is open then

$$V_i = I_{ZK} R_s + V_{ZO} + I_{ZK} r_z$$

$$\text{or, } 9.6 = 2 \times 10^{-3} \times R_s + 5.6 + 2 \times 10^{-3} \times 20$$

$$\text{or, } R_s = 1980 \Omega$$

$$\therefore R_s \leq 1980 \Omega$$

- b. When  $V_i = 14.4V$ , in this case also, the  $R_s$  should be selected in a such a way that zener diode should not burn out.

$$V_{i\max} = I_{Z\max} R_s + V_{ZO} + I_{Z\max} r_z$$

$$\text{or, } 14.4 = 158 \times 10^{-3} R_s + 5.6 + 158 \times 10^{-3} \times 20$$

$$\text{or, } R_s = 35.69 \Omega$$

$$\therefore R_s \geq 35.69 \Omega$$

So, the resistor  $R_s$  should be selected in between  $35.69 \Omega$  to  $1980 \Omega$ .

We know,

$$I_S = I_Z + I_L$$

$$\text{or, } I_L = I_S - I_Z$$

$$\therefore I_{L\max} = (158 - 2) \text{mA} = 156 \text{mA}$$

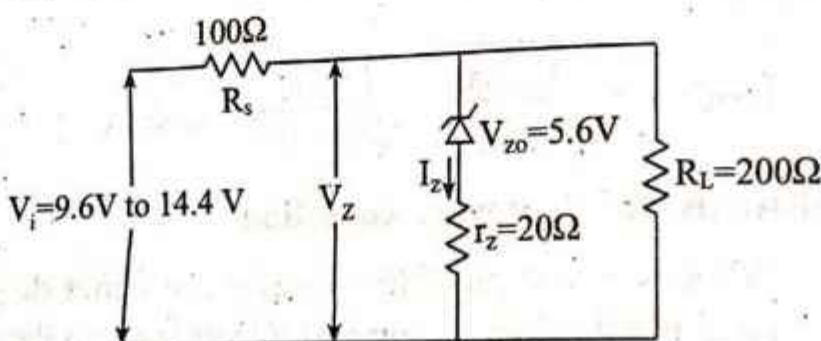
∴  $I_{L\max} = (158 - 2)\text{mA} = 156\text{mA}$   
 Now, for voltage regulation factor, since  $R_s$  is between  
 $35.69 \Omega$  to  $1980 \Omega$  let's choose  $R_s = 100 \Omega$ .

Then from (i) and (ii)

$$R_L \geq 167 \Omega$$

and  $R_1 \geq 71.4 \Omega$

So,  $R_i = 200 \Omega$  (Say)



We know,

$$\dot{VR} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%$$

- a) Then, at no load when  $V_i = 9.6V$

$$V_{NL} = V_{ZO} + I_z r_z \dots \dots \dots \text{(iii)}$$

At no load,  $I_z = I_s$

$$\text{i.e., } I_Z = \frac{9.6 - 5.6}{100 + 20} = 33.3 \text{ mA}$$

Then, from (iii)

$$V_{NL} = 5.6 + 33.3 \times 10^{-3} \times 20 = 6.26 \text{ V}$$

$$I_{FL} = I_S - I_{ZK} = 33.3 - 2 = 31.3 \text{ mA}$$

Also, at full load

$$V_{FL} = \frac{6.26 - 5.64}{5.64} \times 100\%$$

$$= 10.99\%$$

- b) Again at no load when  $V_i = 14.4V$

$$V_{NL} = V_{Z0} + I_z r_z \dots \text{(iv)}$$

Where,

$$I_z = \frac{14.4 - 5.6}{100 + 20} = 73.3 \text{ mA} = I_s$$

Then, from (iv)

$$V_{NL} = 5.6 + 73.3 \times 10^{-3} \times 20 = 7.06V$$

$$I_{FL} = I_s - I_{ZK} = 73.3 \text{ mA} - 2 \text{ mA} = 71.3 \text{ mA}$$

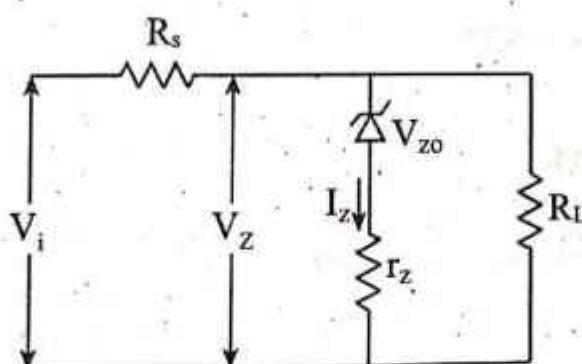
Also, at full load,

$$\begin{aligned} V_{FL} &= V_{Z0} + I_{ZK} \times r_z \\ &= 5.6 + 2 \times 10^{-3} \times 20 \\ &= 5.64V \end{aligned}$$

$$VR = \frac{7.06 - 5.64}{5.64} \times 100\% = 25.17\%$$

- Q. Design DC voltage regulator for 6V output. Given data  $V_Z = 6V$  at  $I_Z = 20 \text{ mA}$ ,  $I_{ZK} = 2 \text{ mA}$ ,  $P_{zmax} = 500 \text{ mA}$  and  $r_z = 10\Omega$ . The normal input voltage is  $15V \pm 30\%$  DC. Find maximum current it can deliver to the load. (072 Chaitra Regular)

*Solution*



Here,

$$V_i = 15V \pm 30\% = 10.5V \text{ to } 19.5V$$

And,

$$V_z = V_{z0} + I_z \Gamma_z$$

$$\text{or, } 6 = V_{z_0} + 20 \times 10^{-3} \times 10$$

$$\therefore V_{z0} = 5.8V$$

Now, for the voltage regulation to breakdown zener diode  
 $V_{RL} \geq V_Z$ .

**When  $V_i=10.5V$**

$$V_{RL} = \frac{R_L}{R_L + R_s} \times V_i$$

$$\text{or, } 6 = \frac{R_L}{R_L + R_s} \times 10.5$$

$$\text{or, } \frac{R_L}{R_L + R_s} = 0.571$$

$$\text{or, } \frac{R_L}{R_s} = 1.33$$

Also,

**When  $V_i = 19.5V$**

$$V_{RL} = \frac{R_L}{R_L + R_S} \times V_i$$

$$\text{or, } 6 = \frac{R_L}{R_L + R_s} \times 19.5$$

$$\text{or, } \frac{R_L}{R_L + R_s} = 0.307$$

$$\text{or, } \frac{R_L}{R_S} = 0.443$$

We know,

$$I_{Zmax} = \sqrt{\frac{P_{Zmax}}{r_Z}} = \sqrt{\frac{500}{10 \times 10^{-3}}} = 223.60 \text{ mA}$$

### Calculation of $R_s$ at worst condition

- a) When  $V_i = 10.5V$ , in that case also the zener diode should be at breakdown reason and if load is open then

$$V_i = I_{zk}R_s + V_{zo} + I_{zk}r_z$$

$$\text{or, } 10.5 = 2 \times 10^{-3} \times R_s + 5.8 + 2 \times 10^{-3} \times 10$$

$$\text{or, } R_s = 2340 \Omega$$

$$\therefore R_s \leq 2340 \Omega$$

- b) When  $V_i = 19.5V$ , in this case also, the  $R_s$  should be selected in a such a way that zener diode should not burn out.

$$V_{imax} = I_{Zmax}R_s + V_{zo} + I_{Zmax}r_z$$

$$\text{or, } 19.5 = 223.60 \times 10^{-3} R_s + 5.8 + 223.60 \times 10^{-3} \times 10$$

$$\text{or, } R_s = 51.27 \Omega$$

So, the resistor  $R_s$  should be selected in between  $51.27 \Omega$  to  $2340 \Omega$ .

We know,

$$I_S = I_Z + I_L$$

$$\text{or, } I_L = I_S - I_Z$$

$$\therefore I_{Lmax} = (223.60 - 2) \text{mA} = 221.60 \text{mA}$$

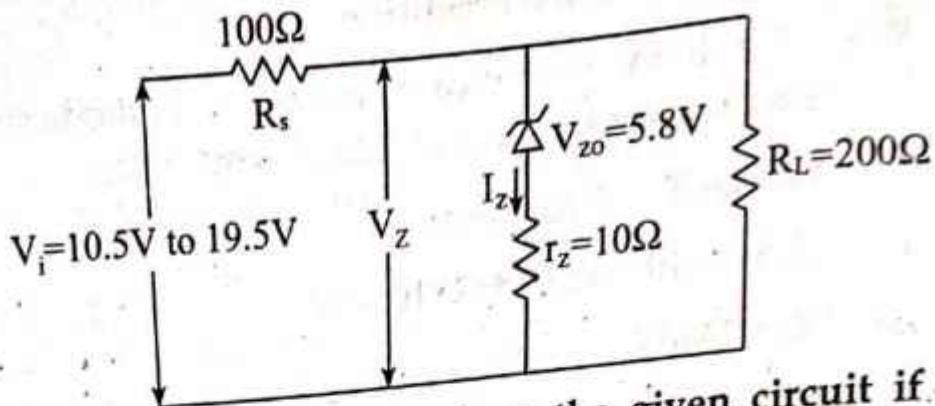
Since  $R_s$  is between  $51.27 \Omega$  to  $2340 \Omega$  let's choose  $R_s = 100 \Omega$ . (Say)

Then from (i) and (ii)

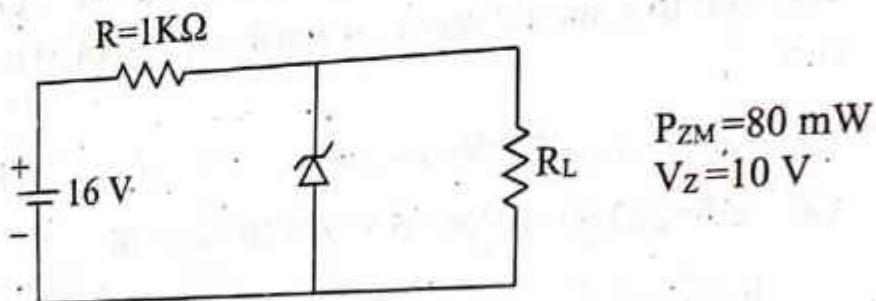
$$R_L \geq 133 \Omega$$

$$\text{and } R_L \geq 44.3 \Omega$$

$$\text{So, } R_L = 200 \Omega$$



Q) Find the zener current from the given circuit if (i)  $R_L = 1.2\text{K}\Omega$  (ii)  $R_L = 3\text{K}\Omega$ . (073 Shrawan Back)



*Solution:*

Case I:- When  $R_L = 1.2\text{K}\Omega$

$$V_L = \frac{R_L}{R+R_L} \times V_i = \frac{1.2}{1+1.2} \times 16 = 8.727\text{V}$$

Since  $V_L = 8.727\text{V}$  is less than  $V_z = 10\text{V}$ , the diode is in OFF state

$$\therefore V_L = 8.727\text{V}$$

$$I_z = 0$$

Case II:- When  $R_L = 3\text{K}\Omega$

$$V_L = \frac{R}{R+R_L} \times V_i = \frac{3}{1+3} \times 16 = 12\text{V}$$

Since  $V_L = 12\text{V}$  is greater than  $V_z = 10\text{V}$ , the diode is in ON state.

$$\therefore V_L = V_z = 10\text{V}$$

$$\text{And, } V_R = V_i - V_L = 16 - 10 = 6\text{V}$$

Now,

$$I_L = \frac{V_L}{R_L} = \frac{10}{3\text{K}\Omega} = 3.33\text{mA}$$

Also,

$$I_R = \frac{V_R}{R} = \frac{6}{1K\Omega} = 6mA$$

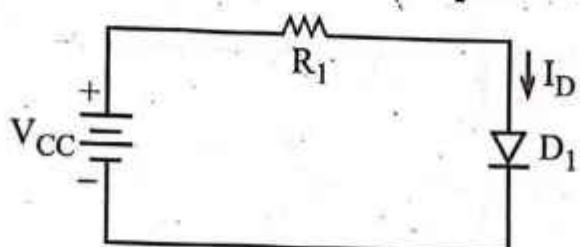
We know,

$$I_R = I_Z + I_L$$

$$\therefore I_Z = I_R - I_L = 6 - 3.33 = 2.67mA$$

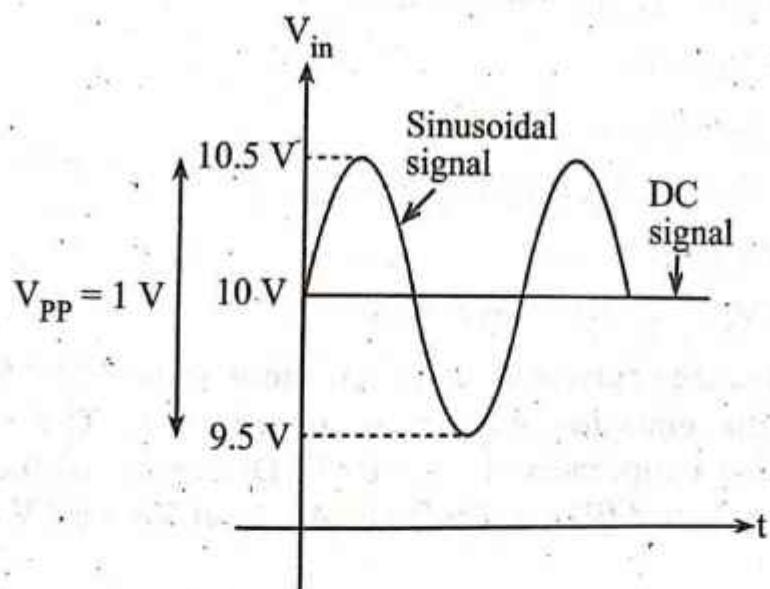
- Q. In the circuit given below, the DC power supply  $V_{CC} = 10V$  is superimposed with 60 Hz sinusoid of 1 V<sub>PP</sub> amplitude. Calculate the amplitude of the sine wave signal appearing across the diode for the case  $R_1 = 10 K\Omega$ . Assume the constant voltage drop of 0.7 V in the diode.

[2073 Chaitra, Regular]

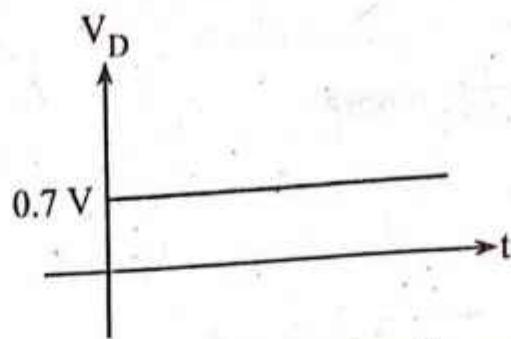


*Solution:*

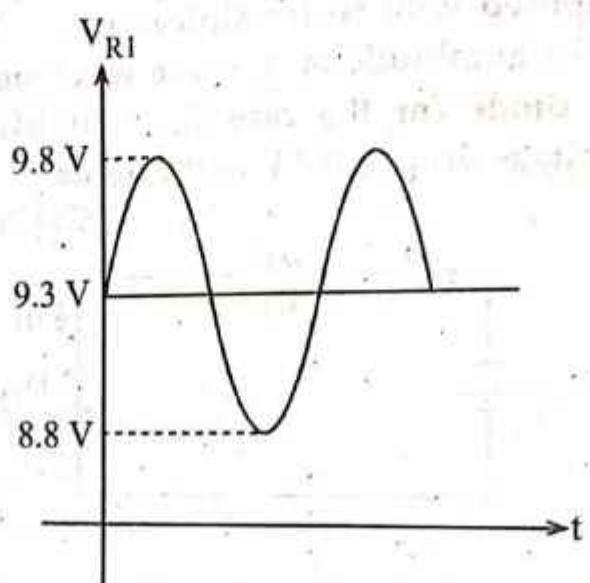
According to question, drawing the input waveform,



Now, amplitude of sine wave signals appearing across the diode will be 0.7 V as shown in figure below.



Note: Amplitude of sine wave signal appearing across the Resistor ( $R_1$ ) would be as shown in figure below.



From given circuit we can write,

$$V_{CC} = V_{R1} + V_D$$

For  $V_{CC} = 10.5 \text{ V}$

$$\therefore V_{R1} = V_{CC} - V_D = 10.5 - 0.7 = 9.8 \text{ V}$$

For  $V_{CC} = 9.5 \text{ V}$

$$V_{R1} = V_{CC} - V_D = 9.5 - 0.7 = 8.8 \text{ V}$$

- Q.** The leakage current of a silicon diode is  $I_S = 10^{-9} \text{ A}$  at  $25^\circ\text{C}$ , and the emission coefficient is  $\eta = 1.6$ . The operating junction temperature is  $T_j = 60^\circ\text{C}$ . Determine (i) the leakage current  $I_S$  and (ii) the diode current  $I_D$  at  $V_D = 0.8 \text{ V}$

*Solution:*

Here,

$$\begin{aligned} \text{Change in temperature } (\Delta t) &= (\theta_2 - \theta_1) \quad [\theta_2 > \theta_1] \\ &= (60 - 25)^\circ\text{C} = 35^\circ\text{C} \end{aligned}$$

$$I_S \text{ at } 25^\circ\text{C} = 10^{-9} \text{ A}$$

i.  $I_S \text{ at } 60^\circ\text{C} = ?$

ii.  $I_D = ? \text{ at } V_D = 0.8 \text{ V and } T_j = 60^\circ\text{C}$ .

For case (i)

We know,  $I_S$  increases by 7% per degree celcius. Then we can write,

$$I_{S02} = I_{S01} \left(1 + \frac{7}{100}\right)^{Dt}$$

$$I_{S60^\circ\text{C}} = I_{S25^\circ\text{C}} \left(1 + \frac{7}{100}\right)^{Dt}$$

or,  $I_{S60^\circ\text{C}} = 10^{-9} \left(1 + \frac{7}{100}\right)^{35}$

$$\therefore I_{S60^\circ\text{C}} = 10.67 \text{ nA}$$

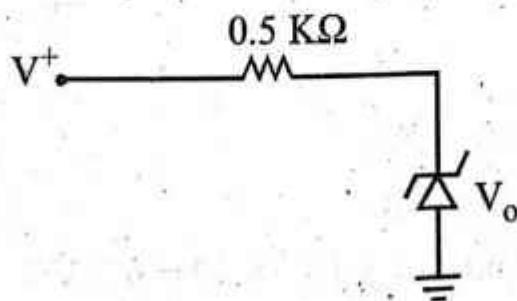
For case (ii)

$$V_T \text{ at } 60^\circ\text{C} = \frac{KT}{q} = \frac{1.38 \times 10^{-23}}{1.6 \times 10^{-19}} \times (273 + 60) = 28.72 \text{ mV}$$

Then,

$$I_D = I_{S60^\circ\text{C}} \frac{V_D}{e^{\eta V_T} - 1}$$
$$= 10.67 \frac{0.8}{e^{1.6 \times 28.72 \times 10^{-3}} - 1} = 0.388 \text{ A}$$

- Q. The 6.8 V zener diode is specified to have  $V_Z = 6.8 \text{ V}$  at  $I_Z = 5 \text{ mA}$ ,  $r_Z = 20 \Omega$  and  $I_{ZK} = 0.2 \text{ mA}$ . The Supply Voltage  $V^+$  is nominally 10 V but can vary  $\pm 1 \text{ V}$ . Find  $V_o$  with no load and with  $V^+$  at its nominal value. Find the change in  $V_o$  resulting from connecting a load resistance  $R_L$  that draws a current  $I_L = 1 \text{ mA}$ . What is the minimum value of  $R_L$  for which the diode still operates in the breakdown region?



**Solution:**

Given,

$$V_Z = 6.8 \text{ V at } I_Z = 5 \text{ mA}$$

$$r_Z = 20 \Omega$$

$$I_{ZK} = 0.2 \text{ mA}$$

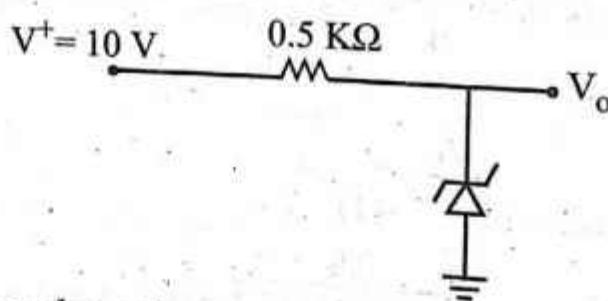
$$V^+ = 10 \text{ V} \pm 1 \text{ V}$$

According to question,

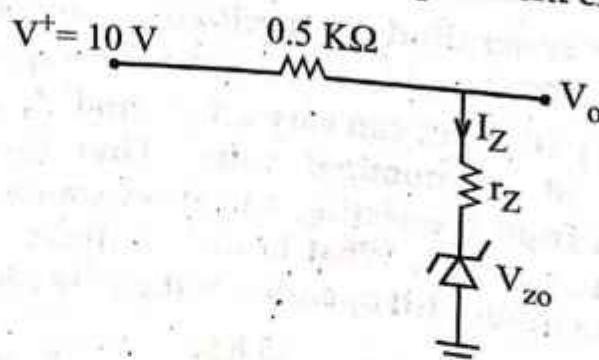
- $V_o$  with no load = ? at  $V^+$  nominal value i.e. at 10 V
- Change in  $V_o$  ( $\Delta V_o$ ) = ? Connecting load resistance  $R_L$  that draws a current  $I_L = 1 \text{ mA}$ .
- Minimum value of  $R_L$  = ? for which diode still operates in the breakdown region

Now,

- $V_o$  with no load = ? at  $V^+$  nominal value



Changing above figure with its equivalent circuit



Here,

$$V_Z = I_Z r_Z + V_{ZO}$$

$$V_{ZO} = V_Z - I_Z r_Z$$

$$= 6.8 - 5 \times 10^{-3} \times 20 = 6.7 \text{ V}$$

Now,

$$V^+ = I_Z \times 0.5 \times 10^3 + I_Z \times 20 + V_{Z0}$$

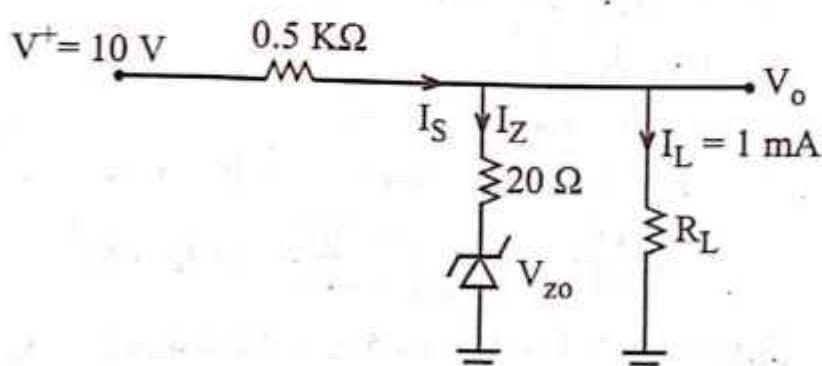
$$\text{or, } 10 \text{ V} = I_Z (0.5 \times 10^3 + 20) + 6.7$$

$$\therefore I_Z = \frac{10 - 6.7}{520} = 6.346 \text{ mA}$$

$$\therefore V_O = I_Z r_Z + V_{Z0}$$

$$\text{or, } V_O = 6.346 \times 10^{-3} \times 20 + 6.7 \text{ V} = 6.83 \text{ V}$$

- ii. Change in  $V_O$  ( $\Delta V_O$ ) = ? Connecting load resistance  $R_L$  that draws a current  $I_L = 1 \text{ mA}$



After connecting the  $R_L$  with  $I_L = 1 \text{ mA}$  finding  $I_Z$  from figure,

$$I_S = I_Z + I_L$$

$$\text{or, } I_Z = I_S - I_L$$

$$= (6.346 - 1) \text{ mA} = 5.346 \text{ mA}$$

Now,

$$V_O = I_Z r_Z + V_{Z0}$$

$$= 5.346 \times 10^{-3} \times 20 + 6.7 = 6.806 \text{ V}$$

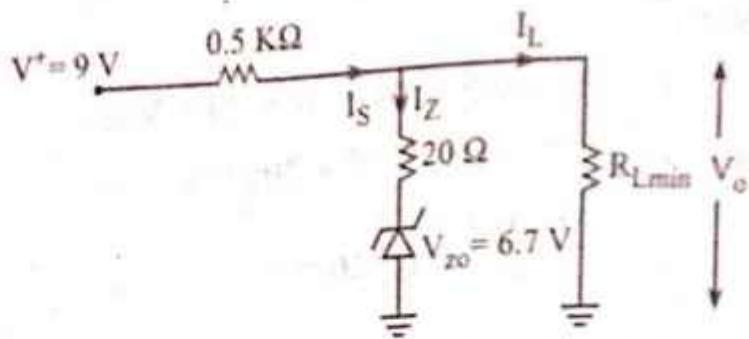
Then, change in  $V_O$

$$\Delta V_O = 6.806 - 6.83 = -0.0246 \text{ V}$$

- iii. Minimum value of  $R_L$  for which diode operates in breakdown region?

For minimum value of  $R_L$ , in worst condition,

$$V^+ = 10 - 1 = 9 \text{ V}$$



$$I_{ZK} = 0.2 \text{ mA}$$

$$I_S = I_Z + I_L$$

$$\text{or, } I_Z = I_S - I_L$$

For  $R_{L\min}$   $I_Z$  must be  $I_{ZK}$

$$\therefore I_{ZK} = I_S - I_L$$

$$\text{or, } I_L = I_S - I_{ZK} \dots \dots \dots \text{(i)}$$

$$V_o = I_{ZK} \times 20 + V_{Z0} = 0.2 \times 10^{-3} \times 20 + 6.7 = 6.704 \text{ V}$$

$$\therefore I_S = \frac{V^* - V_o}{0.5 \times 10^3} = \frac{9 - 6.704}{0.5 \times 10^3} = 4.592 \text{ mA}$$

$$\text{From (i) } I_L = I_S - I_{ZK} = 4.592 - 0.2 = 4.392 \text{ mA}$$

$$\therefore R_{L\min} = \frac{V_o}{I_L} = \frac{6.704}{4.392} = 1.53 \text{ K}\Omega$$

### TUTORIAL - 1

1. Describe the construction and principle of operation of PN junction diode in forward as well as in reverse biased conditions, explaining the terms Barrier potential and Depletion layer.
2. A diode is connected in forward biased mode with a source voltage  $V_S = 5\text{V}$  in series with a resistance of  $500\Omega$ . Find the current flow in the circuit. Given data are: The diodes drop changes by  $0.1\text{V}$  for every decade change in current.
3. Draw a small signal model of the PN junction diode and derive the expression to find the small signal increment resistance of diode?
4. Draw graphs of IV characteristics of ordinary PN junction diode and zener diode. Draw ac equivalent model for PN junction diode and derive its ac resistance.

# BIPOLAR JUNCTION TRANSISTOR

## Introduction

After the knowledge of diode, now the focus shifts towards the study of the three terminals (emitter, base and collector) non-linear semiconductor device which is Bipolar Junction Transistor (BJT). It is an electronic component mainly used for amplification and switching purpose. As the name suggests, it is composed of two junctions namely, emitter-base junction and collector-base junction. BJT was introduced by Shockley in 1948. BJT is called a current controlled device where small current at the base side is used to control the large current at other terminals.

A bipolar junction transistor (BJT) is a specially constructed three terminal semiconductor device containing two p-n junctions. The basic principle involved is the use of the voltage between two terminals to control the current flowing in third terminal. In this type of transistor, the current conduction is due to both electrons and holes, which is the reason for the name bipolar.

## Geometry and Doping Level

A BJT has three different regions: (i) the emitter (ii) the base and iii) the collector. The base region or the central layer is very much narrower than the outer two layers. Also, this region is much lightly doped in comparison to other two layers. The emitter region, with larger area, is the most heavily doped region while the collector region has the largest area and doping level with a value lying in between emitter and base region. The emitter is named emitter as it emits electrons or holes, while the collector collects electrons or holes. Because the outer layers i.e. emitter and collector are heavily doped, the depletion region penetrates deeper into the base reducing the width of the base.

## **Two types of Bipolar Junction Transistors:**

Depending upon the layers formed there are two types of transistors NPN and PNP. In NPN transistor a thin layer of P type semiconductor is sandwiched between two thicker layers of N type semiconductors. Similarly, in PNP transistor a thin layer of N type semiconductor is sandwiched between two thicker layers of p type semiconductors. The structural and circuit diagram of NPN and PNP transistor are shown in following figures.

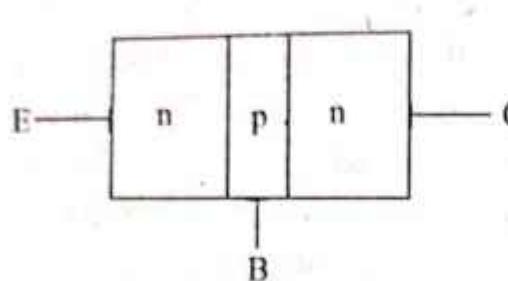


Fig: Structural diagram of npn

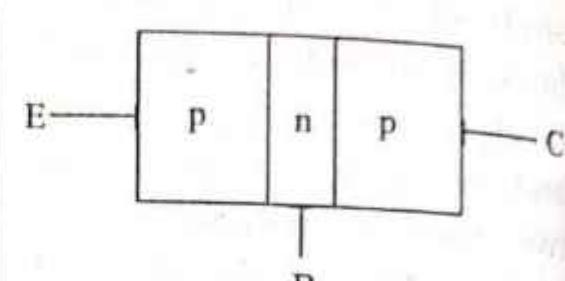


Fig: Structural diagram of pnp

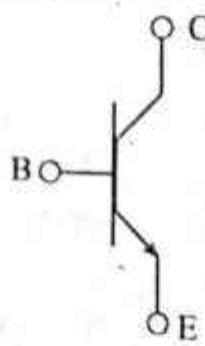


Fig: Symbol of npn transistor

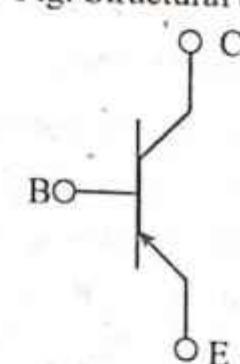


Fig: Symbol of pnp transistor

### **Mode:**

It describes the voltage level across the two junctions emitter base (EB) and collector base (CB) of BJT. The following table illustrates different modes of BJT.

MODE	EB Junction	CB Junction
Cut-off	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward
Reverse active	Reverse	Forward

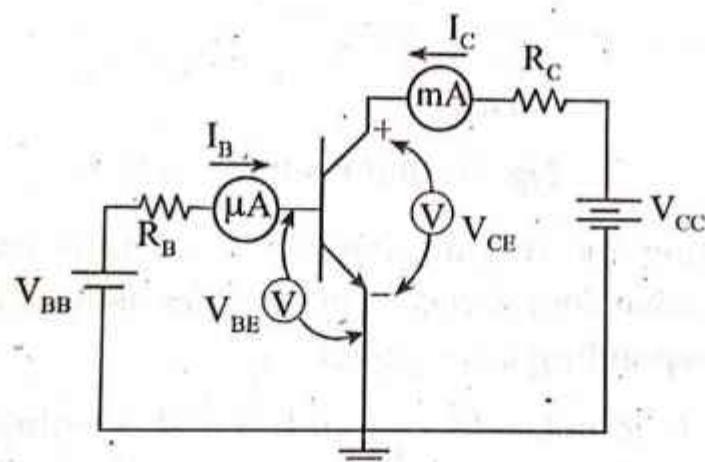
The cutoff mode and saturation mode are used for making switches and logic gates. The active mode is used for making amplifier.

### Transistor circuit configuration:

Configuration simply means arrangement of input and output terminals and is related to investigating transistor behavior based on arrangement. This contains the transistor characteristics based on where the input is applied and where the output is taken from. Transistor can be configured in three ways:

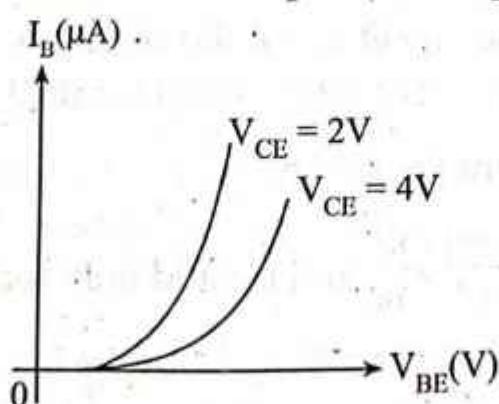
- i. Common Emitter Configuration
- ii. Common Base Configuration
- iii. Common Collector Configuration

#### i. Common Emitter Configuration:



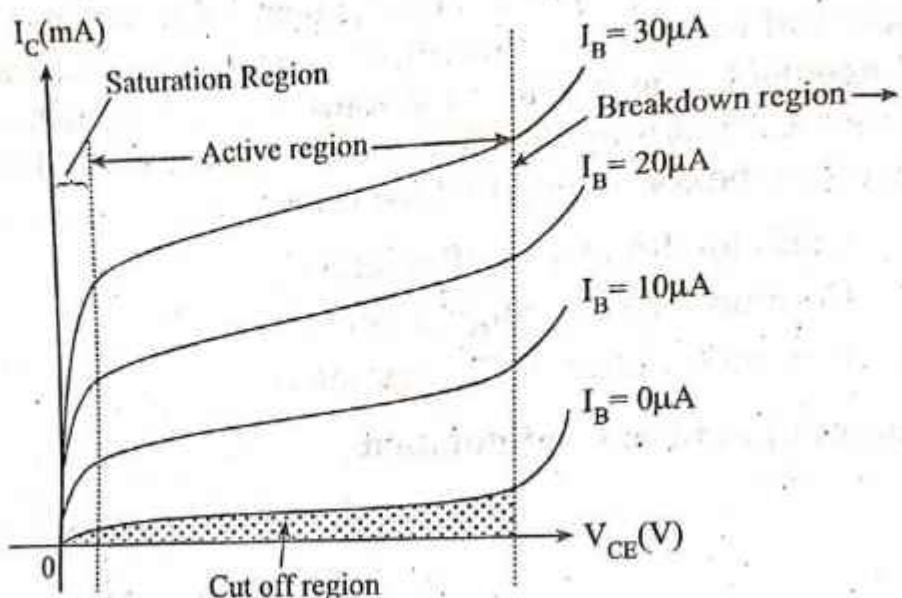
*Fig. Circuit to Study Characteristics of CE Configuration*

For this configuration, the input voltage is applied to the base and the output is taken at the collector and the emitter terminal is common to both input and output.



*Fig. Input Characteristics*

To observe input characteristics of common emitter configuration,  $V_{CE}$  is held constant,  $V_{BE}$  is set at convenient level and the corresponding  $I_B$  is recorded. The graph almost resembles with the I-V characteristic curve of forward-biased diode.



*Fig. Output Characteristics*

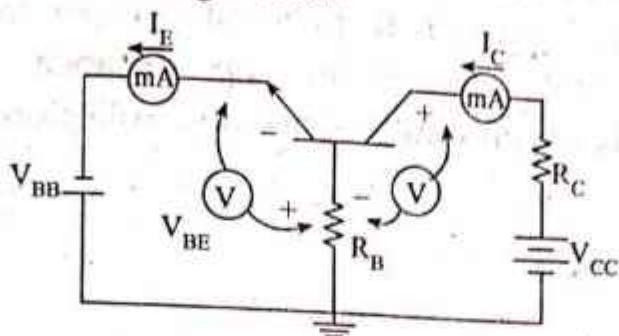
For plotting the output characteristics,  $I_B$  is maintained at several convenient levels, whereas  $V_{CE}$  is adjusted in steps and corresponding  $I_C$  are noted.

Because,  $I_E$  is not held constant, the shortening of distance between depletion regions draws more charge carriers from the emitter to collector. So, although  $I_B$  is constant,  $I_C$  increases to some extent with increasing  $V_{CE}$  causes the slope of common-emitter output characteristics. This slope is sometimes formed as early effect. On extension of slope line towards left, they meet at a point on the horizontal scale. The voltage at this point of intersection is called early voltage.

So, the dc current gain is given by

$$\beta = \frac{\text{output current}}{\text{input current}} = \frac{I_C}{I_B} \text{ and is valid only for active region}$$

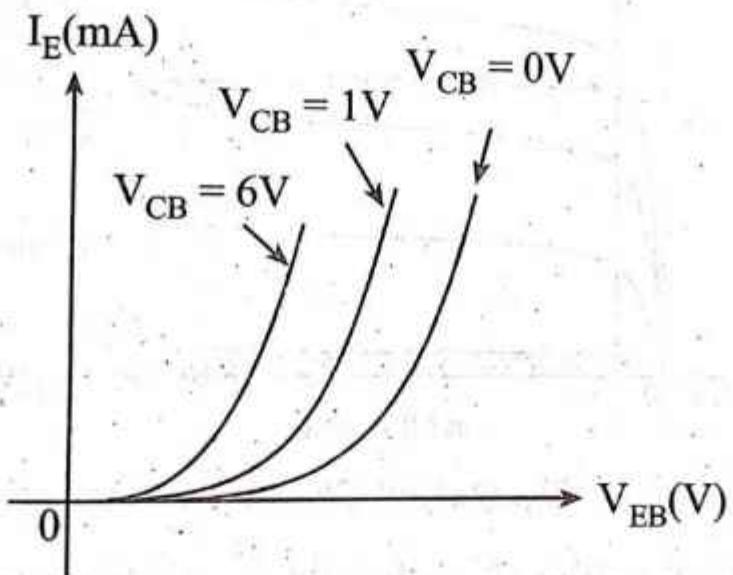
## ii. Common Base Configuration



*Fig. Circuit to Study Characteristics of CB Configuration*

The above diagram shows that a npn transistor is configured with its base terminal common to both the input terminals and output terminals.

### Input characteristics



*Fig. Input Characteristics*

To investigate the input characteristics, the output voltage  $V_{CB}$  is kept constant and the input voltage is set at convenient levels. At each voltage level, the corresponding input current is recorded.

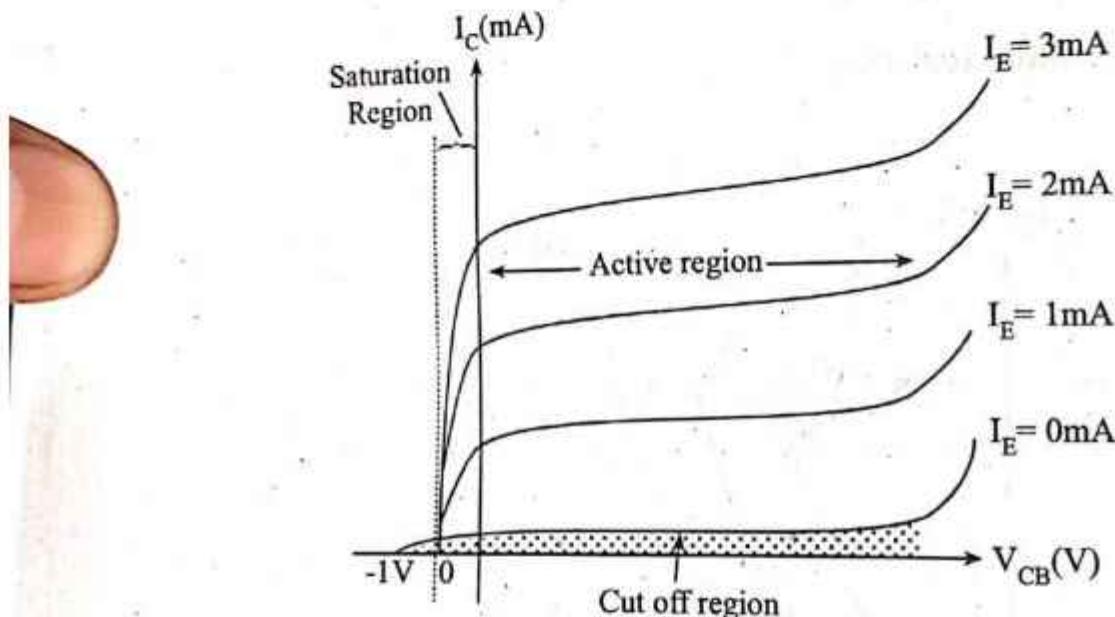
For a given input voltage  $V_{EB}$ , more input current flows when higher level of collector base voltage is used. This is because

larger collector-base voltages cause the depletion region at the collector base junction to penetrate deeper into the base of transistor, thus shortening the distance and reducing resistance between emitter-base and collector-base depletion regions.

**Current gain;**

$$\alpha = \frac{I_C}{I_E} \Rightarrow I_C = \alpha I_E$$

### Output characteristics

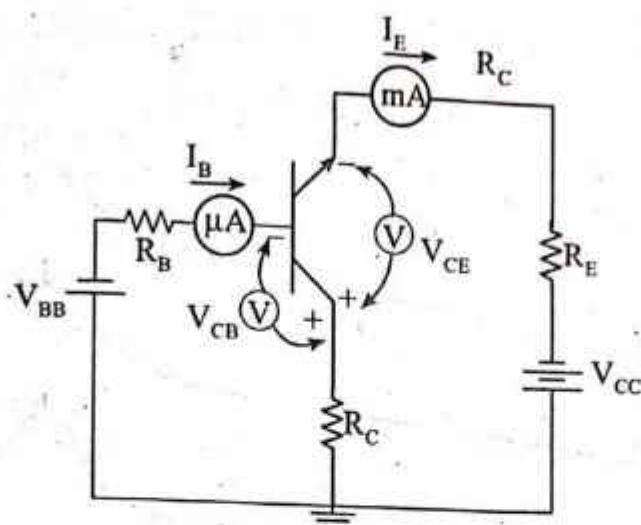


**Fig. Output Characteristics**

For plotting output characteristic,  $I_E$  is held constant and the corresponding  $I_C$  values are noted for  $V_{CB}$  adjusted in convenient steps.

When  $V_{CB}$  is zero,  $I_C$  still flows. This is because even when the externally applied voltage is zero, there is still a barrier voltage existing at the collector base junction and this assists flow of  $I_C$ . And, to stop the flow of charge carriers, the collector base junction has to be forward biased.

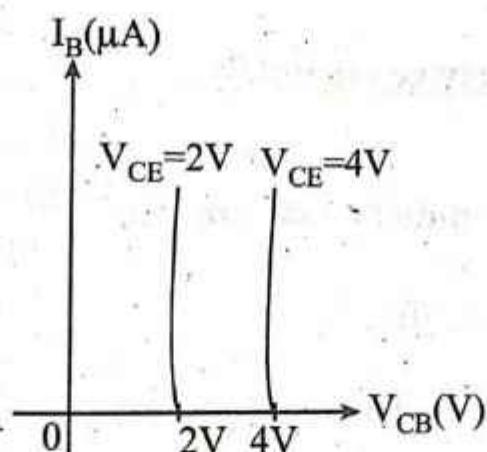
### iii. Common collector configuration:



*Fig. Circuit to Study Characteristics of CC Configuration*

The circuit arrangement in figure above shows that the collector is common to both the input and the output terminal.

#### Input characteristics:

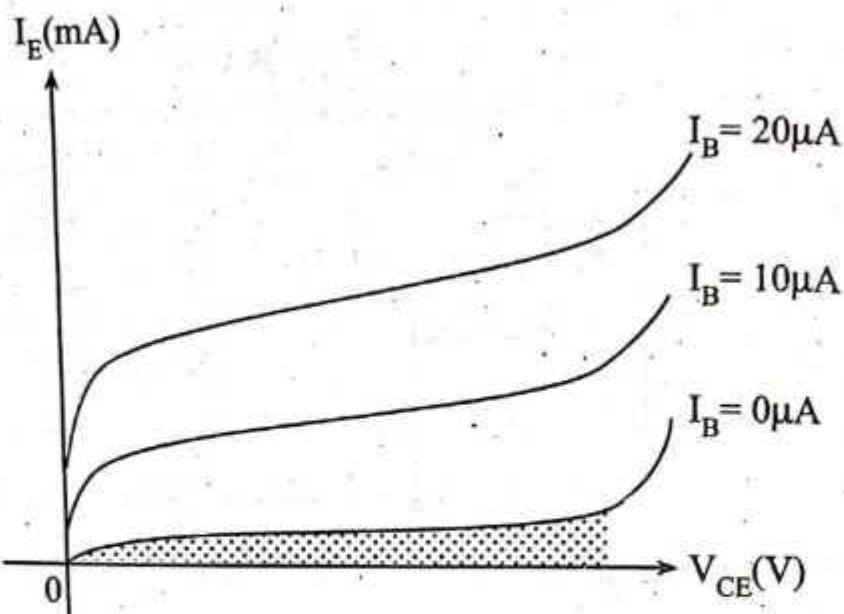


*Fig. Input Characteristics*

The common collector input characteristics are quite different from either common base or common-emitter configuration. The difference is due to the fact that the input voltage is largely determined by the output voltage  $V_{CE}$ . i.e.

$$V_{CE} = V_{CB} + V_{BE} \text{ and, } V_{BE} = V_{CE} - V_{CB}$$

### Output characteristics:



*Fig. Output Characteristics*

The output characteristics are a plot of emitter current  $I_E$  Vs collector-emitter voltage  $V_{CE}$  for several constant levels of base current,  $I_B$ .

#### Relationship between $\alpha$ and $\beta$ :

We have,

From common emitter configuration,

$$\beta = \frac{I_C}{I_B} \dots\dots\dots (i)$$

And, from common base configuration

$$\alpha = \frac{I_C}{I_E} \dots\dots\dots (ii)$$

Moreover, for a transistor,

$$I_E = I_B + I_C$$

$$\text{or, } \frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

$$\text{or, } \frac{1}{\alpha} = \frac{1}{\beta} + 1 \quad \therefore \boxed{\beta = \frac{\alpha}{1 - \alpha}} \text{ and } \boxed{\alpha = \frac{\beta}{\beta + 1}}$$

## 2.1 Operation of npn-transistor in Active Mode (Normal Mode)

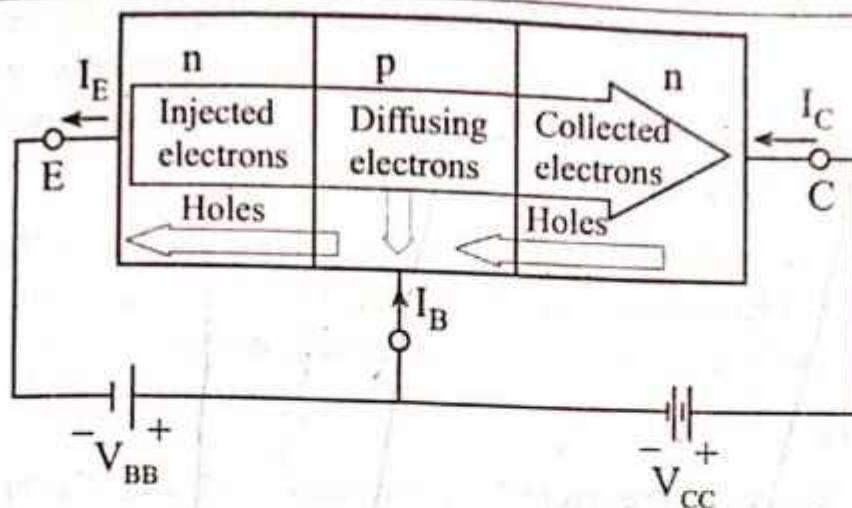


Fig.2.1 Operation of npn in Active Mode

For normal operation, base-emitter junction is forward-biased (i.e. base is more positive with respect to emitter) and the base collector junction is reverse-biased (base is less positive with respect to collector).

The forward bias at emitter-base junction reduces its barrier potential and as a result, electrons from emitter flow into base. Holes also flow from p-type base into n-type region. But, since the base region is much lightly doped than emitter, large numbers of electrons are accumulated in base region, which could not recombine with holes of base region. These electrons behave like minority charge carriers for reverse biased collector-base junction. Hence, they flow into collector region as minority carrier current. The reverse bias at the collector-base junction causes collector-base depletion layer to penetrate deeper into base region. Thus, the thin base region becomes thinner. As, a result, the electrons emitted from emitter region into base region almost immediately reaches the collector base junction where larger positive collector voltage is present, causing almost all of these electrons to cross collector-base junction and flow into collector region as collector current.

Due to this phenomenon, more than 99% of emitter current becomes collector current and very few electrons recombine with holes to give rise to base current. Some of the electrons that are diffused from emitter into base recombine with the majority carriers of the base. The external power supplies the holes lost due to recombination process.

The base current  $I_B$  constitutes the current  $I_{B1}$  due to the holes diffused from base into emitter and the current  $I_{B2}$  due to the electron hole recombination process in the base.

$$I_B = I_{B1} + I_{B2}$$

The direction of current is shown in fig 2.1 and it is opposite to the flow of electrons. Now from above explanation and figure we have

$$I_E = I_B + I_C$$

$$\text{or, } 100\% \text{ of } I_E = 1\% \text{ of } I_E + 99\% \text{ of } I_E$$

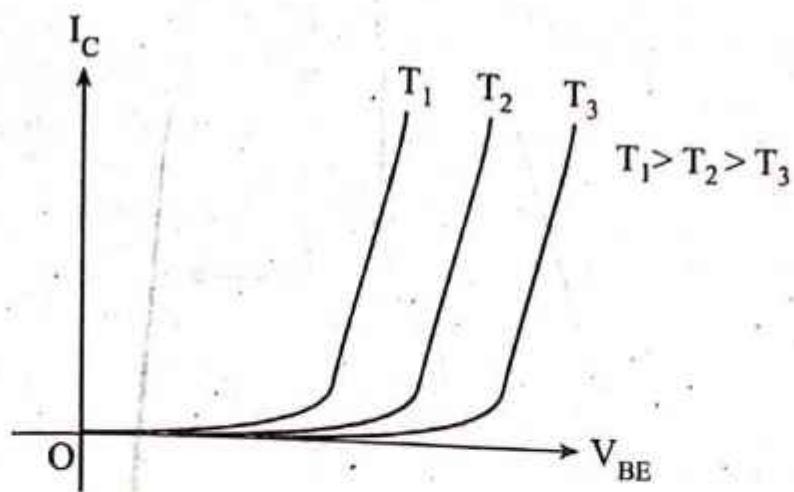
## 2.2 Graphical Representation of Transistor Characteristics

Figure shows the  $I_C-V_{BE}$  characteristics, which is the exponential relationship and given by

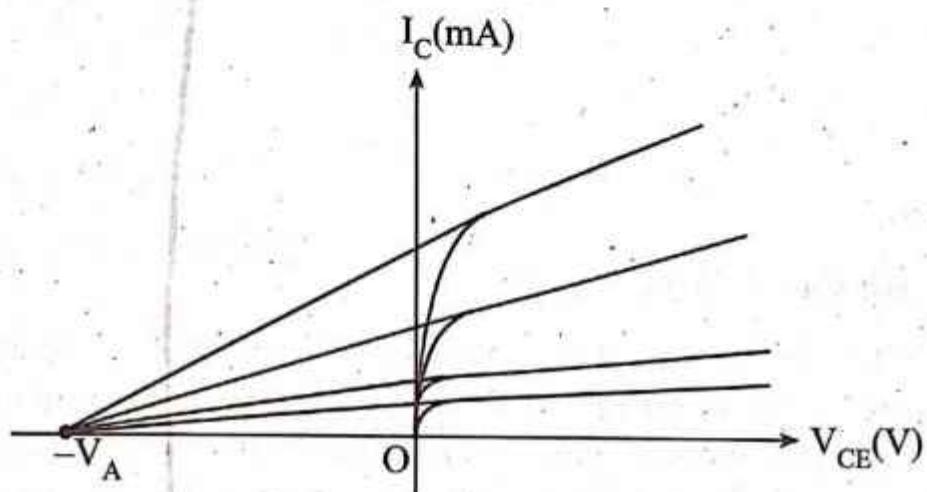
$$I_C = I_s e^{V_{BE}/V_T}$$

It is identical to the diode i-v relationship except for the value of constant  $\eta$ . The  $I_E-V_{BE}$  and  $I_B-V_{BE}$  characteristics are also exponential but with different scale currents,  $I_s/\alpha$  for  $I_E$  and  $I_s/\beta$  for  $I_B$ . For  $V_{BE}$  smaller than about 0.5 V, the current is negligibly small.

The voltage across the emitter base junction decreases by about 2 mV for each rise of  $1^\circ\text{C}$  in temperature, provided that the junction is operating at constant current. Temperature dependence figure is shown below:



*Fig.2.2 (a) Effect of temperature on the characteristics curve*



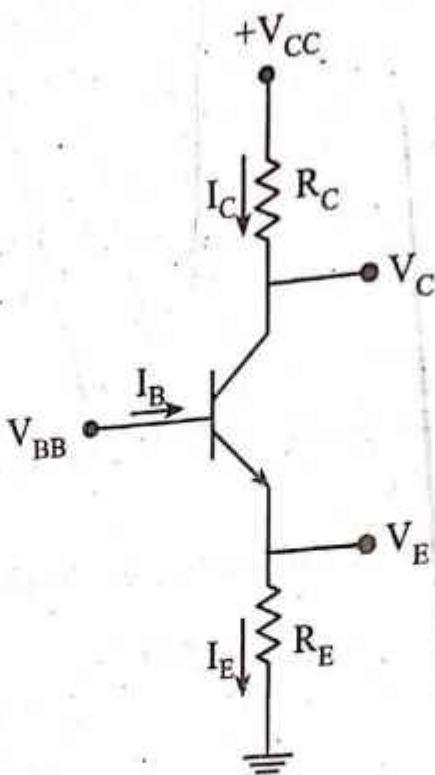
*Fig.2.2 (b) Characteristics curve of a practical BJT*

The voltage  $V_A$ , a positive number, is a parameter for the particular BJT, with typical values in the range of 50 V to 100 V. It is called the Early voltage.

### 2.3 Analysis of Transistor Circuits at DC

Analyze the following circuit given  $V_{CC} = 10V$ ,  $R_C = 4.7K\Omega$ ,  $R_E = 3.3K\Omega$  and  $\beta = 100$  for following different cases.

- i. Case I: When  $V_{BB} = 0V$
- ii. Case II: When  $V_{BB} = 4V$
- iii. Case III: When  $V_{BB} = 6V$



**Solution:**

**For Case I: When  $V_{BB} = 0V$**

Since the base is at zero volts and the emitter is connected to ground through  $R_E$ , the emitter-base junction cannot conduct and the emitter current is zero. Also, the collector-base junction cannot conduct since the n-type collector is connected through  $R_C$  to the positive power supply while the p-type base is at ground. It follows that the collector current will be zero. The base current will also have to be zero, and the transistor is in the cutoff mode of operation.

The emitter voltage will obviously be zero, while the collector voltage will be equal to +10V, since the voltage drop across  $R_C$  is zero.

$$\text{i.e. } I_B = I_C = I_E = 0 \text{ & } V_{CE} = V_{CC} = 10 \text{ V}$$

**For Case II: When  $V_{BB} = 4V$**

$$V_E = V_{BB} - V_{BE} = 4 - 0.7 = 3.3 \text{ V}$$

$$I_E = \frac{V_E - 0}{R_E} = \frac{3.3}{3.3} = 1 \text{ mA}$$

Since the collector is connected through  $R_C$  to the  $+V_{CC}=10V$  power supply, the collector voltage should be higher than the base voltage for active mode. We have

$$\alpha = \frac{\beta}{\beta+1} = \frac{100}{101} = 0.99$$

$$I_C = \alpha I_E = 0.99 \text{ mA}$$

$$V_C = V_{CC} - I_C R_C = 10 - 0.99 \cdot 4.7 = 5.3V$$

Since the base is at  $+4V$ , the collector-base is reverse biased by  $5.3 - 4 = 1.3V$ , and the transistor is in active mode of operation.

$$I_B = \frac{I_E}{\beta+1} = \frac{0.99}{101} = 0.01 \text{ mA.}$$

**For Case III:** When  $V_{BB} = 6V$

Assuming active-mode operation, we have

$$V_E = V_{BB} - V_{BE} = 6 - 0.7 = 5.3V$$

$$I_E = \frac{V_E}{R_E} = \frac{5.3}{3.3} = 1.6 \text{ mA}$$

$$V_C = V_{CC} - I_C R_C = 10 - 1.6 \cdot 4.7 = 2.48V \quad [I_C \approx I_E]$$

Since the collector voltage calculated appears to be less than the base voltage by  $3.52V$ , it follows that our assumption of active mode operation is incorrect. In fact, the transistor has to be in the saturation mode. Now, we have

$$V_E = V_{BB} - V_{BE} = 6 - 0.7 = 5.3V$$

$$I_E = \frac{V_E}{R_E} = \frac{5.3}{3.3} = 1.6 \text{ mA}$$

$$V_C = V_{CEsat} + V_E = 5.3 + 0.2 = 5.5V \quad [V_{CEsat} = 0.2 \text{ V}]$$

$$I_C = \frac{V_{CC} - V_C}{R_C} = \frac{10 - 5.5}{4.7} = 0.96 \text{ mA}$$

$$I_B = I_E - I_C = 1.6 - 0.96 = 0.64 \text{ mA}$$

Thus the transistor is operating at a forced  $\beta$  of

$$\beta_{forced} = \frac{I_C}{I_B} = \frac{0.96}{0.64} = 1.5$$

## 2.4. Transistor as an Amplifier

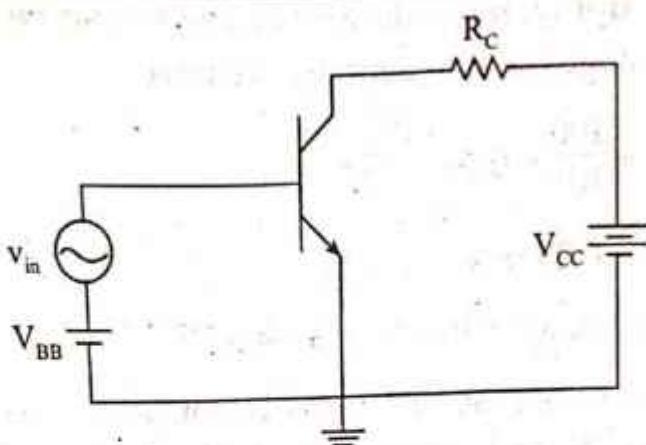


Fig. 2.4 Basic Common Emitter Amplifier

To operate as an amplifier a transistor must be in active region. Consider the basic common-emitter circuit given as an amplifier circuit as shown in fig 2.4.

Here, we know that in active mode of operation  $I_C$  depends upon the magnitude of emitter current  $I_E$  (& not upon  $V_{CE}$ ) which in turn depends upon the forward bias voltage  $V_{BE}$ . That mean  $I_C$  depends upon the magnitude of  $V_{BE}$ .

For the dc condition we have

$$I_C = I_S e^{(V_{BE}/V_T)}$$

And,

$$I_E = \frac{I_C}{\alpha}; I_B = \frac{I_C}{\beta}$$

From circuit diagram we have,

$$V_C = V_{CE} = V_{CC} - I_C R_C$$

Here  $V_C > V_B$  for active mode

The total instantaneous base emitter voltage  $v_{BE}$  becomes

$$v_{BE} = V_{BE} + v_{be}$$

And corresponding collector current  $i_c$  is given by

$$i_c = I_S e^{(V_{BE}/V_T)}$$

$$I_C + i_c = I_S e^{((V_{BE} + v_{be})/V_T)}$$

$$= I_C e^{(v_{be}/V_T)}$$

Expanding the exponential term and neglecting higher terms we have

$$I_C + i_c \approx I_C(1 + \frac{V_{be}}{V_T})$$

$$I_C + i_c = I_C + I_C \frac{V_{be}}{V_T}$$

Comparing dc to dc and ac to ac quantities we have

$$I_C = I_C \text{ and}$$

$$i_c = I_C \frac{V_{be}}{V_T}$$

$$\boxed{\frac{i_c}{V_{be}} = \frac{I_C}{V_T} = g_m} = \text{mutual conductance} = \text{trans-conductance}$$

$$\text{Thus } i_c = g_m V_{be}$$

Similarly, we have total base current

$$i_B = I_B + i_b = \frac{I_C}{\beta} + \frac{i_c}{\beta}$$

Comparing ac to ac

$$i_b = \frac{i_c}{\beta} = \frac{g_m V_{be}}{\beta}$$

$$\boxed{\frac{V_{be}}{i_b} = \frac{\beta}{g_m} = r_n \text{ or } r_b}$$

Also

$$\boxed{r_n = \frac{\beta V_T}{I_C} = \frac{V_T}{I_B} = \frac{\beta}{g_m}}$$

$r_n$  = base ac resistance or small signal ac input resistance between base and emitter looking into base.

**Total emitter current**

$$i_E = i_e + I_E = \frac{i_c}{\alpha} + \frac{I_C}{\alpha}$$

## Comparing ac to ac quantities

$$i_e = \frac{i_c}{\alpha} = \frac{g_m V_{be}}{\alpha}$$

$$\frac{V_{be}}{i_e} = \frac{\alpha}{g_m} = r_e$$

$r_e$  = emitter ac resistance or small signal ac resistance between base and emitter looking into emitter

Also

$$r_e = \frac{V_T}{I_E} \quad [r_e = \frac{\alpha}{g_m} = \frac{\alpha V_T}{I_C} = \frac{V_T}{I_E}]$$

$$\text{Thus } r_e = \frac{\alpha}{g_m} = \frac{1}{g_m} \quad [\alpha \approx 1]$$

$$r_e = \frac{\beta}{(\beta + 1)} \frac{1}{g_m} = \frac{r_n}{(\beta + 1)} \quad [\alpha = \frac{\beta}{\beta + 1}]$$

$$r_n = (\beta + 1)r_e$$

### For voltage gain

From figure

$$v_{CE} = V_{CC} - i_C R_C$$

$$V_{CE} + v_{ce} = V_{CC} - (i_c + I_C) R_C$$

### Comparing ac to ac quantities

$$v_{ce} = -i_C R_C = -g_m v_{be} R_C$$

$$\frac{v_{ce}}{v_{be}} = \frac{\text{output voltage}}{\text{input voltage}} = -g_m R_C$$

Therefore voltage gain of an amplifier ( $A_v$ ) =  $-g_m R_C$ . The negative sign indicates that the output signal voltage is 180° out of phase with respect to input ac signal voltage.

Similarly current gain ( $A_i$ )

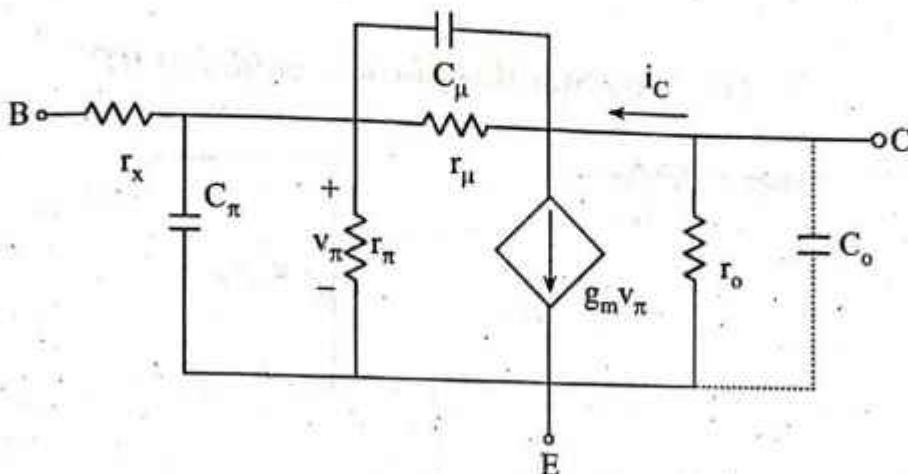
$$A_i = \frac{i_c}{i_b} = -g_m r_n = -\beta$$

## 2.5 Small Signal Equivalent Circuit Models

A bipolar junction transistor (BJT) has been modeled either as  
 (i)  $\pi$ -model (ii) T-model or (iii) h-model whenever ac analysis is performed.

### i. $\pi$ -model :

The  $\pi$ -model of a simple BJT transistor for ac analysis is shown in figure below:



*Fig.2.5 (a) Complete or High frequency hybrid  $\pi$ - model of BJT*

Where,

$r_x$  = lump resistance  $\approx 20\Omega$  (few tens of  $\Omega$ )

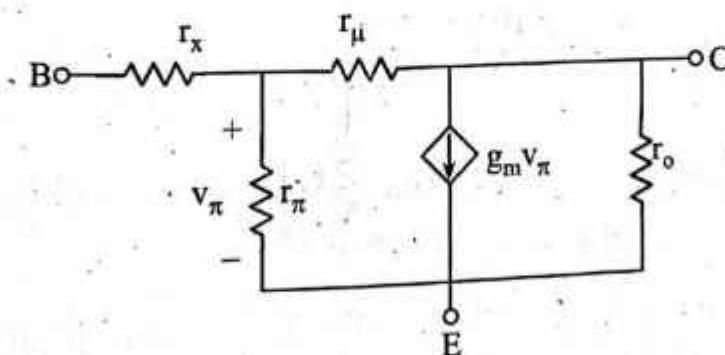
$r_\pi$  =  $2\text{ K}\Omega$

$r_0$  =  $100\text{ K}\Omega$  (usually the effect of  $r_0$  is neglected)

$r_\mu$  =  $40\text{ M}\Omega$  (usually its effect is also negligible)

$C_\mu$  = few pF  $\approx 5\text{ pF}$  (junction capacitance between collector and base due to reversed biased CB junction)

$C_\pi$  = few tens of pF  $\approx 30\text{ pF}$  (diffusion capacitance developed due to storage of charge diffused from emitter).



*Fig. 2.5(b) Low frequency hybrid  $\pi$  model of BJT*

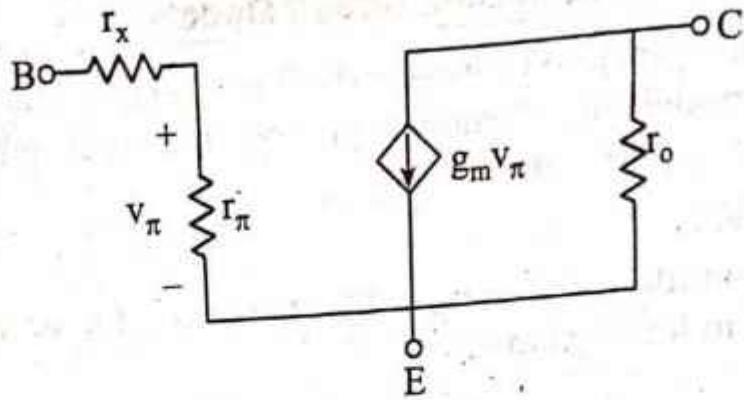


Fig. 2.5(c) Simple hybrid  $\pi$ -model of BJT

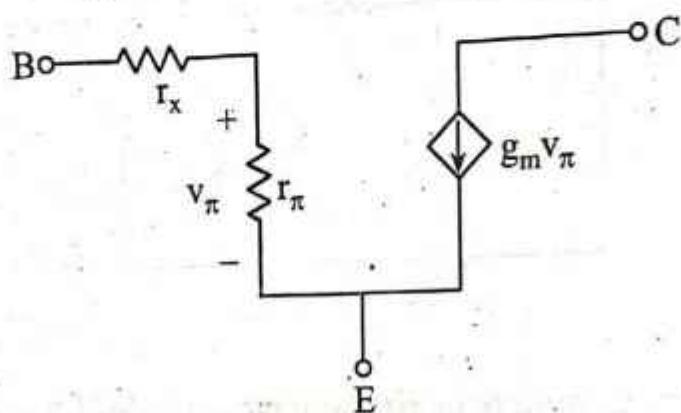


Fig. 2.5(d) Simple  $\pi$ -model (ignoring the effect of  $r_o$ )

## ii. T-model:

The T-model developed for BJT can be drawn as:

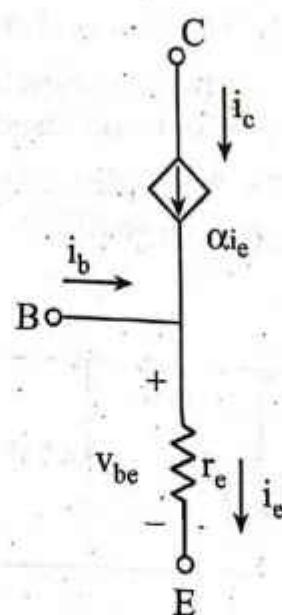


Fig. 2.5(e) T-model of BJT

## 2.6 Graphical Load Line Analysis

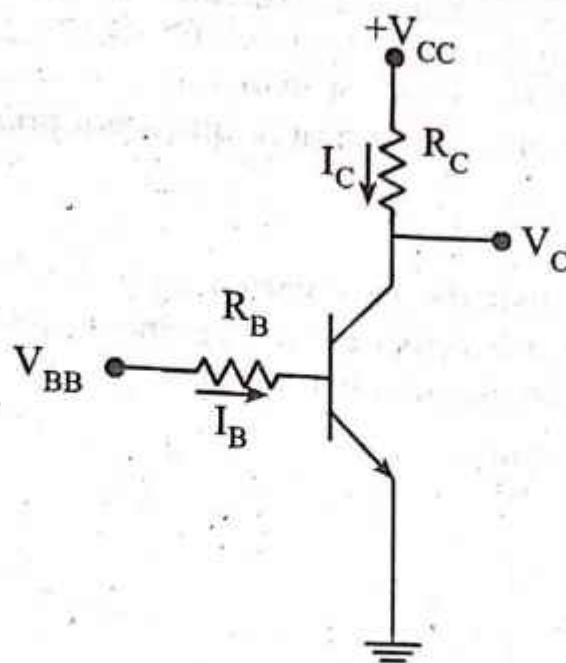


Fig.2.6 (a) Basic Circuit to Study Load Line

The Circuit to study load line is shown in fig.2.6 (a).

Consider output characteristic curve of common emitter configuration as:

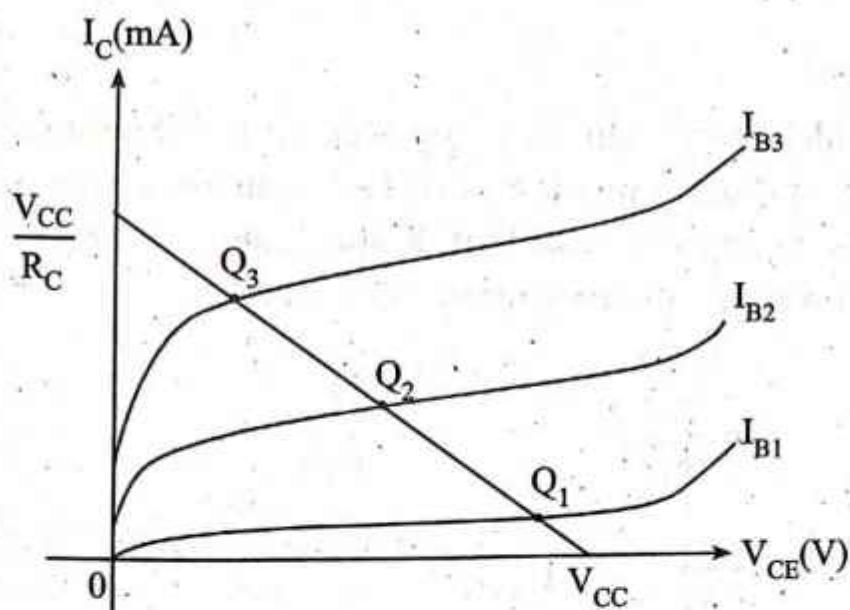


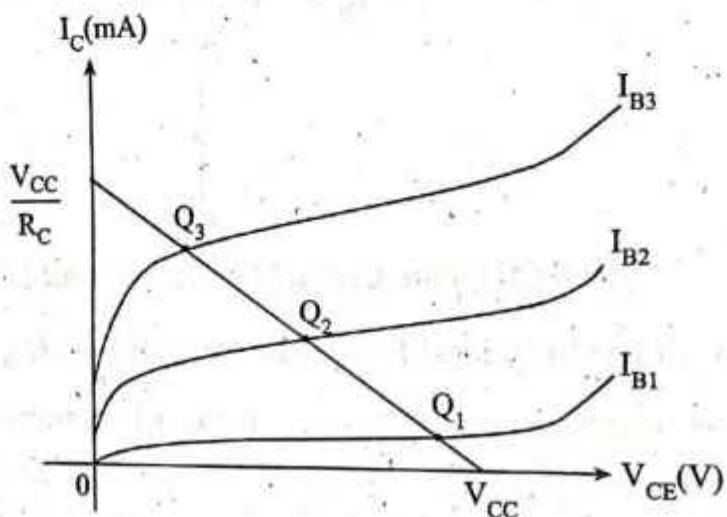
Fig.2.6 (b) Output Characteristics showing load line and operating (Q) points

The straight line is called load line and is guided by the expression  $V_{CE} = V_{CC} - I_C R_C$  such that  $V_{CE} = V_{CC}$  at  $I_C = 0$  and

$I_C = V_{CC}/R_C$  at  $V_{CE} = 0$ . Load line is defined as a straight line joining the maximum current that can flow through the device and the maximum voltage drop across the device. The point of intersection of load line and characteristics curve is known as operating point or quiescent point (Q-point).

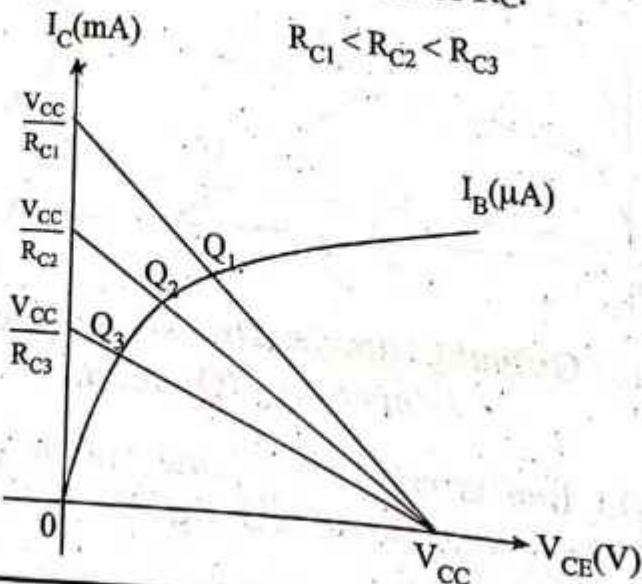
### Case I:

Consider that the  $I_B$  is varied, and then the operating point shifts towards upper left as  $I_B$  is increased from  $I_{B1}$  to  $I_{B2}$  or  $I_{B3}$ , as shown in diagram below:



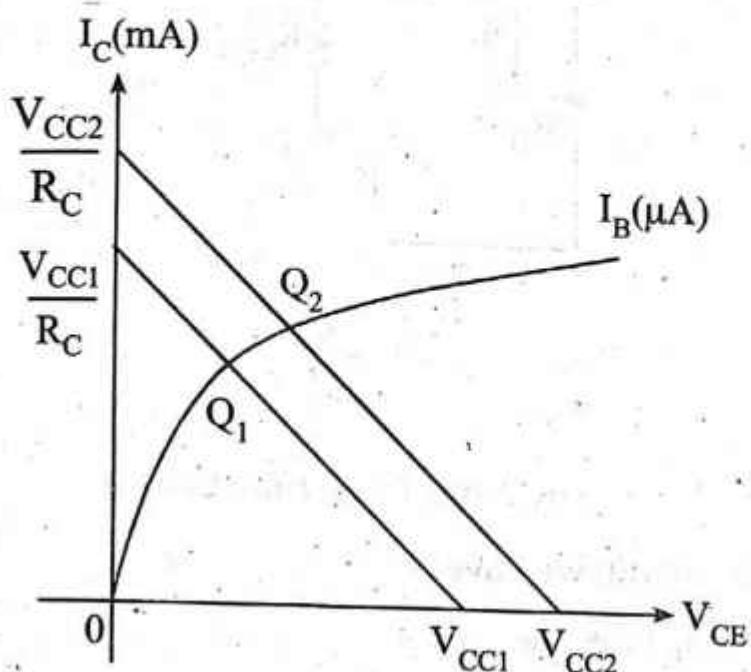
### Case II:

Consider, the resistor  $R_C$  is replaced with different values and the operating points are observed with base current  $I_B$  and supply voltage  $V_{CC}$  constant. In this case, Q-point shifts more to left with the increase in the value of  $R_C$ .



### Case III

Consider that the supply voltage is varied from a value to another value. At that case, Q-point shifts to right with the increase in voltage with the slope of line remaining constant and equal to  $-1/R_C$ .



## 2.7 Biasing BJT for Discrete Circuit Design

Transistors should properly bias in order to utilize device either as an amplifier or switching logic. A desirable dc voltage and dc current are applied to set the operating points or bias points such that improper operation of transistor may be avoided.

There are various ways to fix an operating point of a transistor, which are discussed as below:

- i. Fixed biasing method
- ii. Emitter feedback biasing method
- iii. Collector feedback biasing method
- iv. Voltage divider biasing method

### i. Fixed Biasing Method:

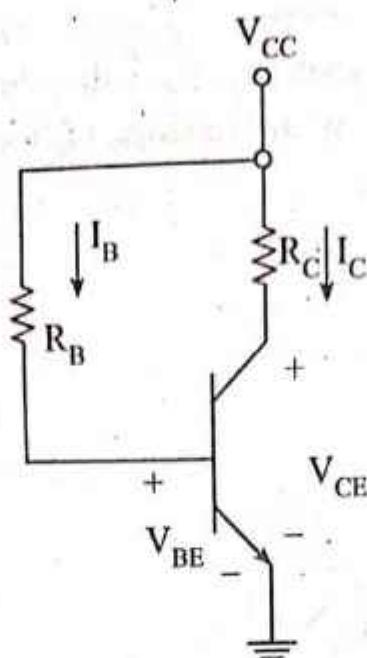


Fig. 2.7(a) Fixed Bias Circuit

From the circuit, we have,

$$V_{CC} = I_B R_B + V_{BE}$$

$$\text{or, } I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

Since, the supply voltage  $V_{CC}$ , the resistor  $R_B$  and the base-emitter voltage  $V_{BE}$  are constant, the current  $I_B$  is also constant and the network is called fixed bias circuit.

And, from the figure, we also have,

$$V_{CC} = I_C R_C + V_{CE}$$

$$V_{CE} = V_{CC} - I_C R_C$$

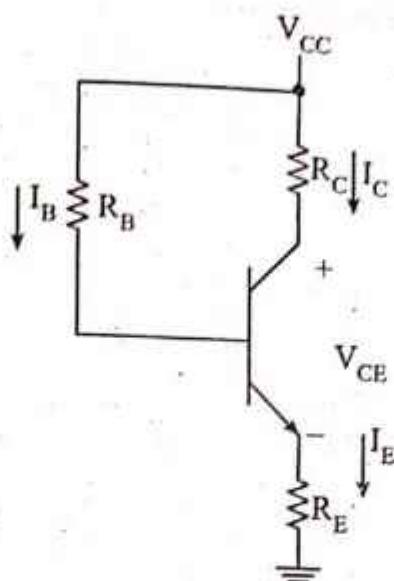
Moreover, we know that,  $I_C = \beta I_B$ .

The value of the required base current is determined from the load line at the selected Q point. As we know for a given Q point the base current  $I_B$  is constant. So this biasing method is also called "fixed biasing".

This method of biasing is the simplest and the worst method to bias a transistor for linear operation because the Q point is

unstable for the temperature change and  $\beta$  change when the original transistors are replaced.

### ii. Emitter feedback biasing:



*Fig.2.7 (b) Emitter Feedback Bias Circuit*

The circuit diagram for the emitter feedback biasing is shown in fig 2.7(b).

This method of biasing is used to reduce instability of Q-point due to  $\beta$  and thermal changes. This circuit has more stable operating point than that of fixed biasing method.

From circuit we have

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

$$\text{or, } I_B R_B = V_{CC} - V_{BE} - I_E R_E \quad [\because I_C \approx I_E]$$

$$\text{or, } I_C \left( \frac{R_B}{\beta} + R_E \right) = V_{CC} - V_{BE} \quad [\because \frac{I_C}{\beta} = I_B]$$

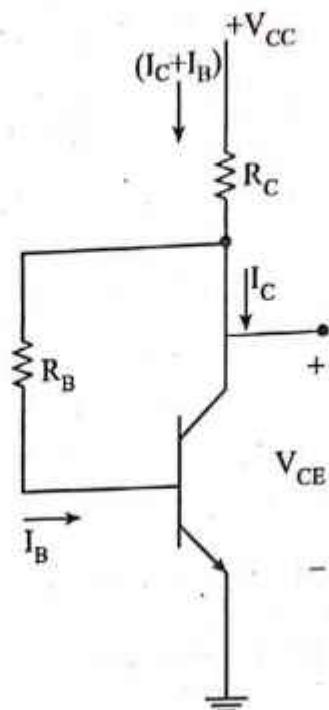
$$\therefore I_C = \frac{V_{CC} - V_{BE}}{(R_E + R_B/\beta)}$$

$$\text{And, } V_{CE} = V_{CC} - I_C (R_C + R_E)$$

From above, it is obvious that  $I_C$  depends upon  $\beta$ . To make  $I_C$  less or not dependent upon  $\beta$  it is necessary to make  $R_E$  very large. When  $R_E$  becomes very large it might take the Q point

to the saturation region which is highly undesirable. Since this method is also  $\beta$  sensitive it is also not a very good biasing method.

### iii. Collector Feedback Biasing:



*Fig.2.7(c) Collector Feedback Bias Circuit*

The circuit diagram for collector feedback biasing is shown in fig2.7(c).

The circuit has the base resistor  $R_B$  connected between transistor collector and base terminals, which significantly improves bias stability as compared to fixed bias method.

From the circuit, we have,

$$V_{CE} = I_B R_B + V_{BE}$$

$$\therefore I_B = \frac{V_{CE} - V_{BE}}{R_B}$$

$$\begin{aligned} \text{Also, } V_{CE} &= V_{CC} - I_C R_C - I_B R_C \\ &= V_{CC} - (I_C + I_B) R_C. \end{aligned}$$

If  $I_C$  increases, then the voltage drop across  $R_C$  increases, and hence,  $V_{CE}$  decreases. This decrease in  $V_{CE}$  results in decrease in

$I_B$  and also in  $I_C$  because  $I_C = \beta I_B$ . Thus, the current  $I_C$  tends to return towards its original level.

Now, we have,

$$V_{CC} = (I_C + I_B) R_C + I_B R_B + V_{BE}$$

$$\text{or, } V_{CC} = \left( I_C + \frac{I_C}{\beta} \right) R_C + \frac{I_C}{\beta} R_B + V_{BE}$$

$$\text{or, } I_C = \frac{V_{CC} - V_{BE}}{R_C \left( \frac{\beta + 1}{\beta} \right) + \frac{R_B}{\beta}}$$

From above relation it shows  $I_C$  depends upon  $\beta$  but it is less sensitive than in emitter feedback biasing method. For design  $R_B$  is selected as

$$R_B = \beta R_C$$

#### iv. Voltage Divider Biasing (Universal Biasing):

It is also called  $\beta$ -independent biasing method. It is the most stable biasing circuit among the discussed methods for various temperature conditions and  $\beta$  value of transistor.

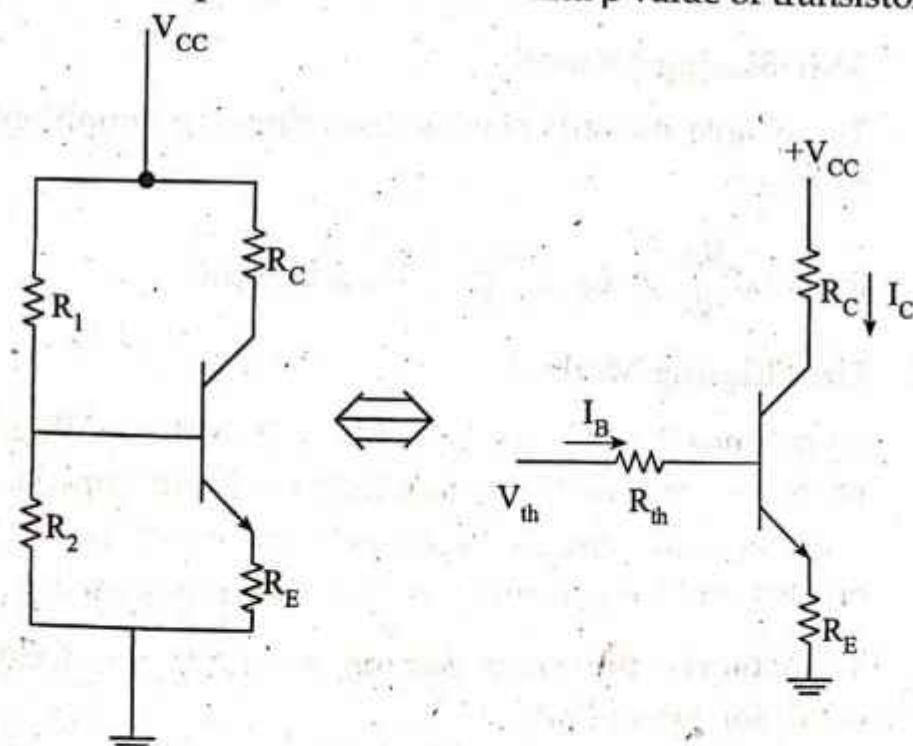


Fig.2.7 (d): Voltage divider bias circuit and its equivalent Thevenin circuit

From Thevenin's theorem, we get,

$$R_{th} = R_1 // R_2 = \frac{R_1 R_2}{R_1 + R_2} \quad \text{and} \quad V_{th} = \frac{R_2}{R_1 + R_2} \times V_{CC}$$

$$\text{So, } V_{th} = I_B R_{th} + V_{BE} + I_E R_E \quad [ I_E \approx I_C \text{ & } I_B = \frac{I_C}{\beta} ]$$

or,  $I_C = \frac{V_{th} - V_{BE}}{(R_E + R_{th}/\beta)}$

$$\text{Also, } V_{CE} = V_{CC} - I_C (R_C + R_E)$$

Since,  $R_{th}/\beta \ll R_E$ , the expression can be reduced to

$I_C = \frac{V_{th} - V_{BE}}{R_E}$  which shows that the collector current,  $I_C$  is almost independent of  $\beta$ .

The voltage divides biasing method can be designed in two ways:

- Stiff Biasing Method and
  - Firm Biasing Method
- a. **Stiff Biasing Method:**

To achieve the stiff biasing the following conditions are fulfilled:

$$R_E \geq 100 \frac{R_{th}}{\beta} \text{ i.e. } R_{th} \leq \frac{\beta R_E}{100} \Rightarrow R_{th} \leq 0.01 \beta R_E$$

- b. **Firm Biasing Method:**

Sometimes in stiff biasing method the value of  $R_1$  and  $R_2$  becomes very small due to which the input impedance of the transistor circuit becomes very small and it may creates problems. In this case firm biasing is used.

To achieve, the firm biasing method, the following condition is fulfilled:

$$10 \frac{R_{th}}{\beta} \leq R_E \text{ i.e. } R_{th} \leq 0.1 \beta R_E$$

When  $V_{th} \gg V_{BE}$ ;  $(V_{th} - V_{BE})$  becomes almost constant for this achievement, the following two guidelines are used.

### Guideline No. 1

Assume,

$$V_{th} = \frac{1}{3} V_{CC} \text{ and } V_{RC} = \frac{1}{3} V_{CC}$$

Which leads to  $R_1 = 2R_2$

or,  $R_{th} = \frac{2}{3} R_2$  biasing becomes

$$\therefore \text{For firm biasing, } V_{th} = \frac{R_2}{R_1 + R_2} \times V_{CC}$$

$$\text{or, } \frac{1}{3} = \frac{R_2}{R_1 + R_2}$$

$$\text{And, } R_{th} = 0.1 \beta R_E = \frac{2}{3} R_2$$

And for stiff biasing  $\Rightarrow R_1 = 2R_2$

$$R_{th} = 0.01 \beta R_E = \frac{2}{3} R_2$$

### Guideline No. 2

Assume

$$V_{CE} = 0.5 V_{CC}$$

$$V_{RE} = V_E = 0.1 V_{CC}$$

$$V_{RC} = 0.4 V_{CC}$$

Because  $V_E = 0.1V_{CC}$  which means it is much smaller compared to  $V_{CC}$ . Hence,  $V_{th}$  is also much smaller than  $V_{CC}$  and it leads to  $R_{th} = R_2$ . And biasing becomes,

$$R_{th} = 0.1 \beta R_E \approx R_2 \text{ for firm biasing}$$

$$R_{th} = 0.01 \beta R_E \approx R_2 \text{ for stiff biasing}$$

Note:

- Guideline No.1 is popular for low voltage power supply ( $V_{CC} \leq 10V$ )

- Guideline No. 2 is popular for high voltage power supply ( $V_{CC} \geq 15V$ )
- If the value of power supply  $V_{CC}$  is in between 10 V and 15 V then any of the guidelines can be used.

**Q.** Design a voltage divider bias circuit of common emitter that is independent of  $\beta$ .

Given  $V_{CC} = 12V$ ,  $I_E = 1\text{ mA}$  and  $\beta = 100$ .

**Solution:**

**Note:** Here,  $V_{CC}$  is in between 10 V and 15 V so in this case any guidelines can be used.

Using Guideline 1, we have,

$$V_{th} = \frac{V_{CC}}{3} = 4V$$

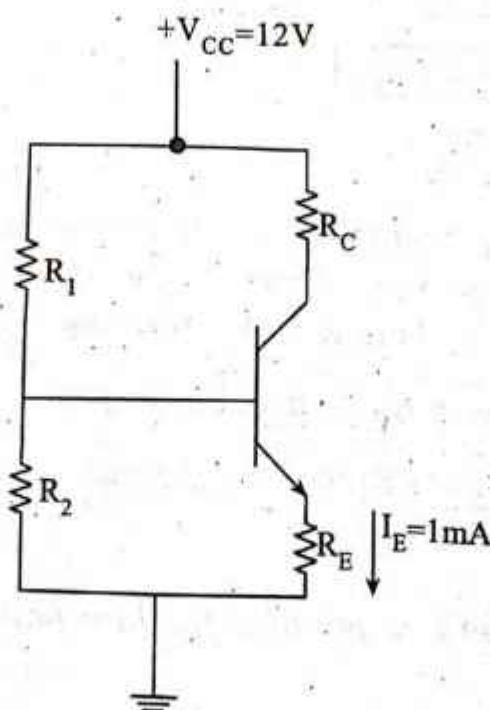
And,

$$V_{RC} = \frac{1}{3} V_{CC} = 4V$$

$$\text{So, } I_C R_C = V_{RC}$$

$$\text{or, } I_E R_C = V_{RC} \quad [\therefore I_C \approx I_E]$$

$$\text{or, } R_C = \frac{V_{RC}}{I_E} = \frac{4V}{1\text{mA}} = 4\text{ K}\Omega$$



Again, we have,

From stiff biasing method,

$$R_{th} = 0.01 \beta R_E$$

Converting Thevenin's equivalent of above figure and using KVL in input loop, we have,

$$V_{th} - V_{BE} = I_B R_{th} + I_E R_E$$

$$\text{or, } V_{th} - V_{BE} = \frac{I_E}{\beta + 1} \times 0.01 \beta R_E + I_E R_E$$

$$\text{or, } 4 - 0.7 = 1 \text{mA} \times \left( \frac{0.01\beta}{\beta + 1} + 1 \right) R_E$$

$$\therefore R_E = 3.3 \text{K}\Omega$$

Also,

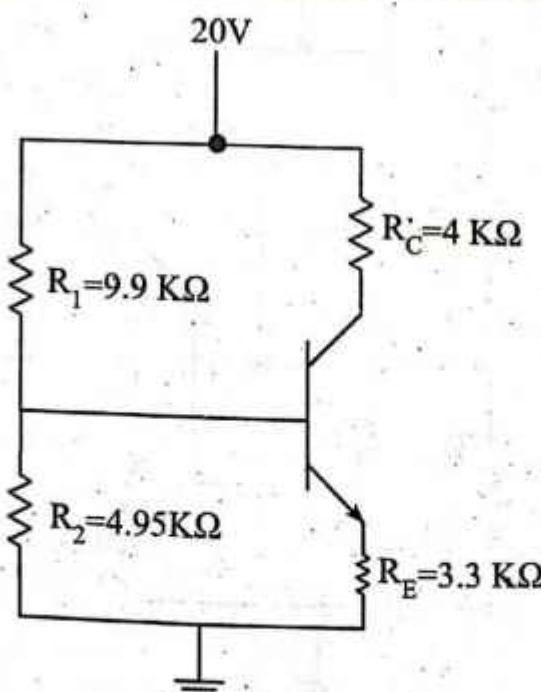
$$R_{th} = 0.01 \beta R_E = 3.3 \text{K}\Omega$$

$$\text{So, } R_{th} = \frac{2}{3} R_2 = 3.3 \text{K}\Omega$$

$$\therefore R_2 = 4.95 \text{ K}\Omega \text{ and,}$$

$$R_1 = 9.9 \text{ K}\Omega \quad [R_1 = 2R_2]$$

Hence  $R_1 = 9.9 \text{ K}\Omega$ ,  $R_2 = 4.95 \text{ K}\Omega$ ,  $R_C = 4 \text{K}\Omega$  and  $R_E = 3.3 \text{K}\Omega$



- Q.** Design  $\beta$ -independent dc biasing common emitter amplifier for which input resistance should be large. Use appropriate guideline. Given data:  $\beta=150$ ,  $I_C=10\text{mA}$ ,  $V_{CC}=20\text{V}$ .

**Solution:**

Since  $V_{CC} \geq 15\text{ V}$ ,

Using guideline 2, we have,

$$V_E = 0.1V_{CC}, V_{RC} = 0.4V_{CC}, V_{CE} = 0.5V_{CC}$$

Since input resistance should be large so we use firm biasing method, we have,

$$R_{th} = 0.1\beta R_E$$

$$R_{th} \approx R_2$$

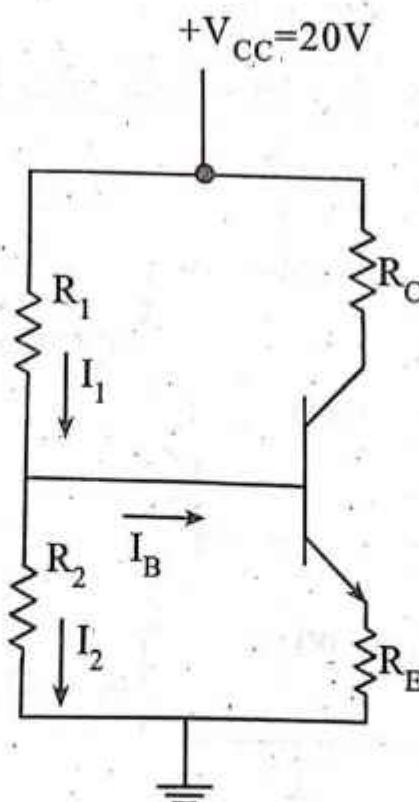
$$R_2 = 0.1\beta R_E$$

Now, we have,

$$V_E = I_E R_E$$

$$\text{or, } 2 = I_C R_E$$

$$R_E = 0.2 \text{ K}\Omega = 200 \Omega$$



Again,

$$I_B = \frac{I_C}{\beta} = \frac{10}{150} \text{ mA} = 0.067 \text{ mA}$$

But,

$$V_{RC} = I_C R_C$$

$$\therefore 8 = 10 \text{ mA} \times R_C$$

$$\therefore R_C = 800 \Omega$$

$$\text{Also, } R_2 = 0.1 \times 150 \times 200 \Omega = 3000 \Omega = 3 \text{ K}\Omega$$

From above figure

$$I_1 = I_B + I_2$$

$$V_B = I_2 R_2 = I_2 \times 3000 \Omega$$

We have,

$$V_B = V_{BE} + V_E = 0.7 + 2 = 2.7 \text{ V}$$

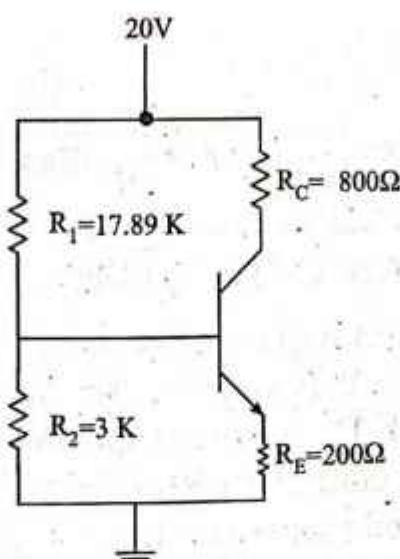
$$\therefore I_2 = \frac{V_B}{R_2} = \frac{2.7}{3000} = 0.9 \text{ mA}$$

Hence,

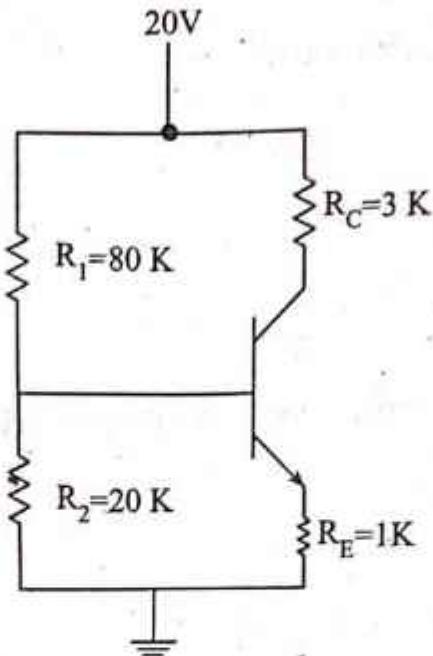
$$I_1 = I_B + I_2 = 0.9 + 0.067 = 0.967 \text{ mA}$$

And,

$$V_{R1} = V_{CC} - V_B \therefore R_1 = \frac{V_{R1}}{I_1} = \frac{(20 - 2.7) \text{ V}}{0.967 \text{ mA}} = 17.89 \text{ K}\Omega$$



**Q. Find quiescent point for the given circuit**



**Solution:**

We have,

$$R_{th} = R_1 // R_2 = 16 \text{ k}\Omega$$

$$V_{th} = \frac{R_2}{R_1 + R_2} \times V_{CC} = 4\text{V}$$

$$\therefore I_{CQ} = \frac{V_{th} - V_{BE}}{R_E + R_{th}/\beta} = 2.8 \text{ mA}$$

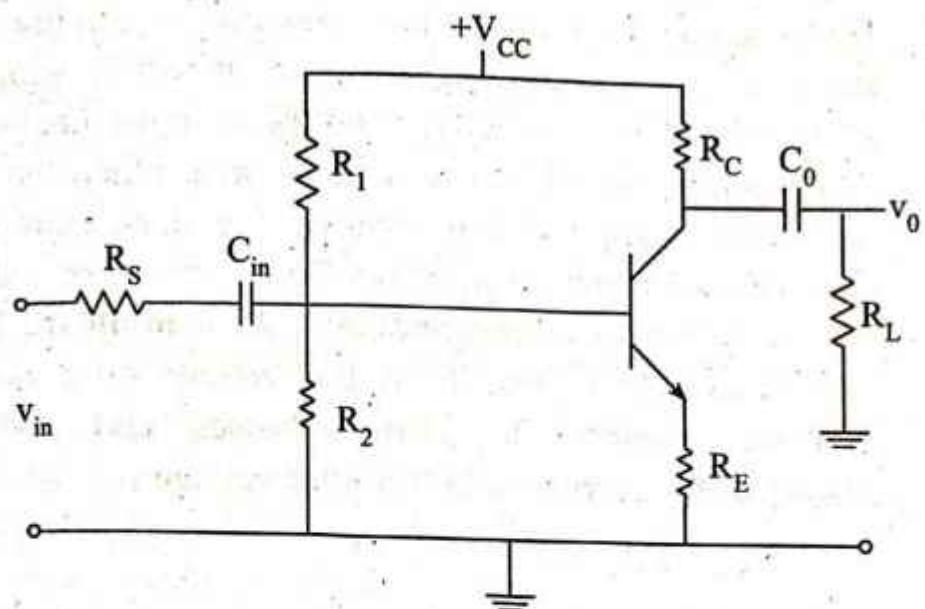
$$\begin{aligned} \text{And, } V_{CEQ} &= V_{CC} - I_{CQ}(R_C + R_E) \\ &= 20 - 2.8\text{mA} \times 4\text{k }\Omega \end{aligned}$$

$$\therefore V_{CEQ} = 8.8\text{V}$$

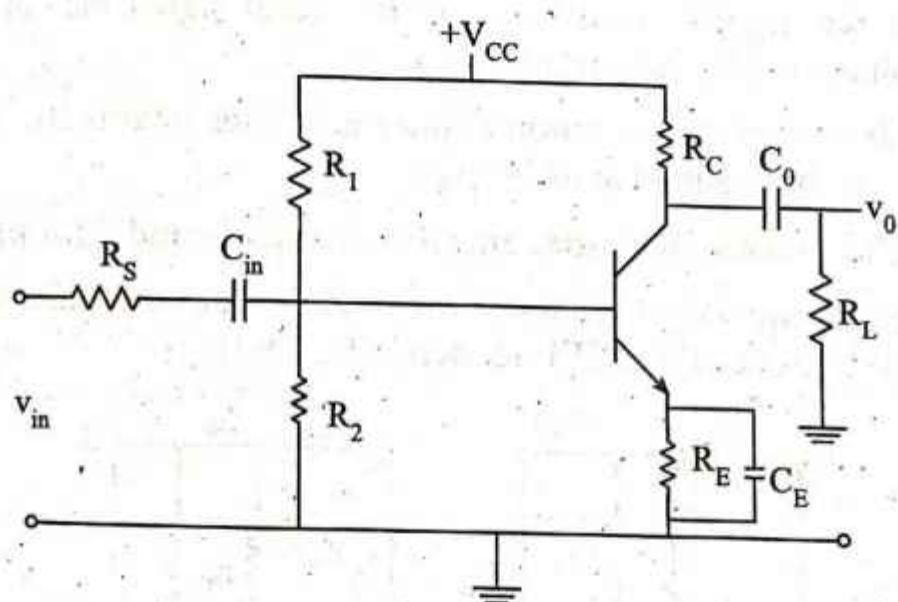
## 2.8 Basic Single Stage BJT Amplifier Configurations (C-E, C-B, C-C)

### 2.8.1 Common Emitter (C-E) Amplifier:

The circuit diagram of common emitter amplifier is shown in fig 2.8.1(a) & (b). It implies the universal voltage divider biasing method. The emitter capacitor  $C_E$  which is connected parallel to the emitter resistor  $R_E$  provides the short circuit path for the ac emitter current.



**Fig.2.8.1 (a) Common emitter Amplifier circuit without using bypass capacitor**



**Fig. 2.8.1(b) Common emitter Amplifier with bypass capacitor  $C_E$**

The input ac signal voltage  $v_{in}$  with its internal resistance  $R_S$  is connected to the input of the amplifier through the input coupling capacitor  $C_{in}$ . The output voltage  $v_o$  from the collector terminal is taken through the output coupling capacitor  $C_0$ . The values of  $C_{in}$  and  $C_0$  should be high enough over the frequency range of the ac signal so that they provide almost a short circuit path for the ac signals and practically blocks the dc signals.

When the ac input signal is applied to the amplifier circuit, the total voltage applying at the input will be equal to the sum of the dc biasing voltage and the ac signal. Let us assume that input ac signal is a pure sine-wave. When the positive half cycle is applied, the applied ac voltage more forward biases the base-emitter junction. Due to this, base and emitter current increases correspondingly. As a result the collector current also increases. Then the voltage drop across the collector resistor  $R_C$  also increases and these will consequently decreases the collector voltage  $v_C$ .

$$V_{CC} = V_{RC} + v_C$$

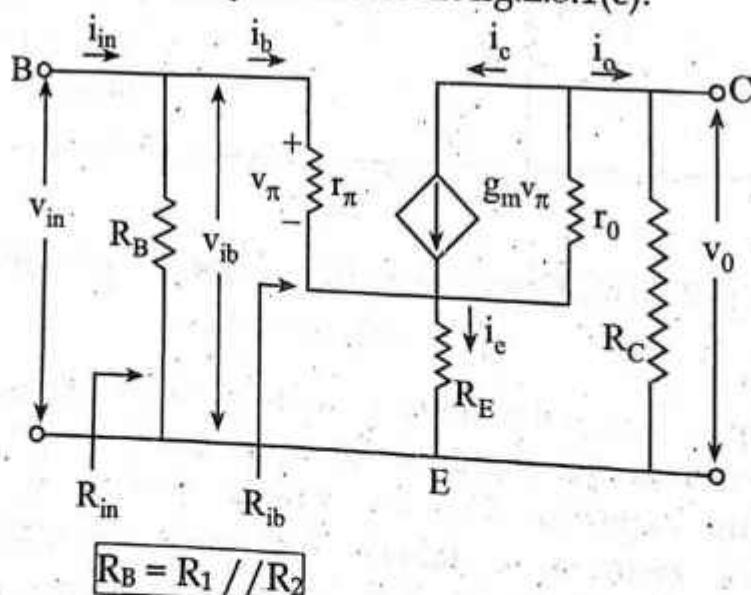
$$\text{or, } v_C = V_{CC} - i_c \cdot R_C$$

From above it is clear that when the input sine wave reaches its positive peak value the collector voltage is minimum and for the negative peak value of the input signal the collector voltage will be maximum.

This shows that common emitter amplifier inverts the phase of the input signal at its output.

#### Analysis of common emitter amplifier using $\pi$ -model for BJT:

The ac equivalent circuit of common emitter amplifier using hybrid  $\pi$  model of BJT is shown in fig.2.8.1(c).



*Fig 2.8.1(c) AC equivalent circuit for given CE amplifier using  $\pi$ -model*

Assume all capacitors are ideal i.e. short circuit for ac and open circuit for dc

### Voltage Gain ( $A_v$ ):

$$A_v = \frac{V_o}{V_{in}}$$

Where,

$$\begin{aligned} V_o &= \text{output voltage} = i_o R_o \approx -i_c R_C && [\text{Ignoring the effect of } r_o] \\ &= -g_m v_n R_C && [\text{From figure } i_o = -i_c] \end{aligned}$$

And

$$\begin{aligned} V_{in} &= \text{input voltage} \\ &= V_{ib} = V_n + i_e R_E && [\text{From figure}] \\ &= V_n + g_m v_n R_E && [i_c \approx i_e = g_m v_n] \\ &= V_n (1 + g_m R_E) \end{aligned}$$

Then,

$$A_v = \frac{V_o}{V_{in}} = \frac{-g_m v_n R_C}{V_n (1 + g_m R_E)}$$

$$\therefore A_v = \boxed{\frac{-g_m R_C}{1 + g_m R_E}}$$

For common emitter amplifier with emitter bypass capacitor  $C_E$ , effect of  $R_E$  will be eliminated. In such case  $R_E = 0$  and from above we have,

$$\boxed{A_v = -g_m R_C}$$

### Input Resistance ( $R_{in}$ ):

We know that,

$$R_{in} = R_B // R_{ib} \quad \dots \dots \dots (i)$$

where,  $\boxed{R_B = R_1 // R_2}$

Now to find  $R_{ib}$ , from figure we have,

$$\begin{aligned} V_{in} &= V_n + i_e R_E \\ &= V_n + i_c R_E && [i_e \approx i_c] \\ \text{or, } V_{in} &= V_n + g_m v_n R_E \\ &= V_n (1 + g_m R_E) \end{aligned}$$

Dividing on both sides by  $i_b$ , we get,

$$\frac{V_{in}}{i_b} = \frac{V_\pi}{i_b} (1 + g_m R_E)$$

$$\text{or, } R_{ib} = r_\pi (1 + g_m R_E)$$

Now, equation (i) becomes

$$R_{in} = R_1 // R_2 // r_\pi (1 + g_m R_E)$$

Now, if  $C_E$  is connected, then  $R_E = 0$ , so

$$R_{in} = R_1 // R_2 // r_\pi$$

### Current Gain ( $A_i$ ):

$$A_i = \frac{i_o}{i_{in}} = \frac{i_L}{i_{in}} \quad [\text{let } R_L \text{ be connected}]$$

Where

$i_L$  = output current

$i_{in}$  = input current

By using current divider rule

$$i_L = \frac{i_o R_C}{(R_C + R_L)} = \frac{-i_c R_C}{(R_C + R_L)} = \frac{-g_m v_\pi R_C}{(R_C + R_L)}$$

Also

$$i_b = i_{in} \frac{R_B}{(R_B + R_{ib})}$$

$$i_{in} = i_b \frac{(R_B + R_{ib})}{R_B}$$

Therefore,

$$\text{Current gain } (A_i) = \frac{i_L}{i_{in}} = \frac{-g_m r_\pi R_C R_B}{(R_C + R_L)(R_B + R_{ib})}$$

Where,  $\beta = g_m r_\pi$

$$\text{Current gain } (A_i) = \frac{i_L}{i_{in}} = \frac{-\beta R_C R_B}{(R_C + R_L)(R_B + R_{ib})}$$

Now, when load is not connected then ignoring  $R_L$  from the above expression of current gain we get,

$$\text{Current gain } (A_i) = \frac{i_L}{i_{in}} = \frac{-\beta R_B}{(R_B + R_{ib})}$$

### Output Resistance ( $R_{out}$ ):

The equivalent circuit to find the output resistance of the common emitter amplifier is shown in fig 2.8.1 (d).

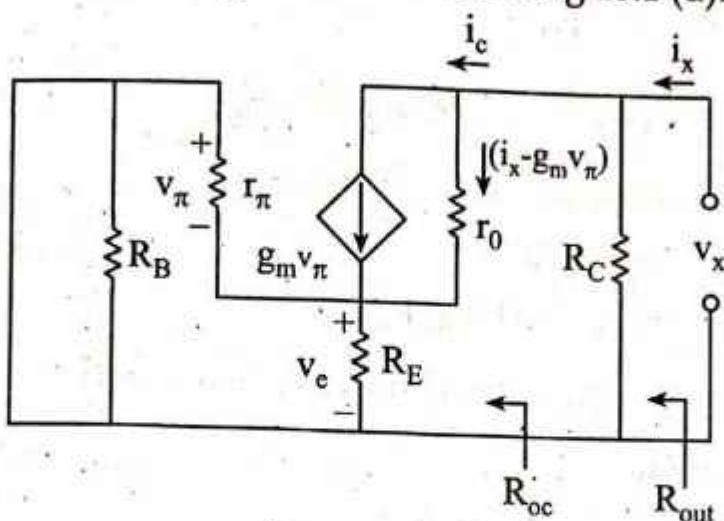


Fig.2.8.1 (d) Equivalent circuit to find Output Resistance

To determine output resistance, its voltage sources  $v_{in}$  is set to zero and a test voltage of  $v_x$  is applied at the output and its corresponding current  $i_x$  is measured. Then

$$R_{oc} = \frac{v_x}{i_x} \text{ and } R_{out} = R_C // R_{oc}$$

The resistance in the base side which is usually much larger compared to emitter resistance  $R_E$ . Therefore, almost all of the  $i_x$  flows through small resistance  $R_E$  and very small (negligible) part of  $i_x$  flows through base branch of the resistance.

Therefore  $v_e \approx i_x R_E$

From figure we have,

$$v_e + v_\pi = 0$$

$$\text{or, } v_e = -v_\pi = -i_x R_E$$

And also from figure,

$$v_x = (i_x - g_m v_\pi) r_o + v_e$$

$$\text{or, } v_x = (i_x - g_m v_\pi) r_o + i_x R_E$$

$$= i_x R_E + [i_x - g_m (-i_x R_E)] r_o$$

$$= i_x [R_E + (1 + g_m R_E) r_o]$$

Now solving for  $\frac{V_x}{i_x} = R_{oc}$

$$\frac{V_x}{i_x} = R_E + (1+g_m R_E) r_o$$

Also neglecting  $R_E$  which is very small

$$R_{oc} \approx r_o (1+g_m R_E) \quad \left[ \therefore \frac{V_x}{i_x} = R_{oc} \right]$$

Also,  $R_{out} \approx R_C // R_{oc}$

$$\approx R_C // r_o (1 + g_m R_E)$$

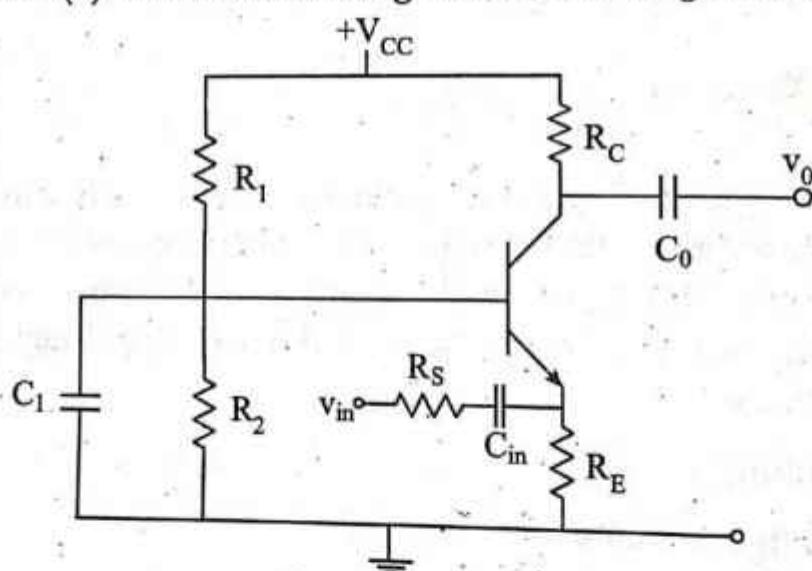
When bypass capacitor  $C_E$  is used then  $R_E = 0$

$$R_{out} \approx R_C // r_o$$

$$R_{out} \approx R_C \quad [r_o \gg R_C]$$

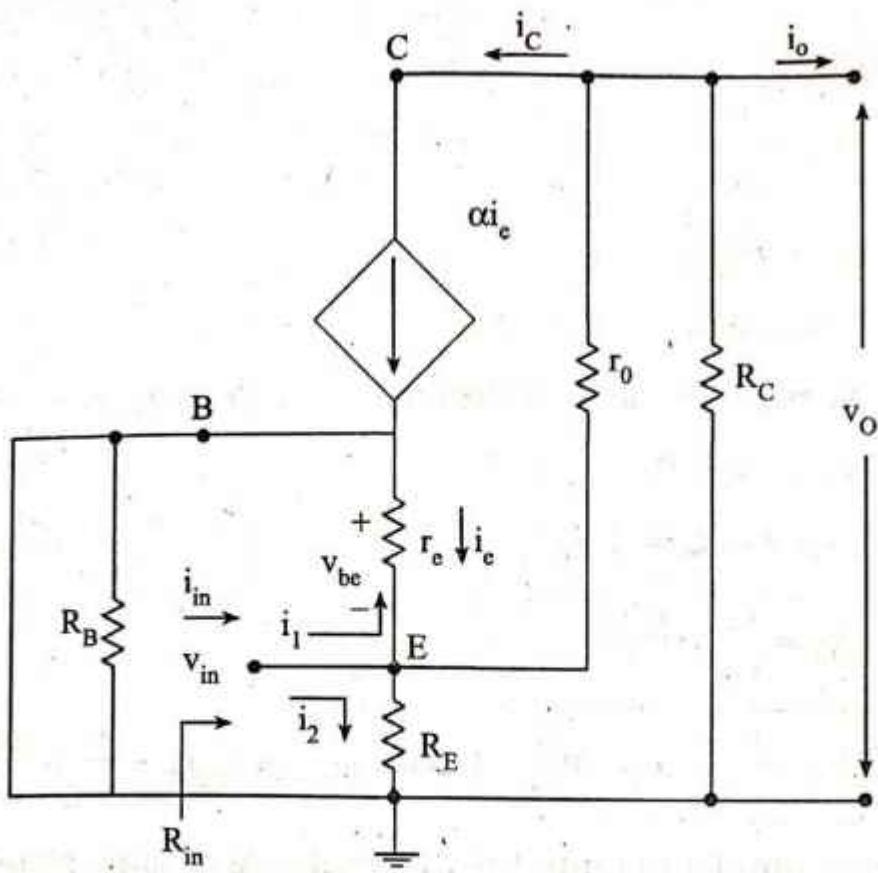
### 2.8.2 Common Base (C-B) Amplifier

The circuit diagram of common base amplifier is shown in fig 2.8.2 (a). It also uses voltage divider biasing method.



*Fig. 2.8.2(a) Common Base Amplifier using Universal Biasing Method*

For ac analysis T model of above circuit is drawn in fig 2.8.2(b).



*Fig.2.8.2 (b) AC equivalent circuit of the given circuit replacing BJT by its T-model*

### Input Resistance ( $R_{in}$ ):

From figure we have,

$$i_{in} = i_1 + i_2 \quad [i_1 = -i_e, \text{ ignoring the effect of } r_0]$$

$$= -i_e + \frac{V_{in}}{R_E} = -\frac{V_{be}}{r_e} + \frac{V_{in}}{R_E} = -\left(\frac{-V_{in}}{r_e}\right) + \frac{V_{in}}{R_E} \quad [V_{in} + V_{be} = 0]$$

$$i_{in} = V_{in} \left[ \frac{1}{r_e} + \frac{1}{R_E} \right] \dots \dots \dots \text{(i)} \quad \therefore V_{in} = -V_{be}$$

$$\frac{i_{in}}{V_{in}} = \left( \frac{1}{r_e} + \frac{1}{R_E} \right)$$

$$\frac{1}{R_{in}} = \left( \frac{1}{r_e} + \frac{1}{R_E} \right)$$

$$R_{in} = r_e // R_E$$

For  $R_E \gg r_e$ ,  $\left( \frac{1}{R_E} \right) \xrightarrow{0}$

$$\text{or, } \frac{1}{R_{in}} = \frac{1}{r_e}$$

$$\therefore R_{in} = r_e$$

### Voltage Gain (Av):

We know, that,

$$v_o = i_o R_o = -i_c R_C \text{ (effect of } r_o \text{ is neglected)}$$

$$\text{or, } v_o = -\alpha i_e R_C$$

$$\text{And, } v_{in} = -v_{be} = -i_e r_e$$

$$\therefore Av = \frac{v_o}{v_{in}} = \frac{\alpha R_C}{r_e}$$

$$\therefore Av = \frac{\alpha R_C}{r_e} = g_m R_C \quad [\text{Assume, } \alpha = 1, g_m = \frac{i_c}{v_{be}} = \frac{i_e}{v_{be}} = \frac{1}{r_e}]$$

Hence, input and output both signals are in same phase.

### Output Resistance ( $R_{out}$ ):

Using Thevenin's equivalent, we get,

$$R_{out} = R_C / r_o$$

$$\therefore R_{out} \approx R_C \quad [\because r_o \gg R_C]$$

### Current Gain ( $A_i$ ):

$$A_i = \frac{i_o}{i_{in}}$$

$$i_o = -i_c = -\alpha i_e$$

And from equation (i)

$$i_{in} = v_{in} \left[ \frac{1}{r_e} + \frac{1}{R_E} \right]$$

Also,

$$v_{in} = -v_{be} = -i_e r_e$$

Now the expression of

$$i_{in} = -i_e r_e \left[ \frac{1}{r_e} + \frac{1}{R_E} \right] = -i_e r_e \left[ \frac{R_E + r_e}{r_e R_E} \right]$$

$$i_{in} = -i_e \left[ \frac{R_E + r_e}{R_E} \right]$$

Then,

$$A_i = \frac{i_o}{i_{in}} = \frac{-\alpha i_e}{-i_e \left[ \frac{R_E + r_e}{R_E} \right]} = \frac{\alpha R_E}{R_E + r_e}$$

Where  $\alpha = g_m r_e$

### 2.8.3 Common Collector (C-C) Amplifier:

The circuit diagram of common collector amplifier is shown in fig 2.8.3 (a). It also uses voltage divider biasing method

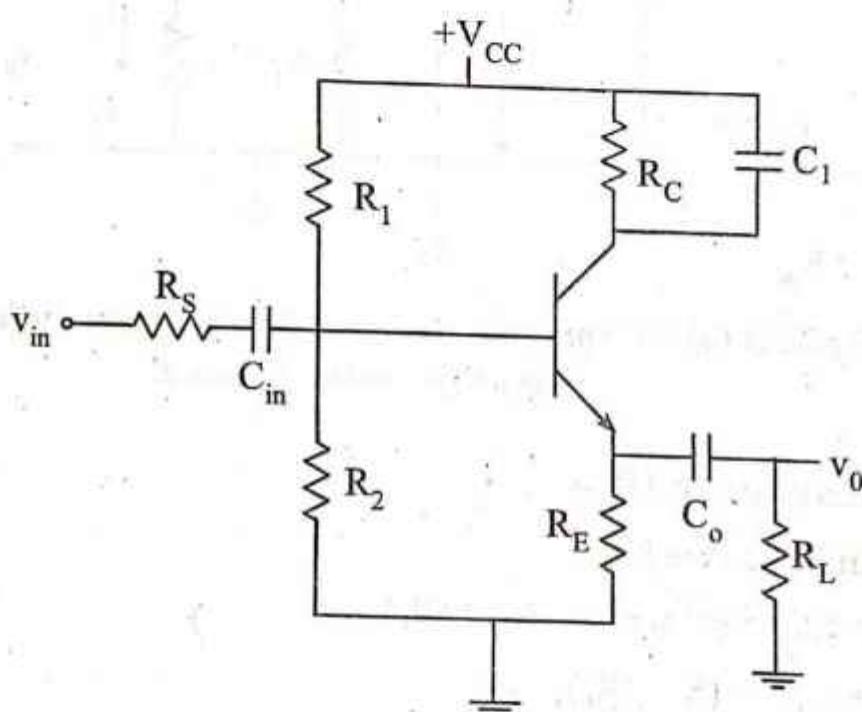


Fig. 2.8.3(a) Common Collector Amplifier circuit

This amplifier is also called "Emitter Follower" because the output voltage is almost an exact replica of input voltage with respect to magnitude and phase. Due to high input and low output impedance it is used as an isolation circuit for connecting a high resistance source to low resistance load.

The ac equivalent circuit using T-model is drawn in fig 2.8.3 (b).

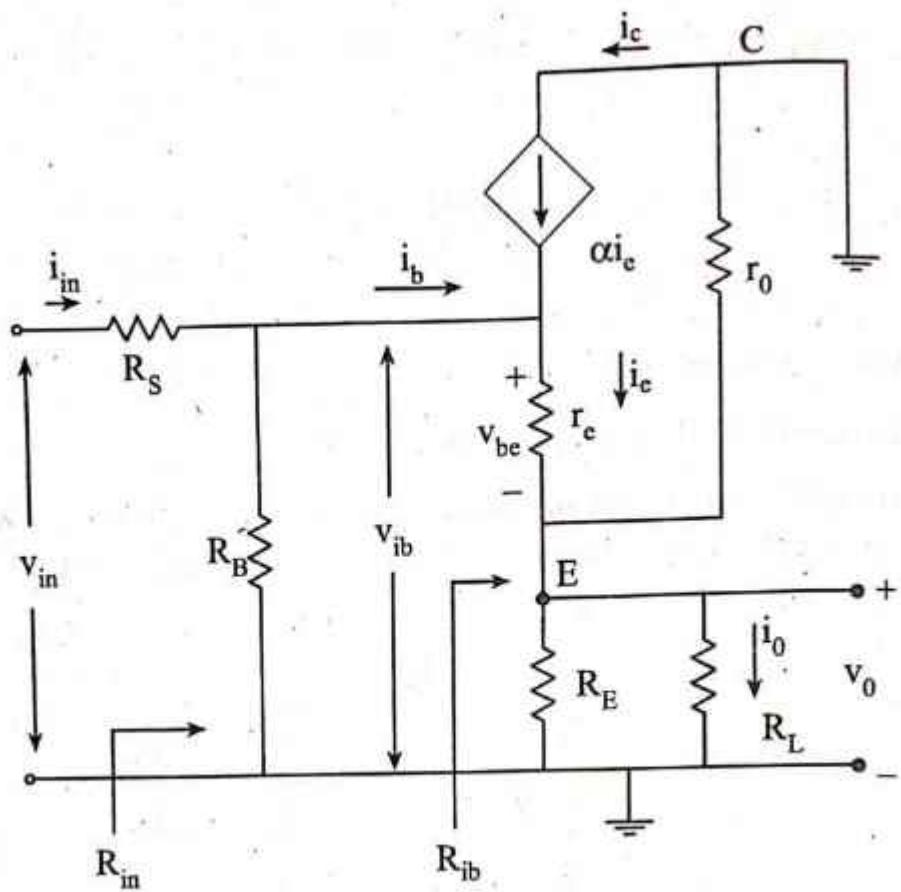


Fig.2.8.3 (b) AC equivalent circuit for Common Collector Amplifier using T-model

### Input Resistance ( $R_{in}$ )

From figure we have,

$$\begin{aligned} V_{ib} &= v_{be} + v_E = i_e r_e + i_e (R_E // R_L) \\ &= i_e [r_e + (R_E // R_L)] \end{aligned}$$

Dividing on both sides by  $i_b$ , we get,

$$\frac{V_{ib}}{i_b} = \frac{i_e}{i_b} [r_e + R_E'] \quad \text{where, } R_E' = R_E // R_L$$

$$\text{or, } R_{ib} = (\beta + 1) (r_e + R_E') \quad [\because \frac{i_e}{i_b} = \beta + 1]$$

$$\therefore R_{in} = R_B // R_{ib} = R_1 // R_2 // (\beta + 1) (r_e + R_E')$$

### Voltage Gain ( $A_v$ )

From figure,

$$A_v = \frac{V_o}{V_{in}} = \frac{i_e R'_E}{V_{ib}}$$

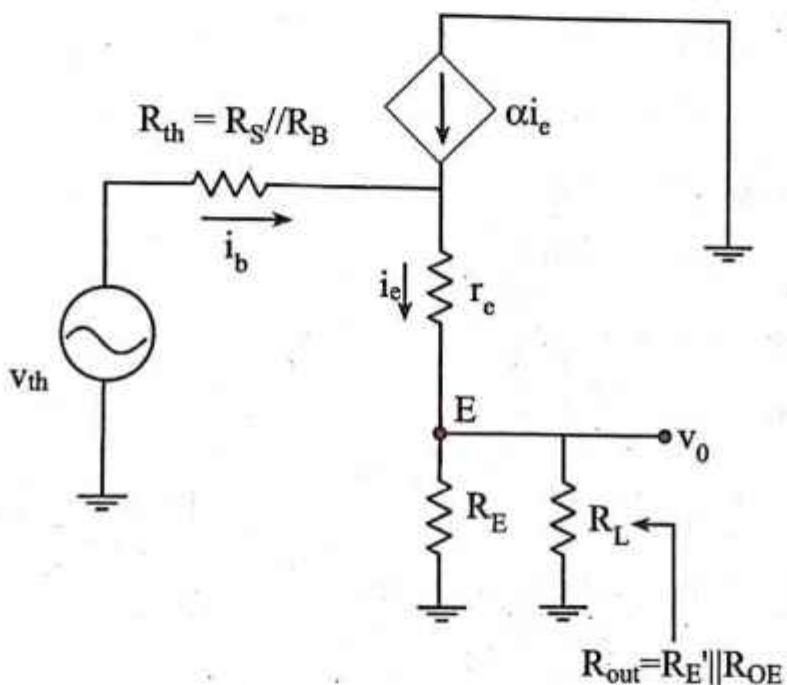
$$A_v = \frac{i_e R'_E}{i_e [r_e + (R_E // R_L)]} = \frac{R'_E}{(r_e + R'_E)} \approx 1$$

### Output Resistance ( $R_{out}$ ):

The Thevenin equivalent circuit for given circuit looking through base of transistor is determined such that,

$$R_{th} = R_S // R_B \text{ and, } V_{th} = \frac{R_B}{R_B + R_S} V_{in}$$

∴ The equivalent circuit can be drawn as:

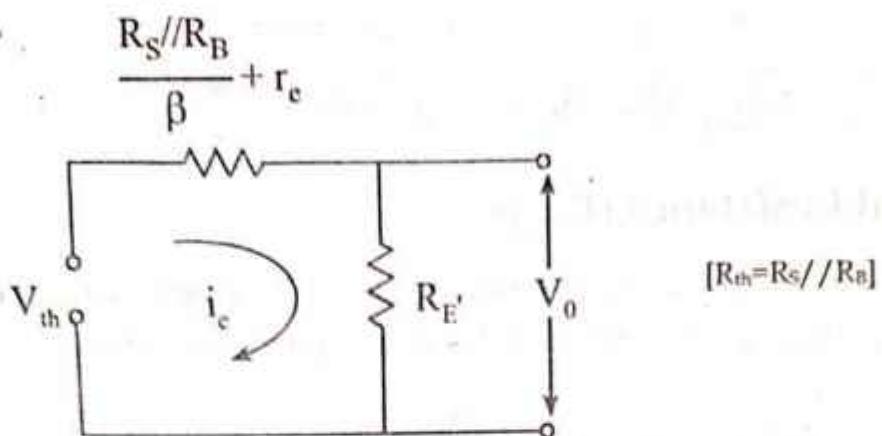


Now, we have,

$$\begin{aligned} V_{th} &= i_b \cdot R_{th} + i_e (r_e + R_E // R_L) \\ &= i_b R_{th} + i_e (r_e + R_E') \\ &= i_e \frac{R_{th}}{\beta} + i_e (r_e + R_E') \quad [i_b = \frac{i_c}{\beta} \approx \frac{i_e}{\beta}] \end{aligned}$$

$$V_{th} = i_e \left( \frac{R_{th}}{\beta} + r_e + R_E' \right) \dots\dots\dots (i)$$

Equation (i) can be drawn as below:



*Equivalent circuit for output current*

$$R_{th} = R_s // R_B$$

From above we have

$$i_e = \frac{V_{th}}{\left( \frac{R_{th}}{\beta} + r_e + R_E' \right)}$$

From figure, we have,

$$R_{OE} = r_e + \frac{R_s // R_B}{\beta}$$

$$R_{out} = R_E' // R_{OE}$$

$$\therefore R_{out} = R_E' // \left( r_e + \frac{R_s // R_B}{\beta} \right)$$

$$[\therefore R_{out} = R_E' // R_{OE}]$$

Since,  $R_E$  and  $R_L$  both are large,

$$R_{out} \approx r_e + \frac{R_s // R_B}{\beta}$$

### Current Gain ( $A_i$ ):

We have from current divider rule

$$i_b = \frac{R_B}{R_B + R_{ib}} \times i_{in}$$

$$\text{or, } i_{in} = \left( \frac{R_B + R_{ib}}{R_B} \right) \times i_b$$

$$= \left( \frac{R_B + R_{ib}}{R_B} \right) \times \left( \frac{i_e}{\beta + 1} \right)$$

Also, we have,

$$i_o = i_e \times \frac{R_E}{R_E + R_L}$$

Thus, the current gain is given by:

$$A_C = \frac{i_o}{i_{in}} = (\beta + 1) \times \frac{R_E}{R_E + R_L} \times \frac{R_B}{R_B + R_{ib}}$$

Now, when no-load is connected then ignoring above expression we get,

$$A_C = (\beta + 1) \times \frac{R_B}{R_B + R_{ib}}$$

## 2.9 Transistor as a Switch – Cutoff and Saturation

BJT can work in one of the following mode of operations:

- i. Active Mode
- ii. Cutoff mode
- iii. Saturation Mode

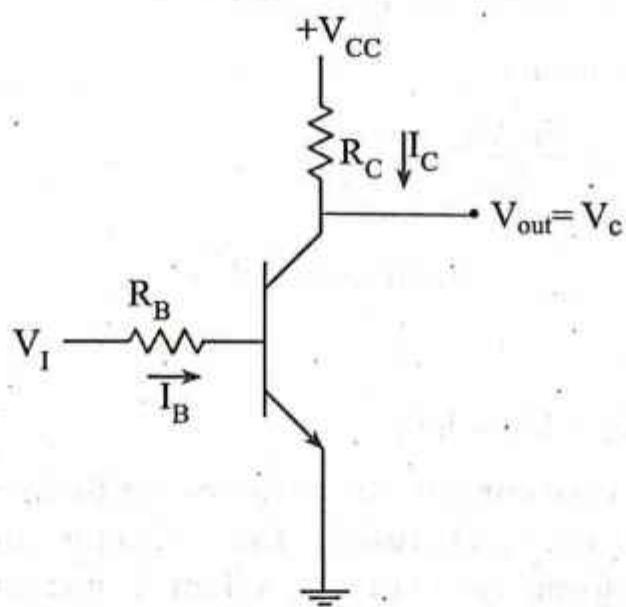


Fig.2.9 (a) BJT as a Switch

Out of these modes of operation the cutoff and saturation mode of operations are used to operate BJT as a switch. When transistor is in cutoff mode, it doesn't conduct any current and this mode of operation is considered as "OFF" position of switch. Now, when base emitter junction voltage will be well

beyond the cut-in voltage the transistor enters into saturation mode and maximum current will flow in it. It is "ON" position.

### Operation in cutoff mode

When base emitter junction is less than 0.5 volt, it will be in reverse biased and practically no current flows in the transistor.

$$V_{BE} < 0.5 \text{ V}; I_B = I_C = I_E = 0$$

$$\text{Therefore, } V_{out} = V_C = V_{CC}$$

Since all the currents in transistor are equal to zero the transistor is in "OFF" condition.

### Operation in saturation mode

When  $V_{BE} > 0.7 \text{ V}$  the transistor enters into active mode. The  $V_{BE}$  can be increased just by increasing the input  $V_I$ . Since emitter is directly grounded.

In active mode

$$I_B = \frac{V_I - V_{BE}}{R_B} = \frac{V_I - 0.7}{R_B}$$

$$I_B = \frac{I_C}{\beta} \quad [\text{for active mode}]$$

Also,

$$V_C = V_{CC} - I_C R_C$$

The base current can be increased by increasing  $V_I$ . It is clear from above expression that collector current increases with increasing base current. When  $I_C$  increases  $V_C$  decreases. In this process if  $V_C$  will be less than  $V_B$  (0.7) then collector-base junction starts to be come forward biased and operation of transistor enters into saturation mode. In saturation mode, if  $I_B$  increases  $I_C$  also increases and  $V_C$  will decreases. This means that collector base junction of transistor becomes more and more forward biased and transistor enters into deep saturation region.

Thus in saturation mode

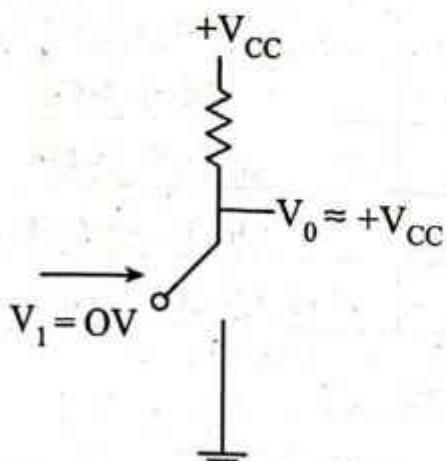
$$I_C \neq \beta I_B$$

We have

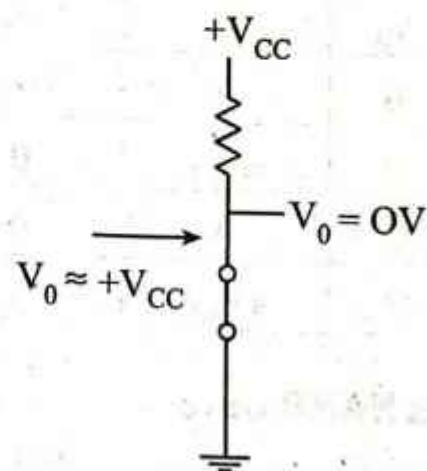
$$I_{C_{sat}} = \frac{V_{CC} - V_{CE_{sat}}}{R_C}$$

$$\beta_{forced} = \frac{I_{C_{sat}}}{I_B}$$

The equivalent circuit diagram for the described conditions can be expressed as follows:



For cut-off mode



For cut-off mode

The truth table can be constructed as:

$V_I$	$V_O$	Transistor states
0	+V <sub>CC</sub>	OFF
+V <sub>CC</sub>	0	ON

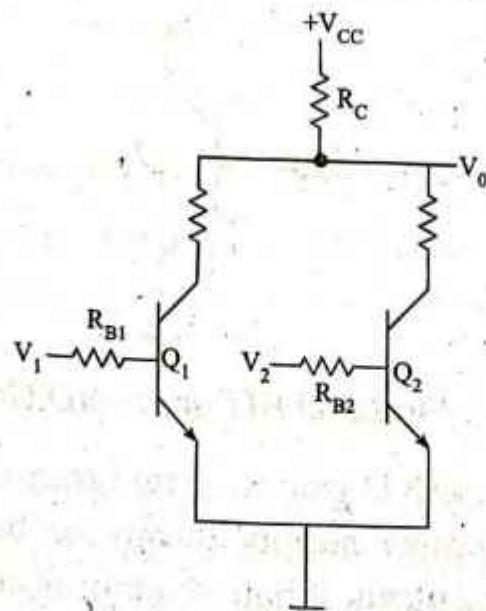


Fig.2.9 (b) BJT as NOR Gate

A simple BJT NOR gate comprises of two transistors connected in parallel to each other such that the two input voltages  $V_1$  and  $V_2$  can be applied. In this circuit, if any of the input, say  $V_1$  and  $V_2$  or both, remains high, the current conducts such that the output voltage  $V_0$  produces  $V_{CE\text{ sat}} \approx 0.2V$ . If the input voltages for both the transistors are low i.e. grounded, the output voltage will approximately equal to a value of  $+V_{CC}$ . Thus, its truth table can be written as:

$V_1$	$V_2$	$V_0$	Transistor states
0	0	$+V_{CC}$	$Q_1$ OFF, $Q_2$ OFF
0	$+V_{CC}$	0	$Q_1$ OFF, $Q_2$ ON
$+V_{CC}$	0	0	$Q_1$ ON, $Q_2$ OFF
$+V_{CC}$	$+V_{CC}$	0	$Q_1$ ON, $Q_2$ ON

### BJT as NAND Gate

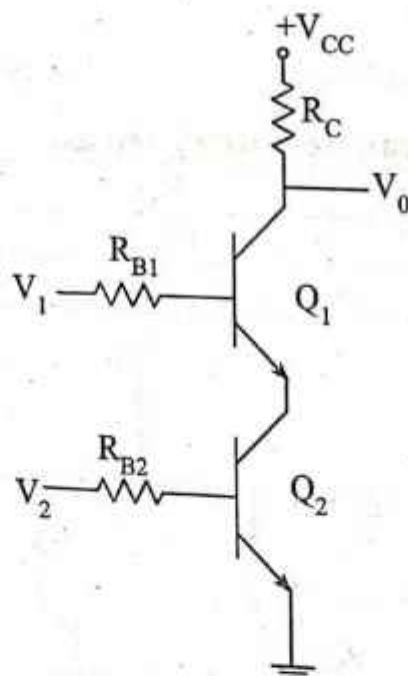


Fig.2.9(c) BJT as NAND Gate

A simple BJT NAND gate uses two transistors in series such that the low power supply to any or both the base input generates high output. If both the inputs are high, only at that very condition, the output voltage is low.

The truth table for the given circuit can be drawn as shown below:

### Truth Table

$V_1$	$V_2$	$V_0$	Transistor states
0	0	$+V_{CC}$	$Q_1$ OFF, $Q_2$ OFF
0	$+V_{CC}$	$+V_{CC}$	$Q_1$ OFF, $Q_2$ ON
$+V_{CC}$	0	$+V_{CC}$	$Q_1$ ON, $Q_2$ OFF
$+V_{CC}$	$+V_{CC}$	0	$Q_1$ ON, $Q_2$ ON

---

### 2.10 A General Large Signal Model for the BJT: The Ebers-Moll Model

---

A transistor's model has been proposed by Ebers and Moll. To determine the model of a transistor the emitter-base junction is considered as a pn junction diode. Then the normal current through the emitter-base junction and the collector base junction can be determined as:

$$i_{EF} = I_{EO}(e^{V_{BE}/nV_T} - 1) \dots \dots \dots (1)$$

where,

$i_{EF}$  = forward emitter current

$I_{EO}$  = reverse saturation emitter current of the junction

$V_{BE}$  = voltage applied across the base-emitter junction

$V_T$  = thermal voltage.

Due to the emitter forward current collector forward current  $i_{CF}$  also flows through the collector base junction which can be expressed as,

$$i_{CF} = -\alpha_F i_{EF} \dots \dots \dots (2)$$

where  $\alpha_F$  is the current gain showing the relation between the collector and emitter currents. The negative sign shows the opposite direction of the collector current  $i_{CF}$  with respect to the emitter current  $i_{EF}$ .

Since the collector-base junction for normal operation will be reverse biased some reverse collector current  $i_{CR}$  flows through the collector-base junction. It can be expressed as,

$$i_{CR} = I_{CO}(e^{V_{CB}/nV_T} - 1) \dots\dots\dots(3)$$

where,  $I_{CO}$  is the reverse saturation collector current.

Due to this reverse collector current  $i_{CR}$  some emitter reverse current  $i_{ER}$  also flows across the base-emitter junction. It can be expressed as,

$$i_{ER} = -\alpha_R i_{CR} \dots\dots\dots(4)$$

where,  $\alpha_R$  is the reverse current gain. The negative sign indicates the opposite direction of  $i_{ER}$  with respect to  $i_{CR}$ .

From above four equations we can write,

$$i_E = i_{EF} + i_{ER} = I_{EO}(e^{V_{BE}/nV_T} - 1) - \alpha_R i_{CR} \dots\dots\dots(5)$$

$$i_C = i_{CF} + i_{CR} = -\alpha_F i_{EF} + I_{CO}(e^{V_{CB}/nV_T} - 1) \dots\dots\dots(6)$$

The equation (5) can be explained as the parallel combination of a forward biased diode with the forward current  $i_{EF}$  and the reverse current generator  $\alpha_R i_{CR}$ . Similarly the equation (6) states that it is parallel combination of current source  $\alpha_F i_{EF}$  and the diode with reverse current  $i_{CR}$ . On the basis of the above equations the Ebers-Moll model of a transistor can be drawn as shown in fig 2.10.

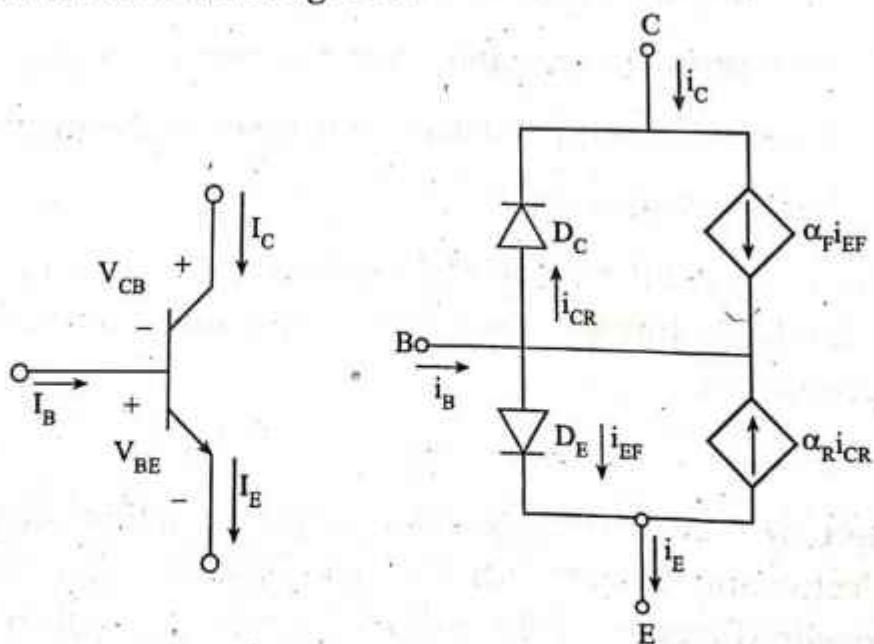


Fig. 2.10 Ebers-Moll Model for a transistor

- Q. Design a voltage divider type dc biased common emitter amplifier circuit. Given parameters are  $V_{CC} = 24$  V<sub>DC</sub>,  $I_C = 2\text{mA}$  and  $\beta = 150$ . Use firm biasing method. And draw its ac equivalent circuit and estimate its input and output resistance and voltage gain for common emitter Unbypassed amplifier.

[070 Ashad Back]

*Solution:*

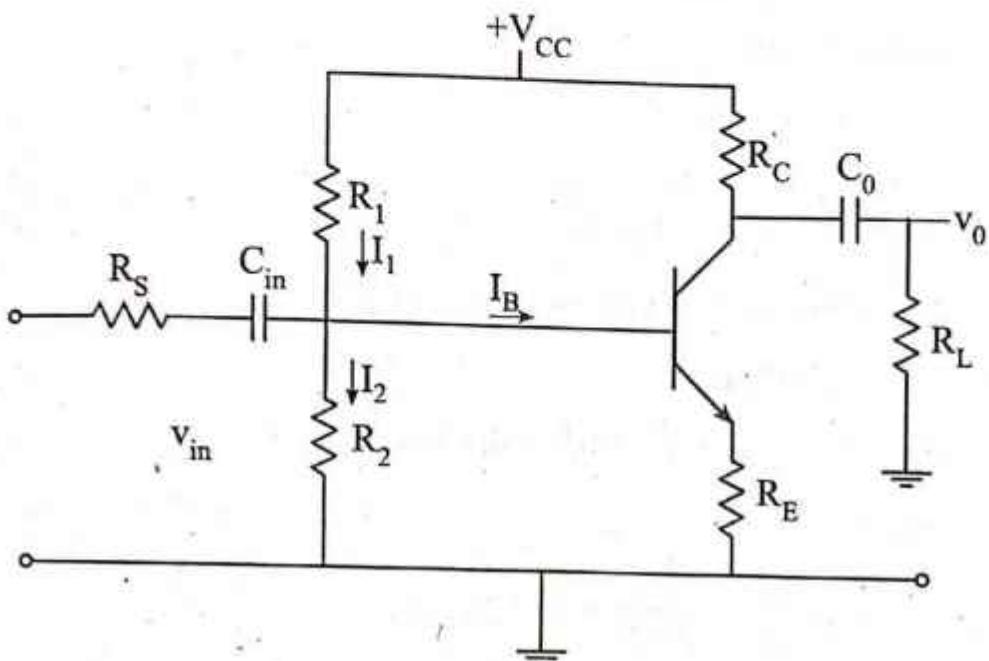


Fig. Common Emitter Amplifier

Since  $V_{CC} > 15$  V DC

So using guideline 2

We have,

$$V_E = 0.1 V_{CC}$$

$$V_{RE} = 0.4 V_{CC}$$

$$V_{CE} = 0.5 V_{CC}$$

Also, for firm biasing

$$R_2 = 0.1 \beta R_E$$

Now,

$$V_E = V_{RE} = I_E R_E \approx I_C R_E = 0.1 V_{CC}$$

$$\text{or, } R_E = \frac{0.1 V_{CC}}{I_C} = \frac{0.1 \times 24}{2\text{mA}} = 1.2 \text{ k}\Omega$$

Also,

$$V_{RC} = I_C R_C = 0.4 V_{CC}$$

$$\text{or, } R_C = \frac{0.4 V_{CC}}{I_C} = \frac{0.4 \times 24}{2 \text{mA}} = 4.8 \text{ K}\Omega$$

We know, for firm biasing,

$$R_2 = 0.1 \beta R_E = 0.1 \times 150 \times 1.2 \text{ K}\Omega = 18 \text{ K}\Omega$$

From figure,

$$I_1 = I_2 + I_B$$

$$R_1 = \frac{V_{R1}}{I_1} = \frac{V_{CC} - V_B}{I_2 + I_B} \dots\dots\dots \text{(i)}$$

Now, to find the values of equation (i)

$$V_{BE} = V_B - V_E$$

$$\text{or, } V_B = V_{BE} + V_E = 0.7 + 0.1 V_{CC} = 3.1 \text{ V}$$

Also,

$$I_2 = \frac{V_B}{R_2} = \frac{3.1}{18 \text{K}\Omega} = 0.172 \text{ mA}$$

And,

$$I_B = \frac{I_C}{\beta} = \frac{2 \text{mA}}{150} = 0.013 \text{ mA}$$

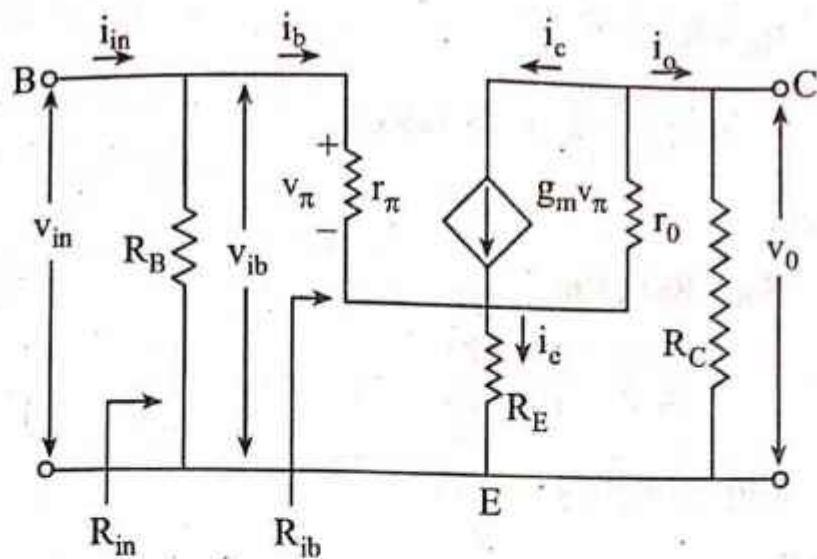
Now, equation (i) becomes,

$$\begin{aligned} \therefore R_1 &= \frac{V_{R1}}{I_1} = \frac{V_{CC} - V_B}{I_2 + I_B} = \frac{24 - 3.1}{(0.172 + 0.013)} \text{ mA} \\ &= 112.98 \text{ K}\Omega \approx 113 \text{ K}\Omega \end{aligned}$$

Hence,

$$R_1 = 113 \text{ K}\Omega; R_2 = 18 \text{ K}\Omega; R_C = 4.8 \text{ K}\Omega; R_E = 1.2 \text{ K}\Omega$$

Now, converting voltage divider dc biased common emitter amplifier circuit into its ac equivalent



$$R_C = 4.8 \text{ k}\Omega$$

$$R_E = 1.2 \text{ k}\Omega$$

$$R_B = R_1 // R_2$$

$$R_1 = 113 \text{ k}\Omega$$

$$R_2 = 18 \text{ k}\Omega$$

Now, to find input resistance  $R_{in}$

$$R_{in} = R_B // R_{ib}$$

Where,

$$R_{ib} = r_\pi (1 + g_m R_E)$$

$$g_m = \frac{I_C}{V_T} = \frac{2 \text{ mA}}{25 \text{ mV}} = 0.08 \text{ mho}$$

Then,

$$\beta = g_m r_\pi$$

$$\text{or, } r_\pi = \frac{\beta}{g_m}$$

$$= \frac{150}{0.08} = 1875 \Omega = 1.875 \text{ k}\Omega$$

Then,

$$\begin{aligned} R_{ib} &= r_\pi (1 + g_m R_E) \\ &= 1.875 (1 + 0.08 \times 1.2 \times 1000) \text{ k}\Omega \\ &= 181.875 \text{ k}\Omega \end{aligned}$$

$$\therefore R_B = R_1 \parallel R_2$$

$$= \frac{113 \times 18}{113 + 18} = 15.52\text{K}\Omega$$

Then,

$$R_{in} = R_B \parallel R_{ib}$$

$$= \frac{15.52 \times 181.875}{15.52 + 181.875}$$

$$R_{in} = 14.3\text{K}\Omega$$

Now,

$$\text{Voltage gain (Av)} = \frac{-gm R_C}{1 + gm R_E}$$

$$= \frac{0.08 \times 1000 \times 4.8}{1 + 0.08 \times 1000 \times 1.2}$$

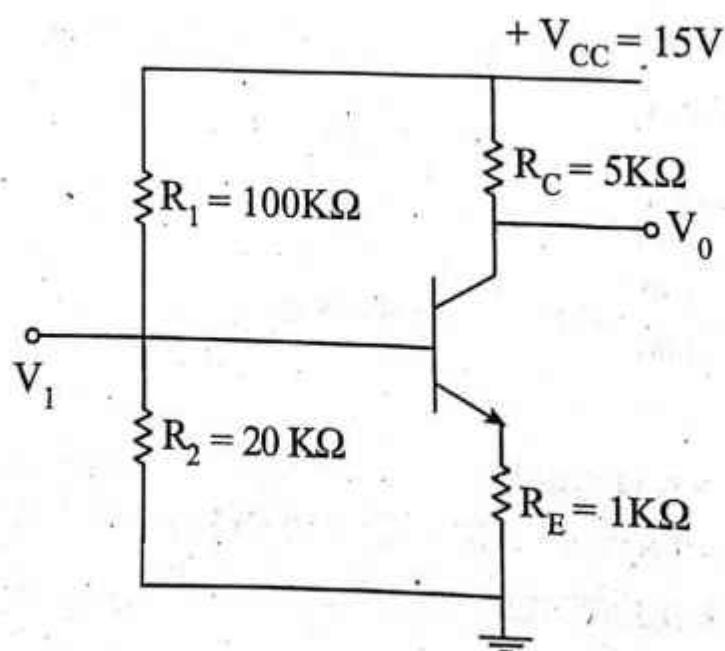
$$\therefore Av = -3.958$$

Also,

$$R_{out} = R_C = 4.8\text{ K}\Omega$$

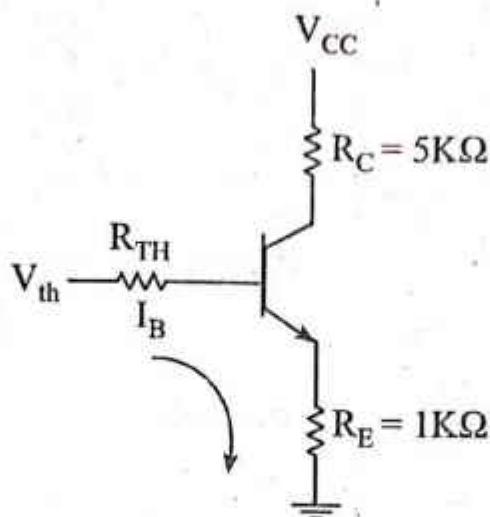
- Q. Draw the ac equivalent circuit for the given circuit and find its input and output resistances. Assume  $\beta = 100$  for the BJT.

[069 Chaitra Regular]



*Solution:*

The equivalent Thevenin's circuit of given circuit can be drawn as:



Here,

$$V_{th} = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{20}{20 + 100} \times 15 = 2.5V$$

$$R_B = R_{th} = R_1 || R_2 = \frac{R_1 \times R_2}{R_1 + R_2} = \frac{100 \times 20}{100 + 20} = 16.67 \text{ K}\Omega$$

$$\therefore V_{th} = I_B R_{th} + V_{BE} + I_E R_E$$

$$= \frac{I_C}{\beta} R_{th} + V_{BE} + I_C R_E$$

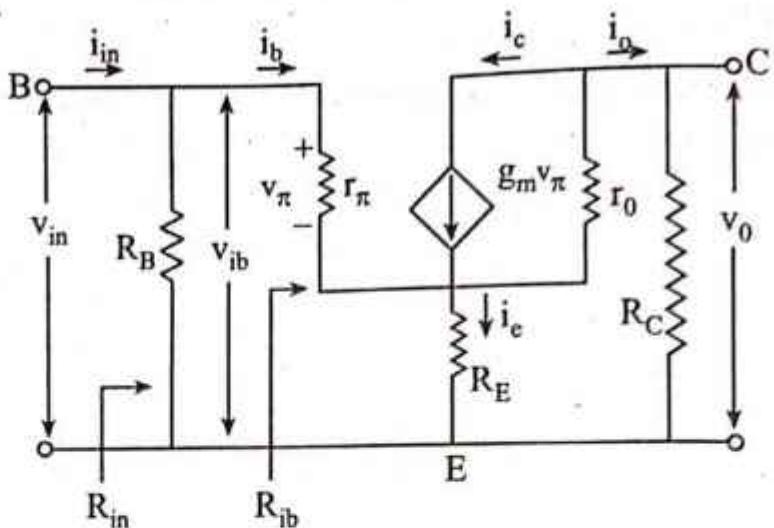
$$= I_C \left( \frac{R_{th}}{\beta} + R_E \right) + V_{BE}$$

$$\therefore 2.5 = I_C \left( \frac{16.67}{100} + 1 \right) + 0.7$$

$$2.5 - 0.7 = I_C (1.1667)$$

$$\boxed{\therefore I_C = \frac{1.8}{1.1667} = 1.54 \text{ mA}}$$

Now, converting voltage divider dc biased common emitter amplifier circuit into its ac equivalent circuit. We have,



$$g_m = \frac{I_C}{\eta V_T} = \frac{1.54}{1 \times 25} = 0.0616 \text{ mho}$$

$$\begin{aligned} R_{in} &= R_B \parallel R_{ib} \\ &= R_B \parallel r_\pi (1 + g_m R_E) = 5 \text{ k}\Omega \end{aligned}$$

$$\beta = g_m r_\pi$$

$$\begin{aligned} \text{or, } r_\pi &= \frac{\beta}{g_m} = \frac{100}{0.0616} = 1623.37 \Omega \\ &= 1.623 \text{ k}\Omega \end{aligned}$$

$$\begin{aligned} \therefore R_{ib} &= r_\pi (1 + g_m R_E) \\ &= 1.623 (1 + 0.0616 \times 1 \times 1000) \text{ k}\Omega \\ &= 101.6 \text{ k}\Omega \end{aligned}$$

$$\therefore R_{in} = R_B \parallel R_{ib}$$

$$\boxed{\therefore R_{in} = \frac{16.67 \times 101.6}{16.67 + 101.6} = 14.32 \text{ k}\Omega}$$

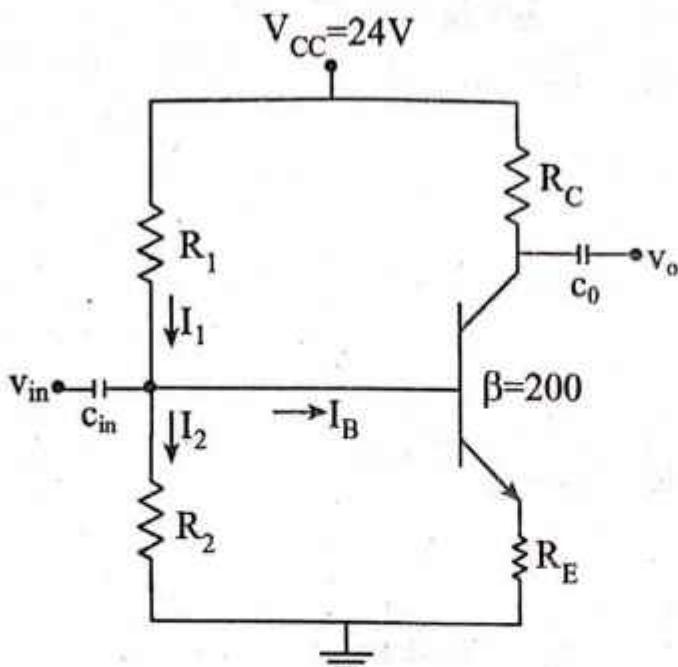
Now, for output resistance ignoring the effect of  $r_o$ , we get,

$$\boxed{R_{out} = R_C = 5 \text{ k}\Omega.}$$

- Q. Design a voltage divider type dc baised common emitter amplifier circuit to obtain  $\beta$  - independent biasing. Use appropriate guideline and firm biasing to suit your design. Given parameters are:  $V_{CC} = 24 \text{ VDC}$ ,  $I_{CQ} = 2 \text{ mA}$  and  $\beta = 200$ .

[063 Baisakh Regular]

*Solution:*



Since  $V_{CC} > 15$  VDC, So using guideline 2

We have,

$$V_E = 0.1 V_{CC}$$

$$V_{RC} = 0.4 V_{CC}$$

$$V_{CE} = 0.5 V_{CC}$$

Also, for firm biasing

$$R_2 = 0.1 \beta R_E$$

Now,

$$V_E = V_{RE} = I_E R_E \approx I_C R_E = 0.1 V_{CC}$$

$$\text{or, } R_E = \frac{0.1 V_{CC}}{I_C} = \frac{0.1 \times 24}{2 \text{mA}} = 1.2 \text{ k}\Omega$$

Also,

$$V_{RC} = I_C R_C = 0.4 V_{CC}$$

$$\text{or, } R_C = \frac{0.4 V_{CC}}{I_C} = \frac{0.4 \times 24}{2 \text{mA}} = 4.8 \text{ k}\Omega$$

We know, for firm biasing,

$$R_2 = 0.1 \beta R_E = 0.1 \times 200 \times 1.2 \text{ k}\Omega = 24 \text{ k}\Omega$$

From figure,

$$I_1 = I_2 + I_B$$

$$R_1 = \frac{V_{R1}}{I_1} = \frac{V_{CC} - V_B}{I_2 + I_B} \dots\dots\dots (i)$$

Now, to find the values of equation (i)

$$V_{BE} = V_B - V_E$$

$$\text{or, } V_B = V_{BE} + V_E \\ = 0.7 + 0.1 V_{CC} = 3.1 \text{ V}$$

Also,

$$I_2 = \frac{V_B}{R_2} = \frac{3.1}{24\text{K}\Omega} = 0.129 \text{ mA}$$

And,

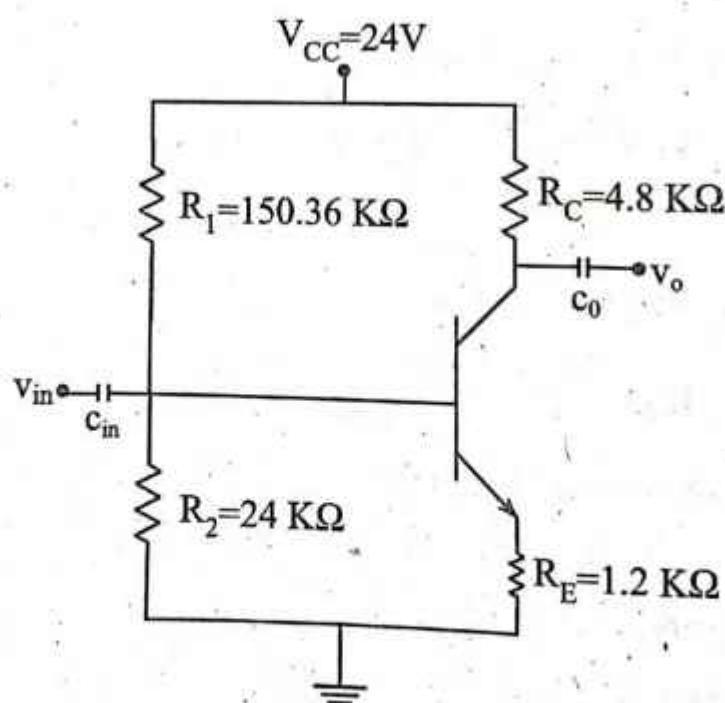
$$I_B = \frac{I_C}{\beta} = \frac{2\text{mA}}{200} = 0.01 \text{ mA}$$

Now, equation (i) becomes,

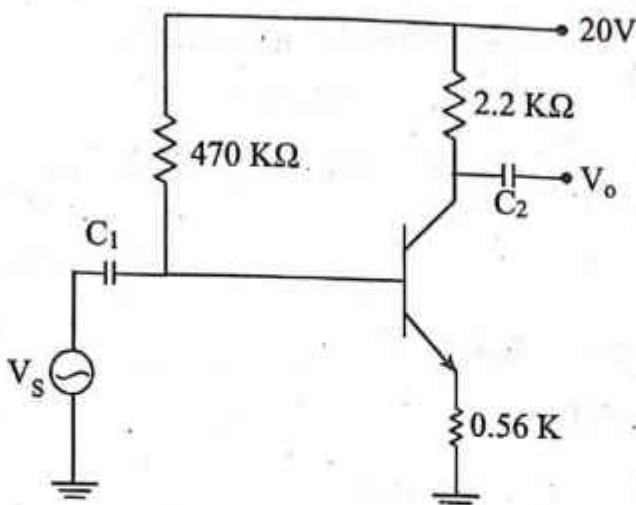
$$\therefore R_1 = \frac{V_{R1}}{I_1} = \frac{V_{CC} - V_B}{I_2 + I_B} \\ = \frac{24 - 3.1}{(0.129 + 0.01)} \text{ mA} = 150.36 \text{ K}\Omega$$

Hence,

$R_1 = 150.36 \text{ K}\Omega; R_2 = 24\text{K}\Omega; R_C = 4.8 \text{ K}\Omega; R_E = 1.2 \text{ K}\Omega$



- Q. For the figure shown below with  $\beta = 120$  find the (a) input impedance (b) output impedance (c) voltage gain (d) current gain. Use small signal model. [068 Chaitra Regular]



*Solution:*

Applying KVL in input loop in given circuit we get,

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

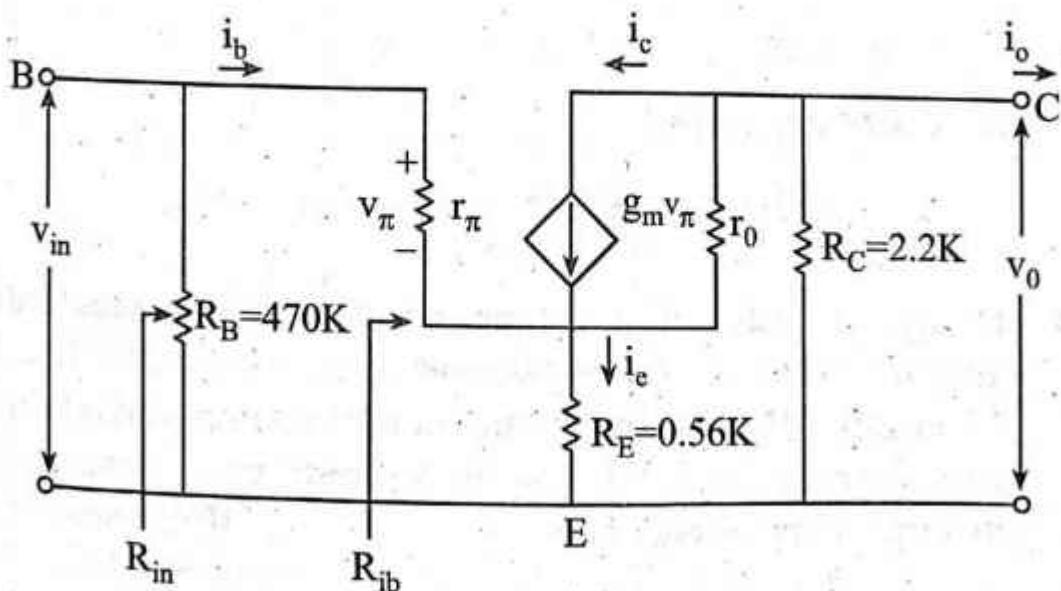
$$\text{or, } 20 - \frac{I_C}{\beta} 470 - 0.7 - I_C 0.56 = 0$$

$$\text{or, } 19.3 - I_C \left( \frac{470}{120} + 0.56 \right) = 0$$

$$\text{or, } 19.3 - 4.47 I_C = 0$$

$$\therefore I_C = 4.3176 \text{ mA.}$$

Now, converting given figure into small signal (ac) model



Assume  $V_T = 25$  mV and  $\eta = 1$

We know,

$$g_m = \frac{I_C}{\eta V_T} = \frac{4.3176}{1 \times 25} = 0.172 \text{ mho and}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{120}{0.172} = 697.67 \Omega = 0.697 \text{ k}\Omega.$$

Now,

a. Input impedance ( $R_{in}$ ):

$$\begin{aligned} R_{in} &= R_B \parallel R_{ib} \\ &= R_B \parallel r_\pi (1 + g_m R_E) \\ &= 470 \parallel 0.697 (1 + 0.172 \times 0.56 \times 1000) \\ &= 470 \parallel 67.83 \text{ k}\Omega \\ &= 59.27 \text{ k}\Omega \end{aligned}$$

b. Output impedance ( $R_{out}$ ):

$$R_{out} = R_C = 2.2 \text{ k}\Omega$$

c. Voltage Gain ( $A_v$ ):

$$\begin{aligned} A_v &= \frac{-g_m R_C}{1 + g_m R_E} \\ &= -\frac{0.172 \times 2.2 \times 1000}{1 + 0.172 \times 0.56 \times 1000} \\ &= -3.88 \end{aligned}$$

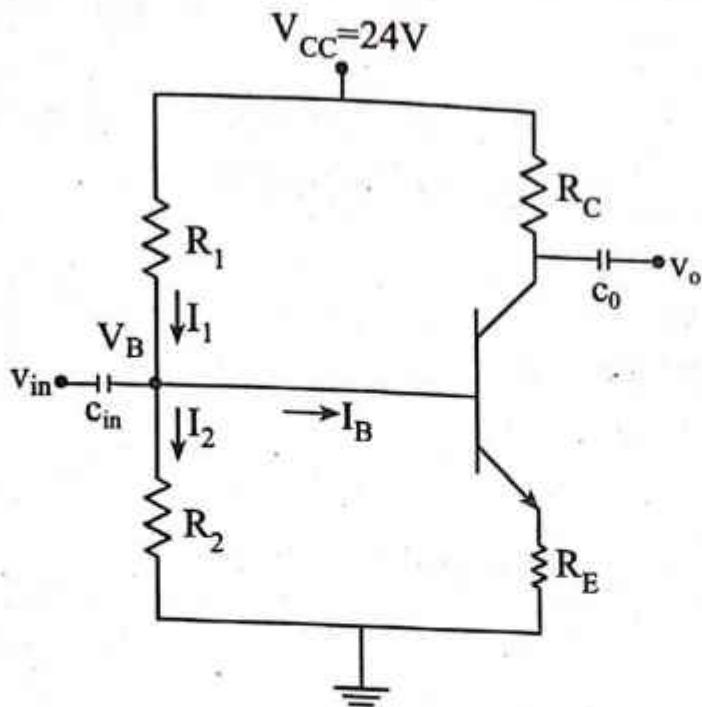
d. Current gain ( $A_i$ ):

$$A_i = \frac{-\beta R_B}{(R_B + R_{ib})} = \frac{-120 \times 470}{(470 + 67.83)} = -104.76.$$

Q. Design  $\beta$  independent type dc biased common emitter amplifier circuit. Given parameters are:  $V_{CC} = 24$  VDC,  $I_C = 1.5$  mA,  $\beta = 150$  and input impedance is comparatively large. Use appropriate guideline to support your design. Also determine its voltage gain.

[069 Ashad Back]

*Solution:*



Since  $V_{CC} \geq 15$  VDC, So using guideline 2

We have,

$$V_E = 0.1 V_{CC}$$

$$V_{RC} = 0.4 V_{CC}$$

$$V_{CE} = 0.5 V_{CC}$$

Since input impedance is comparatively large so we use firm biasing method and we have,

$$R_2 = 0.1 \beta R_E$$

Now,

$$V_E = V_{RE} = I_E R_E \approx I_C R_E = 0.1 V_{CC}$$

$$\text{or, } R_E = \frac{0.1 V_{CC}}{I_C} = \frac{0.1 \times 24}{1.5 \text{mA}} = 1.6 \text{ k}\Omega$$

Also,

$$V_{RC} = I_C R_C = 0.4 V_{CC}$$

$$\text{or, } R_C = \frac{0.4 V_{CC}}{I_C} = \frac{0.4 \times 24}{1.5 \text{mA}} = 6.4 \text{ k}\Omega$$

We know, for firm biasing,

$$R_2 = 0.1 \beta R_E = 0.1 \times 150 \times 1.6 \text{ k}\Omega = 24 \text{ k}\Omega$$

From figure,

$$I_1 = I_2 + I_B$$

$$R_1 = \frac{V_{R1}}{I_1} = \frac{V_{CC} - V_B}{I_2 + I_B} \dots\dots\dots (i)$$

Now, to find the values of equation (i)

$$V_{BE} = V_B - V_E$$

$$\begin{aligned} \text{or, } V_B &= V_{BE} + V_E \\ &= 0.7 + 0.1 V_{CC} \\ &= 3.1 \text{ V} \end{aligned}$$

Also,

$$I_2 = \frac{V_B}{R_2} = \frac{3.1}{24\text{K}\Omega} = 0.129 \text{ mA}$$

And,

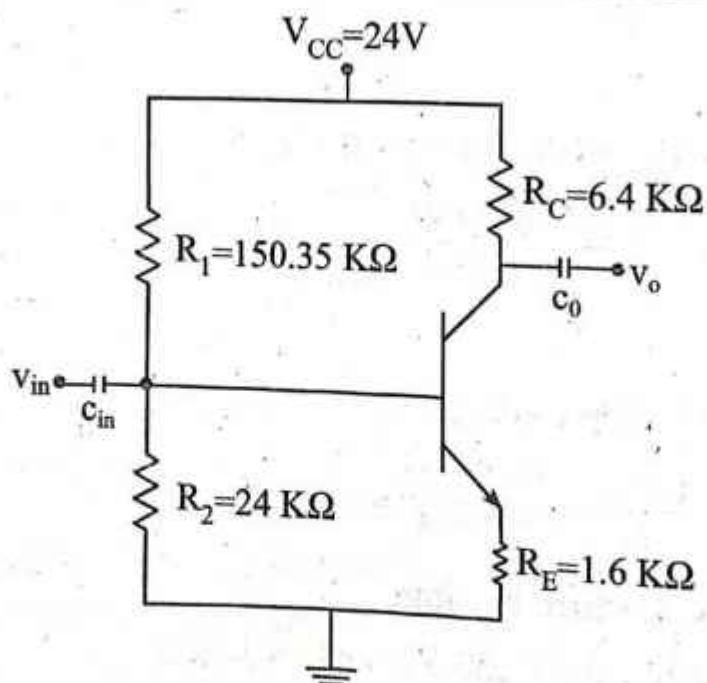
$$I_B = \frac{I_C}{\beta} = \frac{1.5\text{mA}}{150} = 0.01 \text{ mA}$$

Now, equation (i) becomes,

$$\begin{aligned} \therefore R_1 &= \frac{V_{R1}}{I_1} = \frac{V_{CC} - V_B}{I_2 + I_B} \\ &= \frac{24 - 3.1}{(0.129 + 0.01)} = 150.35 \text{ K}\Omega \end{aligned}$$

Hence,

$$R_1 = 150.35 \text{ K}\Omega; R_2 = 24 \text{ K}\Omega; R_C = 6.4 \text{ K}\Omega; R_E = 1.6 \text{ K}\Omega$$



For unbypass capacitor the voltage gain ( $A_v$ ) of common emitter amplifier we have,

$$A_v = \frac{-g_m R_C}{1 + g_m R_E}$$

Where,

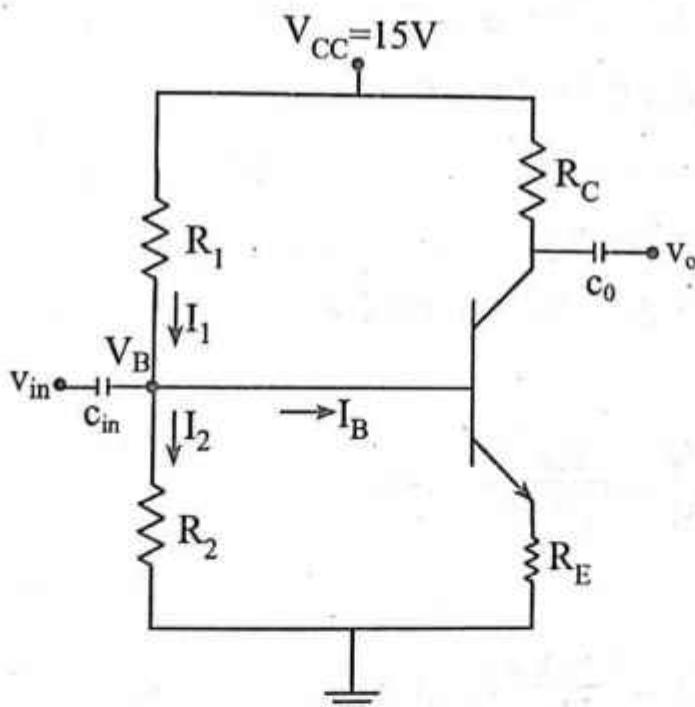
$$g_m = \frac{I_C}{\eta V_T} = \frac{1.5 \text{ mA}}{1 \times 25 \text{ mV}} = 0.06 \text{ mho}$$

$$\therefore A_v = \frac{-0.06 \times 6.4 \times 1000}{1 + 0.06 \times 1.6 \times 1000} = -3.96$$

- Q. Design voltage divider bias (Common emitter configuration) to get  $I_{CQ} = 1.5 \text{ mA}$ . Assume power supply voltage  $V_{CC} = 15 \text{ V}$  and beta of transistor is 110.

[2071 Chaitra Regular]

*Solution:*



Since  $V_{CC} \geq 15 \text{ VDC}$ , So using guideline 2

We have,

$$V_E = 0.1 V_{CC}$$

$$V_{RC} = 0.4 V_{CC}$$

$$V_{CE} = 0.5 V_{CC}$$

Now,

$$V_E = V_{RE} = I_E R_E = I_C R_E = 0.1 V_{CC}$$

$$\text{or, } R_E = \frac{0.1 V_{CC}}{I_C} = \frac{0.1 \times 15}{1.5 \text{mA}} = 1 \text{ K}\Omega$$

Also,

$$V_{RC} = I_C R_C = 0.4 V_{CC}$$

$$\text{or, } R_C = \frac{0.4 V_{CC}}{I_C} = \frac{0.4 \times 15}{1.5 \text{mA}} = 4 \text{ K}\Omega$$

Using stiff biasing (Our Choice)

$$R_2 = 0.01 \beta R_E = 0.01 \times 110 \times 1 \text{ K}\Omega = 1.1 \text{ K}\Omega$$

From figure,

$$I_1 = I_2 + I_B$$

$$R_1 = \frac{V_{R1}}{I_1} = \frac{V_{CC} - V_B}{I_2 + I_B} \dots\dots\dots \text{(i)}$$

Now, to find the values of equation (i)

$$V_{BE} = V_B - V_E$$

$$\text{or, } V_B = V_{BE} + V_E$$

$$= 0.7 + 0.1 V_{CC} = 2.2 \text{ V}$$

Also,

$$I_2 = \frac{V_B}{R_2} = \frac{2.2}{1.1 \text{K}\Omega} = 2 \text{ mA}$$

And,

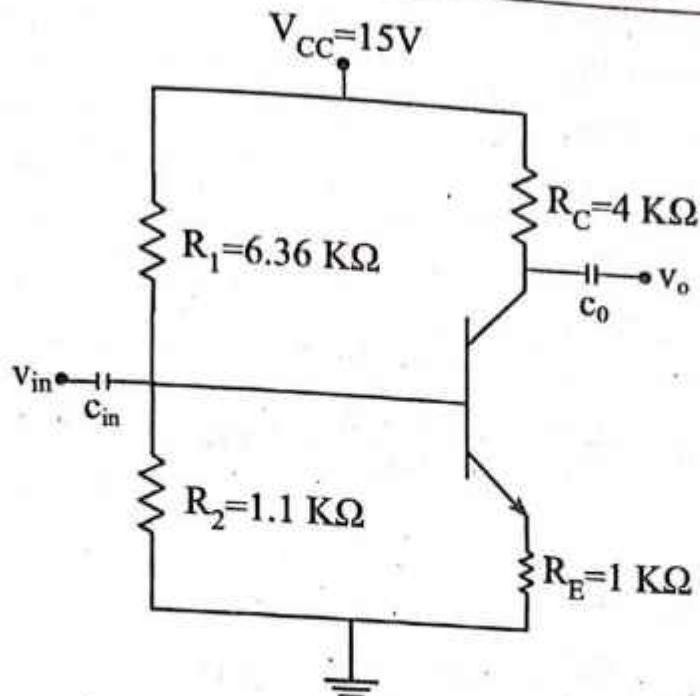
$$I_B = \frac{I_C}{\beta} = \frac{1.5 \text{mA}}{110} = 0.013 \text{ mA}$$

Now, equation (i) becomes,

$$\begin{aligned} \therefore R_1 &= \frac{V_{R1}}{I_1} = \frac{V_{CC} - V_B}{I_2 + I_B} \\ &= \frac{15 - 2.2}{(2 + 0.013)} = 6.36 \text{ K}\Omega \end{aligned}$$

Hence,

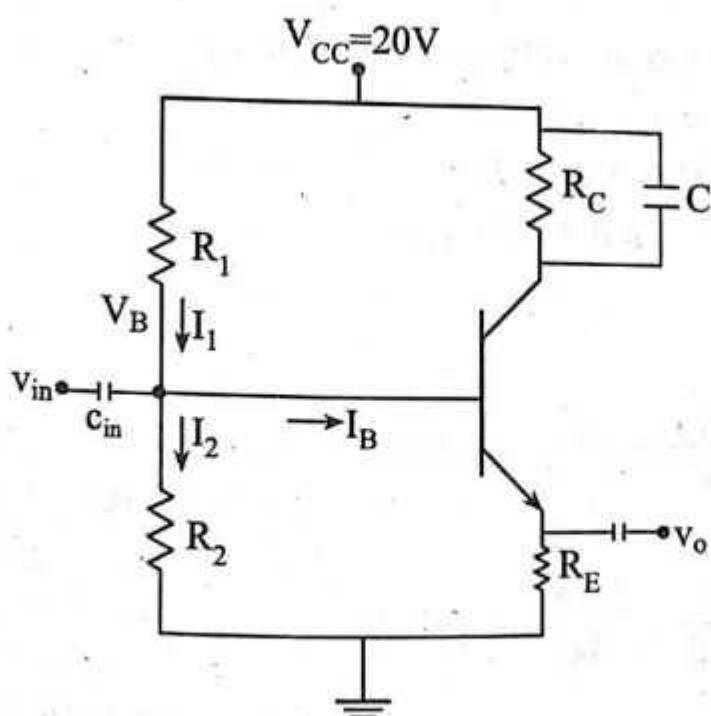
$$R_1 = 6.36 \text{ k}\Omega; R_2 = 1.1 \text{ k}\Omega; R_C = 4 \text{ k}\Omega; R_E = 1 \text{ k}\Omega$$



- Q. Design  $\beta$  independent type dc biased common collector amplifier and find its current gain and input resistance. Given parameters are:  $V_{CC} = 20 \text{ V}$ ,  $I_C = 2 \text{ mA}$ , and  $\beta = 100$ . Use firm biasing method.

[068 Baisakh Regular, 072 Chaitra Regular]

*Solution:*



Since  $V_{CC} > 15$  VDC, So using guideline 2

We have,

$$V_E = 0.1 V_{CC}$$

$$V_{RE} = 0.4 V_{CC}$$

$$V_{CE} = 0.5 V_{CC}$$

Also, for firm biasing

$$R_2 = 0.1 \beta R_E$$

Now,

$$V_E = V_{RE} = I_E R_E \approx I_C R_E = 0.1 V_{CC}$$

$$\text{or, } R_E = \frac{0.1 V_{CC}}{I_C} = \frac{0.1 \times 20}{2 \text{mA}} = 1 \text{K}\Omega$$

Also,

$$V_{RC} = I_C R_C = 0.4 V_{CC}$$

$$\text{or, } R_C = \frac{0.4 V_{CC}}{I_C} = \frac{0.4 \times 20}{2 \text{mA}} = 4 \text{K}\Omega$$

We know, for firm biasing,

$$R_2 = 0.1 \beta R_E = 0.1 \times 100 \times 1 = 10 \text{K}\Omega$$

From figure,

$$I_1 = I_2 + I_B$$

$$R_1 = \frac{V_{R1}}{I_1} = \frac{V_{CC} - V_B}{I_2 + I_B} \dots \dots \dots \text{(i)}$$

Now, to find the values of equation (i)

$$V_{BE} = V_B - V_E$$

$$\begin{aligned} \text{or, } V_B &= V_{BE} + V_E \\ &= 0.7 + 0.1 V_{CC} \\ &= 2.7 \text{ V} \end{aligned}$$

Also,

$$I_2 = \frac{V_B}{R_2} = \frac{2.7}{10 \text{K}\Omega} = 0.27 \text{ mA}$$

And,

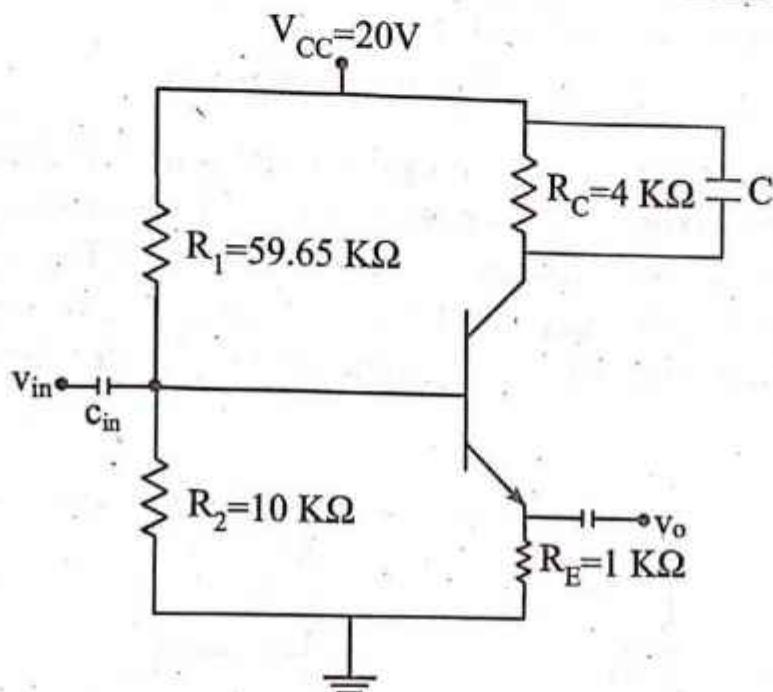
$$I_B = \frac{I_C}{\beta} = \frac{2 \text{mA}}{100} = 0.02 \text{mA}$$

Now, equation (i) becomes,

$$\begin{aligned}\therefore R_1 &= \frac{V_{R1}}{I_1} = \frac{V_{CC} - V_B}{I_2 + I_B} \\ &= \frac{20 - 2.7}{(0.27 + 0.02)\text{mA}} \\ &= 59.65 \text{ K}\Omega\end{aligned}$$

Hence,

$$R_1 = 59.65 \text{ K}\Omega; R_2 = 10 \text{ K}\Omega; R_C = 4 \text{ K}\Omega; R_E = 1 \text{ K}\Omega$$



We know,

$$g_m = \frac{I_C}{\eta V_T} = \frac{2\text{mA}}{1 \times 25\text{ mV}} = 0.08 \text{ mho}$$

Also,

$$\alpha = \frac{\beta}{\beta+1} = \frac{100}{101} = 0.99$$

Now, to find current gain and input resistance consider load is absent. Then for common collector amplifier,

$$R_{th} = R_1 // R_2 = 59.65 // 10 = 8.56 \text{ K}\Omega$$

Also,

$$R_{ib} = (\beta + 1)(R_E + r_e)$$

$$r_e = \frac{\alpha}{g_m} = \frac{0.99}{0.08} = 12.37 \Omega = 0.0123 K\Omega$$

Then,

$$R_{ib} = (\beta + 1) (R_E + r_e) = 101 \times (1 + 0.0123) = 102.24 K\Omega$$

We know,

a. Current gain ( $A_i$ )

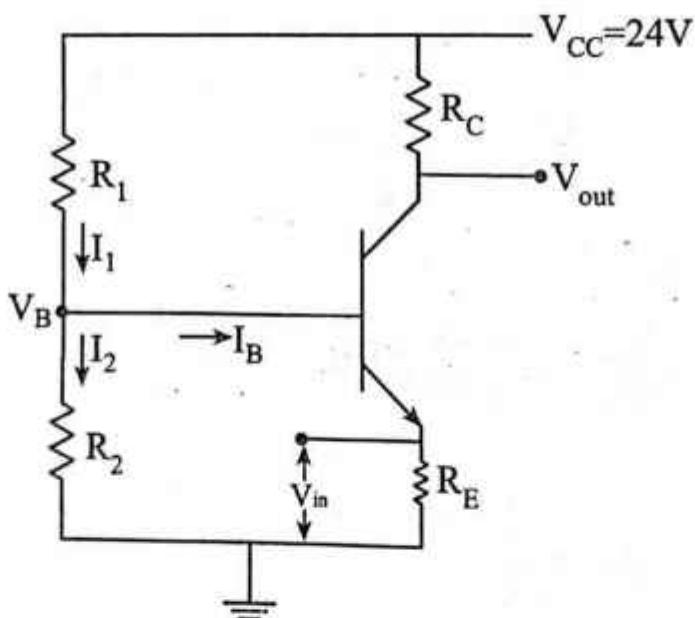
$$= \frac{(\beta+1)R_{th}}{(R_{th} + R_{ib})} = \frac{101 \times 8.56}{(8.56 + 102.24)} = 7.80$$

b. Input Resistance ( $R_{in}$ )

$$= R_{th} // R_{ib} = 8.56 // 102.24 = 7.89 K\Omega$$

- Q. Design common base amplifier using  $\beta$  - independent dc biasing method. Use appropriate guideline to support your design. Given parameters are  $V_{CC} = 24$  VDC,  $I_C = 1$  mA, and  $\beta = 200$ . Also find its voltage gain by using its ac equivalent circuit. [067 Ashad Regular/ 071 Shrawan Back]

*Solution:*



Since  $V_{CC} \geq 15$  VDC, So using guideline 2

We have,

$$V_E = 0.1 V_{CC}$$

$$V_{RC} = 0.4 V_{CC}$$

$$V_{CE} = 0.5 V_{CC}$$

Now,

$$V_E = V_{RE} = I_E R_E \approx I_C R_E = 0.1 V_{CC}$$
$$\text{or, } R_E = \frac{0.1 V_{CC}}{I_C} = \frac{0.1 \times 24}{1 \text{mA}} = 2.4 \text{ K}\Omega$$

Also,

$$V_{RC} = I_C R_C = 0.4 V_{CC}$$

$$\text{or, } R_C = \frac{0.4 V_{CC}}{I_C} = \frac{0.4 \times 24}{1 \text{mA}} = 9.6 \text{ K}\Omega$$

Using stiff biasing (Our Choice)

$$R_2 = 0.01 \beta R_E = 0.01 \times 200 \times 2.4 \text{ K}\Omega = 4.8 \text{ K}\Omega$$

From figure,

$$I_1 = I_2 + I_B$$

$$R_1 = \frac{V_{R1}}{I_1} = \frac{V_{CC} - V_B}{I_2 + I_B} \dots\dots\dots \text{(i)}$$

Now, to find the values of equation (i)

$$V_{BE} = V_B - V_E$$

$$\text{or, } V_B = V_{BE} + V_E$$

$$= 0.7 + 0.1 V_{CC}$$

$$= 3.1 \text{ V}$$

Also,

$$I_2 = \frac{V_B}{R_2} = \frac{3.1}{4.8 \text{K}\Omega} = 0.645 \text{ mA}$$

And,

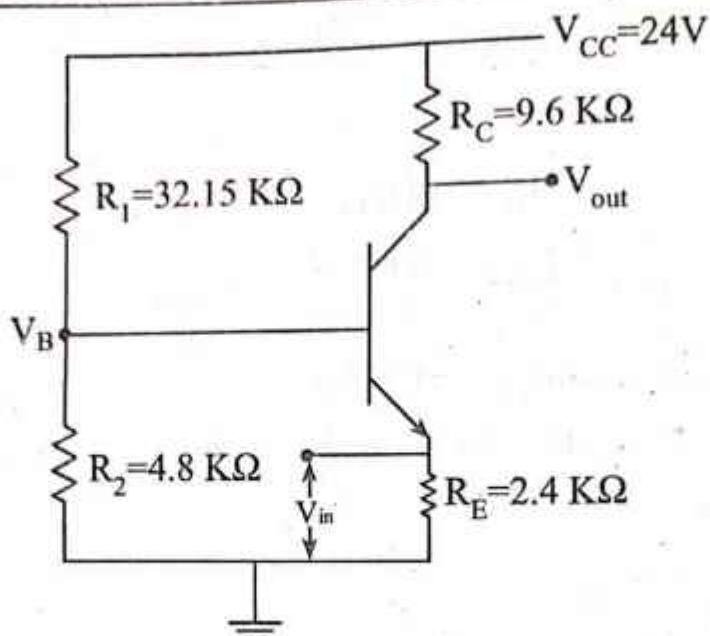
$$I_B = \frac{I_C}{\beta} = \frac{1 \text{mA}}{200} = 5 \times 10^{-3} \text{ mA}$$

Now, equation (i) becomes,

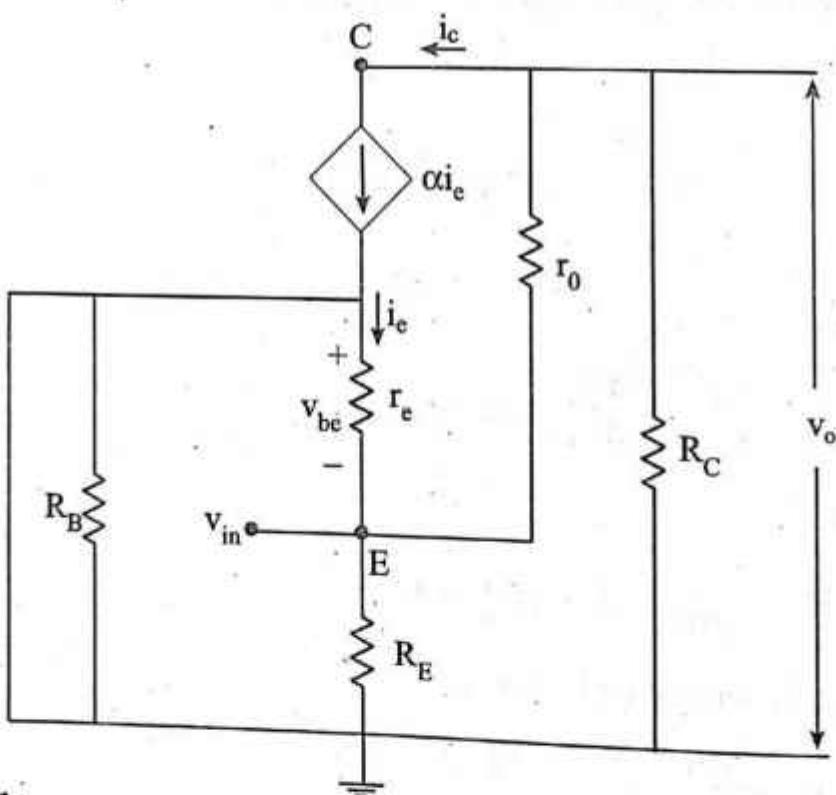
$$\therefore R_1 = \frac{V_{R1}}{I_1} = \frac{V_{CC} - V_B}{I_2 + I_B}$$
$$= \frac{24 - 3.1}{(0.645 + 5 \times 10^{-3})}$$
$$= 32.15 \text{ K}\Omega$$

Hence,

$$R_1 = 32.15 \text{ k}\Omega; R_2 = 4.8 \text{ k}\Omega; R_C = 9.6 \text{ k}\Omega; R_E = 2.4 \text{ k}\Omega$$



Now, drawing the ac equivalent T-model for common base amplifier configuration



We know,

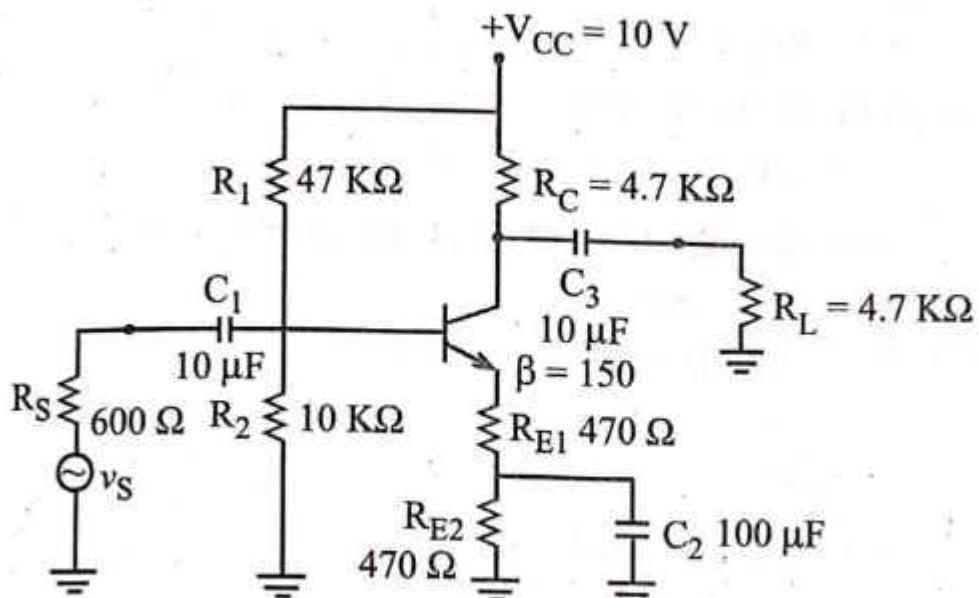
Voltage gain ( $A_v$ ) =  $g_m R_C$   
Where,

$$g_m = \frac{I_C}{V_T} = \frac{1 \text{ mA}}{25 \text{ mV}} = 0.04 \text{ mho}$$

Then

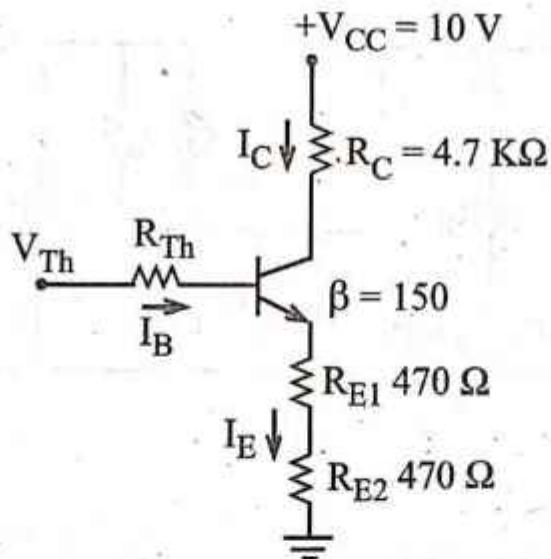
$$Av = g_m R_C = 0.04 \times 9.6 \times 1000 = 384$$

- Q. Determine the input resistance, output resistance and overall voltage gain of the circuit given below:



Solution:

For dc analysis the equivalent thevenin circuit



$$V_{Th} = V_{CC} \times \frac{R_2}{R_1 + R_2}$$

$$= 10 \times \frac{10}{47+10}$$

$$= \frac{100}{57} = 1.8 \text{ V}$$

$$R_{Th} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

$$= \frac{47 \times 10}{47 + 10}$$

$$= 8.2 \text{ k}\Omega$$

Applying KVL we have,

$$V_{Th} = I_B R_{Th} + V_{BE} + I_E (R_{E1} + R_{E2})$$

$$\text{or, } 1.8 = I_B \times 8.2 + 0.7 + (\beta + 1) I_B (470 + 470) \times 10^{-3}$$

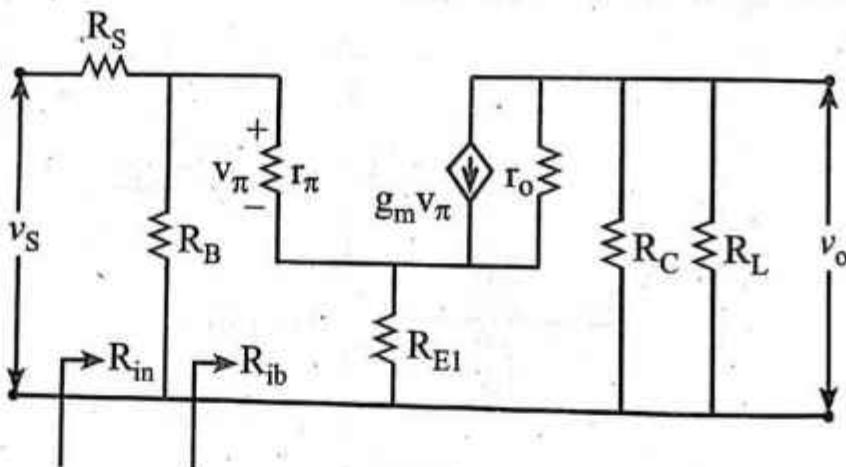
$$\text{or, } I_B = \frac{1.8 - 0.7}{8.2 + 151 \times 0.9}$$

$$= \frac{1.1}{144.1}$$

$$I_B = 7.633 \times 10^{-3} \text{ mA}$$

$$\therefore I_C = \beta I_B = 1.145 \text{ mA}$$

The ac equivalent circuit for given circuit



We have

Input Resistance (\$R\_{in}\$):

$$R_{in} = R_B \parallel R_{ib}$$

$$= R_B \parallel r_\pi (1 + g_m R_{E1})$$

$$R_B = R_1 \parallel R_2 = 8.2 \text{ k}\Omega$$

$$g_m = \frac{I_C}{V_T} = \frac{1.145 \text{ mA}}{25 \text{ mV}} = 0.0458 \text{ U}$$

$$r_\pi = \frac{b}{g_m} = \frac{150}{0.0458} = 3275.109 \Omega$$

$$\therefore R_{ib} = r_\pi (1 + g_m R_E) \\ = 3275.109 (1 + 0.0458 \times 470) \\ = 73775.10533 \Omega = 73.77 \text{ k}\Omega$$

$$\therefore R_{in} = R_B || R_{ib} \\ = 8.2 || 73.77 \\ = \frac{8.2 \times 73.77}{8.2 + 73.77} \\ = \frac{604.914}{81.97} \\ = 7.73 \text{ k}\Omega$$

Output Resistance ( $R_{out}$ ):

$$R_{out} = R_C || R_L \\ = 4.7 || 47 \\ = \frac{4.7 \times 47}{4.7 + 47} \\ = \frac{220.9}{51.7} \\ = 4.72 \text{ k}\Omega$$

Voltage gain ( $A_v$ ):

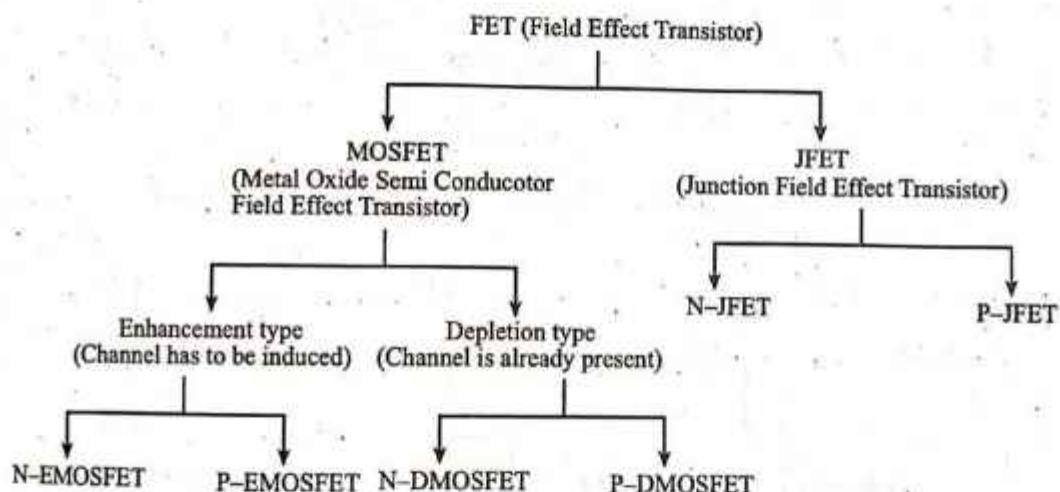
$$A_v = \frac{-g_m R_C}{1 + g_m R_E} \\ = \frac{-0.0458 \times 4.7 \times 10^3}{1 + 0.0458 \times 470} \\ = \frac{-215.26}{22.526} \\ = -9.55$$

1. Draw hybrid- $\pi$  model of BJT.
2. Design a common base amplifier circuit using  $\beta$ -independent dc biasing method. Given parameters are:  $V_{CC} = 15$  V DC,  $I_E = 1.5$  mA,  $\beta = 100$  and input and output impedances are comparatively large. Use appropriate guidelines to support your design.
3. Design  $\beta$ -independent type dc biased common collector amplifier, and find its current gain and input resistance. Given parameters are:  $V_{CC} = 20$  V,  $I_C = 2$  mA,  $\beta = 100$  and use firm biasing method.
4. Derive an expression to find output resistance for emitter unbypassed common emitter amplifier circuit.
5. Draw  $\beta$ -independent type and emitter resistance unbypassed common emitter amplifier and derive its voltage gain using its ac equivalent circuit.
6. Write an expression for voltage gain of common emitter amplifier circuit with emitter resistance bypassed and give the two reasons to connect bypass capacitor in the circuit.
7. Draw Ebers Moll model and ac equivalent T- model for BJT.
8. Derive an expression to find input resistance and voltage gain for common collector amplifier with its equivalent model.

# FIELD – EFFECT TRANSISTOR

## Introduction

The previous chapter covered bipolar junction transistor, which utilizes a small current to control to control a large current. In this chapter, we will introduce the general concept of the **Field effect Transistor** – a device utilizing a small voltage to control current. Field effect transistors are unipolar which mean conduction is due to only type of charge carriers' i.e., either by electrons or holes. We will discuss in detail about structure and operation of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and Junction Field Effect Transistor (JFET).



### 3.1 Structure and Physical Operation of Enhancement type MOSFET

## Structure

The basic structure of enhancement type N-MOSFET is shown in fig 3.1(a). A slab of P-type substrate is formed in which two heavily doped N-type regions (N-Source & N-Drain) are created. A thin ( $\approx 0.1 \mu\text{m}$ ) layer of metal oxide ( $\text{SiO}_2$ ), which is excellent electrical insulator, is formed covering the area between the source and drain regions. Metal contacts are made

to those regions to bring out four terminals: Gate (G), Source (S), Drain (D), & Substrate or Body (B).

Another name for the MOSFET is insulated gate-FET or IGFET. In some cases substrate is internally connected to source terminal. MOSFET's are very popular in designing micro-power circuits and high impedance amplifiers because MOSFET's have very high input resistance and consume very low power.

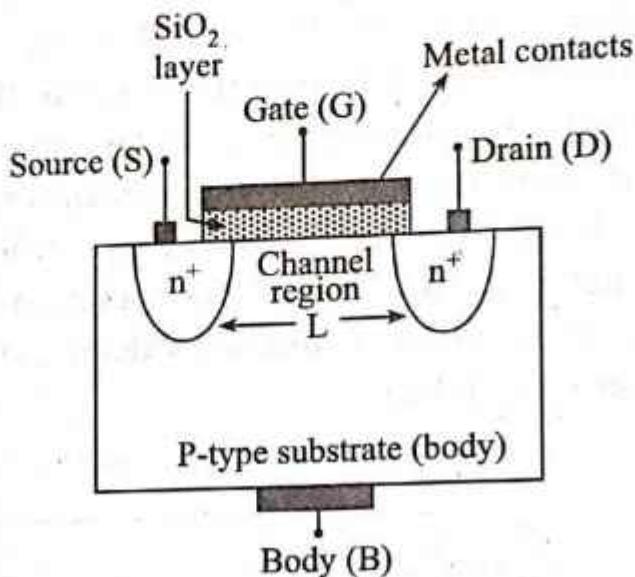


Fig.3.1 (a) Construction of E-MOSFET

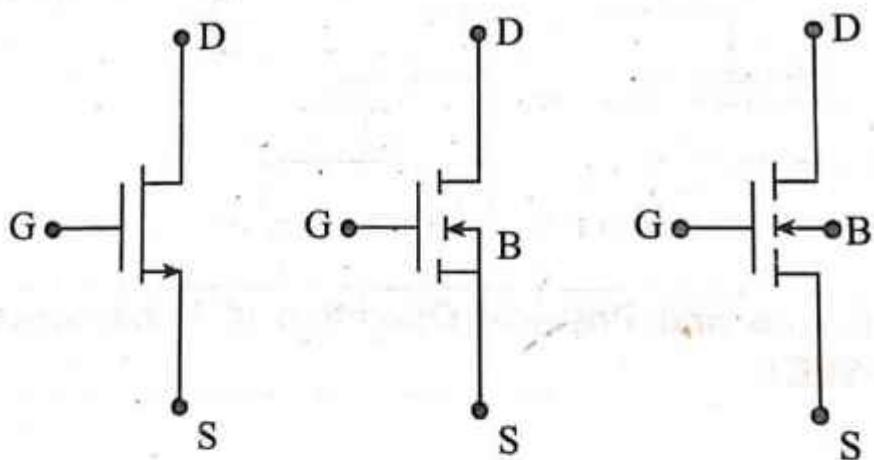


Fig.3.1 (b) Circuit Symbols of N - EMOSFET

## Physical Operation

With no bias voltage applied to the gate, two back to back diodes exist in series between drain and source prevents current conduction from drain to source.

## When $V_{DS}$ is applied and small

Initially drain to source channel is at cutoff state i.e. no conducting channel. When positive gate to source voltage ( $V_{GS}$ ) is applied, channel starts to build as shown in fig 3.1(c).

Here, when  $V_{GS}$  applied, positive voltage on gate causes free holes (positive charges) to be repelled from substrate region under the gate channel region. These holes are pushed downwards into the substrate, leaving behind populated bound negative charges. Also, positive gate voltage attracts electrons from source and drain regions into channel regions. These sufficient accumulated electrons create N region connecting source and drain. The induced N region thus forms a channel for current flow from drain to source. This channel is created inverting the substrate surface from P type to N type, hence is called inversion layer.

The value of  $V_{GS}$  at which sufficient number of mobile electrons accumulates in the channel region to form a conducting channel is called threshold voltage ( $V_t$ ).  $V_t$  is positive for N -channel MOSFET.

I.e. When  $V_{GS} \geq V_t$ ; channel is induced.

Thus at  $V_{GD} = V_t$ , channel is at threshold of pinch-off state i.e. at the point between ohmic region and pinch-off region.

When  $V_{GD} > V_t$  i.e.  $(V_{GS} - V_{DS}) > V_t$

$$V_{DS} < V_{GS} - V_t$$

The channel is continuous and the conductance of the induced channel is proportional to excessive gate voltage ( $V_{GS} - V_t$ ) for small drain to source voltage ( $V_{DS}$ ). The E-MOSFET operates in ohmic region or triode region (i.e. device operates as a linear resistor).

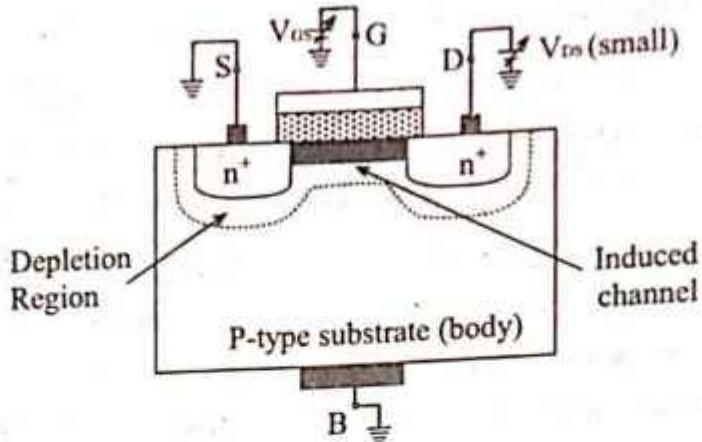


Fig 3.1(c) When  $V_{DS}$  is small

### When $V_{DS}$ is Increased

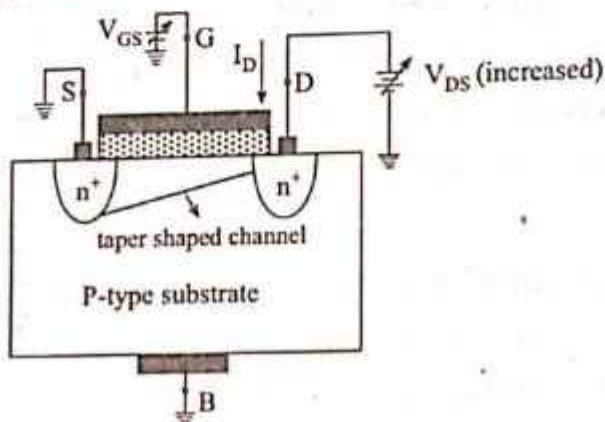


Fig 3.1(d) When  $V_{DS}$  is increased

When  $V_{DS}$  is increased sufficiently so that  $V_{GS} > V_t$ . For this  $V_{DS}$  appears as a voltage drop across the length of the channel ( $L$ ) travelling along the channel from source to drain. This results varying voltage between gate and the point along channel which is  $V_{GS}$  at the source end and  $V_{GS} - V_{DS}$  at the drain end.

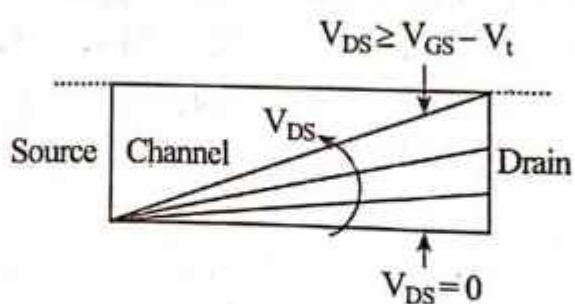


Fig 3.1(e) Effect of  $V_{DS}$  on the shape of channel

This creates non-uniform tapered shape channel, because channel depth depends on this voltage ( $V_{DS}$ ). As  $V_{DS}$

increases, the channel becomes more tapper and its resistance increases correspondingly. Thus the  $I_D$  -  $V_{DS}$  curves bends eventually. When  $V_{DS}$  is increased to the value that reduces the voltage between gate and channel at the drain end to  $V_t$  (i.e.  $V_{GS} - V_{DS} = V_t$ ), the channel depth at drain end decreases to almost zero and the channel is said to be pinched-off.

Increasing  $V_{DS}$  beyond this value has little effect on channel shape and the current through channel remains constant. The drain current saturates at this value and the MOSFET is said to have entered the saturation region of operation. The region of  $I_D$ - $V_{DS}$  characteristics obtained for  $V_{DS} < V_{DS_{sat}}$  is called the triode region. It is shown in fig 3.1(e).

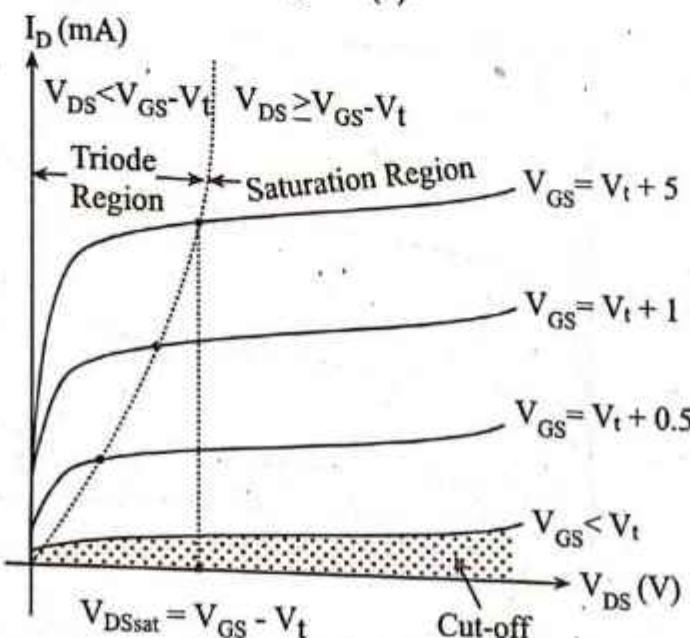


Fig: 3.1(f) Drain characteristics curve

### 3.2 Current Voltage Characteristics of E-MOSFET

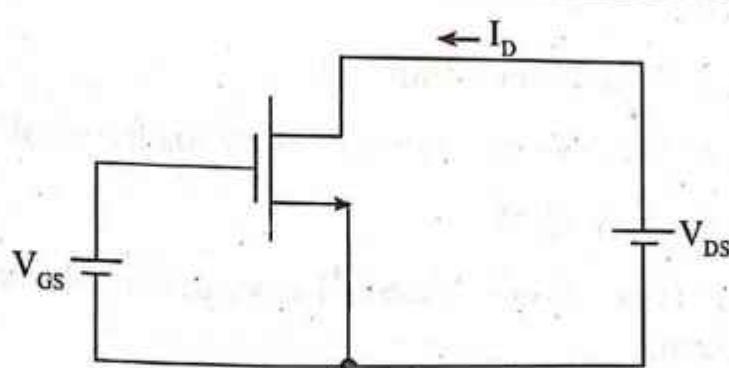
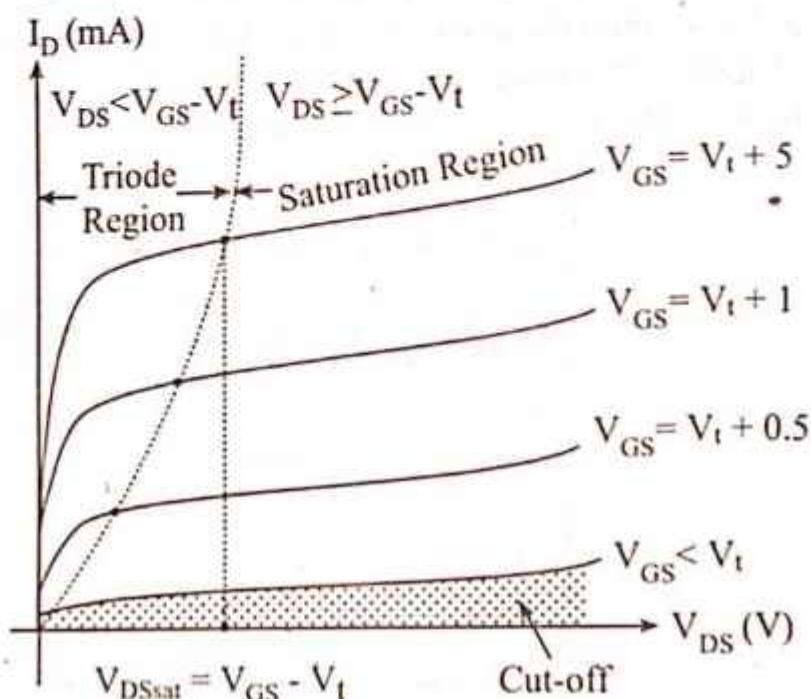


Fig 3.2(a) Conceptual Circuit to Study Characteristics of MOSFET

The conceptual circuit to study characteristics curve of MOSFET is shown in fig 3.2 (a). The following characteristics curve indicates that there are three distinct regions of operation:

- Cut-off region,
- Triode region and
- Saturation region.



*Fig. 3.2(b) Drain characteristics curve of EMOSFET*

The E-MOSFET is in cutoff when  $V_{GS} < V_t$  and to operate it in the triode region, channel must be induced and for this we have

$V_{GS} \geq V_t$ , channel is induced.

When  $V_{GS} > V_t$ , channel is continuous for small  $V_{DS}$

i.e.  $(V_{GS} - V_{DS}) > V_t$

$V_{DS} < (V_{GS} - V_t)$  i.e. MOSFET operates in Ohmic region (Triode region).

The general expression for E-MOSFET is given by following approximate equation

$$I_D = K [2(V_{GS} - V_t) \cdot V_{DS} - V_{DS}^2] \dots \dots \dots \quad (i)$$

Where,

$$K = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} = \frac{1}{2} K'_n \frac{W}{L} = \text{device parameter}$$

$$K'_n = \mu_n C_{\text{ox}}$$

$\mu_n$  = electron mobility in induced channel

**C<sub>ox</sub>** = oxide capacitance per unit area

L = Length of channel

$W$  = width of channel

In Ohmic region or triode region of operation,  $V_{DS}$  is very small so  $V_{DS}^2$  can be neglected.

Now equation (i) becomes

$$I_D = K [2(V_{GS} - V_t) V_{DS} - 0]$$

$$\frac{V_{DS}}{I_D} = R_{DS} = \frac{1}{2 K(V_{GS} - V_t)}$$

The value of  $R_{DS}$  is controlled by  $V_{GS}$ . So, it is called voltage controlled resistance.

When  $V_{DS}$  is increased sufficiently so that  $V_{GD} \leq V_t$ , the channel is pinched off i.e.

$$V_{GD} \leq V_t$$

$$\text{or, } V_{GS} - V_{DS} \leq V_t$$

or,  $V_{DS} \geq (V_{GS} - V_t)$ ; pinched off.

The boundary between the triode region and the saturation region is characterized by

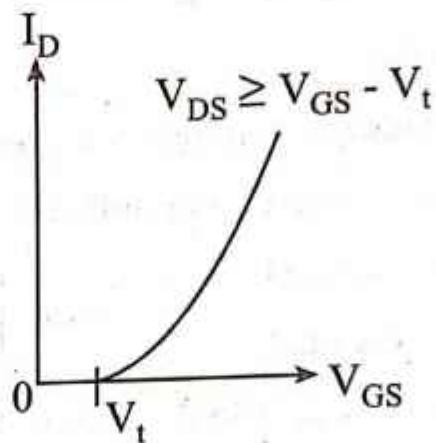
$$V_{DS} = (V_{GS} - V_t); \text{ boundary}$$

Beyond this value of  $V_{DS}$ ,  $I_D$  does not increase.

Put  $V_{DS} = V_{GS} - V_t$  in equation (i) we get

$$I_{Dsat} = K(V_{GS} - V_t)^2$$

In saturation the MOSFET provides a drain current whose value is independent of the drain voltage  $V_{DS}$  and is determined by the gate voltage  $V_{GS}$  according to the square law relationship.



*Fig3.2(c) Transfer Characteristics of EMOSFET*

### 3.3 The Depletion Type MOSFET

For depletion type N channel MOSFET an N channel is diffused on P type substrate (body). Then two heavily doped N type wells are formed at both sides of the channel. One of these two wells functions as Source (S) and the second well functions as Drain (D). A thin layer of silicon-oxide ( $\text{SiO}_2$ ) is developed on the top of the N-channel. Then a metal contact is formed and a gate (G) terminal is taken out. The structure is shown in fig3.3 (a).

Its structure is similar to that of E-MOSFET and the main difference is depletion MOSFET has a physically implanted channel. Thus if a voltage  $V_{DS}$  is applied between drain and source, a current  $i_D$  flow for  $V_{GS} = 0$ . In other words, there is no need to induce channel unlike the E-MOSFET.

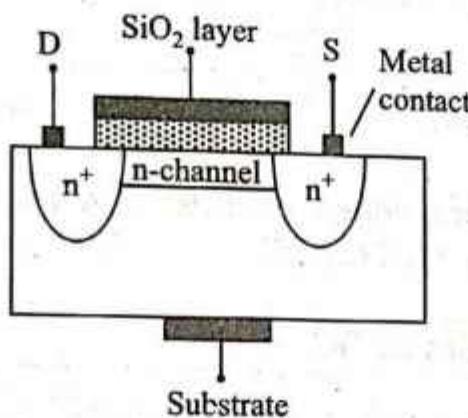
The channel depth and hence its conductivity can be controlled by  $V_{GS}$  as in E-MOSFET. Applying a positive  $V_{GS}$  enhances the channel by attracting more electrons into it. However, we can also apply a negative  $V_{GS}$ , which causes electrons to be repelled from the channel and thus channel becomes thinner. The negative  $V_{GS}$  is said to deplete the

channel and this mode of operation (negative  $V_{GS}$ ) is called depletion mode. As magnitude of  $V_{GS}$  increases in negative direction a value is reached at which channel is completely depleted of charge carriers and  $i_D$  is reduced to zero. This negative value of  $V_{GS}$  is the threshold voltage of the N channels D-MOSFET.

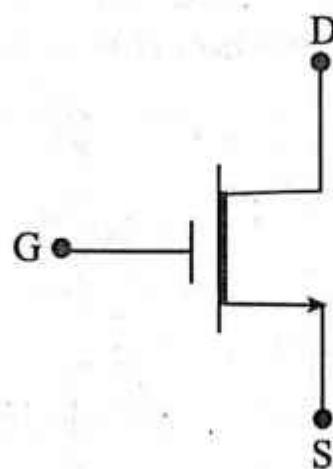
Thus an N channel D-MOSFET can be operated in enhancement mode by applying positive  $V_{GS}$  and in depletion mode by applying negative  $V_{GS}$ .

The current-voltage characteristics of D-MOSFET are described by the equations similar for the enhancement type except that for an N channel depletion type,  $V_t$  is negative. For D-MOSFET the value of drain current obtained in saturation with  $V_{GS} = 0$  is denoted by  $I_{DSS}$  and given by

$$I_{DSS} = KV^2_t.$$



*Fig.3.3 (a) Construction of N-DMOSFET*



*Fig 3.3(b) Symbol of N- DMOSFET*

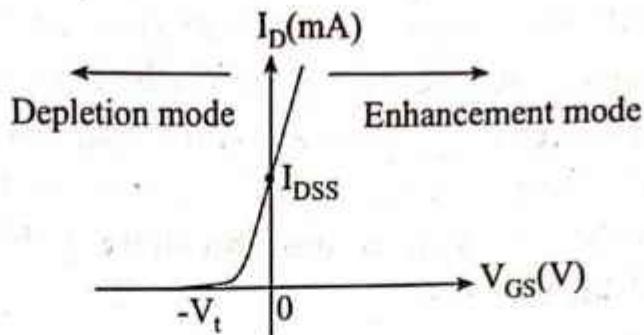


Fig 3.3(c) Transfer characteristics for D-type MOSFET

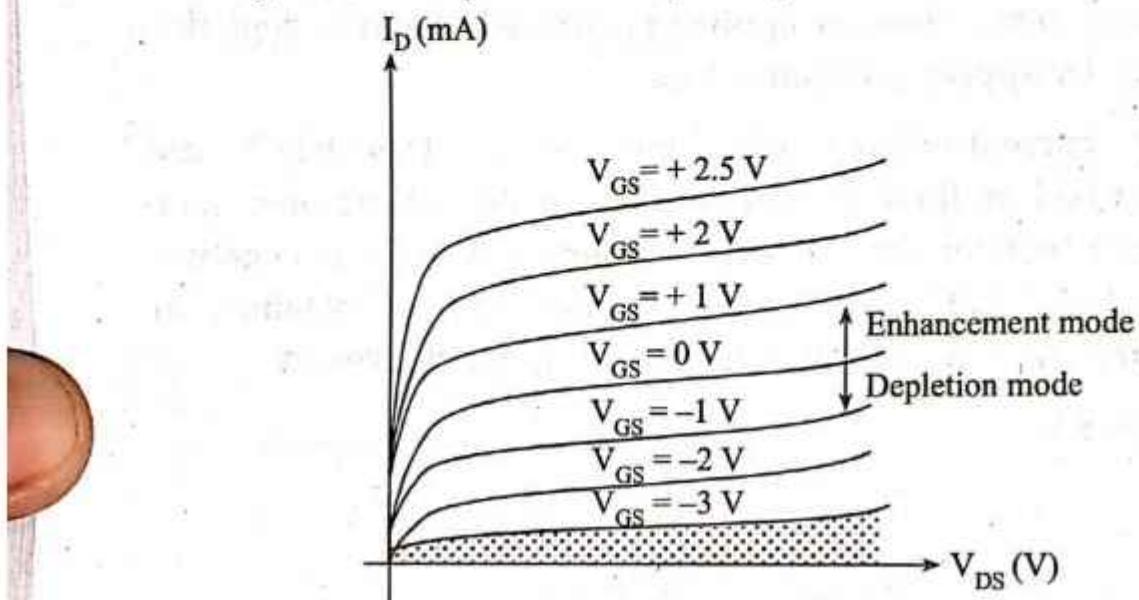
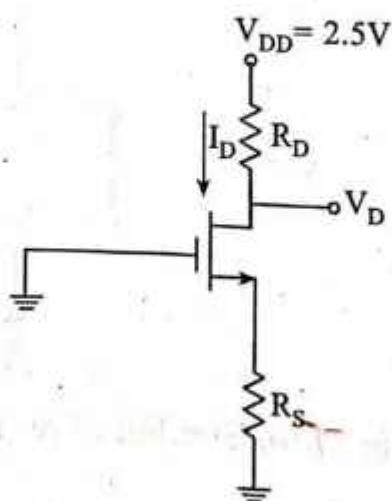


Fig. 3.3 (d) Drain characteristic of n channel depletion and enhancement MOSFET.

### 3.4 MOSFET Circuits at DC

Design the circuit below so that MOSFET operates at  $I_D = 0.4$  mA and  $V_D = + 0.5\text{ V}$ . The NMOSFET has  $V_t = 0.7\text{ V}$ ,  $\mu_n C_{ox} = K'_n = 100 \mu\text{A/V}^2$ ,  $L = 1\mu\text{m}$  and  $W = 32 \mu\text{m}$ . Neglect the channel - length modulation effects. (i.e.  $\lambda = 0$ )



*Solution:*

Since  $V_D = 0.5 \text{ V} > V_t$  transistor is operating in saturation region.

$$I_D = K (V_{GS} - V_t)^2 \quad [\text{For saturation region}]$$

$$= \frac{1}{2} \mu_n C_o x \frac{W}{L} (V_{GS} - V_t)^2$$

Assume  $V_{GS} - V_t = V_{ov}$ ;  $I_D = 0.4 \text{ mA} = 400 \mu\text{A}$ ;

$\mu_n C_o x = 100 \mu\text{A/V}^2$  and

$$\frac{W}{L} = 32 \text{ then,}$$

$$\text{or, } 400 = \frac{1}{2} \times 100 \times 32 \times (V_{ov})^2$$

$$\therefore V_{ov} = 0.5 \text{ V}$$

$$\therefore V_{ov} = V_{GS} - V_t$$

$$\text{or, } V_{GS} = V_t + V_{ov} = 0.7 + 0.5 = 1.2 \text{ V}$$

From figure gate is at ground potential (i.e.  $V_G = 0$ )

$$\therefore V_{GS} = V_G - V_S$$

$$\text{or, } V_{GS} = 0 - V_S$$

$$\therefore V_S = -V_{GS} = -1.2 \text{ V}$$

From fig

$$V_{DD} = I_D R_D + V_D$$

$$\text{or, } R_D = \frac{V_{DD} - V_D}{I_D} = \frac{(2.5 - 0.5) \text{ V}}{0.4 \text{ mA}} = 5 \text{ k}\Omega$$

$$\therefore R_S = \frac{V_S - V_{SS}}{I_D} = \frac{[-1.2 - (-2.5)] \text{ V}}{0.4 \text{ mA}} = 3.25 \text{ k}\Omega$$

[Note: Here we keep reference value  $V_{SS} = -2.5 \text{ V}$  because if we keep  $V_{SS} = 0$  then value of  $R_S$  will be in negative]

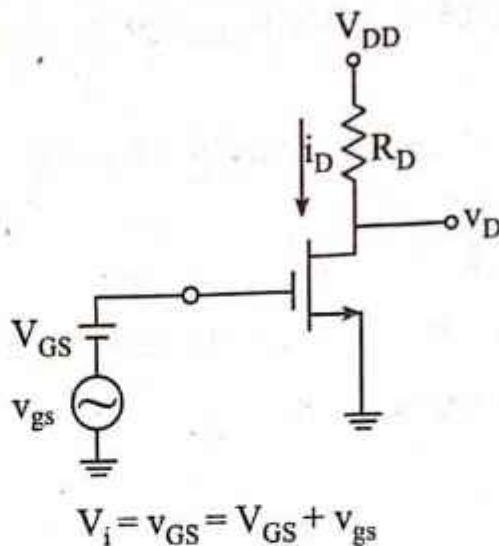


Fig. 3.5(a) MOSFET as an Amplifier

To operate MOSFET as an amplifier, it should be in saturation region. MOSFET acts as a voltage controlled current source (VCCS) i.e. changes in the  $V_{GS}$  give rise to change in drain current  $i_D$ . Basic structure of the common source amplifier is shown in fig 3.5 (a).

As shown above,  $V_{GS}$  is the dc bias voltage for E-MOSFET and  $v_{gs}$  is the input signal to be amplified superimposed on  $V_{GS}$ . The output is taken from the drain end.

Initially  $v_{gs} = 0$ , thus only dc analysis

$$I_D = K(V_{GS} - V_t)^2$$

Also the dc voltage at the drain i.e. output voltage

$$V_D = V_{DD} - I_D R_D$$

To ensure that MOSFET is in saturation region,

$$V_{DS} > V_{GS} - V_t$$

Now when  $v_{gs}$  is applied

$$v_{GS} = V_{GS} + v_{gs}$$

The total instantaneous drain current

$$i_D = K(v_{GS} - V_t)^2$$

$$\text{or, } i_D = K(V_{GS} + v_{gs} - V_t)^2$$

$$\text{or, } i_D = K(V_{GS} - V_t)^2 + 2Kv_{gs}(V_{GS} - V_t) + Kv_{gs}^2$$

Here, first term in RHS is dc bias current  $I_D$ , second term represents a current component proportional to  $v_{gs}$  and the third component is proportional to square of  $v_{gs}$ . This third term represents non-linear distortion and is undesirable.

So for non-linear distortion to be low

$$Kv_{gs}^2 \ll 2Kv_{gs}(V_{GS} - V_t)$$

$$\text{or, } v_{gs} \ll 2(V_{GS} - V_t)$$

If this condition is satisfied  $Kv_{gs}^2$  term can be neglected and hence

$$i_D = I_D + i_d = K (V_{GS} - V_t)^2 + 2Kv_{gs}(V_{GS} - V_t)$$

Comparing ac to ac and dc to dc we have,

$$I_D = K (V_{GS} - V_t)^2$$

$$i_d = 2Kv_{gs}(V_{GS} - V_t)$$

$$g_m = \frac{i_d}{v_{gs}} = 2K (V_{GS} - V_t)$$

Where  $g_m$  = trans-conductance of the MOSFET.

$$i_d = g_m v_{gs}$$

Now, the total instantaneous drain voltage is

$$v_D = V_{DD} - i_D R_D$$

$$\text{or, } V_D + v_d = V_{DD} - (I_D + i_d) R_D$$

$$= (V_{DD} - I_D R_D) - i_d R_D$$

Thus the signal component of drain voltage is

$$v_d = -i_d R_D = -g_m v_{gs} R_D$$

$$\text{Voltage Gain (A}_v\text{)} = \frac{v_d}{v_{gs}}$$

$$= \frac{\text{output voltage}}{\text{input voltage}} = -g_m R_D.$$

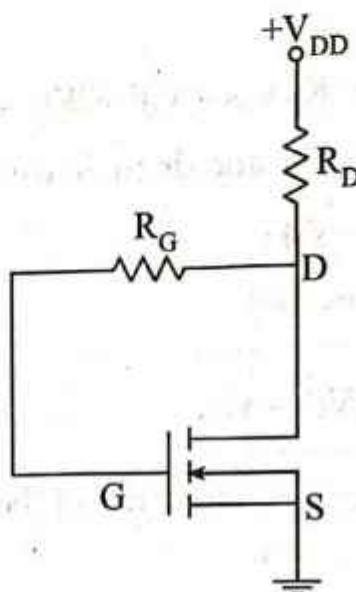
This relation (negative sign) shows that output signal is  $180^\circ$  out of phase with respect to input signal and is amplified.

### 3.6 Biasing in MOS Amplifier Circuits

Biasing in MOSFET circuits means determining the operating point i.e. operating drain current ( $I_D$ ) and gate to source voltage ( $V_{GS}$ ) for MOSFET circuit. We know for  $V_{GS}$  less than  $V_t$  (threshold voltage)  $I_D$  is zero for E-MOSFET and for  $V_{GS} > V_t$ ,  $I_D$  is given by

$$I_D = k (V_{GS} - V_t)^2$$

**Feedback Biasing Method (Drain Feedback Bias):**



Here, a high resistance  $R_G$  is connected between drain and the gate. Since the gate resistance ( $R_G$ ) is very high, no current will flow in the gate circuit ( $I_G=0$ ). So, no voltage will drop across  $R_G$ . This makes the gate will be at the same potential as the drain.

Therefore

$$V_D = V_G \text{ and } V_{DS} = V_{GS}$$

From figure

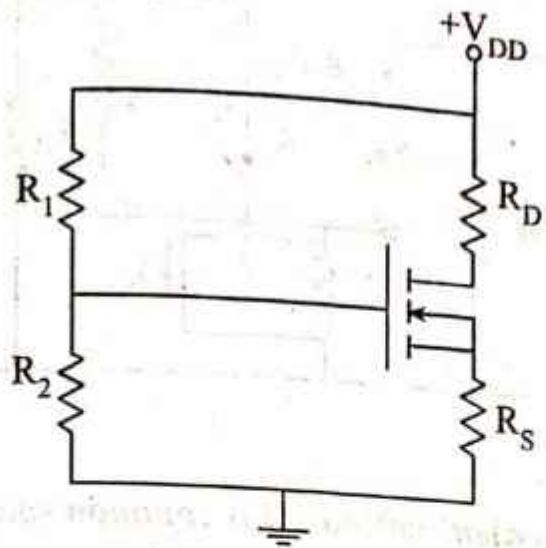
$$V_{DS} = V_{DD} - I_D R_D$$

Now

$$V_{GS} = V_{DS} = V_{DD} - I_D R_D$$

$$\text{or, } I_D = (-1/R_D) V_{GS} + V_{DD}/R_D.$$

## E-MOSFET Bias by voltage Divider method:



$$V_G = \left( \frac{R_2}{R_1 + R_2} \right) V_{DD} \quad \dots \dots \dots (1)$$

$$V_{DS} = V_{DD} - I_D R_D - I_D R_S \quad \dots \dots \dots (2) \quad [I_D \approx I_S]$$

$$I_D = K(V_{GS} - V_t)^2 \quad \dots \dots \dots (3) \quad (\text{For saturation region})$$

### Small Signal (AC) Equivalent Circuit Model of Common Source Amplifier:

MOSFET behaves as a voltage controlled current source. It accepts an input signal  $v_{gs}$  between gate and source and provides a current  $g_m v_{gs}$  at the drain terminal. The input resistance is very high ideally infinite and also the output resistance high. So we can represent MOSFET by the equivalent circuit shown in below fig.

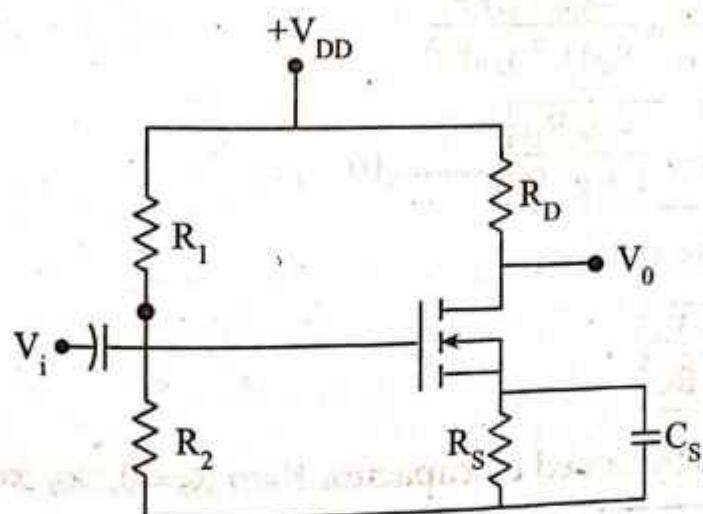


Fig.E-MOSFET voltage - divider configuration

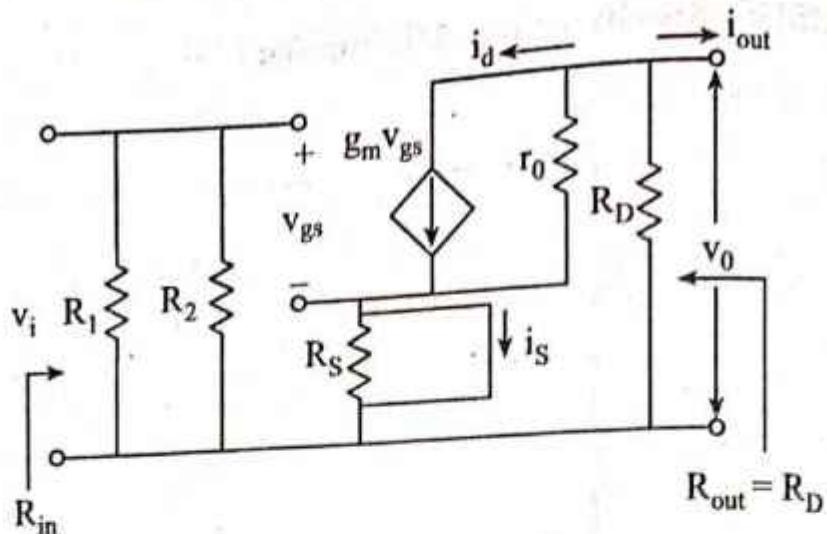


Fig: AC equivalent network for common source amplifier using FET.

To find voltage gain when bypass capacitor ( $C_S$ ) is absent.

$$\begin{aligned}
 v_o &= i_{out} R_{out} \\
 &= -i_d R_D \\
 &= -g_m v_{gs} R_D
 \end{aligned}
 \quad [\text{Ignoring the effect of } r_0]$$

Also,

$$\begin{aligned}
 v_{in} &= v_{gs} + i_S R_S \\
 &= v_{gs} + i_d R_S \quad [ \because i_S \approx i_d ] \\
 &= v_{gs} + g_m v_{gs} R_S \\
 &= v_{gs} (1 + g_m R_S)
 \end{aligned}$$

We know,

$$\begin{aligned}
 A_v &= \frac{v_o}{v_{in}} = \frac{-g_m v_{gs} R_D}{v_{gs} (1 + g_m R_S)} \\
 \therefore A_v &= \boxed{\frac{-g_m R_D}{1 + g_m R_S}} \dots\dots\dots (i)
 \end{aligned}$$

If  $g_m R_S \gg 1$  then

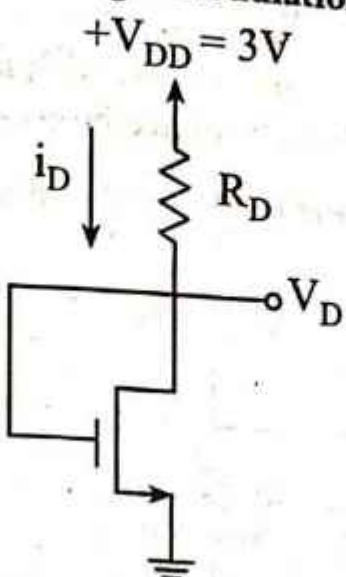
$$\boxed{A_v = \frac{-R_D}{R_S}}$$

If  $R_S$  is bypassed by capacitor then  $R_S \approx 0$ . So, from (i)

$$\boxed{A_v = -g_m R_D}$$

This relation shows that output signal is  $180^\circ$  out of phase with respect to input signal and is amplified.

- Q. Design circuit below to obtain  $I_D = 80 \mu A$ . Find  $R_D$  and  $V_D$ . Given  $V_t = 0.6V$ ,  $K'n = 200 \mu A/V^2$ ,  $L = 0.8 \mu m$ ,  $W = 4\mu m$ . Neglect the channel length modulation effect (i.e.  $\lambda = 0$ ).



*Solution:*

$$\text{Here, } V_D = V_G$$

So FET is in saturation region,

$$\therefore I_D = K [V_{GS} - V_t]^2$$

$$\text{or, } I_D = \frac{1}{2} \mu_n C_o x \frac{W}{L} (V_{GS} - V_t)^2$$

Assume  $V_{ov} = V_{GS} - V_t$ , then

$$I_D = \frac{1}{2} \mu_n C_o x \frac{W}{L} V_{ov}^2$$

$$\text{or, } V_{ov} = \sqrt{\frac{2I_D}{\mu_n C_o x \left(\frac{W}{L}\right)}}$$

$$\text{or, } V_{ov} = \sqrt{\frac{2 \times 80 \times 10^{-6}}{200 \times 10^{-6} \times \left(\frac{4}{0.8}\right)}}$$

$$\therefore V_{ov} = 0.4 \text{ V}$$

$$\text{or, } V_{GS} = V_t + V_{ov} = 0.6 + 0.4 = 1 \text{ V}$$

$$\text{or, } V_G - V_S = 1 \text{ V}$$

$$\therefore V_G = 1V \quad [\because V_S = 0V]$$

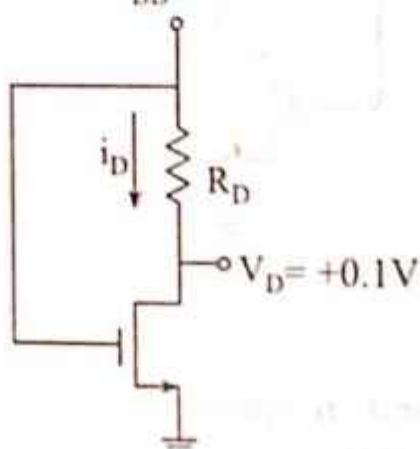
$$\therefore V_D = V_G = 1V$$

Then,

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{3 - 1}{0.080} = 25000\Omega = 25K\Omega$$

- Q. Design the circuit below to establish a drain voltage of 0.1V what is the effective resistance between drain and source at this operating point? Let  $V_t = 1V$  and  $K'n\frac{W}{L} = 1mA/V^2$ .

$$V_{DD} = +5V$$



**Solution:**

Since the drain voltage is less than gate voltage MOSFET is in triode region of operation.

So,

$$I_D = K [2(V_{GS} - V_t), V_{DS}]$$

$$= \frac{1}{2} \mu_n C_o \frac{W}{L} [2(V_{GS} - V_t), V_{DS}]$$

$$= \frac{1}{2} K' n \frac{W}{L} [2(V_{GS} - V_t), V_{DS}]$$

$$= K' n \frac{W}{L} [(V_{GS} - V_t), V_{DS}]$$

$$= 1 [(5 - 1), 0.1]$$

$$= 0.4mA$$

Then,

$$V_{DD} = I_D R_D + V_D$$

$$\text{or, } R_D = \frac{V_{DD} - V_D}{I_D} = \frac{5 - 0.1}{0.4 \text{ mA}} = 12.25 \text{ k}\Omega$$

Also, effective resistance between drain and source is,

$$\therefore r_{DS} = \frac{V_{DS}}{I_D} = \frac{0.1V}{0.4 \text{ mA}} = 0.25 \text{ k}\Omega$$

### 3.7 Junction Field Effect Transistor (JFET)

JFET is an unipolar semiconductor device (transistor) because the current flow in the device is due to only one type of charges (either electrons or holes). The place where the charges flow is called channel. JFETs are used in designing special amplifiers with very high input impedance. They are also used in designing very high frequency (giga hertz) amplifiers. The basic structural diagram of n channel JFET is shown below:

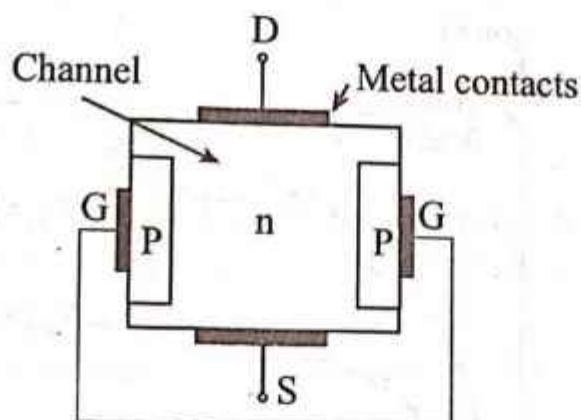


Fig. 3.7 (a) Construction of N- JFET

As it is clear from the diagram that JFET consists of n type of slab. Opposite type of semi-conductor is doped on the both sides of the slab. These doped semiconductor layers function as "Gates" of the device. The two gates are internally connected to each other. Metal contacts are formed at the both ends of the channel and on the top of gates as shown. One end of the channel with metal contact functions as "Source" (S) and other functions as "Drain" (D).

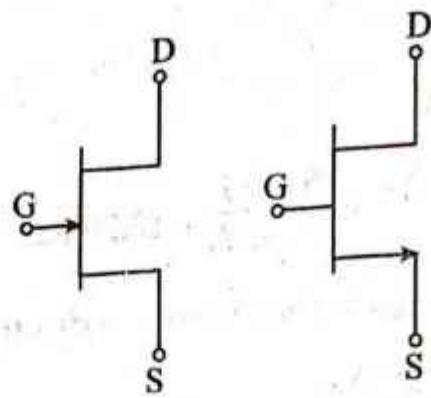


Fig. 3.7(b) Symbols of N-JFET

### Working principle of n-type JFET:

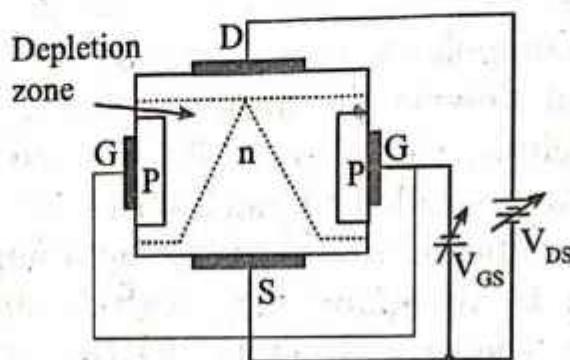


Fig. 3.7(c) Operation of JFET

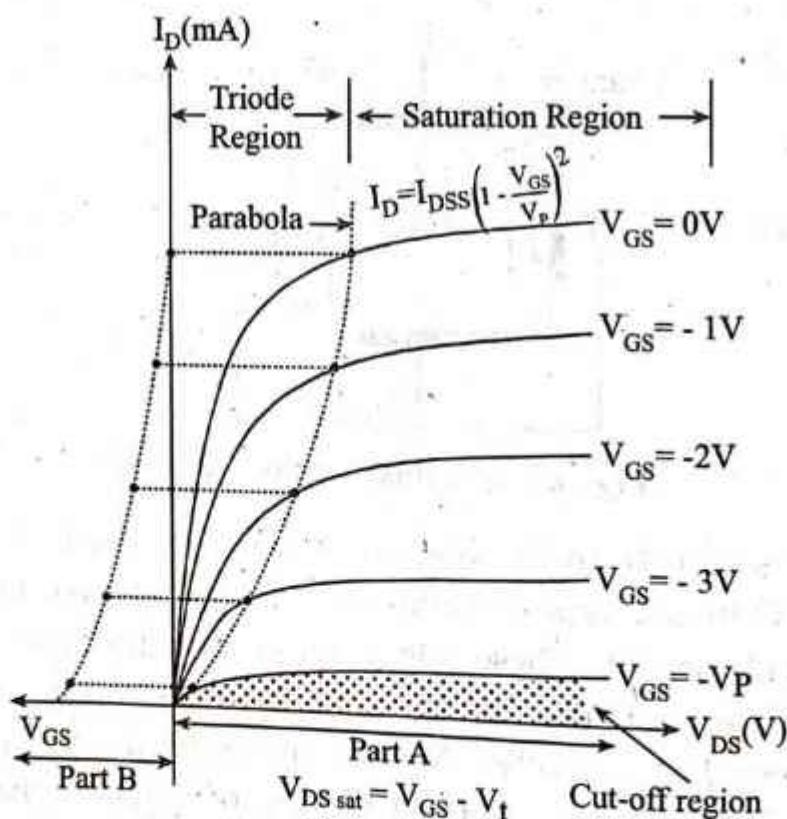


Fig: 3.7(d) Drain characteristics curve (Part A)  
Transfer characteristics curve (Part B)

When  $V_{GS} = 0$  i.e. when voltage between the source and gate is zero there will be small uniform depletion layer between the channel and the gates. Now when  $V_{DS}$  is increased i.e. due to increasing voltage between drain and source the voltage between gate and channel at the drain side  $V_{DG}$  will be equal to  $V_{DS}$ . Due to this reason the depletion layer will have tapered shape as shown in figure. This means the width of channel will be narrower as it moves from source side to the drain side. For higher value of  $V_{DS}$  the channel will be more tapered and the channel gets narrower and narrower. Thus the channel resistance will go on increasing with increasing  $V_{DS}$ . Now if  $V_{DS}$  is kept on increasing a point will come when the channel will be pinched off at the drain side. This happens when  $V_{GD} = -V_p$ . Since this is the case for  $V_{GS} = 0$  the pinch off occurs when  $V_{DS} = V_{GD} = -V_p$ . At this point drain current remains practically constant and any further increase in  $V_{DS}$  will not affect  $I_D$ . This value of drain-source current is called "saturation current".

$$I_{DS} = I_D = I_{DSS} \text{ for } V_{GS} = 0 \text{ and } V_{DS} = -V_p.$$

Where,

$I_{DSS}$  = Drain to source with a shorted gate.

Now, let us increase  $V_{GS}$  from 0 to  $-V$  volt. As  $V_{DS}$  increases depletion region will be more taper shaped and the channel will get more and more narrower at the drain side. When  $V_{DS}$  is kept on increasing pinch off condition of channel at drain side will be reached earlier than in the previous case. At this condition following voltage condition will reach.

$$V_{GD} = -V_p$$

$$\text{or, } V_{DS} - V_{GS} = -V_p$$

$$\text{or, } V_{DS} = -V_p + V_{GS}$$

$$\text{or, } V_{DS} = V_{GS} - V_p, \text{ at pinch off point.}$$

The general expression of JFET can be approximated by

$$I_D = I_{DSS} \left[ 2 \left( 1 - \frac{V_{GS}}{V_p} \right) \left( -\frac{V_{DS}}{V_p} \right) - \left( \frac{V_{DS}}{V_p} \right)^2 \right] \dots\dots\dots (1)$$

### Analysis of JFET in ohmic or triode region:

In this region of operation we have  $V_{DS} < V_{GS} - V_P$

i.e.  $\frac{V_{DS}}{V_P} < 1$  so that  $\left(\frac{V_{DS}}{V_P}\right)^2 \ll 1$

Then equation (1) becomes

$$I_D = I_{DSS} [2(1 - V_{GS}/V_P) (-V_{DS}/V_P) - 0]$$

$$\text{or, } \frac{I_D}{V_{DS}} = \left( \frac{2 I_{DSS}}{-V_P} \right) \left( 1 - \frac{V_{GS}}{V_P} \right)$$

$$\text{or, } \frac{1}{R_{DS}} = \left[ \left( 2 \frac{I_{DSS}}{-V_P} \right) \left( 1 - \frac{V_{GS}}{V_P} \right) \right]$$

$$\text{or, } R_{DS} = \left[ 2 \frac{I_{DSS}}{-V_P} \left( 1 - \frac{V_{GS}}{V_P} \right) \right]^{-1} \dots\dots\dots (2)$$

Where,

$R_{DS}$  = drain to source resistance in ohmic region (triode region).

- **Analysis of JFET in pinch off region:**

For pinch off region  $V_{DS} \geq V_{GS} - V_P$  and therefore substituting  $V_{DS} = V_{GS} - V_P$  in equation(1) we get,

$$I_D = I_{DSS} \left[ 2 \left( 1 - \frac{V_{GS}}{V_P} \right) \left( 1 - \frac{V_{GS}}{V_P} \right) - \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \right]$$

$$\text{or, } I_D = I_{DSS} \left[ 2 \left( 1 - \frac{V_{GS}}{V_P} \right)^2 - \left( 1 - \frac{V_{GS}}{V_P} \right)^2 \right]$$

$$\text{or, } I_D = I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 = I_{Dsat} \dots\dots\dots (3)$$

- The curve represented by this equation (3) is parabola so is also called **square law principle** of JFET.
- The pinch-off region is the region where JFET works as an amplifier so this region is also called "Active Region."

\* AC equivalent model for JFET and MOSFET

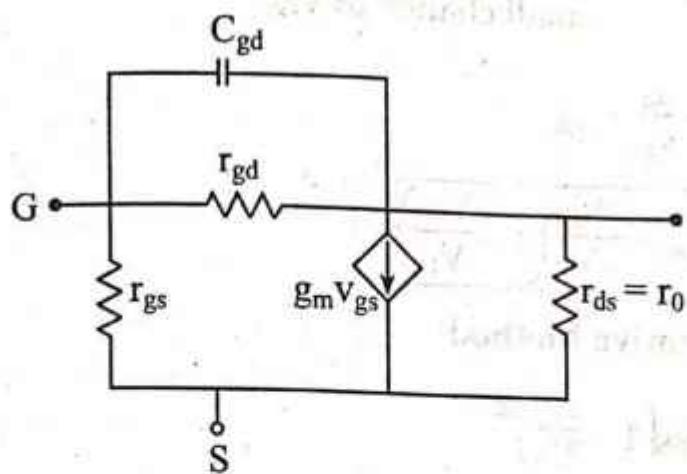


Fig. 3.7 (e) Equivalent  $\pi$ -model for FET

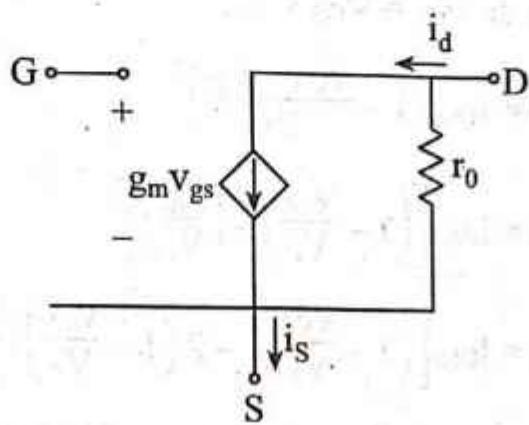


Fig. 3.7 (f) Simple  $\pi$ -model for FET

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \text{ for JFET}$$

$$I_D = K (V_{GS} - V_t)^2 \text{ for MOSFET}$$

When they are operating in active mode or pinch off mode.

To find Transconductance ( $g_m$ ) of JFET:

We have,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2 \dots\dots (i)$$

Differentiating eqn (i) w.r.t.  $V_{GS}$  we get,

$$\frac{dI_D}{dV_{GS}} = 2I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right) \left(-\frac{1}{V_P}\right)$$

$$= \frac{\text{Small change in drain current}}{\text{small change in } V_{GS}}$$

$$= \frac{i_d}{v_{gs}} = g_m$$

$$\therefore g_m = \frac{2I_{DSS}}{-V_P} \left(1 - \frac{V_{GS}}{V_P}\right)$$

**Alternative Method:**

$$i_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

But,

$$i_D = I_D + i_d \quad \& \quad v_{GS} = V_{GS} + v_{gs}$$

$$\therefore I_D + i_d = I_{DSS} \left(1 - \frac{V_{GS} + v_{gs}}{V_P}\right)^2$$

$$\text{or, } I_D + i_d = I_{DSS} \left[ \left(1 - \frac{V_{GS}}{V_P}\right) - \left(\frac{v_{gs}}{V_P}\right) \right]^2$$

$$\text{or, } I_D + i_d = I_{DSS} \left[ \left(1 - \frac{V_{GS}}{V_P}\right)^2 - 2 \left(1 - \frac{V_{GS}}{V_P}\right) \left(\frac{v_{gs}}{V_P}\right) + \left(\frac{v_{gs}}{V_P}\right)^2 \right]$$

[ $\because v_{gs}$  is small  $v_{gs}/V_P < 1$ . Hence  $(v_{gs}/V_P)^2$  can be neglected]

$$\text{or, } I_D + i_d = I_{DSS} \left[ \left(1 - \frac{V_{GS}}{V_P}\right)^2 - 2 \frac{v_{gs}}{V_P} \left(1 - \frac{V_{GS}}{V_P}\right) \right]$$

Comparing a.c. to a.c and d.c to d.c we get,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

And,

$$i_d = I_{DSS} \left[ -2 \frac{v_{gs}}{V_P} \left(1 - \frac{V_{GS}}{V_P}\right) \right]$$

$$\text{or, } \frac{i_d}{v_{gs}} = \frac{2I_{DSS}}{-V_P} \left(1 - \frac{V_{GS}}{V_P}\right)$$

$$\therefore g_m = \frac{2I_{DSS}}{-V_P} \left(1 - \frac{V_{GS}}{V_P}\right)$$

## JFET Biasing or DC Biasing for JFET:

### a) Fix Bias:

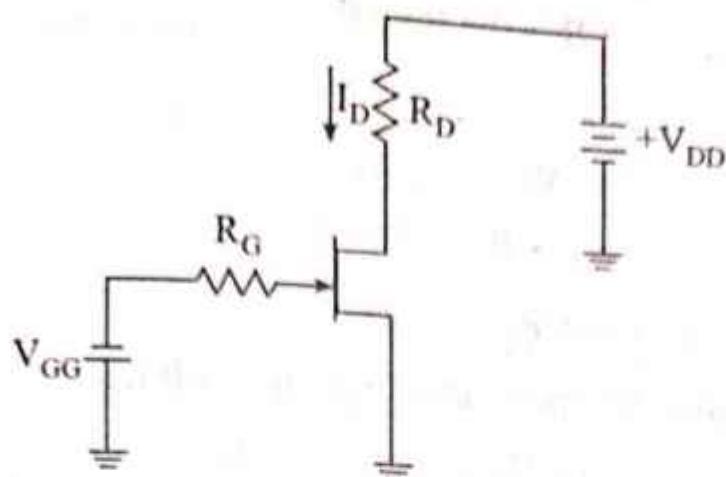


Fig. 3.79(g) Fix Biasing of JFET

- Simplest way of biasing just like BJT
- Also called gate biasing
- Q point is highly unstable

### b) Self Biasing:

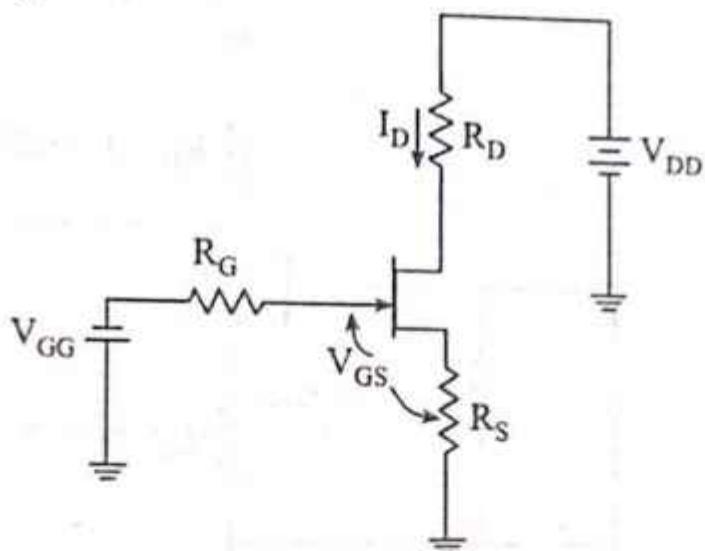


Fig. 3.79(h) Self biasing circuit for JFET

When  $I_D$  increases voltage drop across  $R_S$  also increases because voltage drop across this resistor is the product of  $I_D$  and  $R_S$ . This increased voltage keeps gate more negative with respect to source as a result channel width decreases which consequently decreases the increased drain current  $I_D$ . The expression for  $V_{GS}$  which describes the self biasing is derived below:

The gate current is negligible low. So the gate voltage  $V_G$  with respect to ground is also zero. That is,

$$V_G = I_G \times R_G \approx 0 \times R_G = 0$$

Then,

$$\begin{aligned} V_{GS} &= V_G - V_S \\ &= 0 - I_S \times R_S \approx - I_D \times R_S \\ \therefore V_{GS} &= - I_D \times R_S \dots\dots\dots (1) \end{aligned}$$

According to square law principle of JFET

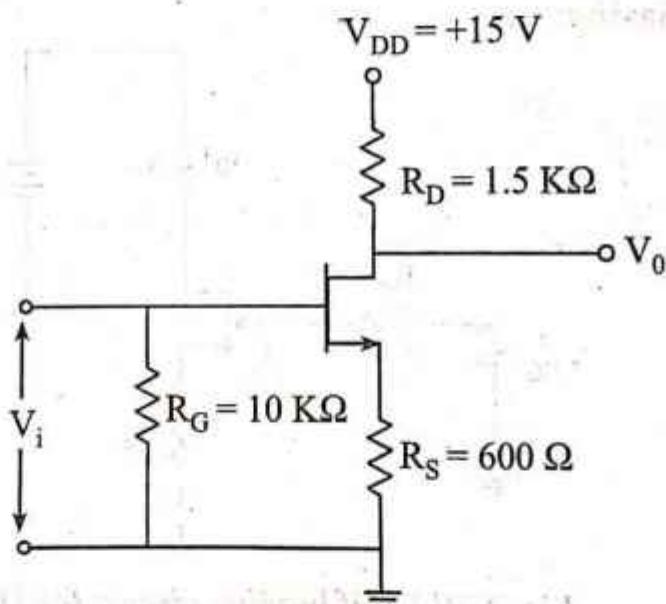
$$I_D = I_{DSS} (1 - V_{GS}/V_P)^2 \dots\dots\dots (2)$$

Solving (1) & (2) we can get,  $I_D$

*Example:*

Find  $I_D$  and  $V_{DS}$  of given circuit.

Given,  $V_P = -4V$  and  $I_{DSS} = 10 \text{ mA}$



*Solution:*

Assuming JFET operates in pinch-off (saturation) region.

$$V_{GS} = -I_D R_S$$

$$\text{or, } V_{GS} = -600 I_D \dots\dots\dots (1)$$

By square law principle (pinch off) of JFET

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\text{or, } I_D = 10 \times 10^{-3} \left(1 + \frac{600I_D}{-4}\right)^2 \quad [\text{From (1)}]$$

$$\text{or, } I_D = \frac{10 \times 10^{-3}}{16} (4 - 600 I_D)^2$$

$$\text{or, } 16I_D = 0.01 (16 - 4800 I_D + 360000 I_D^2)$$

$$\text{or, } 1600I_D = 16 - 4800 I_D + 360000 I_D^2$$

$$\text{or, } 360000 I_D^2 - 6400 I_D + 16 = 0 \quad \dots\dots\dots (2)$$

Solving equation (2) we get

$$I_D = 14.7 \text{mA or } 3 \text{mA}$$

$I_D = 14.7 \text{mA}$  is invalid because it is greater than  $I_{DSS}$ .

$$\therefore \boxed{I_D = 3 \text{mA}}$$

From figure,

$$V_{DD} = I_D R_D + V_{DS} + I_S R_S$$

$$\text{or, } V_{DS} = V_{DD} - I_D R_D - I_S R_S$$

$$\text{or, } V_{DS} = V_{DD} - I_D R_D - I_S R_S \quad [\because I_D \approx I_S]$$

$$\text{or, } V_{DS} = 15 - I_D (R_D + R_S)$$

$$\text{or, } V_{DS} = 15 - 3 \text{mA} (1.5 + 0.6) \text{ K}\Omega$$

$$\therefore \boxed{V_{DS} = 8.7 \text{V}}$$

Now, testing for pinch off region we have,

$$V_{DS} \geq V_{GS} - V_P$$

$$\text{or, } 8.7 \geq -I_D R_S - V_P$$

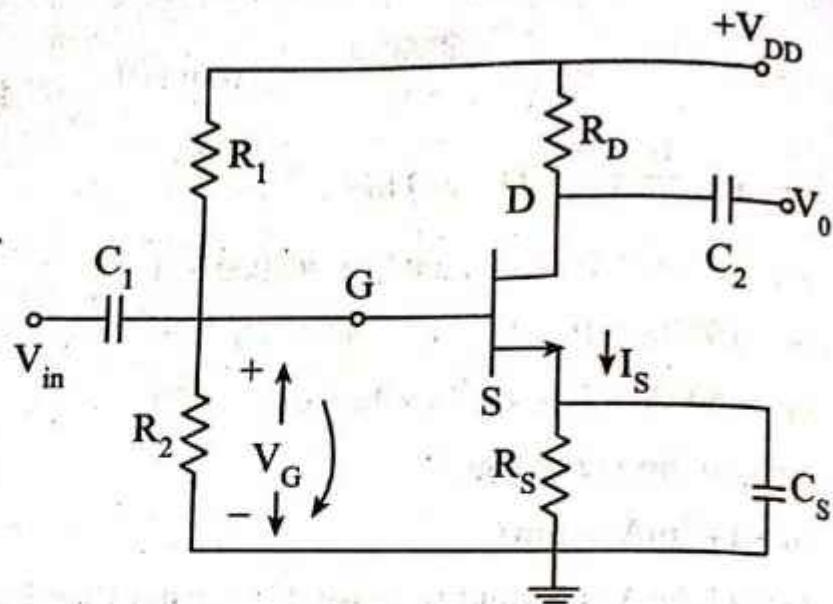
$$\text{or, } 8.7 \geq -3 \times 0.6 - (-4)$$

$$\text{or, } 8.7 \geq -1.8 + 4$$

$$\therefore 8.7 \geq 2.2 \text{ (valid)}$$

Therefore circuit operates in pinch off region as supposed earlier.

**(c) Voltage divider Biasing:**



$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} \dots\dots\dots (1)$$

Applying KVL in input loop

$$V_G - V_{GS} - V_{RS} = 0$$

$$\text{or, } V_{GS} = V_G - V_{RS} \dots\dots\dots (2)$$

And,

$$V_{RS} = I_S R_S = I_D R_S \dots\dots\dots (3)$$

From equation (2) & (3)

$$V_{GS} = V_G - I_D R_S$$

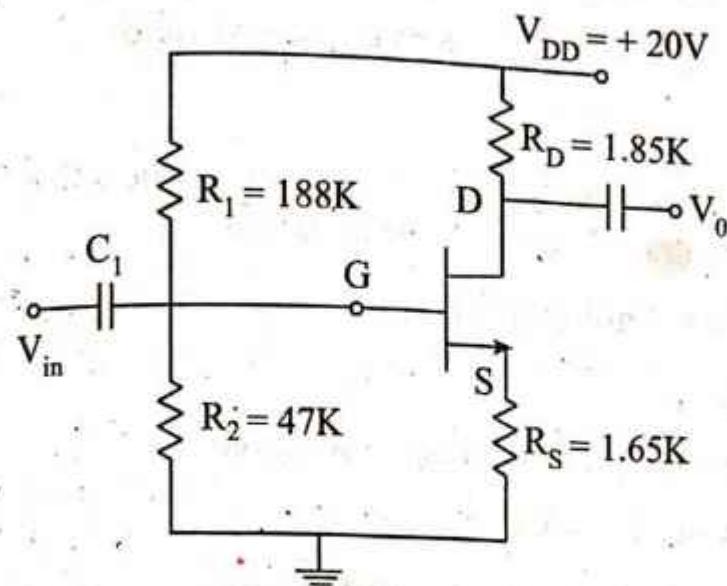
$$= \frac{R_2}{R_1 + R_2} V_{DD} - I_D R_S \dots\dots\dots (4)$$

From square law principle of JFET

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2 \dots\dots\dots (5)$$

By solving equations (4) & (5) we can get  $I_D$ .

Q. Given  $V_P = -5V$ ,  $I_{DSS} = 18mA$ , Find  $I_D$  and  $V_{DS}$ .  
 [069 Chaitra Regular / 072 Kartik Back / 073 Shrawan Back]



*Solution:*

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{47}{47 + 188} \times 20 = 4V$$

We know,

$$V_{GS} = V_G - V_S = 4 - I_D (1.65 \times 10^3) \quad [\therefore V_S = I_D R_S]$$

$$\text{or, } V_{GS} = 4 - 1650 I_D \dots\dots\dots (1)$$

Also, assuming JFET operates at pinch-off mode

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2$$

$$\text{or, } I_D = 18 \times 10^{-3} \left( 1 + \frac{4 - 1650 I_D}{5} \right)^2$$

$$\text{or, } 1960.2 I_D^2 - 22.384 I_D + 0.05832 = 0 \dots\dots\dots (2)$$

Solving above equation we get

$$I_D = 7.4mA \text{ or } 4mA$$

For  $I_D = 4mA$

$$V_{DD} = I_D R_D + V_{DS} + I_S R_S$$

$$\text{or, } V_{DD} = V_{DS} + I_D (R_D + R_S) \quad [\because I_D \approx I_S]$$

$$\text{or, } V_{DS} = 20 - 4\text{mA} (1.85 + 1.65) \text{ K}\Omega$$

$$\text{or, } V_{DS} = 20 - 14$$

$$\therefore V_{DS} = 6\text{V} \quad (\because V_{DS} = +\text{ve value so valid})$$

But,

$I_D = 7.4 \text{ mA}$  is invalid because we get negative  $V_{DS}$  from this value. Since  $V_{DS}$  cannot be negative

$$\text{So, } I_D = 4 \text{ mA} \quad (\text{Valid})$$

Then,

Testing for pinch off region we have,

$$V_{DS} \geq V_{GS} - V_P$$

$$\text{or, } V_{DS} \geq (4 - 1650 \times 4 \times 10^{-3}) - (-5\text{V})$$

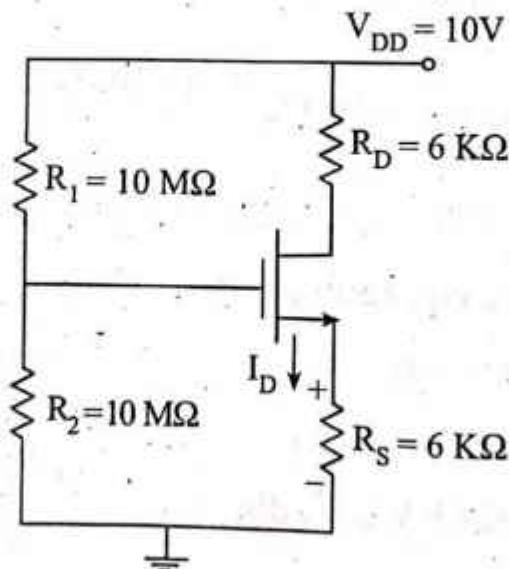
$$\text{or, } V_{DS} \geq (4 - 6.6) + 5$$

$$\text{or, } V_{DS} \geq -2.5 + 5$$

$$\therefore 6 \geq 2.4 \quad (\text{Valid})$$

Hence, circuit operates in pinch off region as assumed earlier

- Q. Analyze the circuit below to determine the voltages at all nodes and the current through all branches. Given  $V_t = 1\text{V}$ ,  $K' n \frac{W}{L} = 1\text{mA/V}^2$  and  $\lambda = 0$ . [068 Chaitra Regular]



*Solution:*

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{10}{10 + 10} \times 10 = 5V$$

Also,

$$V_S = I_D R_S = 6 \times 10^3 I_D$$

And,

$$V_{GS} = V_G - V_S$$

$$\text{Or, } V_{GS} = 5 - 6 \times 10^3 I_D \dots\dots\dots (i) \quad [V_S = I_D R_S]$$

Assuming MOSFET operates in saturation region

Then,

$$I_D = \frac{1}{2} K' n \frac{W}{L} (V_{GS} - V_t)^2$$

$$\text{or, } I_D = \frac{1}{2} \times 1 \times 10^{-3} (5 - 6 \times 10^3 I_D - 1)^2$$

$$\text{or, } 2000 I_D = (4 - 6 \times 10^3 I_D)^2$$

$$\text{or, } 2000 I_D = 16 - 48 \times 10^3 I_D + 36 \times 10^6 I_D^2$$

$$\text{or, } 36 \times 10^6 I_D^2 - 50 \times 10^3 I_D + 16 = 0$$

Solving above equation we get,

$$\therefore I_D = 0.89 \text{ mA or } 0.5 \text{ mA}$$

For  $I_D = 0.89 \text{ mA}$

$$V_S = I_D R_S$$

$$= 0.89 \times 10^{-3} \times 6 \times 10^3$$

$$= 5.34 \text{ V} (> V_G)$$

$\Rightarrow$  Invalid  $\Rightarrow$  NMOSFET OFF ( $V_G > V_S$  to be ON)

So,

For  $I_D = 0.5 \text{ mA}$

$$V_S = I_D R_S$$

$$= 0.5 \times 10^{-3} \times 6 \times 10^3$$

$$= 3 \text{ V} (< V_G) \Rightarrow \text{Valid MOSFET ON because } V_G > V_S.$$

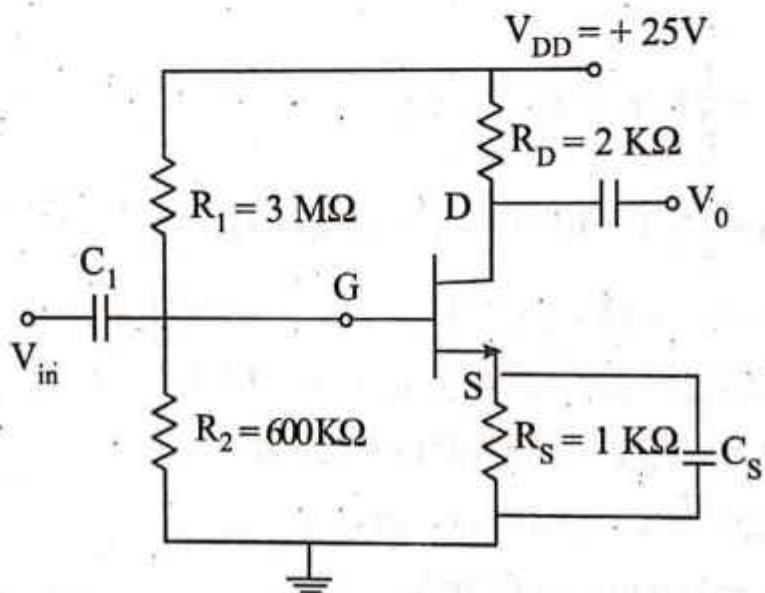
Then,

$$\begin{aligned}V_D &= V_{DD} - I_D R_D \\&= 10V - 0.5 \text{ mA} \times 6 \text{ K}\Omega \\&= 7V\end{aligned}$$

$\therefore V_D > V_G - V_t$  the transistor is operating in saturation as assumed initially.

- Q. Find value of  $I_D$  and  $V_{DS}$  in given circuit. Capacitors are ideal. Given  $V_{DD} = 25V$ ,  $R_D = 2 \text{ K}\Omega$ ,  $R_S = 1 \text{ K}\Omega$ ,  $R_1 = 3 \text{ M}\Omega$ ,  $R_2 = 660 \text{ K}\Omega$ ,  $I_{DSS} = 10 \text{ mA}$  and  $V_{GS(\text{off})} = -4V$ .

[067 Ashad Regular]



Solution:

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} = 4.5 \text{ V}$$

We know,

$$\begin{aligned}V_{GS} &= V_G - V_S = 4.5 - I_D R_S \quad [\because V_S = I_D R_S] \\ \text{or, } V_{GS} &= 4.5 - 1000 I_D \dots\dots (1)\end{aligned}$$

Also, assuming JFET operates at pinch-off mode

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2$$

$$\text{or, } I_D = 10 \times 10^{-3} \left( 1 + \frac{4.5 - 1000 I_D}{4} \right)^2$$

Solving for  $I_D$  we have

$$I_D = 13 \text{ mA and } 5.47 \text{ mA.}$$

$I_D = 13 \text{ mA}$  is invalid because it is greater than  $I_{DSS}$ .

$\therefore I_D = 5.47 \text{ mA}$  is valid.

Now, from figure

$$V_{DD} = I_D R_D + V_{DS} + I_S R_S$$

$$V_{DD} = V_{DS} + I_D (R_D + R_S) [\therefore I_D \approx I_S]$$

$$25 = V_{DS} + 5.47(2 + 1)$$

$$V_{DS} = 8.59 \text{ V}$$

Now, testing for pinch off region.

$$V_{DS} \geq V_{GS} - V_P$$

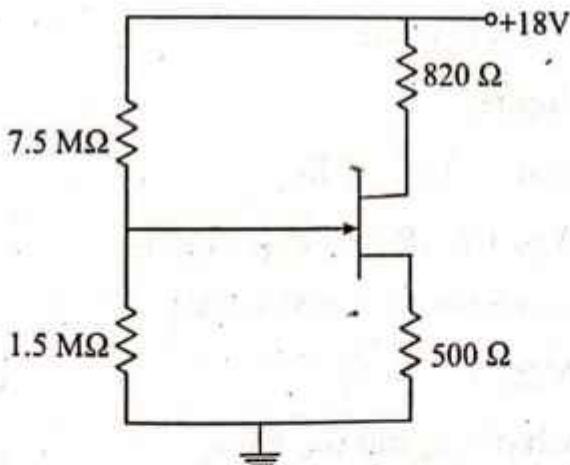
$$\text{or, } 8.59 \geq (4.5 - 1000 \times 5.47 \times 10^{-3}) - (-4V)$$

$$\therefore 8.59 \geq 3.04 \text{ (Valid)}$$

Hence, our assumption is correct as assumed earlier.

Q. Find  $I_D$  and  $V_{DS}$ . Given data:  $I_{DSS} = 18 \text{ mA}$ ,  $V_P = -5 \text{ V}$ .

[066 Bhadra Regular / 2063 Baisakh Regular]



*Solution:*

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{1.5}{7.5 + 1.5} \times 18 = 3 \text{ V}$$

Also,

$$V_{GS} = V_G - V_S = 4.5 - I_D R_S \quad [\because V_S = I_D R_S]$$

$$\text{or, } V_{GS} = 3 - 500I_D \dots\dots (1)$$

Also, assuming JFET operates at pinch-off mode

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2$$

$$\text{or, } I_D = 18 \times 10^{-3} \left( 1 - \frac{3 - 500I_D}{-5} \right)^2$$

$$\text{or, } I_D = 18 \times 10^{-3} \left( 1 + \frac{3 - 500I_D}{5} \right)^2$$

$$\text{or, } I_D = \frac{18 \times 10^{-3}}{25} (8 - 500I_D)^2$$

$$\text{or, } I_D = 7.2 \times 10^{-4} (64 - 8000I_D + 25000I_D^2)$$

$$\text{or, } I_D = 0.04608 - 5.76I_D + 180I_D^2 = 0$$

$$\text{or, } 180I_D^2 - 6.76I_D + 0.04608 = 0$$

Solving for  $I_D$  we have

$$I_D = 0.0286 \text{ A} = 28.6 \text{ mA and}$$

$$I_D = 8.9 \times 10^{-3} \text{ A} = 8.9 \text{ mA.}$$

$I_D = 28.6 \text{ mA}$  is invalid because it is greater than  $I_{DSS}$ .

$\therefore I_D = 8.9 \text{ mA}$  is valid.

Now from figure,

$$V_{DD} = I_D R_D + V_{DS} + I_S R_S$$

$$\text{or, } V_{DD} = V_{DS} + I_D (R_D + R_S) [\because I_D \approx I_S]$$

$$\text{or, } 18 = V_{DS} + 8.9 \times 10^{-3} (820 + 500)$$

$$\therefore V_{DS} = 6.252 \text{ V}$$

Test for pinch off region we have,

$$V_{DS} \geq V_{GS} - V_P$$

$$\text{or, } V_{DS} \geq (3 - 500I_D) - V_P$$

$$\text{or, } 6.252 \geq (3 - 500 \times 8.9 \times 10^{-3}) + 5$$

$$\therefore 6.252 \geq 3.55 \text{ V (Valid).}$$

Hence, our assumption is correct as assumed earlier.

- Q. An n-channel JFET has a pinch-off voltage of -4.5 V and  $I_{DSS} = 9 \text{ mA}$ . At what value of  $V_{GS}$  will  $I_D$  be equal to 3 mA? What is its  $g_m$  at this  $I_D$ ? [071 Shawan Back]

*Solution:*

We know,

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2$$

$$\text{or, } 3 = 9 \left[ 1 - \frac{V_{GS}}{-4.5} \right]^2$$

$$\text{or, } \frac{1}{3} = \left[ 1 + \frac{V_{GS}}{4.5} \right]^2$$

$$\text{or, } 0.33 \times 4.5^2 = (4.5 + V_{GS})^2$$

$$\text{or, } 6.75 = (4.5)^2 + 2 \times 4.5 V_{GS} + V_{GS}^2$$

$$\text{or, } V_{GS}^2 + 9V_{GS} + 13.5 = 0$$

$\therefore V_{GS} = -1.90 \text{ V}$  (Valid since it is less than  $V_P$  in magnitude)

$V_{GS} = -7.098 \text{ V}$  (Invalid since it is greater than  $V_P$  in magnitude)

Now,

$$g_m = \frac{2I_{DSS}}{-V_P} \left( 1 - \frac{V_{GS}}{V_P} \right) = \frac{2 \times 9 \times 10^{-3}}{4.5} \left( 1 - \frac{-1.90}{-4.5} \right)$$

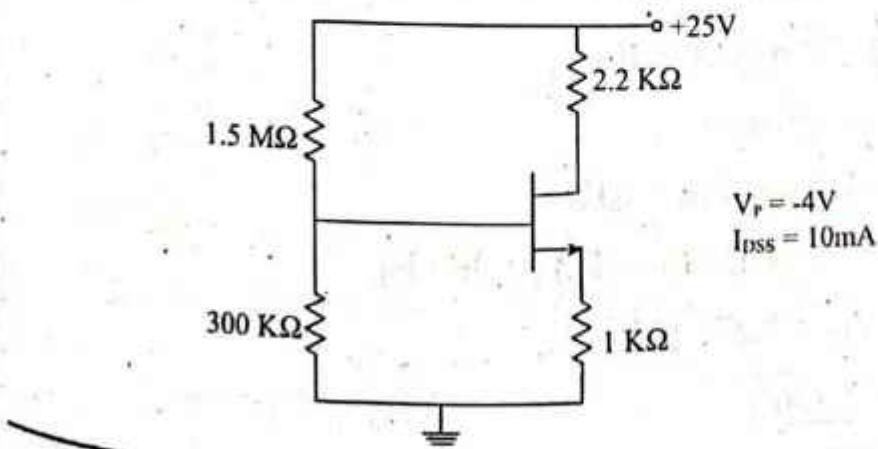
$$g_m = 2.308 \times 10^{-3} \text{ mho.}$$

Hence,

$$\boxed{V_{GS} = -1.90 \text{ V and } g_m = 2.308 \times 10^{-3} \text{ mho.}}$$

- Q. Find  $I_D$  and  $V_{DS}$  for the given circuit.

[068 Baisakh Regular / 070 Chaitra Regular]



**Solution:**

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{300 \times 10^3}{1.5 \times 10^6 + 300 \times 10^3} \times 25 = 4.167 \text{ V}$$

Also,

$$V_{GS} = V_G - V_S = 4.5 - I_D R_S \quad [\because V_S = I_D R_S]$$

$$\text{or, } V_{GS} = 4.167 - I_D \times 10^3 \dots\dots (1)$$

Also, assuming JFET operates at pinch-off mode

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2$$

$$\text{or, } I_D = 10 \times 10^{-3} \left( 1 - \frac{4.167 - I_D \times 10^3}{4} \right)^2$$

$$\text{or, } I_D = 10 \times 10^{-3} \left( 1 + \frac{4.167 - I_D \times 10^3}{4} \right)^2$$

$$\text{or, } I_D = \frac{10 \times 10^{-3}}{16} (4 + 4.167 - I_D \times 10^3)^2$$

$$\text{or, } I_D = 6.25 \times 10^{-4} (8.167 - I_D \times 10^3)^2$$

$$\text{or, } I_D = 6.25 \times 10^{-4} (66.7 - 16334 I_D + I_D^2 \times 10^6)$$

$$\text{or, } I_D = 0.0417 - 10.2 I_D + 625 I_D^2$$

$$\text{or, } 625 I_D^2 - 11.2 I_D + 0.0417 = 0$$

Solving for  $I_D$ , we have

$$I_D = 0.0126 \text{ A} = 12.6 \text{ mA and}$$

$$I_D = 5.277 \times 10^{-3} \text{ A} = 5.277 \text{ mA.}$$

$I_D = 12.6 \text{ mA}$  is invalid because it is greater than  $I_{DSS}$ .

$\therefore I_D = 5.277 \text{ mA}$  is valid.

Now from figure,

$$V_{DD} = I_D R_D + V_{DS} + I_S R_S$$

$$\text{or, } V_{DD} = V_{DS} + I_D (R_D + R_S) \quad [\because I_D \approx I_S]$$

$$\text{or, } 25 = V_{DS} + 5.277 (2.2 + 1)$$

$$\therefore V_{DS} = 8.136 \text{ V}$$

Testing for pinch off Region we have,

$$V_{DS} \geq V_{GS} - V_P$$

$$\text{or, } V_{DS} \geq (4.167 - I_D \times 10^3) - V_P$$

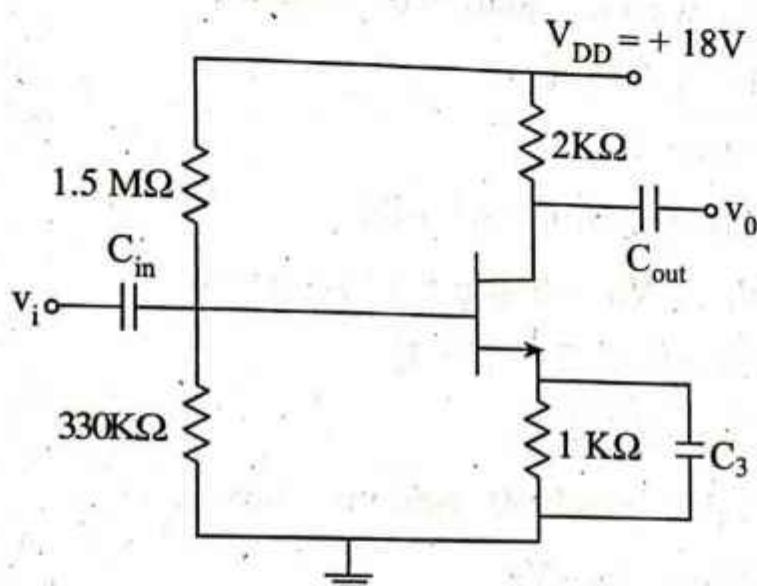
$$\text{or, } 8.136 \geq (4.167 - 5.277 \times 10^{-3} \times 10^3) + 4$$

$$\therefore 8.136 \geq 2.897 \text{ V (Valid).}$$

Hence, our assumption is correct as assumed earlier.

Q. Find  $I_D$  and  $V_{DS}$  for the given circuit. Given data:

$V_P = -5.5 \text{ V}$  and  $I_{DSS} = 12 \text{ mA}$  and assume that all the capacitors are ideal and check whether it is operating in pinch off region or not ?  
[070 Ashad Back]



Solution:

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{330}{1.5 \times 10^3 + 330} \times 18 = 3.25 \text{ V}$$

Also,

$$V_{GS} = V_G - V_S = 4.5 - I_D R_S \quad [\therefore V_S = I_D R_S]$$

$$\text{or, } V_{GS} = 3.25 - I_D$$

$$\text{or, } I_D = 3.25 - V_{GS} \quad \dots \dots \dots \text{(i)}$$

Also, assuming JFET operates at pinch-off mode

$$I_D = I_{DSS} \left[ 1 - \frac{V_{GS}}{V_P} \right]^2$$

$$\text{or, } 3.25 - V_{GS} = 12 \left[ 1 + \frac{V_{GS}}{5.5} \right]^2$$

$$\text{or, } 0.396V_{GS}^2 + 5.363V_{GS} + 8.75 = 0$$

Solving for  $V_{GS}$  we have

$$V_{GS} = -1.8977 \text{ V and}$$

$$V_{GS} = -11.62 \text{ V.}$$

Here,  $V_{GS} = -11.62 \text{ V}$  is impossible since  $V_G$  cannot maintain the magnitude of reverse bias across gate and source terminal. So,

$$V_{GS} = -1.8977 \text{ V} \quad (\text{valid})$$

And now from equation (i) we get,

$$I_D = 5.15 \text{ mA}$$

Now from figure,

$$V_{DD} = I_D R_D + V_{DS} + I_S R_S$$

$$\text{or, } V_{DD} = V_{DS} + I_D (R_D + R_S) \quad [\because I_D \approx I_S]$$

$$\text{or, } 18 = V_{DS} + 5.15 (2 + 1)$$

$$\therefore V_{DS} = 2.55 \text{ V}$$

Testing for pinch off region we have,

$$V_{DS} \geq V_{GS} - V_P$$

$$\text{or, } 2.55 \geq -1.8977 - (-5.5)$$

$$\therefore 2.55 \geq 3.6 \text{ V (False)}$$

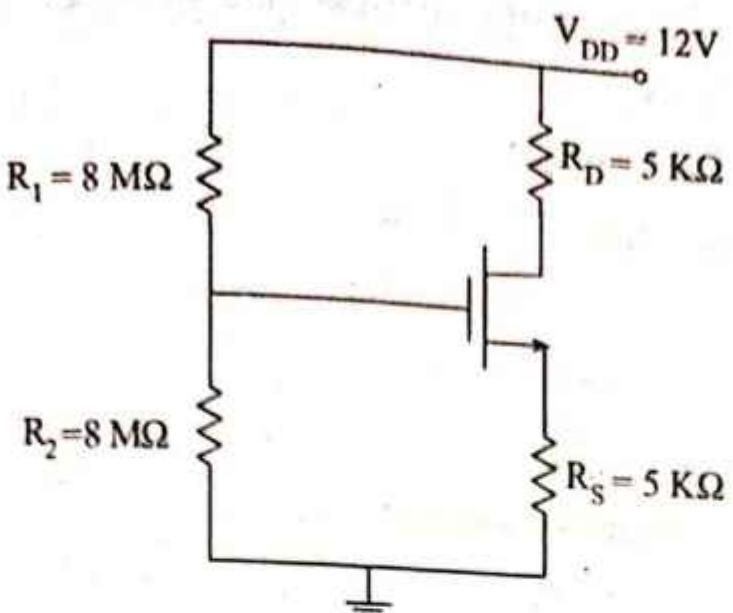
Hence, our assumption is not correct as assumed earlier.

Therefore, JFET is not operating in pinch-off region.

- Q. Find the value of  $I_D$  and  $V_{DS}$  for the following circuits. Given parameters:

$$V_t = 1\text{V}, K = 0.5 \text{ mA/V}^2.$$

[071 Chaitra Regular]



*Solution:*

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{8}{8+8} \times 12 = 6V$$

Also,

$$V_S = I_D R_S = 5I_D$$

We know,

$$V_{GS} = V_G - V_S$$

$$\text{or, } V_{GS} = 6 - 5I_D \quad [V_S = I_D R_S]$$

$$\text{or, } 5I_D = 6 - V_{GS} \dots\dots\dots (i)$$

Assuming MOSFET operates in saturation region we have,

$$I_D = K (V_{GS} - V_t)^2$$

$$\text{or, } I_D = 0.5 (V_{GS} - 1)^2$$

$$\text{or, } 5I_D = 5 \times 0.5 (V_{GS} - 1)^2$$

$$\text{or, } 6 - V_{GS} = 2.5(V_{GS}^2 - 2V_{GS} + 1) \quad [\text{from equation(i)}]$$

$$\text{or, } 6 - V_{GS} = 2.5V_{GS}^2 - 5V_{GS} + 2.5$$

$$\text{or, } 2.5V_{GS}^2 - 4V_{GS} - 3.5 = 0$$

Solving above equation we get,

$$V_{GS} = 2.23 \text{ V (positive and valid) and}$$

$$V_{GS} = -0.63 \text{ V (negative and invalid)}$$

Now, from equation (i) using valid  $V_{GS} = 2.23$  V we have

$$I_D = 0.754 \text{ mA.}$$

Now, from figure,

$$V_{DD} = I_D R_D + V_{DS} + I_S R_S$$

$$\text{or, } V_{DD} = V_{DS} + I_D (R_D + R_S) [\therefore I_D \approx I_S]$$

$$\text{or, } 12 = V_{DS} + 0.754 (5+5)$$

$$V_{DS} = 4.5 \text{ V}$$

Now, testing for saturation region,

$$V_{DS} \geq V_{GS} - V_t$$

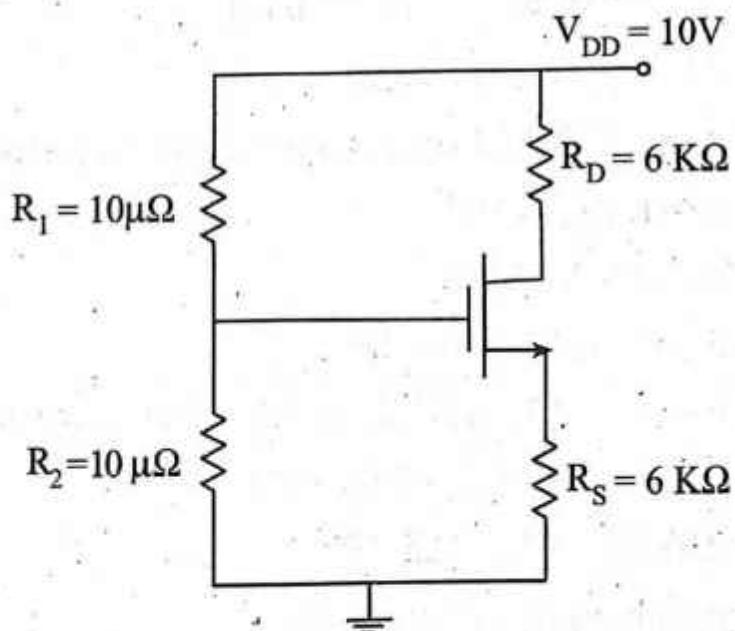
$$\text{or, } 4.5 \geq 2.23 - 1$$

$$\text{or, } 4.5 \geq 1.13 \text{ (true/valid)}$$

Hence, the assumption is true as assumed earlier and we have

$$V_{DS} = 4.5 \text{ V and } I_D = 0.754 \text{ mA.}$$

- Q. For the circuit given below, find  $I_D$  and  $V_{DS}$ . Also determine its region of operation and small signal ac equivalent circuit. Given data:  $V_t = 1\text{V}$ ;  $K = 0.5 \text{ mA/V}^2$ . [072 Chaitra Regular]



*Solution:*

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD} = \frac{10}{10 + 10} \times 10 = 5V$$

We know,

$$V_{GS} = V_G - V_S$$

$$\text{or, } V_{GS} = 5 - I_D R_S$$

$$\text{or, } V_{GS} = 5 - 6 \times 10^3 I_D$$

Assuming MOSFET operates in saturation region then,

$$I_D = K (V_{GS} - V_t)^2$$

$$\text{or, } I_D = 0.5 \times 10^{-3} (5 - 6 \times 10^3 I_D - 1)^2$$

$$\text{or, } 2000 I_D = (4 - 6 \times 10^3 I_D)^2$$

$$\text{or, } 2000 I_D = 16 - 48 \times 10^3 I_D + 36 \times 10^6 I_D^2$$

$$\text{or, } 36 \times 10^6 I_D^2 - 50 \times 10^3 I_D + 16 = 0$$

Solving above equation we get,

$$I_D = 8.9 \times 10^{-4} A = 0.89 \text{ mA and}$$

$$I_D = 5 \times 10^{-4} A = 0.5 \text{ mA.}$$

For  $I_D = 0.89 \text{ mA}$

$$V_S = I_D R_S$$

$$= 0.89 \times 10^{-3} \times 6 \times 10^3$$

= 5.34 V ( $> V_G$ )  $\Rightarrow$  Invalid  $\Rightarrow$  NMOSFET OFF ( $V_G > V_S$  to be ON)

And for  $I_D = 0.5 \text{ mA}$

$$V_S = I_D R_S$$

$$= 0.5 \times 10^{-3} \times 6 \times 10^3$$

= 3V ( $< V_G$ )  $\Rightarrow$  Valid MOSFET ON because  $V_G > V_S$ .

So valid  $I_D$  is 0.5 mA.

Now from figure,

$$V_{DD} = I_D R_D + V_{DS} + I_S R_S$$

$$\text{or, } V_{DD} = V_{DS} + I_D (R_D + R_S) \quad [\therefore I_D \approx I_S]$$

$$\text{or, } 10 = V_{DS} + 0.5 (6 + 6)$$

$$\therefore V_{DS} = 4 \text{ V}$$

Now, testing for saturation region,

$$V_{DS} \geq V_{GS} - V_t$$

$$\text{or, } 4 \geq (5 - 6 \times 0.5) - 1$$

$$\text{or, } 4 \geq 1 \quad (\text{true/ valid})$$

Hence, MOSFET is in saturation region.

Now, small signal ac equivalent circuit for given figure is

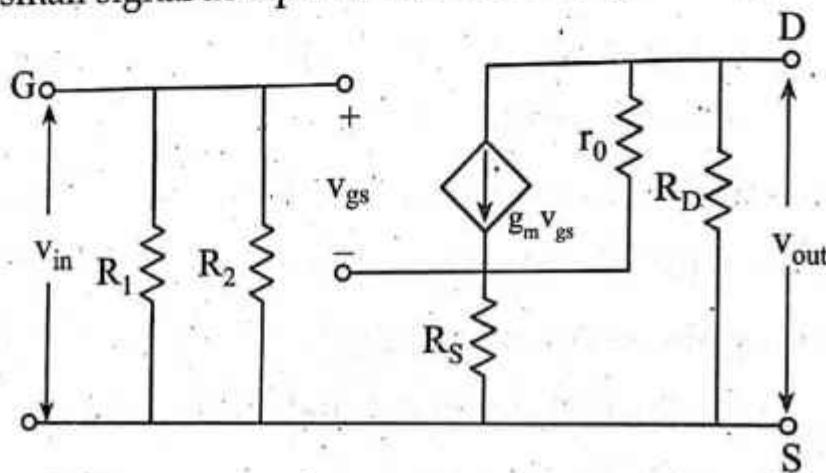
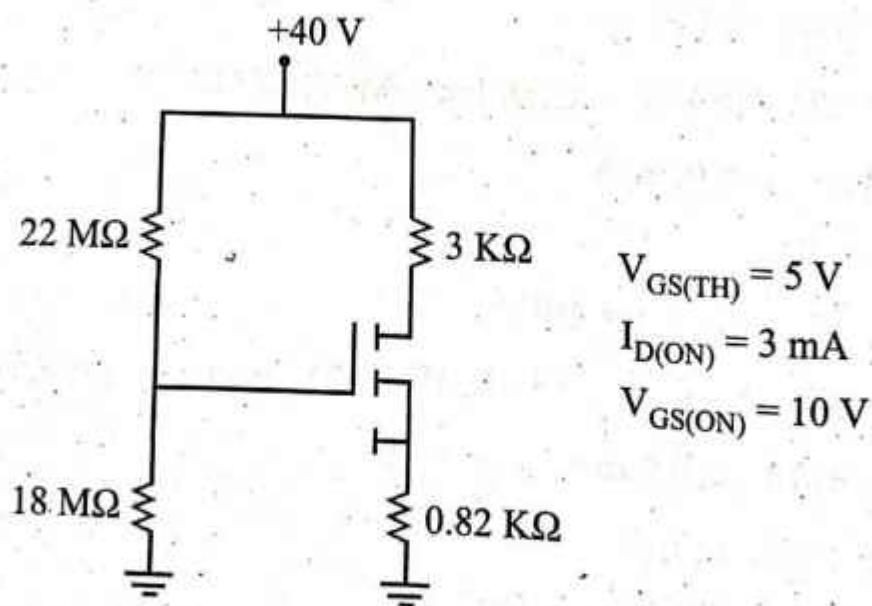


Fig.: Small signal ac equivalent circuit

- Q: Find I<sub>DQ</sub> and V<sub>DSQ</sub> from the following circuit. Show Q point graphically.  
[2075 Ashwin, Back]



*Solution:*

Assuming given circuit is in saturation region.

Given,

$$V_{GS(TH)} = 5 \text{ V} = V_t$$

$$I_{D(ON)} = 3 \text{ mA}$$

$$V_{GS(ON)} = 10 \text{ V}$$

Finding 'K' with the given value

We have,

$$I_{D(ON)} = K (V_{GS(ON)} - V_t)^2$$

$$\text{or, } 3 = K (10-5)^2$$

$$\text{or, } K = \frac{3 \text{ mA}}{(10-5)^2} = 0.12 \text{ mA/V}^2$$

Then,

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{18}{22+18} \times 40 = 18 \text{ V}$$

Also,

$$V_{GS} = V_G - V_S = 18 - I_D R_S = 18 - 0.82 I_D$$

Then,

$$I_D = K(V_{GS} - V_t)^2$$

$$\text{or, } I_D = 0.12 (18 - 0.82 I_D - 5)^2$$

$$\text{or, } I_D = 0.12 (13 - 0.82 I_D)^2$$

$$\text{or, } I_D = 0.12 (169 - 21.32 I_D + 0.6724 I_D)^2$$

$$\text{or, } I_D = 20.28 - 2.5584 I_D + 0.080688 I_D^2$$

$$\text{or, } 0.080688 I_D^2 - 3.5584 I_D + 20.28 = 0$$

Solving above equation we get,

$$I_D = 37.376 \text{ mA or } 6.724 \text{ mA}$$

For  $I_D = 37.376 \text{ mA}$

$$V_S = I_D R_S = 37.376 \times 0.82 = 30.648 \text{ V} > V_G \text{ (Invalid)}$$

For  $I_D = 6.724 \text{ mA}$

$$V_S = I_D R_S = 6.724 \times 0.82 = 5.513 \text{ V} < V_G \text{ (Valid)}$$

Hence,  $I_{DQ} = 6.724 \text{ mA}$

Now,

From figure,

$$V_{DD} = I_D R_D + V_{DS} + I_S R_S$$

$$\text{or, } V_{DS} = V_{DD} - I_D (R_D + R_S) \quad [\because I_D \approx I_S]$$

$$\text{or, } V_{DS} = 40 - 6.724 (3 + 0.82)$$

$$\therefore V_{DS} = 14.314 \text{ V}$$

Hence,  $V_{DSQ} = 14.314 \text{ V}$

Now,

Testing for saturation region,

$$V_{DS} \geq V_{GS} - V_t$$

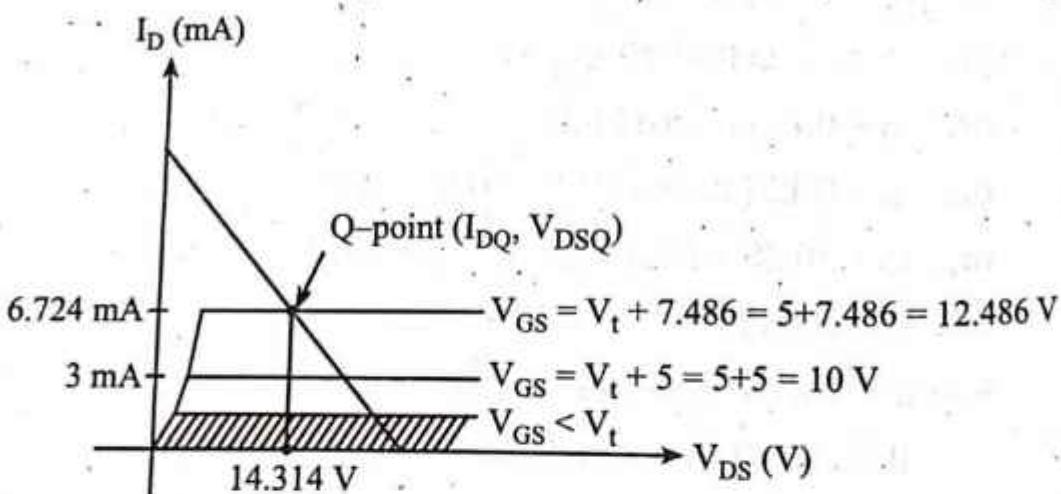
$$\text{or, } 14.314 \geq (18 - 0.82 \times 6.724) - 5$$

$$\text{or, } 14.314 \geq 12.486 - 5$$

$$\text{or, } 14.314 \geq 7.486 \text{ (Valid)}$$

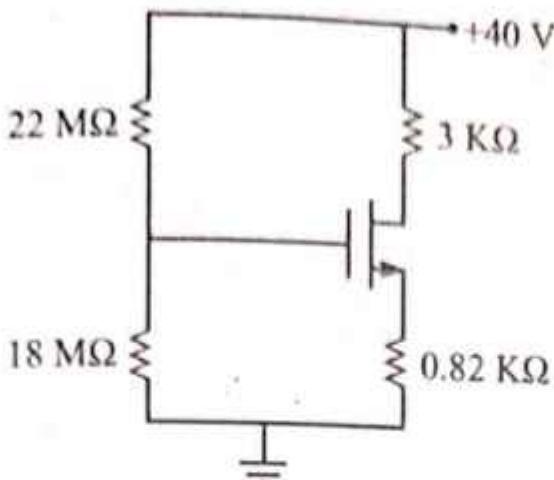
Hence, circuit operates in saturation region as assumed earlier.

Now, Showing Q-point ( $I_{DQ}, V_{DSQ}$ ) graphically,



*Q. Determine  $I_D$  and  $V_{DS}$  for the given circuit and find the region of operation. Given  $K = 0.12 \text{ mA/V}^2$  and  $V_t = 5 \text{ V}$ .*

[2073 Chaitra, Regular]



**Solution:**

$$V_G = \frac{R_2}{R_1+R_2} \times V_{DD} = \frac{18}{22+18} \times 40 = 18 \text{ V}$$

Also,

$$V_{GS} = V_G - V_S = 18 - I_D R_S = 18 - 0.82 I_D$$

Then,

$$I_D = K(V_{GS} - V_t)^2$$

$$\text{or, } I_D = 0.12 (18 - 0.82 I_D - 5)^2$$

$$\text{or, } I_D = 0.12 (13 - 0.82 I_D)^2$$

$$\text{or, } I_D = 0.12 (169 - 21.32 I_D + 0.6724 I_D^2)^2$$

$$\text{or, } I_D = 20.28 - 2.5584 I_D + 0.080688 I_D^2$$

$$\text{or, } 0.080688 I_D^2 - 3.5584 I_D + 20.28 = 0$$

Solving above equation we get,

$$I_D = 37.376 \text{ mA or } 6.724 \text{ mA}$$

For  $I_D = 37.376 \text{ mA}$

$$V_S = I_D R_S = 37.376 \times 0.82 = 30.648 \text{ V} > V_G \text{ (Invalid)}$$

For  $I_D = 6.724 \text{ mA}$

$$V_S = I_D R_S = 6.724 \times 0.82 = 5.513 \text{ V} < V_G \text{ (Valid)}$$

Hence,  $I_{DQ} = 6.724 \text{ mA}$

Now,

From figure,

$$V_{DD} = I_D R_D + V_{DS} + I_S R_S$$

$$\text{or, } V_{DS} = V_{DD} - I_D (R_D + R_S) \quad [\because I_D = I_S]$$

$$\text{or, } V_{DS} = 40 - 6.724 (3 + 0.82)$$

$$\therefore V_{DS} = 14.314 \text{ V}$$

Hence,  $V_{DS} = 14.314 \text{ V}$

Now,

Testing for saturation region,

$$V_{DS} \geq V_{GS} - V_t$$

$$\text{or, } 14.314 \geq (18 - 0.82 \times 6.724) - 5$$

$$\text{or, } 14.314 \geq 12.486 - 5$$

$$\text{or, } 14.314 \geq 7.486 \text{ (Valid)}$$

Hence, circuit operates in saturation region as assumed earlier.

### Tutorial 3

1. Describe the construction and working principle of N-channel enhancement type MOSFET with the help of I-V characteristics curve.
2. Derive expressions to obtain drain current and transconductance when MOSFET is operating in pinch off region.
3. Draw the basic diagram to study the  $I_D - V_{DS}$  characteristics of N channel JFET. And show different region of operations.
4. Derive an expression to find the transconductance for JFET and MOSFET.
5. Describe the principle of operation of EMOSFET with the help of IV characteristics curves and algebraic expressions. Also show its ac equivalent circuit model.
6. Find the voltage gain for FET.

# OUTPUT STAGES AND POWER AMPLIFIERS

## Introduction

An amplifier receives a signal from some pick up transducer or other input source and provides a larger version of the signal to some output device or to another amplifier stage. An input transducer signal is generally small (a few mill volts from a cassette or CD input, or a few micro-volts from an antenna) and needs to be amplified sufficiently to operate an output device (speaker or other power handling device). In small-signal amplifiers the main factors are usually amplification linearity and magnitude of gain. Since signal voltage and current are small in a small-signal amplifier, the amount of power-handling capacity and power efficiency are of little concern. A voltage amplifier provides amplification primarily to increase the voltage of the input signal. Large-signal or power amplifiers, on the other hand, primarily provide sufficient power to an output load to drive a speaker or other power device, typically a few watts to tens of watts. The main features of a large-signal amplifier are the circuit's power efficiency, the maximum amount of power that the circuit is capable of handling, and the impedance matching to the output device.

### 4.1 Classification of Output Stages

An amplifier can be classified

a) According to frequency range

- DC amplifier (0 frequency)
- Audio amplifier (20 Hz to 20 KHz)
- Video amplifier (up to few MHz)

- Radio frequency amplifier (a few KHz to 100's of MHz)
- Ultra high frequency amplifier (100's or 1000 of MHz)

**b) According to use**

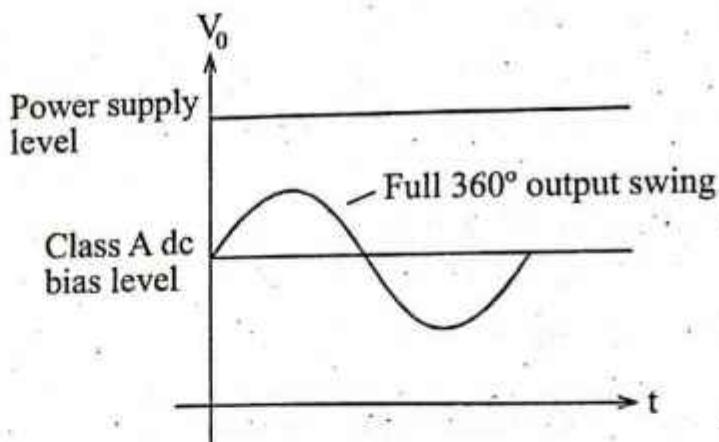
- Current amplifier
- Voltage amplifier
- Power amplifier

**c) According to the type of load**

- Unturned amplifier
- Tuned amplifier

**d) According to the method of operation**

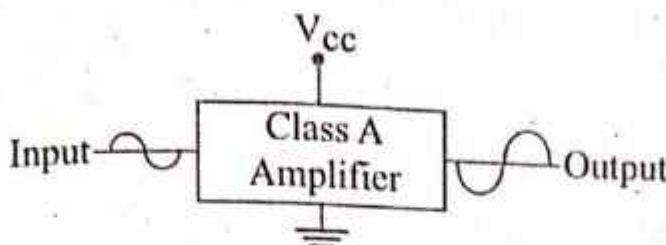
**Class A:** Transistor is so biased that output (or collector) current flows for full  $360^\circ$  of the ac cycle. This operation requires the Q-point to be biased at a level so that at least half the signal swing of the output may vary up and down without going to a high-enough voltage to be limited by the supply voltage, or too low to approach the lower supply level, or 0V as shown in below figure:



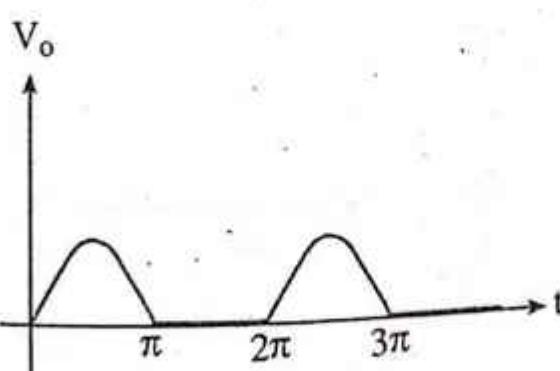
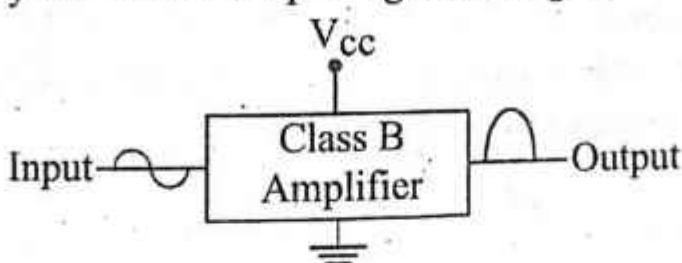
*Fig: Output waveform for Class A amplifier*

→ Class A operation means that transistor operates in active (or linear) region of its load line. So output waveform is exactly similar to the input waveform; (High fidelity)

- It has a maximum efficiency of 25% (without transformer) and 50% (with transformer) and minimum efficiency of 0%.
- $\eta_C > \eta_B > \eta_A$  ( $\eta$  denotes efficiency)

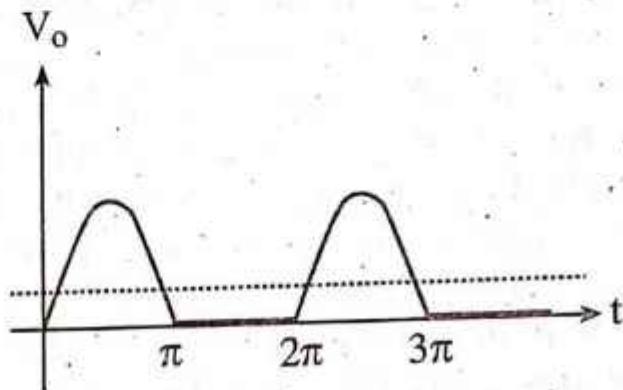


- **Class B:** A class B circuit provides an output signal varying over one-half the input signal cycle, or for  $180^\circ$  of signal as shown in figure. The dc bias point for class B is therefore at 0V, with the output then varying from this bias point for a half cycle. Obviously, the output is not a faithful reproduction of the input if only one half-cycle is present. Two class B operations—one to provide output on the positive-output half cycle and another to provide operation on the negative-output half cycle are necessary. The combined half-cycles then provide an output for a full  $360^\circ$  of operation. This type of connection is referred to as push-pull operation. The class B operation by itself creates a much distorted output signal since reproduction of the input takes place for only  $180^\circ$  of the output signal swing.



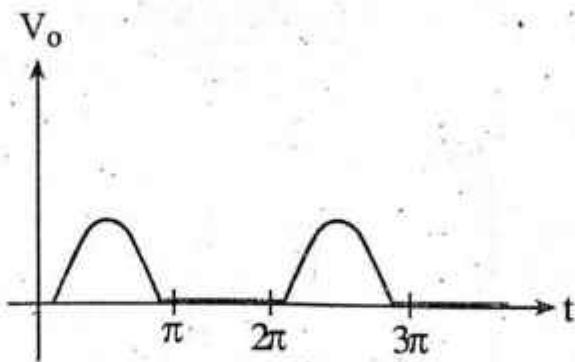
*Fig: Output waveform for Class B amplifier*

- **Class AB:** An amplifier may be biased at a dc level above the zero base-current level of class B and above one-half the supply voltage level of class A, this bias condition is class AB. Class AB operation still requires a push-pull connection to achieve a full output cycle, but the dc bias level is usually closer to the zero-base-current level for better power efficiency. For class AB operation, the output signal swing occurs between  $180^\circ$  and  $360^\circ$  and is neither class A nor class B operation.



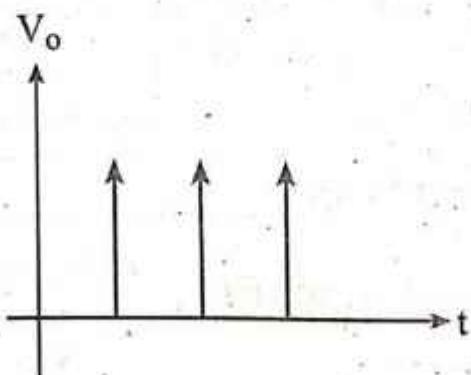
*Fig: Output waveform for Class AB amplifier*

- **Class C:** The output of a class C amplifier is biased for operation at less than  $180^\circ$  of the cycle and will operate only with a tuned (resonant) circuit, which provides a full cycle of operation for the tuned or resonant frequency. This operating class is therefore used in special areas of tuned circuits, such as radio or communications.



*Fig: Output waveform for Class C amplifier*

- **Class D:** This operating class is a form of amplifier operation using pulse (digital) signals, which are ON for a short interval and OFF for a longer interval. Using digital techniques make it possible to obtain a signal that varies over the full cycle (using sample and hold circuitry) to recreate the output from many pieces of input signal. The major advantage of class D operation is that the amplifier is "ON" (using power) only for short intervals and the overall efficiency can practically be very high.



*Fig: Output waveform for Class D amplifier*

### Amplifier efficiency

The power amplifier efficiency of an amplifier defined as the ratio of output power to input power, improves (gets higher) going from class A to class D. In general terms we see that a class A amplifier, with dc bias at one-half the supply voltage level, uses a good amount of power to maintain bias, even with no input signal applied. This results in very poor efficiency, especially with small input signals, when very little ac power is delivered to the load. In fact, the maximum efficiency of a class A circuit, occurring for the largest output voltage and current swing, is only 25% with a direct or series fed load connection and 50% with a transformer connection to the load. Class B operation, with no dc bias power for no input signal, can be shown to provide a maximum efficiency that reaches 78.5%. Class D operation can achieve power efficiency over 90% and provides the most efficient operation

of all the operating classes. Since class AB falls between class A and class B in bias, it also falls between their efficiency ratings between 25% (or 50%) and 78.5%.

### Comparisons of Amplifier Classes

Class	A	AB	B	C	D
Operating cycle	360°	180° to 360°	180°	less than 180°	pulse operation
Maximum power efficiency	25% to 50%	25% (50%) and 78.5%	78.5%	Greater than B	over 90%

### 4.2 Class A Output Stage

#### Series- Fed class A Amplifier

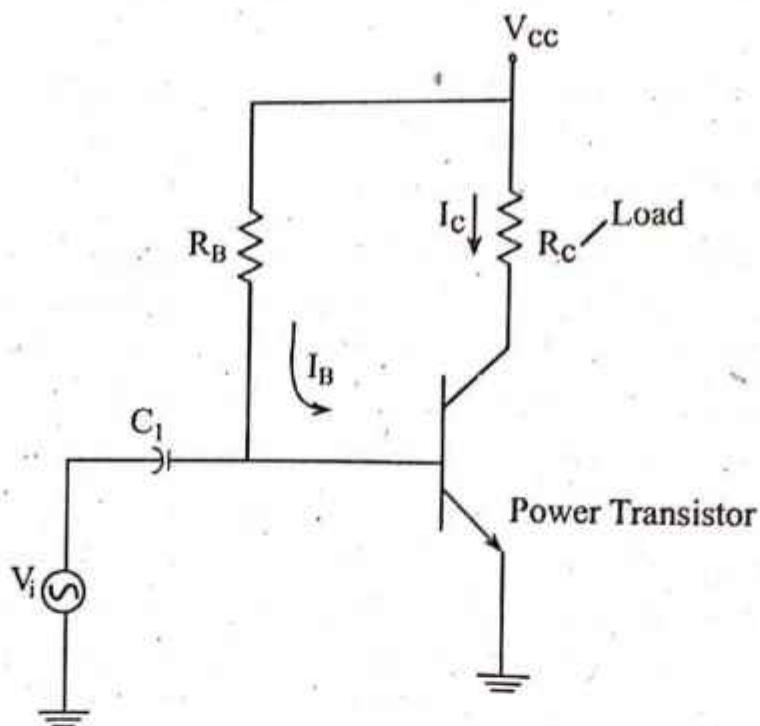


Fig.4.2(a) Series - Fed Class A Amplifier

- It is called series fed as load  $R_C$  is connected in series with transistor output.
- The difference between series fed (large signal) and small signal version is that signals handled by large signal

circuit are in the range of volts and transistor used is a power transistor that is capable of operating in the range of few to tens of watts.

- Series fed circuit is not the best to use as large signal amplifier because of its poor power efficiency.
- $\beta$  is less than 100 (high current or power gain but low voltage gain).
- DC Bias Operation

The dc bias set by  $V_{CC}$  and  $R_B$  fixes the dc base-bias current at

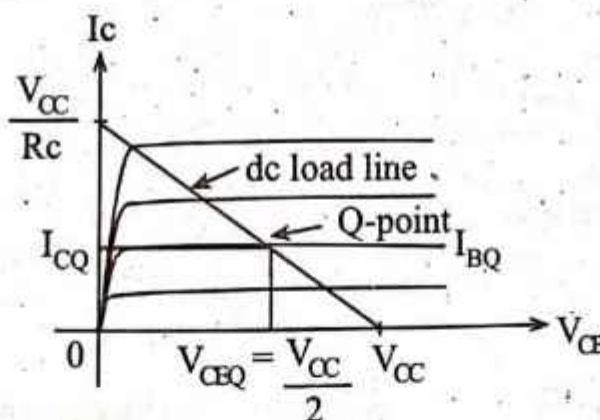
$$I_B = \frac{V_{CC} - 0.7V}{R_B}$$

With the collector current then being

$$I_C = \beta I_B$$

With the collector-emitter voltage then

$$V_{CE} = V_{CC} - I_C R_C$$



*Fig: 4.2(b) Transistor characteristics showing load line and Q point*

- First DC load line is drawn using value of  $V_{CC}$  and  $R_C$  since they are constant. ( $V_{CC}$  &  $R_C$  are constant).
- The quiescent point is calculated using above equations.
- If the dc bias collector current is set at one-half the possible signal swing (between 0 and  $V_{CC}/R_C$ ) the largest

collector current swing will be possible. Additionally, if the quiescent collector is set at one half the supply voltages (0 and  $V_{CC}$ ) the largest voltage swing will be possible.

- With the Q point set at this optimum bias point, the power considerations for the given circuit (series fed circuit) are determined.
- AC operation:**

When an input ac signal is applied to the amplifier for the given circuit, the output will vary from its dc bias operating voltage and current. For the current this limiting condition is either zero current at the low end or  $V_{CC}/R_C$  at the high end of its swing. For the collector-emitter voltage the limit is either 0V or the supply voltage  $V_{CC}$ .

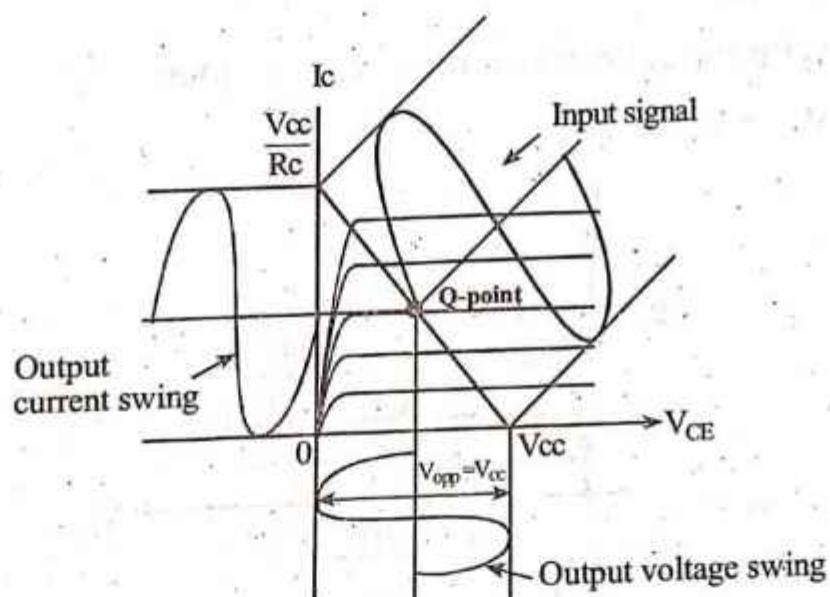


Fig: 4.2(c) Amplifier input and output signal variation (Ideal case) for Class A amplifier.

#### Maximum efficiency for Ideal case:

$$\text{Output power (minimum)}, P_o(\text{ac}) = I_o V_o = \frac{V_o^2}{R_C}$$

But,

$$V_o = \frac{V_{opp}}{2\sqrt{2}} = \frac{V_{CC}}{2\sqrt{2}} \quad [V_{rms} = V_o = \frac{V_{opp}}{2\sqrt{2}}]$$

[ $V_{opp}$  means peak to peak output voltage =  $V_{CC}$  for ideal case]

$$\therefore P_o(ac) = \frac{(V_{CC}/2\sqrt{2})^2}{R_C} = \frac{V_{CC}^2}{8R_C} \dots\dots\dots (i)$$

Input power from collector supply  $V_{CC}$ ,

$$P_i(dc) = V_{CC} I_{dc}(\text{avg})$$

$$= V_{CC} \cdot I_{CQ}$$

$$= V_{CC} \cdot \frac{V_{CEQ}}{R_C}$$

$$= V_{CC} \cdot \frac{V_{CC}}{2R_C} \quad [\therefore V_{CEQ} = \frac{V_{CC}}{2}]$$

$$\text{or, } P_i(dc) = \frac{V_{CC}^2}{2R_C} \dots\dots\dots (ii)$$

$$\therefore \text{Maximum efficiency } (\eta) = \frac{P_o(ac)}{P_i(dc)} \times 100\%$$

$$= \frac{V_{CC}^2}{8R_C} \frac{2R_C}{V_{CC}^2} \times 100\%$$

$$= 25\%$$

Therefore,  $\eta_{max} = 25\%$  for Series Fed Class A amplifier.

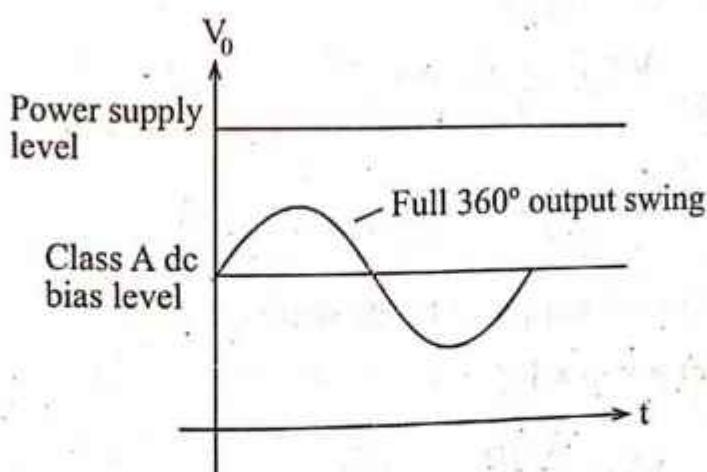
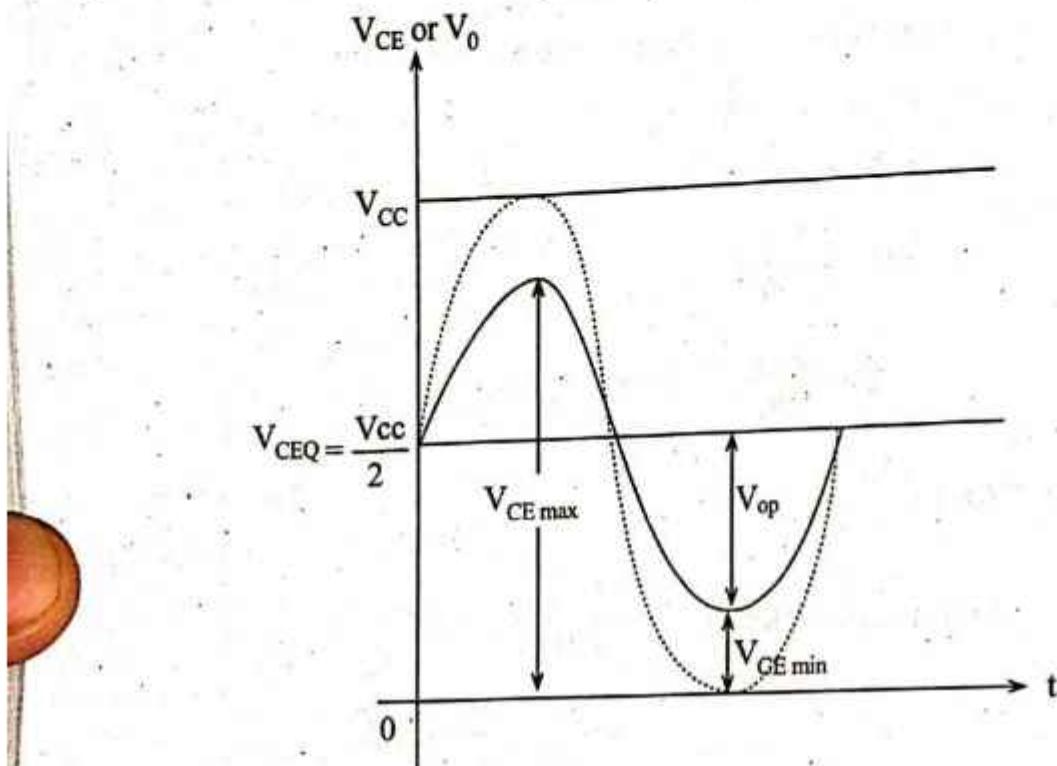


Fig: Output waveform for Class A amplifier

**General efficiency of class A amplifier: (Series fed class A amplifier):**

- DC biasing is set at  $V_{CEQ} = \frac{V_{CC}}{2}$  and  $I_{CQ}$  is chosen such that it doesn't exceed the maximum collector dissipation for the transistor  $Q_1$ .



*Fig.4.2(d) Graphical analysis of Class A amplifier with resistive load*

Here, from figure

$$V_{CEQ} = \frac{V_{CE\ max} + V_{CE\ min}}{2} = \frac{V_{CC}}{2} \dots\dots (i)$$

$$V_{op} = \frac{V_{CE\ max} - V_{CE\ min}}{2} \dots\dots (ii)$$

The power supplied by dc source

$$P_i(\text{dc}) = V_{CC} \times I_{CQ}$$

$$= V_{CC} \cdot \frac{V_{CEQ}}{R_C}$$

$$= V_{CC} \cdot \frac{V_{CC}}{2R_C}$$

$$= \frac{(V_{CE\max} + V_{CE\min})^2}{2R_C} \quad \dots \dots \dots \text{(iii)}$$

Similarly, output power obtained from amplifier as,

$$P_o(\text{ac}) = \frac{V_0^2}{R_C}$$

$$V_0 = \frac{V_{OP}}{\sqrt{2}}$$

$$\therefore P_o(\text{ac}) = \left( \frac{V_{CE\max} - V_{CE\min}}{2\sqrt{2}} \right)^2 \cdot \frac{1}{R_C}$$

$$\text{or, } P_o(\text{ac}) = \frac{(V_{CE\max} - V_{CE\min})^2}{8R_C} \quad \dots \dots \dots \text{(iv)}$$

Thus, efficiency of amplifier

$$\eta_{\text{gen}} = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\%$$

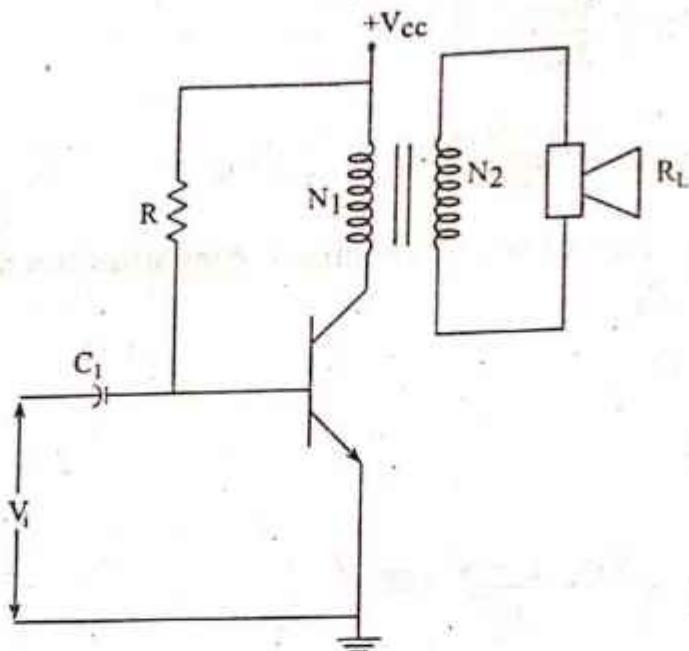
$$= \frac{(V_{CE\max} - V_{CE\min})^2}{(V_{CE\max} + V_{CE\min})^2} \times \frac{100\%}{4}$$

$$\therefore \boxed{\eta_{\text{gen}} = \left( \frac{V_{CE\max} - V_{CE\min}}{V_{CE\max} + V_{CE\min}} \right)^2 \times 25\%}$$

[Note: From above equation we can see that most series-fed circuits will provide efficiencies of much less than 25%.]

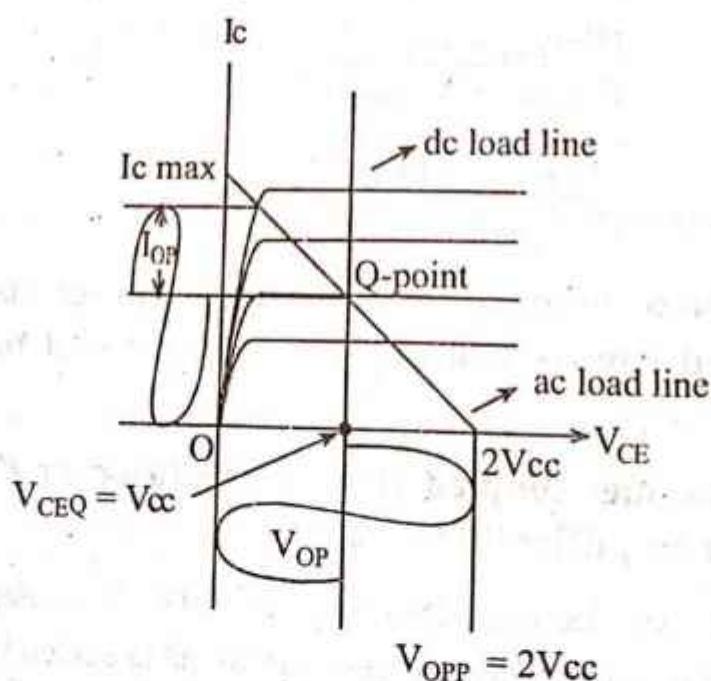
**Transformer coupled class A amplifier: or // single ended power amplifier (Ideal case):**

- It has better efficiency of 50% because no power is wasted in collector resistor  $R_C$  as is series fed.
- A matching transformer (step-down) is provided to couple the high impedance collector circuit to low impedance load.



*Fig. 4.2(e) Transformer Coupled Class A amplifier*

The transformer (dc) winding resistance determines the dc load line for the above circuit. Typically, this dc resistor is small (ideally  $0\Omega$ ). Thus, a  $0\Omega$  dc load line is a straight vertical line.



*Fig. 4.2(f)*

Here,

Input power,

$$P_i(\text{dc}) = V_{cc} \cdot I_{CQ}$$

$$= V_{CC} \cdot \frac{V_{CC}}{Z} = \frac{V_{CC}^2}{Z} \quad [\text{From figure 4.2(f)}]$$

$$P_o(\text{ac}) = \frac{V_o^2}{Z}$$

$$\text{But, } V_o = \frac{V_{opp}}{2\sqrt{2}}$$

$$= \frac{2 V_{CC}}{2\sqrt{2}}$$

[From figure 4.2(f)]

$$= \frac{V_{CC}}{\sqrt{2}}$$

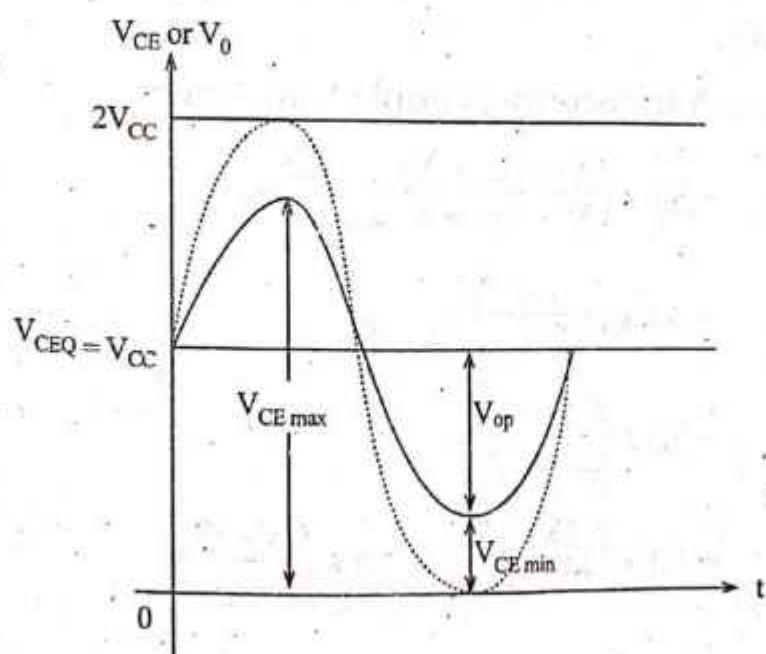
$$\therefore P_o(\text{ac}) = \frac{V_{CC}^2}{2Z}$$

$$\begin{aligned}\therefore \text{Efficiency } (\eta) &= \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% \\ &= \frac{V_{CC}^2}{2Z} \times \frac{Z}{V_{CC}^2} \times 100\% \\ &= 50 \left( \frac{V_{CC}}{V_{CC}} \right)^2\end{aligned}$$

$$\boxed{\eta_{\max} = 50\%}$$

Hence the efficiency of transformer coupled amplifier is 50% for ideal case i.e. when  $V_{opp} = 2V_{CC}$

### General efficiency of Transformer Coupled Class A amplifier:



We know, for transformer coupled class A amplifier

$$V_{CEQ} = V_{CC} = \frac{V_{CE}(\text{max}) + V_{CE}(\text{min})}{2}$$

Then,

$$P_i(\text{dc}) = V_{CC} \cdot \frac{V_{CEQ}}{Z}$$

$$= V_{CC} \cdot \frac{V_{CC}}{Z} = \frac{V_{CC}^2}{Z}$$

$$\text{or, } P_i(\text{dc}) = \frac{[V_{CE}(\text{max}) + V_{CE}(\text{min})]^2}{4Z}$$

Also,

$$P_o(\text{ac}) = \left( \frac{V_{CE}(\text{max}) - V_{CE}(\text{min})}{2\sqrt{2}} \right)^2 \cdot \frac{1}{Z}$$
$$= \frac{(V_{CE\ max} - V_{CE\ min})^2}{8Z}$$

General Efficiency

$$\therefore \eta_{\text{gen}} = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\%$$

$$\therefore \boxed{\eta_{\text{gen}} = 50 \left[ \frac{V_{CE\ max} - V_{CE\ min}}{V_{CE\ max} + V_{CE\ min}} \right]^2 \%}$$

- Q. Calculate the efficiency of a transformer coupled class A amplifier for a supply of 12VDC and output of (i)  $V_P = 12V$  and (ii)  $V_P = 6V$ . [065 Chaitra Regular]

Solution

We have,

For class A transformer coupled amplifier:

$$\begin{aligned}\eta_{\text{gen}} &= 50 \times \left( \frac{V_{CE\ max} - V_{CE\ min}}{V_{CE\ max} + V_{CE\ min}} \right)^2 \% \\ &= 50 \times \left( \frac{V_{PP}}{2V_{CEQ}} \right)^2 \% \\ &= 50 \times \left( \frac{V_{PP}}{2V_{CC}} \right)^2 \% \\ &= 50 \times \left( \frac{2V_P}{2V_{CC}} \right)^2 \% = 50 \times \left( \frac{V_P}{V_{CC}} \right)^2 \%\end{aligned}$$

(i) When  $V_P = 12\text{ V}$

$$\eta = 50 \times \left(\frac{12}{12}\right)^2 = 50\%$$

(ii) When  $V_P = 6\text{ V}$

$$\boxed{\eta = 50 \times \left(\frac{6}{12}\right)^2 = 50 \times \frac{1}{4} = 12.5\%}$$

#### 4.3 Class B Output Stage

Class B operation is provided when the dc bias leaves the transistor biased just OFF, the transistor turning ON when the ac signal is applied. This is essentially no bias and the transistor conducts current for only one half of the signal cycle i.e.  $I_C$  flows for only  $180^\circ$  of ac cycle. Operating point is set at cut-off. To obtain output for the full cycle of signal, it is necessary to use two transistors and have each conduct on opposite half-cycles, the combined operation providing a full cycle of output signal. Since one part of the circuit pushed the signal high during one half-cycle and the other part pulls the signal low during the other half cycle, the circuit is referred to as a **push-pull circuit**, with each half operating on alternate half-cycles, the load then receiving a signal for the full ac cycle. The power transistor used in the push-pull circuit are capable of delivering the desired power to load, and the class B operation of these transistors provides greater efficiency, than was possible using a single transistor.

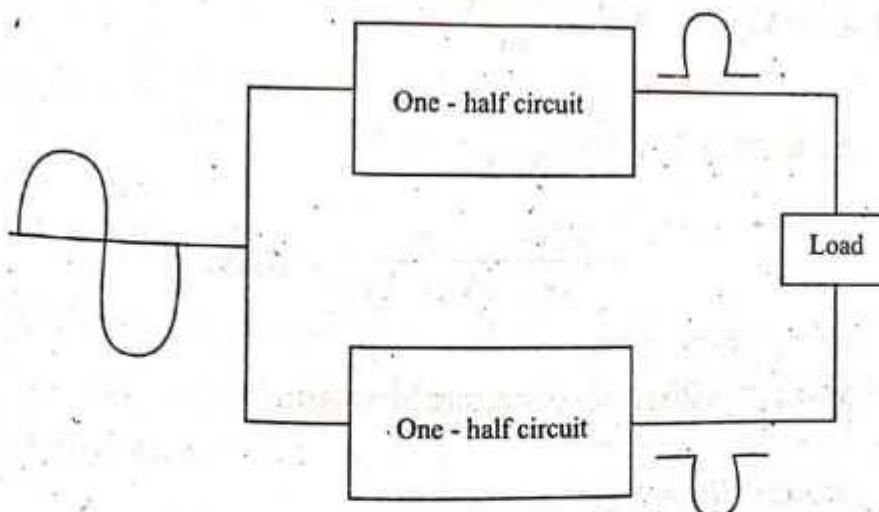


Fig. 4.3(a) Block diagram of Class B

- Class B amplifier has maximum efficiency of 78.5% and minimum of 50%

### Advantage:

The main advantage of class B/AB amplifier over the class A amplifier is that there is very little current in the transistor when there is no input signal. This results in low power dissipation when there is no signal.

### Efficiency of Class B amplifier

Let  $V_{OP}$  be the peak output voltage produced by class B amplifier. Let  $R_L$  (or  $r_p$ ) be the equivalent load resistance in the output circuit.

Then,

$$P_o(\text{ac}) = \frac{V_{OP}^2}{r_p} = \frac{(V_{OP}/\sqrt{2})^2}{r_p} = \frac{V_{OP}^2}{2r_p} \quad \dots\dots \text{(i)}$$

Let  $V_{CC}$  be the dc source voltage and the equivalent dc current supplied by the dc source is the average dc value of the ac output current which may be expressed as,

$$I_{dc} = \frac{2}{\pi} I_{OP} = \frac{2}{\pi} \frac{V_{OP}}{r_p} = \frac{2}{\pi} \frac{V_{OP}}{r_p}$$

Thus, dc power supplied by source is,

$$P_i(\text{dc}) = V_{CC} \cdot I_{dc} = V_{CC} \cdot \frac{2V_{OP}}{\pi r_p} \quad \dots\dots \text{(ii)}$$

$$\begin{aligned} \therefore \text{Efficiency } (\eta) &= \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% \\ &= \frac{V_{OP}^2}{2r_p} \frac{\pi r_p}{2V_{OP} \cdot V_{CC}} \times 100\% \end{aligned}$$

$$\therefore \boxed{\eta = \frac{V_{OP}}{V_{CC}} \cdot 25\pi\%} \rightarrow \text{general formula}$$

When  $V_{OP} \approx V_{CC}$

$$\eta_{\text{max}} = 25\pi\% = 78.5\%$$

## Condition for minimum efficiency

Power loss by class-B amplifier,

$$P_{\text{Loss}} = P_i(\text{dc}) - P_o(\text{ac})$$

$$\text{or, } P_{\text{Loss}} = \frac{2V_{CC} \cdot V_{OP}}{\pi r_p} - \frac{V_{OP}^2}{2 r_p} \quad (\text{iii})$$

Differentiating (iii) with respect to output voltage  $V_{OP}$ ,

$$\frac{dP_{\text{Loss}}}{dV_{OP}} = \frac{2V_{CC}}{\pi r_p} - \frac{V_{OP}}{r_p}$$

For maximum loss,

$$\frac{dP_{\text{Loss}}}{dV_{OP}} = 0 = \frac{2V_{CC}}{\pi r_p} - \frac{V_{OP}}{r_p}$$

$$\text{or, } \frac{V_{OP}}{r_p} = \frac{2V_{CC}}{\pi r_p}$$

$$\text{or, } V_{OP} = \frac{2}{\pi} V_{CC} \quad (\text{iv})$$

$$\text{or } V_{OP} = 0.6366V_{CC}$$

Thus, when output voltage is 63.66% of maximum possible output voltage the efficiency of class B amplifier becomes minimum which may be expressed as,

$$\eta_{\text{min}} = \frac{V_{OP}}{V_{CC}} 25\pi\% \quad [\text{From general formula}]$$

$$\text{or, } \eta_{\text{min}} = \frac{0.6366V_{CC}}{V_{CC}} 25\pi\% \quad [\text{From (iv)}]$$

$$\boxed{\eta_{\text{min}} = 50\%}$$

## Class B amplifier circuits

A number of circuit arrangements for obtaining class B operation are possible.

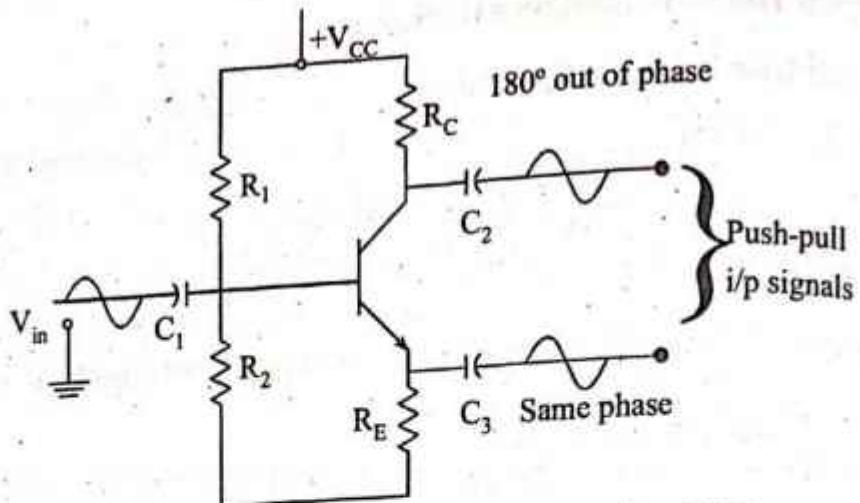
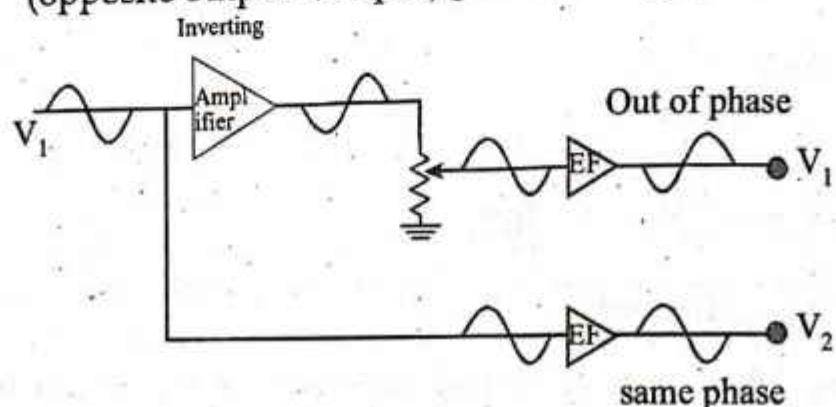


Fig.4.3(b) Phase splitter using BJT

- Same output of input through emitter &  $180^\circ$  out of (opposite output of input) phase through collector.



#### 4.4. Transformer- Coupled Push-Pull Stages

**Transformer coupled class B push pull amplifier:**

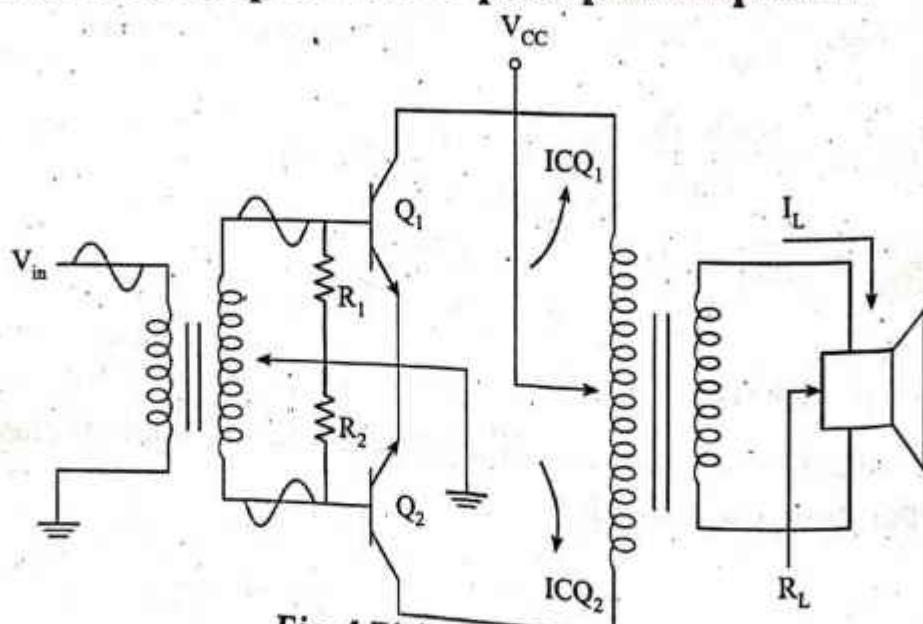
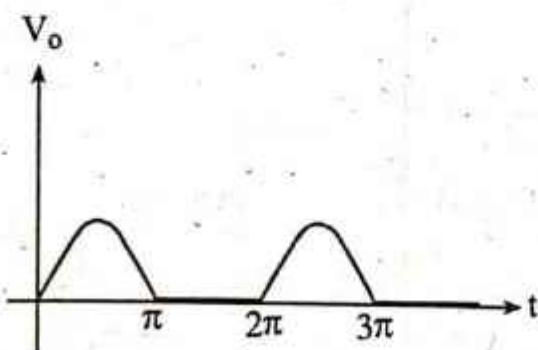


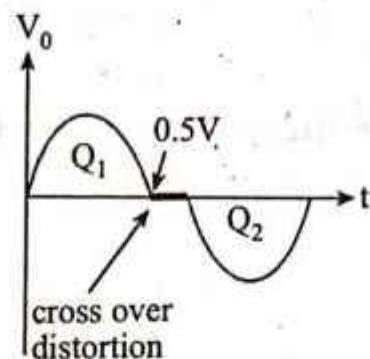
Fig. 4.7(a) Push Pull Circuit

- When  $V_{in} = 0$ ,  $V_1 = V_2 = 0$  then  $I_{CQ1} \approx I_{CQ2} = 0$
- During first half cycle, transistor  $Q_1$  conducts whereas  $Q_2$  is at cut-off mode. So  $I_{CQ1}$  current flows through transformer which results in first half cycle of signal to the load.
- During next half cycle,  $Q_2$  conducts whereas  $Q_1$  is at cutoff mode. So  $I_{CQ2}$  current flows through transformer resulting in second half cycle.
- The output transformer will combine the two outputs of  $Q_1$  &  $Q_2$ .



*Fig: Output waveform for Class B amplifier*

#### \* Cross-over distortion:



*Fig.: Cross over distortion*

In the result of small currents for  $V < V_{Threshold}$  the output is non-linear and is much smaller than it would be if response were linear. This effect is called cross-over distortion. When unbiased, a class B push pull amplifier has no output until the input voltage exceeds approx 0.7V or 0.5V. This results in clipping between positive and negative half cycles. This effect is called crossover distortion.

## Elimination

We need to apply slight forward bias to each diode of transistor i.e. the Q-point should be slightly above cut-off to avoid this distortion. In order to minimize crossover distortion, transistor must operate in a class AB mode where a small stand by current flows at zero excitation which is described in section 4.4.

## Efficiency

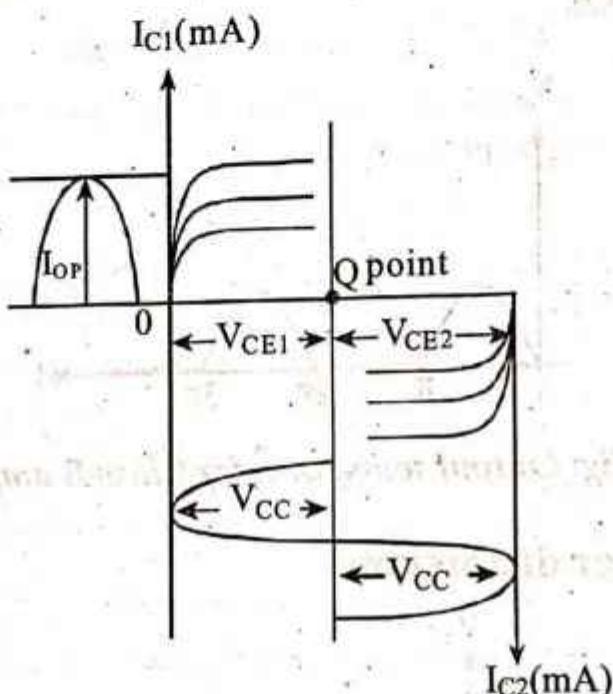


Fig. 4.7(b) Composite Characteristics for Class B push pull amplifier

Here,

$$P_o(ac) = I_o V_o$$

$$= \frac{V_o^2}{Z_L} = \frac{(V_{CC}/\sqrt{2})^2}{Z_L} = \frac{V_{CC}^2}{2Z_L} \quad \dots \dots \dots (i)$$

= maximum possible output power

$$P_i(dc) = V_{CC} I_{dc}$$

$$= V_{CC} \cdot \frac{2}{\pi} I_{OP} = V_{CC} \frac{2}{\pi} \frac{V_{CC}}{Z_L} = \frac{2 V_{CC}^2}{\pi Z_L} \quad \dots \dots \dots (ii)$$

∴ Efficiency,

$$\eta = \frac{P_O(\text{ac})}{P_i(\text{dc})} \times 100\%$$

$$= \frac{V_{CC}^2}{2Z_L} \cdot \frac{\pi}{2} \cdot \frac{Z_L}{V_{CC}^2} \times 100\% = \pi 25\%$$

Therefore,

$$\eta = 78.5\%$$

= maximum efficiency

Transformer less complementary symmetry push-pull amplifier using complementary matched transistor  $Q_1$  and  $Q_2$ . (Class B).

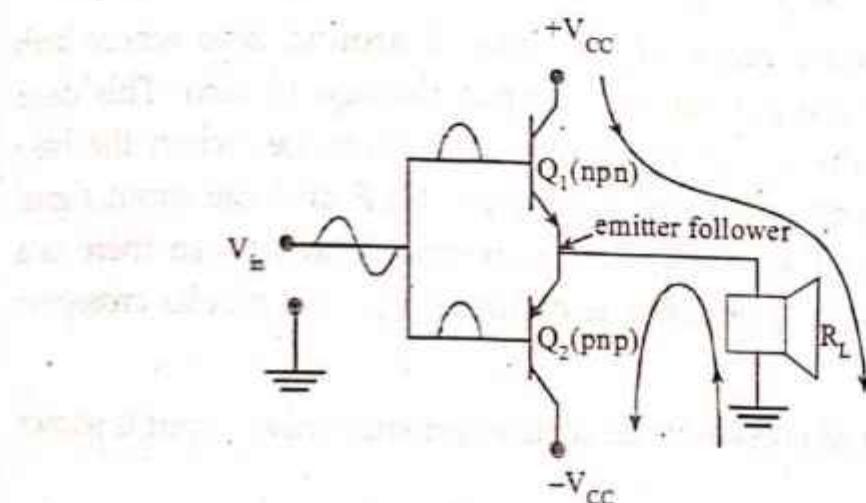
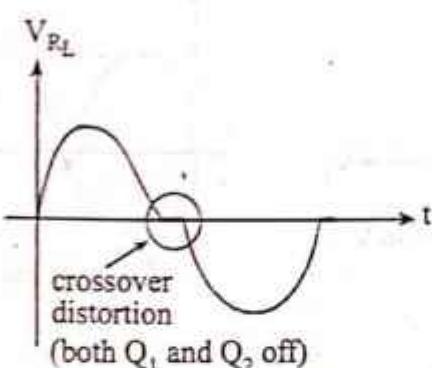


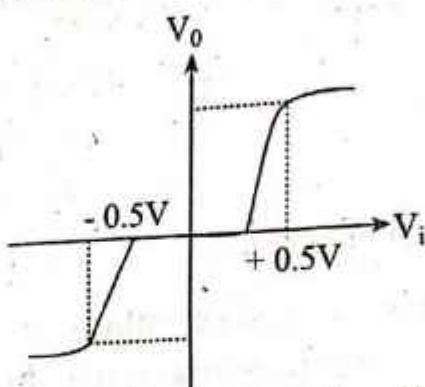
Fig. 4.7(c) Complementary Symmetry push pull amplifier



- A single input signal is applied to base of both transistors
- During first half cycle  $Q_1$  (npn) transistor will be forward biased as it operates in active mode while  $Q_2$  is at cut-off. So current  $I_C$  flows from transistor  $Q_1$  to load to ground.

- During negative half cycle,  $Q_2$  (pnp) will be biased into conduction and  $Q_1$  at cut-off. So, current flows from ground to  $-V_{CC}$ .

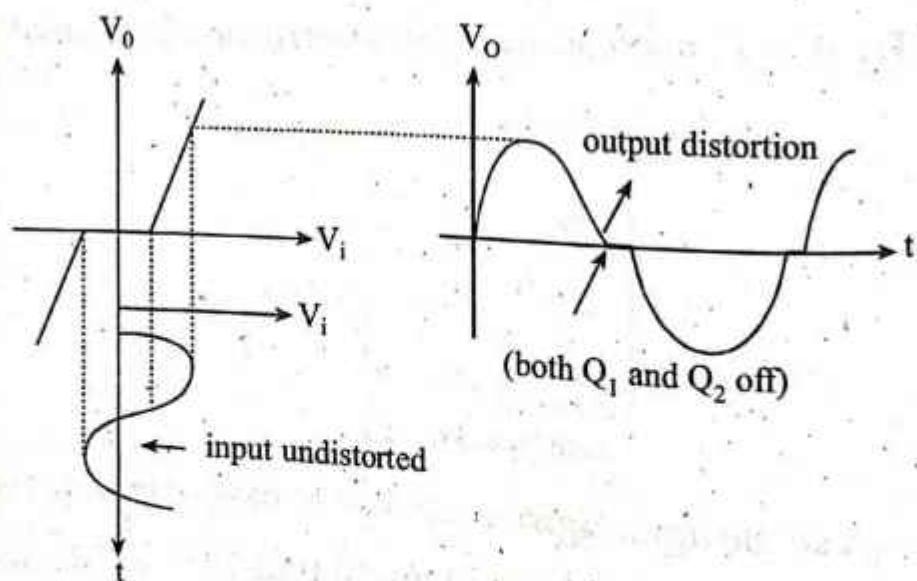
### Transfer characteristic



*Fig. 4.7(d) Transfer Characteristics of Class B amplifier*

There exists a range of  $V_i$  centered around zero where both transistor are cut off and output voltage is zero. This dead band results in the crossover distortion. i.e. when the base voltage is zero both transistor are OFF and the input signal must exceed  $V_{BE}$  before a transistor conducts, so there is a time when no transistor is conducting. This results crossover distortion.

The effect of crossover distortion on sine wave input is shown in fig.



*Fig. 4.7(e) Effect of Crossover Distortion*

## Reducing crossover Distortion

The crossover distortion of a class B output stage can be reduced substantially employing a high-gain op-amp and overall negative feedback as shown in fig:

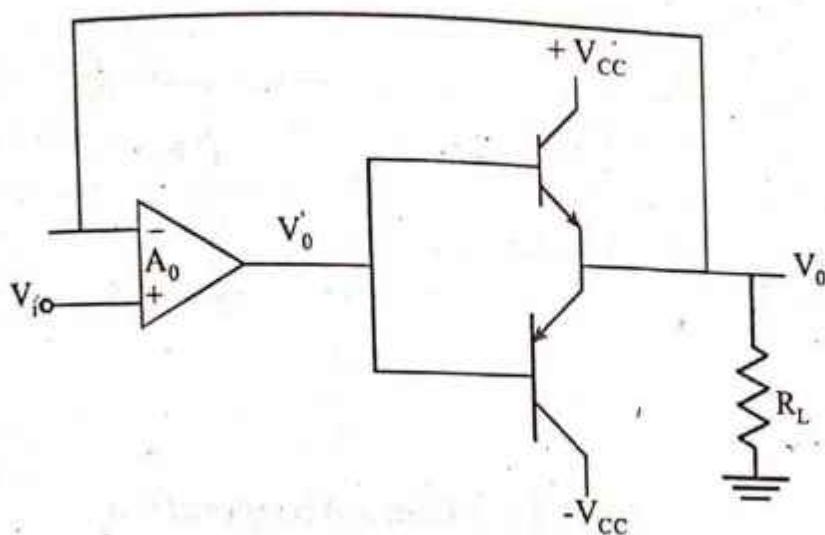


Fig. 4.7 (f) Reducing Crossover Distortion

The  $\pm 0.7$  V dead band is reduced to  $0.7 / A_o$  volts, where  $A_o$  is the dc gain of the op-amp. A more practical method for reducing and almost eliminating crossover distortion is found in the class AB operation.

### 4.5 Class AB Output Stage

An amplifier may be biased at a dc level above the zero base current level of class B amplifiers and above one half the supply voltage level of class A amplifiers. This mode of operation is class AB mode of operation of amplifier, where a small standby current flows at zero excitation resulting in less distortion than class B.

Class AB operation still needs a push-pull connection to achieve a full output cycle but the dc bias level is usually closer to zero base current level for better power efficiency. For class AB operation the output signal swing occurs between  $180^\circ$  and  $360^\circ$  and is neither class A nor class B operation.

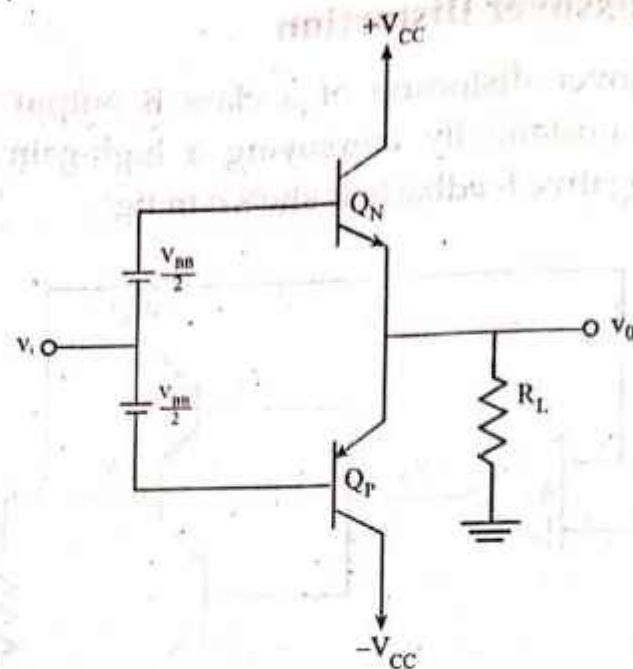


Fig.4.4 (a) Class AB operation

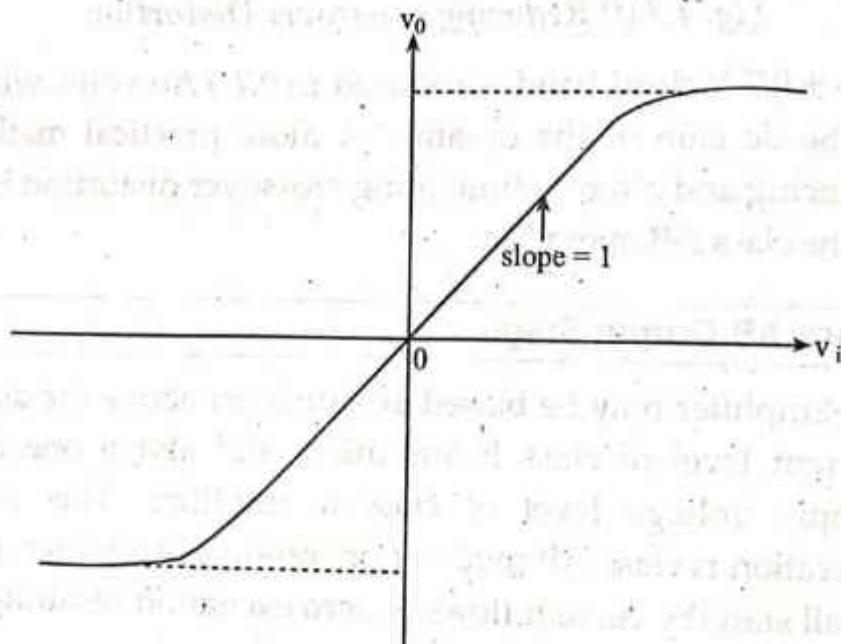


Fig. 4.4(b) Transfer Characteristics of Class AB stage

Here a bias voltage  $V_{BB}$  is applied between the bases of  $Q_N$  and  $Q_P$ , giving rise to bias current  $I_Q$ .

$$I_N = I_P = I_Q = I_S e^{(V_{BB}/2V_T)}$$

For small  $V_{in}$ , both transistors conduct and crossover distortion is almost completely eliminated. The value of  $V_{BB}$  is selected to yield the required quiescent current  $I_Q$ .

## Operation

When  $V_{in}$  goes positive by certain amount the base voltage of  $Q_N$  increases by same amount  $v_{in}$ . This increases  $I_N$  according to the corresponding increase in  $V_{BEN}$ . However since the voltage between two base is constant i.e.  $V_{BB}$ , the increase in  $V_{BEN}$  will result in an equal decrease in  $V_{BPP}$  and hence in  $I_P$ . So  $Q_P$  will be conducting a current that decreases as  $V_o$  increases; for  $V_0$  the current in  $Q_P$  can be ignored. For negative input voltage  $V_{in}$  the opposite occurs. So far small  $V_{in}$  both transistors conduct as  $V_{in}$  increased or decreased one of the two transistors take over the operation.

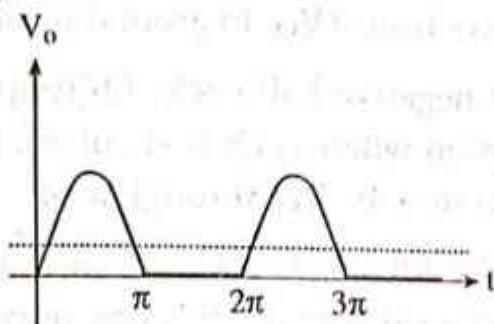


Fig: Output waveform for Class AB amplifier

## Complementary symmetry class AB push-pull amplifier:

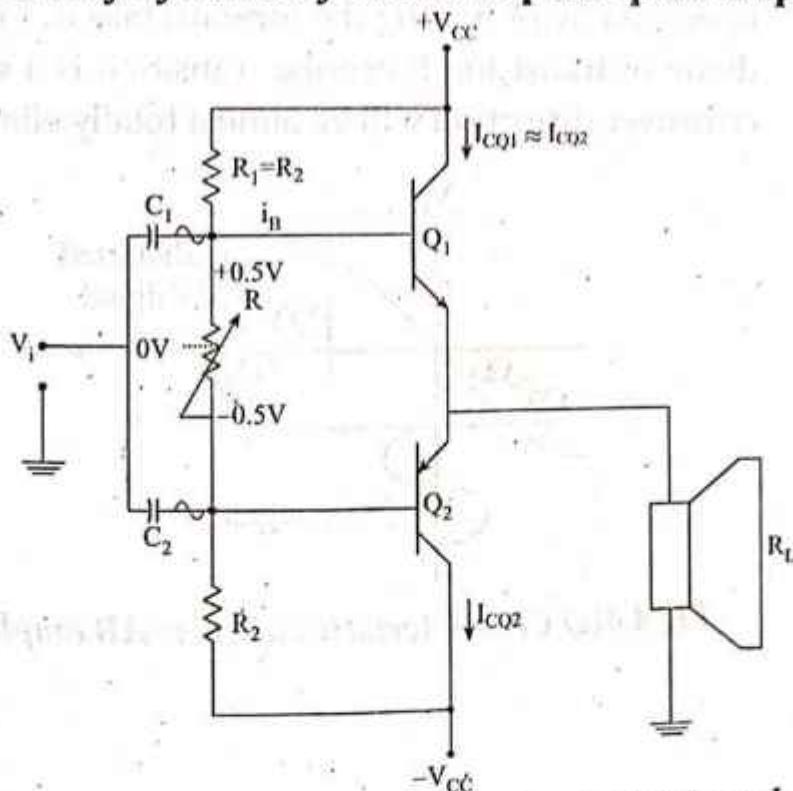
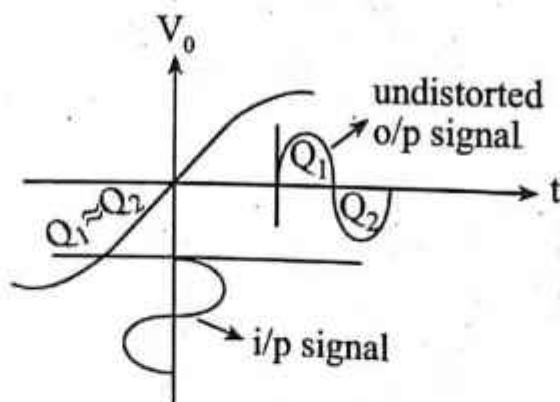


Fig.4.4(b) Complementary symmetry class AB push-pull amplifier

- To overcome the distortion, biasing is adjusted.
- This results in class AB amplifier.
- In class AB amplifier the transistor are biased into conduction even when there is no input signal.
- This is achieved by voltage divides as shown.
- When  $R_1$  and  $R_2$  are same and  $Q_1$  and  $Q_2$  are of same type then the currents in the transistor are same.
- During the positive half cycle,  $Q_1$  (npn) will be biased into conduction whereas  $Q_2$  (pnp) is cut-off. So, current  $I_{CQ1}$  flows from  $+V_{CC}$  to ground through load.
- During negative half cycle,  $Q_2$  (pnp) will be biased into conduction whereas  $Q_1$  is at cut off. So current  $I_{CQ2} \approx I_{CQ1}$  from ground to  $-V_{CC}$  through load.
- The class AB stages operates in much the same manner as the class B circuit, with one important exception. For small  $V_i$ , both transistors conducts, and as  $V_i$  is increased or decreased, one of the two transistor takes over the operation by providing the forward bias of  $\pm 0.5V$  to each diode of transistor. Since the transition is a smooth one, crossover distortion will be almost totally eliminated.



*Fig.4.4(c) Characteristics of class AB amplifier*

Figure for complementary symmetry class AB amplifier using Darlington Pair Transistors

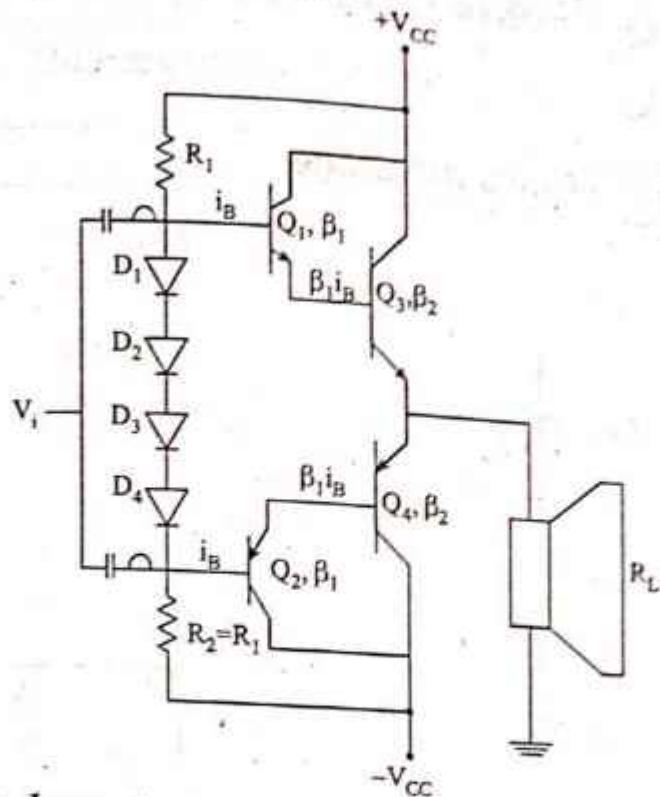


Fig. Complementary symmetry class AB amplifier using matched npn and pnp Darlington Pair Transistors

$Q_1, Q_3 \rightarrow$  npn darlington BJT,

$Q_2, Q_4 \rightarrow$  pnp darlington BJT

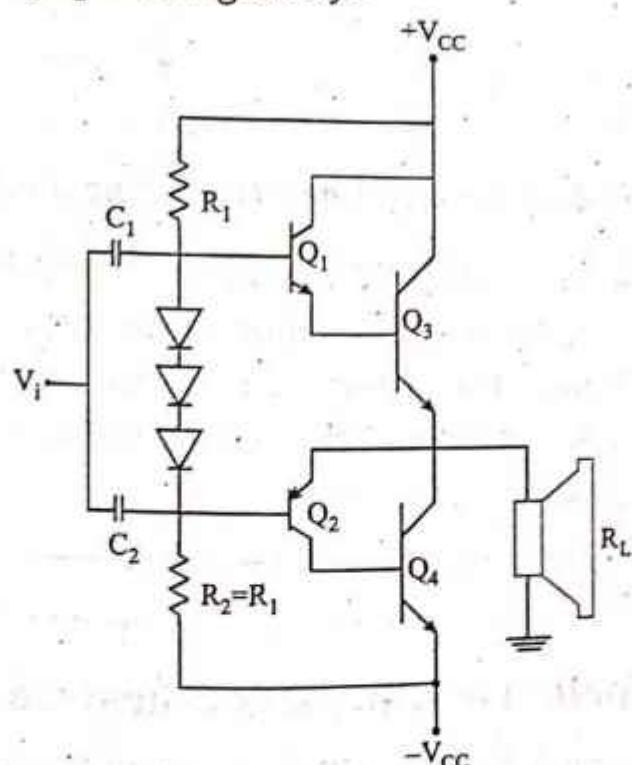


Fig. Quassi complementary symmetry class AB amplifier using matched darlington and complementary darlington pair BJT.

$Q_1, Q_3$  = matched Darlington BJT

$Q_2, Q_4$  = complementary Darlington BJT

#### 4.6 Biasing the Class AB Stage

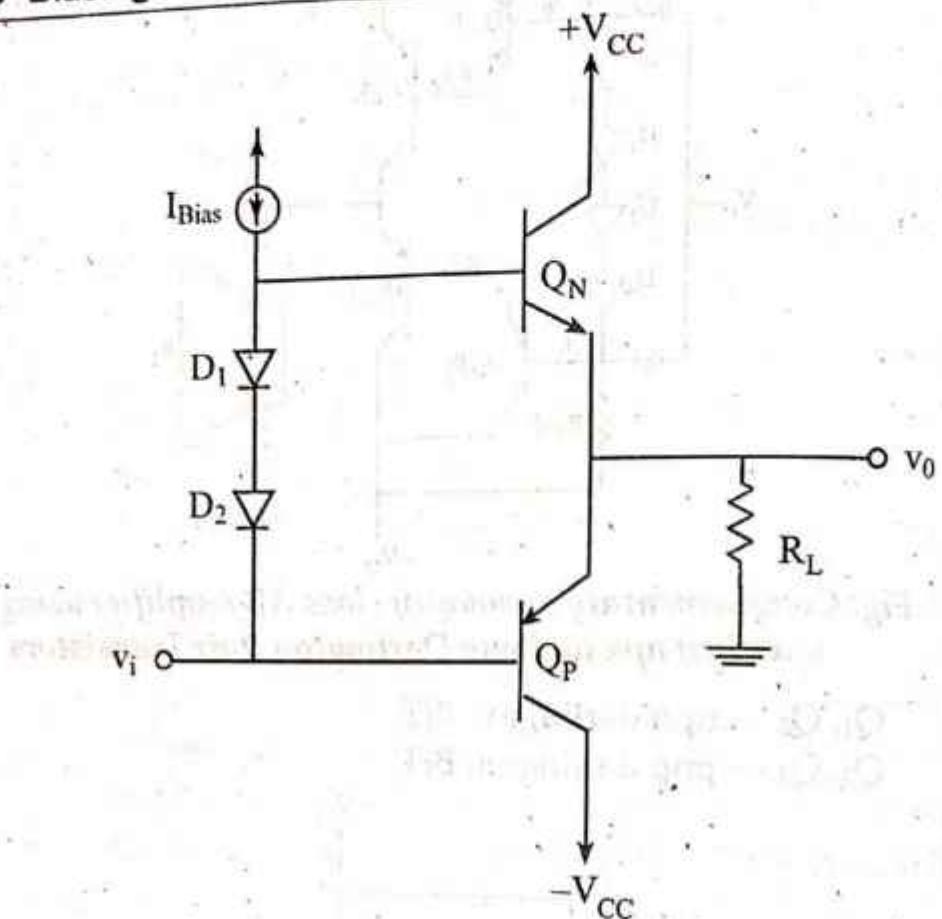


Fig.4.5 Class AB operation using diode biasing

Figure shows a class AB circuit in which the bias voltage is generated by passing a constant current  $I_{bias}$  through a pair of diodes. Though the crossover distortion is eliminated in this type of configuration, the characteristics does not pass through the origin.

#### 4.7 Power BJTs

##### Power dissipation in transistor & heat sink

The temperature at the collector junction of a transistor limits its maximum power attainable because when the power

dissipation in the transistor exceeds the maximum temperature limit of the junction, it will be damaged. Normal maximum temperature quoted by manufacturers is about 150°C to 200°C for silicon devices. Therefore it is necessary to provide some method of removing heat from the transistor. The usual method is to mount the transistor on a sheet of metal (copper or aluminum) known as heat sink. The heat produced at the collector junction of the transistor passes from its metal face casing into heat sink body and from heat sink body it radiates in the surrounding atmosphere. Thus, the junction temperature is always higher than the surrounding air and the difference of the temperature is proportional to the power dissipated in the transistor. It may be expressed mathematically as,

$$T_j - T_{amb} = P_C \times \theta.$$

This relation is called Thermal Ohm's law.

Where,

$T_j$  is temperature at collector junction

$T_{amb}$  is temperature of surrounding air

$P_C$  is power dissipation

$\theta$  is a constant which has unit of thermal resistance ( $^{\circ}\text{C}/\text{W}$ )

Thus, the temperature at junction may be expressed as,

$$T_j = T_{amb} + P_C \times \theta$$

## Design of Heat sink

For a particular power transistor of a power amplifier, the effective total thermal resistance between collector junction and surrounding air of room is made up of following components.

- i) The thermal resistance  $\theta_1$  between collector junction and transistor body (say 1.2  $^{\circ}\text{C}/\text{W}$ )

ii) The thermal resistance  $\theta_2$  of the mica washer which is generally used between the transistor case and heat sink to isolate the collector terminal electrically from heat sink yet thermally connected (say  $0.5 \text{ }^{\circ}\text{C/W}$ )

iii) The thermal resistance  $\theta_3$  of the heat sink itself. Thus depends upon mass and area of the heat sink.

Therefore, total thermal resistance,

$$\theta = \theta_1 + \theta_2 + \theta_3$$

So, equation becomes

$$T_j = T_{\text{amb}} + P_C \times (\theta_1 + \theta_2 + \theta_3)$$

#### 4.8 Tuned Amplifier

The amplifier used for amplifying a signal of specific frequency or narrow band of frequency is known as tuned amplifier. Tuned amplifiers amplify selective frequency only using LC network and hence are useful in receivers. It works only at resonance frequency. Resonant LC circuit as a load provides high impedance and so tuned amplifiers can provide high gain.

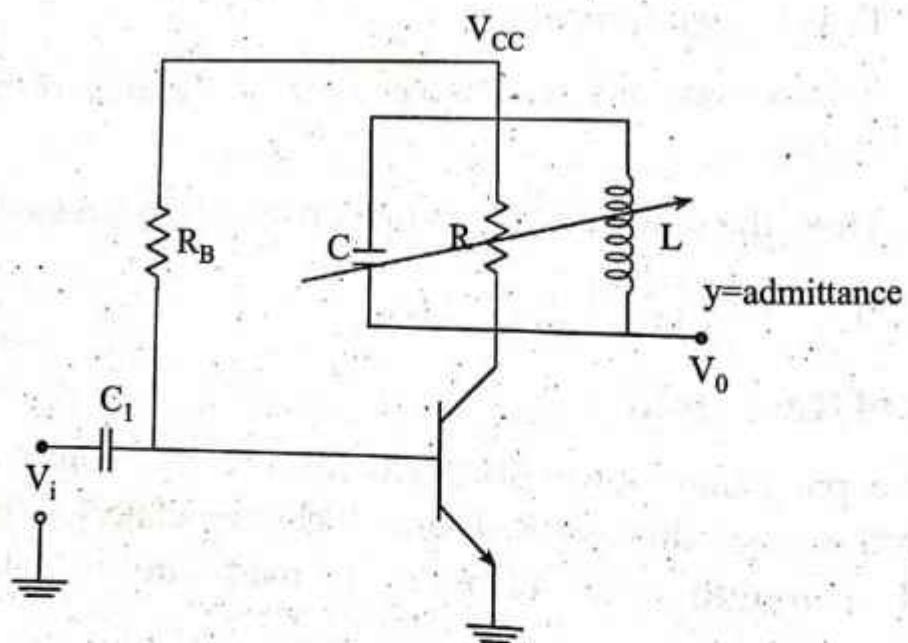


Fig.4.8 (a) Simple Class A tuned amplifier

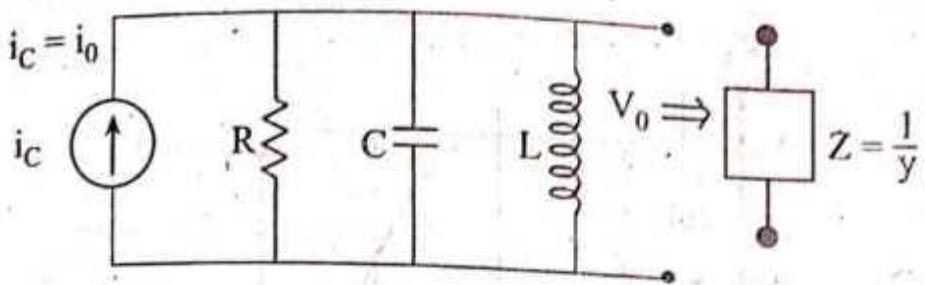


Fig. 4.8(b)

For the parallel resonance circuit as shown, the admittance is given by,

$$Y = \frac{1}{Z} = G + jB$$

Where,

$G$  = conductance and  $B$  = susceptance

$$= \frac{1}{R} + j\left(\omega_o C - \frac{1}{\omega_o L}\right)$$

We have,

$$i_C = V_o \cdot y = V_o (G + jB) \quad [\because y = \frac{1}{Z}]$$

$$\text{or, } i_C = V_o \left[ \frac{1}{R} + j\left(\omega_o C - \frac{1}{\omega_o L}\right) \right] \dots\dots\dots (1)$$

Analysis of equation (1) says that at near zero and near infinity frequency, the admittance is very high. And as a result output voltage is very low near, zero.

When the frequency increases from near zero, the output voltage raises upto a certain frequency called resonant frequency and beyond that, the output voltage falls down. At resonant frequency  $\omega_o$ , the output voltage is therefore highest. But at resonant frequency  $\omega_o$  have  $B = 0$  i.e.

$$\omega_o C - \frac{1}{\omega_o L} = 0$$

$$\text{or, } \omega_o = \frac{1}{\sqrt{LC}} \quad \omega_0 \rightarrow \text{resonant frequency } (= 2\pi f_o)$$

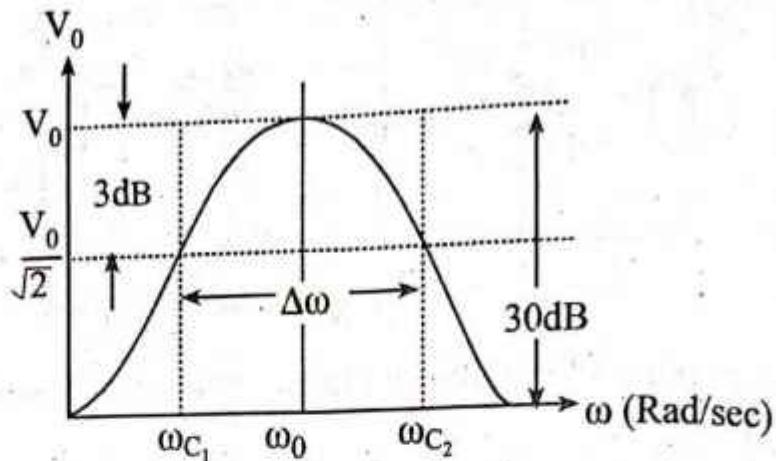


Fig.4.8(d)

At cut-off frequency of -3dB, ( $\omega_0$ ) we have,

$$|G| = |B|$$

$$\text{or, } G^2 = B^2$$

$$\text{or, } \frac{1}{R^2} = \left( \omega_{C1} \cdot C - \frac{1}{\omega_{C1} \cdot L} \right)^2$$

$$\text{or, } \omega_{C1} \cdot C - \frac{1}{\omega_{C1} \cdot L} = \pm \frac{1}{R} \dots\dots\dots (2)$$

At lower cut off frequency  $\omega_{C1}$ , we have from (2)

$$\omega_{C1} \cdot C - \frac{1}{\omega_{C1} \cdot L} = -\frac{1}{R} \dots\dots\dots (3)$$

And at higher cut- off frequency  $\omega_{C2}$ ,

$$\omega_{C2} \cdot C - \frac{1}{\omega_{C2} \cdot L} = +\frac{1}{R} \dots\dots\dots (4)$$

Adding (3) & (4)

$$(\omega_{C1} + \omega_{C2}) \cdot C - \frac{1}{L} \left( \frac{1}{\omega_{C1}} + \frac{1}{\omega_{C2}} \right) = 0$$

$$\text{or, } \omega_{C1} + \omega_{C2} = \frac{1}{LC} \left( \frac{\omega_{C1} + \omega_{C2}}{\omega_{C1} \cdot \omega_{C2}} \right)$$

$$\text{or, } \omega_{C1} \cdot \omega_{C2} = \frac{1}{LC}$$

$$\Rightarrow C \omega_{C1} = \frac{1}{\omega_{C2} L} \dots\dots\dots (5)$$

From equation (5) equation (4) becomes,

$$\omega_{C2} \cdot C - C\omega_{C1} = \frac{1}{R}$$

or,  $\omega_{C2} - \omega_{C1} = \Delta\omega = \frac{1}{RC} = B.W = \text{bandwidth}$

$\therefore$  Band width of resonant circuit

$BW = \frac{1}{RC}$  ..... (6)

### Quality factor (Q)

Quality factor is the measure of the selectivity or sharpness of the tuning of the resonant circuit.

Expressed mathematically as,

$$Q = \frac{\text{Resonant frequency}}{\text{band width}} = \frac{\omega_0}{1/RC} = \omega_0 RC$$

But,  $\omega_0 = \frac{1}{\sqrt{LC}}$

$\therefore Q = R \cdot \sqrt{\frac{C}{L}}$  ..... (7)

### Synchronous Tuning

- Used for shrinking or narrowing the Bandwidth.
- Synchronous tuning means same frequency

i.e.  $\omega_{O1} = \omega_{O2} = \omega_0$

$|T|(\text{dB})$

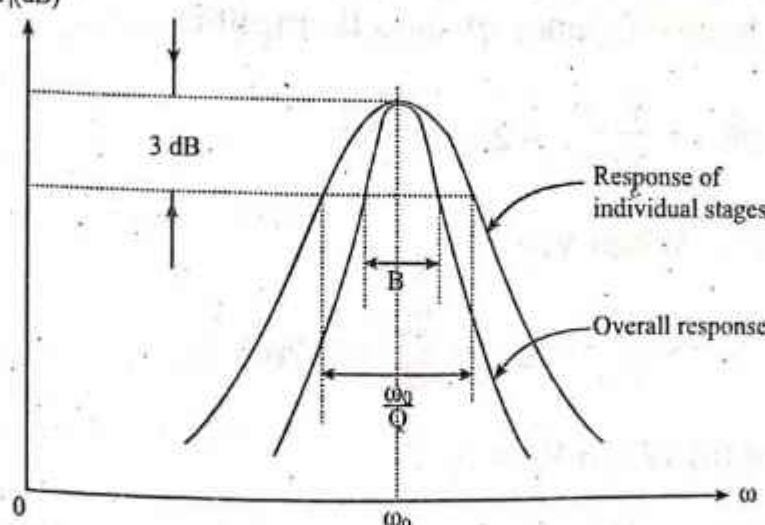


Fig. 4.8(e) Frequency response of a synchronously tuned amplifier

## Stagger Tuning

- Used for broadening the bandwidth.
- Stagger tuning means  $\omega_{01} \pm \omega_{02}$ .

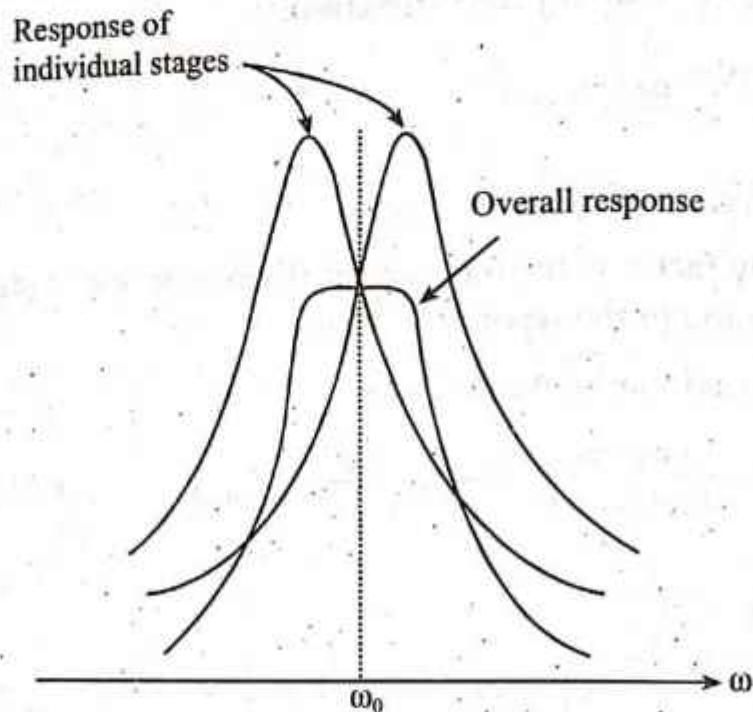


Fig. 4.8(f) Stagger tuning

- Q. Calculate the efficiency of transformer coupled push pull power amplifier for a supply voltage of 20 V and output of  
(i)  $V_P = 20$  V (ii)  $V_P = 16$  V. [069 Chaitra Regular]

*Solution:*

We have efficiency of class B amplifier

$$\eta = 25\pi \times \frac{V_{OP}}{V_{CC}} \% = 25\pi \times \frac{V_P}{V_{CC}} %$$

Case (i) When  $V_P = 20$  V

$$\eta = 25\pi \times \frac{V_P}{V_{CC}} = 25\pi \times \frac{20}{20} \% = 78.5 \%$$

Case (ii) When  $V_P = 16$  V

$$\eta = 25\pi \times \frac{V_P}{V_{CC}} = 25\pi \times \frac{16}{20} \% = 62.83 \%$$

- Q. A class B audio amplifier is providing 20 V peak sine wave signal to  $8\ \Omega$  speaker with power supply of 25 V ( $= V_{CC}$ ). At what efficiency is it operating? [068 Chaitra Regular]

*Solution:*

We know general efficiency of Class B amplifier is given by

$$\eta = 25 \pi \times \frac{V_{OP}}{V_{CC}} \% = 25 \pi \times \frac{20}{25} \% = 62.83 \%$$

Hence its efficiency is 62.83 %.

- Q. A class B push pull amplifier is providing 20V peak signal (sine wave) to a  $16\ \Omega$  load (speaker) and power supply is  $V_{CC} = 30V$ . Determine the input power, output power and circuit efficiency. [065 Chaira Regular]

$$(i) P_i (dc) = V_{CC} \cdot \frac{2V_{OP}}{\pi r_p} = 30 \times \frac{2 \times 20}{\pi \times 16} = 23.873 \text{ W}$$

$$[r_p = R_L = 16\Omega]$$

$$(ii) P_o (ac) = \frac{V_{OP}^2}{2R_L} = \frac{(20)^2}{2 \times 16} = 12.5 \text{ W}$$

$$(iii) \eta = 25 \pi \times \frac{V_{OP}}{V_{CC}} \% = 78.5 \times \frac{20}{30} = 52.33 \%$$

- Q. Suppose a dissipation of 6W is required for a transistor power amplifier & junction temperature shouldn't exceed  $80^\circ\text{C}$  and ambient temperature is  $50^\circ\text{C}$ . Find thermal resistance.

*Solution:*

$$\theta = \frac{T_j - T_{amb}}{P_C} = \frac{80 - 50}{6} = 5^\circ\text{C/W}$$

$$\text{Also, } \theta = \theta_1 + \theta_2 + \theta_3$$

$$\text{Let us assume, } \theta_1 = 1.2^\circ\text{ C/W and } \theta_2 = 0.5^\circ\text{C/W}$$

$$\therefore \theta_3 = \theta - \theta_1 - \theta_2 = 5 - 1.2 - 0.5 = 3.3^\circ\text{C/W}$$

Thus, the thermal resistance of the heat sink used should be equal to or better  $\theta_3$ .

[To achieve  $\theta_3$  of order of  $3.3^\circ\text{C}/\text{W}$ , a sheet of aluminum about 250 sq. cm in area and at least 1.6mm thick is required]

- Q. A silicon power transistor is operated with a heat sink ( $\theta_{SA} = 1.5^\circ\text{C}/\text{W}$ ). The transistor, rated at 150 W ( $25^\circ\text{C}$ ), has  $\theta_C = 0.5^\circ\text{C}/\text{W}$ , and the mounting insulation has  $\theta_{CS} = 0.6^\circ\text{C}/\text{W}$ . What maximum power can be dissipated if the ambient temperature is  $40^\circ\text{C}$  and  $T_{j\ max} = 200^\circ\text{C}$ ?

*Solution:*

$$P_D = \frac{T_j - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}}$$

$$= \frac{200^\circ\text{C} - 40^\circ\text{C}}{0.5^\circ\text{C}/\text{W} + 0.6^\circ\text{C}/\text{W} + 1.5^\circ\text{C}/\text{W}}$$

$$\approx 61.5\text{W.}$$

#### Tutorial 4

1. Why heat sink is necessary in power transistor? Explain with the help of thermal Ohm's law of thermal resistance method.
2. Draw the circuit diagram of class-A tuned amplifier. And determine the range of frequency in which it gives maximum gain within -3 dB range?
3. How does cross over distortion occur in class B push pull amplifier? Discuss the change in effect of cross over distortion when the magnitude of the input signal is reduced, and when the frequency is decreased. What will you do to eliminate cross over distortion? Discuss the impact of this remedy in terms of power dissipation
4. What is the maximum efficiency of class B amplifier? State the condition when it occurs.
5. A class B push pull amplifier is providing a 20 volt peak signal to a  $16\Omega$  (speaker) and power supply of  $V_{CC} = 30$  volt. Determine the input power, output power, and circuit efficiency.
6. What are the tuned amplifiers, and when are they used? How are they characterized?

7. Draw circuit diagram of AB push pull amplifier with darlington pair output stage.
8. Define cross over distortion in class B amplifier. Draw quasi-complementary symmetry class AB amplifier. And explain how cross over distortion is eliminated in class AB amplifier.
9. Draw a transformer coupled push-pull amplifier employing transformer in the driver circuit and using two p-n-p transistors. Comment on the power loss in these transistors at no signal condition.
10. Why the efficiency of class-A amplifier is low? Obtain the expression of the general efficiency of series fed class-A power amplifier circuit.
11. Determine the general efficiency of Transformer Coupled Class-A power amplifier.

# SIGNAL GENERATOR AND WAVEFORM-SHAPING CIRCUITS

## Introduction

Basically, the function of an oscillator (waveform generator) is to generate alternating current or voltage waveforms.

These are two distinctly different types of waveform generators:

- Sinusoidal oscillators, which utilize some form of resonance
- Non-sinusoidal oscillators or function generators, which employ switching mechanism implemented with a multi-vibrator circuit.

## Sinusoidal waveform Generators

A sinusoidal oscillator can be realized by placing a frequency selective network in the feedback path of an amplifier (a transistor or an op-amp). The circuit will oscillate at the frequency at which the total phase shift around the loop is zero, provided that the magnitude of the loop gain at this frequency is equal to, or slightly greater than unity. Some of the sinusoidal waveform generators, here we will discuss are Wein bridge oscillator, RC phase shift oscillator, LC oscillators (Hartley Oscillator, Colpitt's oscillators, Clapp Oscillaor) and crystal oscillator.

## Non-sinusoidal Waveform Generators

Most digital systems require some kind of a timing waveform, for instance, a source of triggers pulses is required for all clocked sequential systems. In digital systems, a rectangular waveform is most desirable (unlike analog systems where sinusoidal signals are often used). The generators of rectangular waveforms are

referred to as multi-vibrators. Multivibrators are of three types viz. astable (or free-running) multivibrators, monostable multivibrators (or one-shot) and bistable multivibrators (or flip-flops).

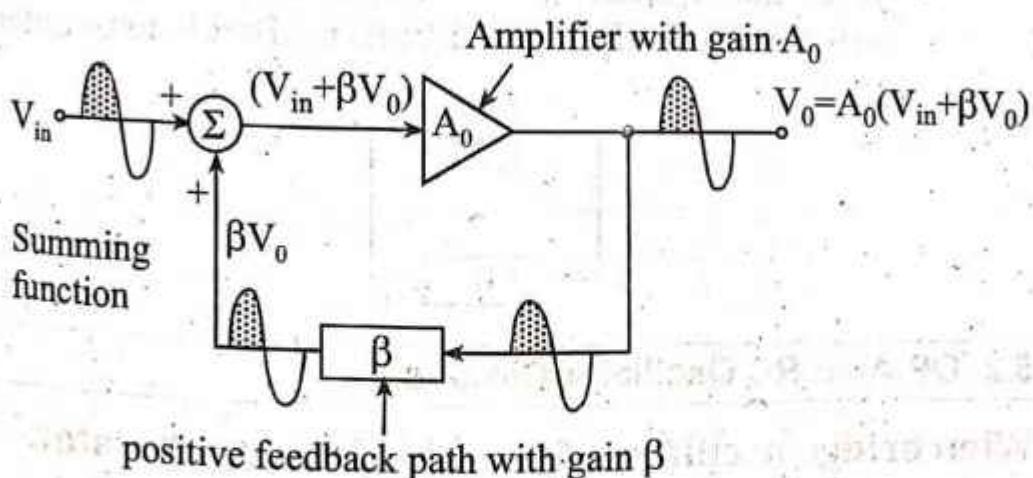
Until a few years ago, multivibrators used to be designed using discrete-devices, such as vacuum triodes, bipolar junction transistor (BJTs), field-effect transistors (FETs) etc, which have become obsolete now because of the availability of various integrated circuits (ICs). The ICs used in multivibrators are (i) opamps (ii) timers (iii) logic gates and (iv) monostable vibrators (MMVs).

Here, in this chapter we will be dealing with use of opamps, transistors, timers, logic gates, flip-flops in non-sinusoidal waveform generators.

### 5.1 Basic Principles of Sinusoidal Oscillator (or Barkhausen Criteria)

An oscillator is a device that generates a periodic, ac output signal without any form of input signal required.

The basic structure of oscillator consists of an amplifier which forms a **positive feedback** (where feedback energy is in phase with the input signal) - loop & frequency selective network as shown in below:



*Fig.5.1 Basic Oscillator Configuration*

Here;

$$V_o = A_o \times (V_{in} + \beta V_o)$$

$$\text{or, } V_o - A_o \beta V_o = A_o V_{in}$$

$$\text{or, } \frac{V_o}{V_{in}} = \frac{A_o}{1 - A_o \beta} = \text{Overall voltage gain of system (A)}$$

$$\therefore A = \frac{A_o}{1 - A_o \beta} = \frac{V_o}{V_{in}} \Rightarrow V_o = A V_{in}$$

When;  $1 - A_o \beta \rightarrow 0$  i.e.  $A_o \beta \rightarrow 1$  ( $A_o \beta$  = loop gain)

So,  $A \rightarrow \infty$

Hence when  $A \rightarrow \infty$  and  $V_{in} \rightarrow 0$

$V_o$  = finite value,

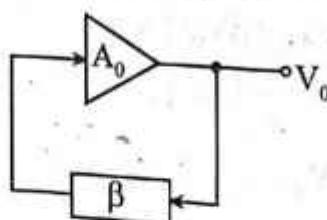
This means output voltage is produced even when no input is given. So this arrangement is called oscillator. And the condition for oscillator (Barkhausen criteria) is as follows;

- 1)  $A_o \beta = 1$  i.e. unity loop gain.
- 2) There should be positive feedback i.e. phases difference between input & output signal of feedback must be zero.

Thus we can see block diagram of an oscillator as below:

which has no input in itself & has a closed loop with no summing junction.

And the system will oscillate at a frequency which satisfies those above conditions i.e. Barkhausen criteria.



## 5.2 OP-Amp RC Oscillator Circuits

### Wien bridge oscillator: Sinusoidal wave generator.

Oscillation could also take place when the amplifier as well as the frequency determining network, both introduces zero phase shifts. This is the principle of Wien bridge oscillator.

Here the upper series RC network and the lower parallel RC network together produce a zero phase shift at the frequency of oscillation. The series RC network ( $Z_1$ ) provides a dynamic lag and the parallel RC network ( $Z_2$ ) provides an equal amount of dynamic lead, when it approaches oscillation frequency.

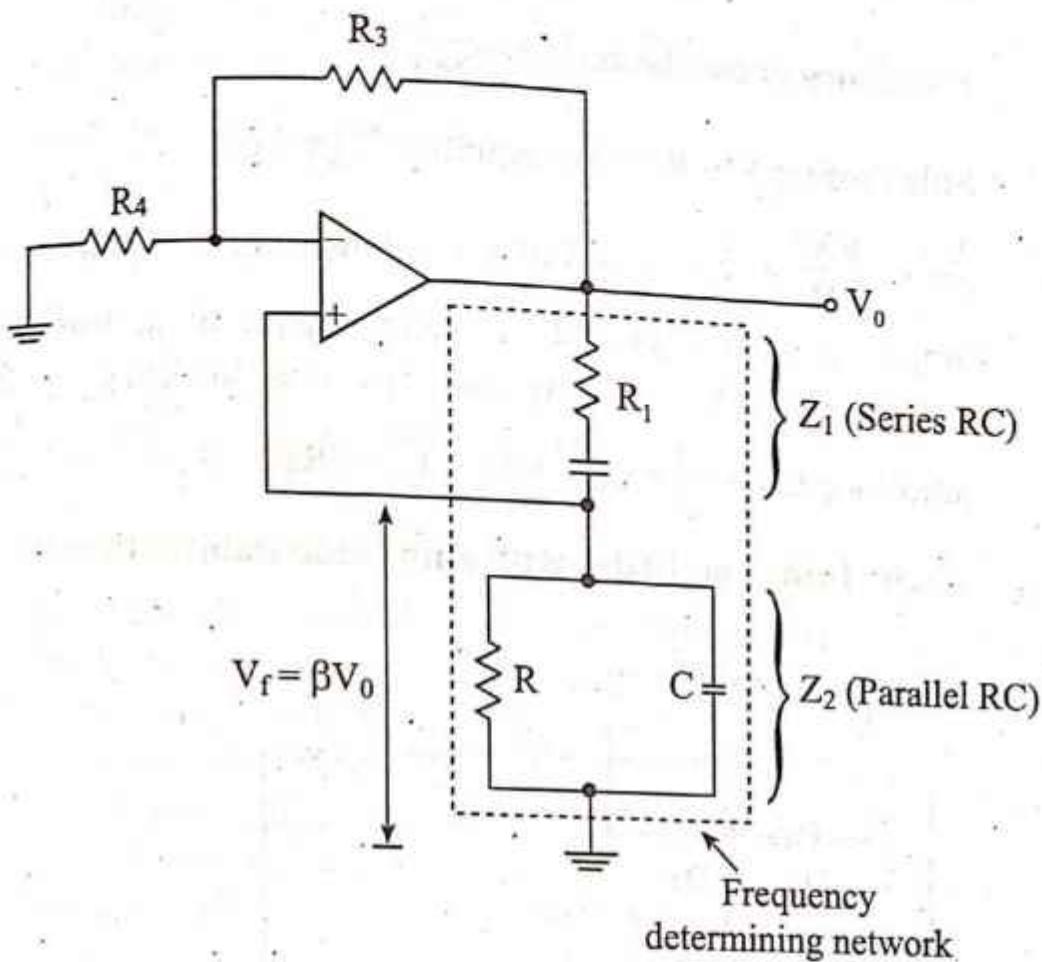


Fig.5.2(a) Wien Bridge Oscillator

From the circuit;

$$V_f = V_o \times \frac{Z_2}{Z_1 + Z_2} \Rightarrow \frac{V_f}{V_o} = \frac{-R \cdot jX / (R - jX)}{(R - jX) + \left( \frac{-R \cdot jX}{R - jX} \right)}$$

$$\text{or, } \frac{V_f}{V_o} = \frac{-jRX}{R^2 - 2jRX - X^2 - R \cdot jX} = \frac{-jRX}{-j^2 R^2 + j^2 X^2 - j^3 RX}$$

$$\therefore \frac{V_f}{V_o} = \frac{-RX}{J(X^2 - R^2) - 3RX} \dots\dots\dots (1)$$

At the frequency of zero phase shift i.e. frequency of oscillators;

We have J - operator vanishes;

$$\text{i.e. } X^2 - R^2 = 0 \text{ or, } X = +R = \frac{1}{2\pi f_0 C}$$

$$\text{Frequency of oscillation } (f_0) = \boxed{\frac{1}{2\pi RC}}$$

Substituting  $X^2 - R^2 = 0$  in equation (1) we get,

$\frac{V_f}{V_o} = \frac{RX}{3RX} = \frac{1}{3} = \beta \Rightarrow$  Voltage attenuation is 3. Hence the amplifier should provide a voltage gain of at least 3 to produce oscillation. Thus gain for non inverting op-amp amplifier, Gain =  $\left(1 + \frac{R_3}{R_4}\right) = 3$  i.e.  $R_3 = 2R_4$

\* Wien - bridge oscillator with amplitude stabilization:

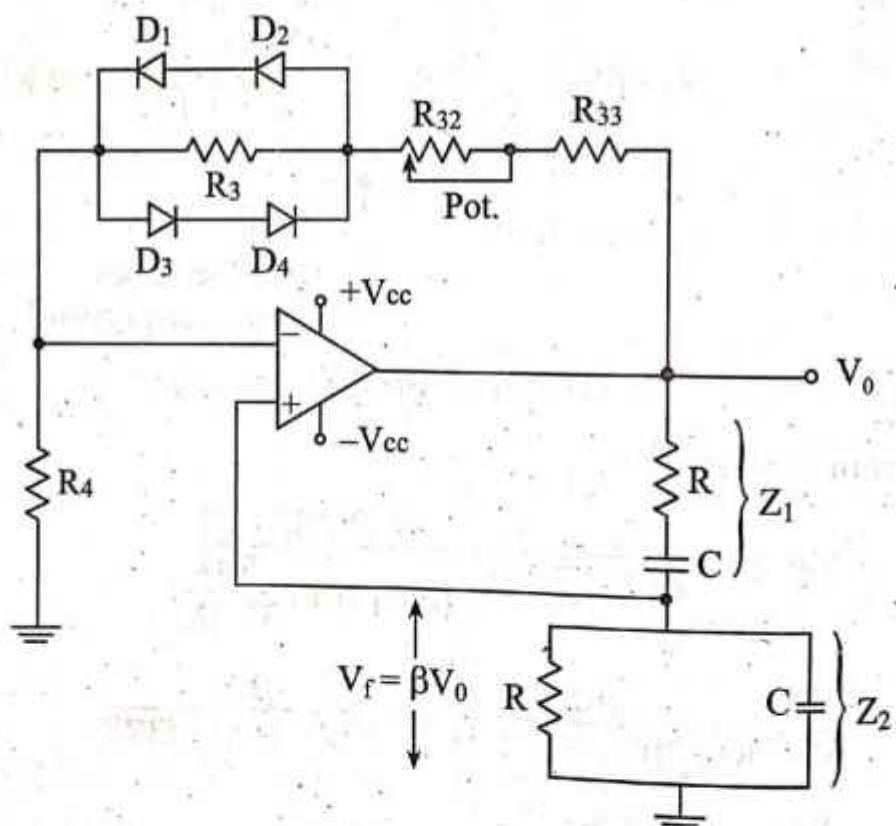


Fig.5.2 (b) Wien - bridge oscillator with amplitude stabilization

Practically  $R_3$  is not exactly  $2R_4$  (component tolerance) & amplifier is not ideal too. So  $R_3$  should be made adjustable so that loop gain can be set as necessary to sustain oscillation. In practical case ' $R_3$ ' should be made adjustable so the loop gain can be set as necessary to sustain oscillation. In practice gain is made slightly larger than 3 to provide smooth continuous oscillation. Non-linear device is used in order to form automatic gain control. (AGC)

Here,  $R_3$  = Composite values of  $R_{31}$ ,  $R_{32}$ ,  $R_{33}$  together, &  $A = \left(1 + \frac{R_3}{R_4}\right) > 3$

Potentiometer 'p' is adjusted to start oscillation. As oscillation grows diodes starts to conduct causing  $R_{31}$  to decrease & the equilibrium will be reached at the output amplitude that causes the loop gain to be unity.

### RC phase shift oscillator: (sinusoidal wave generator)

RC phase shift oscillator consists of a transistor amplifier which causes  $180^\circ$  phase shift in the signal passing through it & the purpose of 3 cascaded RC sections is to introduce an additional  $180^\circ$  ( $60^\circ$  each RC Network) at some frequency of oscillation (as shown in below circuit). This simple circuit has good frequency stability and can be used for very low frequencies.

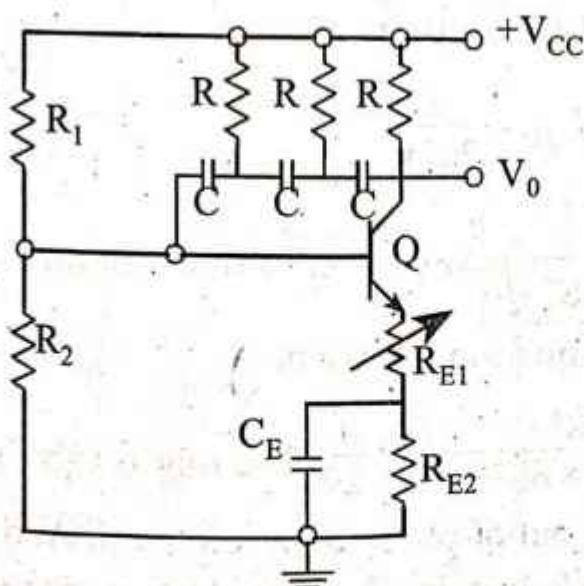
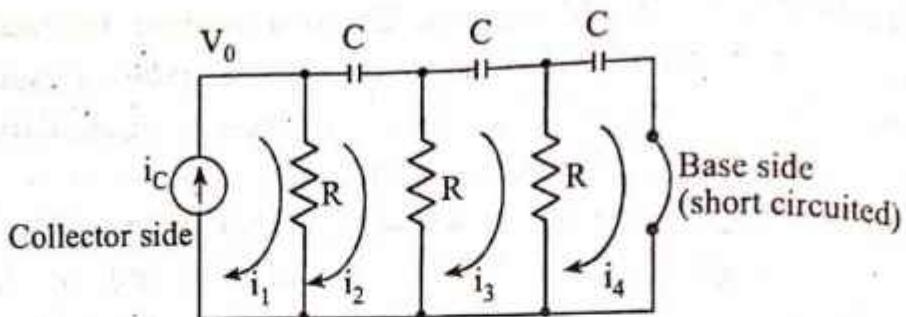


Fig.5.2(c) RC Phase Shift Oscillator



In the above figure, the phase shift network is supplied by a constant current source the collector current. And the final current is terminated into a short circuit the base current. So the current  $i_1 = i_C$  and  $i_4 = i_b$ . The ratio of  $i_4/i_1$  is then the amount of attenuation of the current when  $i_C$  finally reaches back to base as  $i_b$ . From figure 2 we have,

$$i_1R = i_2(2R - jX) - i_3R \dots\dots (i)$$

$$i_2R = i_3(2R - jX) - i_4R \dots\dots (ii) \text{ Where } |X| = \frac{1}{2\pi f_c}$$

$$\& \quad i_3R = i_4(R - jX) \dots\dots (iii)$$

Eliminating  $i_2$  &  $i_3$  from equation (iii), (ii) & (i) we have;

$$\frac{i_4}{i_1} = \frac{R^3}{R^3 - 5RX^2 + j(-6R^2X + X^3)} \dots\dots (iv)$$

For  $180^\circ$  phase shift between  $i_4$  &  $i_1$ , the term containing  $j$  operation vanishes i.e.  $(-6R^2X + X^3) = 0$

$$\text{or, } X(-6R^2 + X^2) = 0 \text{ since } X \neq 0$$

$$\therefore X = +R\sqrt{6} = \frac{1}{2\pi f_0 C}$$

$$\text{or, } f_0 = \frac{1}{2\pi RC\sqrt{6}} \rightarrow \text{frequency of oscillation substituting } X^2 = 6R^2 \text{ in equation (iv) we have}$$

$$\frac{i_4}{i_1} = \frac{R^3}{R^3 - 5R \times 6R^2 + 0} = -\frac{1}{29}; \text{ The minus sign indicates that the ratio is } 180^\circ \text{ out of phase between } i_1 \text{ & } i_4. \text{ And the 29 indicates that feedback loss is 29 times. Hence current gain of 29 is}$$

necessary from the amplifier for proper oscillation. If the gain  $> 29 \rightarrow$  distortion occurs.

$\text{Gain} < 29 \rightarrow$  oscillation can't be sustained smoothly, it decays,

### 5.3 LC and Crystal Oscillators

#### LC oscillators (Sine wave oscillator)

Hartley oscillator:

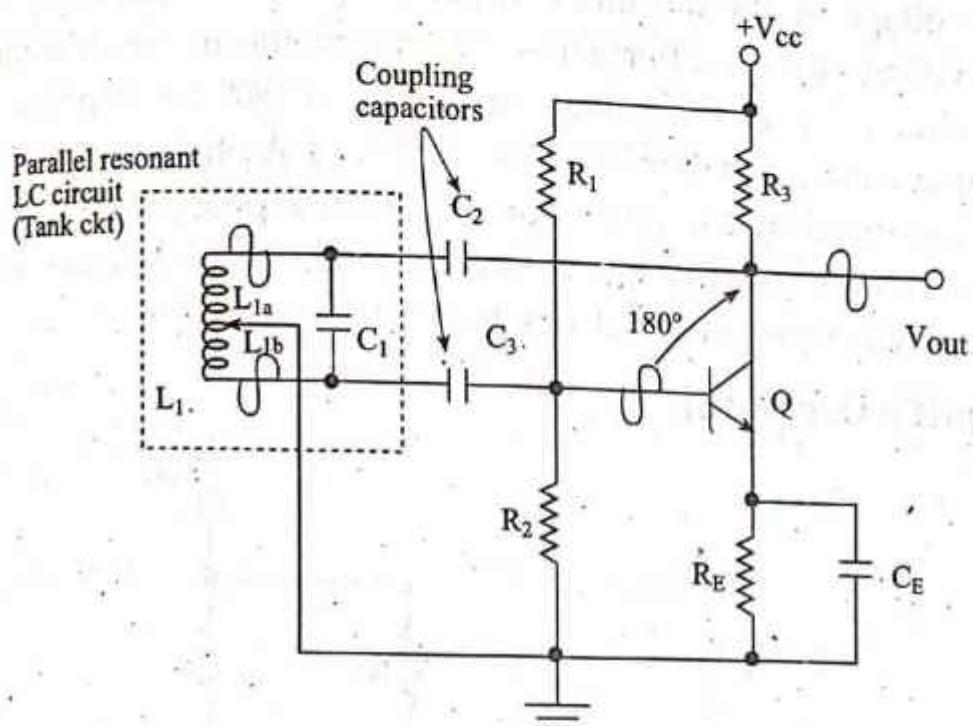


Fig.5.3 (a) Hartley oscillator

Here two inductors L<sub>1a</sub> and L<sub>1b</sub> are placed across C<sub>1</sub> and formed a tank circuit.

Where,  $L_1 = L_{1a} + L_{1b}$

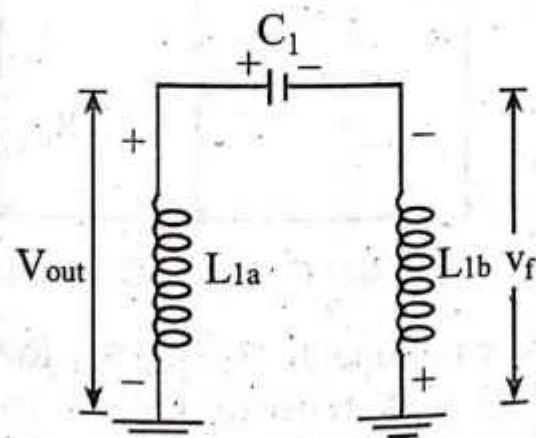


Fig.5.3 (b) Feedback Circuit

When the circuit is turned on, the capacitor is charged. When this capacitor is fully charged, it discharges through  $L_{1a}$  &  $L_{1b}$  coils setting up oscillations of frequency determined by formula;

$$f_o = \frac{1}{2\pi\sqrt{L_1 C_1}} = \frac{1}{2\pi\sqrt{(L_{1a} + L_{1b})C_1}} \Rightarrow \text{at resonance.}$$

At resonance voltage is maximum & gain = 1. The output voltage of the amplifier appears across coil  $L_{1a}$  & feedback voltage to amplifier across  $L_{1b}$ . From the figure of feedback circuit we see the voltage across  $L_{1b}$  is  $180^\circ$  out of phase with the voltage developed across  $L_{1a}$  ( $V_{out}$ ). A phase shift of  $180^\circ$  is produced by the transistor & a further phase shift of  $180^\circ$  is produced by  $L_{1a}$ - $L_{1b}$  voltage divider. In this ways circuit provides positive feedback to produce oscillation.

### Colpitt's Oscillator

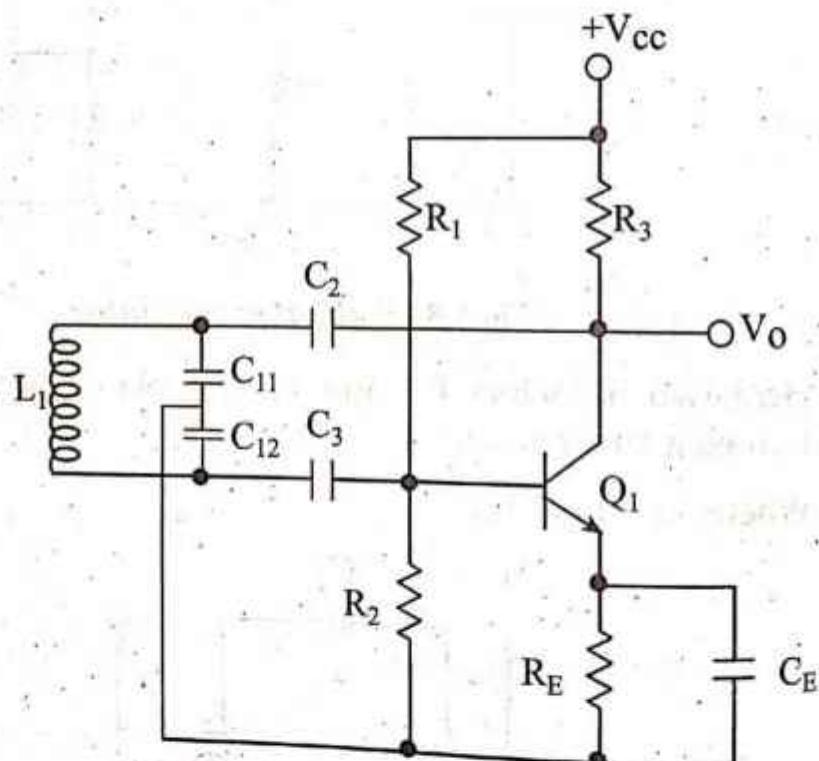


Fig. 5.3(c) Colpitt's Oscillator

In this, circuit components  $R_1$ ,  $R_2$ ,  $R_3$ ,  $R_E$  &  $C_E$  are used to stabilize dc biasing of transistor  $Q_1$ . The capacitor  $C_1$  is split into  $C_{11}$  &  $C_{12}$ . And the center point is grounded so that two  $180^\circ$  out of phase signals are produced.

Thus positive feedback is realized as in Hartley. In Colpitt's oscillator the tank resonant circuit consists of  $L_1$  & series  $C_{11}$  &  $C_{12}$ . As we see that  $C_{11}$  is effectively in parallel with  $C_{ce}$  (collector to emitter junction capacitance) whereas  $C_{12}$  is effectively in parallel with  $C_{be}$  (base to emitter junction capacitance). Therefore at high frequencies these junction capacitances affect the frequency of oscillation. And if these junction capacitances change due to temperature or supply voltage variations, the frequency of oscillation also changes. This kind of effect can be minimized by making  $C_{11}$  and  $C_{12}$  large compared to the transistor junction capacitances. This kind of variation in the circuit is called Clapp oscillator circuit.

The frequency of oscillation is given by,

$$f = \frac{1}{2\pi\sqrt{L_1 C_1}}$$

$$\text{Where, } C_1 = \frac{C_{11} C_{12}}{C_{11} + C_{12}}$$

### Clapp oscillator: (or Gouriet Oscillator)

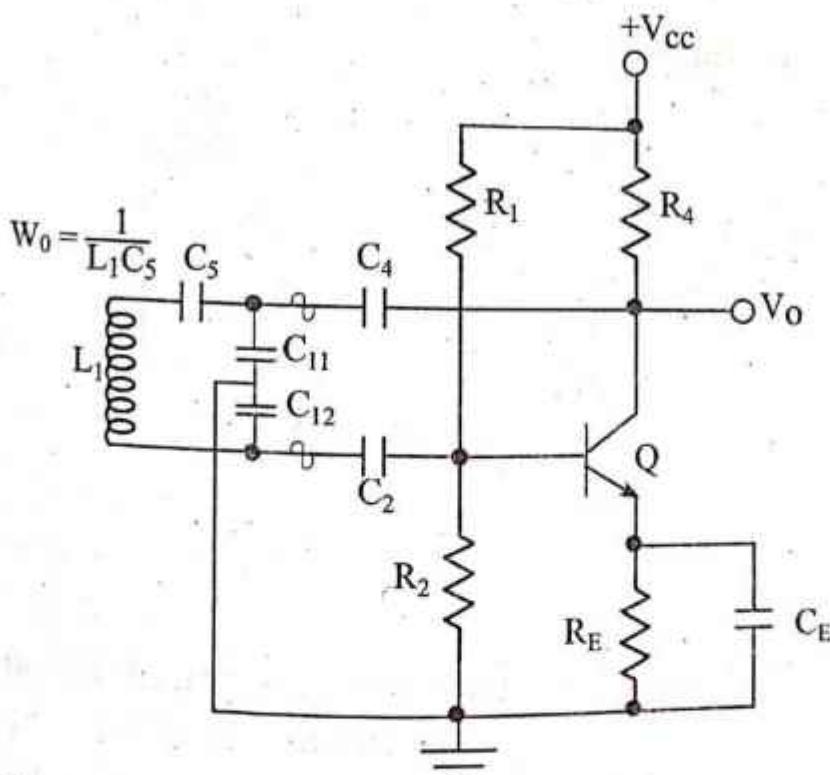


Fig.5.3 (d) Clapp oscillator: (or Gouriet Oscillator)

We can modify the Colpitt's oscillator to suit for high frequency applications which minimizes the effect of  $C_{11}$  and  $C_{12}$  which means it also minimizes the effects of junction capacitances.

A small capacitor  $C_5$  is included in series with the inductor  $L_1$  as shown in fig. Its value is usually kept smaller compared to  $C_{11}$  and  $C_{12}$ . This way the resonant frequency is mainly dependent upon the values of  $L_1$  and  $C_5$  of the tank circuit. Therefore, **very high frequency stability** can be achieved in this circuit. Therefore, it may be considered as improved version of Colpitt's oscillator.

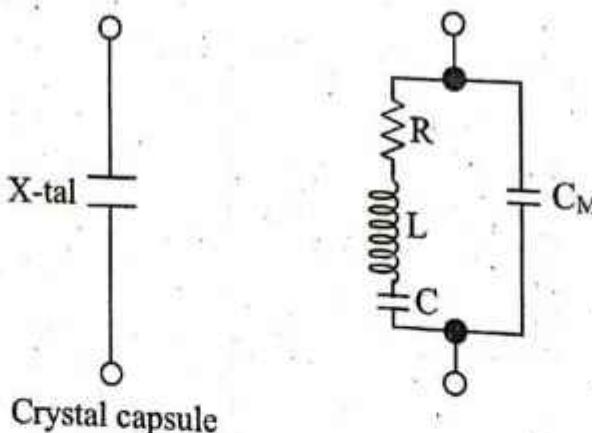
The frequency oscillation;

$$f_0 = \frac{1}{2\pi\sqrt{L_1 C_5}}$$

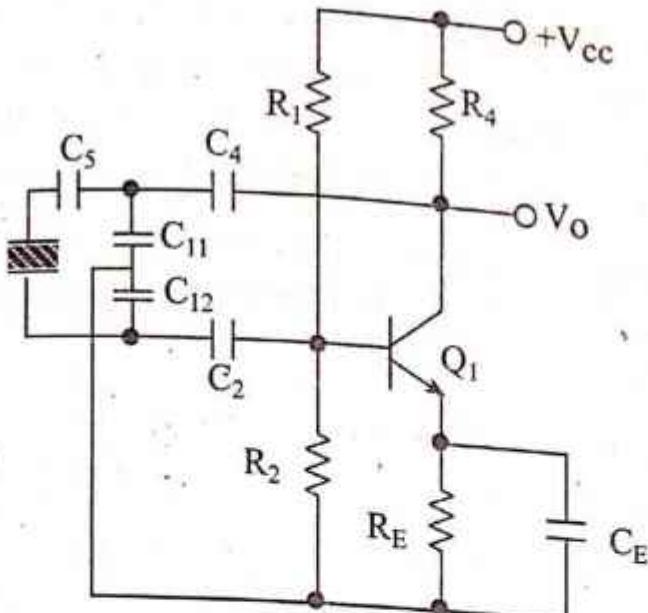
where,

$$C_{eqv} = \frac{1}{\frac{1}{C_{11}} + \frac{1}{C_{12}} + \frac{1}{C_5}}$$

### Crystal oscillator:



*Fig.5.3 (e) Basic symbol for crystal and its equivalent electrical circuit*



*Fig.5.3 (f) Basic crystal oscillator circuit using Clapp circuit*

When accuracy and stability of the oscillation frequency are required greatly, then a crystal oscillator is used. The resonance property of a crystal is very sharp. That means its frequency of resonance is very narrow & stable.

In equivalent electrical circuit,

R = Electrical equivalent of resistance; which is property of crystal structure's internal friction or mechanical resistance.

L = Electrical equivalent of inductance; which is property of crystal structure's mass inertial in mechanics.

C = Electrical equivalent of capacitance which is property of crystal structure's compliance (elasticity)  $\Rightarrow$  analogous to capacitance

$C_M$  = Shunt capacitance equivalent to compliance produced by the mechanical mounting of the crystal.

In this oscillator circuit,  $L_1$  and  $C_5$  (of clapp circuit) is replaced by the crystal module (crystal capsule). The crystal acts as a resonant tank circuit of oscillator. And the  $C_{11}$  and  $C_{12}$  divides the signal voltage between input and output sections. So, the feedback signal comes from a capacitive loop. A crystal module may also be regarded as a series RLC circuit as

shown in above figure, with large inductance of high  $Q_2$  Quality factor & a small capacitance. Therefore, the resonance frequency is almost unaffected by the transistor's junction capacitances as well as external stray capacitances.

When voltage is applied on crystal module, vibrates due to piezoelectric effect & frequency of oscillation is high & depends upon size & nature.

- It is basically a tuned circuit oscillator
- Uses piezoelectric crystal as a resonant tank circuit

The crystal can have two resonant frequencies. One resonant condition occurs when the reactances of the series RLC leg are equal & opposite. For this condition, the series resonant impedance is very low (equal to  $R$ ).

The other resonant condition occurs at a higher frequency when the reaction of the series-resonant leg equals the reactance of capacitor  $C_M$ . This is parallel resonance (also called anti-resonance) of crystal, which offers a very high impedance.

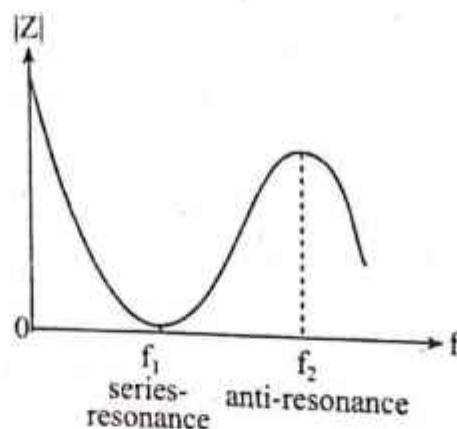


Fig.5.3(g) Crystal impedance Vs frequency

#### 5.4 Generation of Square and Triangular Waveforms Using Astable Multi-vibrators

##### # OP-Amp Square Wave Generator

It produces a square wave (rectangular) output whose frequency depends upon the charging or discharging time of capacitor used.

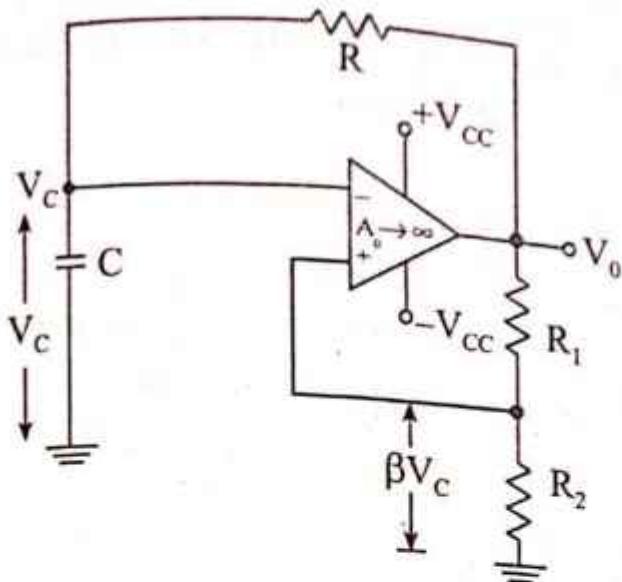


Fig.5.4 (a) OP-Amp Square Wave Generator

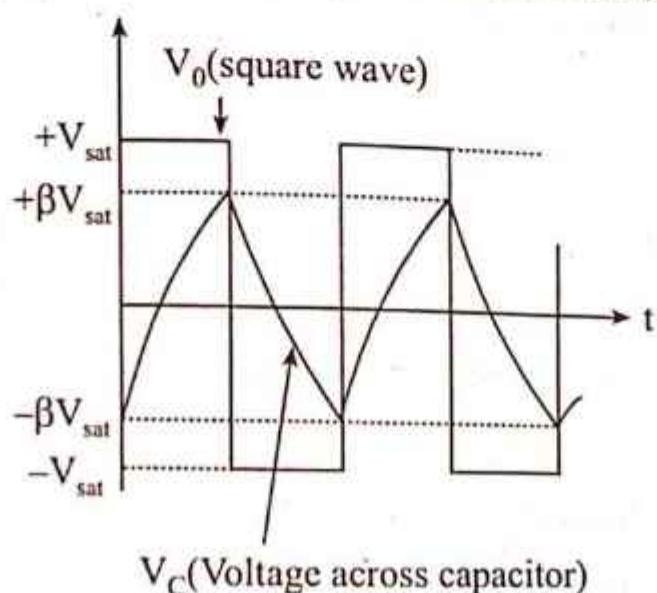


Fig.5.4 (b) Waveform of oscillator

## # Operation of the circuit

Suppose  $V_o = +V_{sat}$  &  $V_C = V^- = \text{voltage across capacitor} = -\beta V_{sat}$ . Thus when  $V_o = +V_{sat}$ , then  $V^+ = +\beta V_{sat}$  &  $V^- = 0 \Rightarrow$  Capacitor charges towards  $+V_{sat}$ , exponentially.

When  $V^- = V_C$  exceeds  $+\beta V_{sat}$   $V_o$  becomes  $-V_{sat}$ . So when  $V_o = -V_{sat}$ ,  $V^+ = -\beta V_{sat}$  &  $V^- = +\beta V_{sat}$ , capacitor discharges for  $+\beta V_{sat}$  towards  $-V_{sat}$ . After certain time when  $V_C$  exceeds  $-\beta V_{sat}$   $V_o$  becomes  $+V_{sat}$ . When  $V_o = +V_{sat}$  &  $V^+ = +\beta V_{sat}$  and  $V^- = -\beta V_{sat} \Rightarrow$  Capacitor again charges from  $-\beta V_{sat}$  towards

$+\beta V_{sat}$ . Thus the cycle repeats & it continues producing square wave output voltage.

## # Determination of time period

Let the time taken to charge the capacitor from  $-\beta V_{sat}$  to  $+\beta V_{sat}$  be  $t_1$  which is equal to  $t_2$  (i.e. time of discharging from  $+\beta V_{sat}$  to  $-\beta V_{sat}$ ). Then time period of square wave is given by

$$T = t_1 + t_2 \quad \therefore t_1 = t_2$$

$$\therefore t_1 = \frac{T}{2} \dots\dots\dots (i)$$

For charging of capacitor using basic formula;

$$V_C(t) = V_{\text{Applied}} - [V_{\text{Applied}} - V_C(\text{initial})]e^{-t/RC} \dots\dots\dots (ii)$$

Where after time  $t_1$ ;

$$V_C(t_1) = +\beta V_{sat}; V_{C(\text{initial})} = -\beta V_{sat}; V_{\text{Applied}} = +V_{sat}$$

From equation (ii)

$$+\beta V_{sat} = +V_{sat} - [+V_{sat} - (-\beta V_{sat})]e^{-t_1/RC}$$

$$\text{or, } \beta = 1 - (1 + \beta)e^{-t_1/RC}$$

$$\text{or, } (1 + \beta)e^{-t_1/RC} = (1 - \beta)$$

$$\text{or, } \frac{(1 + \beta)}{(1 - \beta)} = e^{t_1/RC}$$

Taking natural log,

$$\text{or, } \frac{t_1}{RC} = \ln \left( \frac{1 + \beta}{1 - \beta} \right)$$

$$\therefore t_1 = RC \ln \left( \frac{1 + \beta}{1 - \beta} \right) = t_2$$

$$\therefore \text{Time period } T = 2RC \ln \left( \frac{1 + \beta}{1 - \beta} \right)$$

& frequency of oscillation

$$f = \frac{1}{T} = \frac{1}{2RC \ln \left( \frac{1 + \beta}{1 - \beta} \right)}$$

## # Triangular Wave Generator

By integrating square wave, triangular wave can be generated. Actually the integrator causes linear charging & discharging of the capacitor, providing a triangular waveform.

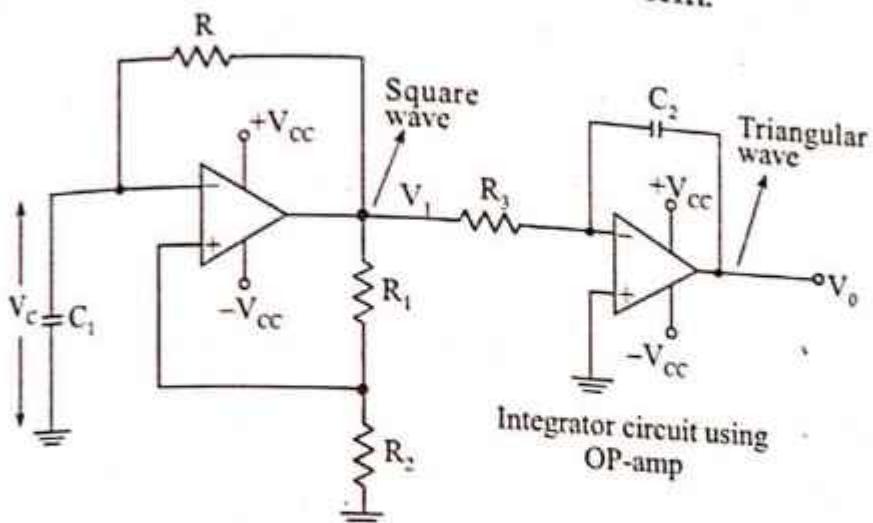


Fig. 5.4(c) Triangular Wave Generator:

Let the output of square wave generator circuit ( $V_1$ ) be  $+V_{sat}$ . A current equal to  $\frac{+V_{sat}}{R_3}$  will flow into resistor  $R$  & through capacitor  $C_2$ , causing the output of the integrator to linearly decrease with a slope of  $\frac{-V_{sat}}{R_3 C_2}$ . Because output of an op-comp integrator circuit will be

$$V_o = -\frac{1}{R_3 C_2} \int V_1 dt = \text{either } +V_{sat} \text{ or } -V_{sat}$$

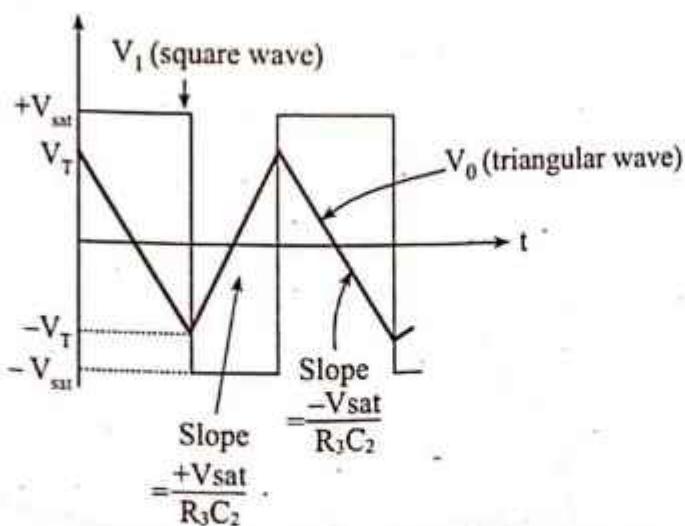


Fig. 5.4(d) Waveform of oscillator

This will continue until the integrator output reaches the lower threshold  $-V_T$  of the circuit, at which point  $V_1$  will switch states from  $+V_{sat}$  to  $-V_{sat}$ . At this moment the current through  $R_3$  &  $C_2$  will reverse direction & the integrator output will start to increase linearly with a positive slope  $\frac{+V_{sat}}{R_3 C_2}$ . This will continue until the integrator output voltage reaches the positive threshold of the circuit  $V_T$ . At this point  $V_1$  will switch its state from  $-V_{sat}$  to  $+V_{sat}$ . And the cycle will repeat so on.

#### Square wave generator using Astable multivibrator (AMV) (BJT Relaxation oscillator):

An astable multivibrator (AMV) has no stable state. It oscillates between two quasi-stable states. Thus it generates a periodic waveform at output.

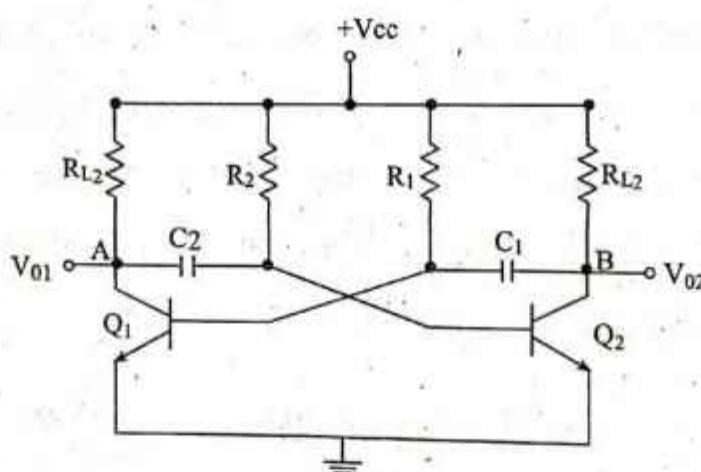


Fig.5.4 (e) BJT Relaxation oscillator

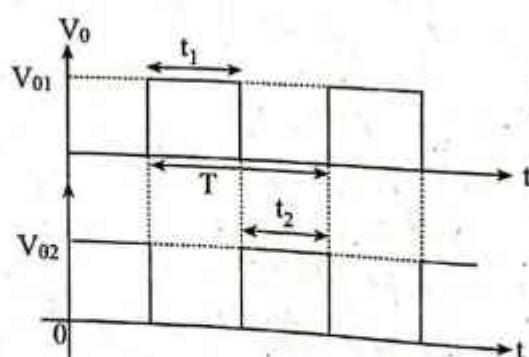


Fig.5.4 (f) Waveform of Oscillator

## Operation

When  $V_{CC}$  is applied, collector currents start flowing in  $Q_1$  and  $Q_2$ . In addition, the coupling capacitors  $C_1$  and  $C_2$  also starts charging up. As the characteristics of no two transistors (i.e.  $\beta$ ,  $V_{BE}$ ) are exactly alike, therefore, one transistor  $Q_1$  will conduct more rapidly than the other  $Q_2$ . The rising collector current in  $Q_1$  drives its collector less positive, which is applied to base transistor  $Q_2$  through  $C_2$ . Decreasing potential at A (i.e. decreasing biasing of  $Q_2$ ) will reduce collector current of  $Q_2$ . Their actions occur very rapidly & may be considered practically instantaneous.

So initial state:  $Q_2$  = cut off = OFF state;  $Q_1$  = saturation = ON state. So  $V_{BE1} = +0.7V \approx 0V$ .  $C_2$  was previously charged to  $V_{CC}$  with base of  $Q_2$  at negative potential.

$Q_1$  is kept ON by forward bias current through  $R_1$  to its base. And, as a result, its collector voltage approaches near ground potential. And  $C_1$  charges to  $V_{CC}$  with base negative potential rapidly.  $Q_2$  is kept OFF by voltage  $-V_{CC}$  applied at its base due to charge stored in  $C_2$ . This is unstable state,  $C_2$  discharges through  $R_2$ . After certain time of  $t_2$ ,  $C_2$  completely discharges and then reverse charges to  $+0.7V$ . As a result,  $Q_2$  becomes ON.

→ Each CE amplifier state provides strong feedback to other. The transistors are driven into saturation or cut off.

$Q_2$  is kept ON by forward bias current through  $R_2$  to its base. And as a result, its collector voltage approaches near ground potential. And  $C_1$  charges to  $V_{CC}$  voltage with base negative potential rapidly. The charge stored in  $C_1 (-V_{CC})$  reverse biases  $Q_1$ . And so,  $Q_1$  is OFF. This is unstable state,  $C_1$  discharges through  $R_1$ . After certain time of  $t_1$ ,  $C_1$  completely discharges and then reverse charges to  $+0.7V$ . As a result,  $Q_1$  becomes ON; forcing  $Q_2$  OFF.

This is initial state of operation, which is just described. Thus next cycle begins.

## Determination of time period

The time taken to discharge  $C_2$  from  $-V_{CC}$  to  $0V$  is given by following basic formula.

$$V_{C2} = V_{\text{Applied}} - [V_{\text{Applied}} - V_{C(\text{initial})}]e^{-t_2/R_2 C_2}$$

where,  $V_{C2} = 0V$ ;  $V_{\text{Applied}} = +V_{CC}$ ,  $V_C(\text{initial}) = -V_{CC}$  & time taken =  $t_2$

$$\therefore 0 = V_{CC} - [V_{CC} - (-V_{CC})]e^{-t_2/R_2 C_2}$$

$$\text{or, } 1 = 2 e^{-t_2/R_2 C_2} \Rightarrow \therefore t_2 = R_2 C_2 \ln 2$$

$$\text{Similarly, } t_1 = R_1 C_1 \ln 2$$

And time period  $T = t_1 + t_2 = (R_1 C_1 + R_2 C_2) \ln 2$  if  $R_1 = R_2 = R$  &  $C_1 = C_2 = C$  then it becomes square wave oscillator

$$\& T = 2RC \ln 2 = 1.38 RC$$

$$\therefore f = \frac{1}{T} = \frac{0.72}{RC} \rightarrow \text{frequency of oscillation}$$

## 5.5 Integrated Circuit Timers

### Astable Multivibrator (AMV) using 555 timer IC (Square wave Generator):

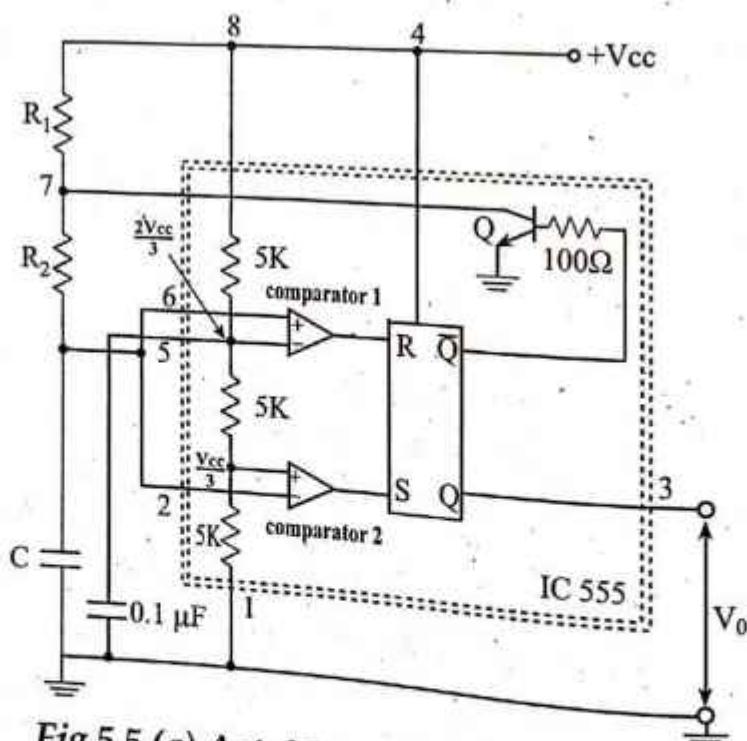


Fig.5.5 (a) Astable Multivibrator using 555 timer IC  
(Square wave Generation)

## operation

Suppose the initial state is  $V_C = 0$  (capacitor C completely discharged),  $R = 0, S = 1$ . When  $V_C = 0, R = 0, S = 1$ , result is  $Q = 1, \bar{Q} = 0$ . So pin 7 will be open circuited due to internal transistor at cut off i.e. unbiased by  $\bar{Q} = 0$ , base input. So the capacitor 'C' charges through  $(R_1 + R_2)$  towards  $V_{CC}$ .

When,  $V_C > \frac{V_{CC}}{3}, R = 0, S = 0 \Rightarrow$  result is no change. So capacitor continues to charge.

When,  $V_C \geq 2\frac{V_{CC}}{3}$  (equal to  $V^-$  of comparator 1)

$R = 1, S = 0$  result is  $Q = 0$  and  $\bar{Q} = 1$ ; Now pin 7 short circuited to ground due to  $\bar{Q} = 1$ . Capacitor 'C' starts to discharge through  $R_2$  from  $\frac{2V_{CC}}{3}$  towards ground.

When  $V_C < \frac{2V_{CC}}{3} \Rightarrow R = 0, S = 0$ , result is no change capacitor continues to discharge.

When  $V_C \leq \frac{V_{CC}}{3}, \Rightarrow R = 0, S = 1$  result is  $Q = 1, \bar{Q} = 0$ ; Now pin 7

open circuited due to  $\bar{Q} = 0$ . The capacitor starts charging again towards  $V_{CC}$ . This action continues endlessly, And the capacitor

charges and discharges between  $\frac{V_{CC}}{3}$  to  $2\frac{V_{CC}}{3}$  and back.

## Determination of time period:

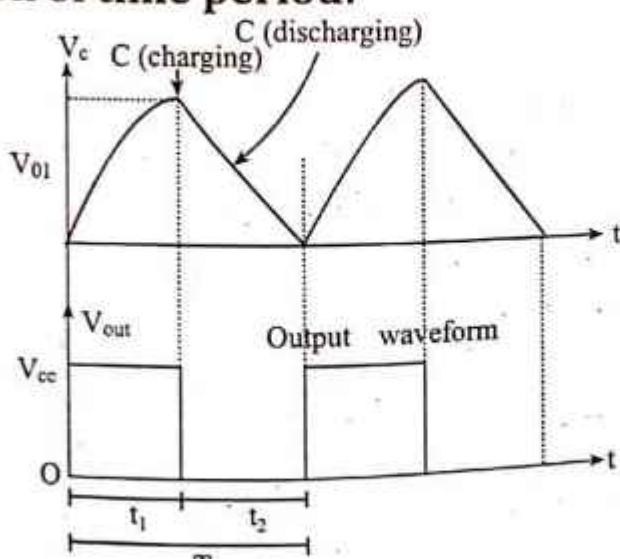


Fig.5.5 (b) Waveform

Let  $t_1$  = charging time of 'C'

$t_2$  = discharging time of 'C'

$$V_C(t_1) = V_{\text{applied}} - [V_{\text{applied}} - V_{\text{initial}}] e^{-t_1/(R_1 + R_2)C}$$

$$\Rightarrow t_1 = (R_1 + R_2)C \ln 2$$

$$V_C(t_2) = V_{\text{applied}} - [V_{\text{applied}} - V_{\text{initial}}] e^{-t_2/R_2C}$$

For Charging:

$$\frac{2}{3}V_{CC} = V_{CC} - \left[ V_{CC} - \frac{V_{CC}}{3} \right] e^{-t_1/(R_1 + R_2)C}$$

$$t_1 = (R_1 + R_2)C \ln 2$$

For discharging;

$$\frac{1}{3}V_{CC} = 0 - \left[ 0 - \frac{2}{3}V_{CC} \right] e^{-t_2/R_2C}$$

$$\Rightarrow t_2 = R_2C \ln 2$$

$$\therefore T = t_1 + t_2 = (R_1 + 2R_2)C \ln 2$$

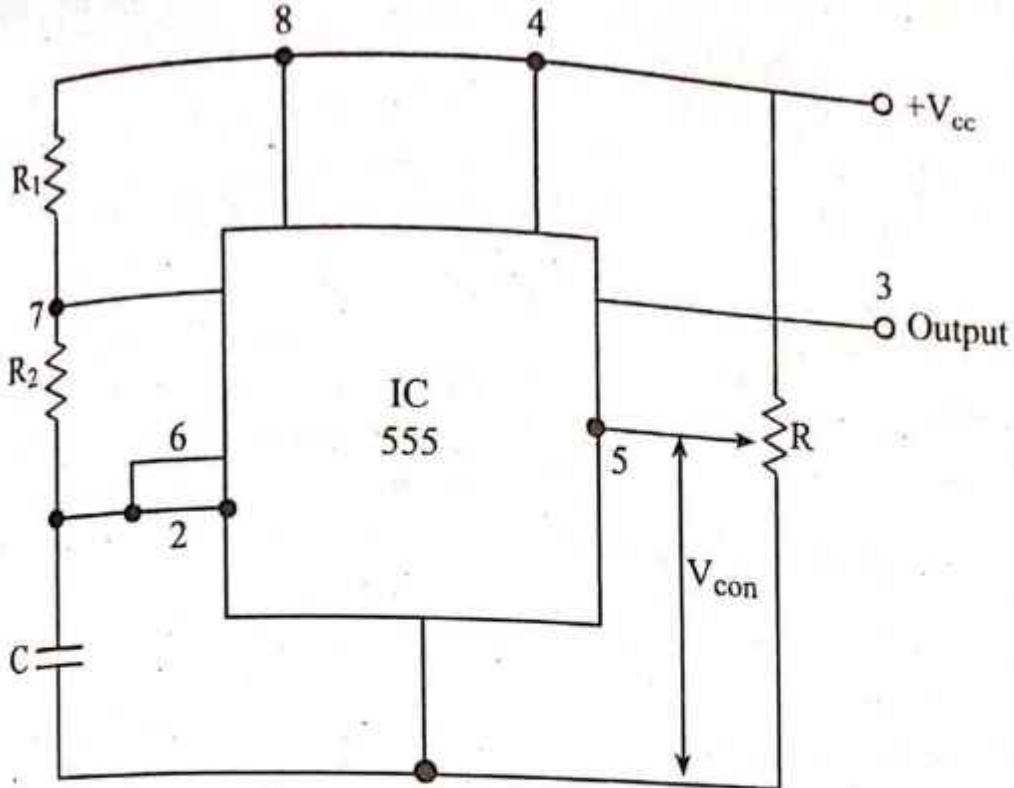
When  $2R_2 \gg R_1 \rightarrow$  then  $R_1 + 2R_2 \approx 2R_2$

$$\therefore T = 2R_2 C \ln 2$$

$$\therefore f = \frac{1}{T} = \frac{0.72}{R_2 C}$$

## # Voltage controlled oscillator using IC 555:

Voltage controlled oscillator is sometimes called a voltage to frequency converter because an input voltage can change the output frequency. By adjusting potentiometer, we can change control voltage  $V_{\text{con}}$ .



*Fig.5.5(c) Voltage controlled oscillator using IC 555:*

$V_C$  varies between  $\frac{V_{con}}{2}$  and  $+V_{con}$ . If we increase  $V_{con}$ , it takes capacitor longer to charge and discharge so frequency decreases. So we can change frequency of circuit by varying control voltage.

Let  $t_1$  and  $t_2$  be the time taken to charge & discharge capacitor 'C' respectively. Then

$$V_C(t_1) = V_{applied} - [V_{applied} - V_{C \text{ initial}}] e^{-t_1/(R_1 + R_2)C}$$

$$\& \quad V_C(t_2) = V_{applied} - [V_{applied} - V_{C \text{ initial}}] e^{-t_2/(R_1 + R_2)C}$$

$$\text{For charging, } V_{con} = V_{CC} - \left[ V_{CC} - \frac{V_{con}}{2} \right] e^{-t_2/(R_1 + R_2)C}$$

$$\text{or, } \frac{t_1}{(R_1 + R_2)C} = \ln \left( \frac{V_{CC} - 0.5V_{con}}{V_{CC} - V_{con}} \right)$$

$$\text{or, } t_1 = (R_1 + R_2)C \ln \left( \frac{V_{CC} - 0.5V_{con}}{V_{CC} - V_{con}} \right)$$

For discharging

$$\frac{V_{con}}{2} = 0 - [0 - V_{con}] e^{-t_2/R_2 C}$$

$$\Rightarrow t_2 = R_2 C \ln 2$$

$$\therefore \text{Total time period} = T = t_1 + t_2$$

$$= (R_1 + R_2)C \ln \left( \frac{V_{CC} - 0.5V_{con}}{V_{CC} - V_{con}} \right) + R_2 C \ln 2 \text{ and } f = \frac{1}{T}$$

### 5.6 Precision Rectifier Circuit

Precision rectifier circuit considered as a special class of wave shaping circuit used in design of instrumentation systems where the need arises for rectifier circuits with very precise transfer characteristics.

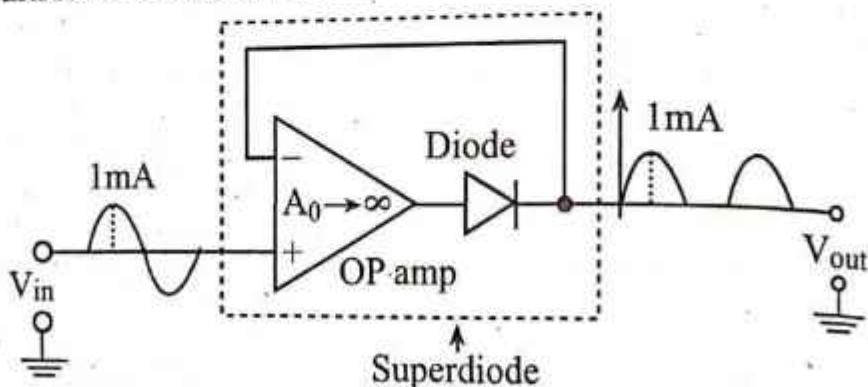
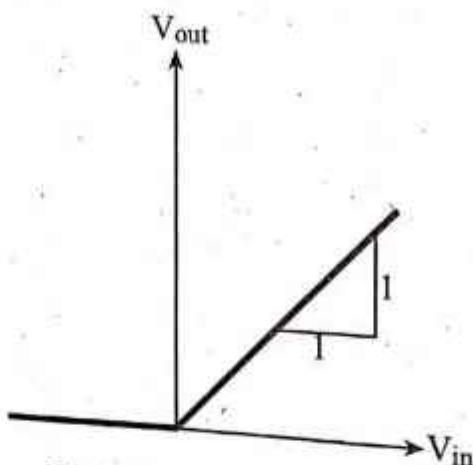


Fig.5.6 (a) Precision Rectifier Circuit



Ideal Transfer Characteristics

For positive input cycle output voltage of op-amp will go positive & the diode will conduct, thus establishing closed feedback path between the op-amp's output terminal & negative input terminal. This negative feedback path will cause a virtual short circuit to appear between the two input terminals of the op-amp.

$$V_{out} = V_{in} \text{ for } V_{in} \geq 0$$

Note that the offset voltage ( $\approx 0.5V$ ) exhibited in the simple half wave rectifier circuit is no longer present. For the op-amp circuit to start operation,  $V_{in}$  has to exceed only a negligibly small voltage equal to the diode drop divided by the op-amp's open-loop gain. This makes the circuit suitable for applications involving very small signals.

- "Configuration obtained with an op-amp in order to have a circuit behaving an ideal diode & rectifier."
- Used for high precision signal processing.
- Actual threshold of super diode is very close to zero  
$$= \frac{\text{actual threshold of diode}}{\text{gain of op-amp}}$$

### Tutorial 5

1. Describe "Barkhausen Criteria" for oscillation. Write down the general expression for the gain of a feedback amplifier, and state the condition of oscillation.
2. Draw a circuit diagram of RC sinusoidal oscillator and explain its working principle.
3. Explain the working principle of square wave generator circuit and determine its oscillation frequency.
4. Draw Wien Bridge Oscillator circuit and write the expression for frequency of oscillation.
5. Define oscillator. Explain how you can generate square wave using an op-amp. Design an oscillator for producing an output of 2 KHz frequency.
6. Draw and explain AMV circuit using IC 555 or BJT.
7. Define the term multivibrator. Explain the operation of op-amp based a stable multivibrator with the help of circuit diagram and waveform.
8. Write the applications of tuned LC oscillators. Draw the Colpitt's oscillator circuit and derive the expression for frequency of oscillation.
9. Draw the square wave generator circuit using op-amp.
10. Draw different types of LC oscillator circuits.

# POWER SUPPLIES, BREAKDOWN DIODES, AND VOLTAGE REGULATORS

## Introduction

Most electronic circuits require a direct voltage supply that is usually derived from the standard industrial or domestic ac supply by transformation, rectification, and filtering. The resultant raw dc is not sufficiently stable for most purposes, and it normally contains an unacceptably large ac ripple wave form. To render the voltage more constant, and to attenuate the ripple, voltage regulators must have stable reference voltage source which is provided by a special kind of diode operated in reverse breakdown called a breakdown diode, or Zener diode.

The regulator performance can be proved by the addition of an error amplifier to detect and amplify the difference between the output voltage and the voltage reference source. IC operational amplifiers make ideal error amplifiers. Complete voltage regulator circuits are available in integrated circuit form. Some of these ICs have a wide range of applications as different types of regulators. Other IC regulators are simply connected to a suitable supply to provide a fixed output voltage.

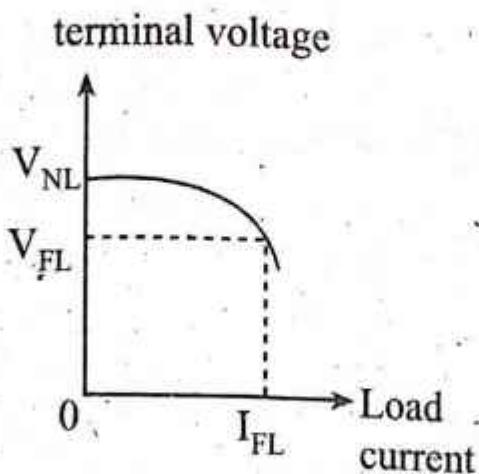
### 6.1 Unregulated Power Supply

The rectifier-filter combination constitutes an ordinary dc power supply whose dc output voltage remains constant so long as input ac mains voltage or load is unaltered. Such power supply is called unregulated power supply. Unregulated power supply has following drawbacks:

- i. The dc output voltage changes directly with input ac voltage.

- ii. The dc output voltage decreases as the load current increases (by decreasing load impedance), because there is greater voltage drop in power supply & hence smaller dc output voltage occurs.

## Voltage regulation



*Fig. 6.1(a) No load and Full load condition in Power Supply*

The voltage provided at the output under no-load condition (no current drawn from the supply) is reduced when load current is drawn from the supply (under full load condition). The amount the dc voltage changes between the no-load & full load condition is described by a factor called "voltage regulation", which is one measure of power supply performance & is expressed by;

$$\text{Voltage regulation} = \frac{\text{no-load voltage} - \text{full load voltage}}{\text{full load voltage}}$$

$$\% \text{ VR} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 \%$$

## DC Voltage Regulators:

### DC Voltage series regulator:

The block diagram of DC series regulator is shown below:

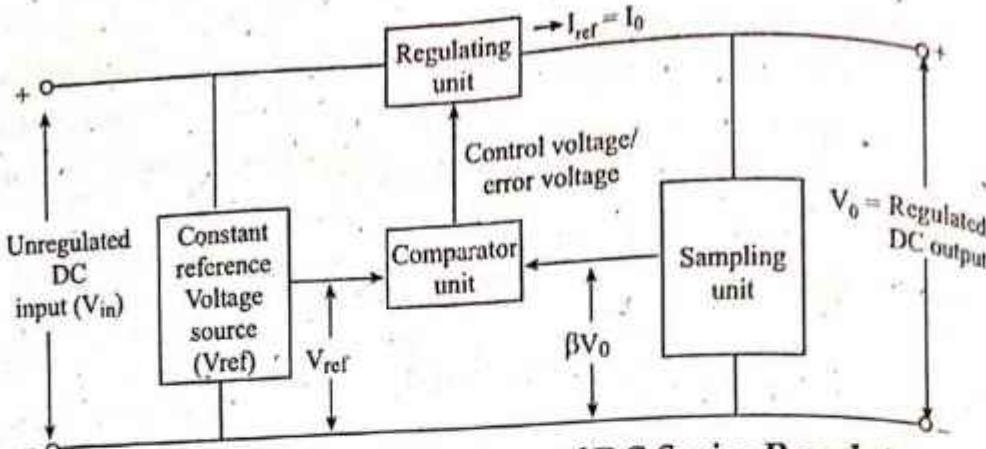


Fig.6.1(b) Block Diagram of DC Series Regulator

Here  $V_{in}$  is the unregulated power supply (such as obtained from rectifier with filter) and  $V_o$  is regulated output voltage. The series regulating element controls the amount of the input voltage that gets to the output. The output voltage is sampled by a circuit that provides a feedback voltage to be compared to a reference voltage ( $V_{ref}$ ).

- If the output voltage increases, the comparator circuit provides a control/error signal to cause the series control element to decrease the amount of the output voltage thereby maintaining the output voltage.
- If the output voltage decreases, the comparator circuit provides a control signal to cause the series control element (regulating unit) to increase the amount of the output voltage.

- **Series DC Voltage regulator using op-amp:**

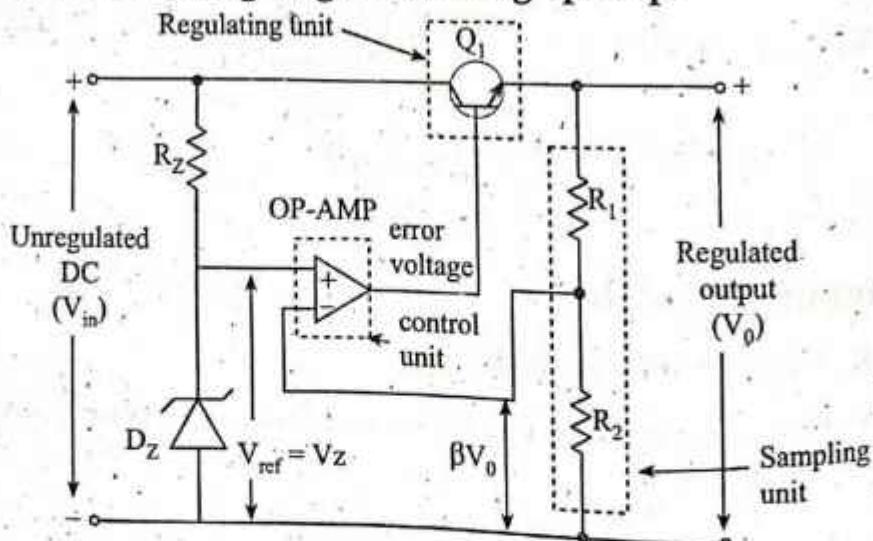


Fig.6.1(C) Series DCV Regulator using Op-amp

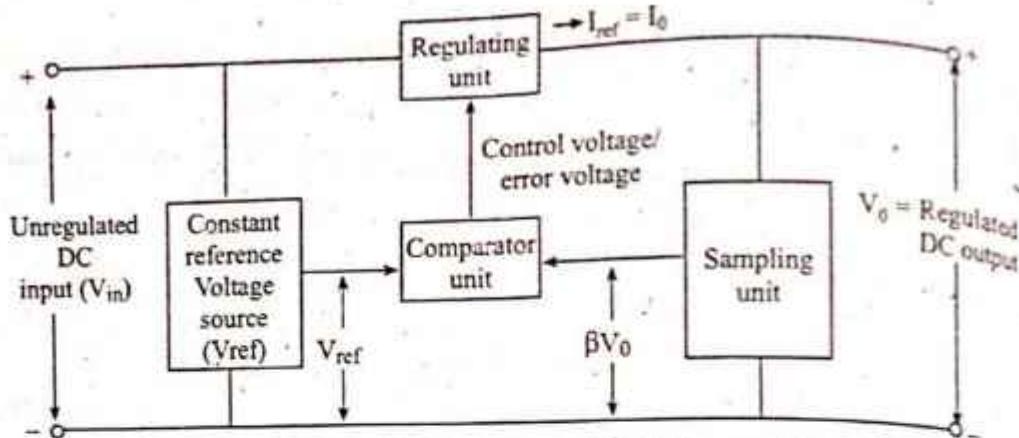


Fig.6.1(b) Block Diagram of DC Series Regulator

Here  $V_{in}$  is the unregulated power supply (such as obtained from rectifier with filter) and  $V_o$  is regulated output voltage. The series regulating element controls the amount of the input voltage that gets to the output. The output voltage is sampled by a circuit that provides a feedback voltage to be compared to a reference voltage ( $V_{ref}$ ).

- If the output voltage increases, the comparator circuit provides a control/error signal to cause the series control element to decrease the amount of the output voltage thereby maintaining the output voltage.
- If the output voltage decreases, the comparator circuit provides a control signal to cause the series control element (regulating unit) to increase the amount of the output voltage.

- **Series DC Voltage regulator using op-amp:**

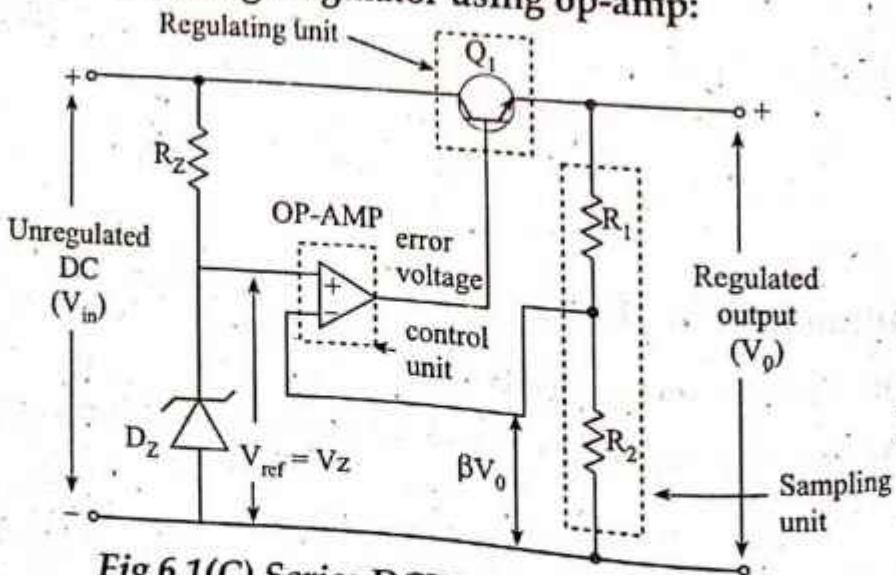


Fig.6.1(C) Series DCV Regulator using Op-amp

Potentiometer  $R_1 - R_2$  senses any change in output voltage  $V_o$ . When,  $V_o$  decreases  $\beta V_o$  applied to inverting input of op-amp tends to decrease.

So, small difference in input (error voltage) developed which is amplified & output of op-amp increases.

Here op-amp compares the zener diode reference voltage with the feedback voltage from sensing resistors  $R_1$  and  $R_2$ . If the output voltage varies, the conduction of transistor  $Q_1$  is controlled to maintain the output voltage constant.

For zero error voltage i.e. constant output;

Input voltage to the op-amp:

$$V_d = V^+ - V^- = 0$$

$$\text{or, } V_Z - \beta V_o = 0$$

$$\text{or, } V_o = \frac{1}{\beta} V_Z = \left( \frac{R_2 + R_1}{R_2} \right) V_Z$$

$$\therefore V_o = V_Z \frac{(R_2 + R_1)}{R_2} \Rightarrow \text{Regulated output voltage}$$

#### ♦ Series DC Voltage Regulator using Discrete Components:

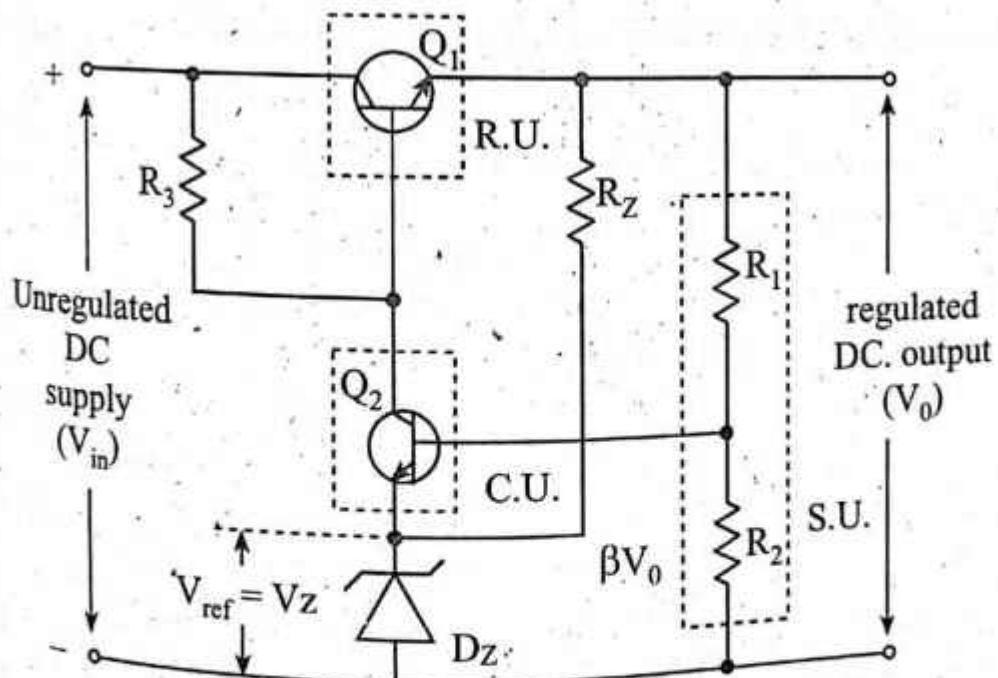


Fig. 6.1(d) Series DCV Regulator using Discrete Components

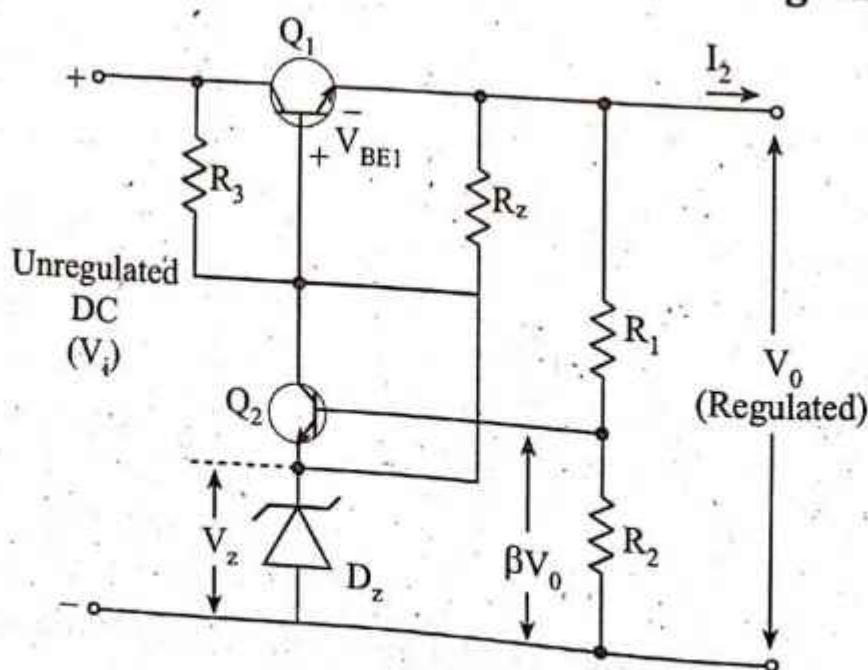
$$\beta = \frac{R_2}{R_1 + R_2} = \text{voltage feedback ratio}$$

The unregulated dc supply is fed to the voltage regulator. The circuit maintains constant output voltage irrespective of the variations in load or input voltage.

- (i) Suppose the output voltage increases due to any reason. This causes an increase in voltage across  $R_2$  as it is a part of the output circuit. This in turn means that more  $\beta V_o$  is fed back to the base of transistor  $Q_2$ ; producing larger collector current of  $Q_2$ . Most of this collector current flows through  $R_3$  and causes the base voltage of  $Q_1$  to decrease. This results in less output voltage i.e. increase in voltage is offset. Thus output voltage remains constant.
- (ii) Similarly, if output voltage tries to decrease, the feedback voltage  $\beta V_o$  also decreases. This reduces the current through  $Q_2$  &  $R_3$ . This means more base voltage at  $Q_1$  and more output voltage.

Consequently, the output voltage remains at the original level.

### Estimation of stability factor ( $S_V$ ) for the DC regulator:



The voltage gain of common emitter type transistor amplifier of  $Q_2$  is expressed as;

$$A_v = \frac{\text{total resistance in collector section}}{\text{total resistance in emitter section}} = \frac{R_3}{r_e + r_z}$$

Where,

$$r_e \approx \frac{1}{g_m} = \frac{V_T}{I_{E2}} = \text{emitter dynamic resistance}$$

$r_z$  = dynamic resistance of zener diode

Input unregulated voltage;  $V_i = V_{R3} + V_o + V_{BE1}$

Let  $V_i = \Delta V_i$ ,  $V_o = \Delta V_o$  be small changes in dc voltages. We assume  $\Delta V_o = V_o = \text{very small}$  & can be ignored with respect to  $V_{R3}$ . Because by definition and by our requirement  $\Delta V_o$  should be zero for constant dc output voltage. Taking ac quantities only,

$$v_i = V_{R3} + v_{be1} + v_o \approx V_{R3} \quad [v_{be1} \text{ and } v_o \text{ very small}]$$

The output of the transistor  $Q_2$

$$v_{R3} = A_v \times (\text{input to the base of } Q_2)$$

$$= A_v \cdot (\beta \cdot V_o) = \frac{R_3}{r_e + r_z} \times \beta V_o$$

$$\approx v_i$$

The stability factor of the regulator may be expressed as,

$$S_v = \frac{\Delta V_o}{\Delta V_i} \times 100\%$$

$$= \frac{V_o}{V_i} \times 100\%$$

$$= \frac{V_o}{\left( \frac{R_3}{r_e + r_z} \right) \beta V_o} \times 100\%$$

$$= \frac{r_e + r_z}{R_3} \cdot \frac{R_1 + R_2}{R_2} \times 100\%$$

$$\text{Thus, } S_v = \frac{r_e + r_z}{R_3} \cdot \frac{R_1 + R_2}{R_2} \times 100 \approx 1.5\%$$

Best case:  $S_v = 0$

Worst case:  $S_v = 1$

## 6.2 Band Gap Voltage Reference, a Constant Current Diodes

- i. Fixed dc reference voltage that does not change with temperature
- ii. Temperature independent voltage reference circuit widely used in IC circuits.

It is popular voltage reference method, also called as  $V_{BE}$  reference because it actually compensates negative temperature coefficient (NTC) characteristics of PN junction of  $V_{BE}$  with its PTC characteristics (thermal voltage)  $V_T$ , that means it involves generation of a voltage with PTC which is same as  $V_{BE}$  NTC. When added they yield zero temperature coefficient.

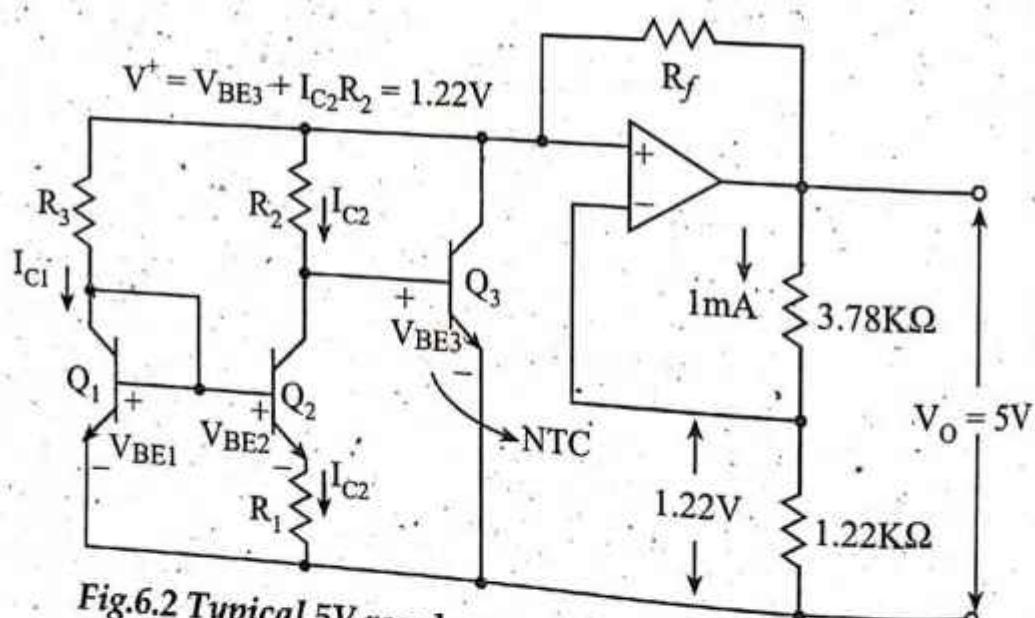


Fig.6.2 Typical 5V regulator circuit using Bandgap reference

From figure, transistor  $Q_1$  and  $Q_2$  form a typical Widlar current source

Where;

$$I_{C2} R_1 = V_{BE1} - V_{BE2}$$

$$\& \quad I_{C1} = I_s e^{\frac{V_{BE1}}{V_T}}$$

$$I_{C2} = I_s e^{\frac{V_{BE2}}{V_T}}$$

$$\text{So, } \frac{I_{C1}}{I_{C2}} = \frac{e^{\frac{V_{BE1}}{V_T}}}{e^{\frac{V_{BE2}}{V_T}}} = e^{\frac{V_{BE1} - V_{BE2}}{V_T}}$$

Taking 'ln' on both sides,

$$\text{or, } \frac{V_{BE1} - V_{BE2}}{V_T} = \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

$$\text{or, } V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

$$\therefore R_1 I_{C2} = V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right)$$

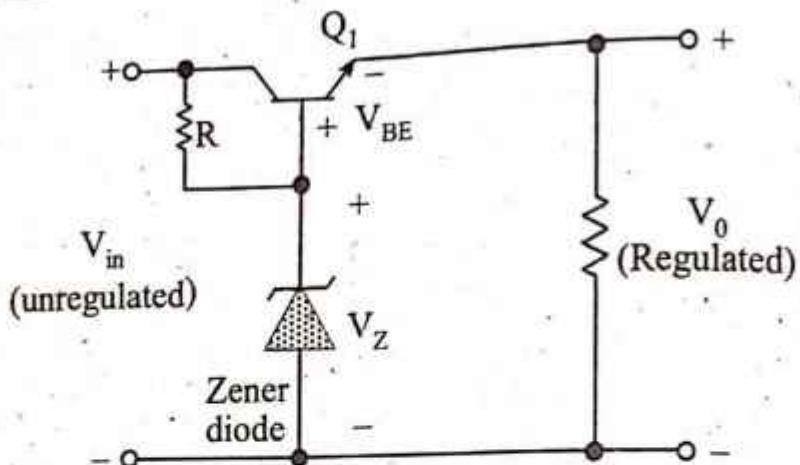
This current  $I_{C2}$  produces  $R_2 I_{C2}$  voltage across  $R_2$ . This voltage has PTC characteristics and  $V_{BE3}$  of  $Q_3$  has NTC characteristics. If we add these two voltages as shown in fig so that PTC of  $R_2 I_{C2}$  is equal to NTC of  $V_{BE3}$ ; then the whole circuit behaves as zero TC.

To make PTC of voltage across  $R_2$  equal to NTC of  $V_{BE3}$ , the current densities  $\left[ \ln\left(\frac{I_{C1}}{I_{C2}}\right) \right]$  of  $Q_1$  and  $Q_2$  are chosen approx as 10:1.  $R_2$  also sets magnitude of PTC which is added to  $V_{BE3}$ . And by choosing them approx, we get dc voltage with zero TC. Normally zero TC occurs when the total voltage equals the silicon band-gap voltage of about 1.22 V dc.

Thus the circuit above has  $V^+ = I_{C2} R_2 + V_{BE3}$   
 $\approx 1.22 \text{ V dc}$

With the values shown is above, circuit provides the regulated output dc voltage +5V, which is also temperature compensated.

### 6.3 Transistor Series Regulator



*Fig.6.3 Transistor Series Regulator*

This is a transistor series voltage regulator because the load current passes through the series transistor  $Q_1$ . Here the transistor behaves like variable resistor determined by base current & the zener diode provides reference voltage.

#### Operation

The base voltage of transistor  $Q_1$  is held to a relatively constant voltage across the zener diode in breakdown region.

Applying KVL we get

$$V_Z = V_{BE} + V_o \Rightarrow V_{BE} = V_Z - V_o \dots\dots\dots (1)$$

Here  $V_Z$  is considered constant for breakdown operation so any change in  $V_o$  causes the change in  $V_{BE}$ . Suppose  $R_L$  decreases and current demand increases,  $V_o$  tends to decrease. This decrease in  $V_o$  increases  $V_{BE}$  (by equation (1)). Increase in  $V_{BE}$  means the transistor gets more forward biased thus resulting decrease in collector-emitter resistance and increasing load current. Thus  $V_o = I_L R_L$  will remain almost constant.

The increase in  $V_o$  similarly causes the opposite effects hence finally stabilizing the output voltage.

#### Limitations

- No provision to vary output voltage

- Output will be affected by temperature variation
- Regulator will perform only when zener diode is in breakdown region.

#### 6.4 Improving Regulator Performance

By incorporating an additional transistor we can improve performance of such regulator because it increases the gain. Here,  $R_1$  and  $R_2$  act as the voltage divider. Assuming, zener diode current doesn't load it appreciably.

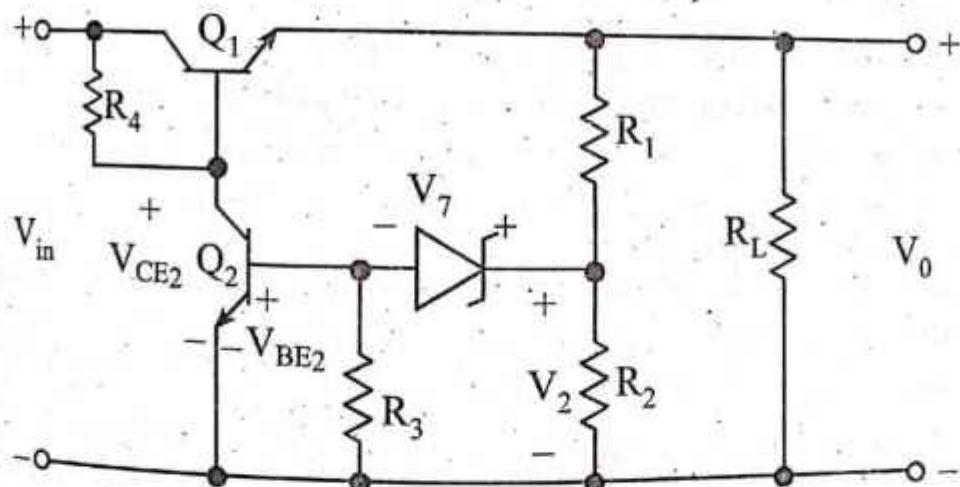
$$V_2 = \frac{R_2}{R_1 + R_2} V_o \quad \dots \dots \dots (2)$$

By Kirchhoff's voltage law,

$$V_{BE2} + V_Z = V_2$$

$$\therefore V_{BE2} = V_2 - V_Z \quad \dots \dots \dots (3)$$

Here any decrease in  $V_o$  causes decrease in  $V_2$  and hence in  $V_{BE2}$ . Decrease in  $V_{BE2}$  results increase in  $V_{BE1}$ , which results  $Q_1$  to conduct more heavily, hence increasing  $I_L$  & thus ( $V_o = I_L R_L$ ) output voltage becomes almost constant.



*Fig.6.4 An Improved Transistor Series Regulator*

Similarly, any increase in  $V_o$  causes just opposite events & hence maintain constant output voltage.

$$V_2 = \frac{R_2}{R_1 + R_2} V_o \Rightarrow V_o = \frac{R_1 + R_2}{R_2} V_2 = \frac{R_1 + R_2}{R_2} (V_Z + V_{BE2})$$

## 6.5 Current Limiting

Current Limiting Circuit: (Short Circuit/Overload Protection Circuit)

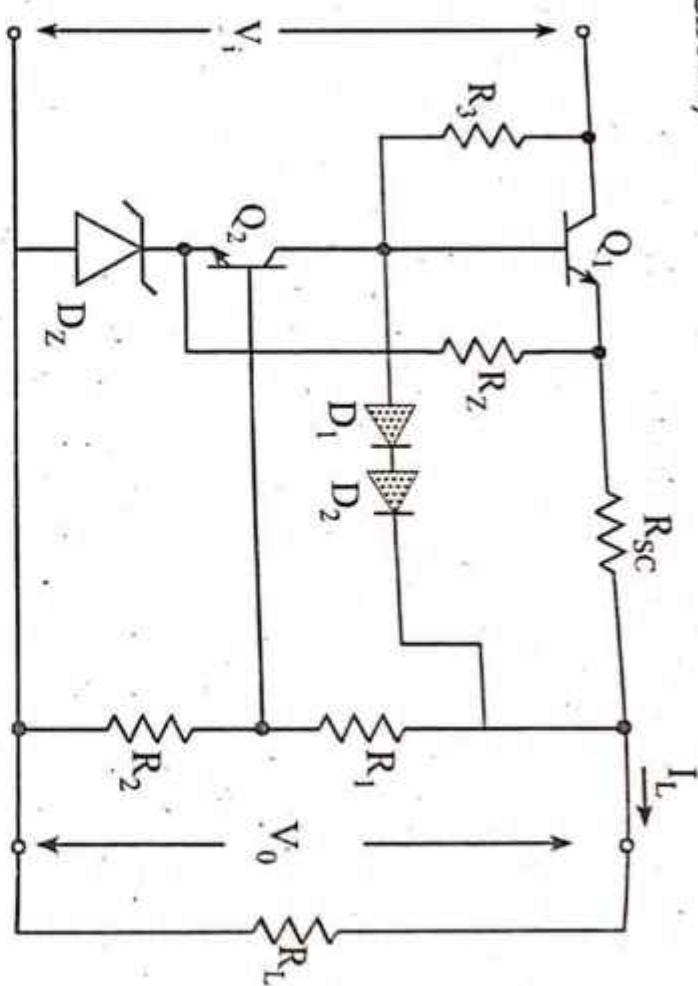


Fig.6.5 (a) Current Limiting Circuit using Diodes

The above circuit uses a current limiting circuit to provide protection in case of overload or short circuit in a series regulator. As we know the main drawback of any series regulator is that the pass transistor ( $Q_1$ ) can be destroyed by excessive load current if the load is accidentally shorted. Here a current limiting circuit consists of two diodes ( $D_1$  and  $D_2$ ) and a series resistor  $R_{SC}$ .

Here the diodes  $D_1$  and  $D_2$  are non-conducting until voltage drop across  $R_{SC}$  exceeds their forward threshold voltage, i.e. when  $V_{RSC} = 0.7V$ , diodes  $D_1$  and  $D_2$  conduct by passing the current through  $R_3$  thereby decreasing the base voltage of  $Q_1$ . The decrease in base voltage of  $Q_1$  reduces the conduction of  $Q_1$ , finally preventing any further increase in load current.

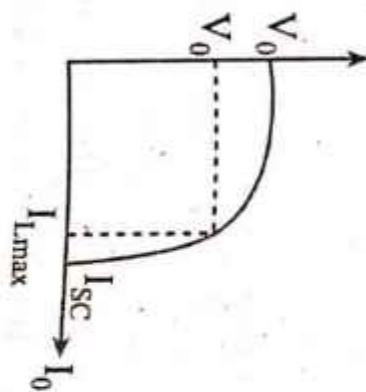
Here,

$$V_{D1} + V_{D2} = V_{BE1} + V_{RSC}$$

$$\text{or, } V_{RSC} = V_{D1} + V_{D2} - V_{BE1}$$

$$\text{or, } I_s R_{SC} = V_{D1} + V_{D2} - V_{BE1}$$

$$I_S = \frac{V_{D1} + V_{D2} - V_{BE1}}{R_{SC}} \dots\dots (1)$$

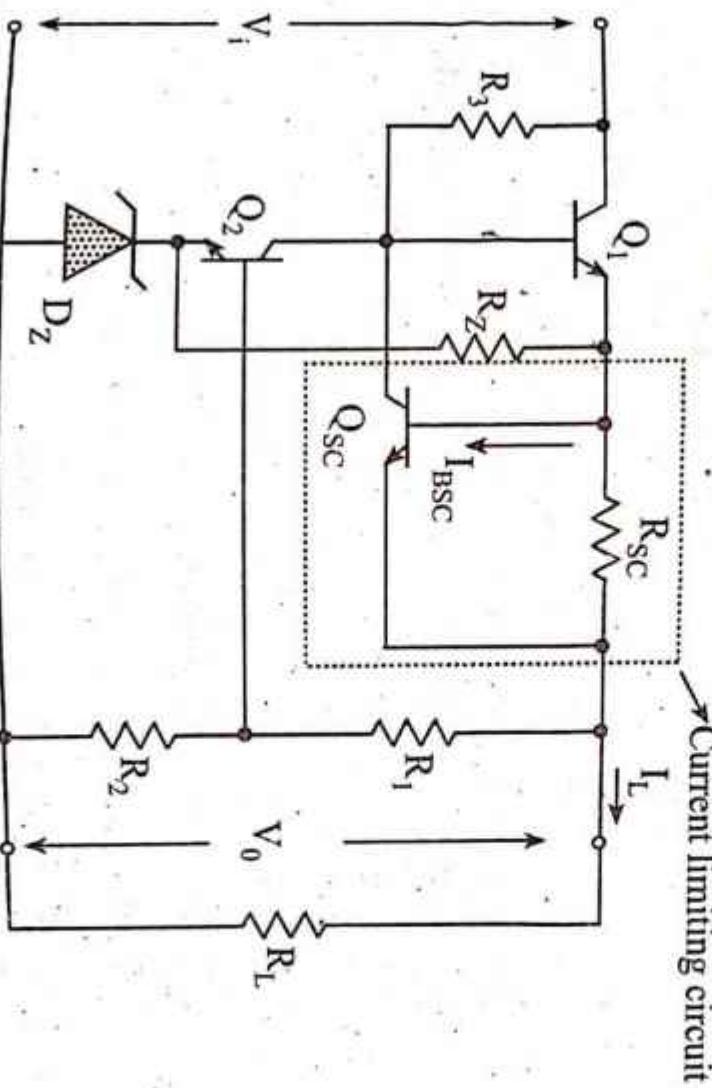


*Fig 6.5 (b) Voltage-Current Relationship of Voltage Regulator*

At limiting point;

$$0.7V = I_{L\max} \cdot R_{SC} = V_{RSC}$$

#### \* Current Limiting Circuit using Transistor



*Fig 6.5 (c) Protection Circuit using Transistor*

Here a current limiting circuit consists of a transistor  $Q_{SC}$  and a series resistor  $R_{SC}$  that is connected between base & emitter terminals of  $Q_{SC}$ .

#### Operation

When the load current is normal, the voltage across  $R_{SC}$  (i.e. voltage across base emitter of  $Q_{SC}$ ) is small and  $Q_{SC}$  is off.

Under this, circuit works as simple series regulator as discussed.

If the load current becomes excessive (due to short circuit or overload), the voltage across  $R_{SC}$  becomes large enough to turn on  $Q_{SC}$ . The collector current of  $Q_{SC}$  flows through  $R_L$ , thereby decreasing the base voltage of  $Q_L$ . The decrease in base voltage of  $Q_L$  reduces the conduction of pass transistor  $Q_L$ , preventing any further increase in load current.

When  $Q_{SC}$  turned on, it diverts current from the base of transistor  $Q_L$ , thereby reducing load current through  $Q_L$ , preventing any additional current to load  $R_L$ . The action of components  $R_{SC}$  and  $Q_{SC}$  provides limiting of the maximum load current.

## 6.6 Integrated Circuit Voltage Regulator

We can use integrated circuits (IC) to produce voltage regulators. One advantage of IC voltage regulators is that properties like thermal compensation, short circuit protection & surge protection can be built into the device. Most of the commonly used IC voltage regulators are 3-terminal devices.

**Types:**

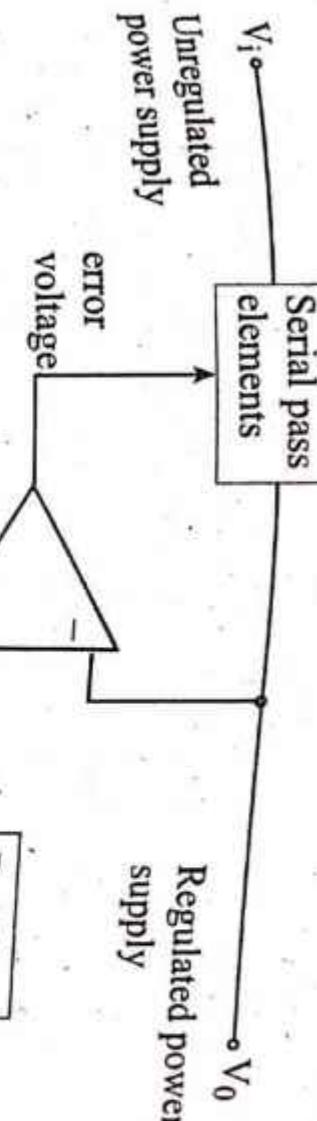
- a) Fixed IC voltage regulator
- b) Variable IC voltage regulator

### a) Fixed IC voltage regulator

Fixed IC voltage regulator can provide either fixed positive output voltage or fixed negative IC voltage depending on their IC type. The 78XX series of IC regulator is most popular for fixed positive output voltage and the 79XX series of IC regulators is for fixed negative output voltage.

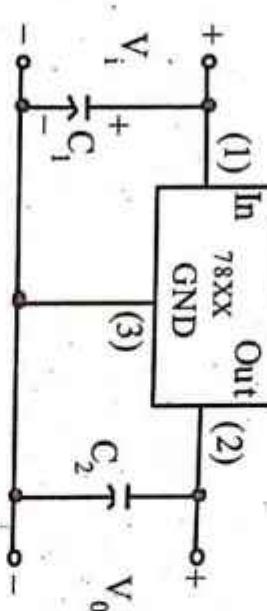
Ex:  $\{7815 \rightarrow +15V$  (output voltage); Fixed positive IC voltage regulator.  
 $7915 \rightarrow -15V$  (output voltage); Fixed Negative IC voltage regulator

Thermal short down  
current limiting

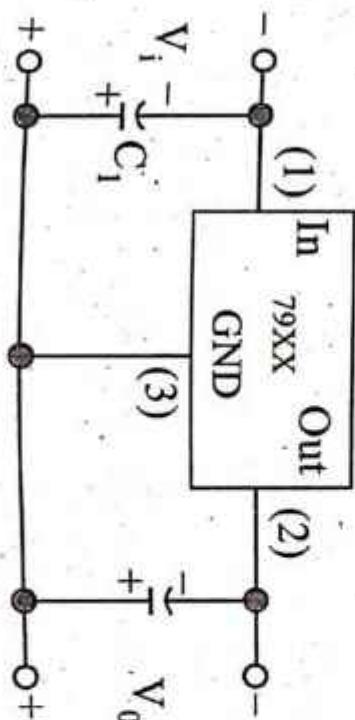


*Fig.6.6 (a) Block Diagram of Fixed IC Voltage Regulator*

IC regulator with 3 pin



*Fig.6.6 (b) Connection of fixed positive IC voltage regulator*



*Fig.6.6(c) Connection of fixed negative IC voltage regulator.*

### b) Variable IC voltage regulator: (Adjustable type)

The adjustable voltage regulator can be adjusted to provide any dc output voltage that is within its two specified limits. The LM317, which has 3 terminals, can be operated with the output voltage regulated at any setting over the range of voltage from 1.2 V to 37 V. An external voltage divider is used to change the dc output

voltage of the regulator. By changing  $R_2$ , a wide range of output voltage can be obtained.

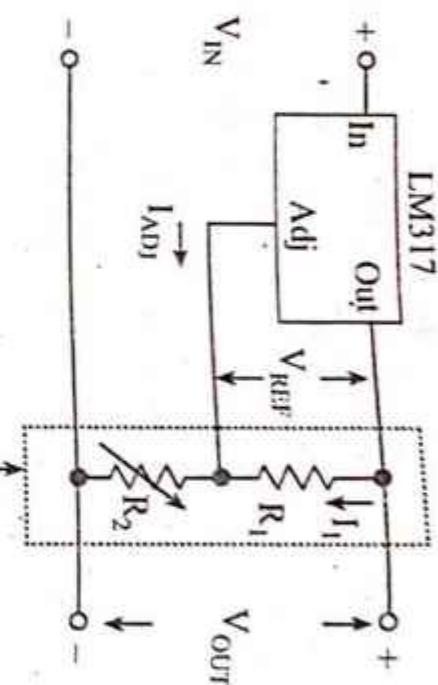


Fig 6.6(d) Connection of LM317 adjustable Voltage Regulator

The desired output voltage

$$\begin{aligned} V_o &= I_1 R_1 + (I_1 + I_{\text{Adj}}) R_2 \\ &= V_{\text{REF}} + \left( \frac{V_{\text{REF}}}{R_1} + I_{\text{Adj}} \right) R_2 \\ \therefore V_o &= V_{\text{REF}} \left( 1 + \frac{R_2}{R_1} \right) + I_{\text{Adj}} R_2 \end{aligned}$$

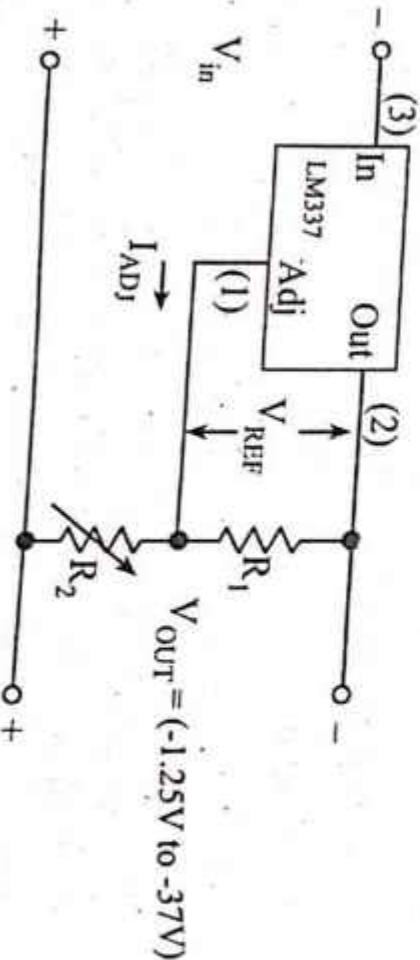
With typical IC value;

$$V_{\text{REF}} = 1.25V \text{ & } I_{\text{Adj}} = 100 \mu\text{A}$$

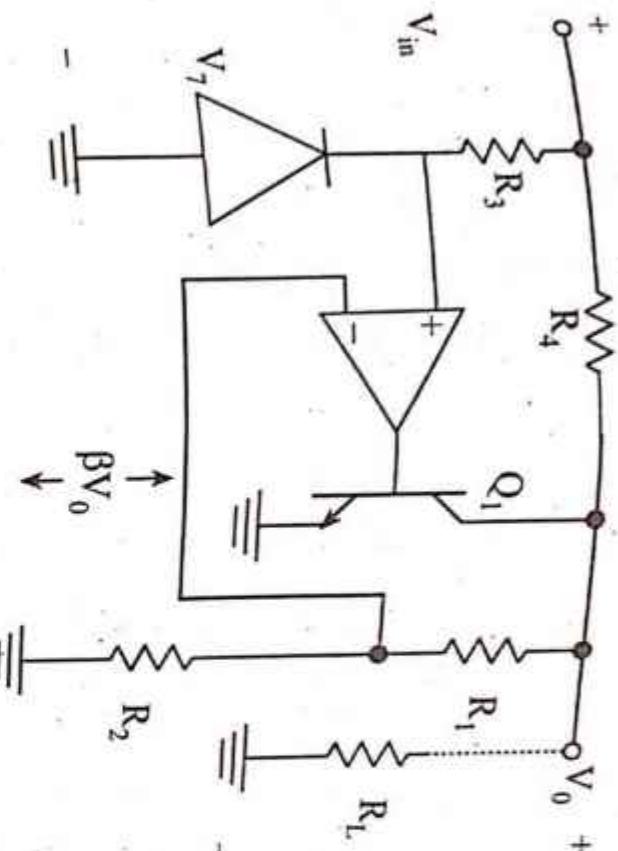
$$\therefore V_o \approx V_{\text{REF}} \left( 1 + \frac{R_2}{R_1} \right) = 1.25 \left( 1 + \frac{R_2}{R_1} \right)$$

For variable negative IC

Voltage regulator use LM337 as;



## Shunt voltage regulator using op-amp



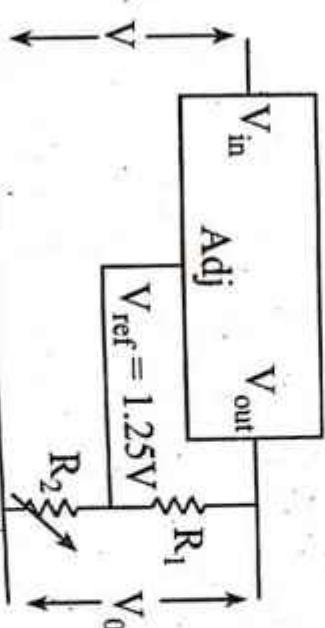
Here, when  $V_o$  increases, output of op-amp also increases then  $Q_1$  conducts more, thus more current is diverted from load & output voltage decreases to maintain constant.

*Main advantage: it has inherent current limiting.*

- Q. Design a 4.2V to 12V variable dc voltage regulator using IC LM317.

Solution:

LM317.



Here,

$$V_{\text{omin}} = 4.2 \text{ V}$$

$$V_{\text{omin}} = V_{\text{ref}} \left( 1 + \frac{R_2}{R_1} \right) = 1.25 \left( 1 + \frac{R_2}{R_1} \right)$$

$$\therefore 4.2 = 1.25 \left( 1 + \frac{R_{2\text{min}}}{R_1} \right)$$

$$4.2 = 1.25 \left( 1 + \frac{R_{2\text{min}}}{R_1} \right)$$

$$\frac{R_{2\min}}{R_1} = 2.36$$

$$R_{2\min} = 2.36 R_1$$

Also,

$$V_{\text{onax}} = 12V$$

$$V_{\text{onax}} = 1.25 \left( 1 + \frac{R_{2\max}}{R_1} \right)$$

$$R_{2\max} = 8.6 R_1$$

$$R_{2\min} = 2.36 K\Omega$$

$$R_{2\max} = 8.6 K\Omega$$

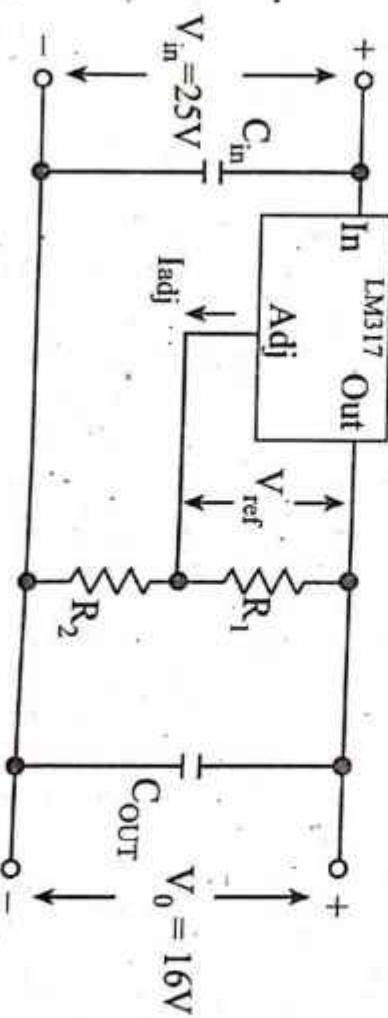
$$\therefore 2.36 K\Omega \leq R_2 \leq 8.6 K\Omega$$

- Q. Design a regulator circuit to obtain 16 V DC. Choose approximate values of the parameters. Input voltage is 25 V DC.

[062 Bhadra Regular, 064 Poush Regular, 071 Shawan Back]

*Solution:*

Using LM317 IC circuit to obtain 16 V DC.



We know,

$$V_o = V_{\text{ref}} \left( 1 + \frac{R_2}{R_1} \right)$$

$$\text{or, } \frac{R_2}{R_1} = \left( \frac{V_o}{V_{\text{ref}}} - 1 \right)$$

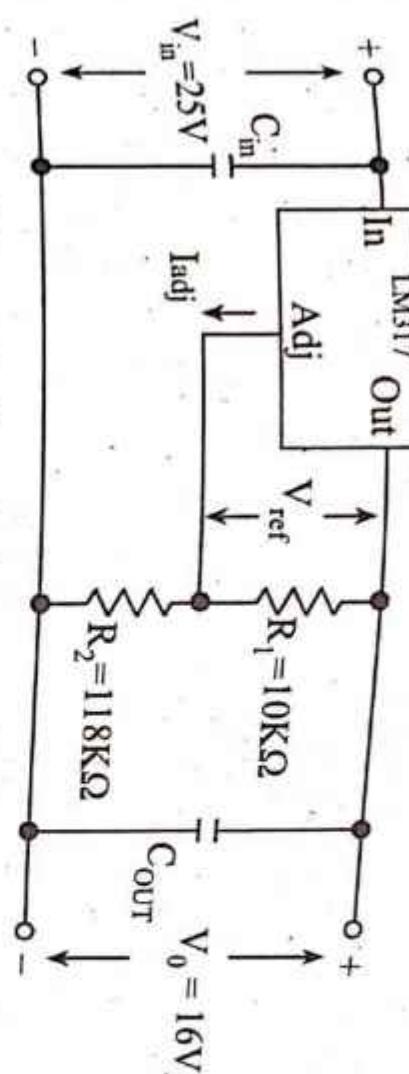
Assume  $V_{\text{ref}} = 1.25 V$

$$\text{or, } R_2 = R_1 \left( \frac{16}{1.25} - 1 \right)$$

or,  $R_2 = 11.8R_1$

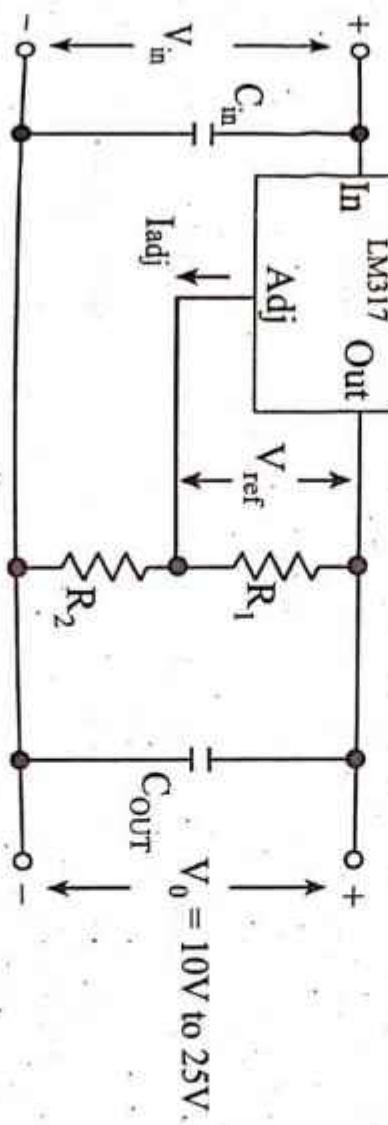
Taking  $R_1 = 10 \text{ k}\Omega$  then,

$$R_2 = 118 \text{ k}\Omega$$



Q. Design a (10 - 25) V variable dc series voltage regulator using LM317 IC. [070 Chaitra Regular]

**Solution:**



We know,

$$V_o = V_{\text{ref}} \left( 1 + \frac{R_2}{R_1} \right)$$

Here,

$$\underline{V_{o\text{min}} = 10 \text{ V}}$$

$$V_{\text{o}\text{min}} = V_{\text{ref}} \left( 1 + \frac{R_{2\text{min}}}{R_1} \right) = 1.25 \left( 1 + \frac{R_{2\text{min}}}{R_1} \right)$$

or,  $R_{2\text{min}} = 7R_1$

Also,

$$\underline{V_{o\text{max}} = 25 \text{ V}}$$

$$V_{\text{omax}} = 1.25 \left( 1 + \frac{R_{2\text{max}}}{R_1} \right)$$

$$R_{2\text{max}} = 19 R_1$$

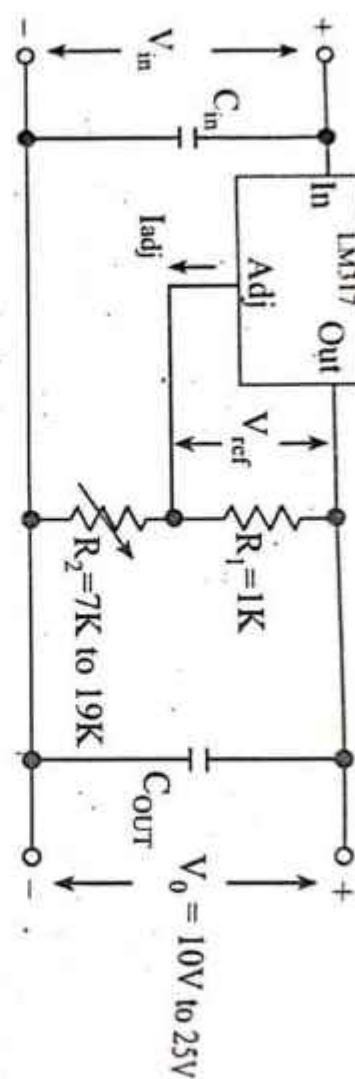
Let  $R_1 = 1 \text{ k}\Omega$  then

$$R_{2\text{min}} = 7 \text{ k}\Omega \text{ and}$$

$$R_{2\text{max}} = 19 \text{ k}\Omega.$$

$$\therefore 7 \text{ k}\Omega \leq R_2 \leq 19 \text{ k}\Omega$$

$$7R_1 \leq R_2 \leq 19R_1$$

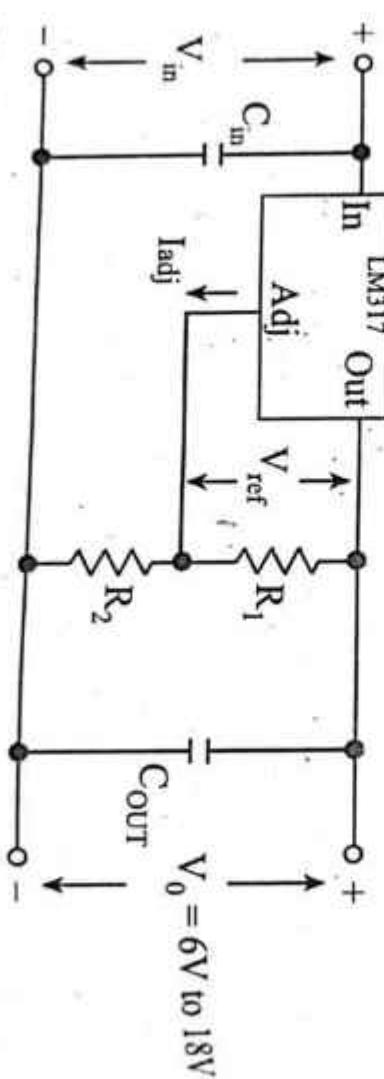


Q. Design a dc voltage regulator for  $V_o = 6 \text{ V}$  to  $18 \text{ V}$ .

[071 Chaitra Regular]

**Solution:**

Using LM317 IC circuit to obtain output voltage 6 V to 18 V.



We know,

$$V_o = V_{\text{ref}} \left( 1 + \frac{R_2}{R_1} \right)$$

$$\text{Assume } V_{\text{ref}} = 1.25 \text{ V}$$

Here,

$$V_{\text{omin}} = 6 \text{ V}$$

$$V_{\text{omin}} = V_{\text{ref}} \left( 1 + \frac{R_{2\text{min}}}{R_1} \right) = 1.25 \left( 1 + \frac{R_{2\text{min}}}{R_1} \right)$$

or,  $R_{2\text{min}} = 3.8R_1$

Also,

$$\underline{V_{\text{omax}} = 18 \text{ V}}$$

$$V_{\text{omax}} = 1.25 \left( 1 + \frac{R_{2\text{max}}}{R_1} \right)$$

$$R_{2\text{max}} = 13.4 R_1$$

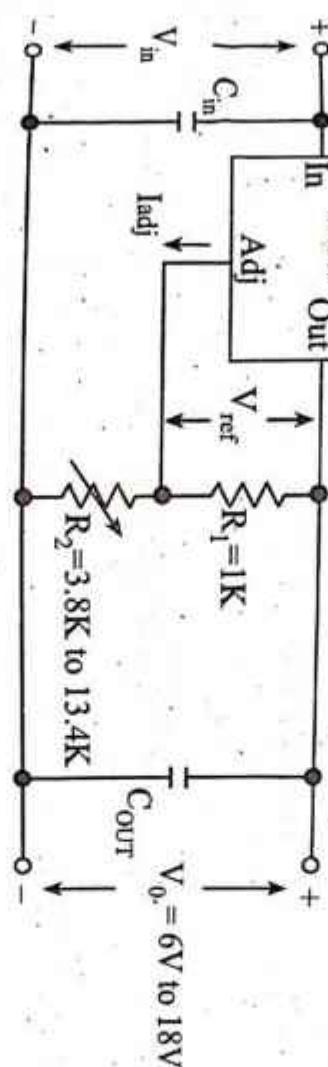
Let  $R_1 = 1 \text{ k}\Omega$  then

$R_{2\text{min}} = 3.8 \text{ k}\Omega$  and

$$R_{2\text{max}} = 13.4 \text{ k}\Omega.$$

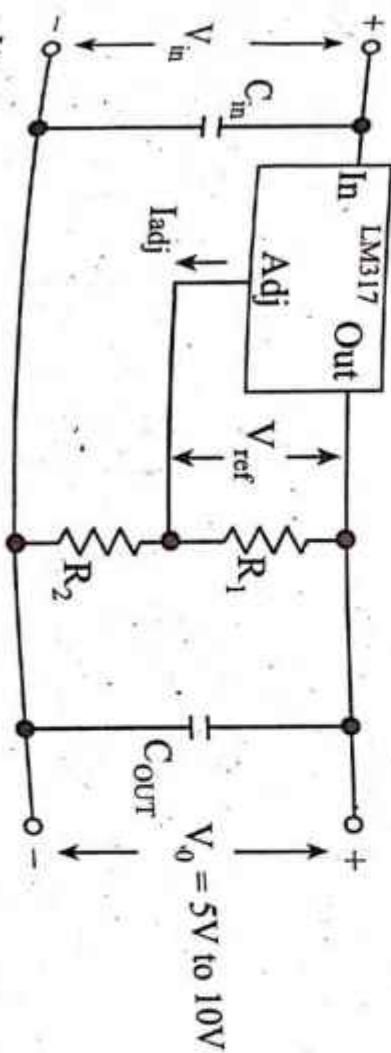
$$\therefore 3.8 \text{ k}\Omega \leq R_2 \leq 13.4 \text{ k}\Omega$$

$$3.8R_1 \leq R_2 \leq 13.4R_1$$



Q. Design a (5 - 10) V variable dc voltage regulator using LM317 IC.

Solution:



We know,

$$V_o = V_{\text{ref}} \left( 1 + \frac{R_2}{R_1} \right)$$

Assume  $V_{ref} = 1.25$  V

Here,

$$\underline{V_{omin}} = 5\text{ V}$$

$$V_{omin} = V_{ref} \left( 1 + \frac{R_{2min}}{R_1} \right) = 1.25 \left( 1 + \frac{R_{2min}}{R_1} \right)$$

or,  $R_{2min} = 3R_1$

Also,

$$\underline{V_{omax}} = 10\text{ V}$$

$$V_{omax} = 1.25 \left( 1 + \frac{R_{2max}}{R_1} \right)$$

$$R_{2max} = 7R_1$$

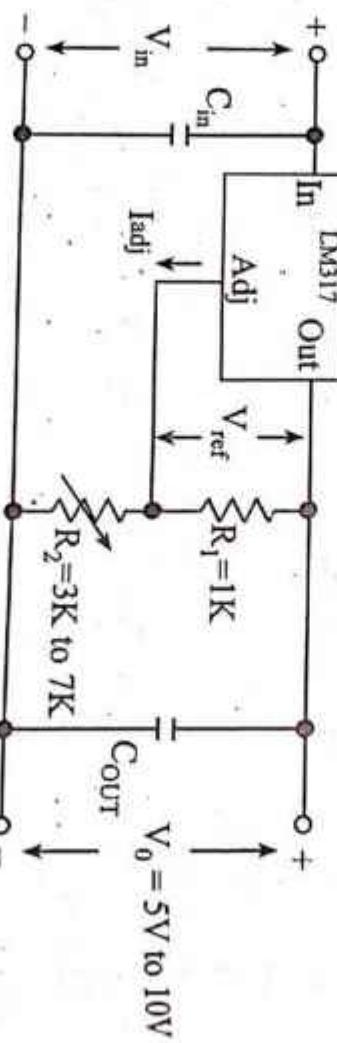
Let  $R_1 = 1\text{ k}\Omega$  then

$R_{2min} = 3\text{ k}\Omega$  and

$R_{2max} = 7\text{ k}\Omega$ .

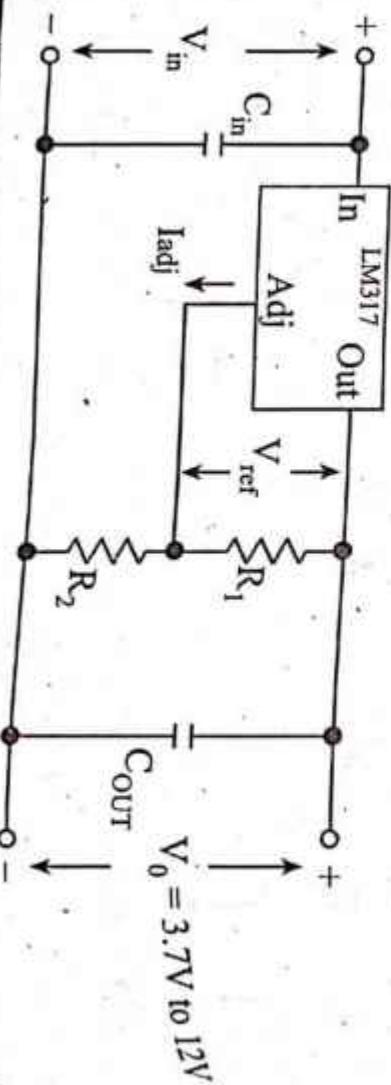
$$\therefore 3\text{ k}\Omega \leq R_2 \leq 7\text{ k}\Omega$$

$$3R_1 \leq R_2 \leq 7R_1$$



Q. Design a DCV regulator for 3.7 V to 12 V output using LM317.

Solution:



We know,

$$V_o = V_{ref} \left( 1 + \frac{R_2}{R_1} \right)$$

Assume  $V_{ref} = 1.25$  V

Here,

$$\underline{V_{omin} = 3.7\text{ V}}$$

$$V_{omin} = V_{ref} \left( 1 + \frac{R_{2min}}{R_1} \right) = 1.25 \left( 1 + \frac{R_{2min}}{R_1} \right)$$

or,  $R_{2min} = 1.96R_1$

Also,

$$\underline{V_{omax} = 12\text{ V}}$$

$$V_{omax} = 1.25 \left( 1 + \frac{R_{2max}}{R_1} \right)$$

$R_{2max} = 8.6R_1$

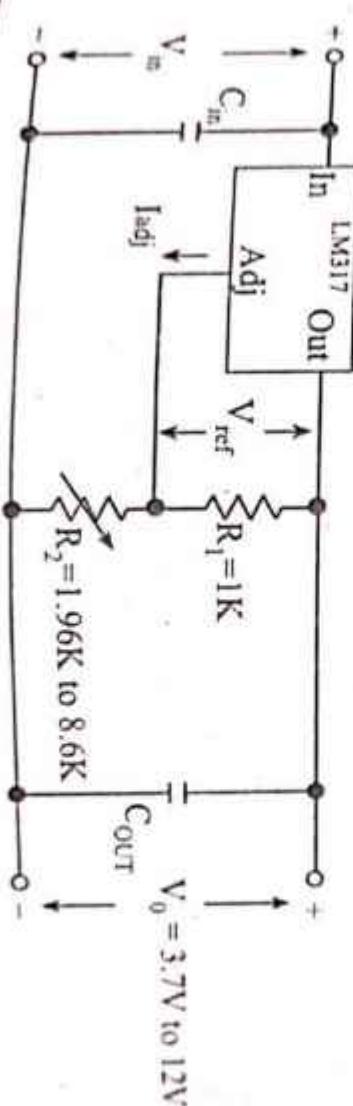
Let  $R_1 = 1\text{ k}\Omega$  then

$R_{2min} = 1.96\text{ k}\Omega$  and

$R_{2max} = 8.6\text{ k}\Omega$ .

$$\therefore 1.96\text{ k}\Omega \leq R_2 \leq 8.6\text{ k}\Omega$$

$$1.96R_1 \leq R_2 \leq 8.6R_1$$



### Tutorial 6

- Define loading effect in unregulated power supply. Draw a series transistor zener diode voltage regulator, and state how this problem is taken care of by this circuit.
- Define the regulated power supply. Determine the voltage stability (input regulation) factor of variable series voltage regulator circuit with transistor Q2 as error amplifier circuit.

3. Draw series voltage regulator with current limiting circuit and explain how this protection circuit works?
4. Design a regulator circuit to obtain 16 VDC with input voltage of 25 VDC.
5. Why a full wave rectifier followed with a capacitive filter cannot be used as a reliable DC source? How can a zener diode be used to improve the performance of this circuit? What are the limitations of the resulting circuit? Suggest an alternative circuit for a better voltage regulation, and draw its circuit diagram.
6. Draw and explain the operation of the protection circuit that can be employed in voltage regulators. How will you choose the value of the sensing resistor  $R_s$  in such a circuit?
7. Draw a circuit diagram for Bandgap reference voltage source.
8. Draw a voltage regulator circuit using IC LM 317.
9. Design a dc regulator to obtain 16VDC/1A with input voltage of 25V (average value).
10. Draw block diagram for IC voltage regulator.

## MODEL QUESTION

1. Design DC voltage regulator for 6V output. Given data  $V_Z = 6V$  at  $I_Z = 20mA$ ,  $I_{ZK} = 2mA$ ,  $P_{Zmax} = 500mW$  and  $r_z = 10\Omega$ . The normal input voltage is  $15V \pm 30\%$  DC. Find maximum current it can deliver to the load. [8]
2. Draw common emitter amplifier with bypass capacitor and derive its current gain and output resistance using its ac equivalent circuit. [8]
3. Design voltage divider bias circuit to get  $I_{CO} = 1.5 mA$ . Assume power supply voltage  $V_{CC} = 15 V$  and  $\beta$  of transistor is 110. [8]
4. Derive the expression for trans-conductance of BJT. [7]
5. Describe the construction and working principle of N-channel enhancement type MOSFET with the help of I-V characteristics curve and mathematical expression. [8]
6. Find  $I_D$  and  $V_{DS}$  for voltage divider JFET circuit. Given:  $V_{DD} = 18 V$ ,  $R_D = 2 K\Omega$ ,  $R_S = 1 K\Omega$ ,  $R_1 = 1.5 M\Omega$ ,  $R_2 = 330 K\Omega$ ,  $V_P = -5.5 V$  and  $I_{DSS} = 12 mA$ . [6]
7. Draw transformer coupled Class A amplifier and find its maximum efficiency. [6]
8. Draw the circuit diagram of Class A tuned amplifier and determine the range of frequency in which it gives maximum gain within -3 dB range. [7]
9. Draw circuit diagram of AB push pull amplifier with Darlington pair output stage. [3]
10. Draw and explain the working principle of RC phase shift oscillator and also derive the expression of frequency of oscillation [8]
11. Draw series voltage regulator with current limiting circuit and explain how this protection circuit works. [6]
12. Design a regulator circuit using LM317 to obtain 16 V DC with input voltage of 25 V DC. [4]
13. Write short notes on:
  - a. Voltage controlled oscillator using IC 555.
  - b. Heat sink[6]

## REFERENCES

- Sedra, Smith. *Microelectronic Circuits: Theory and Applications*, 5<sup>th</sup> ed. New York, Oxford University Press, 2010.
- R.L. Boylestad, Louis Naschelsky. *Electronic Device and Circuit Theory*. 9<sup>th</sup> ed. New Jersey: Pearson Education, 2006.
- Malvino. *Electronic Principles*. 6<sup>th</sup> ed. New York: The Mc Graw-Hill Companies, 2006.
- Theodore F. Bogart. *Electronic Devices and Circuits*. 4<sup>th</sup> ed. New York: Bell & Howell Company, 2000.
- Jacob Millman, Christos C. Halkias. *Electronic Devices and Circuits*. 5<sup>th</sup> ed. New York: The Mc Graw-Hill Companies, 2008.
- J.B. Gupta. *A Course in Electrical Technology*. 12<sup>th</sup> ed. New Delhi: S.K. Kataria & Sons, 2010.
- David A. Bell *Electronic devices and Circuits* 3<sup>rd</sup> ed. Prentice Hall of India Pvt. Ltd New Delhi - 2000