Development of Virtual lab :Round 2 (R2)-Storyboard - Template (Worksheet)

Name of Faculty: Dr. Siddhartha Arjaria
Institute: Rajkiya Engineering College Banda
Email ID (as submitted in the registration form)**: arjarias@gmail.com**
Discipline to which the Lab belongs: Electronics Engineering
Name of the Lab: Basic Electronics VLab
Name of experiment:Logic Gates
(only one Experiment per worksheet)**:**

Kindly Refer these documents before filling the worksheet

1. **Coursework (MOOC) on Pedagogy , Storyboard , Lab Manual : http://bit.ly/Vlabs-MOOC**
2. **Additional Documentation booklet for reference. http://vlabs.iitb.ac.in/vlabs-dev/document.php**
3. **Sample Git Repository. : https://github.com/Web-planner/Electronic-Simulator.git**

Round 2

1. Story Outline:

The earliest **logic gates** were made mechanically. Charles Babbage, around 1837, devised the Analytical Engine. His **logic gates** relied on mechanical gearing to perform operations. Electromagnetic relays were later used for **logic gates**.

2. Story:

2.1 Set the Visual Stage Description:

A logic gate performs a logical operation on one or more logic inputs and produces a single output. The logic normally performed is Boolean logic and is most commonly found in digital circuits. Logic gates are primarily implemented electronically using diodes or transistors, but can also be constructed using electromagnetic relays, fluidics, optics, or even mechanical elements.

2.2 Set User Objectives & Goals:

1- To study and understand the 7 basic gates.
2- Implement the basic gateV
3- The study the specifications of every gate when connected it with one input constant and the other is variable.

2.3 Set Challenges and Questions/Complexity/Variations in Questions:

1. Electronic circuits that operate on one or more input signals to produce standard output _____

a). Series circuits

b). Parallel Circuits

c). Logic Signals

d). Logic gates

2. Logic Gates are the building blocks of all circuits in a computer.

a). True

b). False

3. A _____ gate gives the output as 1 only if all the inputs signals are 1.

a) AND

b) OR

c) EXOR

d) NOR

4. The boolean expression of an OR gate is _____

a). A.B

b). A’B+AB’

c). A+B

d). A’B’

5. The gate which is used to reverse the output obtained is _____

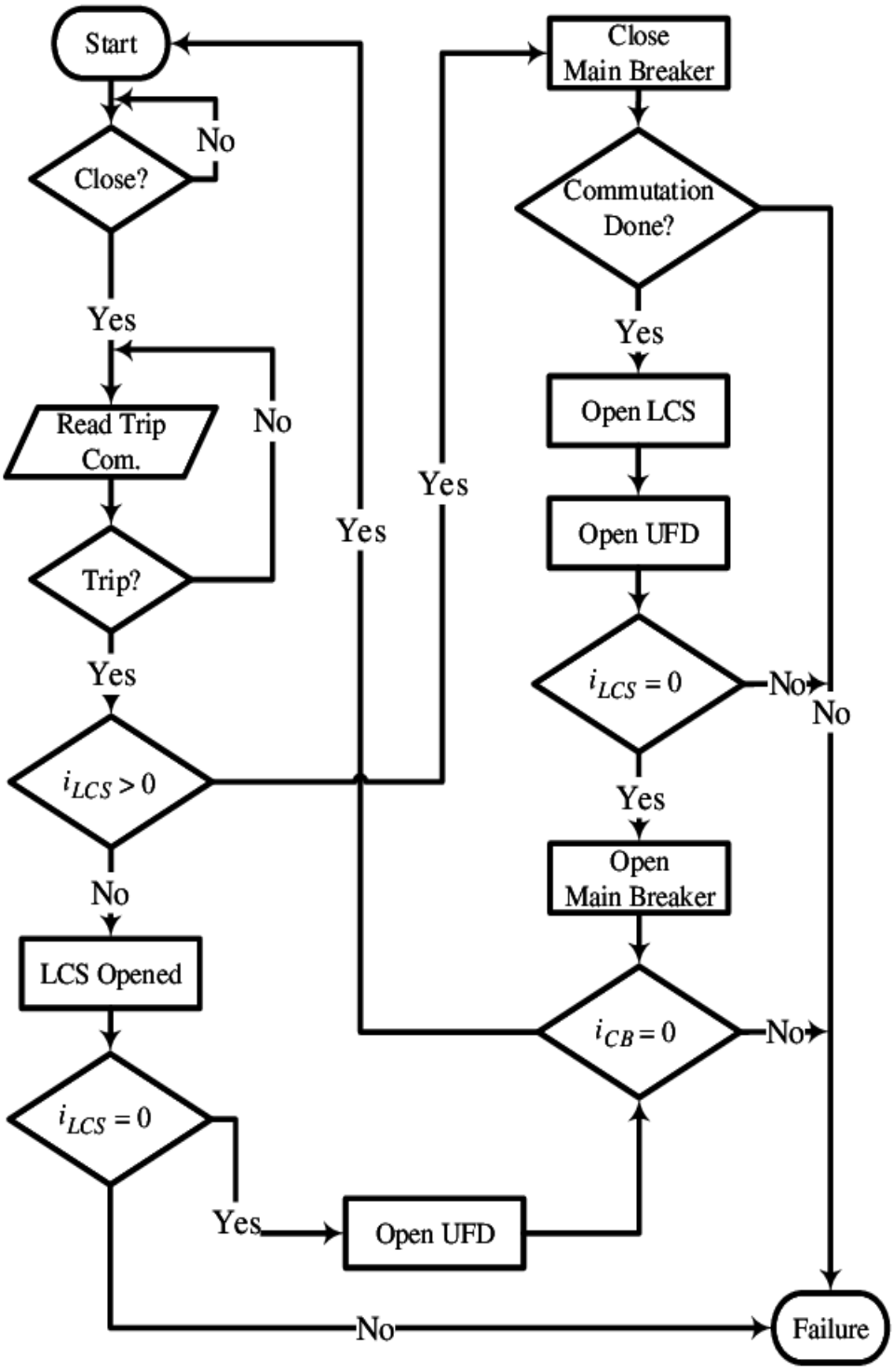
a). NOR

b). NAND

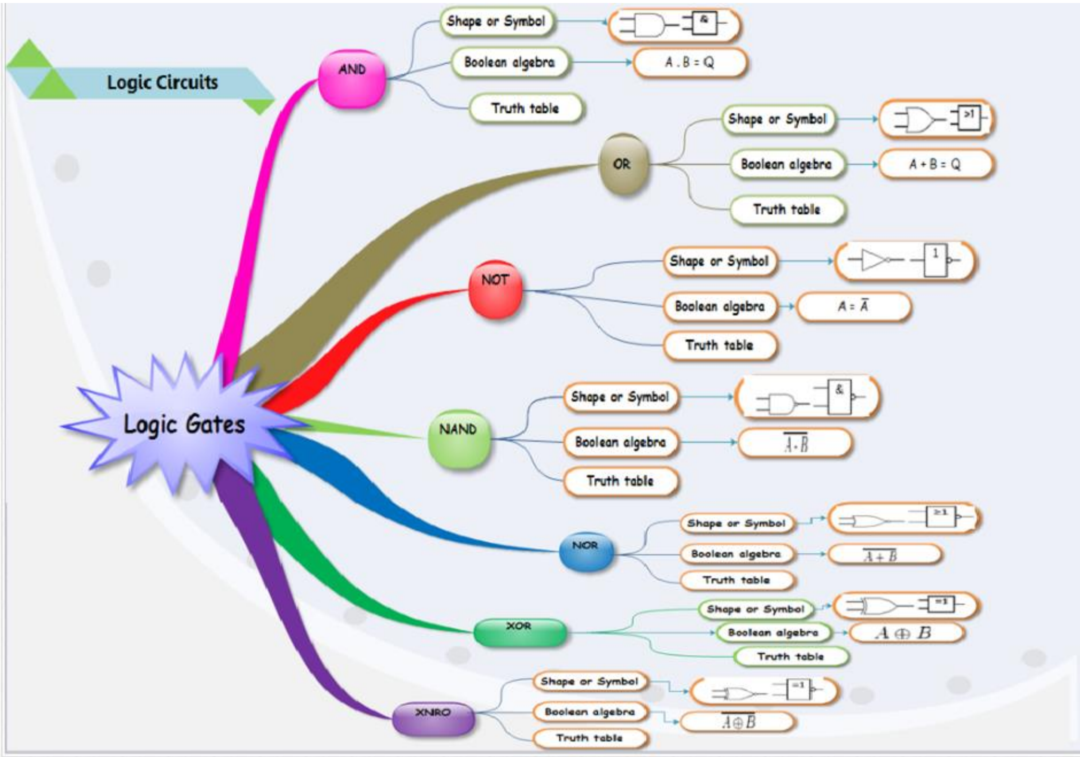
c). EXOR

d). NOT

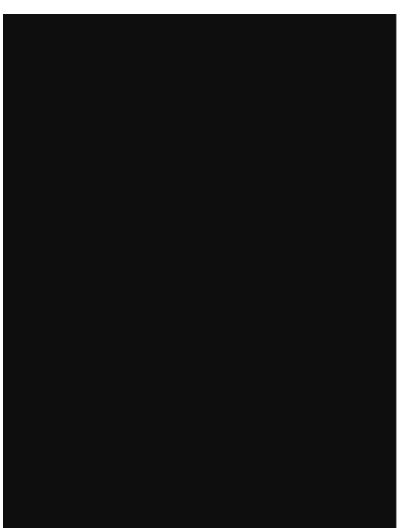
3. Flowchart

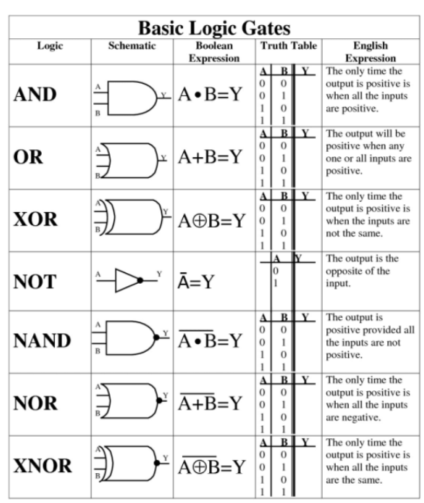

Start
Close?
No
Yes
Read Trip Com.
No
Trip?
Yes
$i_{LCS} > 0$
No
LCS Opened
$i_{LCS} = 0$
Yes
Open UFD
No
Failure
Yes
Yes
Close Main Breaker
Commutation Done?
Yes
Open LCS
Open UFD
$i_{LCS} = 0$
No
No
Yes
Open Main Breaker
$i_{CB} = 0$
No

4. Mindmap



4. Storyboard





Basic Logic Gates

Logic	Schematic	Boolean Expression	Truth Table	English Expression
AND		A•B=Y	A B Y 0 0 0 1 1 0 1 1	The only time the output is positive is when all the inputs are positive.
OR		A+B=Y	A B Y 0 0 0 1 1 0 1 1	The output will be positive when any one or all inputs are positive.
XOR		A⊕B=Y	A B Y 0 0 0 1 1 0 1 1	The only time the output is positive is when the inputs are not the same.
NOT		Ā=Y	A Y 0 1	The output is the opposite of the input.
NAND		$\overline{A \cdot B}$=Y	A B Y 0 0 0 1 1 0 1 1	The output is positive provided all the inputs are not positive.
NOR		$\overline{A + B}$=Y	A B Y 0 0 0 1 1 0 1 1	The only time the output is positive is when all the inputs are negative.
XNOR		$\overline{A \oplus B}$=Y	A B Y 0 0 0 1 1 0 1 1	The only time the output is positive is when all the inputs are the same.