



Notification: Final Exam

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- Date: Dec. 19 (Thursday)
- Class Time (1h 15m), Closed book

T/F problems + Computation problems + Descriptive problems

Scope: All the material learned after the midterm

Notification: HW3

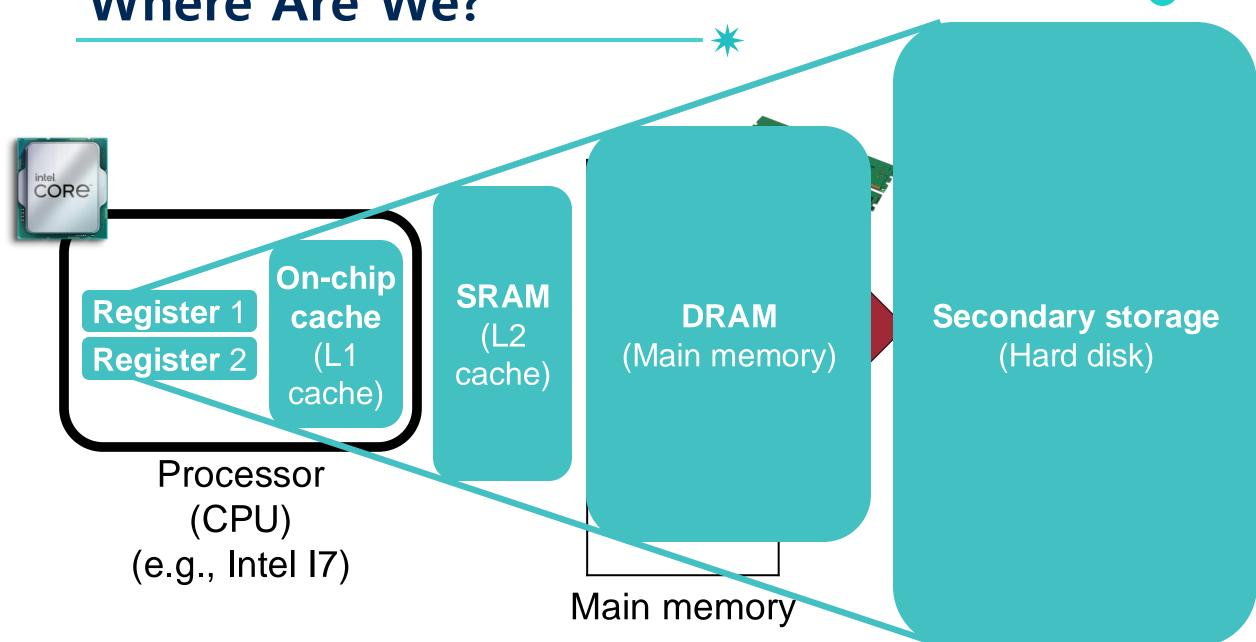


Implementing a cache simulator

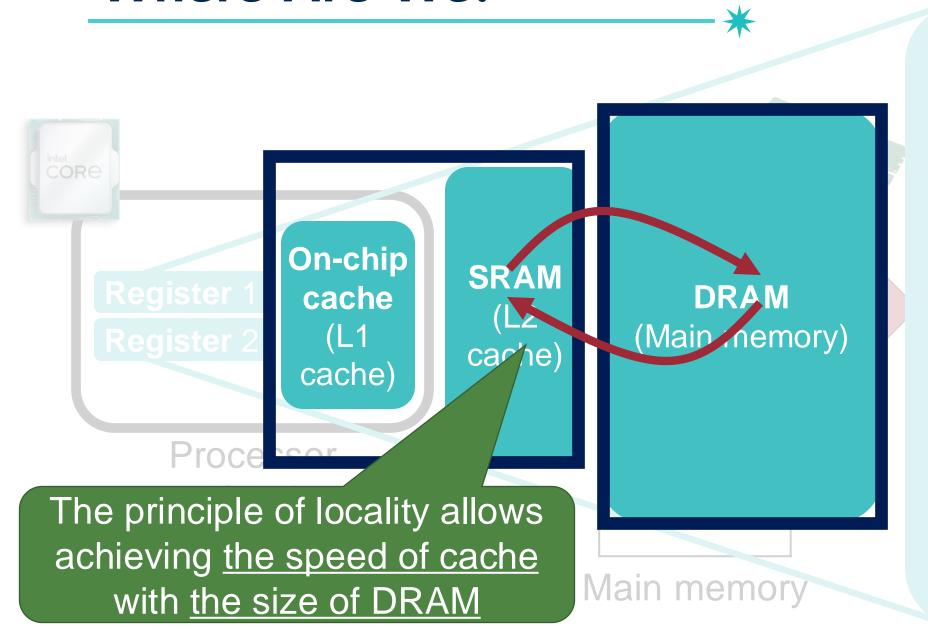
Due: Dec 15, 11:59 PM

 Since the final exam period is approaching, it is recommended to complete this assignment <u>as soon as possible</u>

Where Are We?



Where Are We?



Secondary storage (Hard disk)

Today's Topic: DRAM/HDD

We want to give the speed of DRAM with the size of hard disk!

Register 1
Register 2

cache (L1 cache) SRAM (L2 cache)

DRAM (Main memory)

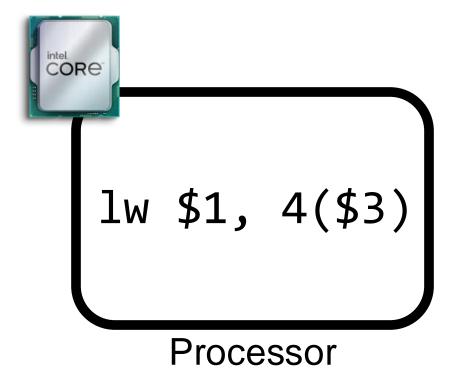
Secondary storage (Hard disk)

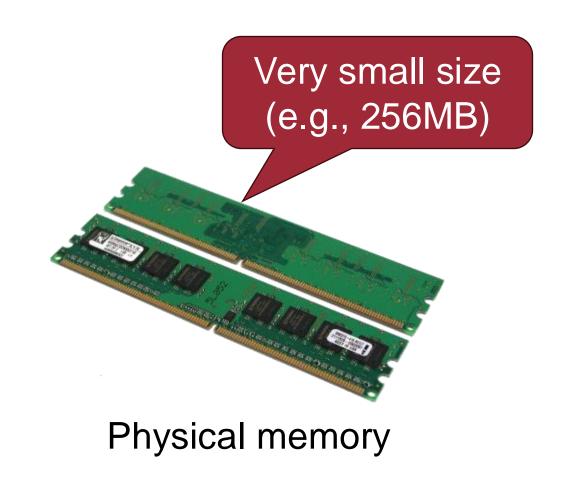
Processor (CPU) (e.g., Intel I7)

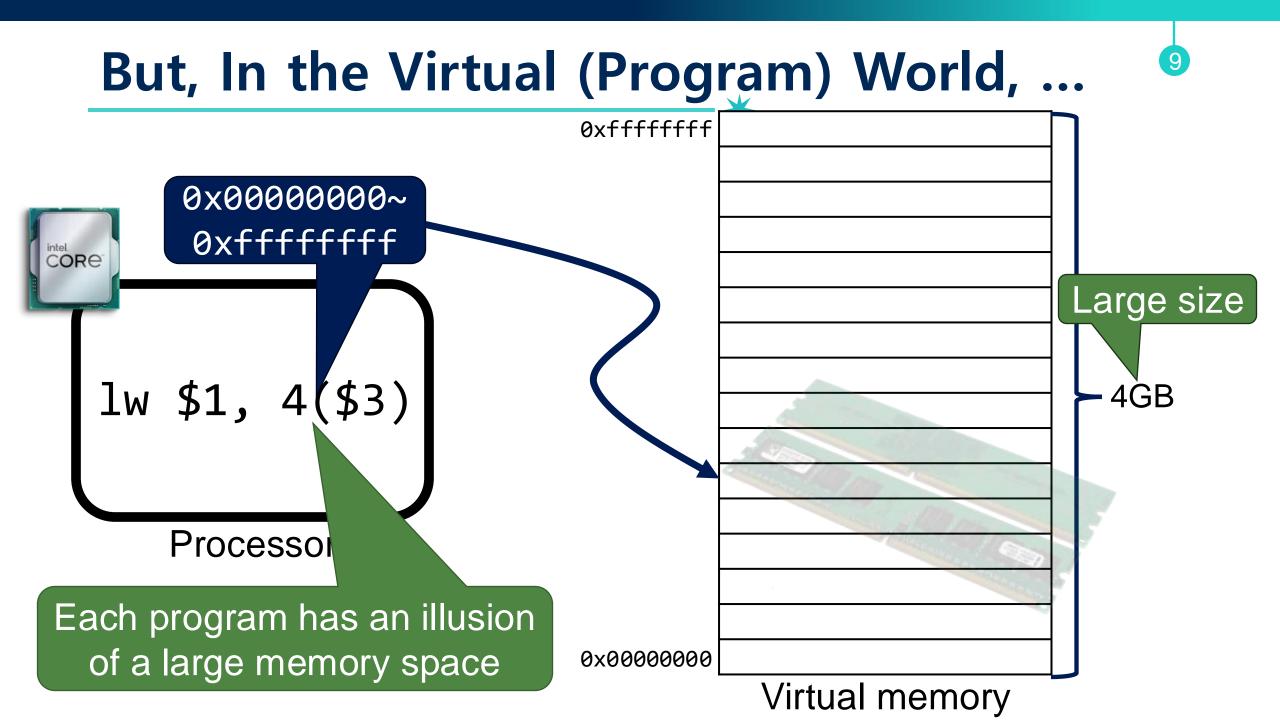
Main memory

Introduction to Virtual Memory

In the Physical World, We Have Limited-sized Memory







Virtual Memory

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 Give programmers an illusion of a large memory space irrespective of actual capacity

Virtual Memory

1

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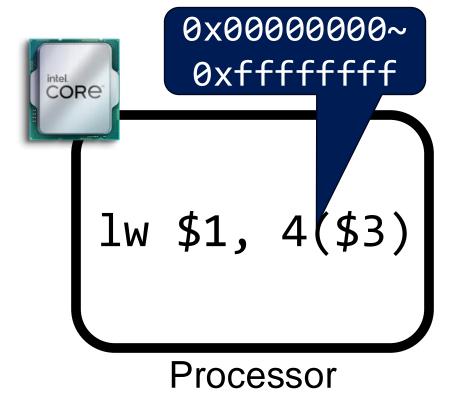
 Give programmers an illusion of a large memory space irrespective of actual capacity

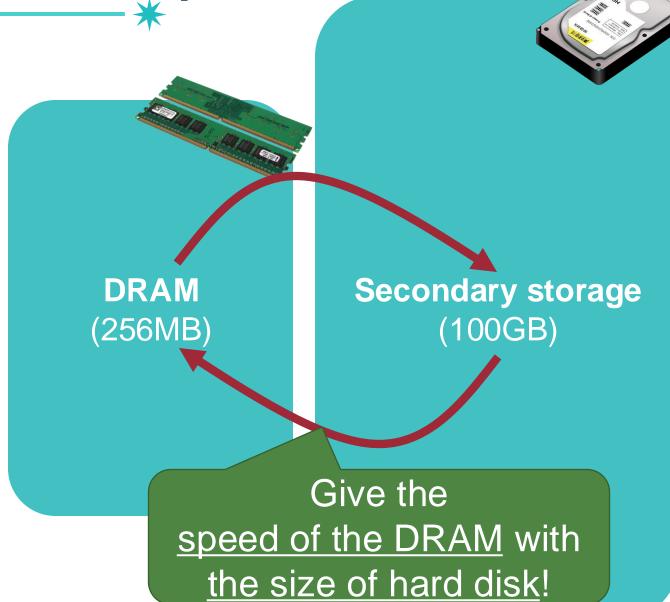


How do we give an illusion despite having small-sized physical memory?

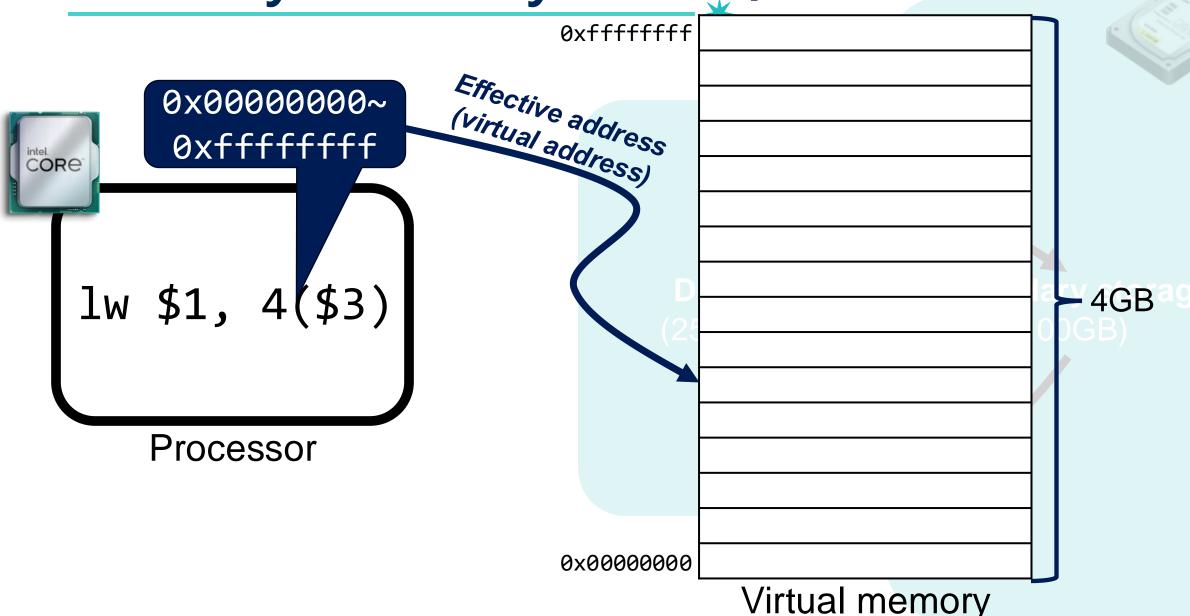
Memory hierarchy between RAM and HDD

Memory Hierarchy: DRAM/HDD



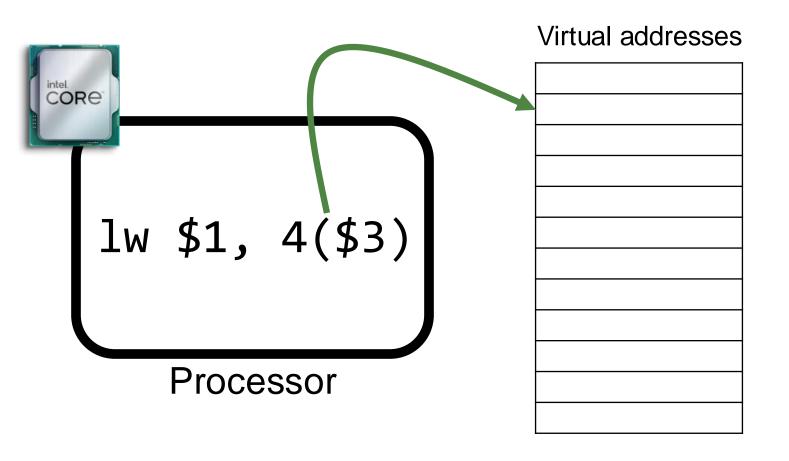


Memory Hierarchy: DRAM/HDD

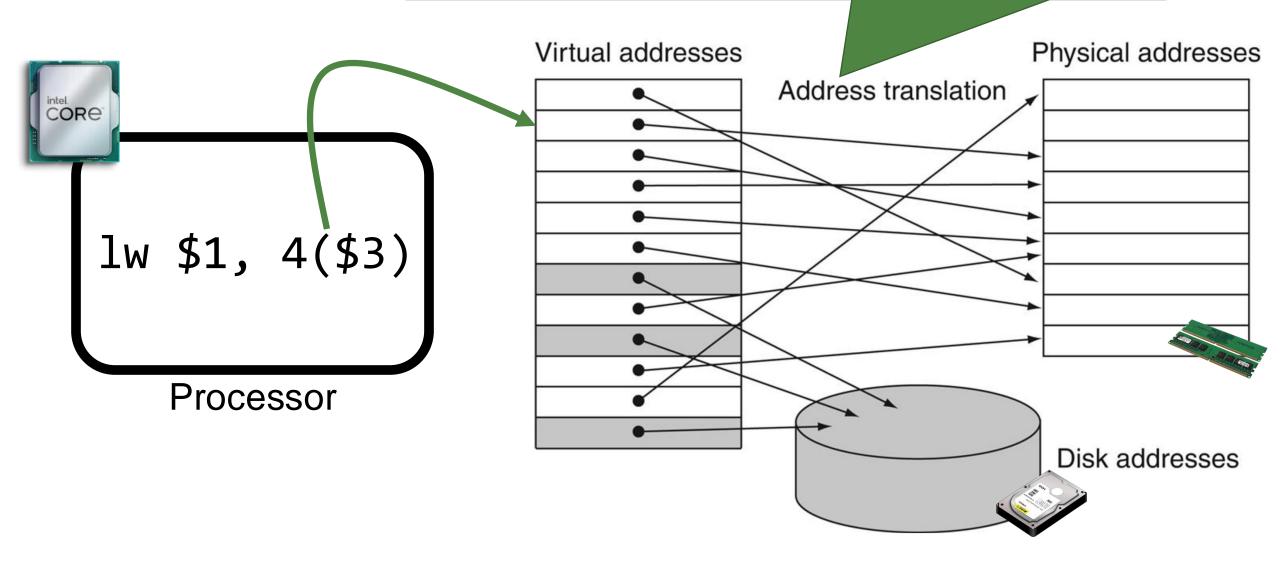


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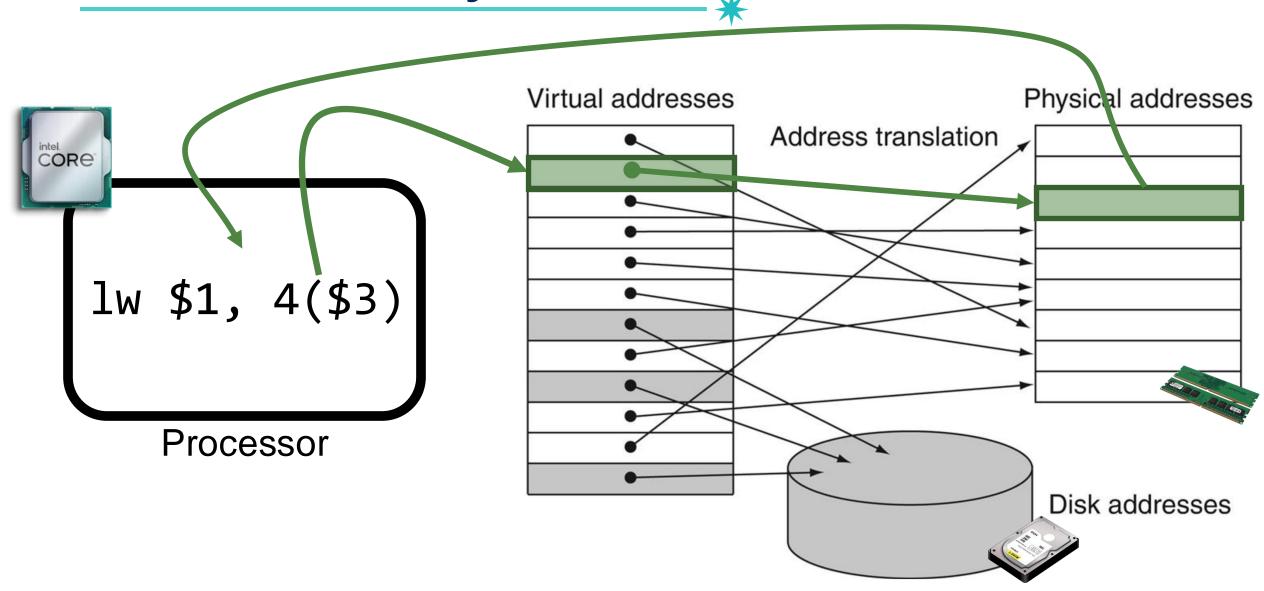
Memory Hierarchy: DRAM/HDD



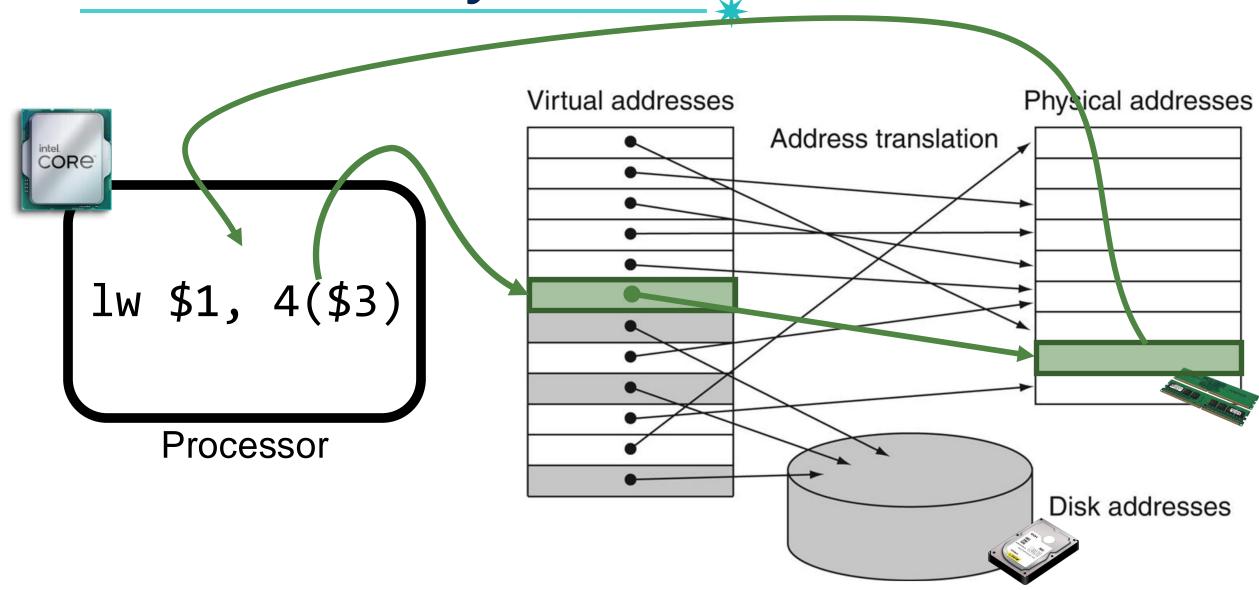
Memory Hi Address translation table (OS-managed table) Virtual address → Physical address

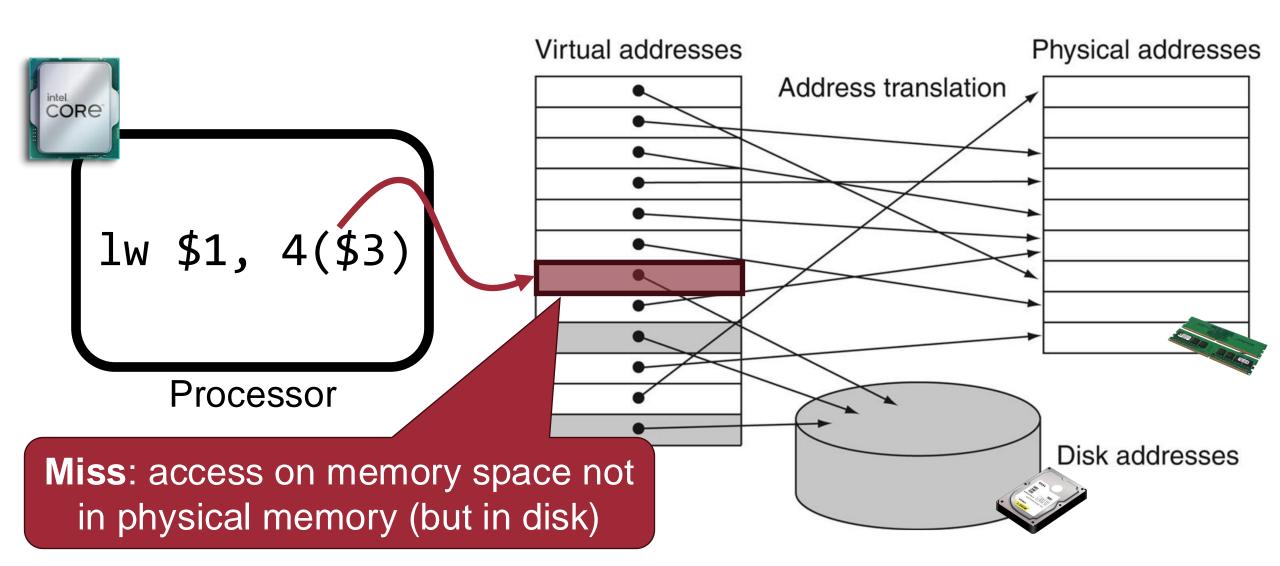


Virtual Memory Hit

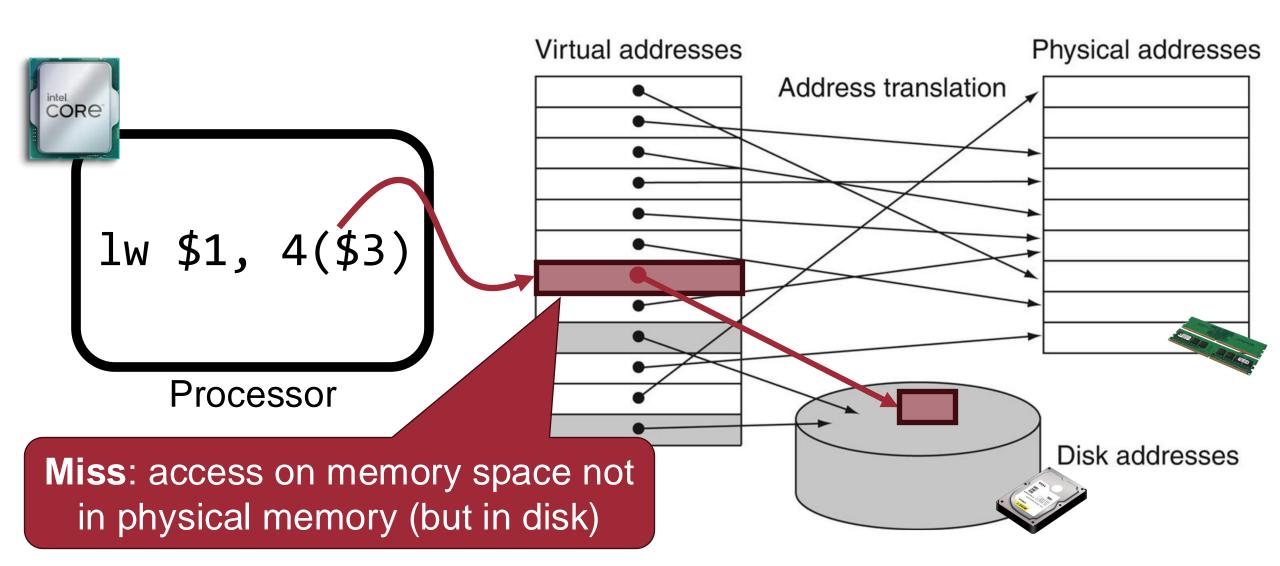


Virtual Memory Hit

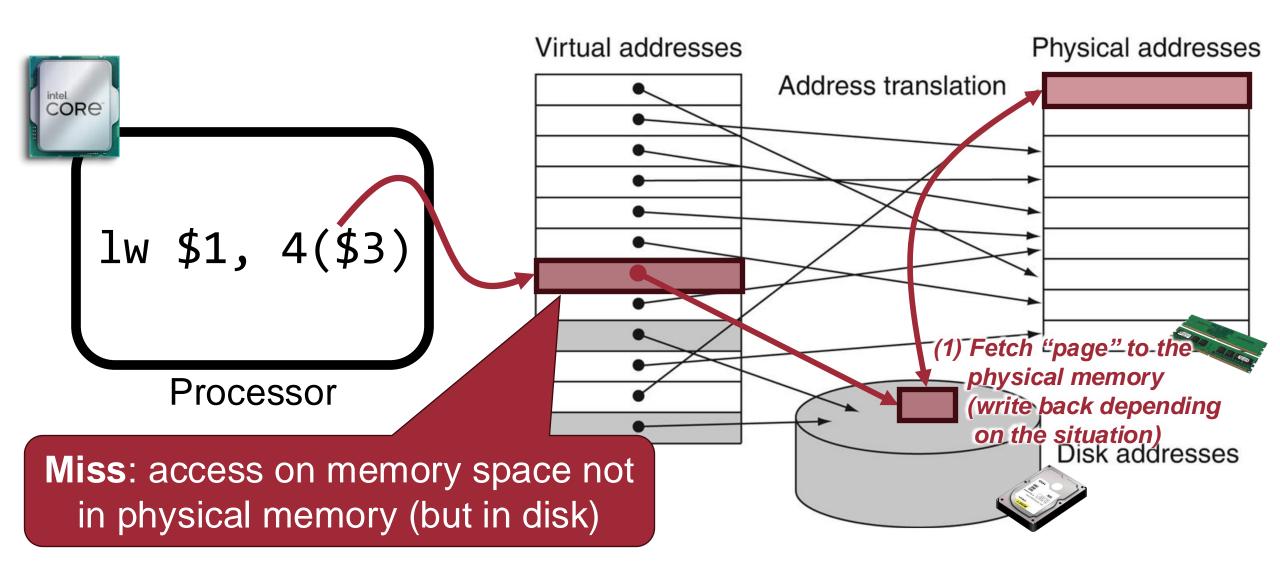


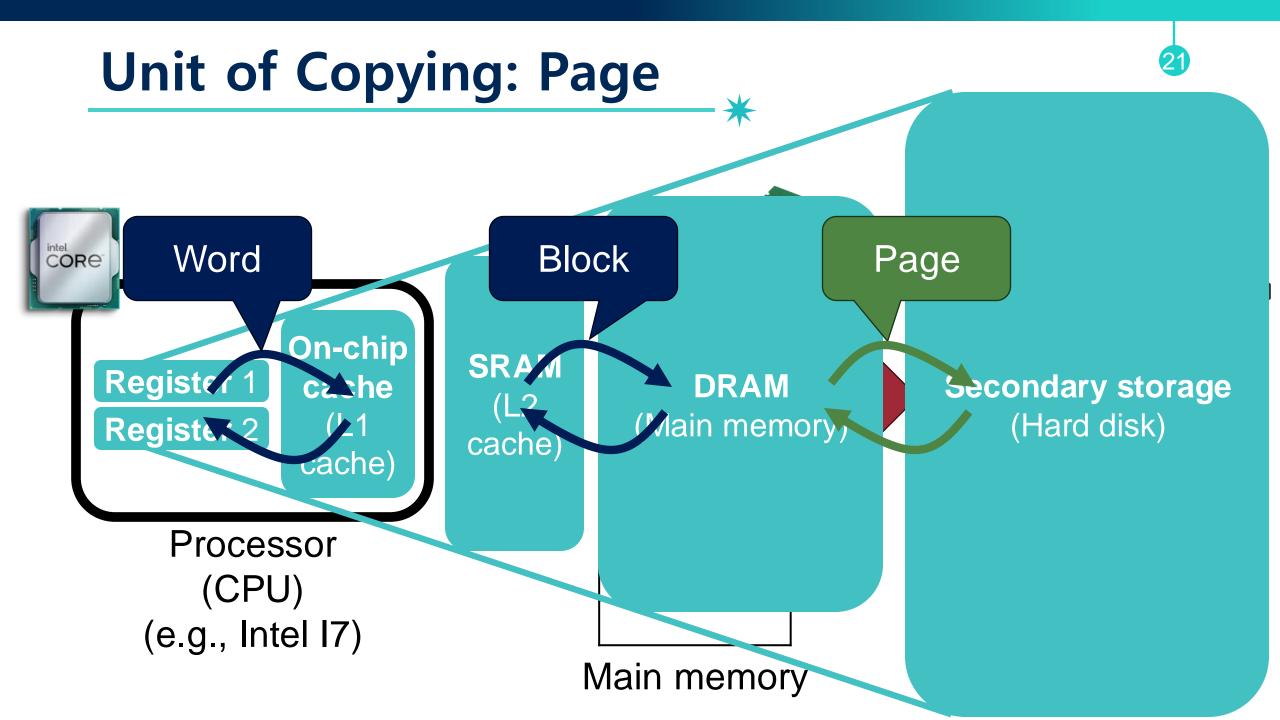


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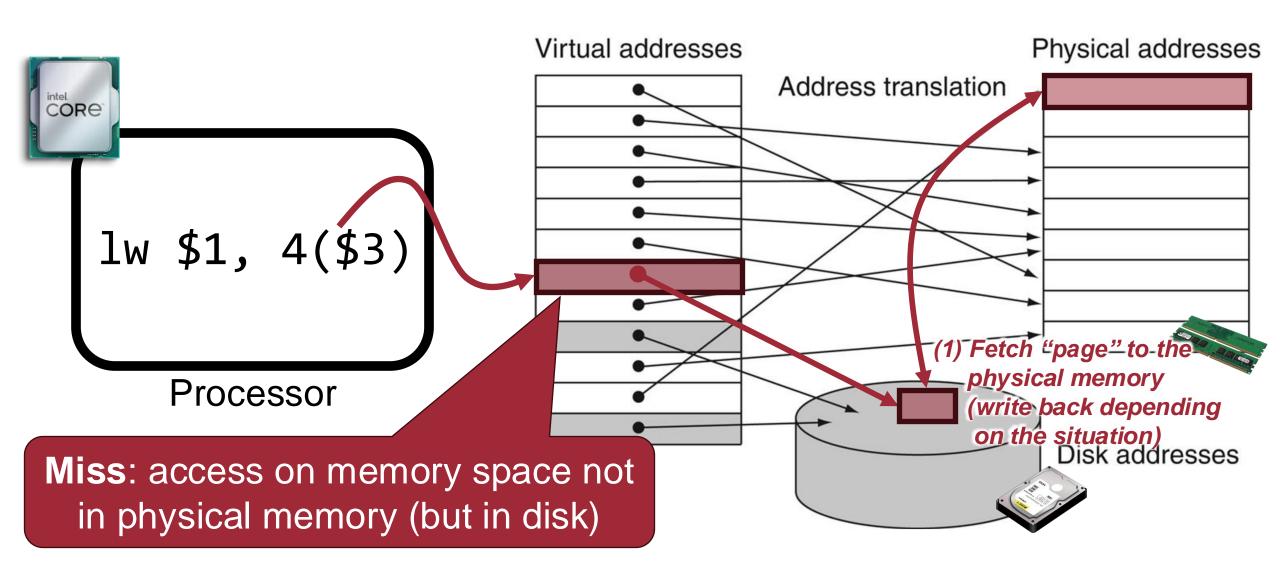




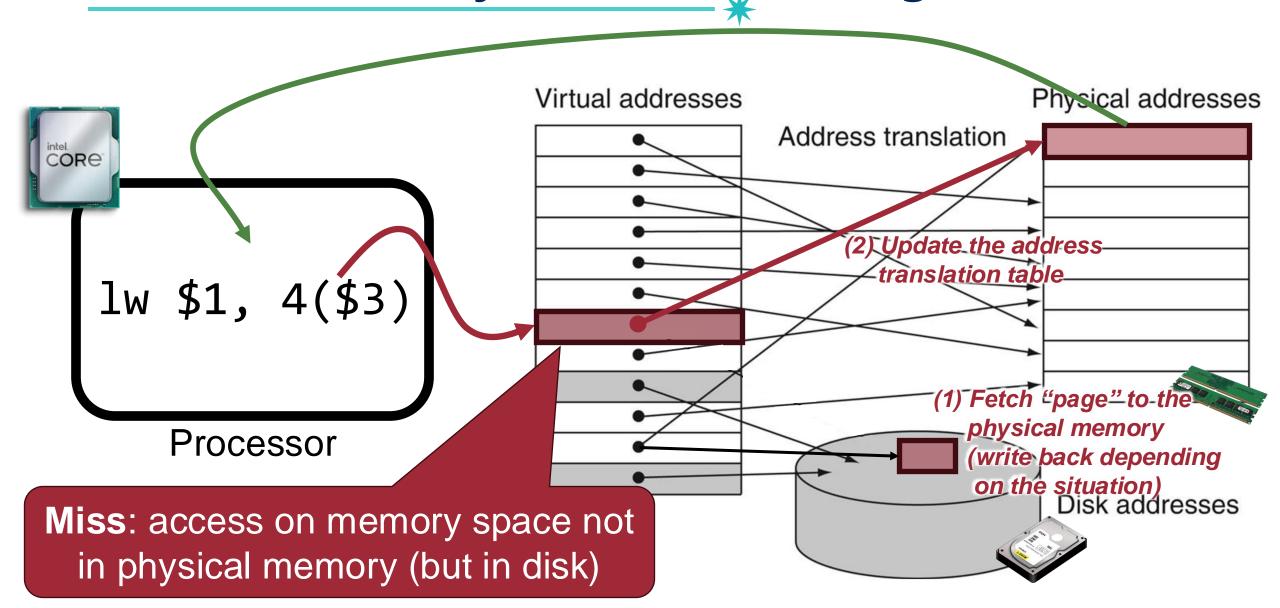












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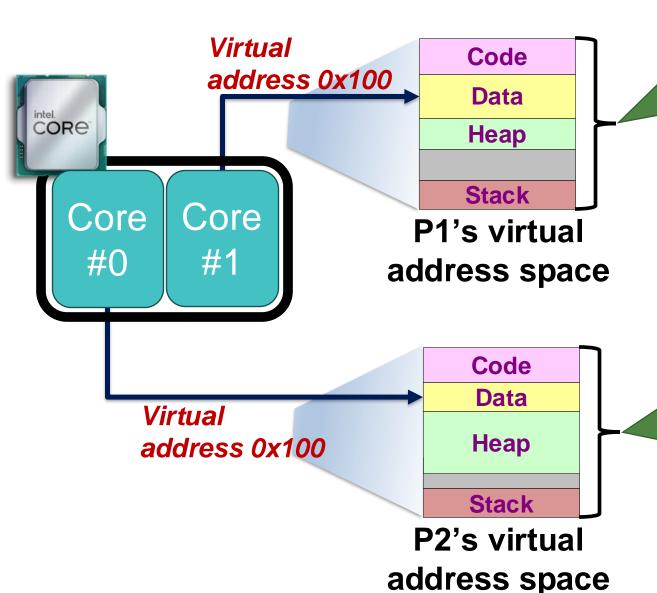
Virtual Memory



- Give programmers an illusion of a large memory space irrespective of actual capacity
- Uses main memory as a "cache" for the hard disk

- Other benefits?
 - -Program simplification: give each program the illusion that it has its own private memory (e.g., 0x00000000~0xffffffff)

Program Simplification

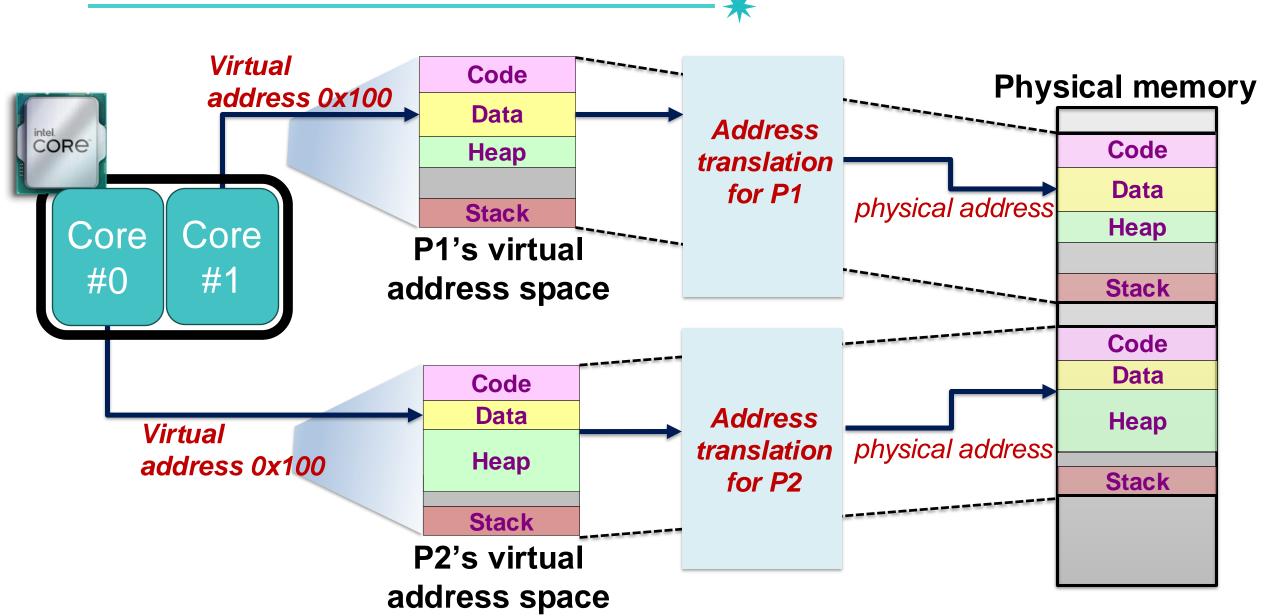


P1 can use the entire address space (starting from 0x0)

Each process thinks it has its *own memory space!*

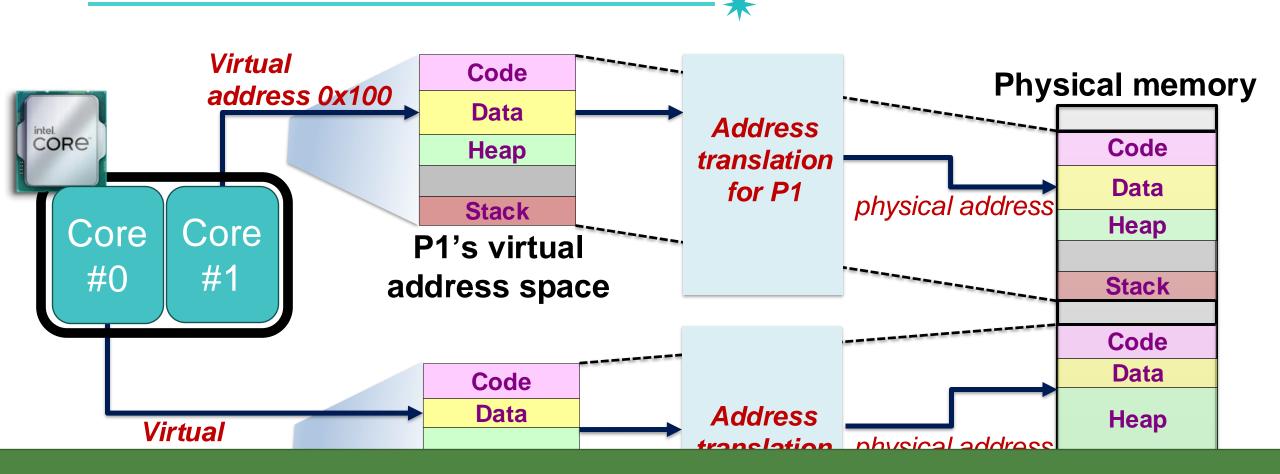
P2 can use the entire virtual address space (starting from 0x0)

Program Simplification









Programming and storage management ease

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Virtual Memory

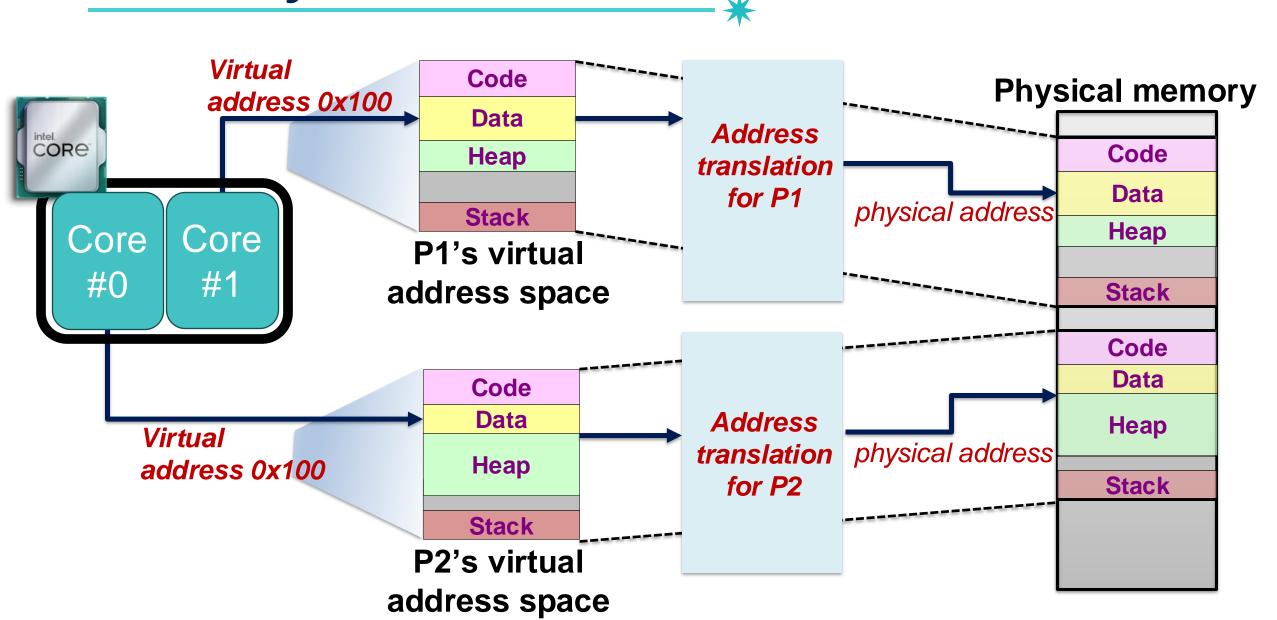


- Give programmers an illusion of a large memory space irrespective of actual capacity
- Uses main memory as a "cache" for the hard disk

- Other benefits?
 - -Program simplification: give each program the illusion that it has its own private memory (e.g., 0x00000000~0xffffffff)
 - -Security: memory protection between processes

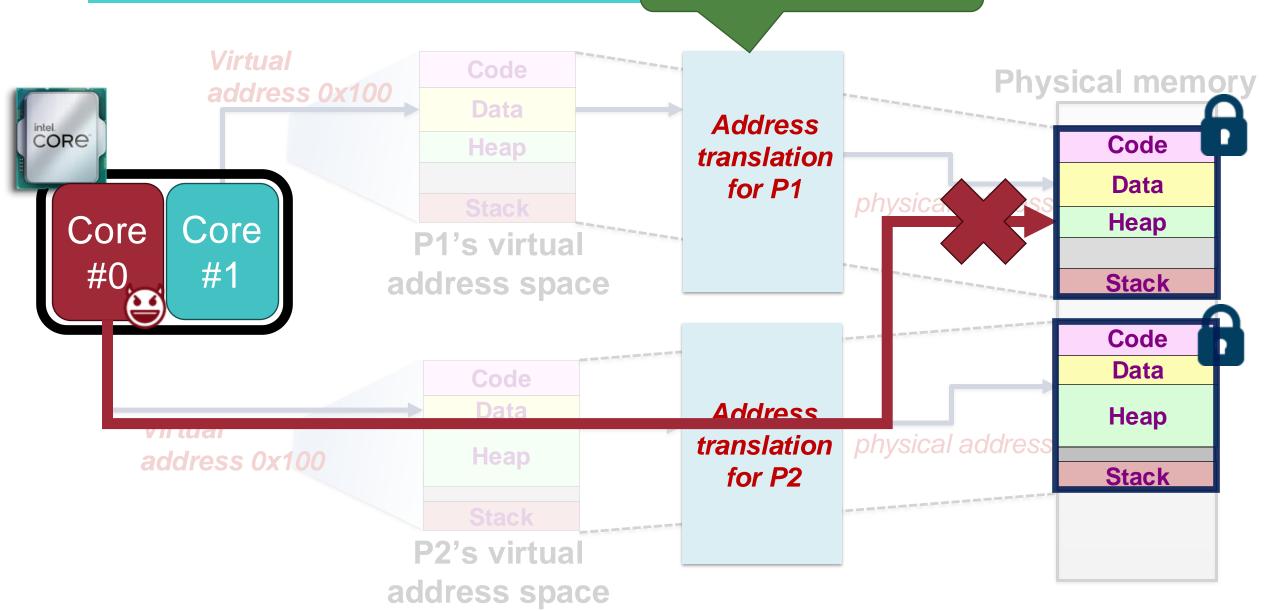
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Memory Protection



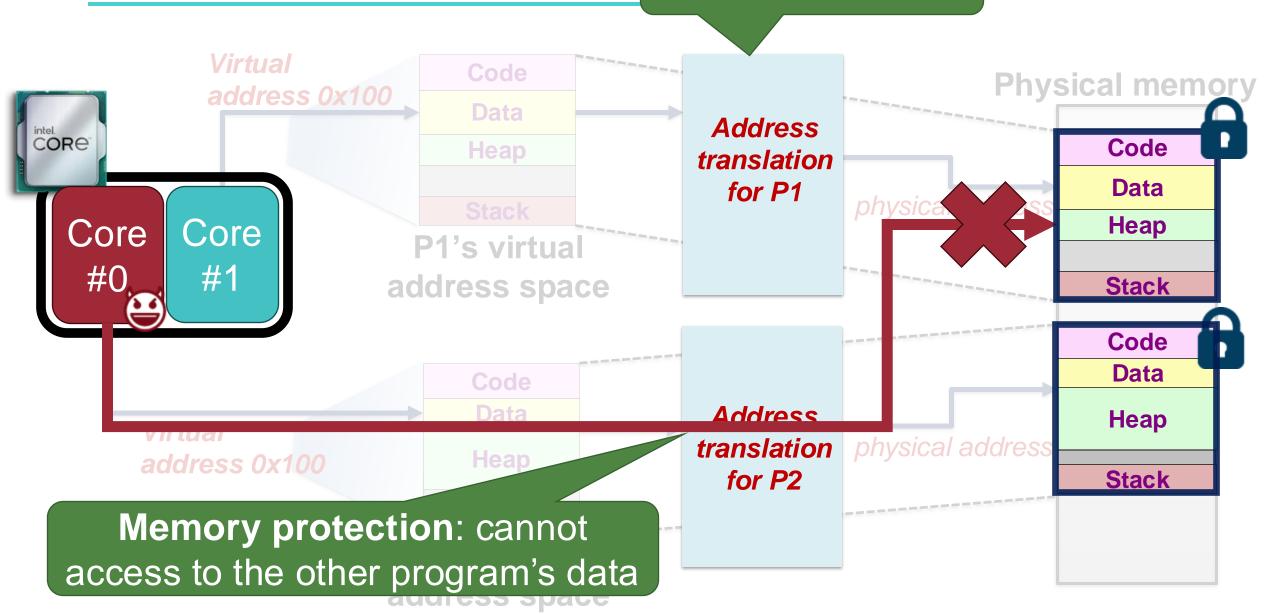
Memory Protection

OS-managed table



Memory Protection

OS-managed table



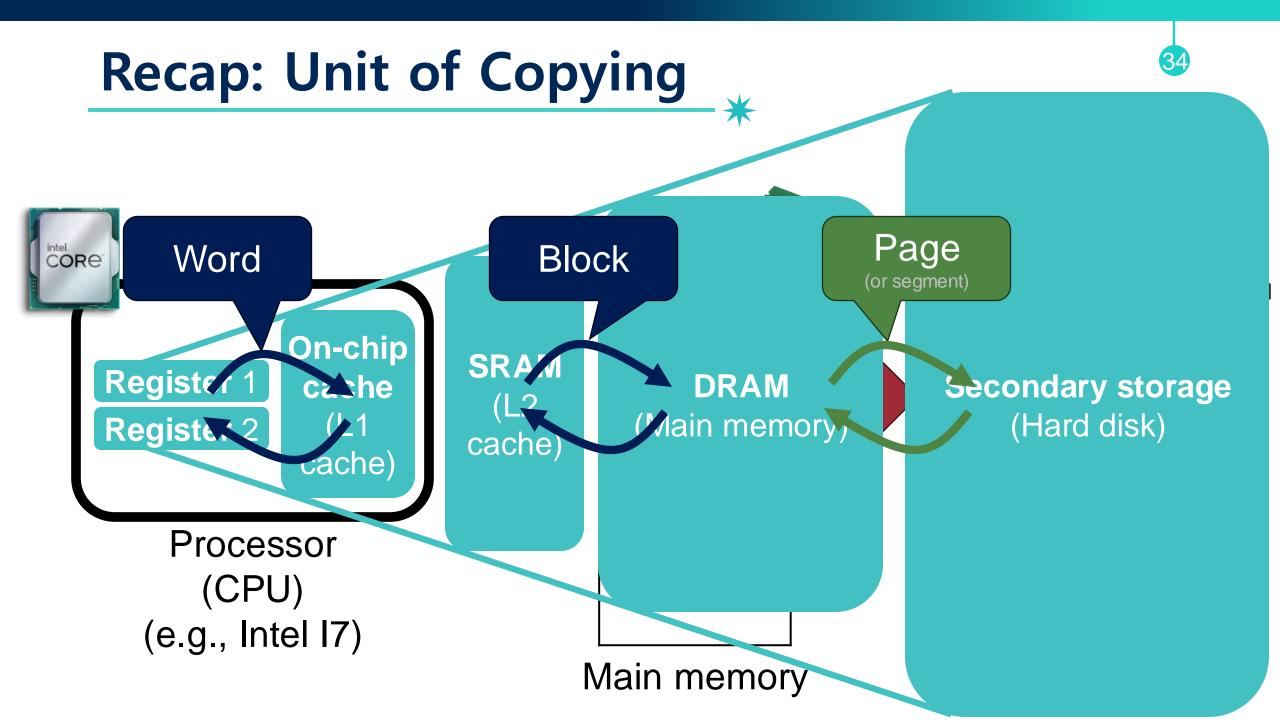
Virtual Memory Summary



- Idea: Give programmers an illusion of a large memory space irrespective of actual capacity
 - Programmers assume they have "infinite" amount of physical memory
 - Programmers do not need to worry about how to manage it (simplifies memory management for multi-processing system)

- CPU and OS cooperatively manage physical memory space to provide the illusion on behalf of users
 - Illusion is maintained for each independent process
 - Let OS to share memory, protect programs from each other

Unit of Copying: Page



Virtual Memory Block Type #1: Page

- A block of virtual memory
- Unit of copying
 - between DRAM and Disk
- Fixed length
 - -e.g., 4KB
 - Generally, 4KB ~ 4MB

Page #1

Page #2

Page #3

Page #4

Page #5

. . .

Page #N

Process A (Virtual memory)

Virtual Memory Block Type #1: Page

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Page #1

Page #2

Page #3

Page #4

Page #5

. . .

Page #N

Process A (Virtual memory)

Fixed-length virtual memory block

Virtual Memory Block Type #2: Segment

Segment length is variable!

Code segment

Data segment

• • •

Stack segment

Process A (Virtual memory)

Page

- A block of virtual memory
- Unit of copying
 - between DRAM and Disk
- Fixed length
 - -e.g., 4KB
 - Generally, 4KB ~ 4MB

Page #1

Page #2

Page #3

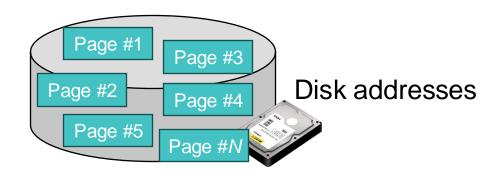
Page #4

Page #5

. . .

Page #N

Process A (Virtual memory)



Memory Paging (a.k.a., Swapping)

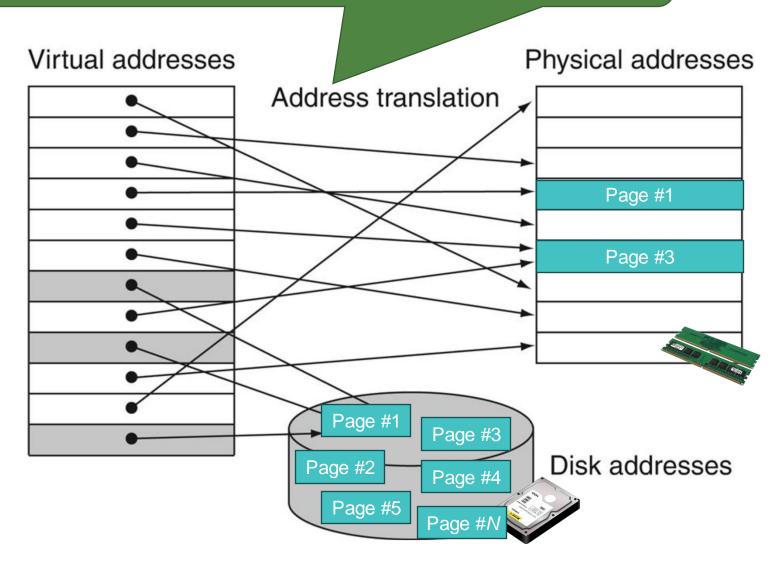
Memory management scheme by which a computer stores and retrieves data from secondary storage for

use in main memory

Physical addresses Page: unit of copying! Page #1 Page #3 **Paging** (Swapping) Page #1 Page #3 Disk addresses Page #2 Page #4 Page #5 Page #/

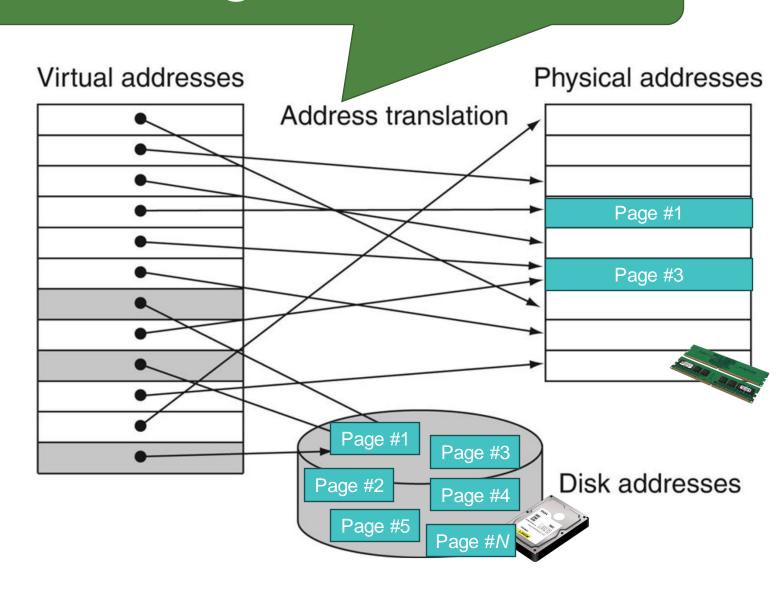
Address Translation

Memory Hi Address translation table (OS-managed table) Virtual address → Physical address



Memory Hi

"Page Table"



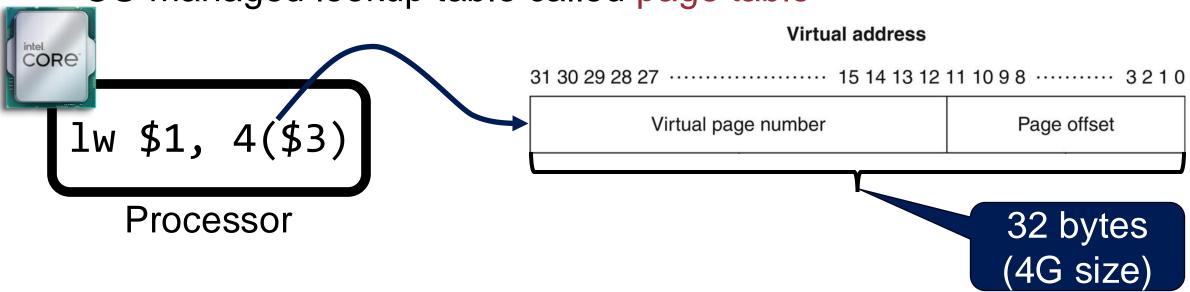


Page Table: Address Translation

CPU converts virtual addresses into physical addresses via an OS-managed lookup table called page table

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CPU converts virtual addresses into physical addresses via an OS-managed lookup table called page table



Recap: the range of memory addresses a 32-bit machine (e.g., MIPS) can access?

Representable range $= 0 \sim 2^{32}-1$

0xffffffff

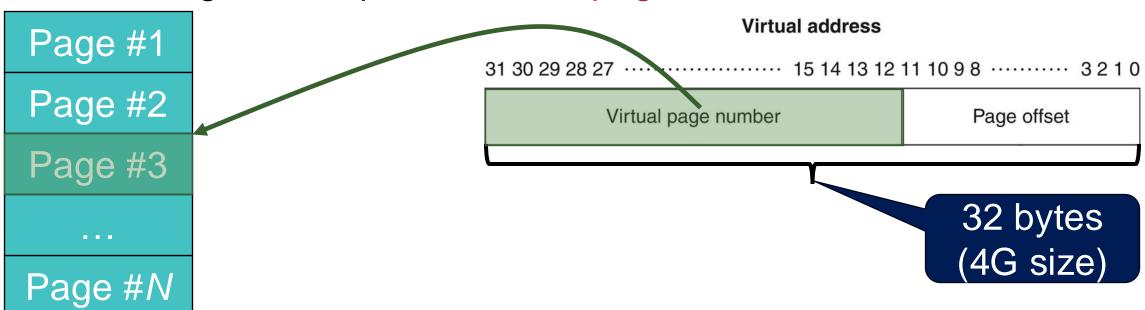
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0x00000001 0x000000000 Q. What is the maximum memory capacity a 32-bit machine can handle?

2³² bytes = 4GB

Programmer's Point of View

CPU converts virtual addresses into physical addresses via an OS-managed lookup table called page table

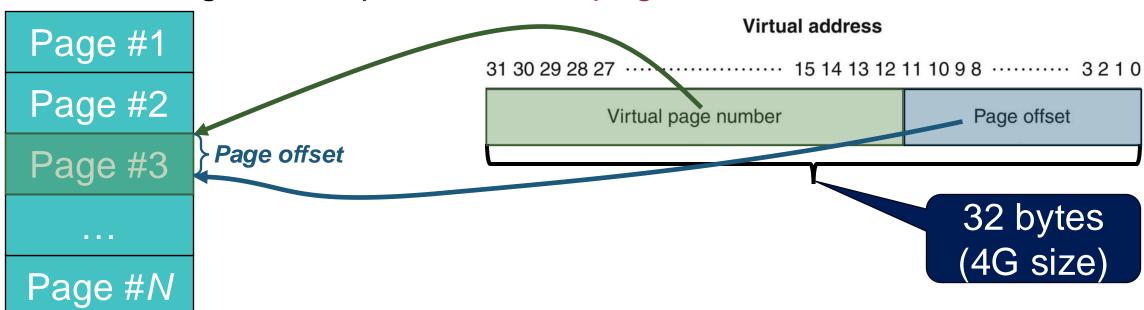


Virtual addresses

Programmer's Point of View

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CPU converts virtual addresses into physical addresses via an OS-managed lookup table called page table

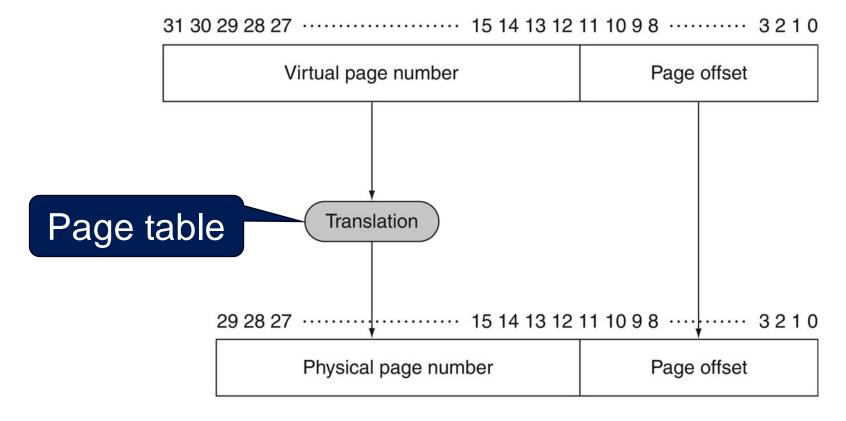


Virtual addresses

Page Table: Address Translation

CPU converts virtual addresses into physical addresses via an OS-managed lookup table called page table

Virtual address

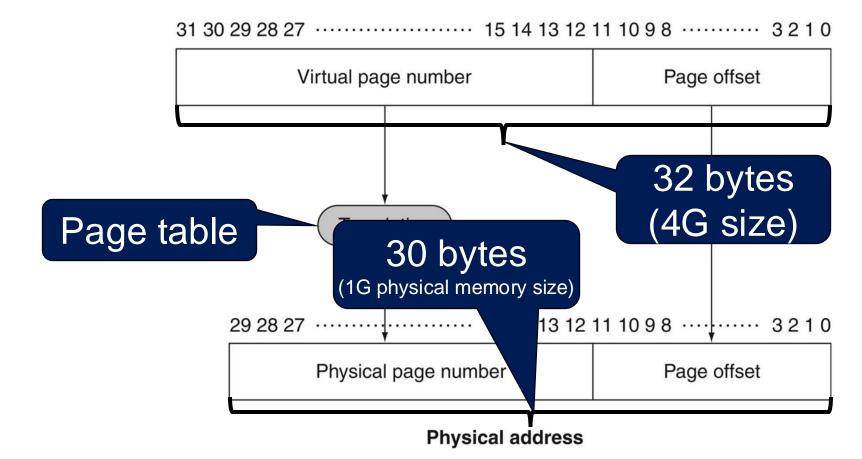


Physical address

Page Table: Address Translation

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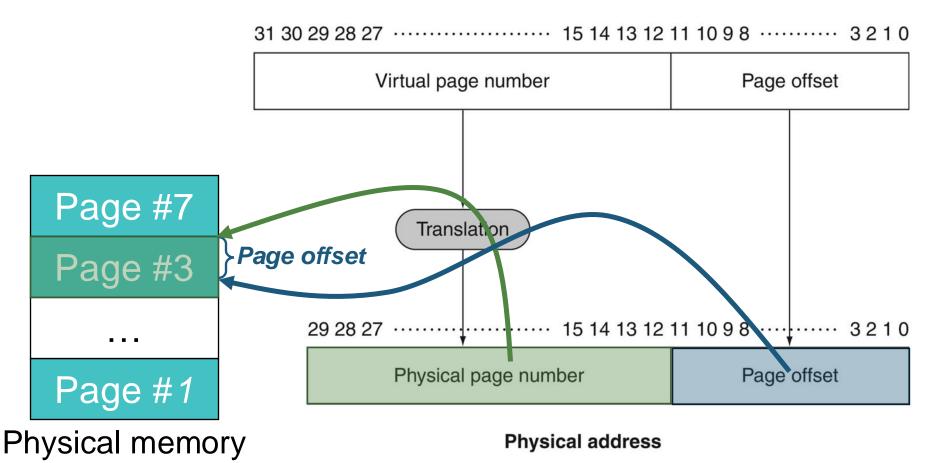
Virtual address



Page Table: Address Translation

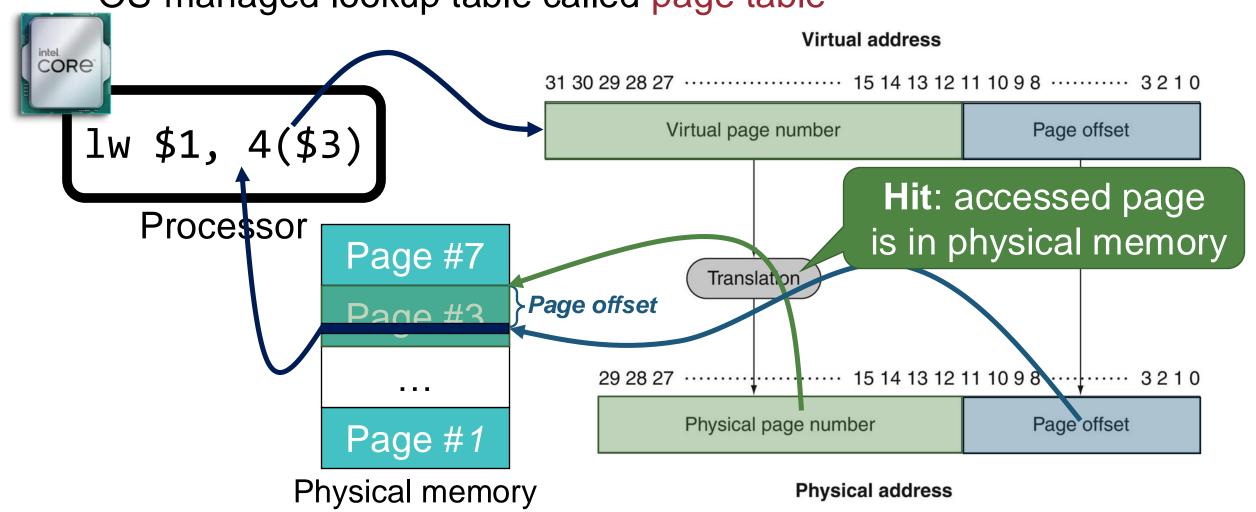
CPU converts virtual addresses into physical addresses via an OS-managed lookup table called page table

Virtual address



Address Translation Flow (Hit Case)

CPU converts virtual addresses into physical addresses via an OS-managed lookup table called page table

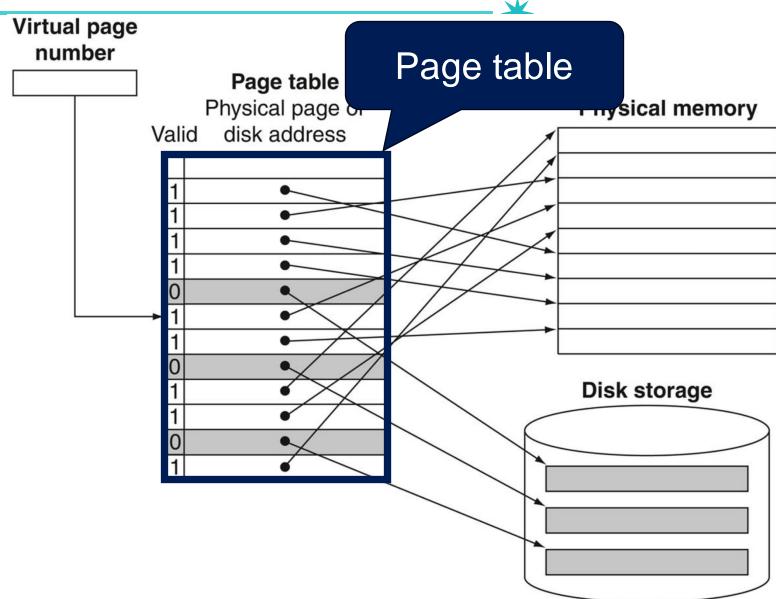


Page Table: Address Translation

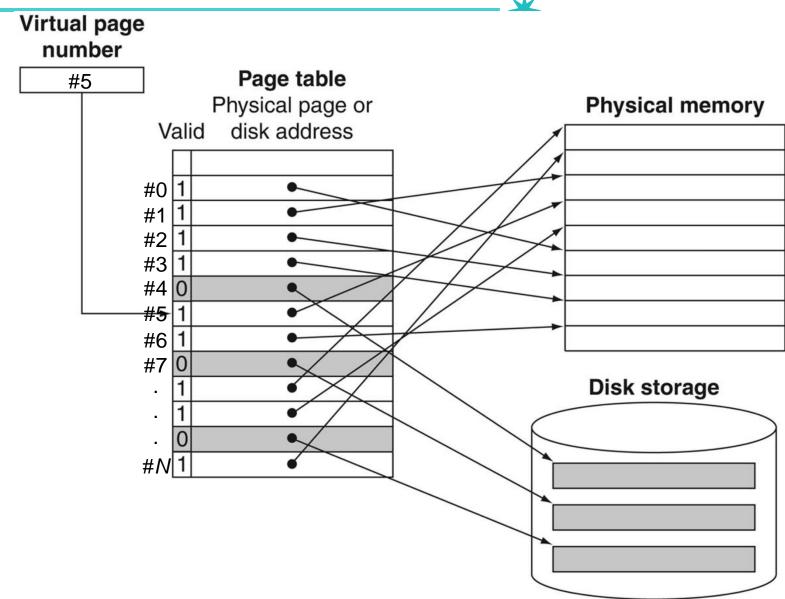
- 52
- CPU converts virtual addresses into physical addresses via an OS-managed lookup table called page table
- Mapping from a virtual to physical address
 - Virtual address = virtual page number + page offset
 - Physical address = physical page number + page offset

Each program has its own page table!

Page Table: Details

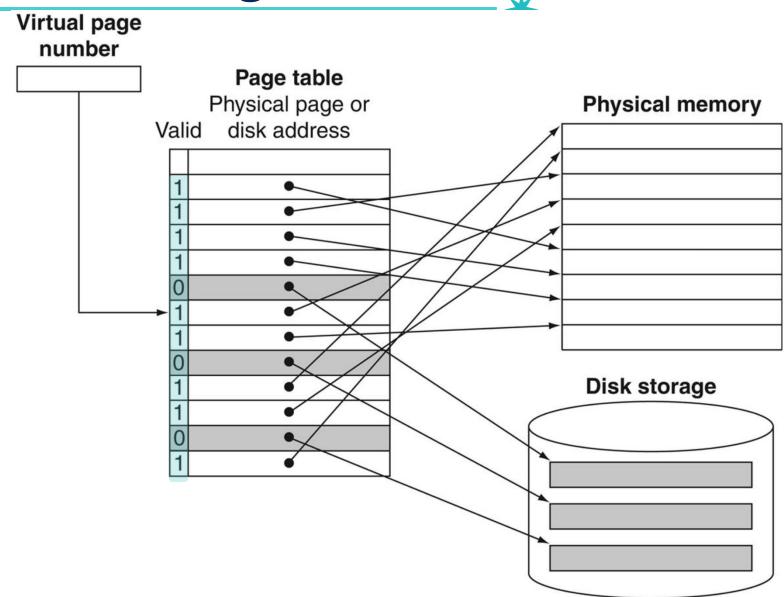


Page Table: Details

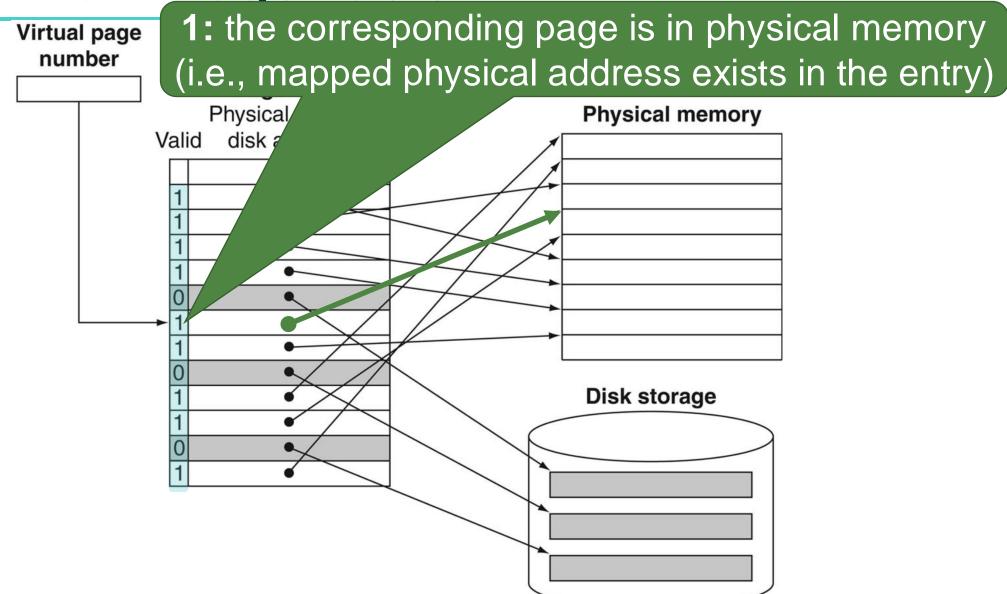


Page Table: Details Entry: Physical page number Virtual page (or disk address) number Page table #5 Physical page or Physical memory disk address Valid #0 #1 #3 #6 Disk storage #N Index: virtual page number (as offset) (+ page table base address)

Valid Bit in Page Table

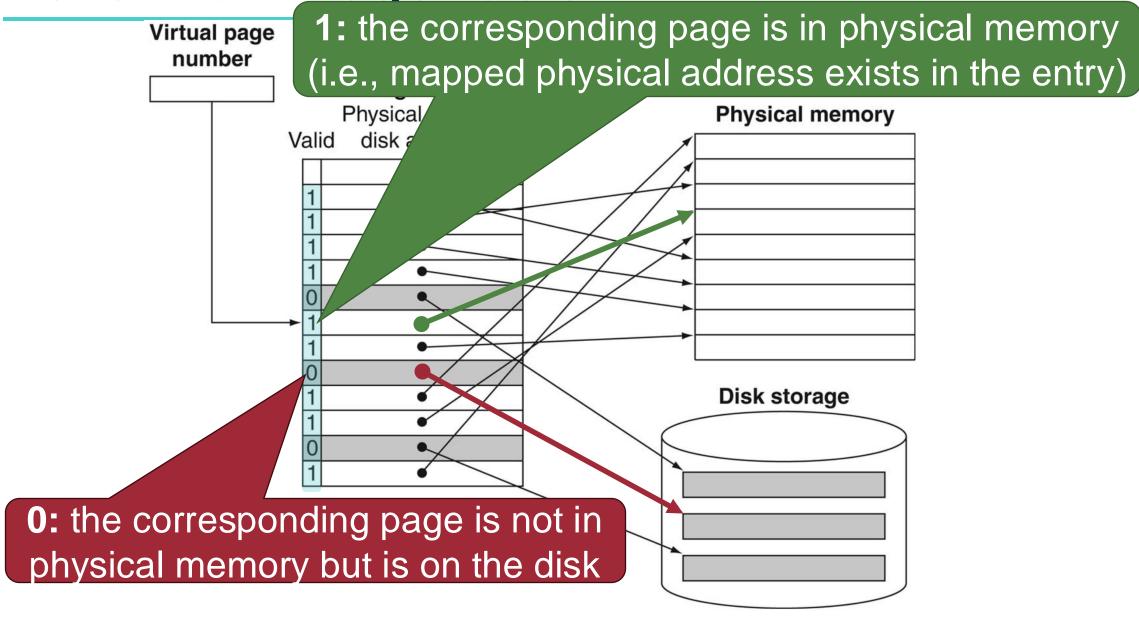


Valid Bit in Page Table



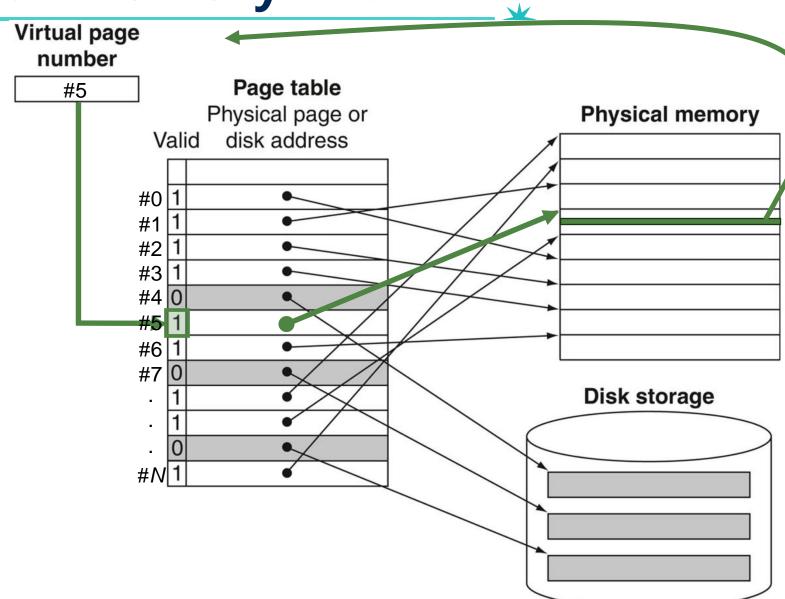




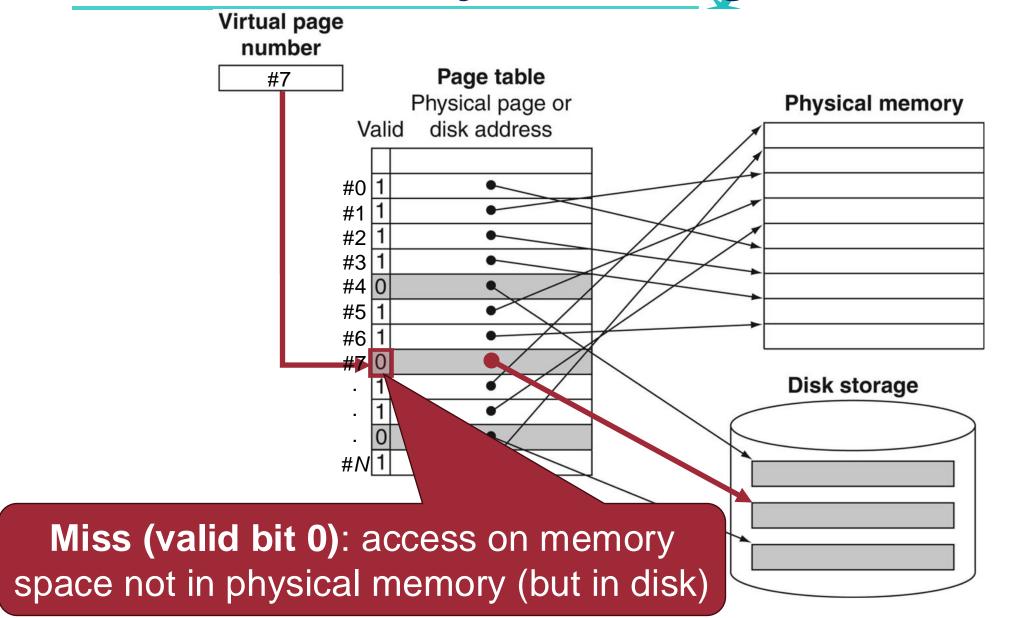


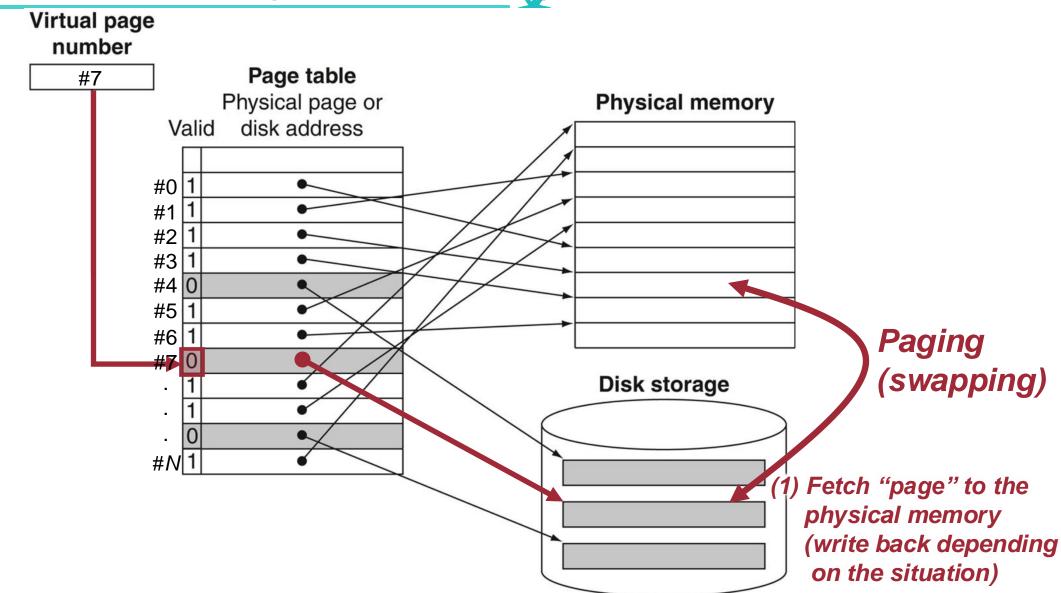


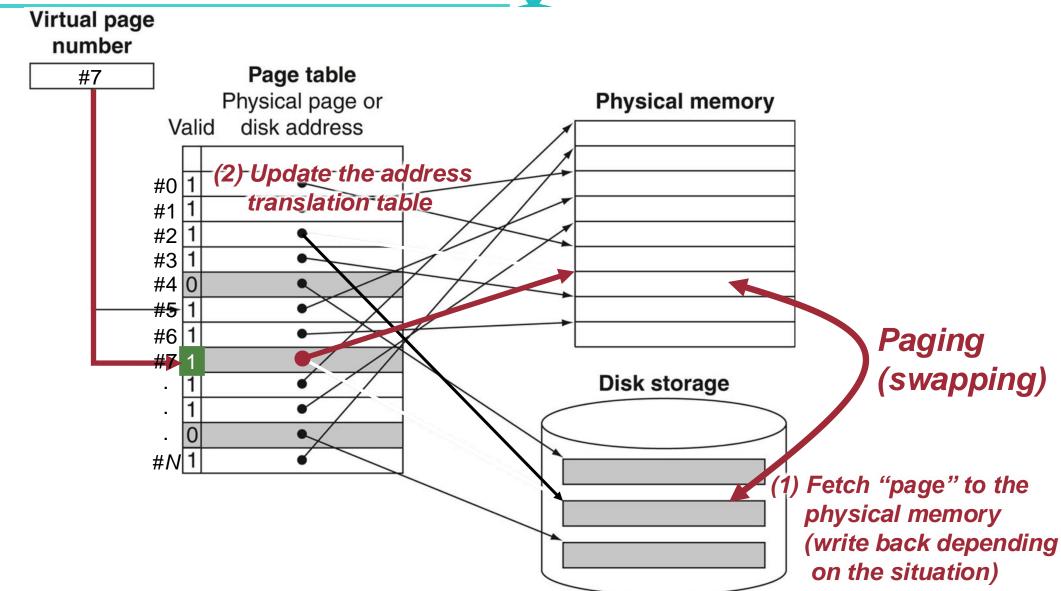
Virtual Memory Hit



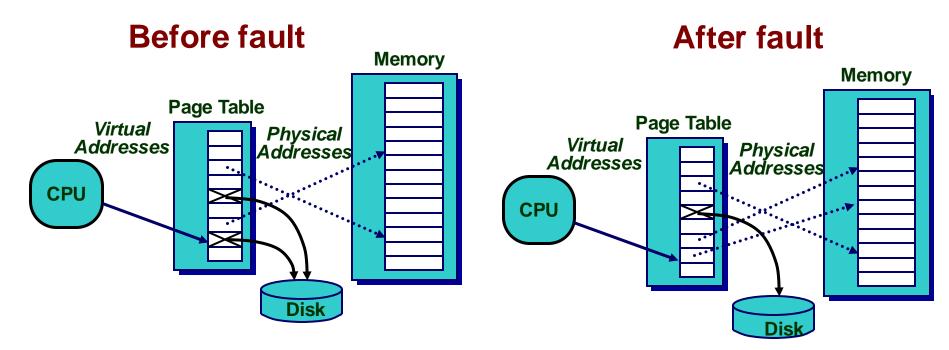
Do not need to access to the disk







- If a page is not in physical memory but disk (if valid == 0)
 - Page table entry (especially, valid bit) indicates that the page not in memory
 - Page fault exception is occurred! OS trap handler invoked to move data from disk into memory
 - OS has full control over placement!



Page Fault Penalty



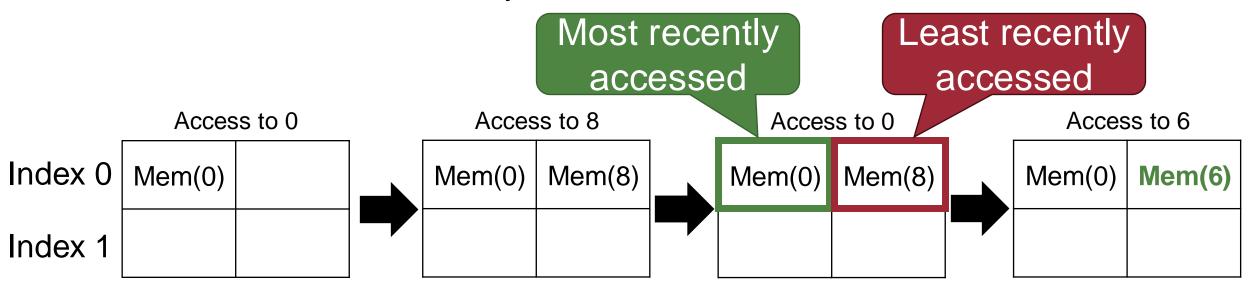
- On page fault, the page must be fetched from disk
 - Takes millions of clock cycles
- Try to minimize page fault rate and fault penalty
 - Prefer write back (write through is impractical)
 - Dirty bit in each page table entry
 - Prefer **LRU** replacement
 - Reference bit in each page table set to 1 on access to page
 - Periodically cleared to 0 by OS
 - A page with reference bit = 0 has NOT been used recently

Reference Dirty Valid Physical page number

Recap: LRU



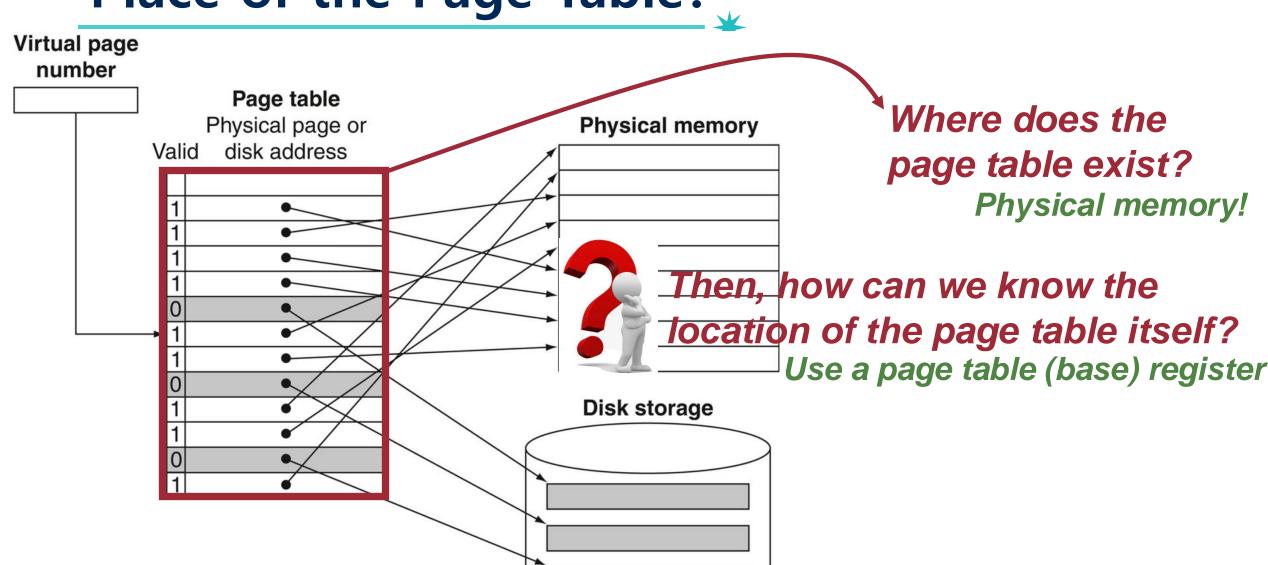
- Least Recently Used (LRU): replace the one NOT used (accessed) for the <u>longest time</u>
 - Temporal locality of access is considered
 - Need a reference history information



2-way set associative

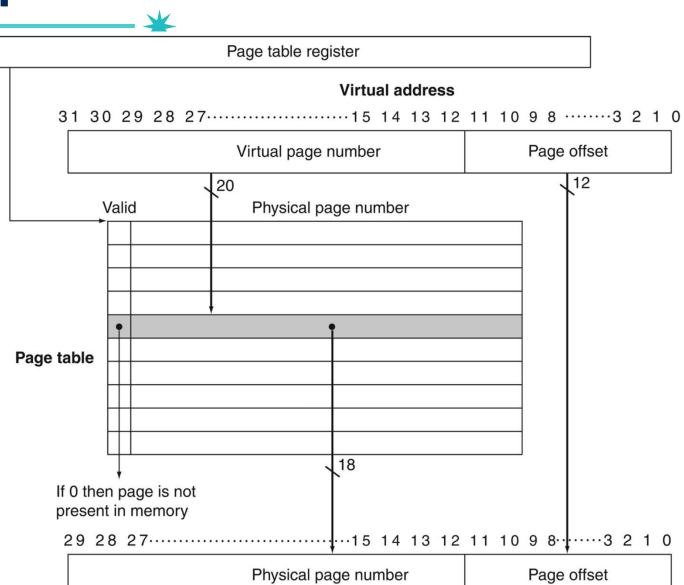






Page Table Register





Physical address

Page Table Register



Page offset

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CPU register pointing to page table in physical memory (Absolute address)

Page table register

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Virtual page number

Physical page number

Virtual address

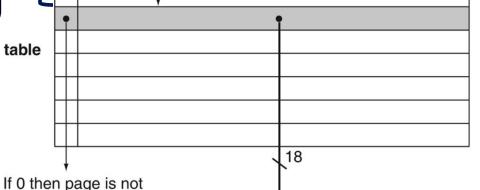
31 30 29 28 27...... 15 14 13 12 11 10 9 8 3 2 1 0

Index: value of the page table register + virtual page number

1 (20) A (20)

Page table

Valid



29 28 27...... 21 10 9 8...... 2 1 0

present in memory

Physical page number

Page offset

Physical address

Question?