

Wenlin Yi

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Education: Electrical and Electronic Engineering, MEng, Imperial College London 2019-2023

- **Relevant modules:** Programming for Engineers, Computing Architecture, Optimisation, Large Dimensional Data Processing, Machine Learning, Deep Learning, Digital System Design, Digital Signal Processing, Digital Image Processing, Signal Processing and Machine Learning for Finance.
- **A Levels, Royal Grammar School, Newcastle upon Tyne** 2016-2018
As and A1: Mathematics (A*A*), Further Mathematics (A*A), Physics (A*A), Chemistry (A)

University Projects

- **Discovering Neural Responses to Continuous Speech**, Individual Final Year Project 2022-Now
Discover the correlation of brain EEG signal and selective attended speech, by using data-driven, time series to process EEG and audio signals and to build forward and backward machine learning models.
- **Multi-Agent System Design** 2022
Organised a team of 5. Based on diverse research of MAS theory, and application to a game scenario MAS model. Built infrastructure towards fairness as the game, and soft-coded rule-based agents as players with machine learning. The players' performances increasingly outperform a highly randomised baseline model. Collaborated effectively and awarded with the highest grade.
- **FPGA Accelerated Machine Learning Projects**
 - **Mapping CNNs to FPGAs Summer Research at Imperial College London** 2022
 - Researched and benchmarked neural networks and explored edge conditions of the existing ConveNet to FPGA mapping framework on simulation. Refined the instructions and improve user experience.
 - **FPGA Accelerate Super-resolution Network with Imperial College London and ARM** 2022
 - Worked in a team of 5, made quantisation benchmark from both TensorFlow and PyTorch, increased the inference speed by 21% with less than 1% peak signal-to-noise ratio drop.
 - Individually built hardware IPs to map a parameterisable bicubic interpolation layer that is used in ESPCN super-resolution network, tool flow is suited to fit any size of video of up to 3 folds enhancement depending on hardware resource.
- **Build clock on DE10-light FPGA Board** 2020
By building fundamental blocks such as counters and registers, made a LED clock on a series of 8-segment LED on DE10-Light FPGA board for F1 games. Wrote and simulated with Verilog HDL on Quartus.
- **Analogue Music Synthesiser** 2020
Designed and synthesised a fully working market standard analogue music synthesiser deploying fundamental analogue signal processing on LTSpice by using only fundamental components. Employed unique characteristics of JFET to bring novel simplification to the ADSD stage, while maintaining qualities.

Work Experience

- **Software Intern at Jetstack** 2021
Refined and updated the use of protocol tokens for the certification manager and agents. Replaced existing infrastructure on the echo server and customer server, and improved the user's onboarding experience.
- **Undergraduate Teaching Assistant** 2021
Helped and led juniors in tackling difficult theory example problems through interactive discussions. Assisted the juniors to present and shared solutions to the year cohort and academic group.
- **JP Morgan Early Insight Program** 2021
Participated in a coding challenge and learned Java and Python basics from courses on cyber security and frontend programming. Developed sanction screening and real-time alert programs.

Skills and Interests:

- Skills: Intermediate at *System Verilog; C++, Golang, Python; PyTorch, TensorFlow; shell script; Linux, MATLAB* and Simulink, Arduino IDE; *LTSpice*.
- Language: English – Proficient, IELTSs 7.0 (2017), Chinese (Mandarin) – Native, French – Elementary.
- Clubs and societies: Imperial College Robotics Society, Chinese Debating team, Badminton and Poker Club.

Awards:

- 15th place, UKMT Senior Team Maths Challenge National Final 2017
- 1st place, UKMT Senior Team Maths Challenge National Final Poster Round: Cellular Automat 2017
- UKMT Senior Maths Individual Challenge Gold Prize 2016, Silver Prize 2017