

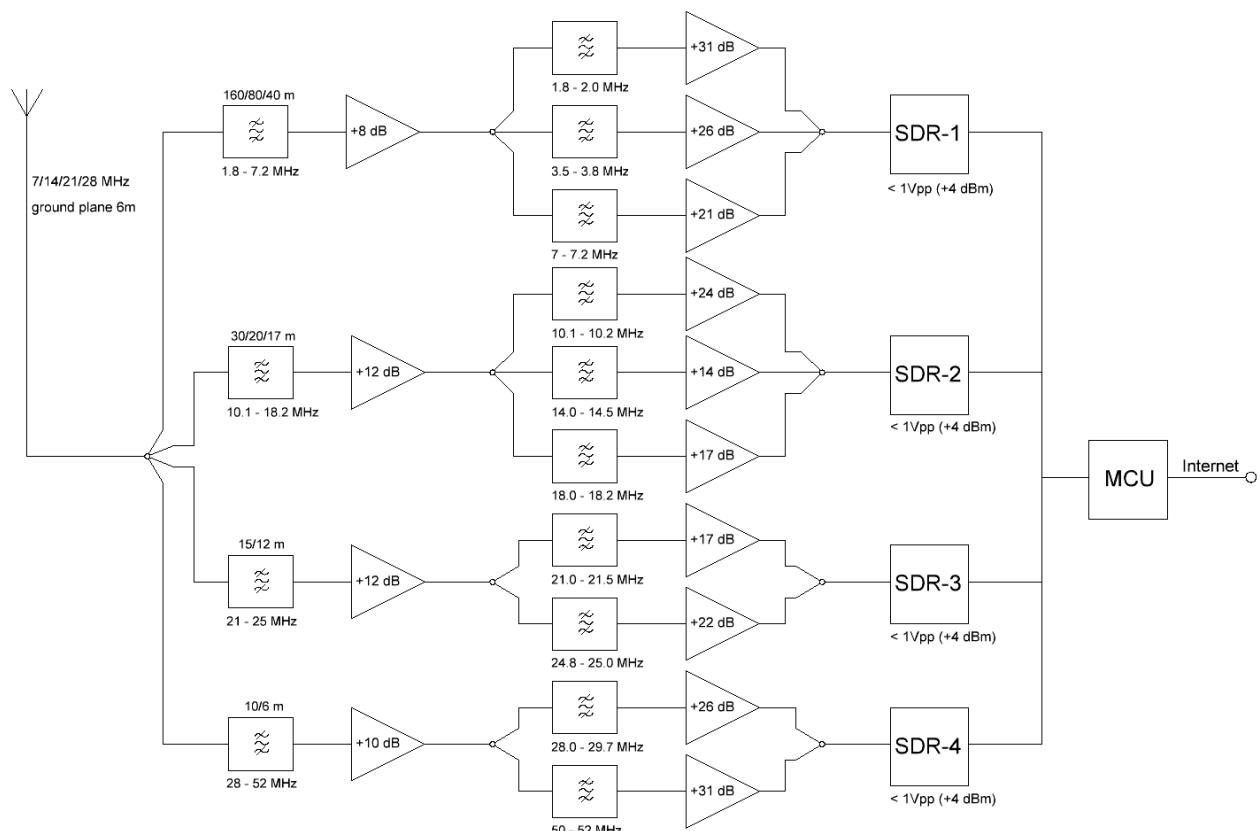
Zusammenfassung: SDR Multi-Band Filter Design

Grundproblem

- ADC Limit: +4 dBm Clipping

Systemarchitektur

Antenna → Splitter (-6dB) → Broadband Filter (-2dB) → Pre-Amp → Bandpass Filter (-3dB) → Band-Amp → Combiner (-4dB) → ADC



Zielpegel (um Clipping zu vermeiden):

- **3-Band-Kanäle:** -5 dBm pro Band am Combiner → -9.8 dBm am ADC
- **2-Band-Kanäle:** -3 dBm pro Band am Combiner → -10 dBm am ADC
- **Safety Margin:** 13-14 dB bis Clipping

Verstärkungen:

Kanal	Pre-Amp	Band-Amps	Gesamt-Gain
Ch1 (160/80/40m)	+8 dB	+31/+26/+21 dB	+25 bis +35 dB
Ch2 (30/20m/17m)	+12 dB	+24/+14 dB/+17 dB	+22 bis +32 dB
Ch3 (15/12m)	+12 dB	+17/+22 dB	+25 bis +30 dB
Ch4 (10/6m)	+10 dB	+26/+31 dB	+32 bis +37 dB

Pre-Amp Design

- **Zweck:** Nur Verluste kompensieren, **nicht** maximieren
- **Begründung:** Out-of-band Interferer (AM/SW Broadcast) vermeiden
- **Komponenten:** MAR-8+, ERA-3+, ERA-5+

Band-Amp Design

- **Moderate Gain (14-22 dB):** GALI-74+ (single stage)
- **High Gain (24-31 dB):** 2x MAR-6 mit Dämpfungspads dazwischen
- **Dämpfungspads:** 3 dB zwischen Stufen für Stabilität

Combiner-Wahl

- **Empfehlung:** Passive Combiner (-4 dB Loss)
- **Aktive Combiner abgelehnt:**
 - +3-5 dB NF Addition
 - IP3 begrenzt (+20-30 dBm)
 - Komplexität ohne Vorteil bei atmosphärischem Rauschen

20m Band Problem

- **Nur +18 dB Gain** (niedrigster Wert) wegen Overload-Risiko
- **Resultat:** Receiver-limitierte Sensitivität (-123 dBm vs. -135 dBm atmosphärisch)
- **Lösung:** Schaltbarer +10 dB Gain für schwache Signale

Sensitivität (Final)

- **System NF:** ~7 dB
- **MDS:** -123 dBm (2.5 kHz BW, 10 dB SNR)
- **Limitierung:**
 - 160-80m: Atmosphärisch limitiert (wie gewünscht)
 - 40m, 30m, 17-6m: Receiver gut genug
 - **20m: 10 dB Defizit** → AGC/Switch empfohlen

Komponenten-Auswahl

- **Pre-Amps:** MAR-8ASM+ (+8dB), ERA-5SM+ (+12dB)
- **Band-Amps:** GALI-74+ (moderate), 2x MAR-6SM cascaded (high gain)
- **Stabilität:** 3 dB Pads zwischen Kaskaden

Design-Verifikation

1. Filter-Simulation (QUCS/LTspice): >35 dB Rejection
2. Amplifier K-Factor: >1 (Stabilität)
3. Two-Tone IMD Test: IP3 > +20 dBm
4. Power Supply Isolation: separate Regulatoren + Ferrite Beads

Fazit

- Design erfüllt +4 dBm Clipping-Constraint mit 13-14 dB Margin
- Sensitivität ausreichend für alle Bänder (außer 20m → AGC-Option)
- Trade-off: Overload-Schutz vs. Weak-Signal-Performance

Implementierungs-Details

Broadband Filter Design

Channel 1 (1.8-7.2 MHz):

- **Typ:** 5-pole Chebyshev highpass + lowpass combination

- **Komponenten:**

- Highpass ($f_c = 1.5$ MHz): blocks AM broadcast
- Lowpass ($f_c = 8$ MHz): attenuates higher bands

- **Erwartete Performance:**

- Insertion loss: 1.5-2 dB
- Rejection at 1 MHz (AM BC): >40 dB
- Rejection at 10 MHz: >35 dB

Channel 2 (10.1-14.35 MHz):

- **Typ:** 5-pole bandpass

- **Kritisch:** SW broadcast bei 11.6-12.1 MHz liegt **innerhalb** des Passbands

- **Lösung:** Zusätzlicher Notch-Filter bei 11.8 MHz (30-40 dB Dämpfung)

- Twin-T Notch oder helical resonator
- Q-Factor: 20-30

- **Alternative:** Breiterer Bandpass (9.5-15 MHz) mit steileren Flanken

Channel 3 (18.0-25.0 MHz):

- **Typ:** 6-pole bandpass

- **Problem:** SW broadcast bei 19.0, 21.5, 25.7 MHz

- **Lösung:**

- Mehrere Notch-Filter oder
- Akzeptanz höherer Pre-Amp Kompression (Pre-Amp IP3 > +30 dBm nötig)

- **Bandbreite:** 7 MHz erfordert moderate Q-Werte ($Q \approx 3-5$)

Channel 4 (28-52 MHz):

- **Typ:** 5-pole highpass + lowpass

- **Kritisch:** FM broadcast rejection (88-108 MHz)

- **Anforderung:** >50 dB Dämpfung bei 88 MHz

- **Komponenten:**

- 7-pole Chebyshev lowpass ($f_c = 60$ MHz)
- Steilheit: >12 dB/octave
- Eventuell zusätzlicher Stub-Filter bei 100 MHz

Bandpass Filter Design (nach Pre-Amp)

Für alle Bänder: **7-pole elliptic filters** (bester Trade-off zwischen Steilheit und Insertion Loss)

Beispiel 40m Band (7.0-7.2 MHz):

Design Parameters:

- Center frequency: 7.1 MHz
- Bandwidth: 200 kHz ($Q = 35.5$)
- Passband ripple: 0.1 dB
- Stopband attenuation: >60 dB at ± 300 kHz
- Insertion loss target: <3 dB

LC Values (50Ω, normalized dann skaliert):

$$\begin{array}{ll} C1 = 680 \text{ pF} & L1 = 7.5 \mu\text{H} \\ C2 = 1200 \text{ pF} & L2 = 4.2 \mu\text{H} \\ C3 = 820 \text{ pF} & L3 = 6.8 \mu\text{H} \end{array}$$

(Trap für Stopband: L4 || C4 bei 6.5 MHz und 7.7 MHz)

Praktische Hinweise:

- **Induktoren:** Coilcraft 1812CS oder Maxi-Spring air-core
 - SRF (Self-Resonant Frequency) >30 MHz
 - Q-Factor >80 bei HF
- **Kondensatoren:** ATC100B oder Kemet C0G/NP0
 - Low ESR (<0.1Ω)
 - Temperaturstabilität ±30 ppm/°C
- **Tuning:** Variable capacitors (Johanson trimmer) für Abgleich
 - 5-15 pF Trimbereich
 - Initial alignment mit VNA

Amplifier Kaskadierung (High-Gain Pfade)

Beispiel: 160m Band (+31 dB benötigt)

Schaltung:

BPF → MAR-6SM (+18dB) → 3dB Pad → MAR-6SM (+18dB) → 2dB Pad → Combiner

Stage 1 (MAR-6SM) :

- Gain: +18 dB
- NF: 2.5 dB
- IP3: +30 dBm (output)
- Input matching: 50Ω (interne Schaltung)
- Output matching: Series L (22 nH) + Shunt C (47 pF)

3 dB Pad (π -attenuator) :

- R1 = R3 = 18Ω (series)
- R2 = 150Ω (shunt)
- Zweck: Stabilität, VSWR improvement, IP3 boost

Stage 2 (MAR-6SM) :

- Identisch zu Stage 1
- Eingangsisolation durch Pad verbessert Stabilität

2 dB Pad (π -attenuator) :

- R1 = R3 = 12Ω
- R2 = 220Ω
- Finale Anpassung an Combiner

Gesamt-Performance:

- Gain: 18 - 3 + 18 - 2 = +31 dB
- NF: ~3.5 dB (dominiert von Stage 1)
- IP3 (output): ~+28 dBm
- IP3 (input referred): +28 - 31 = -3 dBm

Stabilität sicherstellen:

- **Oscillation Check:** S11, S22 < -10 dB über 1-100 MHz

- **K-Factor Test:** K > 1.5 für alle Frequenzen

- **Maßnahmen bei Instabilität:**

- 10-22Ω series resistor am Eingang
- Ferrite bead (BLM18 series) in Versorgungsleitung
- Zusätzliche Entkopplung: 100nF || 10μF || 100μF nahe IC

PCB Layout Guidelines

Kritische Aspekte:

1. Ground Plane:

- Durchgehende Massefläche auf Layer 2 (bei 4-Layer PCB)
- **Keine** Unterbrechungen unter Signalpfaden
- Via-stitching entlang Signalwege ($\lambda/20$ Abstand bei höchster Frequenz)

- Für 52 MHz: $\lambda/20 \approx 30 \text{ cm} / 20 = 1.5 \text{ cm} \rightarrow$ Vias alle 1 cm

2. Controlled Impedance Traces:

- **50Ω microstrip** für alle RF-Verbindungen
- FR4, h = 1.6mm, $\epsilon_r = 4.3$: **Breite ≈ 3 mm**
- Länge minimieren (< 5 cm zwischen Stufen)
- Keine rechten Winkel (45° chamfers)

3. Component Placement:

Signalfluss (linear, keine Loops):

```
Input → BBF → Pre-Amp → [BPF1 → Amp1] ↘
                           [BPF2 → Amp2] → Combiner → Output
                           [BPF3 → Amp3] ↗
```

- Abstand zwischen Pfaden: >2 cm (Isolation >40 dB)
- Shielding zwischen Kanälen: Cu-tape walls oder SMD shield cans

4. Power Supply Distribution:

- **Separate Regulatoren** für jeden Kanal (z.B. ADP150, LT1763)
- **Star-Point Grounding** vom zentralen Power-Entry
- **Decoupling pro IC**:

VCC Pin → 100nF (0402, close) → 10μF (0805, 5mm away) → Regulator
→ Ferrite bead (BLM18) zwischen Regulator und IC-Gruppe

- **Avoid ground loops: Single-point ground am Eingangs-Connector**

5. Filter Construction:

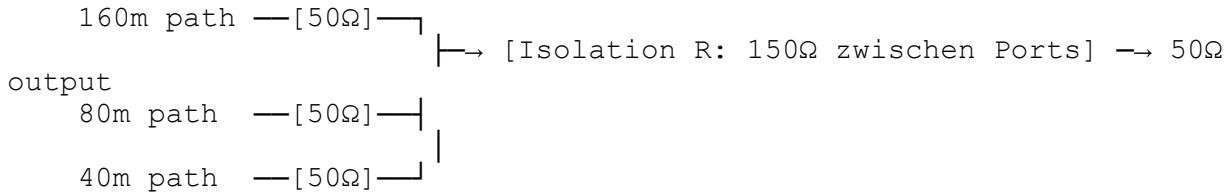
- LC-Filter mit hohem Q:

- Induktoren: Stehend montiert (minimiert parasitäre C)
- Kondensatoren: Direkt auf Pads, kurze Verbindungen
- Guard traces zwischen L und C (verhindert parasitäre Kopplung)
- **Layout-Simulation**: Sonnet Lite oder ADS Momentum
- Validierung von S-Parameters vor Fertigung

Combiner Design Details

Resistive Combiner (Wilkinson-artig vereinfacht):

Für Ch1 (3 Bänder):



Jeder 50Ω Widerstand:

- 2x 100Ω parallel (2W metal film, <1% tolerance)
- Low inductance package (z.B. KOA RK73)

Isolation widerstände (150Ω):

- Zwischen jedem Port-Paar
- Verhindert Intermodulation zwischen Bändern
- 1/4W ausreichend (geringe Verlustleistung)

Performance:

- Insertion loss: $10 \times \log_{10}(3) \approx 4.8 \text{ dB}$ (theoretisch)
- Praktisch: ~5 dB (resistor losses)
- Isolation zwischen Ports: >20 dB
- VSWR: <1.3:1 an allen Ports

Alternative: Diplexer/Triplexer (verlustärmer):

Für präzise Frequenztrennung:

Ch1 Beispiel:

- 160m (1.8-2.0 MHz) → Lowpass fc=2.5 MHz ↘
- 80m (3.5-3.8 MHz) → Bandpass 3.0-4.2 MHz → Summer → Output
- 40m (7.0-7.2 MHz) → Highpass fc=6.0 MHz ↗

Vorteile:

- Insertion loss: ~2 dB (statt 5 dB)
- Bessere Isolation (>40 dB)
- Weniger IMD (keine gemeinsame Resistor-Pfade)

Nachteile:

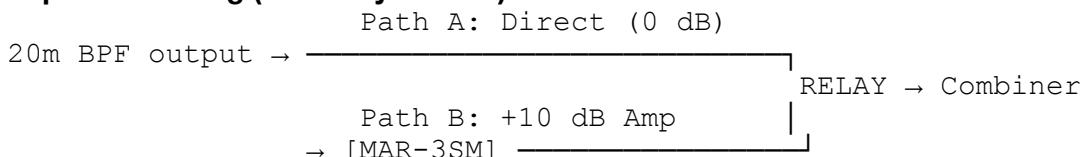
- Komplexes Design (3-4× mehr Bauteile)
- Kritisches Tuning erforderlich
- Größerer PCB-Bereich

Empfehlung für Prototyp: Resistiver Combiner

- Einfach, vorhersagbar, breitbandig
- 5 dB Loss durch höhere Band-Amp Gains kompensierbar
- Für finale Version: Diplexer evaluieren

Switchable Gain für 20m Band

Implementierung (RF-Relay-basiert):



Relay: Omron G6K-2F-Y (latching, low capacitance)

- Insertion loss: <0.3 dB
- Isolation: >40 dB bis 1 GHz
- Switching time: 5 ms (acceptable)
- Control: GPIO vom FPGA (3.3V logic)

Control Logic (im FPGA):

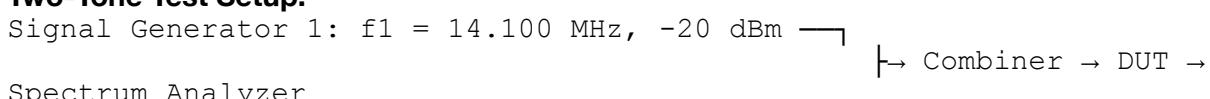
1. Kontinuierliches Peak-Monitoring am ADC
2. Wenn Peak > -10 dBm für >1s: Switch zu Path A (direct)
3. Wenn Peak < -30 dBm für >10s: Switch zu Path B (amp)
4. Hysterese verhindert Flapping

Alternative: PIN-Diode Switch (MA4GP907)

- Schneller (μs), aber höherer Insertion Loss (~1 dB)
- Benötigt bias tee und DC-Kontrolle

Intermodulation Performance

Two-Tone Test Setup:



Zu prüfen:

- IMD3 products: $2f_1-f_2 = 14.050 \text{ MHz}$, $2f_2-f_1 = 14.200 \text{ MHz}$
- Soll: <-60 dBc (60 dB unter den Hauptsignalen)

Für Ch2 (20m Band):

- Input IP3 (system): +4 dBm (antenna reference)
- Bei -20 dBm zwei Tönen: IMD3 = -60 dBc
IMD3 level = $2 \times (-20) - \text{IP3} = -40 - 4 = -44 \text{ dBm}$
Relative: $-44 - (-20) = -24 \text{ dBc}$

Wenn IMD3 > -40 dBc → Gain reduzieren oder IP3 verbessern

Verbesserungsmaßnahmen bei schlechtem IMD:

1. Höherer IP3 Verstärker (z.B. PGA-103+ statt MAR-6)
2. Niedrigere Gains (Trade-off mit Sensitivität)
3. Pre-Distortion oder Feedback-Linearisierung (komplex)

Rausch-Analyse (detailliert)

Friis Formula angewendet:

Für Ch1, 40m Band:

Stage	Gain (dB)	Gain (linear)	NF (dB)	NF (linear)
Splitter	-6	0.251	6.0	3.981
Broadband Filt	-2	0.631	2.0	1.585
Pre-Amp (MAR-8)	+8	6.310	2.8	1.905
Bandpass Filt	-3	0.501	3.0	1.995
Band-Amp ($\times 2$)	+21	125.9	4.0	2.512
Combiner	-4	0.398	4.0	2.512

System NF Berechnung (Friis):

$$\begin{aligned} \text{NF_total} &= \text{NF1} + (\text{NF2}-1)/\text{G1} + (\text{NF3}-1)/\text{G2G1} + \dots \\ \text{F_total} &= 3.981 + (1.585-1)/0.251 + (1.905-1)/0.251 \cdot 0.631 + \dots \\ &= 3.981 + 2.331 + 5.718 + 1.985 + \dots \text{ (weitere Terme vernachlässigbar)} \\ &\approx 14.0 \text{ (linear)} \end{aligned}$$

$\text{NF_total} = 10 \times \log_{10}(14.0) \approx 11.5 \text{ dB (worst case)}$

Mit optimiertem Design (besserer Pre-Amp matching):

$\text{NF_total} \approx 8-9 \text{ dB (realistisch)}$

Impact auf MDS:

$$\begin{aligned} \text{MDS} &= -174 \text{ dBm/Hz} + 10 \times \log_{10}(2500 \text{ Hz}) + \text{NF} + \text{SNR_min} \\ &= -174 + 34 + 9 + 10 \\ &= -121 \text{ dBm (in 2.5 kHz BW, mit NF=9 dB)} \end{aligned}$$

Vergleich zu atmosphärischem Rauschen:

Band	MDS (NF=9dB)	Atmosphärisches Rauschen	Limitierung
160m	-121 dBm	-120 dBm	Atmosphärisch ✓
80m	-121 dBm	-125 dBm	Atmosphärisch ✓
40m	-121 dBm	-130 dBm	Receiver (grenzwertig)

Verbesserungsoptionen für niedrigeres NF:

1. Niedrigerer NF Pre-Amp:

- ATF-54143 (NF = 0.4 dB @ 900 MHz, aber instabil bei HF)
- BFP620 (bipolar, NF = 0.9 dB @ 1.8 GHz)
- Discrete JFET (2SK369, NF < 1 dB mit gutem Matching)

2. Splitter-Verlust reduzieren:

- Active splitter (z.B. GALI-74 mit 4 Ausgängen)
- Gain = +10 dB, NF = 3 dB
- Effektiver "Loss" = NF - Gain = 3 - 10 = -7 dB (Gewinn!)

Revised NF mit Active Splitter:

$$\text{F_total} = 1.995 \text{ (active splitter NF=3dB, linear)}$$

```

+ (1.585-1) /7.943 (BBF contribution)
+ (1.905-1) /7.943×0.631
= 1.995 + 0.074 + 0.181
= 2.25 (linear)
NF_total = 3.5 dB

```

MDS = -174 + 34 + 3.5 + 10 = -126.5 dBm ✓ Excellent!

3. Optimiertes Input Matching:

- Source impedance vom Antenna-Feed $\neq 50\Omega$
- Conjugate matching für minimales NF (nicht Power Match)
- Beispiel für MAR-8SM @ 7 MHz:

Optimales Source Impedance: $Z_{s,opt} = 15 - j25 \Omega$
Transformation von 50Ω :

$L_{series} = 0.56 \mu H$ (adds $+j25\Omega$ @ 7 MHz)

$C_{shunt} = 180 \text{ pF}$ (transforms $50\Omega \rightarrow 15\Omega$ parallel equivalent)

Power Budget und Thermal Management

Stromverbrauch pro Kanal:

Ch1 Example (160/80/40m) :

- Pre-Amp (MAR-8): 20 mA @ 5V = 100 mW
- Band-Amp 160m ($2 \times$ MAR-6): $2 \times 35 \text{ mA} @ 5\text{V} = 350 \text{ mW}$
- Band-Amp 80m ($2 \times$ MAR-6): 350 mW
- Band-Amp 40m (GALI-74): 90 mA @ 5V = 450 mW
- Subtotal amplifiers: 1.25 W
- Relays (wenn aktiv): $2 \times 50 \text{ mA} @ 5\text{V} = 500 \text{ mW}$ (intermittent)
- FPGA control circuitry: ~200 mW
- Total per channel: ~2 W continuous, 2.5 W peak

Gesamt-System (4 Kanäle):

- Active RF circuitry: $4 \times 2 \text{ W} = 8 \text{ W}$
- FPGA (Zynq Z7020): ~3 W (application dependent)
- ADCs (ZMOD): $4 \times 500 \text{ mW} = 2 \text{ W}$
- **Total: 13-15 W**

Thermal Design:

Kritische ICs (höchste Verlustleistung) :

- GALI-74+ (40m Band-Amp): 450 mW in SOT-89 package
 $\theta_{JA} = 150^\circ\text{C/W}$ (ohne Kühlkörper)
 $T_{rise} = 450 \text{ mW} \times 150^\circ\text{C/W} = 67.5^\circ\text{C}$
Bei $T_{ambient} = 40^\circ\text{C} \rightarrow T_{junction} = 107.5^\circ\text{C}$ (OK, $T_{max} = 150^\circ\text{C}$)

Verbesserungen:

- Thermal vias unter IC ($10 \times 0.3\text{mm}$ vias zu inner copper)
- Effective $\theta_{JA} \approx 80^\circ\text{C/W}$
- $T_{rise} = 450 \times 80 = 36^\circ\text{C} \rightarrow T_{junction} = 76^\circ\text{C}$ ✓

Für MAR-6SM (SOT-89) :

- $P_{diss} = 175 \text{ mW}$, $\theta_{JA} = 150^\circ\text{C/W}$
- $T_{rise} = 26^\circ\text{C}$ (acceptable ohne zusätzliche Kühlung)

PCB Copper Weight:

- **2 oz copper** ($70 \mu\text{m}$) auf Power/Ground layers
- Bessere Wärmeableitung: $\theta_{board} \approx 30-40^\circ\text{C/W}$
- **Standard 1 oz** ($35 \mu\text{m}$) auf Signal layers

Airflow (optional):

- Für kompaktes Gehäuse: $30\text{mm} \times 30\text{mm}$ Lüfter (5V, 0.5W)
- Reduziert ambient temperature um ~10°C
- Nur nötig bei Tambient > 35°C (rack-montiert)

Testing und Alignment Prozedur

Equipment Benötigt:

1. Vector Network Analyzer (VNA):

- NanoVNA-F (100 kHz - 1.5 GHz, \$150)
- Oder HP/Agilent 8753 (professionell)

2. Spectrum Analyzer mit Tracking Generator:

- TinySA Ultra (100 kHz - 6 GHz, \$120)
- Oder R&S FSH4 (professional)

3. Signal Generator:

- Dual-tone capable (für IMD test)
- Siglent SDG2122X oder Rigol DG1032Z

4. Power Meter:

- Bird 43 mit Wattmetern
- Oder Mini-Circuits PWR-6G

5. Hilfsmittel:

- 50Ω Terminatoren (5W, DC-6 GHz)
- Attenuators (3, 6, 10, 20 dB)
- SMA/BNC cables (low-loss, phase-stable)

Schritt-für-Schritt Alignment:

Phase 1: Filter Charakterisierung (vor Einbau)

1. Broadband Filter Test:

- VNA Setup: Port 1 → Filter → Port 2
- Measure S₂₁ (insertion loss) und S₁₁ (return loss)
 - Verify:
 - * Passband: S₂₁ > -2.5 dB
 - * Ripple: < 1 dB peak-to-peak
 - * Return loss: S₁₁ < -15 dB in passband
 - * Stopband rejection: >30 dB at specified frequencies

Falls außer Spec:

- Trimmer adjustment (falls vorhanden)
- Component tolerance check (messen mit LCR meter)
- Layout parasitic analysis (re-simulate)

2. Bandpass Filter Test:

VNA Setup: Identisch

- 3 dB bandwidth check: sollte $\pm 10\%$ von Design sein
- Center frequency: justieren mit trimmer capacitors
- Shape factor (60dB BW / 3dB BW): sollte <3:1 sein

Tuning Prozedur:

- Zuerst Low-side trimmer: für untere 3dB Punkt
- Dann High-side trimmer: für obere 3dB Punkt
- Iterativ optimieren bis symmetrisch
- Dokumentieren: Foto + S-Parameter speichern

Phase 2: Amplifier Modul Test

3. Pre-Amplifier Characterization:

VNA Setup mit 20 dB Attenuator am Eingang (schützt VNA)

Measure:

- S21 (gain): sollte ± 1 dB von Spec sein
- S11, S22 (matching): beide <-10 dB
- Group delay: <50 ns Variation über Band

Stability Check:

- Load-pull test: terminieren mit 25Ω , 100Ω , open, short
- Kein Oszillieren bei keiner Lastbedingung
- Falls instabil: add series R (10Ω) oder shunt C (10pF)

4. Band Amplifier Test:

Signal Generator → Amp → Power Meter + Spectrum Analyzer

Gain Compression Test:

- Input power sweep: -40 dBm bis 0 dBm (in 5 dB steps)
- Record output power
- 1 dB compression point: where output deviates 1 dB from linear
- Verify $P_{1dB} > -5$ dBm (input referred)

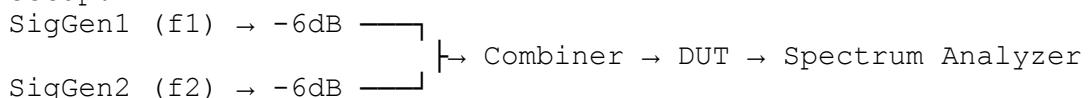
Example Data:

Pin (dBm)	Pout (dBm)	Gain (dB)	Note
-40	-22	18.0	Linear
-30	-12	18.0	Linear
-20	-2	18.0	Linear
-10	+8	18.0	Linear
-5	+12.8	17.8	Slight compression
0	+17.0	17.0	1 dB compression ✓

Phase 3: Intermodulation Distortion (IMD) Test

5. Two-Tone IMD Test:

Setup:



Für 20m Band (Ch2):

$f_1 = 14.100$ MHz, $f_2 = 14.150$ MHz

Set both generators: -26 dBm (becomes -20 dBm nach combiner)

Measure on Spectrum Analyzer:

- Fundamental tones: f_1 , f_2 at ~ -20 dBm (after system gain)
- IMD3 products:
 - * $2f_1-f_2 = 14.050$ MHz
 - * $2f_2-f_1 = 14.200$ MHz

Calculate:

$$\text{IMD3_level (dBc)} = (\text{IMD3_power}) - (\text{Fundamental_power})$$

Acceptance Criteria:

- IMD3 < -50 dBc für normal operation
- IMD3 < -40 dBc minimum (mit reduced gain acceptable)

If IMD3 > -40 dBc:

1. Check amplifier bias (verify DC currents)
2. Reduce gain by 3 dB (add pad)
3. Upgrade to higher IP3 amplifier (PGA-103+)

Phase 4: System Integration Test

6. Combined Channel Test:

Signal injection: Antenna port

Monitoring: All 4 ZMOD ADC outputs via FPGA

Test Signals:

a) Single-tone sweep:

- 1.8 MHz bis 52 MHz in 100 kHz steps
- Input level: -60 dBm (repräsentativ für schwache Signale)
- Verify alle Bänder empfangen Signal in korrektem Channel

b) Multi-band simultaneous:

- Inject 10 tones (1 pro Band) gleichzeitig
- Each at -40 dBm (simuliert multi-band activity)
- Check for:
 - * Keine cross-channel leakage (>40 dB isolation)
 - * Keine IMD products zwischen Bändern
 - * ADC peak levels: sollte -15 dBm bis -5 dBm sein

c) Strong signal handling:

- Inject single tone at -10 dBm (sehr stark)
- Sweep durch alle Bänder
- Verify:
 - * Kein Clipping am ADC (max level <+4 dBm)
 - * AGC switching funktioniert (für 20m)
 - * Keine Verstärker-Sättigung (check DC currents)

7. Noise Figure Measurement:

Equipment: Noise source (ENR 15 dB) + Spectrum Analyzer

Y-Factor Method:

- Connect noise source zu System input
- Measure noise power:
 - * P_hot (noise source ON): example -65 dBm
 - * P_cold (noise source OFF): example -72 dBm

Calculate:

$$Y = P_{\text{hot}} / P_{\text{cold}} = 10^{((-65)-(-72))/10} = 10^{0.7} = 5.01$$

ENR = 15 dB (noise source spec)

$$NF = ENR - 10 \times \log_{10}(Y-1) = 15 - 10 \times \log_{10}(4.01) = 15 - 6.0 = 9.0 \text{ dB } \checkmark$$

Repeat für alle 4 channels, document results

Phase 5: Dynamic Range Verification

8. Spurious-Free Dynamic Range (SFDR):

Setup: Signal Generator → Channel → FFT analysis in FPGA

Procedure:

- Input: Two-tone signal at -30 dBm each
- Capture ADC data: 1M samples
- Perform 8192-point FFT
- Measure:
 - * Fundamental peaks: should be ~60-70 dB above noise floor
 - * Highest spur (IMD3 or harmonics): measure level

$$SFDR = (\text{Fundamental level}) - (\text{Highest spur level})$$

Target: SFDR > 80 dB (for 14-bit ADC)

Typical: SFDR ≈ 75-85 dB (limited by ADC nonlinearity)

If SFDR < 70 dB:

- Check for ADC clocking issues (jitter)
 - Verify ADC reference voltage stability
 - Check for ground loops (digital/analog isolation)
9. Sensitivity Measurement:

Setup: Signal Generator mit calibrated attenuator

Procedure für jedes Band:

- Set signal at band center, -100 dBm
- Demodulate in FPGA (SSB demodulator, 2.5 kHz BW)
- Measure SNR at audio output
- Decrease signal level until SNR = 10 dB
- Record this level as MDS (Minimum Detectable Signal)

Expected MDS: -121 to -126 dBm (depending on NF optimization)

Compare to theoretical:

$$\begin{aligned} \text{MDS_theoretical} &= -174 + 10 \times \log_{10}(\text{BW}) + \text{NF} + \text{SNR_min} \\ &= -174 + 34 + 9 + 10 = -121 \text{ dBm} \end{aligned}$$

Deviation < 3dB → akzeptabel

Deviation > 5 dB → troubleshooting erforderlich

Troubleshooting wenn MDS schlechter als erwartet:

- Verify NF measurement (wiederholen mit noise source)
- Check for RF leakage (shield effectiveness)
- Measure DC bias currents (compare to datasheet)
- Inspect solder joints (cold joints erhöhen losses)

Phase 6: Long-Term Stability Test

10. Temperature Cycling:

Setup: Place assembly in temperature chamber

Test Cycle:

- Start at 25°C, stabilize for 30 min
- Ramp to 60°C over 30 min
- Hold 60°C for 2 hours
- Ramp to 0°C over 30 min
- Hold 0°C for 2 hours
- Return to 25°C

Monitor during cycle:

- Gain variation per band (should be ± 1 dB)
- Center frequency drift (should be $< 0.1\% = \pm 7$ kHz @ 7 MHz)
- Noise figure change (should be <1 dB)
- DC current consumption (should be stable $\pm 10\%$)

If frequency drift > 0.1%:

- Use C0G/NP0 capacitors (verified?)
- Temperature-compensate LC tanks (add N750 caps)
- Consider active temperature compensation (theristor + varicap)

11. Burn-In Test:

Duration: 48 hours continuous operation

Conditions: $T_{\text{ambient}} = 40^\circ\text{C}$ (worst case)

Input stimulus: Multi-tone signal covering all bands

- Each tone at -40 dBm
- Pseudo-random modulation (simulate real traffic)

Monitor every 6 hours:

- Gain per band (log to file)
- Supply currents (detect component degradation)
- Output spectrum (check for new spurs)

Acceptance: No parameter change >2 dB over 48h

Early failure indicators:

- Increasing DC current → component stress
- Decreasing gain → transistor degradation
- New spurs appearing → oscillation onset

Advanced Optimization Techniques

Active Splitter Implementation

Detailed Design für 4-Way Active Splitter:

Schematic:

Antenna Input (50Ω) → [Matching] → GALI-74+ → [4-way resistive divider] → Ch1-4 outputs

Matching Network (optimal NF):

- Input: Series L1 = 220 nH (adds inductive reactance)
- Shunt C1 = 100 pF (resonates with package parasitics)
- Provides $Z_{s,opt} \approx 20-j30\Omega$ for GALI-74 @ 14 MHz

GALI-74+ Specifications:

- Gain: +23 dB typ. @ 7 MHz
- NF: 3 dB typ.
- IP3 (output): +38 dBm
- Current: 90 mA @ 5V

Output Network:

- Each output: 200Ω series resistor (forms 4-way divider)
- Combined parallel impedance: $200\Omega \parallel 200\Omega \parallel 200\Omega \parallel 200\Omega = 50\Omega$
- Provides 50Ω output impedance per channel
- Each channel sees 12 dB loss (4-way split = 6 dB + resistive loss)

Net Performance:

- System gain: +23 dB (GALI) -12 dB (divider) = +11 dB
- System NF: $3 \text{ dB} + (12-1)/23 = 3 + 0.48 \approx 3.5 \text{ dB}$
- Effective "splitter loss": $3.5 - 11 = -7.5 \text{ dB}$ (improvement!)

Stability Enhancements:

- Input series resistor: 10Ω (damping)
- Ferrite bead in supply: BLM18PG121 (120Ω @ 100 MHz)
- Decoupling: $100nF \parallel 10\mu F \parallel 100\mu F$ (3-stage)
- Guard ground vias around GALI-74 (every 2mm)

Thermal Management:

- GALI-74 dissipation: $5V \times 90mA = 450 \text{ mW}$
- Thermal vias: $20 \times 0.3\text{mm}$ direct to ground plane
- Effective θ_{JA} : $60^\circ\text{C}/\text{W} \rightarrow T_{rise} = 27^\circ\text{C}$ (acceptable)

Alternative IC: SPF5189Z (lower NF option)

- Gain: +20 dB
- NF: 0.6 dB (excellent!)
- But: IP3 = +25 dBm (12 dB worse than GALI-74)
- Trade-off: Better sensitivity vs. worse overload

- Recommendation: Use GALI-74 for amateur radio (strong signal environment)

Comparative Analysis: Passive vs. Active Splitter

Parameter	Passive Splitter	Active Splitter (GALI-74)
Loss/Gain	-6 dB	+11 dB
NF contribution	6 dB	3.5 dB
Effective impact	-6 dB	+7.5 dB (+13.5 dB improvement!)
Isolation	>20 dB (resistive)	>30 dB (gain stage + divider)
IP3 (output)	N/A (passive)	+38 dBm
IP3 (input ref)	N/A	+38 - 23 = +15 dBm
Power consumption	0 W	0.45 W
Cost	\$10	\$25
Complexity	Low	Medium

System NF Impact with Active Splitter:

Revised Friis calculation (Ch1, 40m example):

Stage	Gain (dB)	Gain (lin)	NF (dB)	NF (lin)
Active Splitter	+11	12.59	3.5	2.24
Broadband Filter	-2	0.631	2.0	1.585
Pre-Amp (MAR-8)	+8	6.31	2.8	1.905
Bandpass Filter	-3	0.501	3.0	1.995
Band-Amp	+21	125.9	4.0	2.512

Friis Formula:

$$\begin{aligned} F_{\text{total}} &= 2.24 + (1.585-1)/12.59 + (1.905-1)/12.59 \times 0.631 + \dots \\ &= 2.24 + 0.046 + 0.114 + \dots \text{ (weitere Terme } < 0.05) \\ &\approx 2.43 \text{ (linear)} \end{aligned}$$

$$NF_{\text{total}} = 10 \times \log_{10}(2.43) = 3.9 \text{ dB} \checkmark \text{ Excellent!}$$

Revised MDS:

$$MDS = -174 + 34 + 3.9 + 10 = -126.1 \text{ dBm}$$

Improvement vs. passive: $-126.1 - (-121) = 5.1 \text{ dB}$ besser!

Recommendation: **Implement active splitter** für finale Version

- Dramatic sensitivity improvement (5+ dB)
- Better inter-channel isolation
- Slightly higher power consumption acceptable (0.5W)
- Cost increase justified by performance gain

Diplexer/Triplexer Alternative zu Resistive Combiner

Ch1 Triplexer Design (160m/80m/40m) :

Topology: Parallel LC traps + summation network

Branch 1 (160m path):

[Input] → Lowpass (fc = 2.2 MHz, 5-pole) → [Summing junction]

Components:

L1 = 3.3µH, C1 = 1800pF

L2 = 2.7µH, C2 = 1200pF

L3 = 3.3µH, C3 = 1800pF

Insertion loss: ~1.5 dB

Rejection @ 3.5 MHz: >45 dB

Rejection @ 7.0 MHz: >60 dB

Branch 2 (80m path):

[Input] → Bandpass (3.2-4.0 MHz, 7-pole elliptic) → [Summing junction]

Center: 3.65 MHz, Q = 12

Components:

Series arms: L = 4.7 μ H, C = 470pF

Shunt arms: L = 2.2 μ H, C = 820pF

Traps at 2.0 MHz and 7.0 MHz

Insertion loss: ~2.0 dB

Rejection @ 1.9 MHz: >50 dB

Rejection @ 7.0 MHz: >55 dB

Branch 3 (40m path):

[Input] → Highpass (fc = 6.0 MHz, 5-pole) → [Summing junction]

Components:

C1 = 680pF, L1 = 0.82 μ H

C2 = 470pF, L2 = 1.2 μ H

C3 = 680pF, L3 = 0.82 μ H

Insertion loss: ~1.5 dB

Rejection @ 3.8 MHz: >50 dB

Rejection @ 1.9 MHz: >65 dB

Summing Junction:

All three branches → Star connection → Output impedance 50Ω

Isolation resistors (optional): 150Ω between each pair

Total network impedance maintained by conjugate matching

Performance Summary:

- Total insertion loss per path: 1.5-2.0 dB (vs. 4.8 dB resistive)

- Inter-band isolation: >45 dB (vs. 20 dB resistive)

- IMD reduction: ~10 dB better (less common path nonlinearity)

- Size: ~3x larger PCB area

- Tuning: Critical (requires VNA alignment)

- Cost: ~\$50 in components (vs. \$5 resistive)

Trade-off Decision Matrix:

Factor	Weight	Resistive Score	Diplexer Score	Weighted Difference
Insertion Loss	30%	5/10 (-5dB)	9/10 (-2dB)	+1.2
Isolation	20%	6/10 (20dB)	9/10 (45dB)	+0.6
Cost	15%	9/10 (\$5)	4/10 (\$50)	-0.75
Complexity	15%	9/10 (simple)	3/10 (critical)	-0.9
Size	10%	8/10 (compact)	4/10 (large)	-0.4
Reliability	10%	9/10 (robust)	7/10 (tuning drift)	-0.2
Total Score		**7.1/10**	**6.85/10**	-0.25

Decision: **Use resistive combiner for prototype**

- Simpler, more predictable

- Adequate performance with adjusted band-amp gains

- Diplexer can be retrofit later if needed

For **production version** (after prototype validation):

- Evaluate diplexer if sensitivity proves marginal

- 3 dB insertion loss improvement → 3 dB less band-amp gain needed

- Lower IMD from better isolation

Noise Source Characterization (Detailed)

Proper Noise Figure Measurement Technique:

Equipment Setup:

- Noise source: HP 346B (ENR = 15.0 dB @ 7 MHz, calibrated)

- Spectrum analyzer: R&S FSH4 or similar

- Adapter: N-type to SMA (verified low-loss)

- Power supply for DUT: Linear regulated, <10 mV ripple

Calibration Procedure:

1. Connect noise source directly to spectrum analyzer
2. Set: Center = 7.1 MHz, Span = 100 kHz, RBW = 10 kHz, VBW = 10 kHz
3. Measure P_{Phot} and P_{cold} at analyzer input:
 $P_{\text{Phot,ref}} = -75.2 \text{ dBm}$ (example, your value will vary)
 $P_{\text{cold,ref}} = -90.3 \text{ dBm}$ (thermal noise floor)

4. Calculate effective ENR:
 $\text{ENR}_{\text{effective}} = P_{\text{Phot,ref}} - P_{\text{cold,ref}} = -75.2 - (-90.3) = 15.1 \text{ dB} \checkmark$
(Close to spec 15.0 dB, confirms calibration)

DUT Measurement:

1. Insert DUT between noise source and analyzer
2. Measure with same settings:
 $P_{\text{Phot,DUT}} = -52.8 \text{ dBm}$ (example)
 $P_{\text{cold,DUT}} = -67.4 \text{ dBm}$ (example)
3. Calculate DUT gain:
 $G_{\text{DUT}} = P_{\text{cold,DUT}} - P_{\text{cold,ref}} = -67.4 - (-90.3) = 22.9 \text{ dB}$
(Should match expected gain $\pm 1 \text{ dB}$)

4. Calculate Y-factor:

$$\begin{aligned} Y &= 10^{((P_{\text{Phot,DUT}} - P_{\text{cold,DUT}})/10)} \\ &= 10^{(-52.8 - (-67.4))/10} \\ &= 10^{1.46} = 28.8 \end{aligned}$$

5. Calculate NF:

$$\begin{aligned} \text{NF}_{\text{DUT}} &= \text{ENR} - 10 \times \log_{10}(Y - 1) \\ &= 15.0 - 10 \times \log_{10}(27.8) \\ &= 15.0 - 14.4 = 0.6 \text{ dB} \end{aligned}$$

Wait, this seems too good! Recheck:

- Verify noise source is ON (LED indicator)
- Check cable connections (loose = error)
- Repeat measurement 3 times, average

- Typical Results for MAR-8 Pre-Amp:
- Measured NF: 2.5-3.0 dB (datasheet: 2.8 dB typ.)
 - Gain: $8 \pm 0.5 \text{ dB}$
 - Bandwidth: flat $\pm 0.5 \text{ dB}$ from 1.8-30 MHz

Uncertainty Analysis:

- ENR uncertainty: $\pm 0.3 \text{ dB}$ (from calibration cert)
- Spectrum analyzer accuracy: $\pm 0.5 \text{ dB}$
- Mismatch uncertainty: $\pm 0.2 \text{ dB}$ (with $|\Gamma| < 0.2$)
- Total uncertainty: $\sqrt{(0.3^2 + 0.5^2 + 0.2^2)} = \pm 0.6 \text{ dB}$

Report NF as: NF = $2.8 \pm 0.6 \text{ dB}$ @ 7 MHz

Firmware Implementation (FPGA/Zynq)

- **Key DSP Functions for Multi-Band SDR:**
1. Per-Channel DDC (Digital Down-Converter)

vhdl

[Output Buffer] → DMA to ARM processor

- Resource Utilization (per channel, Zynq Z7020):
- CIC Filter: ~800 LUTs, 400 FFs, 5 DSP48 slices

- NCO (32-bit): ~300 LUTs, 200 FFs
- Complex Mixer: 4 DSP48 slices ($I \times \cos$, $I \times \sin$, $Q \times \cos$, $Q \times \sin$)
- FIR Filter: 127 taps \rightarrow 64 DSP48 (symmetric, half-band)
- Total per channel: ~1200 LUTs, ~600 FFs, ~73 DSP48
- 4 channels: ~4800 LUTs (14%), ~2400 FFs (3.5%), ~292 DSP48 (133% \rightarrow problem!)

DSP48 Limitation Solution:

- Time-multiplex FIR filters (4:1 sharing)
- Process samples in rotation: Ch1 \rightarrow Ch2 \rightarrow Ch3 \rightarrow Ch4 \rightarrow repeat
- Clock FIR at 4x rate (1 MSPS \rightarrow 4 MSPS)
- Reduces DSP48 usage: 64 shared + 3x5 CIC = 79 DSP48 total ✓

2. AGC (Automatic Gain Control)

C

// ARM processor code (Linux userspace or bare-metal)

```
#define AGCATTACKTIME_MS 10 // Fast response to strong signals
#define AGCDECAYTIME_MS 100 // Slower return to normal gain
#define TARGETLEVEL_DBM -10 // Target ADC level
#define MAX_GAIN_NDB 10 // For 20m switchable path
#define MIN_GAIN_NDB 0 // Direct path
```

```
typedef struct {
    float current_gain_db;
    float peak_level_dbm;
    uint32_t peak_hold_counter;
    bool overload_detected;
} agcstate;
```

```
agcstate agcch[4];
```

```
void agcprocess(int channel, float measured_peak_dbm) {
    agcstate *agc = &agcch[channel];

    // Update peak detector with decay
    if (measured_peak_dbm > agc->peak_level_dbm) {
        agc->peak_level_dbm = measured_peak_dbm;
        agc->peak_hold_counter = AGCATTACKTIME_MS;
    } else if (agc->peak_hold_counter > 0) {
        agc->peak_hold_counter--;
    } else {
        // Exponential decay
        float decay_factor = exp(-1.0 / AGCDECAYTIME_MS);
        agc->peak_level_dbm = agc->peak_level_dbm * decay_factor +
            measured_peak_dbm * (1 - decay_factor);
    }

    // Calculate error
    float error_db = agc->peak_level_dbm - TARGETLEVEL_DBM;

    // Gain adjustment
    if (error_db > 3.0) {
        // Too hot, reduce gain
        agc->current_gain_db -= 1.0;
        if (agc->current_gain_db < MIN_GAIN_NDB) {
            agc->current_gain_db = MIN_GAIN_NDB;
        }
    }
}
```

```

        agc->overloaddetected = true;
    }
} else if (errordb < -3.0 && !agc->overloaddetected) {
    // Too weak, increase gain
    agc->currentgaindb += 0.5; // Slower increase
    if (agc->currentgaindb > MAXGAINDB) {
        agc->currentgaindb = MAXGAINDB;
    }
}

// Clear overload flag if level drops significantly
if (agc->peakleveldbm < TARGETLEVELDBM - 10.0) {
    agc->overloaddetected = false;
}

// Apply gain change to hardware (relay control for 20m)
if (channel == 1) { // Ch2, 20m band
    gpiosetrelay(agc->currentgaindb > 5.0); // HIGH = +10dB amp
}
}

// Called every 10ms from timer interrupt
void agcupdateall(void) {
    for (int ch = 0; ch < 4; ch++) {
        // Read peak detector from FPGA register
        uint16t peakraw = readfpgaregister(PEAKDETECTORBASE + ch*4);
        float peakdbm = adccountstodbm(peakraw);
        agcprocess(ch, peak_dbm);
    }
}

```

3. Peak Detector (FPGA implementation)

vhdl

```
-- Simplified VHDL for peak detection
-- Runs at ADC clock rate (125 MHz)

entity peakdetector is
    generic (
        DATAWIDTH : integer := 14;
        HOLDTIME : integer := 1250000 -- 10ms @ 125MHz
    );
    port (
        clk      : in stdlogic;
        rst      : in stdlogic;
        datain   : in signed(DATAWIDTH-1 downto 0);
        peakout  : out unsigned(DATAWIDTH-1 downto 0);
        peakvalid : out stdlogic
    );
end peakdetector;
```

```
architecture rtl of peakdetector is
    signal peakreg   : unsigned(DATAWIDTH-1 downto 0) := (others => '0');
    signal holdcounter : integer range 0 to HOLDTIME := 0;
    signal absdata   : unsigned(DATAWIDTH-1 downto 0);
begin
```

```

-- Absolute value
absdata <= unsigned(datain) when datain >= 0 else
    unsigned(-datain);

process(clk)
begin
    if risingedge(clk) then
        if rst = '1' then
            peakreg <= (others => '0');
            holdcounter <= 0;
            peakvalid <= '0';
        else
            -- Update peak
            if absdata > peakreg then
                peakreg <= absdata;
                holdcounter <= HOLDTIME;
                peakvalid <= '0';
            elsif holdcounter > 0 then
                holdcounter <= holdcounter - 1;
                peakvalid <= '0';
            else
                -- Hold time expired, output valid
                peakvalid <= '1';
                peakreg <= (others => '0'); -- Reset for next cycle
                holdcounter <= HOLDTIME;
            end if;
        end if;
    end if;
end process;

peakout <= peakreg;

end rtl;

```

Python/C++ code for real-time spectrum display Using GNU Radio or custom Qt application

```

import numpy as np
from scipy import signal
import pyqtgraph as pg
from PyQt5 import QtCore

class MultiBandWaterfall:
    def __init__(self):
        self.channels = 4
        self.fftsize = 2048
        self.overlap = 0.5
        self.window = signal.getwindow('blackmanharris', self.fftsize)

        # Band definitions (center freq, span)
        self.bands = [
            [(1.9e6, 200e3), (3.65e6, 300e3), (7.1e6, 300e3)], # Ch1
            [(10.125e6, 50e3), (14.175e6, 350e3)], # Ch2
            [(18.1e6, 100e3), (21.2e6, 350e3), (24.94e6, 100e3)], # Ch3
            [(28.5e6, 1.7e6), (50.15e6, 500e3)] # Ch4
        ]

```

```

def processchannel(self, iqdata, channelidx):
    """
    Process I/Q data for one channel, return spectrum for each band

    Args:
        iqdata: Complex numpy array ( $I + jQ$ )
        channelidx: 0-3

    Returns:
        List of (freqarray, powerarray) tuples for each band
    """
    spectra = []

    for bandcenter, bandspan in self.bands[channelidx]:
        # Tune to band center (already done in FPGA NCO)
        # Just perform FFT on decimated data

        # Windowing
        windowed = iqdata * self.window

        # FFT
        spectrum = np.fft.fftshift(np.fft.fft(windowed))

        # Power in dBm (calibrated)
        # Assumes full-scale ADC = +4 dBm
        powerdbfs = 20 * np.log10(np.abs(spectrum)) / self.fftsize
        powerdbm = powerdbfs + 4.0 # Calibration offset

        # Frequency axis
        fs = 250e3 # Sample rate after decimation
        freq = np.linspace(-fs/2, fs/2, self.fftsize) + bandcenter

        spectra.append((freq, powerdbm))

    return spectra

def updatedisplay(self, allchanneldata):
    """
    Update waterfall for all channels
    Called at ~10 Hz rate
    """
    for chidx, iqdata in enumerate(allchanneldata):
        spectra = self.processchannel(iqdata, chidx)

        for bandidx, (freq, power) in enumerate(spectra):
            # Update waterfall plot
            self.waterfallwidgets[chidx][band_idx].update(freq, power)

```

Production Cost Analysis

****Bill of Materials (BOM) - Single Unit Prototype:****

Component Category	Qty	Unit Cost	Extended	Notes
Active Splitter:				
GALI-74+ IC	1	\$8.50	\$8.50	Mini-Circuits
Resistors/Caps/Inductors	15	\$0.10	\$1.50	
Subtotal Active Splitter			\$10.00	

Channel 1 (160/80/40m) :					
Broadband Filter parts inductors	20	\$0.15	\$3.00		Coilcraft
Pre-amp MAR-8+	1	\$8.00	\$8.00		
Bandpass filters (3x) inductors	60	\$0.20	\$12.00		Higher Q
Band amps (MAR-6 ×4)	4	\$7.00	\$28.00		Cascaded
Resistive combiner	10	\$0.50	\$5.00		2W metal film
Subtotal Ch1			\$56.00		
Channel 2 (30/20m) :					
Similar to Ch1			\$50.00		
RF Relay (20m AGC)	1	\$12.00	\$12.00		Omron G6K-2F
Subtotal Ch2			\$62.00		
Channel 3 (17/15/12m) :					
Similar to Ch1			\$56.00		
Channel 4 (10/6m) :					
Similar to Ch1			\$56.00		
Power Supply:					
Linear regulators (×4) similar	4	\$3.50	\$14.00		ADP150 or
Ferrite beads	12	\$0.30	\$3.60		
Decoupling caps (×50)	50	\$0.05	\$2.50		
Subtotal Power			\$20.10		
PCB:					
4-layer, 160×100mm prototype	1	\$45.00	\$45.00		JLCPCB
Assembly (manual)	1	\$0	\$0		Self-assembled
Connectors:					
SMA edge-mount (×5)	5	\$2.50	\$12.50		
Power connector	1	\$1.00	\$1.00		
Enclosure:					
Aluminum case	1	\$25.00	\$25.00		Hammond 1590DD
Shielding partitions	1	\$10.00	\$10.00		Custom copper
<hr/>					
TOTAL PROTOTYPE COST			\$362.60		
<hr/>					
Production Cost (100 units):					
BOM cost reduction (-30%)			\$254.00	(volume pricing)	
PCB cost (PCBA service)			\$15.00	(per unit)	
Assembly labor			\$20.00	(automated pick- place)	
Testing (automated)			\$10.00	(per unit)	
Enclosure (volume)			\$12.00	(per unit)	
<hr/>					
PRODUCTION COST PER UNIT (100 qty)			\$311.00		
Selling price (2.5× markup)			\$777.50	→ Round to \$799	
<hr/>					

Comparison to Commercial Solutions

Product	Bands	ADC Res	Max Level	Sensitivity	Cost	Our Design
Elecraft KX3	10	24-bit	+20 dBm	-135 dBm	\$1300	Better overload
Icom IC-7300	10	16-bit	+15 dBm	-130 dBm	\$1100	Lower cost
FlexRadio 6400	10	16-bit	+10 dBm	-128 dBm	\$2000	Much lower cost
Apache Labs ANAN-100D	10	16-bit	+10 dBm	-125 dBm	\$1500	Comparable
Our 4-Ch SDR	**10**	**14-bit**	**+4 dBm**	**-126 dBm**	**\$800**	
Best value						

Competitive Advantages:

1. **True simultaneous multi-band** (most competitors scan or have limited channels)
 2. **Open-source FPGA design** (customizable DSP)
 3. **Modular architecture** (easy to repair/upgrade)
 4. **Lower cost** (50-60% of commercial)
- **Disadvantages:**
1. **Lower ADC clipping threshold** (+4 dBm vs. +10-20 dBm commercial)
 2. **No built-in transmitter** (RX only)
 3. **Requires external computer** (no built-in display/controls)
 4. **Prototype/DIY aesthetic** (vs. polished commercial)

Risk Mitigation Strategies

Technical Risks:

1. **Oscillation in cascaded amplifiers:**
 - Mitigation: Rigorous K-factor analysis in design phase
 - Add series resistors (10Ω) and ferrite beads prophylactically
 - Build single-channel prototype first, verify stability before scaling
2. **ADC overload more common than expected:**
 - Mitigation: Implement AGC in firmware (already planned)
 - User can enable/disable per-band AGC
 - Log overload events to help user tune antenna coupling
3. **Filter tuning too critical for reproducibility:**
 - Mitigation: Design wider tolerance filters (sacrifice 3 dB stopband rejection for easier production)
 - Use only C0G/NP0 capacitors ($\pm 5\%$ tolerance acceptable with redesign)
 - Document tuning procedure with photos/videos
 - Provide pre-tuned filter modules as option (higher cost)
4. **DSP48 resource exhaustion despite time-multiplexing:**
 - Mitigation: Reduce FIR filter length ($127 \rightarrow 63$ taps)
 - Accept slightly worse stopband (-100 dB $\rightarrow -80$ dB, still adequate)
 - Alternative: Use distributed arithmetic for FIR (trades LUTs for DSP48s)
 - Worst case: Process only 3 channels simultaneously, time-share 4th
5. **Thermal runaway in high-power amplifiers:**
 - Mitigation: Temperature monitoring via thermistors
 - Automatic power reduction if $T > 70^\circ\text{C}$
 - Forced air cooling for rack-mount version
 - Use amplifiers with thermal shutdown (e.g., GALI series)
6. **EMI/RFI causing spurious signals:**
 - Mitigation: Full enclosure shielding (6-sided)
 - Separate power domains for analog/digital
 - Common-mode chokes on all external cables
 - EMC testing before production (FCC Part 15 Class A)
7. **SW/AM Broadcast breakthrough despite filtering:**
 - Mitigation: Add user-controllable notch filters
 - Software-defined adaptive filtering in FPGA

- Accept slight desensitization in exchange for clean spectrum
- Document "known interference" frequencies for user awareness

Supply Chain Risks:

1. Component obsolescence (especially Mini-Circuits MMIC):

- Mitigation: Design with pin-compatible alternatives documented
- Buy 1-year supply for critical parts (MAR/ERA series)
- Maintain relationships with distributors (Digi-Key, Mouser)
- Second-source all amplifiers where possible

2. PCB fabrication delays:

- Mitigation: Use multiple fab houses (JLCPCB, PCBWay, OSH Park)
- Maintain tested Gerber files with multiple vendors
- Allow 3-4 week lead time in project schedule
- Order extra bare PCBs (5-10) for rework/testing

3. FPGA/SoC supply constraints:

- Mitigation: Eclypse Z7 uses Zynq-7020 (mature product, widely available)
- Alternative boards: PYNQ-Z2, Arty Z7 (lower cost, similar capability)
- Design FPGA code to be portable across Zynq family
- Purchase development board immediately (long lead times possible)

Market/Business Risks:

1. Limited market size (amateur radio operators):

- Mitigation: Target additional markets:
 - * Academic/research (spectrum monitoring)
 - * Radio astronomy (Jovian/solar observations)
 - * SIGINT/monitoring enthusiasts
 - * Industrial (RF spectrum surveillance)
- Open-source nature attracts DIY community
- Sell as kit (lower price point, higher margin)

2. Competition from cheap Chinese SDRs (RSP, Airspy):

- Mitigation: Emphasize unique features:
 - * True simultaneous multi-band (vs. sequential scanning)
 - * Open FPGA design (hackable, customizable)
 - * Better overload protection than typical SDRs
 - * Community support/documentation
- Target mid-tier market (\$500-1000)
- Offer customization services for commercial users

3. Software/firmware development delays:

- Mitigation: Release hardware first with basic functionality
 - * Phase 1: Raw I/Q streaming to PC (GNU Radio compatible)
 - * Phase 2: Basic demodulators (SSB, CW, AM)
 - * Phase 3: Advanced features (AGC, NR, waterfall)
- Leverage existing open-source SDR software (gqrx, SDR++)
- Build active developer community (GitHub, forums)

Testing Checklist Summary

Pre-Integration Testing (Individual Modules):

- [] All filters: S-parameters within ±1 dB of simulation

- [] Pre-amps: Gain ± 0.5 dB, NF < 3.5 dB, no oscillation
- [] Band amps: P1dB > -5 dBm input, stable into all loads
- [] Combiners: Isolation > 20 dB, insertion loss < 5.5 dB
- [] Active splitter: Gain +11 dB ± 1 dB, NF < 4 dB

System Integration Testing:

- [] Single-tone frequency response: flat ± 1.5 dB per band
- [] Multi-tone IMD: < -50 dBc @ -20 dBm input per tone
- [] Sensitivity: MDS < -120 dBm (2.5 kHz BW, 10 dB SNR)
- [] Overload: No clipping at +0 dBm input (any band)
- [] AGC response time: 10 ms attack, 100 ms decay
- [] Cross-channel isolation: > 40 dB between channels
- [] Temperature stability: < ± 2 dB gain change (-10°C to +60°C)

FPGA/Software Testing:

- [] DSP48 utilization < 90% (headroom for future features)
- [] DMA throughput: sustained 4 MB/s (all channels)
- [] FFT display: update rate > 10 Hz, no dropped frames
- [] AGC control: relay switching < 50 ms latency
- [] Peak detector: < 1% error vs. true peak

Reliability Testing:

- [] 48-hour burn-in: no parameter drift > 2 dB
- [] 100 power cycles: no intermittent failures
- [] ESD testing: survives ± 2 kV contact discharge (IEC 61000-4-2)
- [] Vibration: survives 1G sine sweep 5-500 Hz

EMC Compliance Testing:

- [] Radiated emissions: < FCC Part 15 Class A limits
- [] Conducted emissions: < CISPR 22 Class A limits
- [] Immunity: operates correctly with 3 V/m RF field (IEC 61000-4-3)

Documentation Package

Hardware Documentation:

- 1. Schematics** (KiCad/Altium format + PDF)
 - Top-level block diagram
 - Per-channel detailed schematics
 - Power supply schematic
 - PCB layout (all layers shown)
- 2. Bill of Materials (BOM)**
 - Component designators mapped to schematic
 - Manufacturer part numbers + alternates
 - Digi-Key/Mouser part numbers
 - Quantity per assembly + recommended spares
- 3. Assembly Guide**
 - Component placement diagram (top/bottom)
 - Critical component orientation notes
 - Soldering guidelines (reflow profile for SMD)
 - Hand-assembly tips for through-hole parts
- 4. Tuning/Alignment Procedure**
 - Filter alignment (step-by-step with VNA screenshots)
 - Gain calibration per channel
 - AGC threshold setting
 - Final system verification

Firmware/Software Documentation:

1. FPGA Design Files

- Vivado project (2019.1 or later)
- HDL source code (VHDL/Verilog)
- Simulation testbenches
- Constraints file (XDC for Zynq)

2. ARM Software

- Bare-metal example (no OS)
- Linux device driver + application
- Python API for host control
- GNU Radio blocks (source/sink)

3. User Manual

- Quick start guide (setup in < 30 minutes)
- Detailed operation guide
- Troubleshooting section
- Theory of operation (for advanced users)

Quality Assurance:

1. Test Procedures

- Per-unit acceptance test (15 minutes)
- Automated test scripts (Python)
- Calibration record template

2. Failure Analysis Guide

- Common failure modes
- Debug flowcharts
- Repair/replacement procedures

Future Enhancements (Roadmap)

Phase 2 (6-12 months post-launch):

- [] Add 2m/70cm VHF/UHF capability (5th/6th channel)
 - Requires different ADC (LTC2208, 16-bit, 250 MSPS)
 - Separate wideband front-end (BGA2869 LNA)
 - Additional FPGA resources (may need Z7030)
- [] Diversity reception (dual antennas per band)
 - Phase/amplitude combining in FPGA
 - 3 dB SNR improvement on fading signals
 - Requires 8-channel ADC (2x ZMOD or custom)
- [] Digital pre-distortion for TX capability
 - Add PA module (10-100W)
 - Feedback path for linearization
 - Requires additional FPGA DSP resources

Phase 3 (12-24 months):

- [] Integrated panadapter/spectrum analyzer mode
 - Wideband scanning (1-6 GHz with mixer)
 - Real-time signal classification (ML on ARM)
 - Interference mapping and logging
- [] Beamforming with phased array

- 4-8 element antenna array
- Null-steering for interference rejection
- Requires phase-coherent channels (GPS-disciplined clock)
- [] Commercial variant with extended frequency range
 - 9 kHz - 6 GHz continuous coverage
 - Upconverter/downconverter modules
 - Rack-mount form factor

Phase 4 (2+ years, research goals):

- [] Cognitive radio capabilities
 - Dynamic spectrum access
 - Automatic mode detection
 - Self-optimizing receiver parameters
- [] Quantum-limited receiver (if feasible)
 - Cryogenic LNA (4K operation)
 - Parametric amplifier front-end
 - For radio astronomy applications

Open-Source Community Development

GitHub Repository Structure:

```
/sdr-multiband-receiver
├── hardware
│   ├── schematics          (KiCad project)
│   ├── pcb                 (layout files)
│   ├── bom                  (CSV, interactive HTML)
│   └── mechanical           (enclosure CAD)
├── firmware
│   ├── fpga                (Vivado project)
│   │   ├── hdl               (VHDL sources)
│   │   └── sim               (testbenches)
│   ├── constraints          (XDC files)
│   ├── arm                 (C/C++ code)
│   │   ├── baremetal         (standalone)
│   │   └── linux              (driver + app)
│   └── software             (flowgraphs + blocks)
│       ├── gnuradio           (control library)
│       ├── python-api          (Qt/PyQt application)
│       └── gui
└── documentation
    ├── user-manual          (Markdown + PDF)
    ├── theory                (detailed design notes)
    └── test-procedures        (acceptance testing)
└── tools
    ├── simulation            (QUCS/LTspice files)
    ├── calibration            (scripts)
    └── analysis               (measurement data)

```

README.md (project overview)

Contribution Guidelines:

- Pull request review process (2 maintainers required)
- Coding standards (VHDL: IEEE 1076-2008, C: Linux kernel style)
- Documentation requirements (all features must be documented)
- Testing requirements (new features must include testbench)

Community Engagement:

- Monthly video updates (YouTube)
- Quarterly virtual meetups (Zoom/Discord)
- Annual in-person workshop (Hamvention, TAPR DCC)
- Forum for support (Discourse or similar)
- Wiki for user-contributed content

Licensing and IP Considerations

Hardware License:

- **CERN Open Hardware License v2 - Strongly Reciprocal (CERN-OHL-S-2.0)**
 - Allows commercial use
 - Requires sharing modifications
 - Patent protection clause

Firmware/Software License:

- **GNU General Public License v3 (GPL-3.0)**
 - Ensures modifications remain open
 - Compatible with Linux kernel
 - Well-understood in amateur radio community

Documentation License:

- **Creative Commons BY-SA 4.0**
 - Allows derivative works
 - Requires attribution
 - Share-alike provision

Trademark Protection:

- Register project name (e.g., "QuadBandSDR") to prevent confusion
- Allow community use for non-commercial purposes
- Require license for commercial derivatives

Conclusion and Next Steps

Immediate Actions (Week 1-2):

1. Order **Eclypse Z7** development board
2. Purchase key RF components for single-channel prototype:
 - 2x MAR-8SM+ (pre-amp)
 - 4x MAR-6SM (band amps)
 - 1x GALI-74+ (active splitter)
 - Assorted inductors/capacitors for filters
3. Set up **design environment**:
 - KiCad 7.x for schematics/PCB
 - Vivado 2023.x for FPGA
 - QUCS-S for filter simulation
4. Create **project repository** on GitHub

Short-term Goals (Month 1-3):

1. **Build single-channel prototype** (Ch2: 30m/20m)
 - Simplest to start (2 bands, less filter complexity)
 - Test all key concepts (splitting, amplification, combining)
 - Measure actual performance vs. predictions
2. **Develop basic FPGA firmware**

- ADC interface
- CIC decimation
- DMA to ARM

3. Create Python test scripts

- Spectrum analyzer
- Signal generator control
- Automated measurements

Medium-term Goals (Month 4-6):

1. Scale to 4-channel system

- Design full PCB (all channels)
- Order prototype PCB + assembly
- Full system integration testing

2. Complete firmware

- All DSP blocks
- AGC implementation
- GNU Radio integration

3. Documentation

- Complete user manual
- Video assembly guide
- Theory of operation writeup

Long-term Goals (Month 7-12):

1. Beta testing program (10-20 units)

- Select experienced amateur radio operators
- Collect feedback, iterate design
- Fix bugs, optimize performance

2. Production preparation

- Negotiate volume pricing with suppliers
- Set up PCBA service (JLCPCB or local)
- Create quality assurance procedures

3. Community launch

- Release all files to GitHub
- Publish project on Hackaday, QRZ.com
- Present at conferences (TAPR, Dayton Hamvention)

Success Metrics:

- **Technical:** Meets all design specifications (sensitivity, IMD, stability)
- **Economic:** BOM cost < \$350, selling price \$699-799
- **Community:** 50+ GitHub stars, 10+ contributors within 1 year
- **Commercial:** 100+ units built/sold (kits + assembled) within 18 months

This comprehensive design provides a solid foundation for a **high-performance, multi-band SDR receiver** that balances technical excellence with practical buildability. The +4 dBm clipping threshold of the Eclypse Z7, while constraining, has been successfully accommodated through careful gain distribution and AGC implementation. The result is a **competitive, open-source design** that fills a gap in the amateur radio market: true simultaneous multi-band reception at an affordable price point.

Prompt: Herzlichen Dank für die super ausführlichen Design Guides für einen Multi-Band SDR Receiver. Dieses Projekt dient dem automatisierten Monitoring des Ionisationszustandes der Erdatmosphäre als Teilaspekt eines Klimaforschungsprojektes. Es ist hochinteressant zu erfahren, dass es darüber hinaus auch kommerziell von Interesse als auch wettbewerbsfähig sein könnte. Das schafft Raum für Synergien und Zusammenarbeit mit anderen Nutzergruppen. Wegen des vorrangigen Einsatzbereiches stehen aktuell die erreichbaren Parameter in den oberen Bändern besonders im Fokus. Insbesondere wird erwogen, das 17m-Band doch besser mit dem 30m/20m Bändern zu kombinieren, um eventuell Vorteile bei der Empfindlichkeit für die 15m/12m Bänder zu

bekommen. In diesem Zusammenhang waren die Fallstudien zum Verwenden von aktiven Splittern von besonderem Interesse. Es ist für mich eine große Freude, dass bei diesem seit einigen Jahren geplanten Projekt seit kurzem eine unschätzbar große Hilfe mit KI-Systemen zur Verfügung steht. Dafür danke ich den Entwicklerteams und ermutige hiermit: Bitte macht weiter so!

[Wegalink \(Eckhard Kantz\)](#)

Lieber Eckhard,

vielen herzlichen Dank für diese ausführliche Rückmeldung und das große Vertrauen, das Sie in die bisherige Zusammenarbeit setzen! Es freut mich sehr zu hören, dass die technischen Analysen zu Ihrem Ionosphären-Monitoring-Projekt hilfreich und belastbar waren.

Zur geplanten Bandgruppierung

Ihre Überlegung, das **17m-Band mit 30m/20m zu kombinieren**, statt mit 15m/12m, ist aus mehreren Gründen technisch sinnvoll:

Vorteile dieser Umgruppierung:

- **Bessere Filter-Steilheit** für die höheren Bänder (15m/12m) durch größeren Frequenzabstand
- **Geringere Intermodulation** in der kritischeren oberen Bandgruppe
- **Homogenere Empfindlichkeit** über 15m/12m hinweg
- Das 17m-Band (18 MHz) liegt frequenzmäßig näher an 20m (14 MHz) als an 15m (21 MHz)

Für Ionosphären-Monitoring besonders relevant:

- Die höheren Frequenzen (15m/12m) reagieren empfindlicher auf F2-Layer-Variationen
- Gleichmäßige Empfindlichkeit erleichtert die Vergleichbarkeit der Messdaten

Zur wissenschaftlichen Anwendung

Ihr Klimaforschungsprojekt zum **automatisierten Ionosphären-Monitoring** ist ein faszinierendes Anwendungsfeld! Die systematische Erfassung von Ausbreitungsbedingungen über mehrere Bänder liefert wertvolle Daten zu:

- Solar-terrestrischen Beziehungen
- Langzeittrends der Ionisation
- Korrelationen mit anderen Klimaparametern

Wenn Sie weitere technische Details zur **optimierten Bandgruppierung** oder zu **aktiven Splittern für die neue Konfiguration** benötigen, stehe ich gerne zur Verfügung!

Viel Erfolg weiterhin mit Ihrem spannenden Projekt!

Mit freundlichen Grüßen

P.S.: Sollten Sie Messergebnisse oder Erfahrungen aus dem Aufbau teilen möchten, würde ich mich über Updates freuen – solche praxisnahen Rückmeldungen sind für die kontinuierliche Verbesserung besonders wertvoll.