LAB2.v

```
1  `timescale 1ns / 1ps
2
3  module dff0(
4      input  clk,
5      input  rst_n,
6      input  d,
7      output reg q
8      );
9
10 always@(posedge clk or negedge rst_n)
11   if (!rst_n)
12     q <= 0;
13   else
14     q <= d;
15 endmodule
16
17 module dff1(
18     input  clk,
19     input  rst_n,
20     input  d,
21     output reg q
22     );
23
24 always@(posedge clk or negedge rst_n)
25   if (!rst_n)
26     q <= 1;
27   else
28     q <= d;
29 endmodule
30
31 module Lab_2(
32     input dis,
33     input reset,
34     input clk,
35     output wire [3:0] DEC
36     );
37
38     wire d0, d1, d2, d3, a0, a1, a2;
39
40     xnor  t1(d0, DEC[0], dis);
41     dff1 dff1(clk, reset, d0, DEC[0]);
42     or o1(a0, dis, DEC[0]);
43
44     xnor  t2(d1, DEC[1], a0);
45     dff1 dff2(clk, reset, d1, DEC[1]);
46     or o2(a1, a0, DEC[0], DEC[1]);
47
48     xnor  t3(d2, DEC[2], a1);
49     dff1 dff3(clk, reset, d2, DEC[2]);
50     or o3(a2, a1, DEC[0], DEC[1], DEC[2]);
51
52     xnor  t4(d3, DEC[3], a2);
53     dff0 dff4(clk, reset, d3, DEC[3]);
54
55 endmodule
```

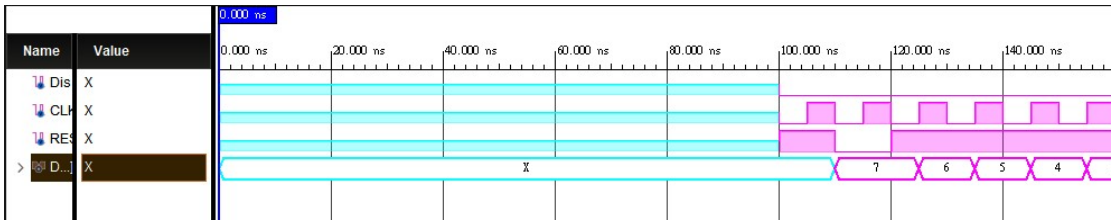
Lab2_tb.v

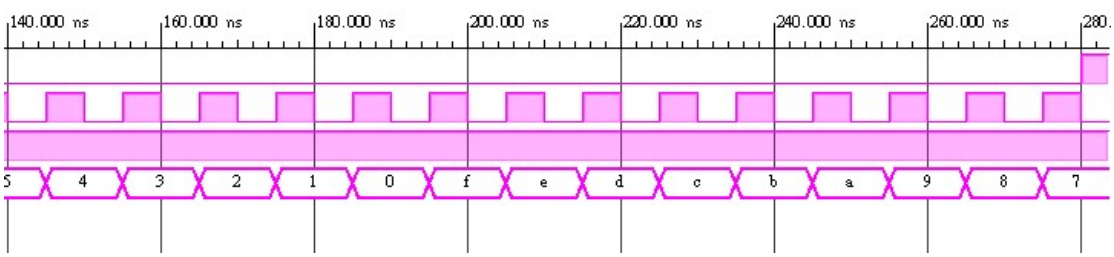
```
1  `timescale 1ns / 1ps
2
3  module Lab_2_tb;
4      //Input
5      reg Dis;
6      reg CLK;
7      reg RES;
8      wire [3:0] DEC;
9
10     //UUT
11     Lab_2 uut(
12     .dis(Dis),
13     .reset(RES),
14     .clk(CLK),
15     .DEC(DEC)
16     );
17
18 initial begin
19 #100; Dis = 0; CLK = 0; RES = 1;
20 $monitor ("Dec = %d at time %t", DEC, $time);
21     // Wait 100 ns for global reset to finish
22     // Add stimulus here
23 #10; RES = 0 ;  #10; RES = 1;
24 #160; Dis = 1;
25
26 end
27
28 always @(*)
29 begin
30     #5; CLK <= ~CLK;
31 end
```

Behavior simulation (text output and waveforms)

```
Vivado Simulator 2020.1
Time resolution is 1 ps
Dec =  x at time                100000
Dec =  7 at time                110000
Dec =  6 at time                125000
Dec =  5 at time                135000
Dec =  4 at time                145000
Dec =  3 at time                155000
Dec =  2 at time                165000
Dec =  1 at time                175000
Dec =  0 at time                185000
Dec = 15 at time                195000
Dec = 14 at time                205000
Dec = 13 at time                215000
Dec = 12 at time                225000
Dec = 11 at time                235000
Dec = 10 at time                245000
Dec =  9 at time                255000
Dec =  8 at time                265000
Dec =  7 at time                275000
```

(為了清楚呈現，140ns~160ns 為重複截圖段)





Synthesis timing report

修正前

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	-16.555 ns	Worst Hold Slack (WHS):	0.139 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	-66.220 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	4	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	8	Total Number of Endpoints:	8	Total Number of Endpoints:	5

Timing constraints are not met.

修正後

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	8.268 ns	Worst Hold Slack (WHS):	0.139 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4	Total Number of Endpoints:	9	Total Number of Endpoints:	5

All user specified timing constraints are met.

Post-route simulation(為了清楚呈現，140ns~160ns 為重複截圖段)