Digital System Design and Implementation

Homework #1

(Due by 03/11 PM 8:00)

Note: Please upload your codes and hand in the **hardcopy** of this experiment including

a. Verilog Codes (60%)
b. Test bench (20%)
c. Input/Output waveforms.(20%)

For even-numbered students, please implement Fig. 1. For odd-numbered students, please implement Fig. 2. The logic gates of the respective sub-block are described in Fig. 3.

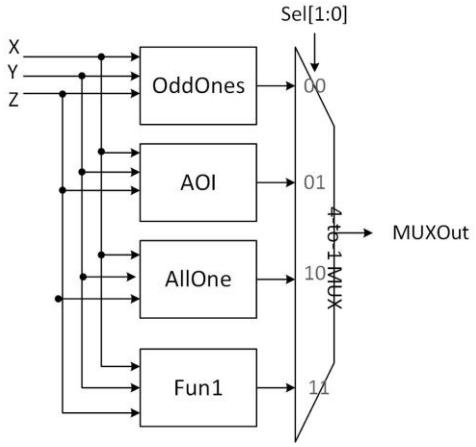

Fig. 1 Block diagram of type 1

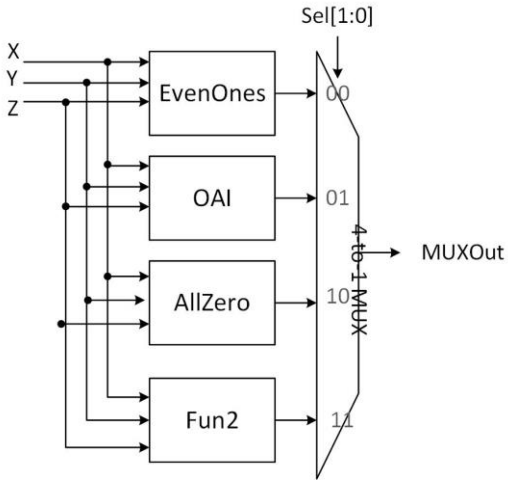

Fig. 2 Block diagram type 2

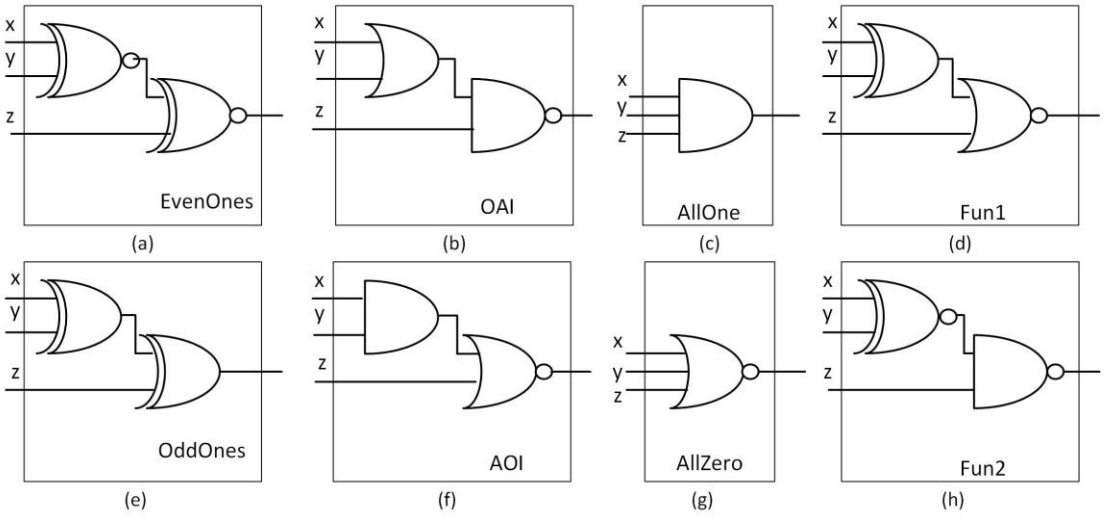

Fig. 3 Logic gates of each sub-block.

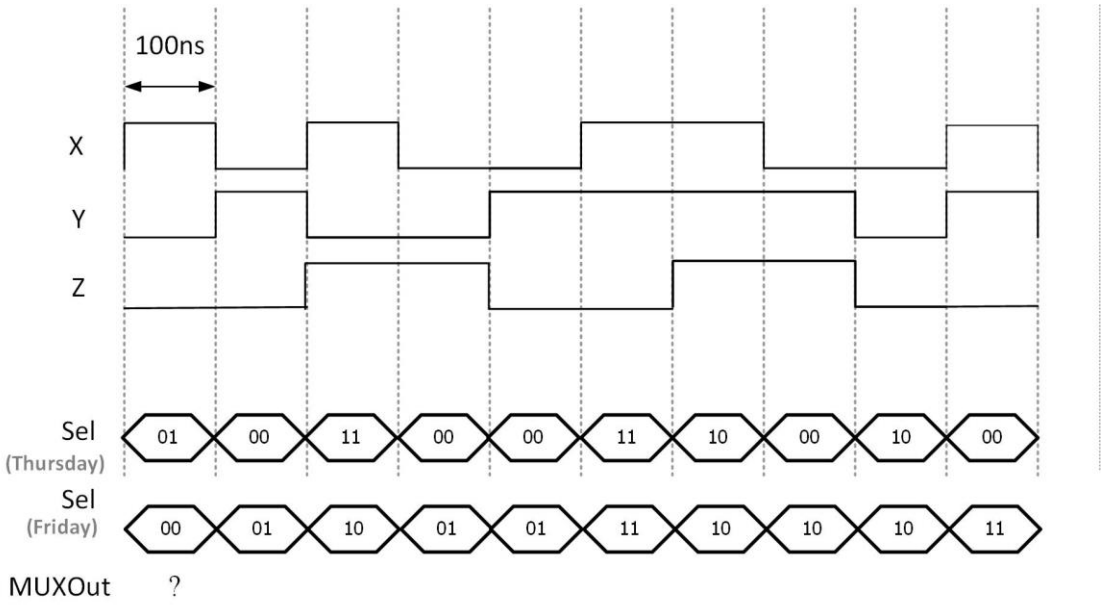

Fig. 4 Test pattern.

1. For even-numbered students,
   a. Please use Verilog to describe the digital circuits in Fig. 1.
   b. Write a test bench to test your design.
   c. The input waveforms are given in Fig. 4. Note the difference for signal "**Sel[1:0]**" of students with lab. time on Thursday and Friday.

2. For odd-numbered students,
   a. Please use Verilog to describe the digital circuits in Fig. 2.
   b. Write a test bench to test your design.
   c. The input waveforms are given in Fig. 4. Note the difference for signal "**Sel[1:0]**" of students with lab. time on Thursday and Friday.