

Computer-Aided VLSI System Design

Final Project: 5G MIMO Demodulation

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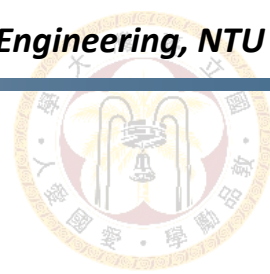
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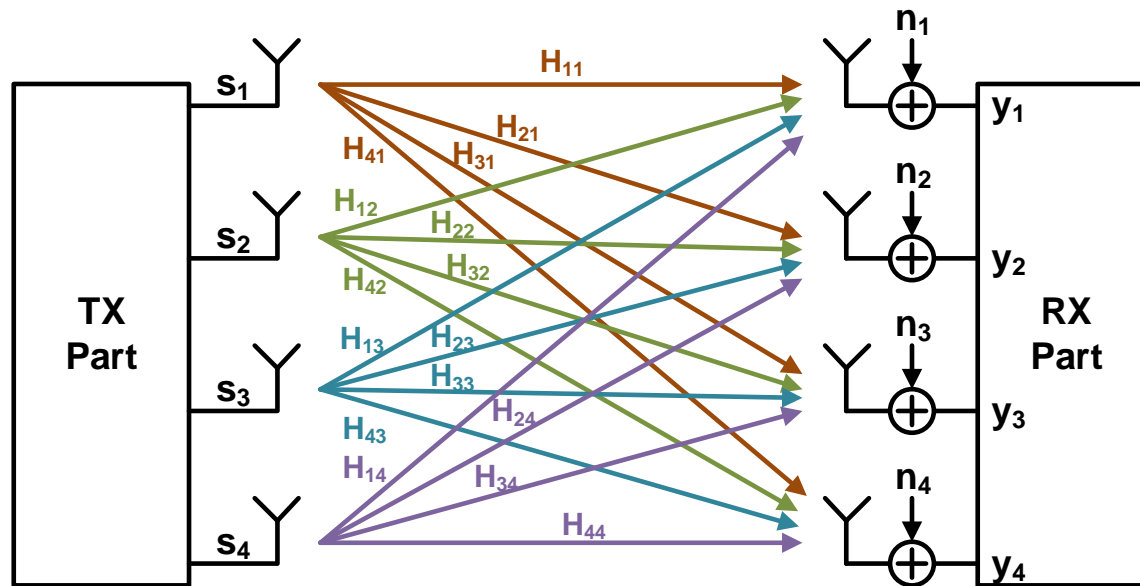
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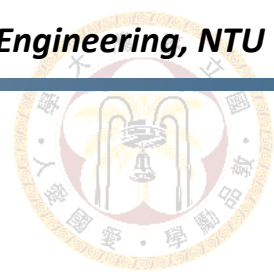


Overview

- **MIMO** (multiple input, multiple output) is an antenna technology for wireless communications, the encode flow is as follows:



- At the receiver, we need to decode the data by reverting the encode flow
- In this project, we'll try to implement a part of simple **MIMO receiver** to demodulate the RX data
 - AWGN (additive white Gaussian noise) channel



System Model

- The received signal \underline{y} per data RE can be expressed as [2] **RE: resource element**

- $\underline{y} = \underline{H}\tilde{\underline{s}} + \underline{n}$

- \underline{H} : channel, $\tilde{\underline{s}}$: transmitted symbol, \underline{n} : noise

- At the 4TX * 4RX transmission, the formula can be re-written as

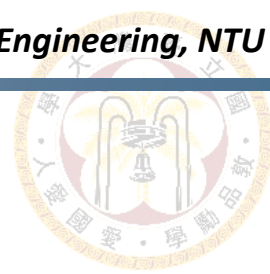
- $$\begin{bmatrix} \underline{y}_1 \\ \underline{y}_2 \\ \underline{y}_3 \\ \underline{y}_4 \end{bmatrix} = \begin{bmatrix} H_{11} & H_{12} & H_{13} & H_{14} \\ H_{21} & H_{22} & H_{23} & H_{24} \\ H_{31} & H_{32} & H_{33} & H_{34} \\ H_{41} & H_{42} & H_{43} & H_{44} \end{bmatrix} \begin{bmatrix} \tilde{s}_1 \\ \tilde{s}_2 \\ \tilde{s}_3 \\ \tilde{s}_4 \end{bmatrix} + \begin{bmatrix} \underline{n}_1 \\ \underline{n}_2 \\ \underline{n}_3 \\ \underline{n}_4 \end{bmatrix}$$

- The MIMO receiver is to demodulate the $\tilde{\underline{s}}$ by \underline{y} , \underline{H} , \underline{n} .

- $\tilde{s}_1, \tilde{s}_2, \tilde{s}_3$ and \tilde{s}_4 are the symbol with modulation (**QPSK – 2-bit data**)

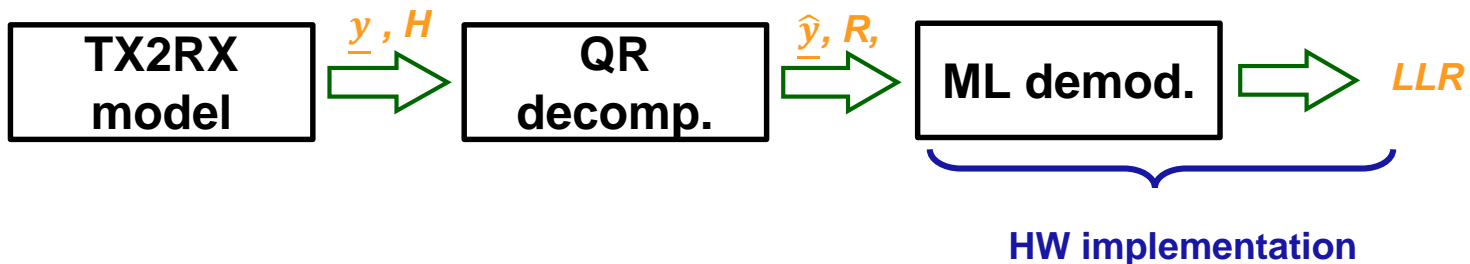
- The output of MIMO receiver is the LLR per bit

- LLR : log likelihood ratio, if the value is positive, it means the possibility of this bit is 0 is much higher than 1, and vice versa
 - Total **8 LLRs** per data RE (4-signal * 2-bit (QPSK))



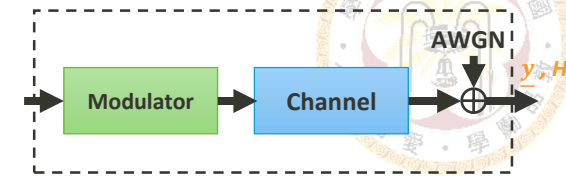
System Model

- From [2], MIMO receiver is composed of QR decomposition (QRD) and Maximum Likelihood (ML) demodulation

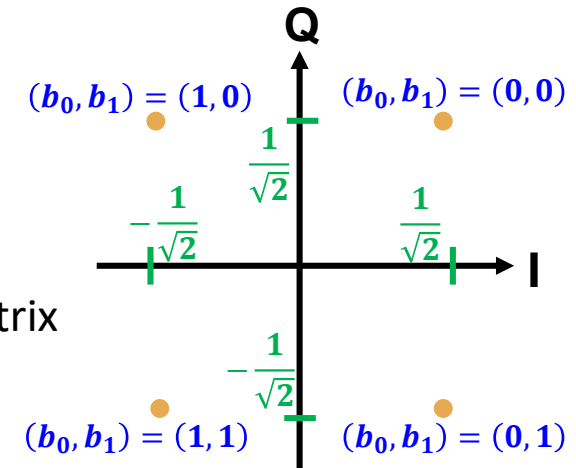


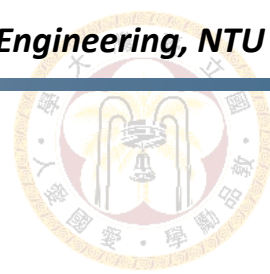
- At this project, we will provide the detailed formula of ML demod. with full search for implementation
- To reduce the complexity of MIMO receiver, many proposals can be found on papers, you can try different proposals to observe the performance and the area/power/latency if you have interest

Tx2Rx Model



- Tx2Rx Model
 - $\underline{y} = \underline{H}\tilde{\underline{s}} + \underline{n}$
- Modulator: transmitted signal $\tilde{\underline{s}}$
 - QPSK (TS 38.211 Section 5.1 [1]): pairs of bits are mapped to complex-valued modulation symbols
- MIMO
 - Channel: multiply by channel matrix: \underline{H}
 - 4X4 matrix, complex number
 - use Normal distribution to generate a random matrix
 - $\underline{H} \sim N(0, 1/4)$
 - AWGN: add noise \underline{n}
 - adds white Gaussian noise from MATLAB function: `awgn()`
 - $\underline{n} \sim N(0, 1)$





QR Decomposition (QRD)

■ Motivation

- Reduce the complexity of Maximum Likelihood (ML) demodulation

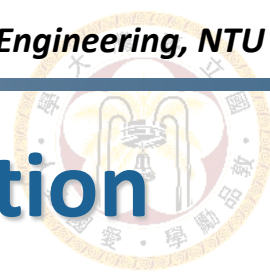
$$\bullet \hat{\underline{s}} = \underset{\underline{s} \in A}{\operatorname{argmin}} (\|\underline{y} - H\underline{s}\|^2)$$

**A: a set of all combinations of
4 transmitted symbol vectors ($s_1 \sim s_4$)**

- With QR decomposition, a signal model can be re-written as

$$\begin{aligned} \underline{y} &= H\underline{s} + \underline{n} \\ \underline{y} &= (\underline{Q}\underline{R})\underline{s} + \underline{n} \\ \underline{Q}^H \underline{y} &= \underline{Q}^H \underline{Q} \underline{R} \underline{s} + \underline{Q}^H \underline{n} \\ \hat{\underline{y}} &= \underline{R} \underline{s} + \underline{v} \end{aligned} \quad \left\{ \begin{array}{l} \underline{Q}: \text{an } \textcolor{red}{orthogonal} \text{ matrix, where } \underline{Q}^H \underline{Q} = I \\ \underline{R}: \text{an } \textcolor{green}{upper triangular} \text{ matrix} \end{array} \right.$$

- ML demodulation question becomes $\hat{\underline{s}} = \underset{\underline{s} \in A}{\operatorname{argmin}} (\|\hat{\underline{y}} - \underline{R}\underline{s}\|^2)$



Maximum Likelihood (ML) Demodulation

■ Soft-bit calculation [2]

$$LLR: L(\underline{x}_{k,b} | \underline{y}) \approx \min_{\underline{x} \in X_{k,b,1}} \|\underline{y} - H\underline{s}\|^2 - \min_{\underline{x} \in X_{k,b,0}} \|\underline{y} - H\underline{s}\|^2 \quad \underline{x} = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} = \begin{bmatrix} (x_{1,1}, x_{1,2}) \\ (x_{2,1}, x_{2,2}) \\ (x_{3,1}, x_{3,2}) \\ (x_{4,1}, x_{4,2}) \end{bmatrix} \Leftrightarrow \underline{s}$$

↓
↓

kth entry of \underline{x} ,
bth bit in the x_k

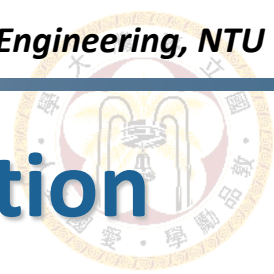
 $X_{k,b,1}$: subsets of $\{\underline{x}\}$ with the bth bit in the kth entry = 1
 $X_{k,b,0}$: subsets of $\{\underline{x}\}$ with the bth bit in the kth entry = 0

$$\|\underline{y} - H\underline{s}\|^2 \Rightarrow \|\hat{\underline{y}} - R\underline{s}\|^2 = \left(\begin{bmatrix} \hat{y}_1 \\ \hat{y}_2 \\ \hat{y}_3 \\ \hat{y}_4 \end{bmatrix} - \begin{bmatrix} R_{11} & R_{12} & R_{13} & R_{14} \\ 0 & R_{22} & R_{23} & R_{24} \\ 0 & 0 & R_{33} & R_{34} \\ 0 & 0 & 0 & R_{44} \end{bmatrix} \begin{bmatrix} s_1 \\ s_2 \\ s_3 \\ s_4 \end{bmatrix} \right)^2$$

$$= \sum_{i=1}^4 |[\hat{y}_i - \sum_{j=1}^4 R_{ij}s_j]|^2$$

■ Hard-bit calculation

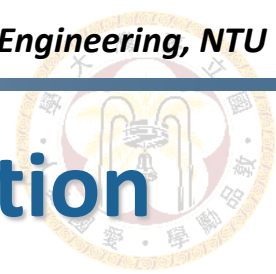
- $L(x_{k,b} | \underline{y})$'s sign-bit = 0, hard-bit out = 0
- $L(x_{k,b} | \underline{y})$'s sign-bit = 1, hard-bit out = 1



Maximum Likelihood (ML) Demodulation

■ Formula

- LLR for $x_{1,1} : L(x_{1,1}|\underline{y}) = \min_{\underline{x} \in X_{1,1,1}} \sum_{i=1}^4 |\hat{y}_i - \sum_{j=i}^4 R_{ij}s_j|^2 - \min_{\underline{x} \in X_{1,1,0}} \sum_{i=1}^4 |\hat{y}_i - \sum_{j=i}^4 R_{ij}s_j|^2$
- LLR for $x_{1,2} : L(x_{1,2}|\underline{y}) = \min_{\underline{x} \in X_{1,2,1}} \sum_{i=1}^4 |\hat{y}_i - \sum_{j=i}^4 R_{ij}s_j|^2 - \min_{\underline{x} \in X_{1,2,0}} \sum_{i=1}^4 |\hat{y}_i - \sum_{j=i}^4 R_{ij}s_j|^2$
- LLR for $x_{2,1} : L(x_{2,1}|\underline{y}) = \min_{\underline{x} \in X_{2,1,1}} \sum_{i=1}^4 |\hat{y}_i - \sum_{j=i}^4 R_{ij}s_j|^2 - \min_{\underline{x} \in X_{2,1,0}} \sum_{i=1}^4 |\hat{y}_i - \sum_{j=i}^4 R_{ij}s_j|^2$
- LLR for $x_{2,2} : L(x_{2,2}|\underline{y}) = \min_{\underline{x} \in X_{2,2,1}} \sum_{i=1}^4 |\hat{y}_i - \sum_{j=i}^4 R_{ij}s_j|^2 - \min_{\underline{x} \in X_{2,2,0}} \sum_{i=1}^4 |\hat{y}_i - \sum_{j=i}^4 R_{ij}s_j|^2$
- LLR for $x_{3,1} : L(x_{3,1}|\underline{y}) = \min_{\underline{x} \in X_{3,1,1}} \sum_{i=1}^4 |\hat{y}_i - \sum_{j=i}^4 R_{ij}s_j|^2 - \min_{\underline{x} \in X_{3,1,0}} \sum_{i=1}^4 |\hat{y}_i - \sum_{j=i}^4 R_{ij}s_j|^2$
- LLR for $x_{3,2} : L(x_{3,2}|\underline{y}) = \min_{\underline{x} \in X_{3,2,1}} \sum_{i=1}^4 |\hat{y}_i - \sum_{j=i}^4 R_{ij}s_j|^2 - \min_{\underline{x} \in X_{3,2,0}} \sum_{i=1}^4 |\hat{y}_i - \sum_{j=i}^4 R_{ij}s_j|^2$
- LLR for $x_{4,1} : L(x_{4,1}|\underline{y}) = \min_{\underline{x} \in X_{4,1,1}} \sum_{i=1}^4 |\hat{y}_i - \sum_{j=i}^4 R_{ij}s_j|^2 - \min_{\underline{x} \in X_{4,1,0}} \sum_{i=1}^4 |\hat{y}_i - \sum_{j=i}^4 R_{ij}s_j|^2$
- LLR for $x_{4,2} : L(x_{4,2}|\underline{y}) = \min_{\underline{x} \in X_{4,2,1}} \sum_{i=1}^4 |\hat{y}_i - \sum_{j=i}^4 R_{ij}s_j|^2 - \min_{\underline{x} \in X_{4,2,0}} \sum_{i=1}^4 |\hat{y}_i - \sum_{j=i}^4 R_{ij}s_j|^2$



Maximum Likelihood (ML) Demodulation

■ Formula

– $s_1 \sim s_4$: one of $\left(\frac{1}{\sqrt{2}} + \frac{1}{\sqrt{2}}\mathbf{j}\right)$, $\left(-\frac{1}{\sqrt{2}} + \frac{1}{\sqrt{2}}\mathbf{j}\right)$, $\left(\frac{1}{\sqrt{2}} - \frac{1}{\sqrt{2}}\mathbf{j}\right)$, and $\left(-\frac{1}{\sqrt{2}} - \frac{1}{\sqrt{2}}\mathbf{j}\right)$

– At $\sum_{i=1}^4 \left| \hat{y}_i - \sum_{j=i}^4 R_{ij} s_j \right|^2$ part:

- 4th entry: $\hat{y}_4 - R_{44}s_4 = a + bj \rightarrow a^2 + b^2$

- 3rd entry: $\hat{y}_3 - R_{33}s_3 - R_{34}s_4 = c + dj \rightarrow c^2 + d^2$

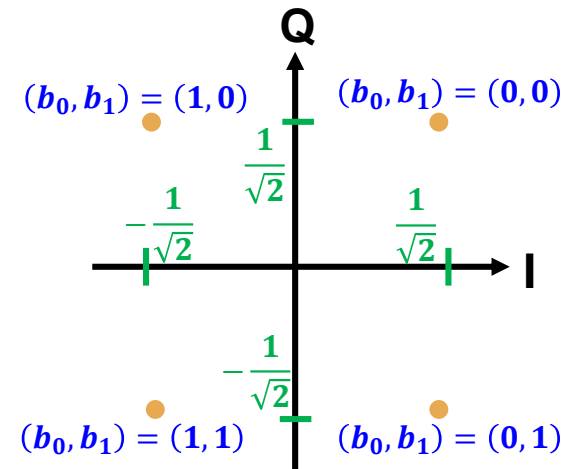
- 2nd entry: $\hat{y}_2 - R_{22}s_2 - R_{23}s_3 - R_{24}s_4 = e + fj \rightarrow e^2 + f^2$

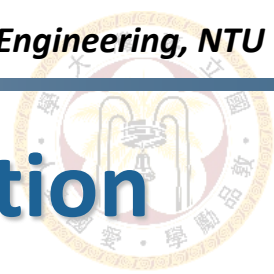
- 1st entry: $\hat{y}_1 - R_{11}s_1 - R_{12}s_2 - R_{13}s_3 - R_{14}s_4 = g + hj \rightarrow g^2 + h^2$

– $\sum_{i=1}^4 \left| \hat{y}_i - \sum_{j=i}^4 R_{ij} s_j \right|^2 = a^2 + b^2 + c^2 + d^2 + e^2 + f^2 + g^2 + h^2$

Maximum Likelihood (ML) Demodulation

- QPSK constellation [1]
 - $\mathbf{x}_1 \sim \mathbf{x}_4$: one of (0,0), (1,0), (0,1), and (1,1)
 - $\mathbf{s}_1 \sim \mathbf{s}_4$: one of $\left(\frac{1}{\sqrt{2}} + \frac{1}{\sqrt{2}}\mathbf{j}\right)$, $\left(-\frac{1}{\sqrt{2}} + \frac{1}{\sqrt{2}}\mathbf{j}\right)$, $\left(\frac{1}{\sqrt{2}} - \frac{1}{\sqrt{2}}\mathbf{j}\right)$, and $\left(-\frac{1}{\sqrt{2}} - \frac{1}{\sqrt{2}}\mathbf{j}\right)$
 - Total 256 ($=4^4$) possibilities for 4-layer QPSK
 - **Full search with 256 possibilities**

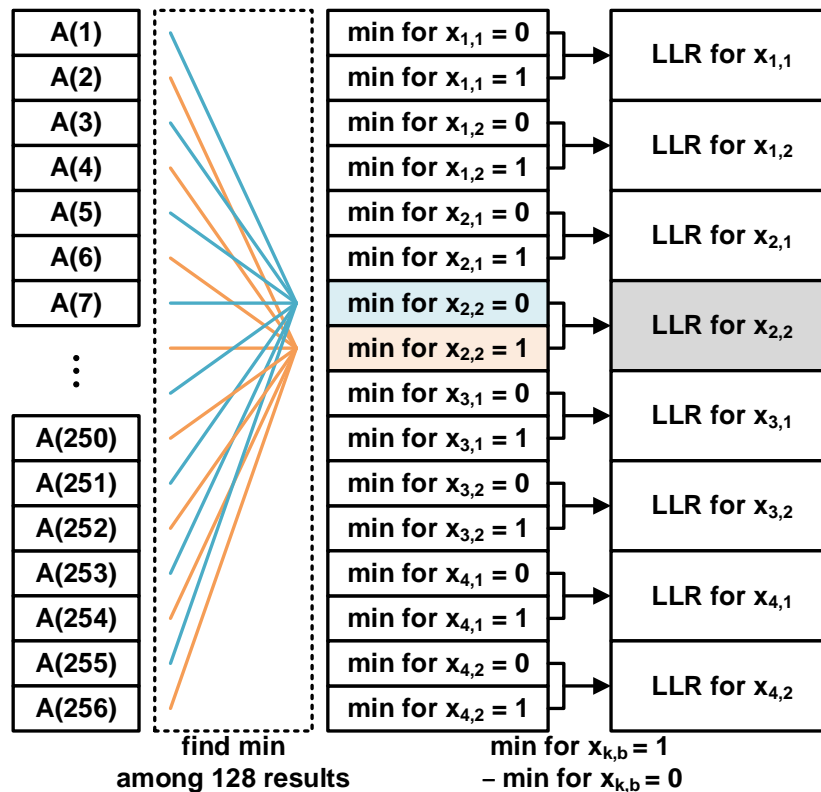


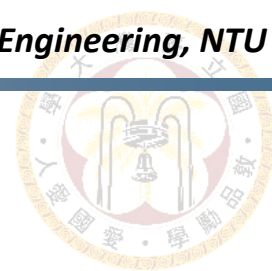


Maximum Likelihood (ML) Demodulation

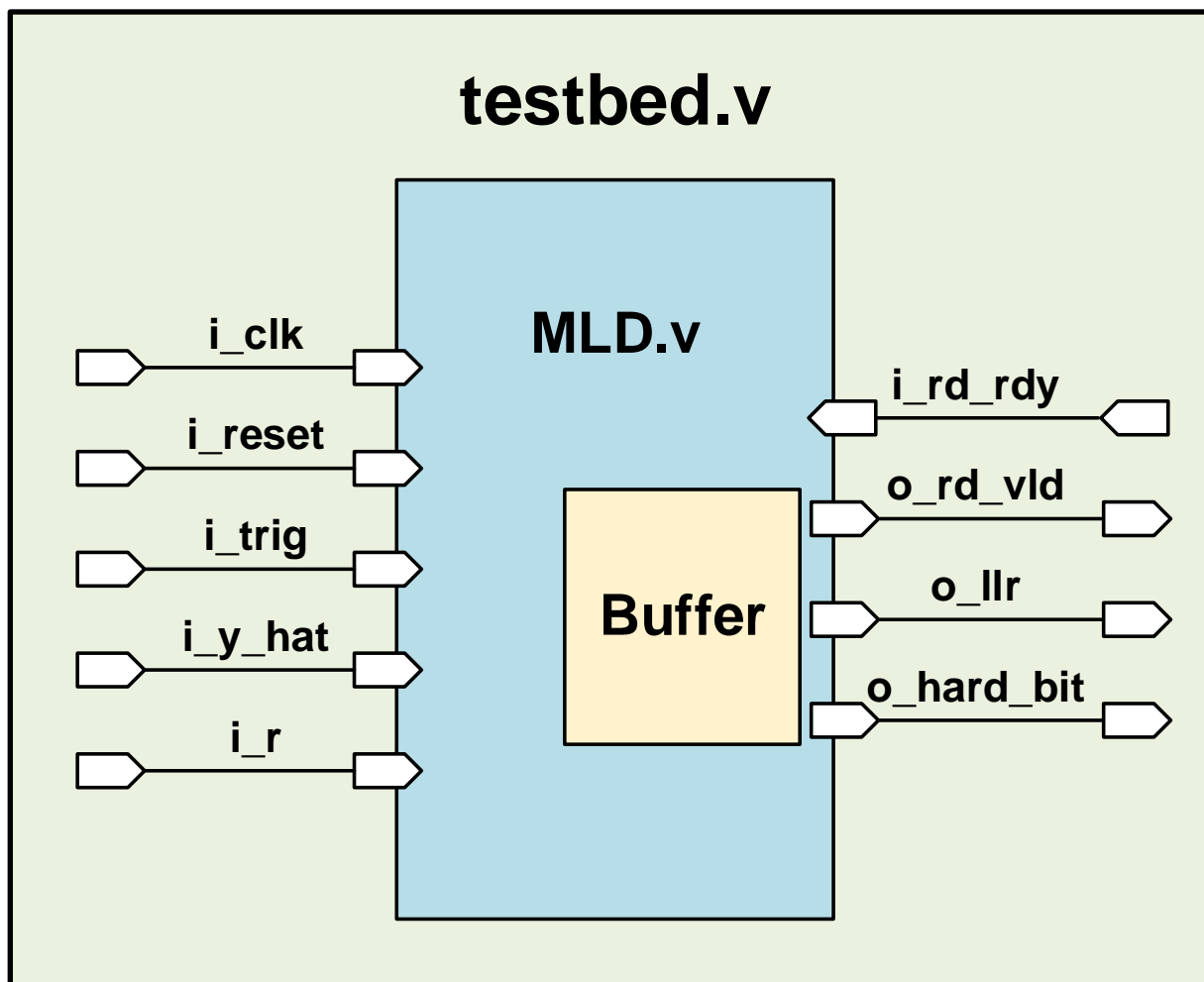
- Compute $\sum_{i=1}^4 \left| \hat{y}_i - \sum_{j=i}^4 R_{ij} s_j \right|^2$ for each A(path M), M=1~256
 - Bring in total **256 results** to compute each bit LLR, exactly **128 results** for $\mathbf{X}_{k,b,0}$ and $\mathbf{X}_{k,b,1}$ **without overlapping**

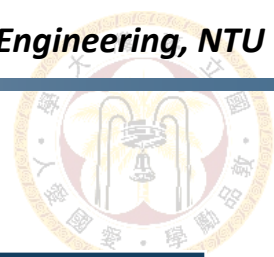
- A**: a set of all combinations of s_1 - s_4 with total $4^4 = 256$ combinations
- A(M)**: one of the combination





Block Diagram

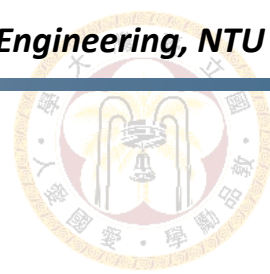




Input/Output

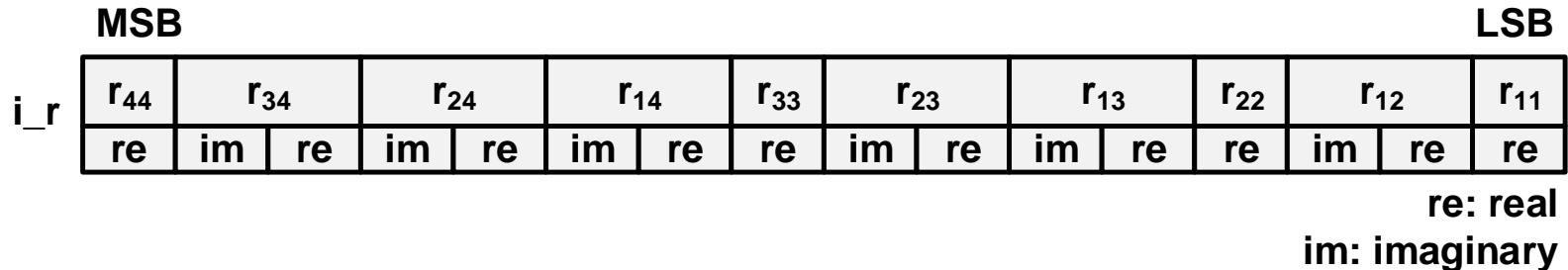
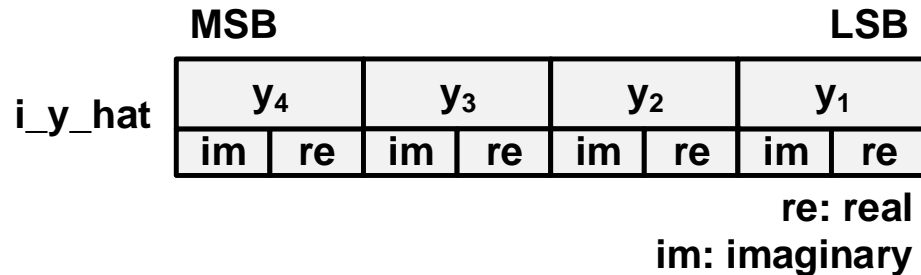
Signal Name	I/O	Width	Simple Description
i_clk	I	1	本系統為同步於時脈正緣之同步設計。 (註: Host端採clk正緣時送資料。)
i_reset	I	1	高位準“非”同步(active high asynchronous)之系統重置信號。
i_trig	I	1	輸入資料有效控制訊號。當為high時i_y_hat與i_r有效。
i_y_hat	I	160	\hat{y} 資料傳輸，包含4筆，每筆各40 bits，i_y_hat [159:120] 為 y_4 ， i_y_hat [119:80] 為 y_3 ，依此類推，每筆資料包含虛部與實部 ({imaginary, real})，各20位元，為{S3.16}之fixed point。
i_r	I	320	R資料傳輸，依序為 $\{r_{44}, r_{34}, r_{24}, r_{14}, r_{33}, r_{23}, r_{13}, r_{22}, r_{12}, r_{11}\}$ ， r_{ij} 僅 包含實部，為20位元，{S3.16}之fixed point， r_{ij} 則包含虛部與實 部({imaginary, real})，各20位元，同樣為{S3.16}之fixed point。
i_rd_rdy	I	1	準備讀取資料控制訊號。當為High時，表示準備好接收資料。
o_rd_vld	O	1	輸出資料有效之控制訊號。當為High時，表示目前輸出的 o_llr 與 o_hard_bit 為有效的。
o_llr	O	8	輸出llr。一次輸1bit的llr，為{S3.4}之fixed point，詳細參考 ML demodulation。
o_hard_bit	O	1	輸出hard bit。一次輸出1bit的hard bit，詳細參考 ML demodulation。

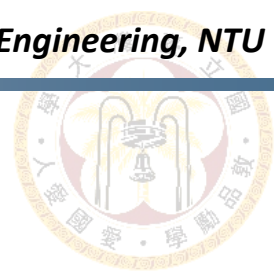
{SA.B}: fixed point with sign bit, A-bit integer, and B-bit fraction



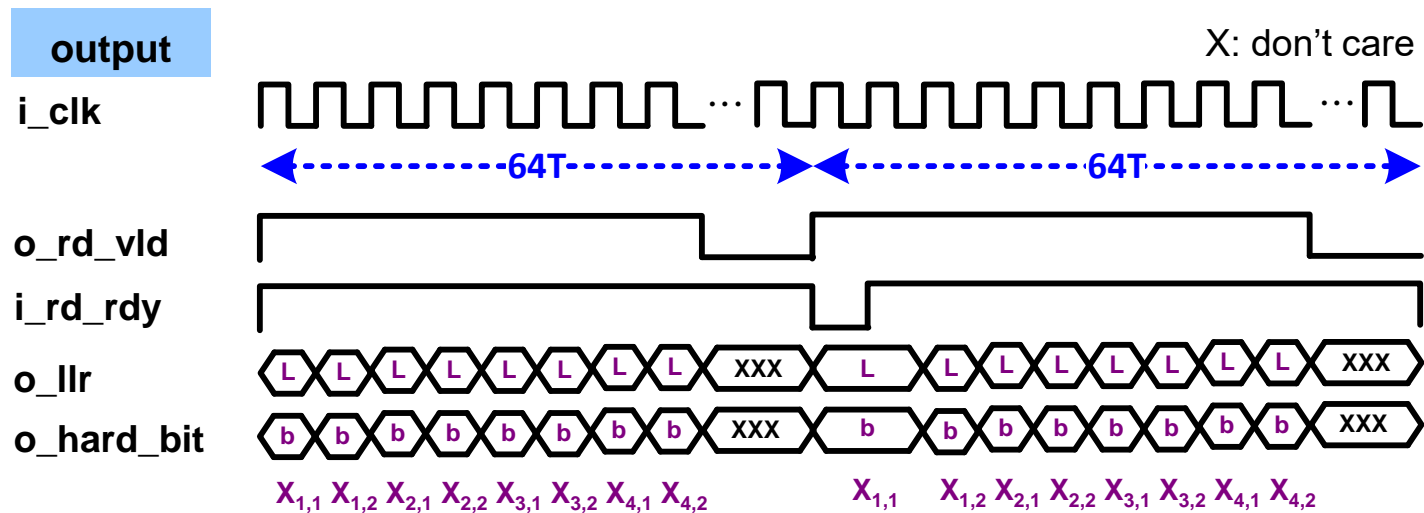
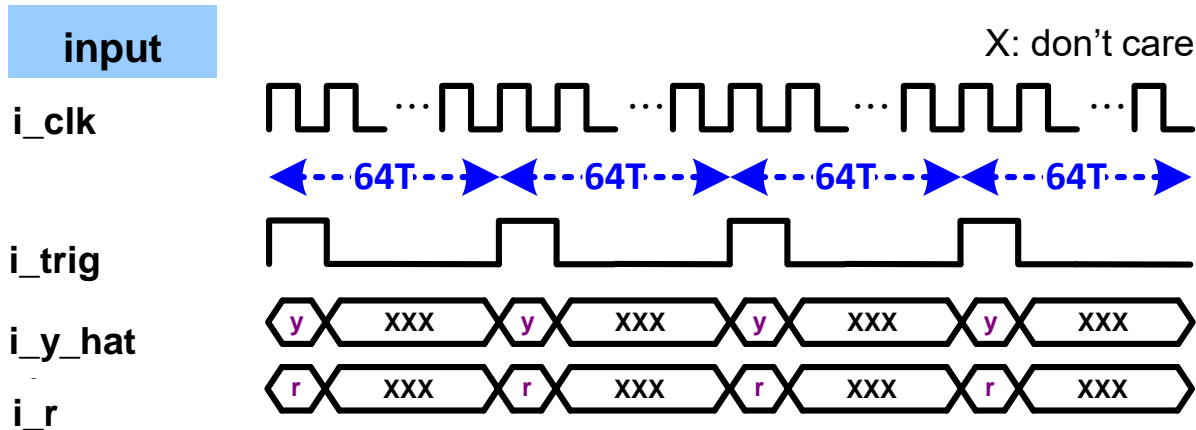
Data format

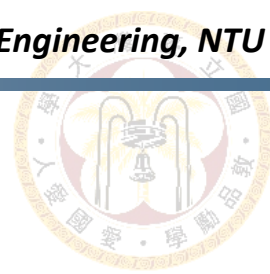
- i_y_hat and i_r
 - Real and imaginary are both S3.16





Waveform



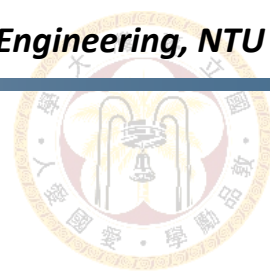


Waveform

- Output buffer depth evaluation
 - i_rd_rdy is high randomly, be high **128T** every **640T**
 - The worst case:

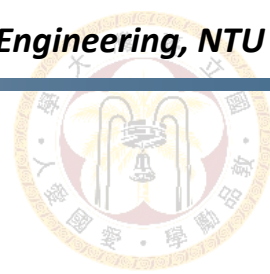


- Buffer should store at least $1024T/64T = 16$ REs output



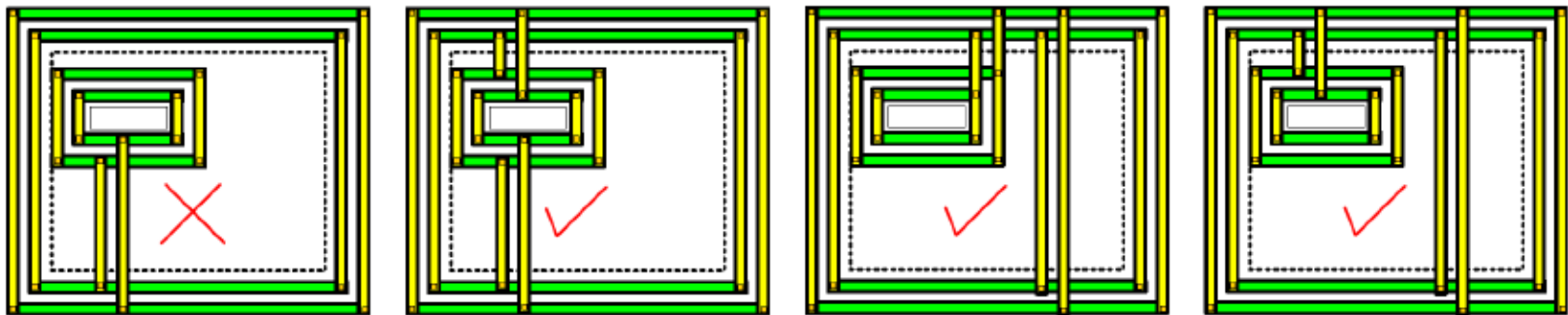
Specification

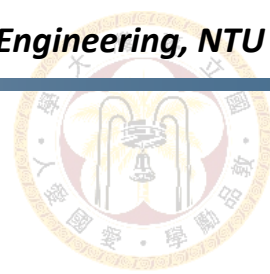
- Only worst-case library is used for synthesis and APR.
- The slack for setup-time should be non-negative.
- **No any timing violation and glitches** for the gate level simulation and post-layout simulation.



Specifications for APR (1)

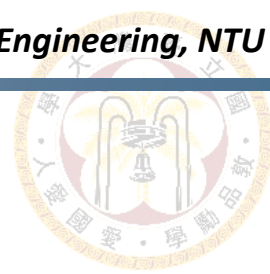
- 只需做 Marco layout 即不用包含 IO Pad 、 Bonding Pad)
- VDD 與 VSS Power Ring 寬度請各設定為 **2um** 只須做一組
- 不需加 Dummy Metal
- **Power Stripe** 務必至少加一組，其 VDD 、 VSS 寬度各設定為 **2um**
 - **Power Stripe** 垂直方向至少一組，水平方向可不加





Specifications for APR (2)

- 務必要加 Power Rail (follow pin)
- Core Filler 務必要加
- APR 後之 GDSII 檔案務必產生
- 完成 APR DRC/LVS 完全無誤
- 記得先產生 ml_demodulator.ioc，再重新讀取該檔來設定 pin position

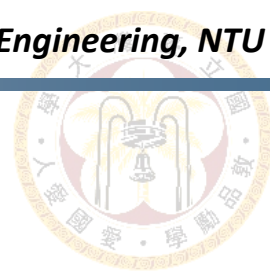


Grading Policy

- **Baseline** 50% + **Performance** 40% + **Report** 10%

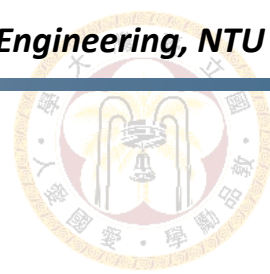
Item	%	Description
RTL Simulation	20	Pass full pattern simulation with specs
Synthesis	10	Pass gate-level sim
APR	20	Finish APR with no DRC/LVS errors Pass post-layout simulation
Performance	40	Area x Time x Power
Report	10	1. Algorithm 2. Performance 3. Hardware implementation

Violation	Penalty
Gate-level sim pass but post-sim fail	Performance*0.5
Only RTL pass	Performance不評分
違反繳交格式與規則	總分-3



Grading Policy - Test Pattern

- AWGN channel
- Total 6 packets,
 - 3 Packets: SNR = 10dB, Data Error Rate < 0.12
 - 3 Packets: SNR = 15dB, Data Error Rate < 0.01
 - If any LLR == 0, it will be identified as fail data
- Total 1000 data RE at each packet



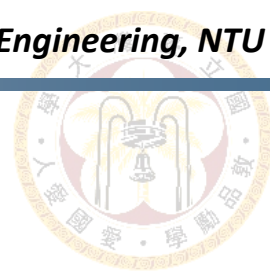
Data Error Rate

- Any of the 8 hard bits is wrong or any LLR = 0, this data is identified as fail data

Golden hard bit: 1 0 0 0 1 0 1 1

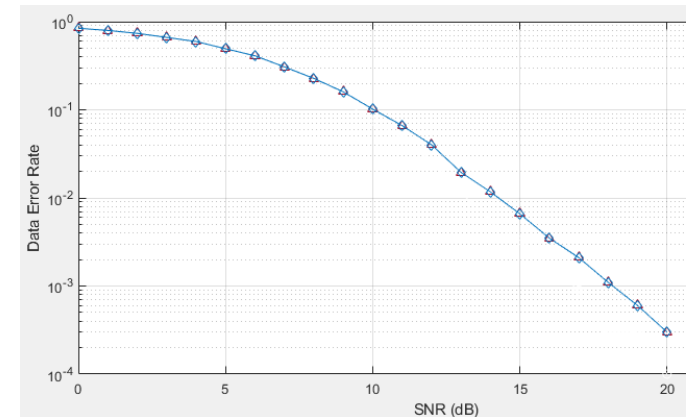
Your result: 1 0 **1** 0 1 0 1 1 → fail

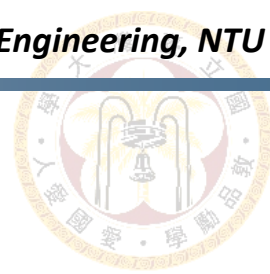
- Total 1000 data in one packet
- Data error rate = # of fail data / 1000



Grading Policy - Report

- Algorithm
 - ML demod. algorithm introduction
 - FXP setting
- Performance
 - The plot with Data Error Rate vs. SNR
- HW implementation
 - HW scheduling
 - HW block diagram
 - Area / Power / Latency report
 - Technique sharing for HW improvement



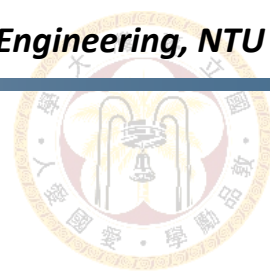


Submission (1)

- **Due Tuesday, June 6, 23:59**
 - **No late submission**
- **Require data (with the required directory hierarchy):**

Violation	Penalty
01_RTL	1. All design Verilog files 2. rtl.f
02_SYN	1. Area/timing reports
03_GATE	1. ml_demodulator_syn.v/sdf 2. rtl.f
04_APR	1. All design database 2. ml_demodulator.gds
05_POST	1. ml_demodulator_pr.v/sdf 2. rtl.f
reports	1. design.spec. 2. teamXX_report.pdf

- **Final project presentation (MTK experience sharing)**
 - **Date: June 13, 2023**

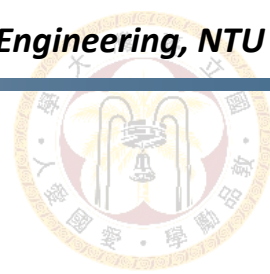


Submission (2)

- Create a folder named `teamID_final_project` and follow the hierarchy below

```
team03_final_project
├── 01_RTL
│   ├── m1_demodulator.v (and other verilog files)
│   └── rtl.f
├── 02_SYN
│   ├── m1_demodulator.area
│   ├── m1_demodulator.max.timing
│   └── m1_demodulator.min.timing
├── 03_GATE
│   ├── m1_demodulator_syn.sdf
│   ├── m1_demodulator_syn.v
│   └── rtl.f
├── 04_APR
│   ├── route
│   ├── route.dat
│   └── m1_demodulator.gds
├── 05_POST
│   ├── m1_demodulator_pr.sdf
│   ├── m1_demodulator_pr.v
│   └── rtl.f
└── reports
    ├── design.spec
    └── team03_report.pdf
```

- Compress the folder `teamID_final_project` in a tar file named `teamID_final_project_vk.tar` (k is the number of version, k =1,2,...), e.g. **team03_final_project_v1.tar**
- Submit to NTU Cool



Reference

- [1] 5G 3GPP spec 38.211 : [Link](#)
- [2] Parallel High Throughput Soft-output Sphere Decoder : [Link](#)
- [3] Gram-Schmidt process : [Link](#)