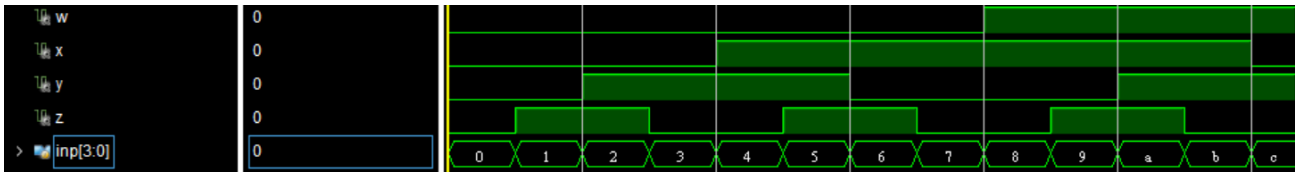
Lab01

Experiment 1:

1 Design and verify a binary-to-Gray-code converter for a Gray code sequence with 10 code words (input: ***abcd***, output: ***wxyz***, ***a*** and ***w*** are the MSB).
- 1.1 Derive the Boolean function/logic equation.
- 1.2 Draw the related logic diagram.
- 1.3 Construct the Verilog RTL code for the converter and use a testbench to simulate the logic behavior for verification.

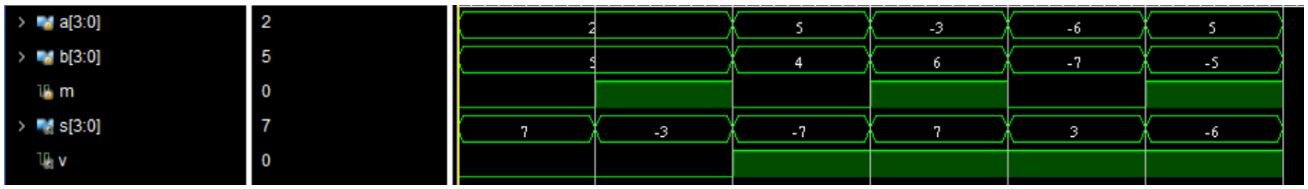
Result:



Experiment 2:

2 Design a signed 4-bit binary adder/subtractor with input ***a*** ($\mathbf{a_3a_2a_1a_0}$), ***b*** ($\mathbf{b_3b_2b_1b_0}$), **m** as the operator control (0 for addition and 1 for subtraction); output **s** ($\mathbf{s_3s_2s_1s_0}$), **v** as overflow indicator.
- 2.1 Derive the Boolean function/logic equation.
- 2.2 Draw the related logic diagram.
- 2.3 Construct the Verilog RTL code for the function and use a given testbench to simulate the logic behavior for verification.

Result:



Experiment 3:

3 (Bonus) For three 3-bit signed numbers ***a*** ($\mathbf{a_2a_1a_0}$), ***b*** ($\mathbf{b_2b_1b_0}$), and ***c*** ($\mathbf{c_2c_1c_0}$), build a logic circuit to output ***o***($\boldsymbol{o_2o_1o_0}$) as the smallest number and use a given testbench for verification.

Result: