

Lab03

Experiment 1:

- 1 Frequency Divider: Construct a 27-bit synchronous binary counter. Use the MSB of the counter, we can get a frequency divider which provides a $1/2^{27}$ frequency output (f_{out}) of the original clock ($f_{crystal}$, 100MHz). Construct a frequency divider of this kind.
 - 1.1 Write the specification of the frequency divider.
 - 1.2 Draw the block diagram of the frequency divider.
 - 1.3 Implement the frequency divider with the following parameters.

I/O	$f_{crystal}$	f_{out}
Site	W5	U16

Result:

<https://lurl.cc/vFpb0>

Experiment 2:

- 2 Frequency Divider: Use a count-for-50M counter and some glue logics to construct a 1 Hz clock frequency. Construct a frequency divider of this kind.
 - 2.1 Write the specification of the frequency divider.
 - 2.2 Draw the block diagram of the frequency divider.
 - 2.3 Implement the frequency divider with the following parameters.

I/O	$f_{crystal}$	f_{out}
Site	W5	U16

Result:

<https://lurl.cc/Pn04X>

Experiment 3:

- 3 Implement pre-lab1 with clock frequency of 1 Hz.

I/O	$f_{crystal}$	q ₃	q ₂	q ₁	q ₀
Site	W5	V19	U19	E19	U16

Result:

<https://lurl.cc/IiFQa>

Experiment 4:

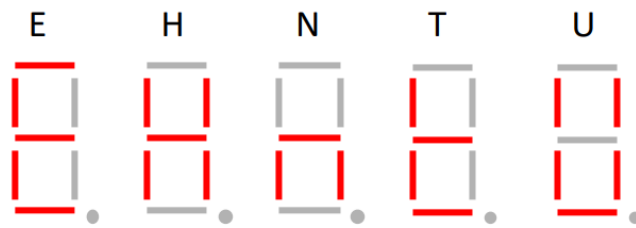
- 4 Implement pre-lab2 with clock frequency of 1 Hz. The I/O pins can be assigned by yourself.

Result:

<https://lurl.cc/g3HLv>

Experiment 5:

- 5 Use the idea from pre-lab2. We can do something on the seven-segment display. Assume we have the pattern of E, H, N, T, U for seven-segment display as shown below. Try to implement the scrolling pre-stored pattern "NTHUEE2023" with the four seven-segment displays.



Result:

<https://lurl.cc/uNbdZ>