This README file serves as a guide to understand the purpose of each file and folder contained within this ZIP file.

Cadence Project Folders

This ZIP file contains three folders with Cadence files: ece_482_pdn_v2, final_proj_ece482, and wei_final_project. The top-level design is found in **ece_482_pdn_v2** under the cell "**pdn_rev3**". However, all three of these folders are necessary to properly open the top-level design, as the cells used to make the top-level design are spread across these three folders.

HSpice Files

This ZIP files contains 10 HSpice netlist files. 5 of them correspond to simulating the top-level design with test bench 1 under all 5 process corners, while the remaining 5 correspond to simulating the top-level design with test bench 2 under all 5 process corners. Each files uses the following naming convention:

4BitMultiplier_[test bench]_[process corner].cir

(e.g. the file 4BitMultiplier_tb1_tt.cir contains the netlist used to simulate the top-level design with test bench 1 in the TT process corner).

Project Report.pdf

This PDF corresponds to the final report for this project.