UCD School of Electrical and
Electronic Engineering

EEEN40280
Digital and Embedded Systems

AHB-Lite GPIO Block

Overview

This is a simple general-purpose input-output (GPIO) block, designed to be a slave on an AHB-Lite bus. The block provides two 16-bit output ports and two 16-bit input ports.

Programmer's Model

The GPIO block presents four 32-bit registers to the processor, as shown in the table below. Byte writes are supported. Only the rightmost 16 bits in each register are active, others will be ignored on write and will read as 0.

Register	Relative Address	Access	Description
out0	0x0	R/W	Value written to bits 15:0 appears on gpio_out0 port, and can be read back from the register (not from the port).
out1	0x4	R/W	As above, but for gpio_out1 port.
in0	0x8	R	Read gives value on gpio_in0 port, synchronised with the bus clock, as bits 15:0.
in1	0xC	R	As above, but for gpio_in1 port.

Implementation

The RTL diagram is shown below. This hardware is described in Verilog in the file `AHBgpio.v` and a simple testbench is provided as `TB_AHBgpio.v`.

All registers operate on the bus clock, with synchronous active-low reset. External inputs are assumed asynchronous and are synchronised using pairs of flip-flops, to minimise risk.

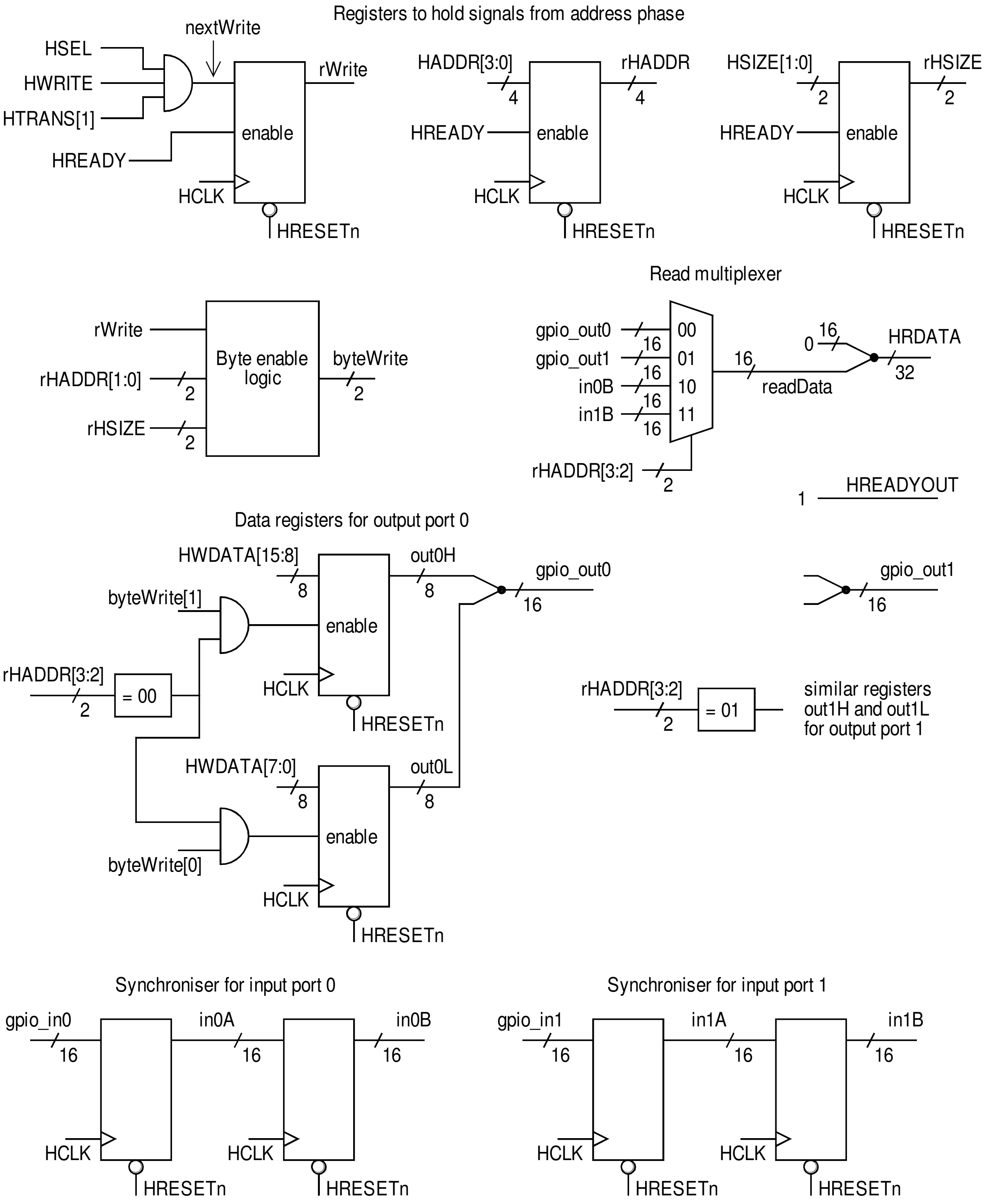
Registers hold the relevant bits of the address and size control signals from the address phase of each bus transaction, for use in the data phase. A write enable signal is generated during the address phase, and held for use in the data phase also.

The output data registers are implemented as pairs of 8-bit registers, to allow individual byte writes. The byte enable logic is shown in the table below. The byteWrite signals are combined with address decoding to enable the appropriate registers.

Transfer Size	rWrite	rHSIZE [1:0]	rHADDR [1:0]	byteWrite	Description
Word	1	10	00	11	Word transfer, write both bytes
Half	1	01	00	11	Lower half-word, write both bytes
Byte	1	00	00	01	Lowest byte, write low byte only
Byte	1	00	01	10	Next byte, write high byte only
?	?	??	??	00	Ignore all other combinations

A read multiplexer selects the required 16-bit value for read transfers, based on the held address bits. This is combined with 16 zero bits to give a 32-bit read value.

No wait states are needed, so HREADYOUT is always 1.



Registers to hold signals from address phase
nextWrite
HSEL
HWRITE
HTRANS[1]
HREADY
enable
rWrite
HCLK
HRESETn
HADDR[3:0]
4
rHADDR
4
HREADY
enable
HCLK
HRESETn
HSIZE[1:0]
2
rHSIZE
2
HREADY
enable
HCLK
HRESETn
rWrite
rHADDR[1:0]
2
rHSIZE
2
Byte enable logic
byteWrite
2
Read multiplexer
gpio_out0
16
gpio_out1
16
in0B
16
in1B
16
00
01
10
11
rHADDR[3:2]
2
16
readData
0
16
HRDATA
32
1
HREADYOUT
Data registers for output port 0
HWDATA[15:8]
8
byteWrite[1]
enable
out0H
8
gpio_out0
16
rHADDR[3:2]
2
= 00
HCLK
HRESETn
HWDATA[7:0]
8
byteWrite[0]
enable
out0L
8
HCLK
HRESETn
gpio_out1
16
rHADDR[3:2]
2
= 01
similar registers out1H and out1L for output port 1
Synchroniser for input port 0
gpio_in0
16
in0A
16
in0B
16
HCLK
HRESETn
HCLK
HRESETn
Synchroniser for input port 1
gpio_in1
16
in1A
16
in1B
16
HCLK
HRESETn
HCLK
HRESETn