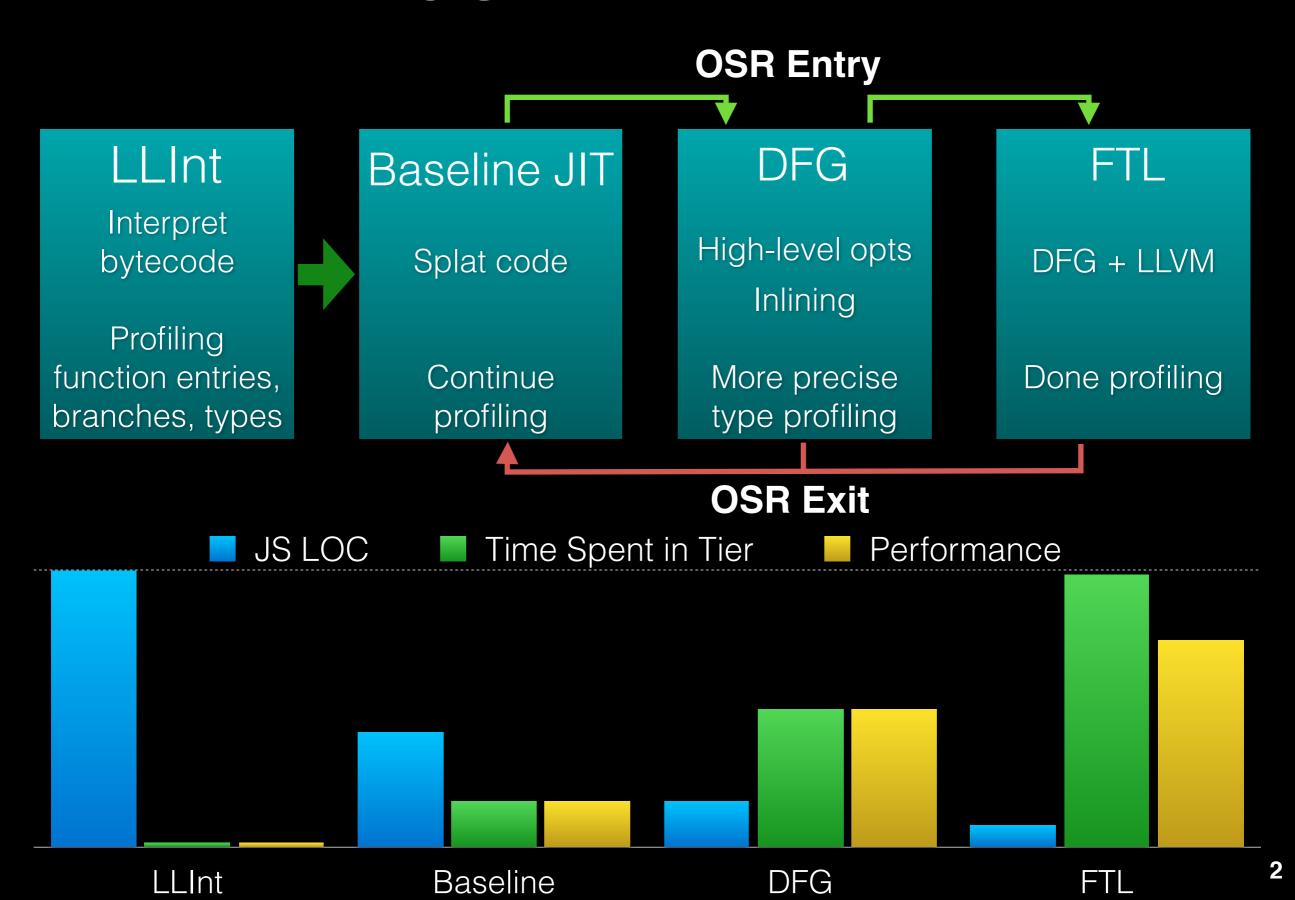


Andrew Trick, Apple Juergen Ributzka, Apple

LLVM Developers' Meeting 2014 San Jose, CA

### WebKit JS Execution Tiers



# Optimizing FTL Code

As with any high-level language...

FTL does...

1. Remove abstraction

**Speculative Type Inference** 

2. Emit the best code sequence for common operations

**Patchpoint** 

3. Do everything else

**LLVM Pass Pipeline** 

# Patchpoint

- What are they?
- How do they work?

# Patchpoint

Looks like an LLVM IR varargs call

@patchpoint == (i64, i32, i8\*, i32, ...)\*
@llvm.experimental.patchpoint

# Patchpoint - Lowering

```
%result = call i64 @patchpoint.i64
             (i64 7, i32 15, i8* %rtcall, i32 2,
              i64 %arg0, i64 %arg1, i64 %live0, i32 %live1)
                                                  Live Values
                           Call Args
    LLVM IR
                                                (may be spilled)
     to MI
                   Calling Conv. ID
PATCHPOINT 7, 15, 4276996625, 2, 0, %RDI, %RSI,
            %RDX, %RCX,
            <regmask>, %RSP<imp-def>, %RAX<imp-def >,...
                   Call-Clobbers
                                      Return Value Scratch Regs
```

# Patchpoint - Assembly

```
%result = call i64 @patchpoint.i64
(i64 7, i32 15, i8* %rtcall, i32 2, ...)
```

#### 15 bytes reserved

```
0x00 movabsq $0xfeedca11, %r11
0x0a callq *%r11
0x0d nop
0x0e nop
```

The address and call are materialized within that space

The rest is padded with nops

fat nop optimization (x86)
 runtime must repatch all bytes

### Patchpoint - Stack Maps

Call args omitted

```
__LLVM_STACKMAPS section:
callsite 7 @instroffset
has 2 locations
Loc 0: Register RDX
Loc 1: Register RCX
has 2 live-out registers
LO 0: RAX
LO 0: RSP
```

Map ID -> offset (from function entry)

Live Value Locations (can be register, constant, or frame index)

Live Registers
(optional)
allow the runtime
to optimize spills

# Patchpoint

- Use cases
- Future designs

# Inline Cache Example

WebKit patches fast field access code based on a speculated type

```
cmpl $42, 4(%rax)
jne Lslow
leaq 8(%rax), %rax
movq 8(%rax), %rax
movq 8(%rax), %rax
cmpl $53, 4(%rax)
jne Lslow
movq 8(%rax), %rax
movq -16(%rax), %rax
```

Type check + direct field access

Type check + indirect field access

- The speculated shape of the object changes at runtime as types evolve.
- Inline caches allow type speculation without code invalidation - this is a delicate balance.

## AnyReg Calling Convention

- A calling convention for fast inline caches
- Preserve all registers (except scratch)
- Call arguments and return value are allocatable

### Ilvm.experimental.stackmap

- A stripped down patchpoint
- No space reserved inline for patching Patching will be destructive
- Nice for invalidation points and partial compilation
- Captures live state in the stack map the same way
- No calling convention or call args
- Preserves all but the scratch regs

# Code Invalidation Example

#### **Speculatively Optimized Code**

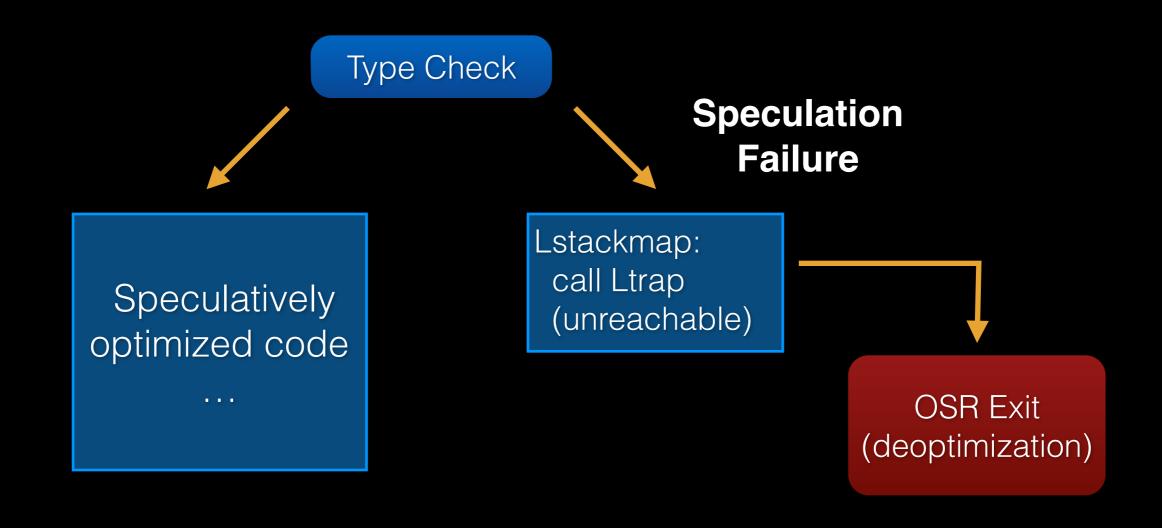
```
Type event triggered (watchpoint)
```

jmp Ltrap

branch target

```
call @RuntimeCall(...)
Lstackmap:
addq ..., %rax
nop
Lstackmap+5:
...
```

# Speculation Check Example



### Using Patchpoints for Deoptimization

- Deoptimization (bailout) is safe at any point that a valid stackmap exists
- The runtime only needs a stackmap location to recover, and a valid reason for the deopt (for profiling)
- Deopt can also happen late if no side-effects occurred - the runtime effectively rolls back state
- Exploit this feature to reduce the number of patchpoints by combining checks

# Got Patchpoints?

- Dynamic Relocation
- Polymorphic Inline Caches
- Deoptimization
  - Speculation Checks
  - Code Invalidation
  - Partial Compilation
- GC Safepoints\*Not in FTL

### Proposal for IIvm.patchpoint

- Pending community acceptance
- Only one intrinsic: Ilvm.patchpoint
- Call attributes will select behavior
  - "deopt" patchpoints may be executed early
  - "destructive" patchpoints will not emit code or reserve space.
- Symbolic target implies callee semantics
- Add a condition to allow hoisting/combining at LLVM level

### Proposal for Ilvm.patchpoint

Optimizing Runtime Checks Using Deoptimization

```
%a = cmp <TrapConditionA>
call @patchpoint(1, %a, <state-before-loop>) deopt
Loop:
%b = cmp <TrapConditionB>
call @patchpoint(2, %b, <state-in-loop>) deopt
(do something...)
```

Can be optimized to this...
As long as C implies (A or B)

```
%c = cmp <TrapConditionC>

@patchpoint(1, %c, <state-before-loop>)

Loop:

(do something...)
```

LLVM as a high performance JIT

```
; <label>:13
                                            ; preds = \%0
 %14 = add i64 \%8, 48
 %15 = inttoptr
 %16 = load i64
%17 = add i64
                   Instructions
 %18 = inttoptr
 %19 = load i64* %18, !tbaa !5
 %20 = icmp ult i64 %19, -281474976710656
 br i1 %20, label %21, label %22, !prof !3
; <label>:21
 <label>:21
call void (i64
                 Instruction 4 3, i32 5, i64 %19)
 unreachable
; <label>:22
                                            ; preds = %13
 %23 = trunc i6
 %24 = add i64
                    Instructions
 %25 = inttoptr
 %26 = load i64
 %27 = icmp ult i64 %26, -281474976710656
 br i1 %27, label %28, label %29, !prof !3
; <label>:28
 call void (i64 1 Instruction 1 4, i32 5, i64 %26) unreachable
; <label>:29
                                            ; preds = \%22
 %30 = trunc i64 \%26 to i32
 %31 = add i64
 %32 = inttoptr
                    Instructions
 %33 = load i64
 %34 = and i64
 %35 = icmp eq 164 %34, 0
 br i1 %35, label %36, label %37, !prof !3
 call void (i64 1 Instruction 1 5, i32 5, i64 %33, i32 %23, i32 %30
; <label>:36
i32 %23, i32 %30
 unreachable
```

Many small BBs

```
; <label>:13
                                               ; preds = \%0
 %14 = add i64 \%8, 48
 %15 = inttoptr i64 %14 to i64*
 %16 = load i64* %15, !tbaa !4
 %17 = add i64 \%8, 56
 %18 = intto
                     1474976710656
 %19 = load
 %20 = icmp
 br i1 %20, Laber %21, raber %22, !prof
; <label>:21
                                               ; preds = %13
 call void (i64, i32, ...)* @llvm.experimental.stackmap(i64 3, i32 5, i64 %19)
 unreachable
; <label>:22
                                               ; preds = %13
 %23 = trunc i64 \%19 to i32
 %24 = add i64 \%8, 64
 %25 = inttoptr i64 %24 to i64*
 %26 = load
              -281474976710656
 %27 = icmp
 br i1 %27,
; <label>:28
 call void (i64, i32, ...)* @llvm.experimental.stackmap(i64 4, i32 5, i64 %26)
 unreachable
; <label>:29
                                               ; preds = \%22
 %30 = trunc i64 \%26 to i32
 %31 = add i64 \%8, 72
 %32 = intto
               281474976710656
 %33 = load
 %34 = and i
 %35 = icmp
 br i1 %35, label %36, label %37, !prof !3
; <label>:36
                                               ; preds = %29
 call void (i64, i32, ...)* @llvm.experimental.stackmap(i64 5, i32 5, i64 %33,
i32 %23, i32 %30)
 unreachable
```

- Many small BBs
- Many large constants

```
5699271192

store i64 %54, i64* inttoptr (i 5682233400)
%55 = load double* inttoptr (i6 6 6 6 8 2 2 3 3 4 5 6 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 4 5 6 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 4 5 6 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 3 5 1 2 6 8 1 0 ad double* inttoptr (i6 6 6 8 2 2 3 3 3 5 1 2 6
```

- Many small BBs
- Many large constants
- Many similar constants

- Many small BBs
- Many large constants
- Many similar constants
- Some Arithmetic with overflow checks
- Lots of patchpoint/stackmap intrinsics

# Constant Hoisting

- Reduce materialization of common constants in every basic block
- Coalesce similar constants into base + offset
- Works around SelectionDAG limitations
- Optimizes on function level

### LLVM Optimizations for FTL

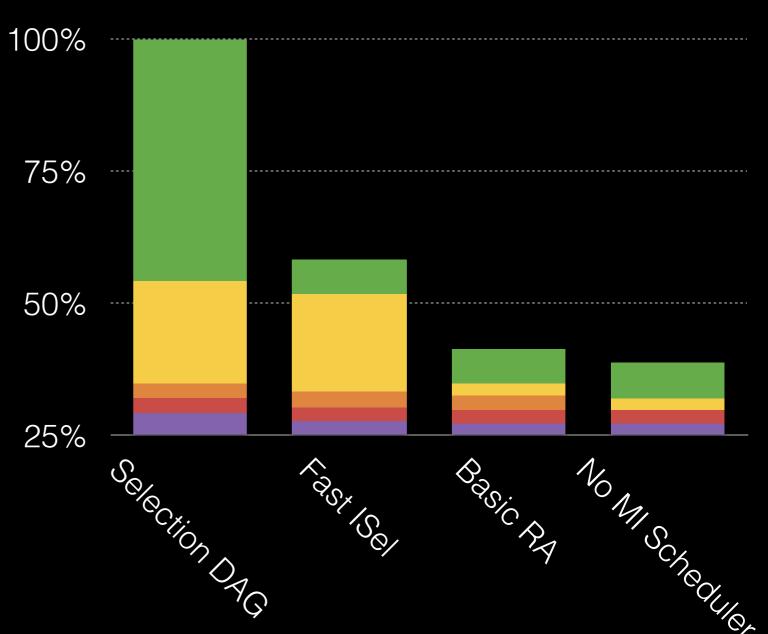
- Reduced OPT pipeline
  - InstCombine
  - SimplifyCFG
  - GVN
  - DSE
- TBAA
- Better ISEL
- Good register allocation

# Compile Time Is Runtime

Codegen Compile Time



- Register Allocator
- MI Scheduler
- Machine Dominator Tree (6)
- Misc



### Reference

- Filip Pizlo's WebKit FTL blog post https://www.webkit.org/blog/3362/introducing-the-webkit-ftl-jit
- Filip Pizlo's Lightning Talk from LLVM Dev, Nov 2013: <a href="http://llvm.org/devmtg/2013-11/videos/Pizlo-JavascriptJIT-720.mov">http://llvm.org/devmtg/2013-11/videos/Pizlo-JavascriptJIT-720.mov</a>
- Andrew Trick's LLVM blog post on compilation with FTL: <a href="http://blog.llvm.org/2014/07/ftl-webkits-llvm-based-jit.html">http://blog.llvm.org/2014/07/ftl-webkits-llvm-based-jit.html</a>
- Current stack maps and patch points in LLVM: http://llvm.org/docs/StackMaps.html
- Proposal for a first-class llvm.patchpoint intrinsic: TBD: llvm-dev list
- LLVM implementation details:
   Much of the work done by Juergen Ributzka and Lang Hames

# Questions?