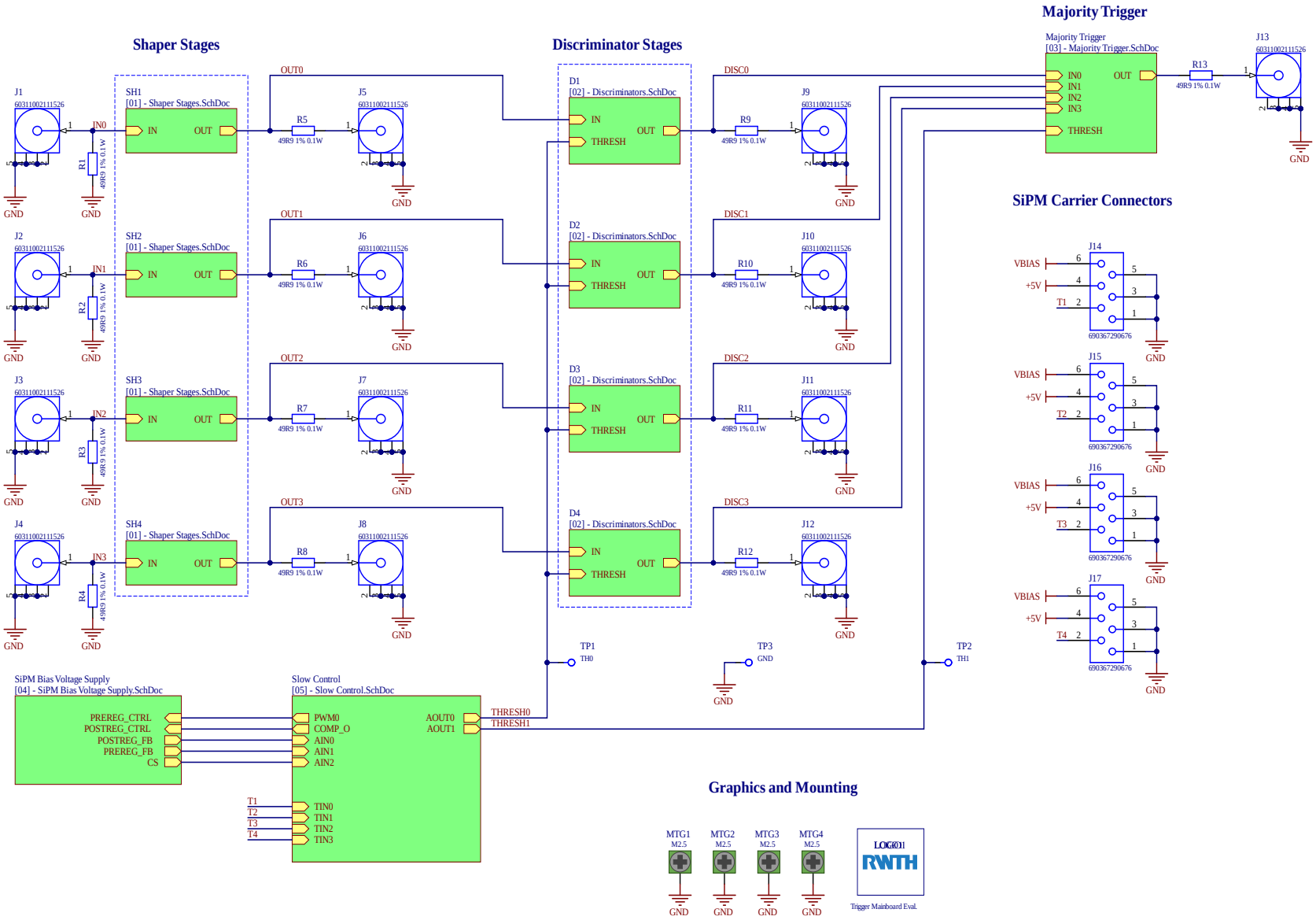

PROJECT	Trigger Mainboard.PrjPcb			
TITLE	**[00] - Top Sheet.SchDoc**			
DESC.				
REVISION	0	DATE 17.08.2020	SHEET 1 OF 6	
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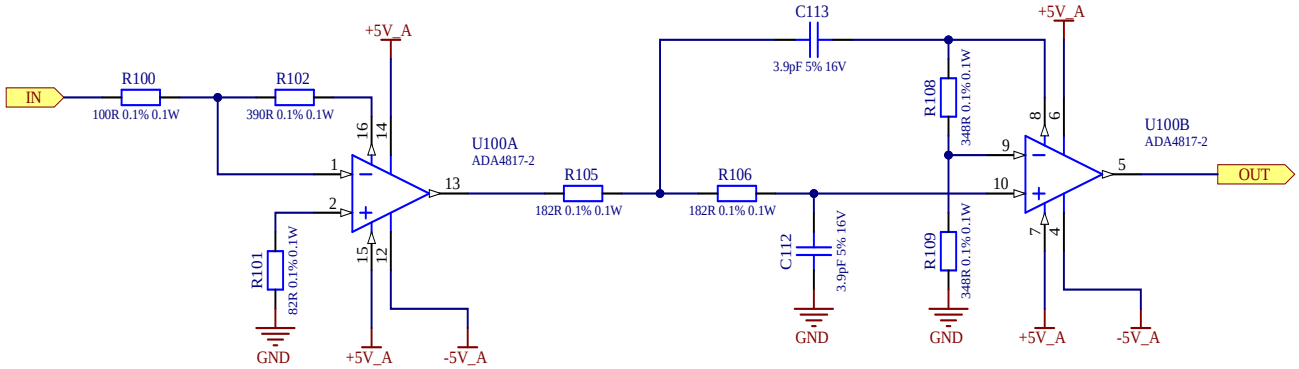
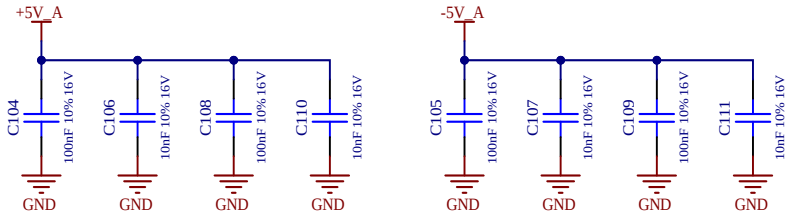
Two Stage Shaper

Inverter (G=-4, BW=210MHz) and 2nd order sallen key low pass filter (G=+4, BW=90MHz, see datasheet p. 22)



Power Supply Bypass

For recommended values refer datasheet p. 23



PROJECT	Trigger Mainboard.PrjPcb			
TITLE	**[01] - Shaper Stages.SchDoc**			
DESC.				
REVISION	0	DATE 17.08.2020	SHEET 2 OF 6	
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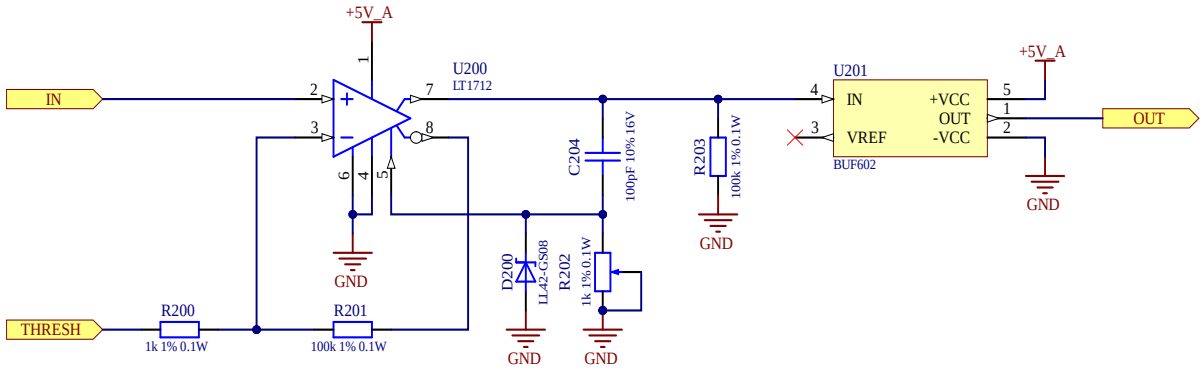
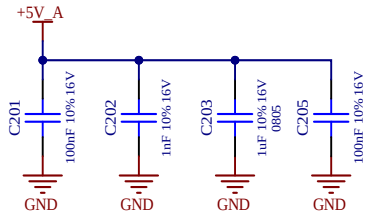
Leading Edge Discriminator

non-inv. comparator with hysteresis (optional) and pulse stretcher (tp = R*C)



Power Supply Bypass



PROJECT	Trigger Mainboard.PrjPcb			
TITLE	**[02] - Discriminators.SchDoc**			
DESC.				
REVISION	0	DATE 17.08.2020	SHEET 3 OF 6	
AUTHOR	Name			

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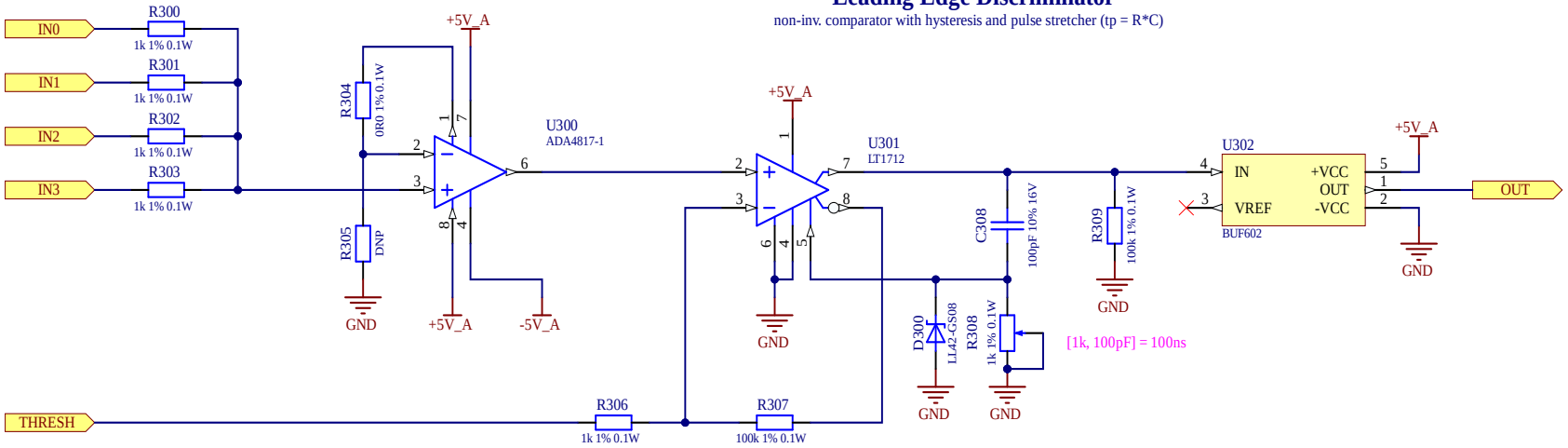
Summing Amplifier

with optional gain (RF = 100...400 recommended, see datasheet p. 20)

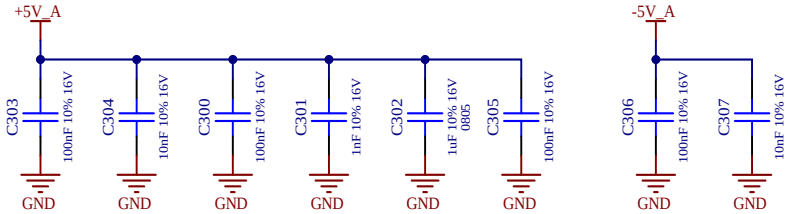
Uout = (U1 + U2 + U3 + U4)/4

Leading Edge Discriminator

non-inv. comparator with hysteresis and pulse stretcher (tp = R*C)



Power Supply Bypass



PROJECT	Trigger Mainboard.PrjPcb			
TITLE	**[03] - Majority Trigger.SchDoc**			
DESC.				
REVISION	0	DATE 17.08.2020	SHEET 4 OF 6	
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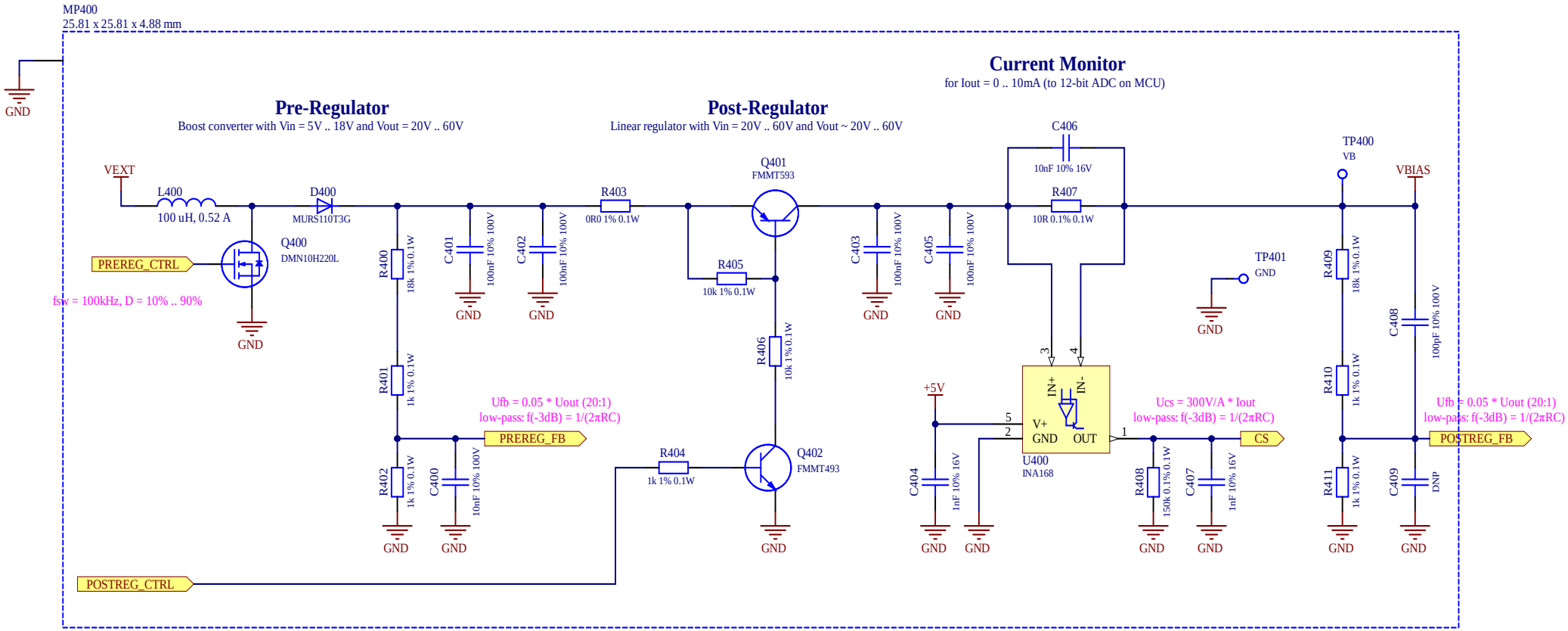

PROJECT	Trigger Mainboard.PrjPcb			
TITLE	[04] - SiPM Bias Voltage Supply.SchDoc			
DESC.				
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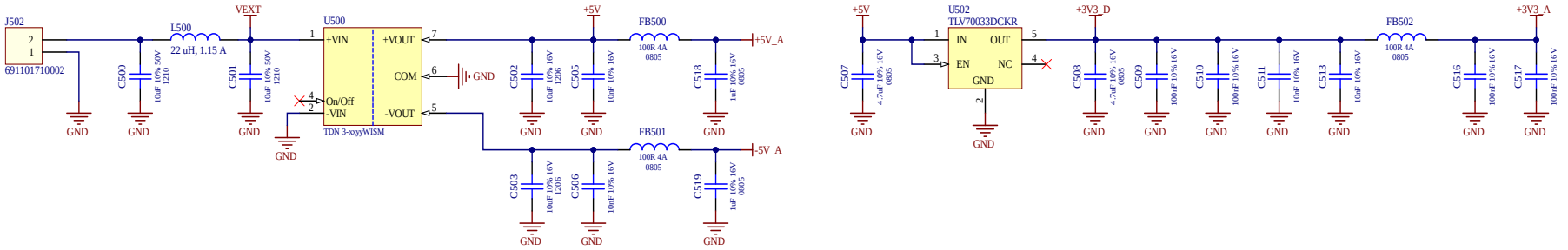
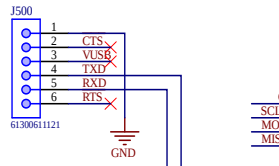
Low Voltage Power Supply



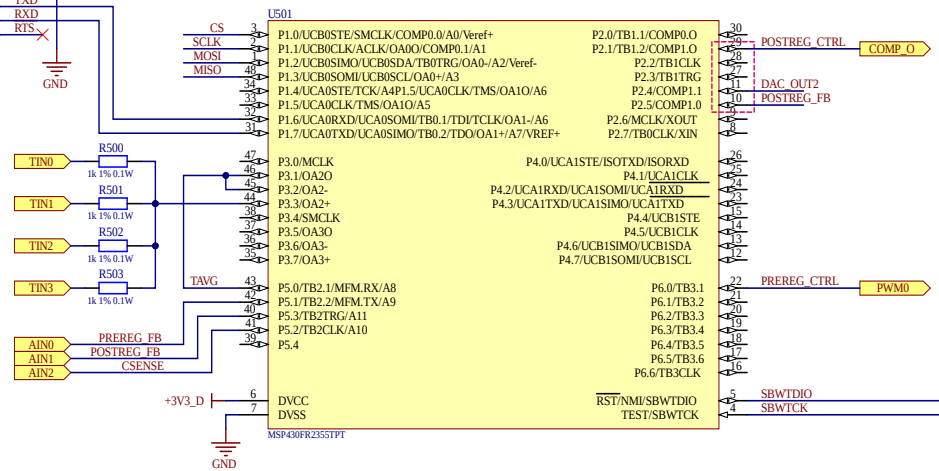
Serial Interface

e.g. FTDI TTL-232R-3V3 smart cable (pinout see datasheet p. 11-12, tab. 4.1)

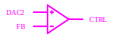


Microcontroller

for pin and signal attributes refer to datasheet (p. 18-25, tab. 4.1-4.2)



Comparator (eComp1)

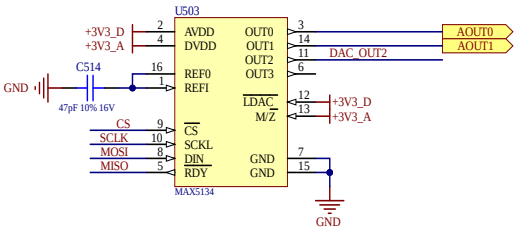


CPPSEL = 001, CPNSEL = 000

16-/12-bit DAC

for post-regulator control and discriminator threshold

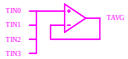
16-bit resolution for post-regulator: 3.3V/2^16*20 = 1.00mV
12-bit resolution for discriminator threshold 3.3V/2^12 = 0.81mV



Summing Amplifier

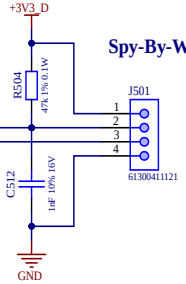
outputs average temperature reading
TAVG = (TIN0 + TIN1 + TIN2 + TIN3)/4

Operational Amplifier (SAC2 OA)

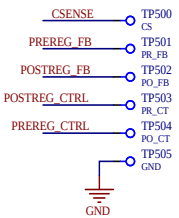


PSEL = 00, NSEL = 00

Spy-By-Wire Header



Some Testpoints ...



PROJECT	Trigger Mainboard.PrjPcb				
TITLE	[05] - Slow Control.SchDoc				
DESC.					
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