Download .pdf for component details

Click on schematic symbols for component data

IceCube Upgrade Mini MB Schematic Revision History:

Rev1 Jan 28 2019

Older Revision Perry
1. Transferred selected design files from PDOM project
2. MCU: Removed Net OSC_MCU_CLOCK from MCU Pin 8 = PC14-OSC32_IN.
3. MCU: Added Test point to OSC_MCU_OUT.
4. ICM: Added ICM_+1V8 net to J1-12. (fixed initial error with connection to J1-8)
5. ICM, XTIO: Changed LVDS signals ICM_CAL_TRIG and ICM_CAL_TIME from 3.3V psuedo-diff to 1.8V Diff SSTL 1 (0.9Vcm).
6. ALL: Re-annotated all sheets.
7. MCU: Removed redundant write-protect bypass jumper.
8. XTIO: Added SMA TRIG OUT and SMA TIME IN connectors, Diff-SE converters and jumper selects.
9. ICM: Added bypass caps on ICM Power in and out
10. MCU: Added connector for Ethernet PHY
11. MCU Changed Ethernet Connector to 2x8 x 0.1"
12. XTIO: Added jumpers for optional termination of LVDS lines
13. XTIO: Fixed net going to Pin2 of P18 to be "ICM_FPGA_CLOCK_N" (was _P)
14. MCU: Changed connector for Ethernet PHY Card to type: SFM-115-X2-XXX-D-A
15. PHY: Removed, LVS1: Removed J1, ICM: Removed USB1 and ICM-JTAG
Feldhäuser:
16. ICM: P1 changed to smaller type
17. ICM: Connect Mini MB B to Mini MB A with PBA, PAB for cable connection
18. ICM: P2 changed to smaller type
19. ICM: P6 changed to smaller type
20. ICM: Connection ICM_FPGA_GPIO_0 to GND cut (R11)
21. ICM: Penetrator from ICM to LVS1 on Mini MB A
22. MCU: P10 changed to smaller type
23 XTIO P13,. P14, P16, P17 changed to smaller type

24. Delete following (only one pin, Electr. Rule Check)
: +5V0_EXT P2-4, ICM_TCK ICM-J1-18, ICM_TDI ICM-J1-14, ICM_TDO ICM-J1-16, ICM_TMS ICM-J1-20 MCU_INTLK U5-46, Aux_P3V3_EN U5-112,
MCU_CAL_A3 U5-47, MCU_GPIO_0 U5-98, MCU_GPIO_01 U5-99, MCU_GPIO_2 U5-113, NetP9_6 P9-6, NetU8_1 U8-1, NetU8_3 U8-3,
NetU12_12 U12-12, NetU12_13 U12-13, NetU12_14 U12-14
25. Delete Floating Net Label MCU_GPIO_3
26. Layer changed in PCB

Mini MB Production History

Rev1.0 Prototype run of (x) PCB Assemblies SN1-SNx

Temprary list made by Perry on 2-27/2-28
MCU: Added Jumpers ID0-ID3 see "DOM_Type_ID_Jumpers" in shared docs
LVS1: Layout note: keep PX3 and PX4 close to each other (from same cable)
LVS1: Added (2) spring contacts for grounding DC-DC converter case.
SLO: Removed L25, L26,L27,L29 Added 2x10uF bypass on magnetormeter U11
ICM: Probably need some ICM JTAG connection?
SLO: Replaced Pressure sensor with different part# for better availability

Revisions.SchDoc			WIPAC Wisconsin IceCube Particle Astrophysics Center
Size: B	Designed: PWS Drafted: PWS Checked: Approve:	Revision:	
Modified: 13.05.2020 Time: 15:40:26		Sheet 1 of 7	
File: Y:\My Hardware\Altium\IceCube\Mini-Mainboard\MMB_Controller (2-27-2020 2-48-15 PM)\Design Projects\Mini MB\Revisions.SchDoc			
Started:			

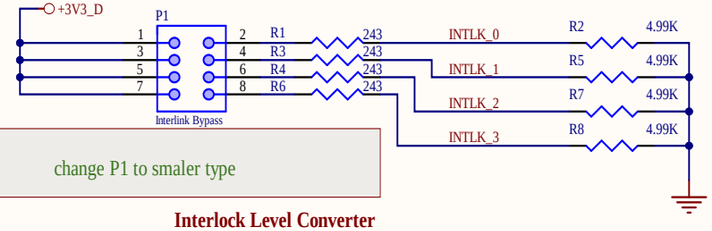
ICM

Power supply connections shown on LVS1

ICM signals INTLK_X are normally low = "safe";
High assertion permits the following:

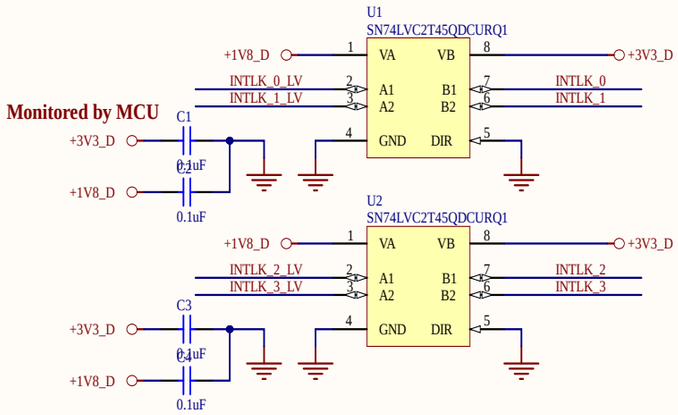
INTLK_0 = Writing to flash memory
INTLK_1 = FPGA Configuration
INTLK_2 = Light In Detector (LID)
INTLK_3 = High Voltage Enable

Changed from 1K to 4.99K



change P1 to smaler type

Interlock Level Converter



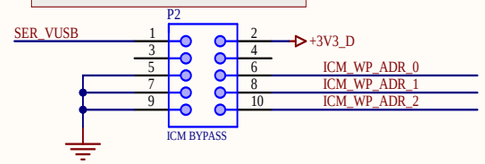
Monitored by MCU

Penetrator changed from ICM.sch to LVS1.sch

ICM - USB Connection

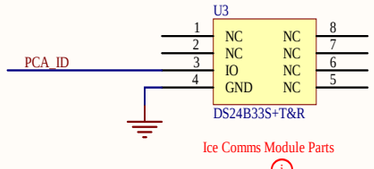
P6= SER Cable Type, PWR from USB, DOM Address

change P2 to smaler type

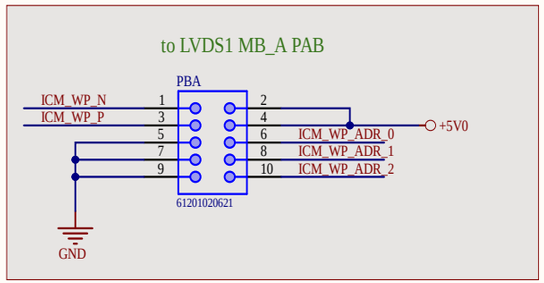


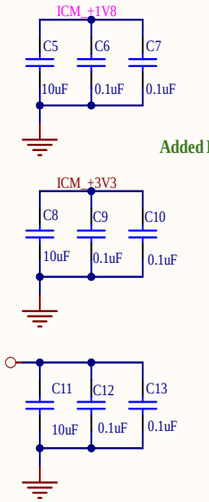
P6 pins 1-2 = FTDI cable type: TTL-232RG-VIP-WE
No Jumper for FTDI cable type: TTL-232R-3V3
P6 pins 3-4 = Power from USB
P6 pins 5-6,7-8,9-10 = WP_ADR_0..2

Mini-Mainboard ID & DATA

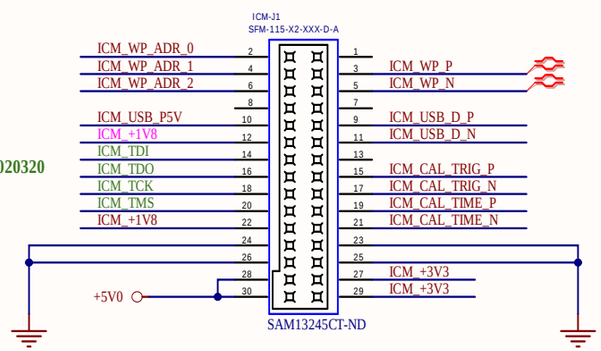


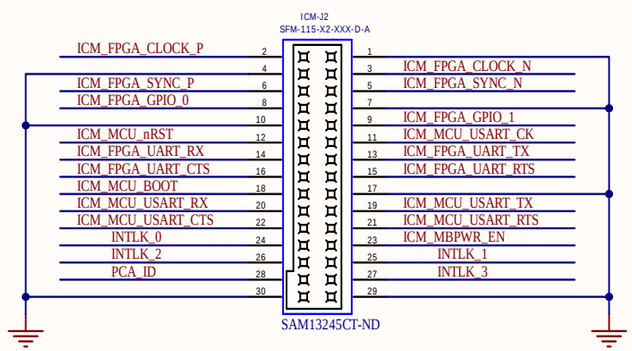
Ice Comms Module Parts

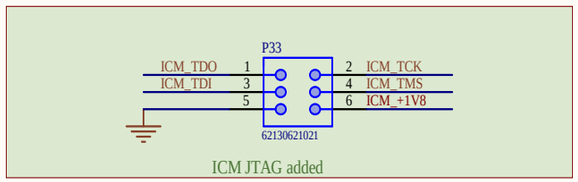




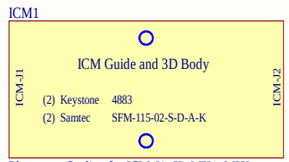
Added Feldh 020320



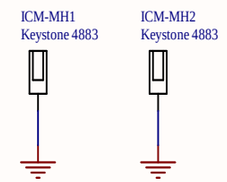




ICM JTAG added



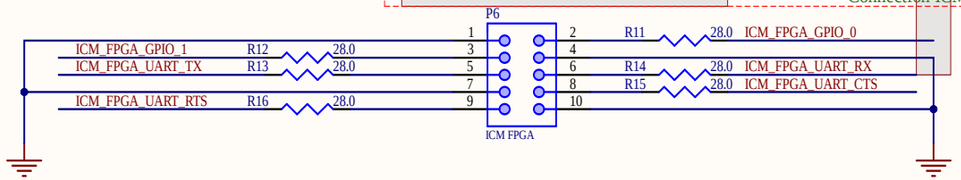
Placement Outline for ICM-J1, J2, MH1, MH2



Ice Comms Module DSN

change P6 to smaler type

Connection ICM_FPGA_GPIO_0 to GND cut



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Modified: 13.05.2020 Time: 15:40:26		Sheet 2 of 7	222 W. Washington Ave.
File: Y:\My Hardware\Altium\IceCube\Mini-Mainboard\MMB_Controller (2-27-2020 2-48-15 PM)\Design Projects\Mini MB\ICM.SchDoc			
Started:			

Microcontroller (MCU)

See STM32 Data Sheet (Tables 10-15) for Alternative Pin functions

Nets used in MMB
Nets to be re-assigned /eliminated
Nets used for Ethernet

U5A

e.g. TIM2, TIM5	ICM_MCU_SYNC_LV	34	PA0	PB0	46	
	ETH_REF_CLK	35	PA1	PB1	47	
	ETH_MDIO	36	PA2	PB2	48	MCU_SPI3_MOSI
e.g. TIM2, TIM5	ICM_MCU_TRIG_LV	37	PA3	PB3	133	MCU_TRACESWO
e.g. DAC1	MCU_GPIO_PA4	40	PA4	PB4	134	MCU_GPIO_PB4
	FMEM_SCLK	41	PA5	PB5	135	FMEM_MOSI
		42	PA6	PB6	136	SLO_I2C1_SCL
	ETH_CRS_DV	43	PA7	PB7	137	SLO_I2C1_SDA
	ICM_MCU_USART_CK	100	PA8	PB8	139	MCU_GPIO_PB8
	MCU_GPIO_PA9	101	PA9	PB9	140	MCU_GPIO_PB9
		102	PA10	PB10	69	MCU_GPIO_PB10
	ICM_MCU_USART_CTS	103	PA11	PB11	70	ETH_TX_EN
	ICM_MCU_USART_RTS	104	PA12	PB12	73	ETH_TXD0
	MCU_SWDIO	105	PA13	PB13	74	ETH_TXD1
	MCU_SWCLK	109	PA14	PB14	75	ICM_MCU_USART_TX
	MCU_TDI	110	PA15	PB15	76	ICM_MCU_USART_RX
		26	PC0	PC8	98	
	ETH_MDC	27	PC1	PC9	99	
	MCU_GPIO_PC2	28	PC2	PC10	111	MCU_SPI3_SCLK
	MCU_GPIO_PC3	29	PC3	PC11	112	
	ETH_RXD0	44	PC4	PC12	113	
	ETH_RXD1	45	PC5	PC13	7	
		96	PC6	PC14-OSC32_IN	8	
e.g. HRTIM, TIM3,8	ICM_MCU_TIME_LV	97	PC7	PC15-OSC32_OUT	9	

STM32H743ZIT6

0.0 DNL ID0
0.0 ID1
0.0 ID2
0.0 ID3

U5B

		114	PD0	PF0/PH0	10	MCU_GPIO_PF0
		115	PD1	PF1/PH1	11	MCU_GPIO_PF1
		116	PD2	PF2	12	MCU_GPIO_PF2
		117	PD3	PF3	13	MCU_GPIO_PF3
		118	PD4	PF4	14	MCU_GPIO_PF4
		119	PD5	PF5	15	MCU_GPIO_PF5
		122	PD6	PF6	18	MCU_GPIO_PF6
		123	PD7	PF7	19	MCU_GPIO_PF7
		77	PD8	PF8	20	MCU_GPIO_PF8
		78	PD9	PF9	21	MCU_GPIO_PF9
		79	PD10	PF10	22	MCU_GPIO_PF10
		80	PD11	PF11	49	MCU_GPIO_PF11
	SLO_I2C4_SCL	81	PD12	PF12	50	MCU_GPIO_PF12
	SLO_I2C4_SDA	82	PD13	PF13	53	MCU_GPIO_PF13
		85	PD14	PF14	54	MCU_GPIO_PF14
		86	PD15	PF15	55	
MCU_SER = UART8						
	MCU_SER_TXD	141	PE0	PG0	56	
	MCU_SER_RXD	142	PE1	PG1	57	
	MCU_GPIO_PE2	1	PE2	PG2	87	
		2	PE3	PG3	88	
	MCU_GPIO_PE4	3	PE4	PG4	89	R27 100K INTLK_0_LV
	MCU_GPIO_PE5	4	PE5	PG5	90	R28 100K INTLK_1_LV
CAL = SPI4	MCU_GPIO_PE6	5	PE6	PG6	91	R29 100K INTLK_2_LV
	MCU_GPIO_PE7	58	PE7	PG7	92	R30 100K INTLK_3_LV
	MCU_GPIO_PE8	59	PE8	PG8	93	FMEM_CSn
	MCU_GPIO_PE9	60	PE9	PG9	124	
	MCU_GPIO_PE10	63	PE10	PG10	125	
		64	PE11	PG11	126	
		65	PE12	PG12	127	FMEM_MISO
		66	PE13	PG13	128	
		67	PE14	PG14	129	
		68	PE15	PG15	132	

STM32H743ZIT6

SPI Flash

+1V8_D
R21 3.00K
INTLK_0 =1= "OK to write"

U4A

FMEM_SCLK	16	SCK	CS# 7
FMEM_MOSI	15	SI/IO0	WP#/IO2 9
FMEM_MISO	8	SO/IO1	IO3/RESET# 1
C40 0.1uF	2	VCC	VSS 10

S25FS512SAGMFV010

FMEM_CSn INTLK_0_LV
R22 3.00K
R23 3.00K
R24 3.00K

New FMEM (1.8V core and I/O)

U4B

3	RFU	DNU	11
4	NC	DNU	12
5	NC	DNU	13
6	RFU	RFU	14

S25FS512SAGMFV010

Bootloader configuration section 40 of AN2606

SPI4 = CAL
SPI3 = PS Config
SPI6 = FMEM
SPI2, UART4, I2C4 = AUX

Requires ICM for clock and sync

ICM_FPGA_CLOCK_P
ICM_FPGA_CLOCK_N
+3V3_D
C43 0.1uF C44 10nF

U6 DS90LV012ATMF

3	IN+	TTLOUT	5
4	IN-		
1	VDD	GND	2

R25 28.0
TP1
ICM_MCU_CLOCK

Place near MCU

ICM_FPGA_SYNC_P
ICM_FPGA_SYNC_N
+3V3_D
C47 0.1uF C48 10nF

U9 DS90LV012ATMF

3	IN+	TTLOUT	5
4	IN-		
1	VDD	GND	2

R26 28.0
TP2
ICM_MCU_SYNC

U7 SN74LVC2T45QDCURQ1

+1V8_D	1	VA	VB 8
ICM_MCU_CLOCK_LV	2	A1	B1 7 ICM_MCU_CLOCK
ICM_MCU_SYNC_LV	3	A2	B2 6 ICM_MCU_SYNC
	4	GND	DIR 5

+3V3_D
+1V8_D +3V3_D
C45 0.1uF C46 0.1uF

Probably can remove level shifter

Serial Interface MCU

P9
MCU_SER_RXD
MCU_SER_TXD
+1V8_D
C41 0.1uF C42 10uF
MCU_SER =UART8

For FTDI Smart Cable:
TTL-232RG-VIP-WE

U8 NUP4301MR6T1G

1	A	D	6 MCU_SER_TXD
3	B	C	4 MCU_SER_RXD
2	G	V+	5 +3V3_D

U5C

ICM_MCU_CLOCK_LV	23	PH0/PF0-OSC_IN	NRST 25 ICM_MCU_nRST
	24	PH1/PF1-OSC_OUT	BOOT0 138 ICM_MCU_BOOT
	33	VDDA	VSSA/VREF- 31
	32	VREF+	
+1V8_D	6	VBAT	VCAP2/PH2/VDDUSB 106
			VCAP1/VSS_1 71
	72	VDD_1	
	108	VDD_2	PDR_ON/VSS_3/NC 143
	144	VDD_3/VDD_SA	
			VSS_4/BYPASS_REG 38
	39	VDD_4	
	17	VDD_5	VSS_2 107
	52	VDD_6	VSS_5 16
	62	VDD_7	VSS_6 51
	84	VDD_8	VSS_7 61
	95	VDD_9/VDDIO_1/VDD_USB33	
			VSS_8 83
	121	VDD_10	VSS_9/VSSIO_1 94
	131	VDD_11/VDDIO_2	VSS_10 120
	30	VDD_12/VSSA	VSS_11/VSSIO_2 130

STM32H743ZIT6

R31 10.0K
C49 0.1uF
C52 2.2uF C53 2.2uF

+3V3_A
0.1uF C50 C51 10uF
+1V8_D
C54 10uF

C55 C56 C57 C58 C59 C60 C61 0.1uF
C62 C63 C64 C65 C66 C67 0.1uF

+1V8_D
P10

MCU_SWCLK	R34	39.2	2
MCU_SWDIO	R35	39.2	4
ICM_MCU_nRST	R36	39.2	5
MCU_TRACESWO	R33	39.2	6

61000618221

Change P10 to smaler type ?

JTAG MCU Changed

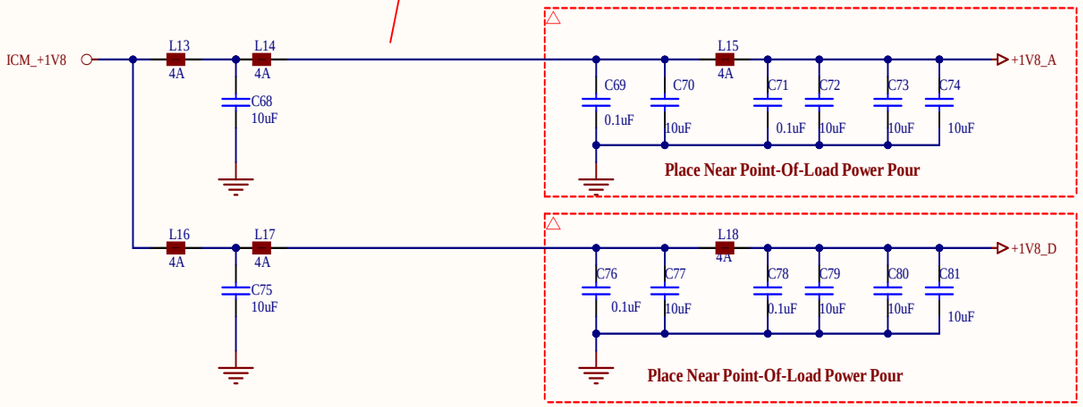
Pinout According to ST UM1075- Page 12

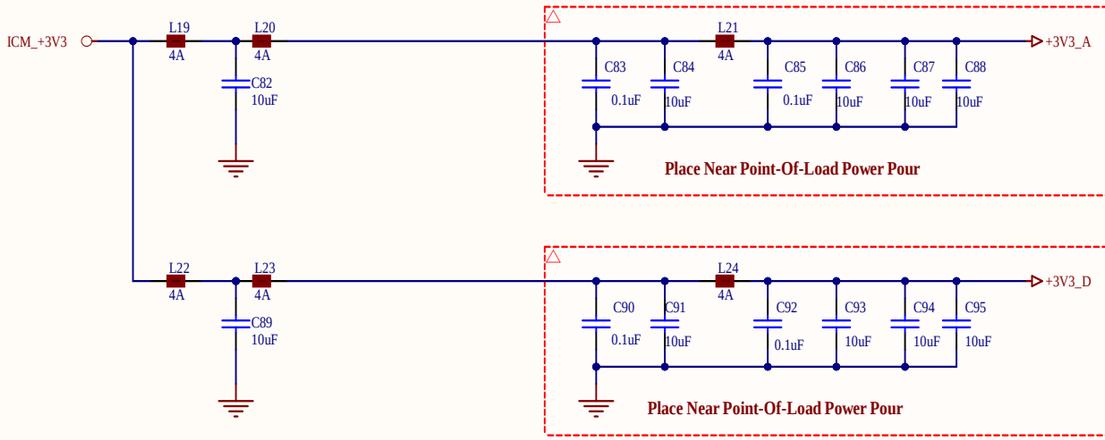
MCU.SchDoc			
Size: B	Designed: PWS Drafted: PWS Checked: Approve:	Revision:	
Modified: 13.05.2020 Time: 15:40:26		Sheet 4 of 7	
File: Y:\My Hardware\Altium\IceCube\Mini-Mainboard\MMB_Controller (2-27-2020 2-48-15 PM)\Design Projects\Mini MB\MCU.SchDoc			
Started:			

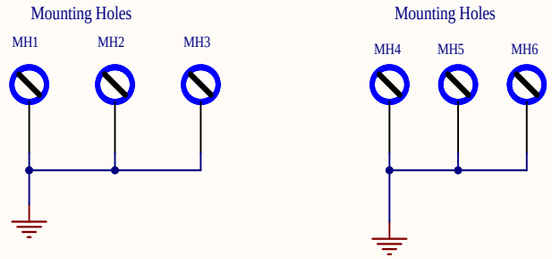
WIPAC
Wisconsin IceCube Particle Astrophysics Center

Mounting Holes and Filters (EMC)

Note: Traces between PSU and power pours can be 50mil-100mil







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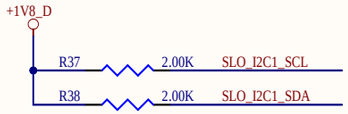
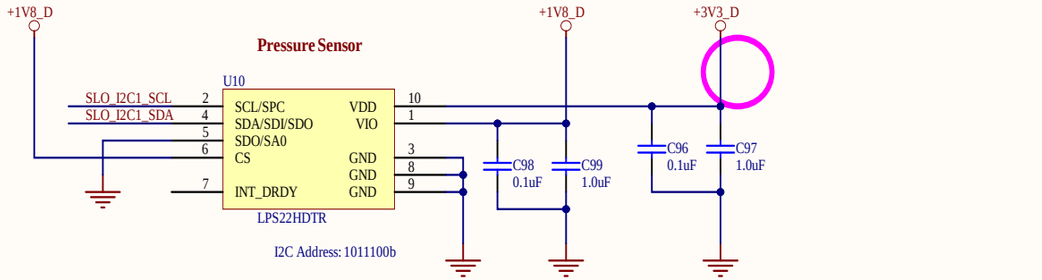
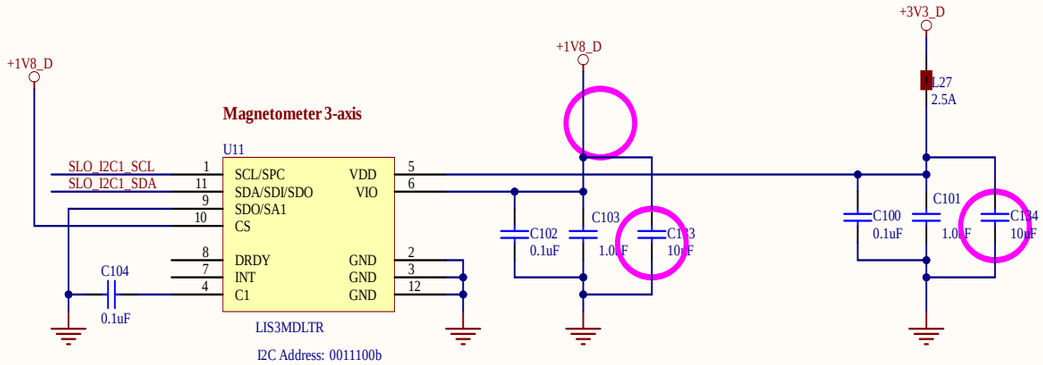
Slow Control and Monitor (SLO)

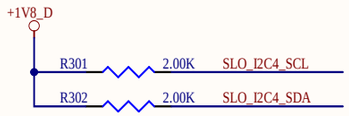


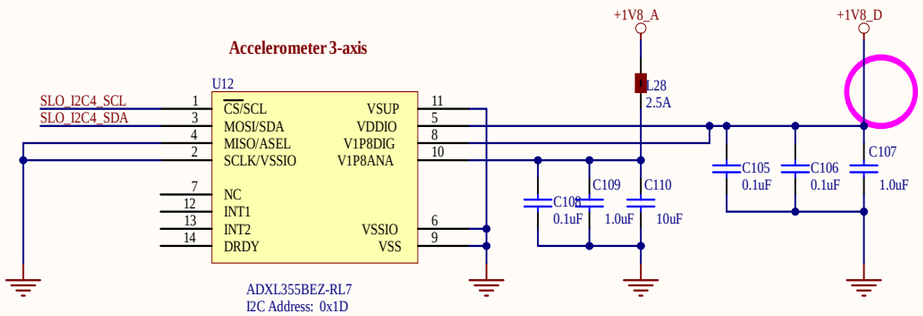


Replaced LPS22HB with LPS22HD



Place away from high-current traces





SLO.SchDoc			
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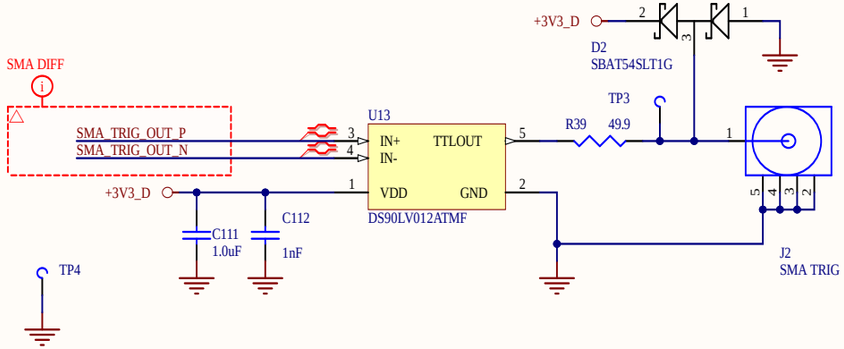
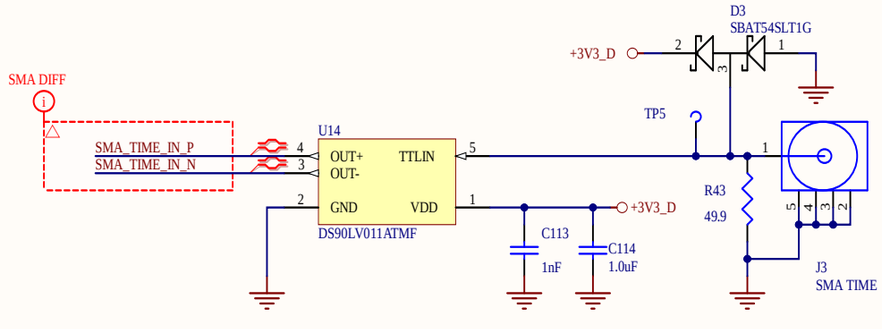
File: Y:\My Hardware\Altium\IceCube\Mini-Mainboard\MMB_Controller (2-27-2020 2-48-15 PM)\Design Projects\Mini MB\SLO.SchDoc			
Started:			

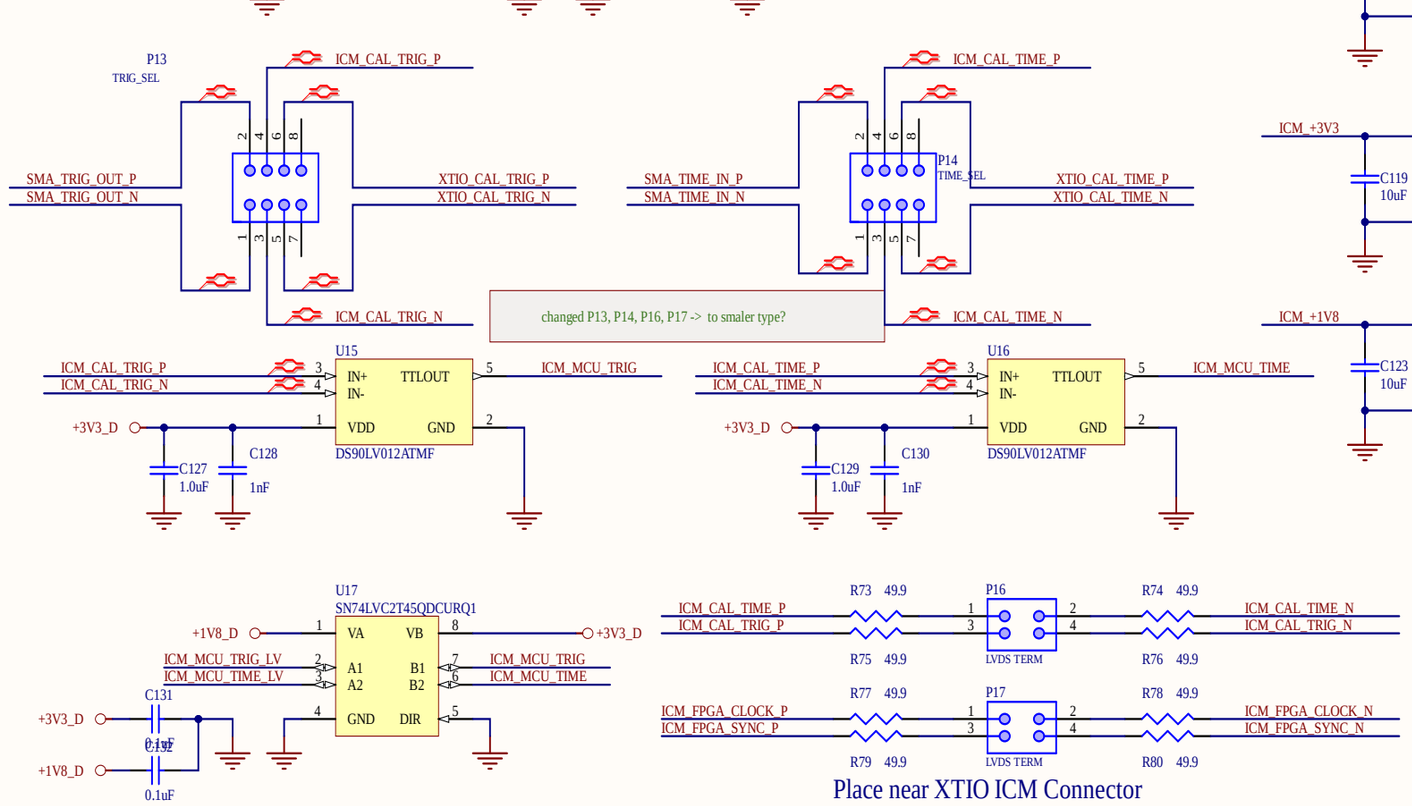
External Host System Interface (XTIO)

SMA TRIG Output



SMA TIME Input





Place near XTIO ICM Connector

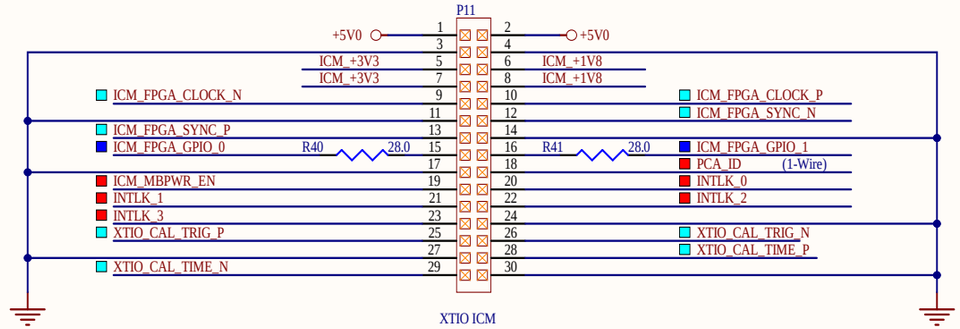
Host Interface Connections

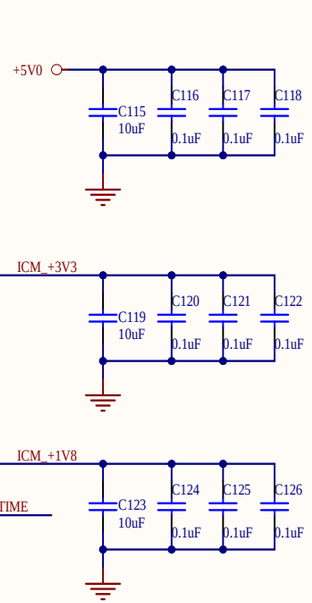
- 3.3V
- 3.3V LVDS
- 1.8V
- 1.8V Diff SSTL 1

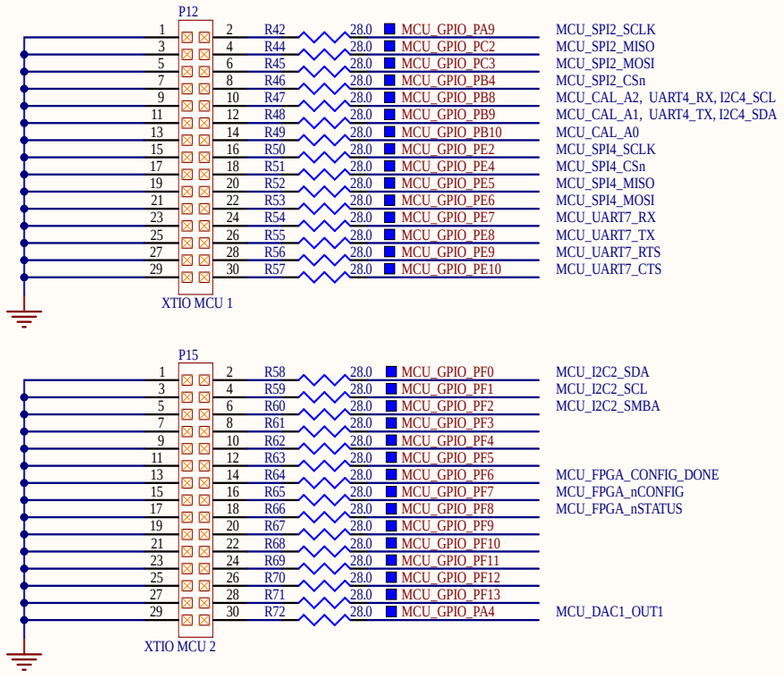
Supplier Link for Connectors

ICM signals INTLK_X are normally low = "safe";
High assertion permits the following:

INTLK_0 = Writing to MCU flash memory
INTLK_1 = FPGA (or MB logic) Configuration
INTLK_2 = Light In Detector (LID)
INTLK_3 = High Voltage Enable







See STM32 Data Sheet (Tables 10-15) for Alternative Pin functions

XTIO.SchDoc			
Size: B	Designed: PWS Drafted: PWS Checked: Approve:	Revision:	IceCube Upgrade Amundsen-Scott South Pole Station, Antarctica
Modified: 13.05.2020 Time: 15:40:27		Sheet 7 of 7	
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