CoreLink NIC-400: a great interconnect for wearables and entry-level smartphones

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As the number of processors and I/O masters in an SoC continues to rise the need for an efficient and easy to design interconnect becomes critical. An interconnect must provide sufficient throughput and low enough latency for all masters in the system. But must also keep costs and power to a minimum. Costs include design time, silicon area and licensing and royalty fees.

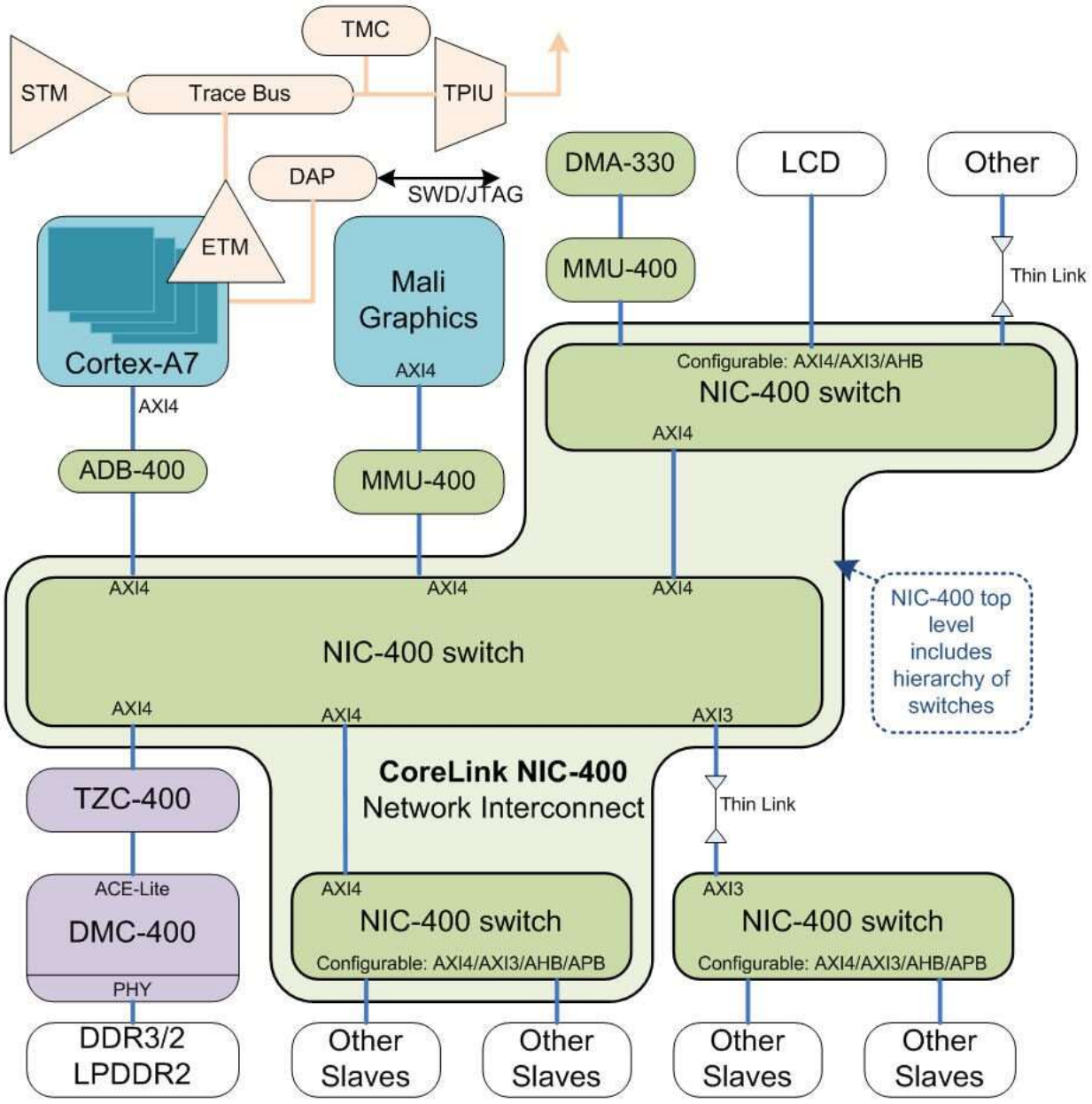

Fig. 1 An example SoC design using CoreLink NIC-400 Network Interconnect

ARM has developed its 4th generation configurable interconnect for connecting up AMBA AXI, AHB and APB devices, the CoreLink NIC-400 Network Interconnect, that addresses these needs. The NIC-400 comes with a powerful and easy to use GUI-driven configuration tool, AMBA Designer, that allows the designer to generate a complex hierarchical network of interconnects within hours. From the user entry of the master and slave interfaces, such as AXI3/4, AHB or APB, the required connectivity matrix and the position of slaves in the address map, the tool generates and connects up all the required interface blocks, switches, upsizers, downsizers and clock and protocol domain bridges.

All unused paths are removed and bus widths selectable to minimise wiring. The network of switches topology employed by NIC-400 allows reduced routing as masters and slaves can be grouped locally and longer cross-SoC data paths are shared to minimise area. From the first pass system generated there are many powerful configurable options to reduce silicon area, ease timing closure, and size buffers to optimize performance without unnecessary overheads.

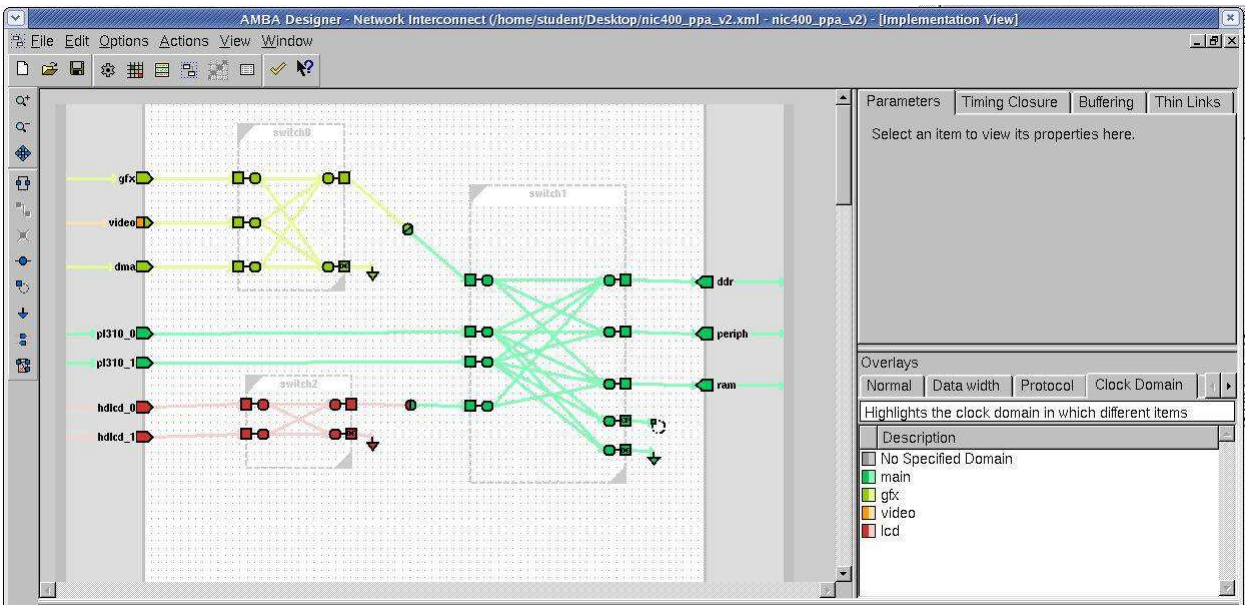

Fig. 2 AMBA Designer: a powerful and easy to use GUI configuration tool

The CoreLink NIC-400 comes with options for data traffic management QoS-400 Advanced Quality of Service and QVN-400 QoS Virtual Networks to ensure all masters are serviced within acceptable bandwidth and latency constraints to maintain the required performance. Dividing traffic up in to virtual networks than run over shared physical networks reducing routing congestion while maintaining QoS contracts, such as min/max latency or required bandwidth, and thus processor performance.

To further reduce routing congestion on long links between different power or clock domains, the TLX-400 Thin Links option is available to pack the AXI bus on to dramatically reduced widths, configurable from 2/3rd to 1/20th number of wires.

The CoreLink NIC-400 has gone through extensive validation to ensure any configuration is known to be good and the NIC-400 is a mature product that has already been silicon proven in dozens of customer designs.

There is a full ecosystem of EDA tools to support the NIC-400. Cycle accurate models from The specified item was not found., derived from the customer configured NIC-400 RTL. For dynamic performance analysis of the NIC-400, the Cadence Interconnect Workbench offers in depth debug and analysis of the RTL with masters and slaves replaced by VIP testbench. SystemC modelling solutions are available from Synopsys SBL-400 for Platform Architect MCO. Check out the upcoming webinar on **Case Study: Performance Analysis and Optimization of ARM® CoreLink™ NIC-400 based Systems Using Synopsys Platform Architect, May 20, 2014 10am PDT. Register here.**

On pricing, the options allow the buyer to select the best value package for their design and CoreLink NIC-400 is royalty free.