ARM introduces two new CoreLink CCN interconnects

by **Tarinder Sandhu** on 22 October 2014, 17:00

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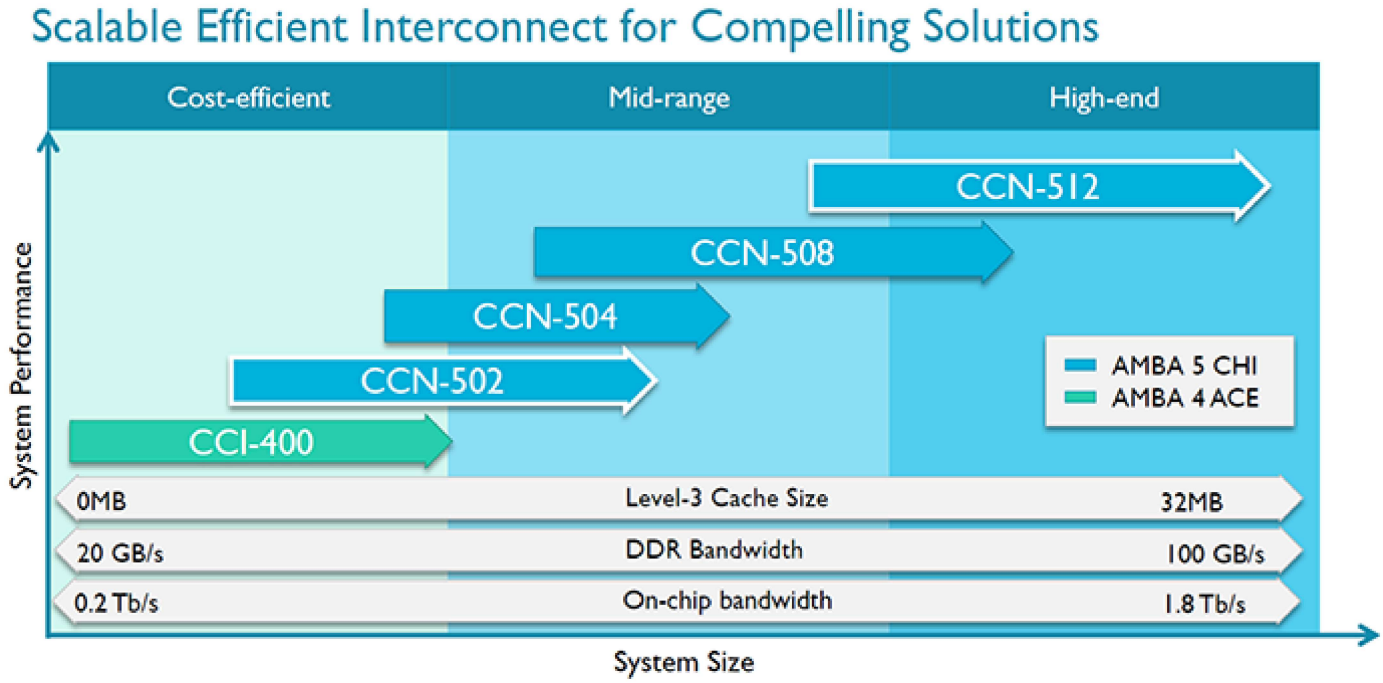
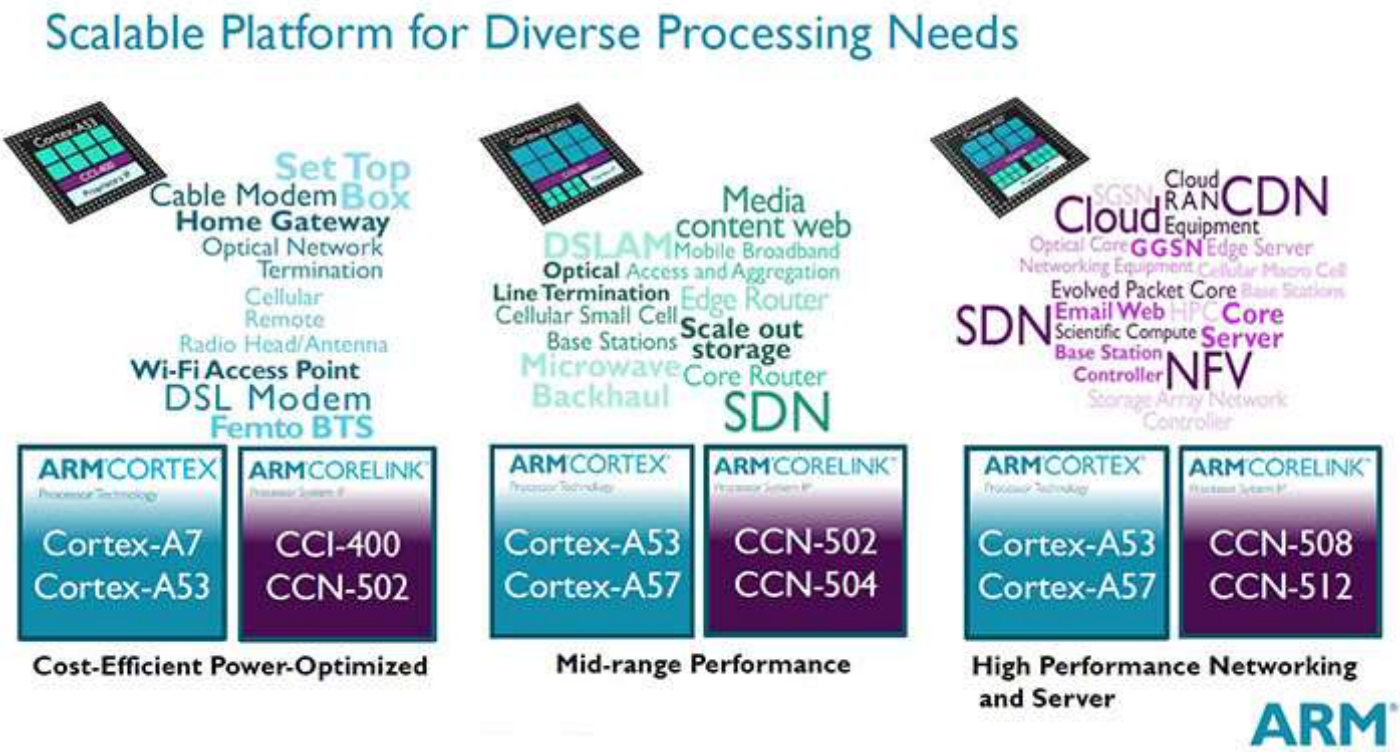


CCN positioning. Image credit to ARM

Modern mainstream and premium ARM system-on-chip (SoCs) products use the CoreLink Cache Coherent Network (CCN) 504 or, more recently, 508 interconnects. These provide access to L3 cache, a number of interfaces for I/O coherent accelerators and access to either DDR3 or DDR4 memory, tying the CPU(s) up to the rest of the chip.

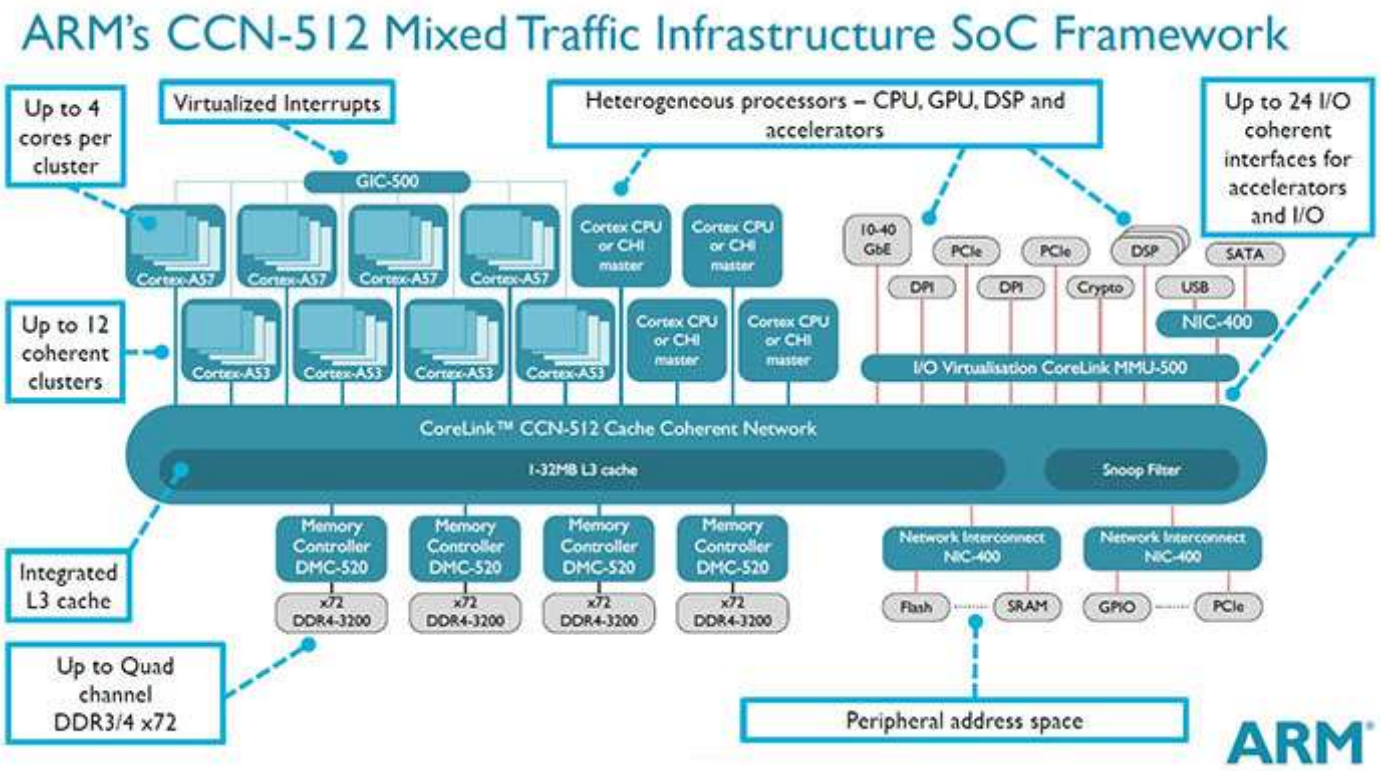
The glue of the SoC, the CCN-504 supports up to four processor clusters (16 cores), 16MB of L3 cache and 18 I/O interfaces. The datacentre-centric CCN-508, meanwhile, increases this to a potential eight clusters and 32 cores, 32MB of L3 cache and 24 I/O interfaces.



Uses of modern ARM interconnects. Image credit to ARM

Now offering partners more choice with respect to SoC interconnects, ARM is today unveiling two new CCN models. The CCN-502 is a lower-cost, smaller interconnect primed for use in products such as WiFi access points, edge routers and base stations. CCN-512, meanwhile, expands the datacentre and HPC reach by offering connectivity for more CPU cores.

CCN-512 - the meaty one



A high-level overview of CCN-512. Image credit to ARM

The topology of the CCN-512 interconnect adheres to the blueprint adopted by the **CCN-508**. Designed to support processor-dense SoCs in a datacentre-type environment, ARM is now providing a means of expanding the CCN-508's eight coherent CPU clusters to 12 on this model, or from a maximum 32 cores to 48. Of course, partners need to design such SoCs - ARM provides the IP necessary for the building blocks.

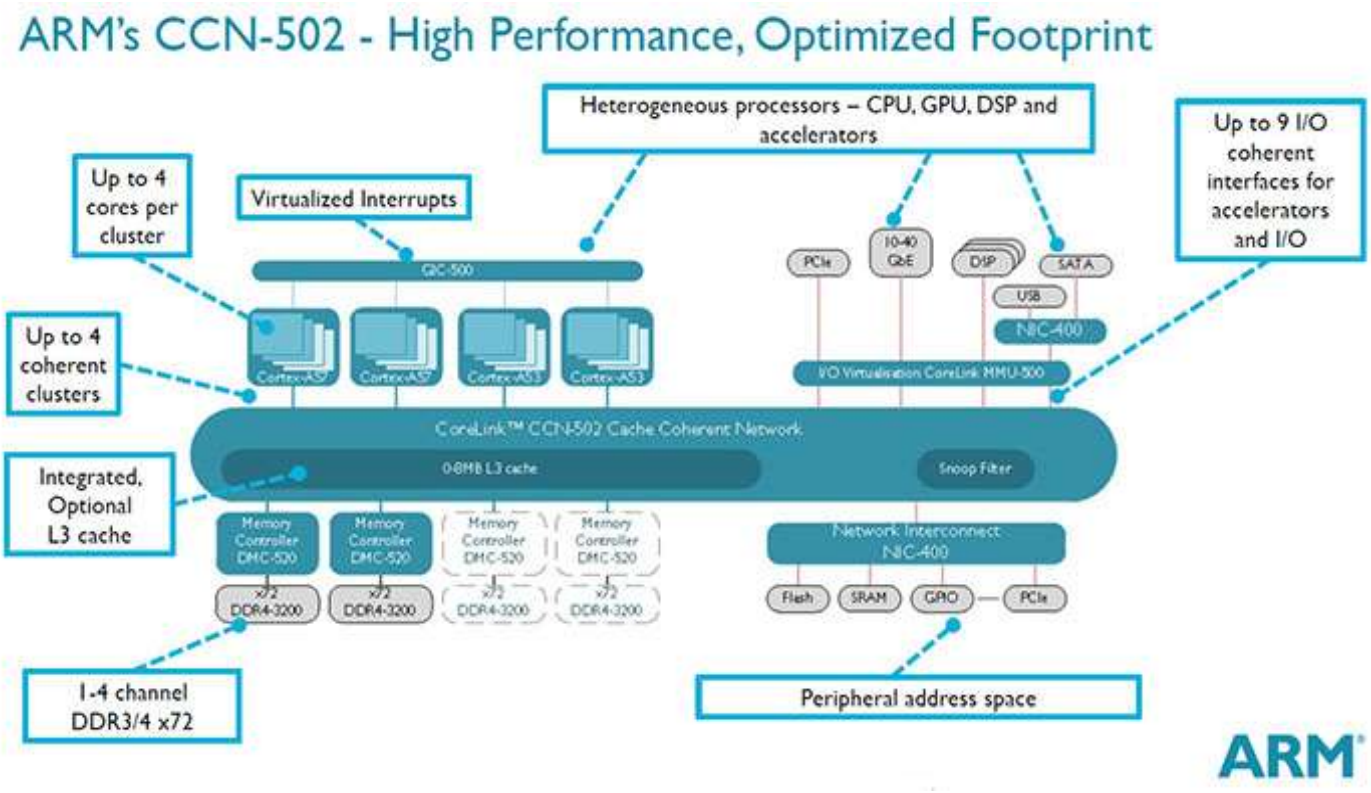
Typically designers of such targeted and performance-rich SoCs tend to build their own interconnect fabric - Cavium, for example, has a 48-core-supporting **technology** implemented on the ThunderX products. ARM, with the CCN-512, is enabling partners who wish to compete in this space quicker entry to market because they don't need to design and validate their own.

ARM is aware that not all partners need provision for 48 Cortex A-series cores in a densely-packed SoC. This is why the four additional clusters can be either Cortex A-series processors or coherent hub interfaces (CHI) conencted to dedicated digital signal processors, general-purpose processors or graphics. Note that processors for these 12 clusters can be from either the Cortex-A57 or Cortex-A53 families, though both sets of cores cannot co-exist in one cluster.

CCN-512 matches CCN-508's 24 I/O coherent interfaces for accelerators and also uses the same quad-channel DMC-520 memory controllers. This time around, though, official supported speed is bumped up to DDR4-3200 per channel. Crunching the numbers reveals CCN-512 has over 100GB/s of bandwidth on tap. With so many processor cores and, potentially, masses of I/O hanging off the interconnect, ARM says peak internal bandwidth speed is 1.8TB/s.

If you consider how ARM-based SoCs are likely to develop in the enterprise space, where dense compute and huge I/O are most important, having a high-bandwidth interconnect is a must. The CCN-512 extends the work laid down by the CCN-508. It is likely that teasing out such an interconnect further means ARM will run into bandwidth-related problems at some point, but the company says it's working on future CCN fabric connect with one another on a single chip.

CCN-502 - the lightweight one



The area-optimised CCN-502. Image credit to ARM

The presently available ARM CoreLink **CCN-504** system IP is used in many-cluster SoCs built for a wide range of uses, but it can be considered both energy and footprint overkill for more basic chips. Answering an obvious need, the CCN-502 is redesigned to offer most of the features but at a significantly lower area and energy cost.

ARM keeps up to 16-core CPU compatibility with CCN-502 but reduces the number of I/O interfaces by half, to nine, and perhaps most importantly for both area and power, has the ability to remove the L3 cache altogether. Putting these potential savings in context, an implementation with 1MB of L3 cache is 70 per cent smaller (and more energy efficient) than a full-complement CCN-508.

ARM is keen to point out that this is not merely a shrunken-down version of the CCN-504. Rather, it's been purposely designed for a different market segment. The introduction of this new interconnect paves the way for

more cutting-edge ARM-based SoCs and provides an avenue for increasing the number of licensees.