ARM CoreLink 400 & 500 Series System IP

PD Product Marketing
December 2012

ARM CoreLink™ and CoreSight™

System IP for the best ARM Cortex™ and Mali™ processor performance

- **Power efficient system**
  - Maximum cache & DDR utilization
  - Shortest path to memory

- **System performance**
  - End-to-end QoS provides b/w & latency per master

- **Optimized system**
  - CoreSight debug and performance profiling

big.LITTLE™ test chip 2

- **System assured**
  - Designed together, verified together

The Architecture for the Digital World®   **ARM**®

CoreLink 400 System IP Available Now
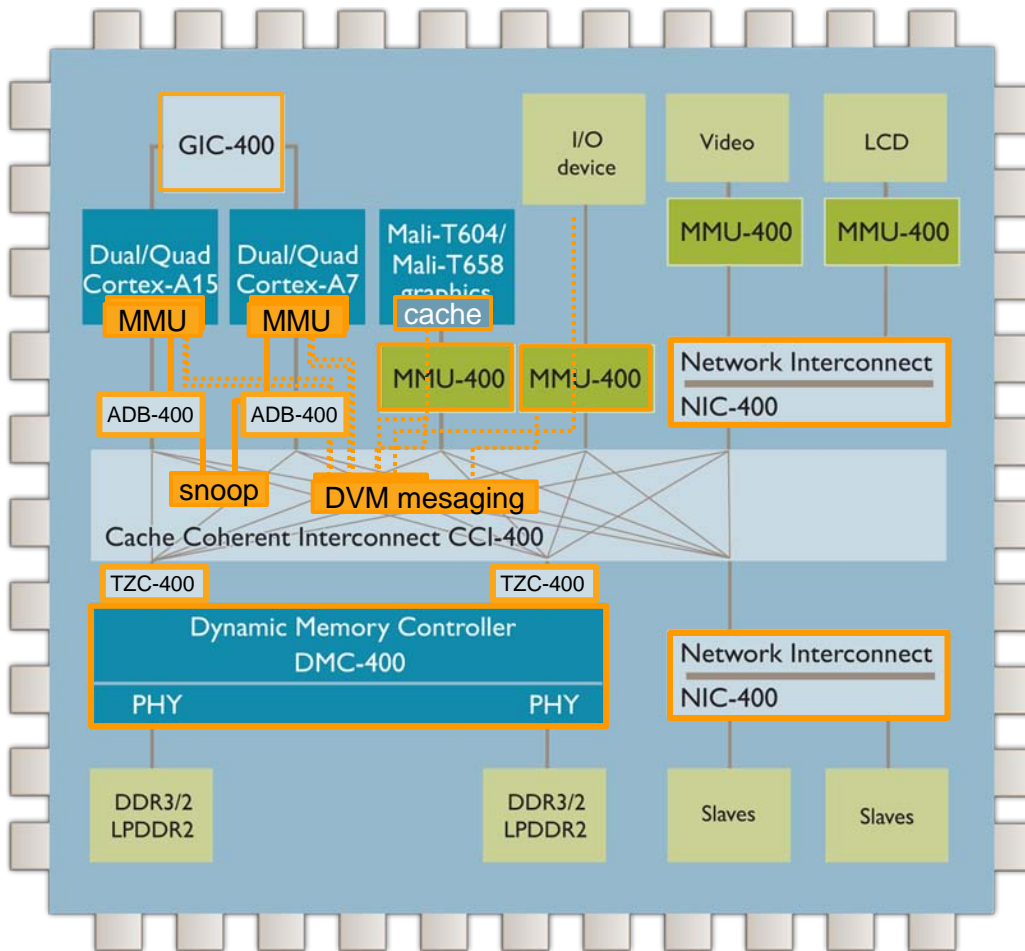
Coherency
- CoreLink CCI-400
  - Full cache coherency
  - I/O coherency
- CoreLink ADB-400
  - For DVFS

Virtualization
- CoreLink MMU-400
  - OS level virtualization
- CoreLink GIC-400
  - Virtual interrupts
  - Multi-processor support

External Memory Sub-system
- CoreLink DMC-400
  - High DDR utilisation
  - Integrated with DDR3 PHY
- CoreLink TZC-400*
  - Secure regions

Rest of SoC Interconnect
- CoreLink NIC-400
  - Low latency
  - Routing efficiency

* TZC-400 available 1Q13

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Wide Adoption of ARM System IP

- 50,000 downloads of AMBA specs in last 3 years

- 80+ licensees of NIC-301, 12+ licensees of NIC-400

- 15+ licensees of CCI-400

- 10+ licensees of DMC-400

- 30 licensees of CoreSight SoC-400

- Adopted across all market segments

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Updates to Existing CoreLink 400 Products

- CoreLink NIC-400 smaller, faster, lower power
    - Hierarchical clock gating reduces idle power by 80%
    - TLX-400 Thin Links to reduce routing

- End-to-end QoS Virtual Networks across:
    - CoreLink NIC-400 + QoS-400 + QVN-400
        - Prevents blocking for higher multi master performance
    - CoreLink CCI-400r1
        - With enhanced throughput up to 25 GB/s @ 533MHz
    - CoreLink DMC-400r1
        - With integrated controller + PHY DDR3 28HPM

- CoreLink TZC-400 secures regions in DRAM

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CoreLink CCI-400 Cache Coherent Interconnect
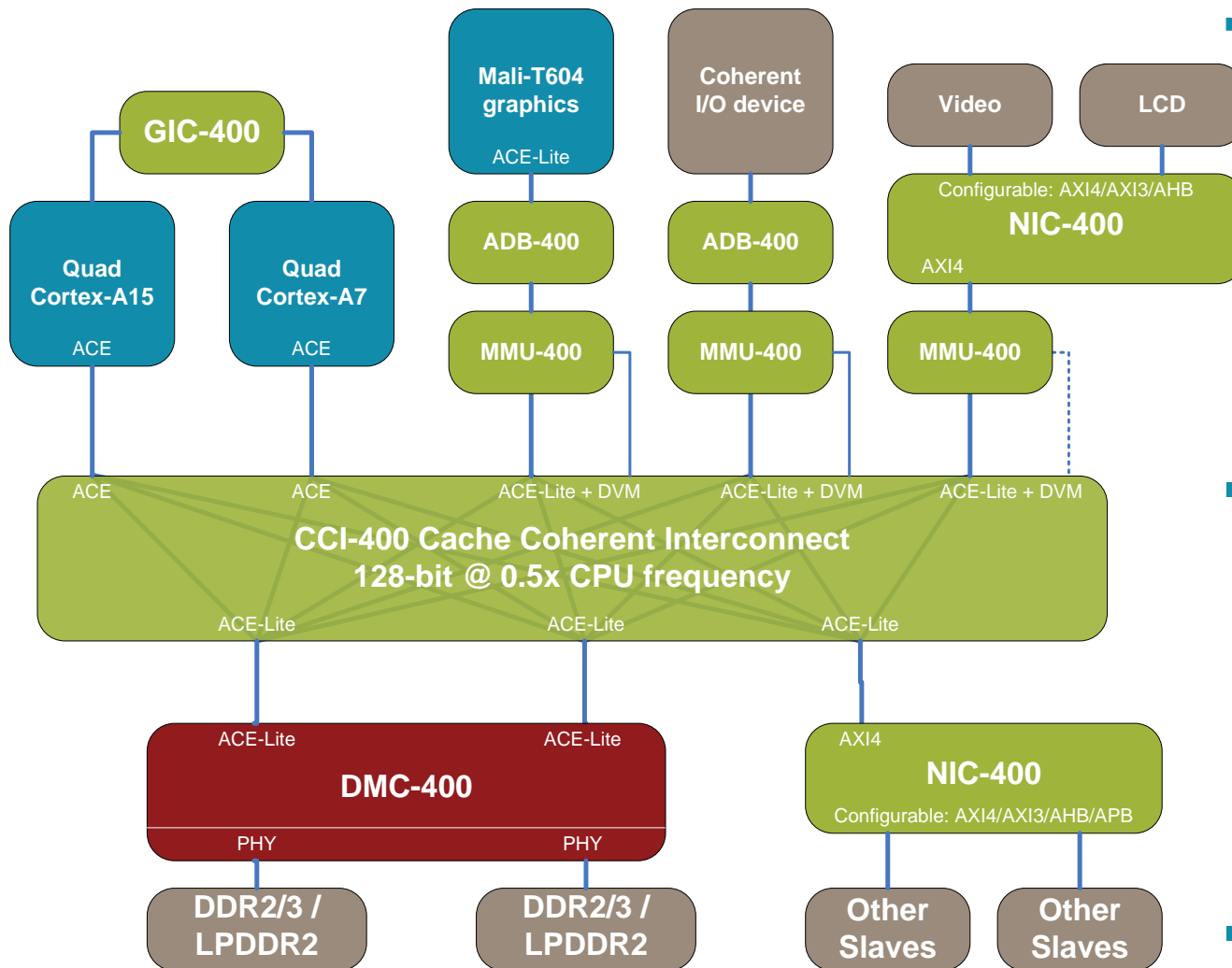
- First ARM interconnect to support AMBA 4 AXI Coherency Extensions (ACE)
  - Extends coherency to the system, multiple processors
  - Supports big.LITTLE™
  - Supports barriers, virtualisation, cache maintenance
- Fixed 5x3 topology, configurable for performance/area from 100k to 500k gates
  - 2x full ACE (CPU)
  - 3x ACE-Lite + DVM I/O coherent slaves
  - 3x master interfaces (2x DRAM + system)
- End-to-end QoS with NIC-400 and DMC-400

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CoreLink NIC-400 Network Interconnect

- New in NIC-400:
  - 20% faster, 20% smaller than NIC-301
  - Addition of AMBA 4 AXI4 interfaces and interconnect switches
    - Long burst support, QoS signalling
  - + everything NIC-301 does, including support for AMBA 3 AXI, AHB, APB
- Hierarchical clock gating
- 90% reduction in idle and near idle power on LP
- Quality of Service Virtual Networks (QVN-400)
  - Separation of critical real-time traffic from high bandwidth low priority traffic
  - Removes head of line and cross stream blocking
  - End-to-end QoS with CCI-400 and DMC-400
- Advanced QoS Regulators (QoS-400)
  - New bandwidth sensitive dynamic regulator
- Thin Links (TLX-400)
  - Packetized links between NIC-400s, masters & slaves, reduces routing, example 65% less wires at 2x freq, same bandwidth
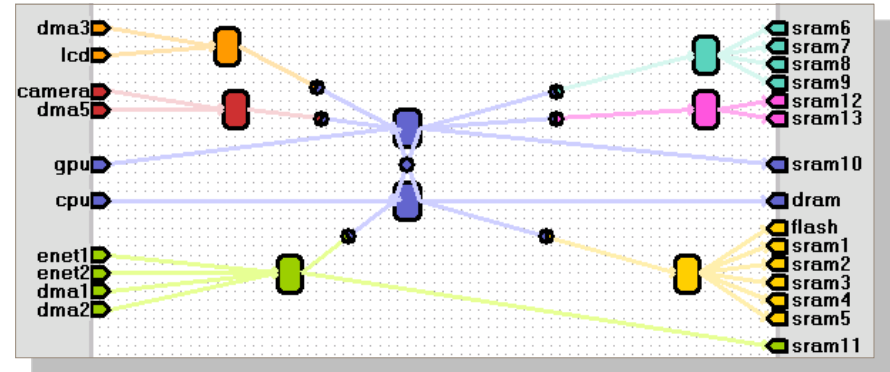
**Configurable Network Interconnect Structure**

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CoreLink DMC-400 Dynamic Memory Controller

- **AMBA 4 Dynamic Memory Controller**
  - Highly efficient interface from ARM systems to off chip LPDDR2 and DDR2 / DDR3
  - Delivers high bandwidth and low latency for high performance multimedia systems
  - Effective management of power in memory sub-system
  - End-to-end QoS with NIC-400 and CCI-400
  - Improves performance for Cortex-A5, Cortex-A9, Cortex-R and Mali processor- based designs

- **Features and functionality**
  - Configurable and programmable
  - Full support for advanced QoS-400 features
  - >90% max theoretical utilization of memory bus traffic
  - 1, 2 or 4 system ports and memory channels
  - Tight integration with ARM DDR3 PHY solutions
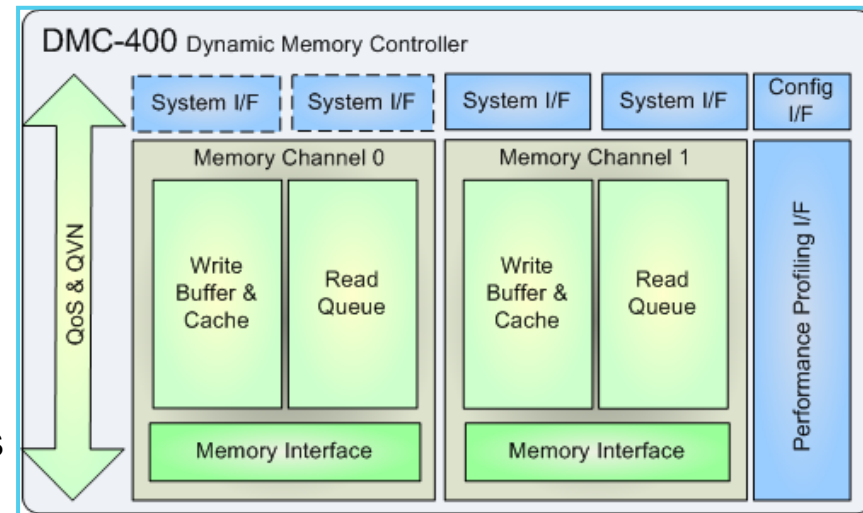
CoreLink MMU-400 and GIC-400
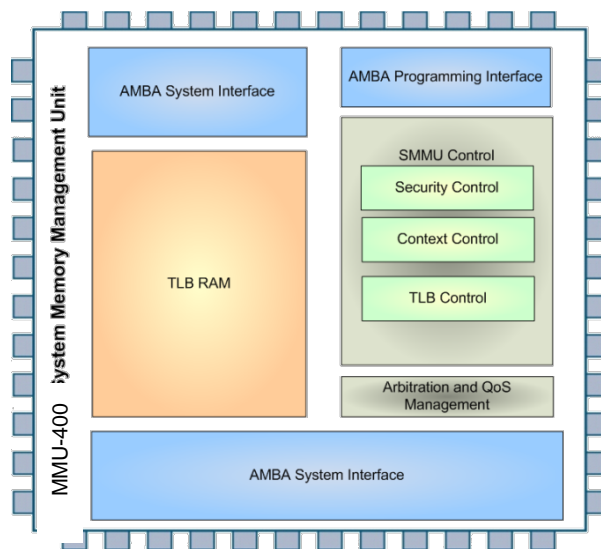
- I/O virtualization with distributed TLB maintenance messaging
- Stage 2 address translation for hypervisor support
- ARMv7 virtualization extension architecture compliant
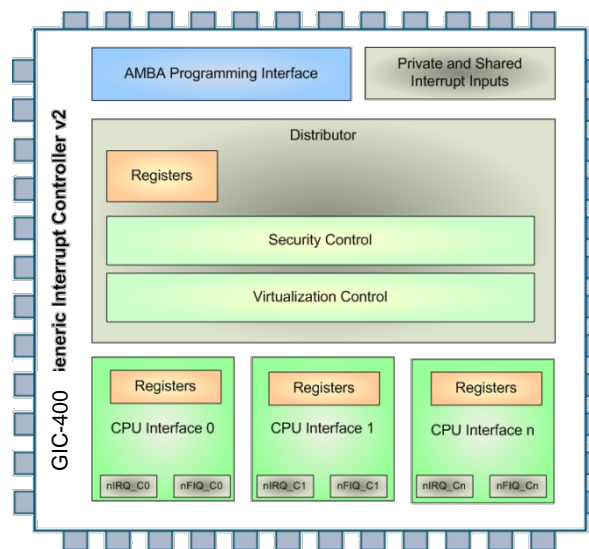
- Generic Interrupt Controller for multiple Cortex-A15, Cortex-A7 clusters
- IRQs and FIQs securely managed by hypervisor for each OS
- ARMv7 virtualization extension architecture compliant

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TZC-400 TrustZone Address Space Controller

- Extends secure memory with low cost external DRAM
- Prevents illegal access to protected memory regions
- Protection from software attacks
- Part of TrustZone® system

- Between CCI/NIC and DMC

- Applications: secure transactions with sensitive data, DRM


Address Map
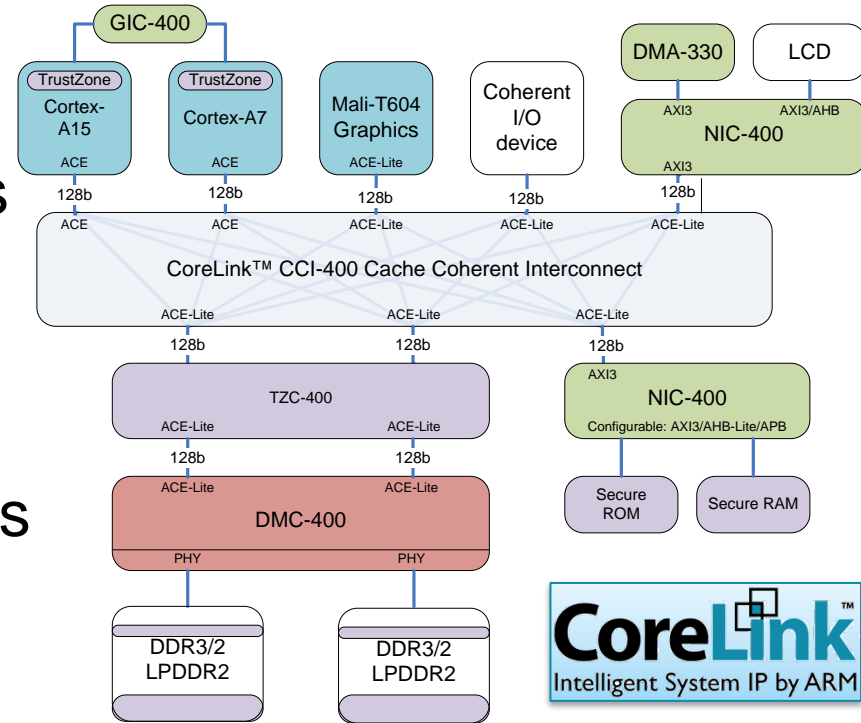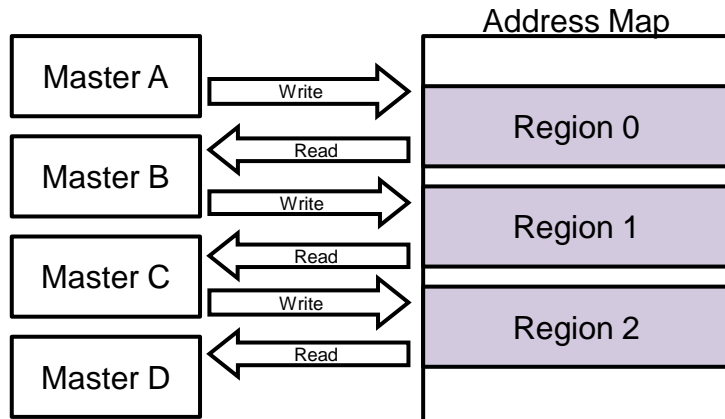
- Supports multiple interfaces (1, 2 or 4)
- Secures 8 memory regions
- Enables a secure data pipe
  - Setup read / write for specific masters
- Fast Path for low latency masters
- 256 outstanding transactions

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CoreSight SoC-400

A debug and trace framework for ARM based SoCs

- Build the most effective on-chip visibility with CoreSight SoC IP
    - Configurable debug & trace infrastructure to address all markets and latest processors
    - SoC level time-stamping infrastructure

- Improve productivity with CoreSight SoC flow
    - Describe, check for compliance your CoreSight systems in minutes.
    - Automated validation of your CoreSight systems

- Unified flow for OEMs and silicon providers
    - Based on IP-XACT 1.4 & AMBA Designer

- A generic solution for all markets & processors
    - Integrate homogeneous & heterogeneous systems
    - Trace Macrocells become add-ons

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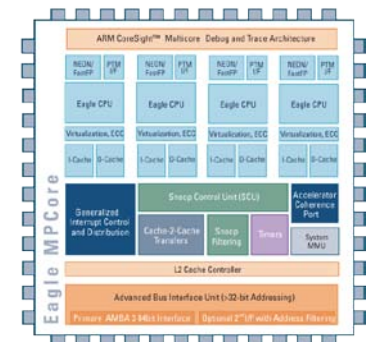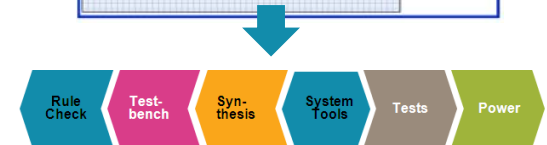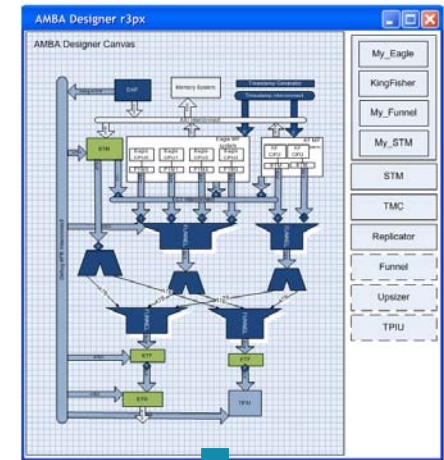
CoreLink 400 Series for AMBA 3

- NIC-400 configurable interconnect
  - High performance **and** rest of SoC interconnect
  - AXI4, AXI3, AHB and APB4
- Thin Links to reduce routing
  - Between switches
- End-to-end Quality of Service with virtual networks and regulation
  - Separates low latency, real-time and high bandwidth masters
  - Prevents head-of-line and cross-stream blocking
- DMC-400 high efficiency, multi-channel memory controller
  - AXI3 and AXI4 supported
  - Unified QoS mechanisms
- MMU-400 assists hypervisor for I/O
  - Stage 2 address translation

The Architecture for the Digital World®

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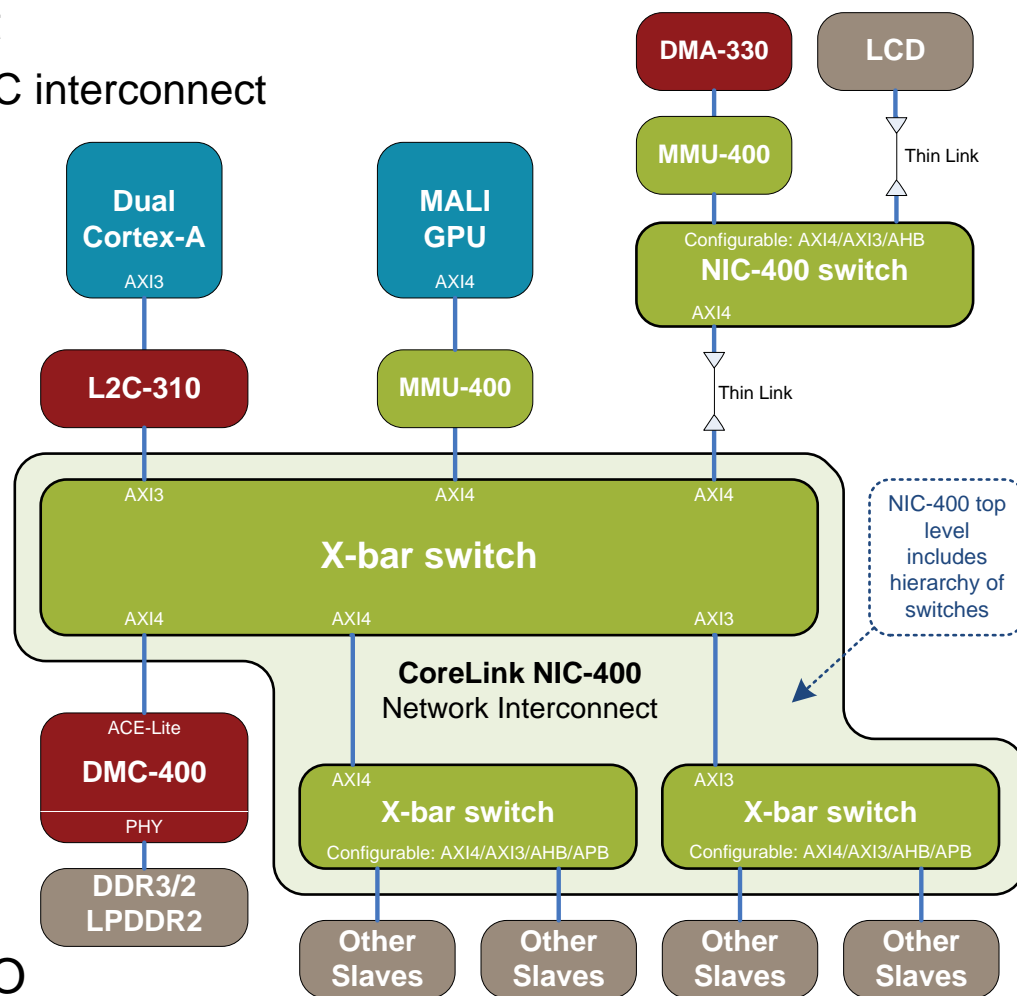
CoreLink 500 System IP for 2013

Support for ARMv8-A Cortex-A57 and Cortex-A53 SoCs

- CoreLink CCN-504 Cache Coherent Network
  - Up to 4 clusters of Cortex-A57, Cortex-A53 and Cortex-A15
  - ~1 terabit/sec useable system bandwidth

- CoreLink DMC-520 Dynamic Memory Controller
  - 72-bit DDR4-3200 and interfaces directly with CCN-504

- CoreLink GIC-500 Generic Interrupt Controller
  - GICv3 Architecture for interrupt scaling with affinity routing
  - Message based interrupts and direct GIC⇔CPU interface

- CoreLink MMU-500 System Memory Management Unit
  - 2 stages of address translation
  - System MMU Architecture v2 with new 64k page tables
  - Up to 48-bit addressing for IO device virtualization

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Example High End Mobile Solution

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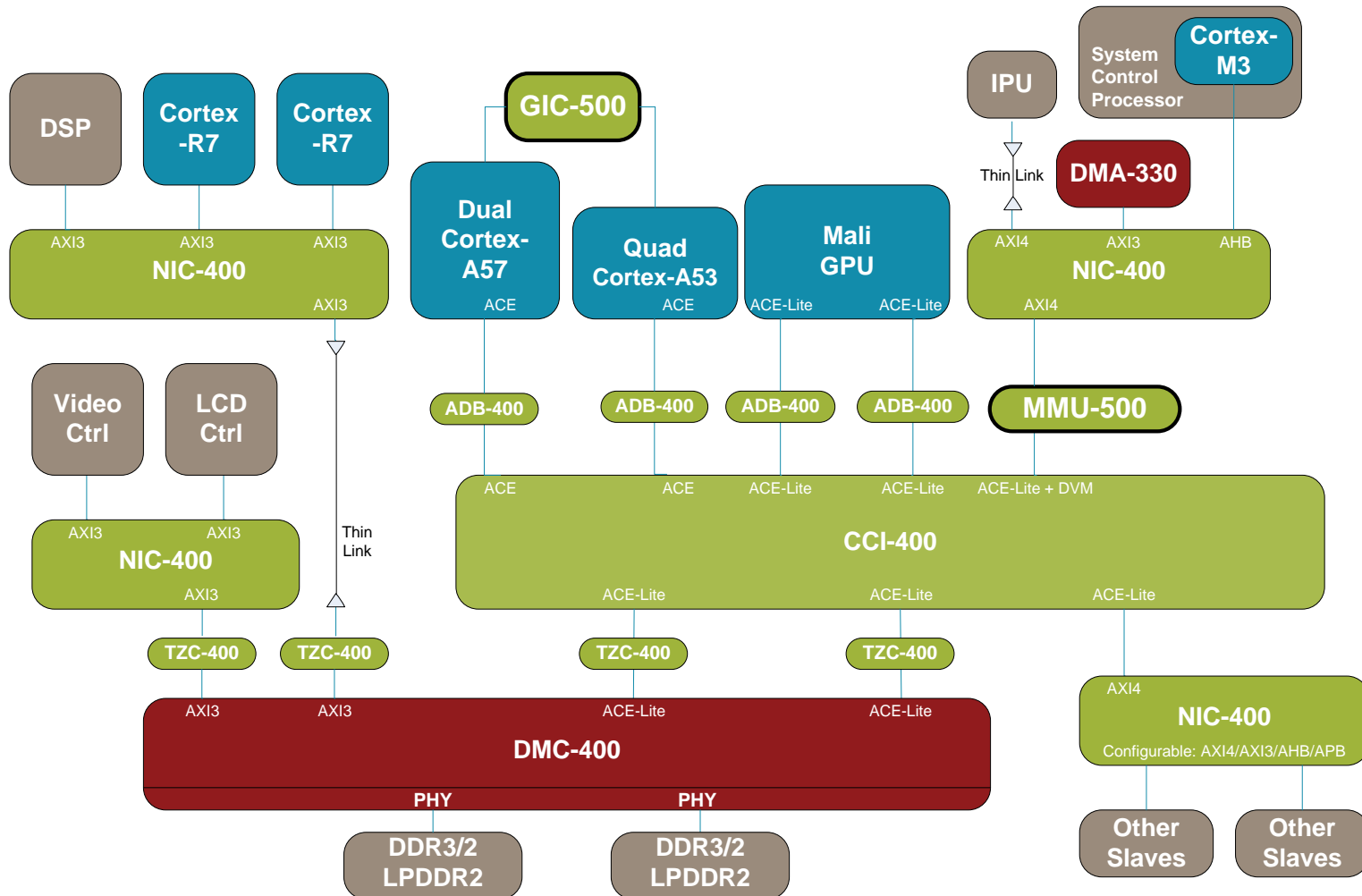
Growing Importance of Virtualization

Virtualization hardware supported in ARMv7-A, ARMv8-A

"Virtualization is execution of software in an environment separated from the underlying hardware resources"

Virtualization use cases

IP obfuscation; IP protection; environment duplication; multiple guest-OS support under hypervisor control

System without virtualization

App 1	App 2

Operating System

Hardware
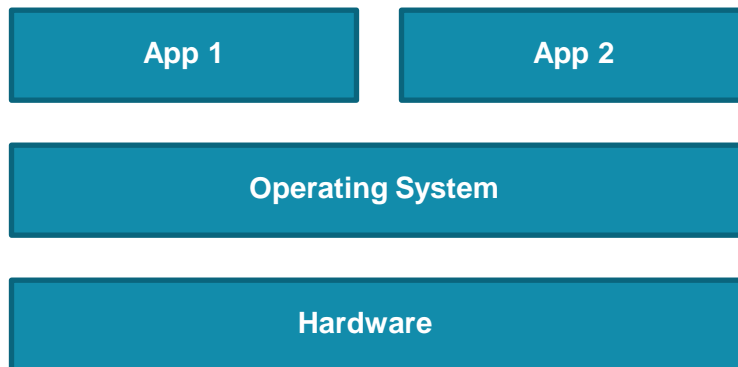
System with virtualization

Virtual Machine 1

App 1	App 2

Guest OS 1

Virtual Machine 2

App 1	App 2

Guest OS 2

Virtual Machine Monitor (VMM, or Hypervisor)

Hardware

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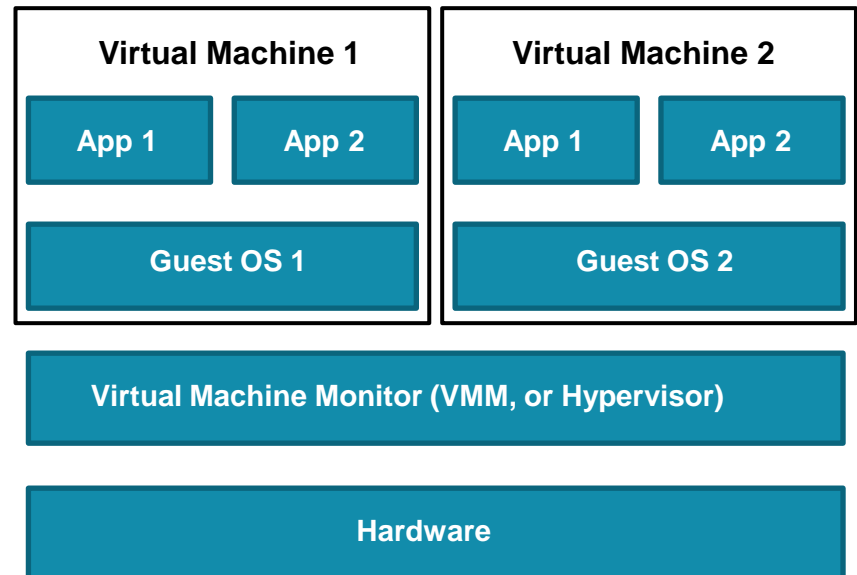
Virtualization with MMU-500

- Nested translation
  - Stage 1 and Stage 2
  - Supports virtual address (VA) programming of devices
  - Scatter/gather function

- Adds ARMv8 support
  - To enable interoperability with Cortex-A57 & Cortex-A53
  - Also supports Cortex-A15 and Cortex-A7 page table formats

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Virtualization with MMU-500
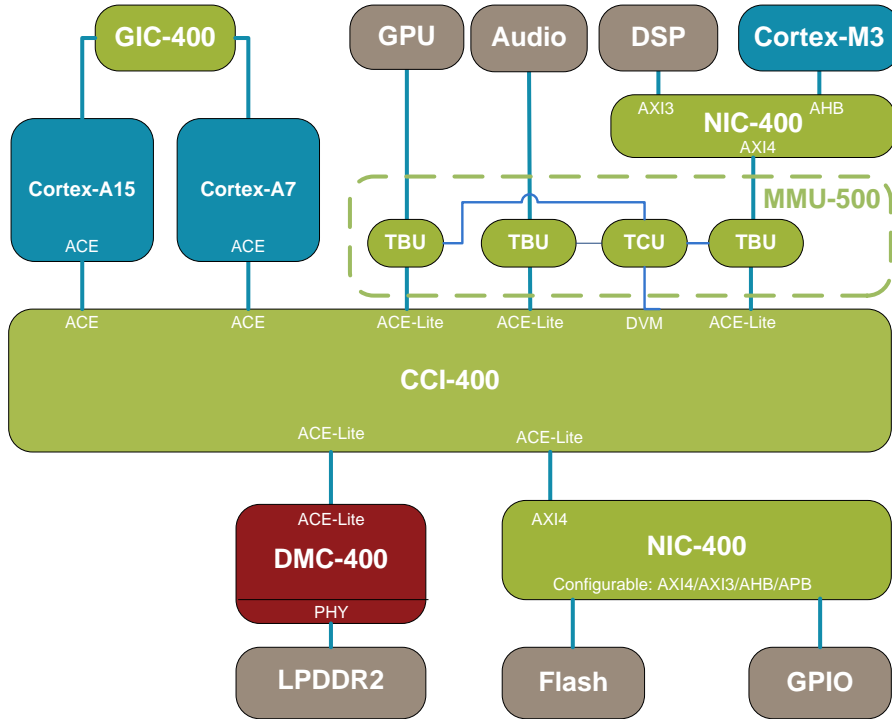
ARM System MMU Terminology:

TBU =   Translation Buffer Unit
           (containing the TLB)
TCU =   Translation Control Unit
           (containing the page table walker)

- Nested translation
  - Stage 1 and Stage 2
  - Supports virtual address (VA) programming of devices
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- Adds ARMv8 support
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  - Also supports Cortex-A15 and Cortex-A7 page table formats

- Distributed TLBs
  - To increase TLB efficiency and   to save power and area
  - Point-to-point connection
  - n x 1:1 TLB⇔TCU interfaces

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Generic Interrupt Controller for ARMv8
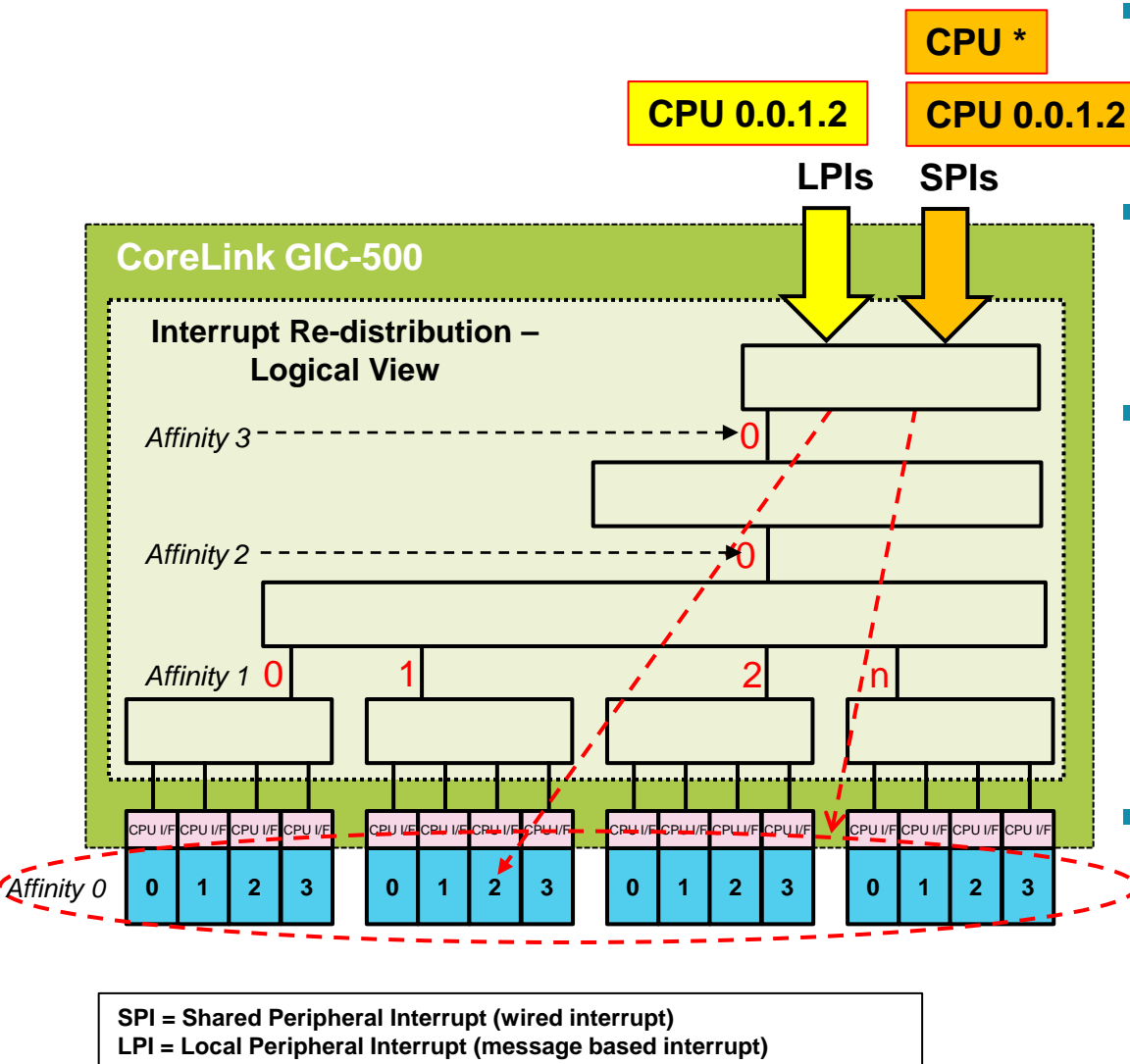
- GIC-500 supports 48 CPUs
  - Cortex-A57 and Cortex-A53
  - GICv3 architecture

- Shared Peripheral Interrupts
  - Up to 960 SPIs
  - Direct to AL0 or all

- Message based interrupts
  - Lower cost per interrupt
  - Direct to AL0
  - MSI(-X) support
  - VMs can directly program peripherals to reduce hypervisor overhead

- Affinity level routing
  - Allows for scalability
  - Consolidated as one monolithic block for GIC-500

SPI = Shared Peripheral Interrupt (wired interrupt)
LPI = Local Peripheral Interrupt (message based interrupt)

High Performance, Efficient, Cache Coherent

Up to 4 cores per cluster

Heterogeneous processors – CPU, GPU, DSP and accelerators

18 AMBA ACE-Lite interfaces for I/O coherency

4 fully coherent clusters

GIC-500

10-40 GbE | PCIe | DSP / DSP / DSP

DPI | Crypto | USB | SATA

NIC-400

Quad Cortex-A57 | Quad Cortex-A57 | Quad Cortex-A57 | Quad Cortex-A57

L2 cache | L2 cache | L2 cache | L2 cache

128-bit bus @ CPU frequency

MMU-500

CoreLink™ CCN-504 Cache Coherent Network

To minimize snoop traffic

8/16MB L3 cache

Snoop Filter

Integrated L3 cache

CoreLink™ DMC-520 | CoreLink™ DMC-520

NIC-400 Network Interconnect

Dual channel DDR3/4 x72

x72 DDR4-3200 | x72 DDR4-3200

Flash .... GPIO

Peripheral address space

Usable system bandwidth: ~ 1 Terabit/second

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Scalable System Features

CoreLink CCN-504	
CPU	4 ports up to 16 cores Cortex-A57, Cortex-A53 and Cortex-A15
IO	18 ports: AMBA® 4 AXI4/ACE-Lite interfaces
DDR	2 channels supported with CoreLink DMC-520
RAS	ECC on RAMs and parity on transport
QoS	QoS regulation and priority management
Security	TrustZone aware
Low Power Support	Extensive clock gating, leakage mitigation hooks, Granular DVFS and CPU shutdown support, Partial or full L3 cache shutdown, Retention modes

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Security, Reliability, Quality of Service

- 5th Generation ARM DMC targeting >95% DRAM efficiency
  - ECC and RAS features
  - Performance Profiling
  - TrustZone Address Space Control
- High efficiency through close integration with CCN-504
  - System wide QoS, designed and verified with ARM CPUs

RAS = Reliability, Availability, Serviceability

The Architecture for the Digital World® **ARM**®

Security, Reliability, Quality of Service

Within the diagram:
CoreLink DMC-520
Dynamic Memory Controller
System I/F
Config I/F
QoS
Memory Channel
Data Buffer for both Reads and Writes
RAS Features
Memory Interface
ECC Features
Performance Profiling I/F
Artisan® DDR4, 3 & 3L PHY 3200 Mbps
TrustZone® System Security by ARM

- 5th Generation ARM DMC targeting >95% DRAM efficiency
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RAS = Reliability, Availability, Serviceability

The Architecture for the Digital World® **ARM**®

High Performance Memory Access

CoreLink DMC-520	
Performance	Max bandwidth: 25.6 GB/s per channel Buffering to optimize read/write turnaround
Interfaces	Optimal direct connection to CCN-504 Industry standard DFI-3.0 to connect to PHY
PHY	Low-latency PHY from ARM
Memory	Support for x72 DRAM DDR3, DDR3L and DDR4 up to DDR4-3200
Low Power Support	Programmable DRAM power modes

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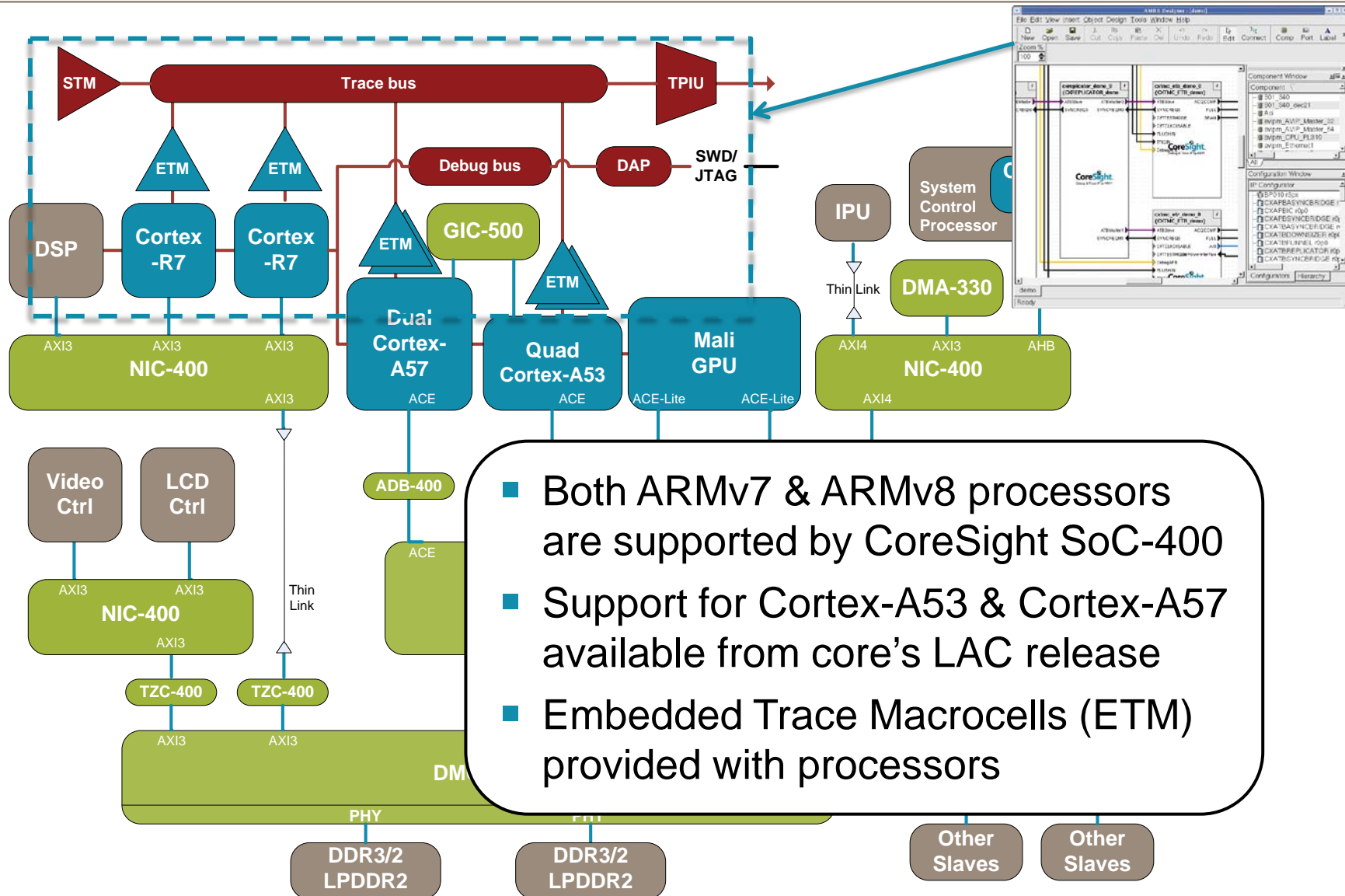# CoreLink End-to-End QoS Architecture

Enterprise Requirements

- "Bursty" datapath
  - High peak bandwidth
  - Multiple interfaces

- "Compute intensive" Control Path
  - Lowest latency requirements

- "Latency Sensitive" Air interface
  - Predictable Latency
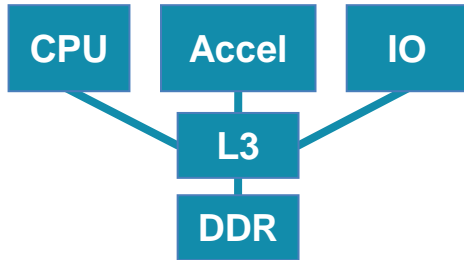
CoreLink End-to-End QoS

- QoS field for every transaction
  - Fixed, programmable or regulated
  - End-to-End propagation

- Programmable QoS mechanisms
  - Regulation of all traffic on ingress
  - Bandwidth management
  - Latency management

- QoS re-ordering and arbitration
  - Interconnect ingress
  - Non-blocking transport
  - L3 cache
  - DMC

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CoreSight SoC-400 for ARMv8

- Both ARMv7 & ARMv8 processors are supported by CoreSight SoC-400
- Support for Cortex-A53 & Cortex-A57 available from core's LAC release
- Embedded Trace Macrocells (ETM) provided with processors

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Summary

- CoreLink 400 series is available now
  - Coherency support for Cortex-A15, Cortex-A7 and the latest Cortex-A50 series
  - NIC-400 Network Interconnect for Cortex-A and Cortex-R series processors

- CoreLink 500 series offers new system scaling
  - 16 core support in CCN-504 Cache Coherent Network for enterprise applications
  - Enterprise DDR3/4 memory support with DMC-520
  - ARMv8 page stable support with MMU-500

- ARM CoreLink System IP offers the best ARM Cortex and Mali™ processor performance
  - Designed together, validated together

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