# Building 2016 Premium Mobile Systems Just Got a Whole Lot Easier

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**Explore ARM IP here**

2015 is looking like it's the year where 64-bit becomes a reality for the majority of major mobile OEMs. There is a particularly strong momentum in manufacturers of application processors targeted at smartphones, with all top-10 players having adopted ARMv8-A. This adoption is set to continue throughout 2015 as premium mobile makers seek to harness the increased potential that the upgrade in system architecture offers. What that means for consumers is devices that are fluid and responsive when handling all of the complex tasks demanded of modern smartphones and tablets.

I don't think I am alone in thinking that the main drivers in the premium mobile device market are human experiences and expectations. The demand for better user experiences on higher resolution displays whilst retaining fluid responses, with more device-to-device connectivity means that consumers are looking for the next great thing every year.

Recent history has shown that mobile devices are the preferred compute devices of choice. As we move forward this is not going to change.


**So why 64-bit in mobile?**

For the marketing folks it makes perfect sense as 64 is double 32, so it must be twice as good right? However there are also a number of technical merits supporting 64-bit designs going forward. The main reason is that it's the architecture and instruction-set-architecture (ISA) that makes the difference. The ISA allows compilers to work smarter and the microarchitecture implementation to be more efficient. Here are a few more benefits to 64-bit that have come off the top of my head:

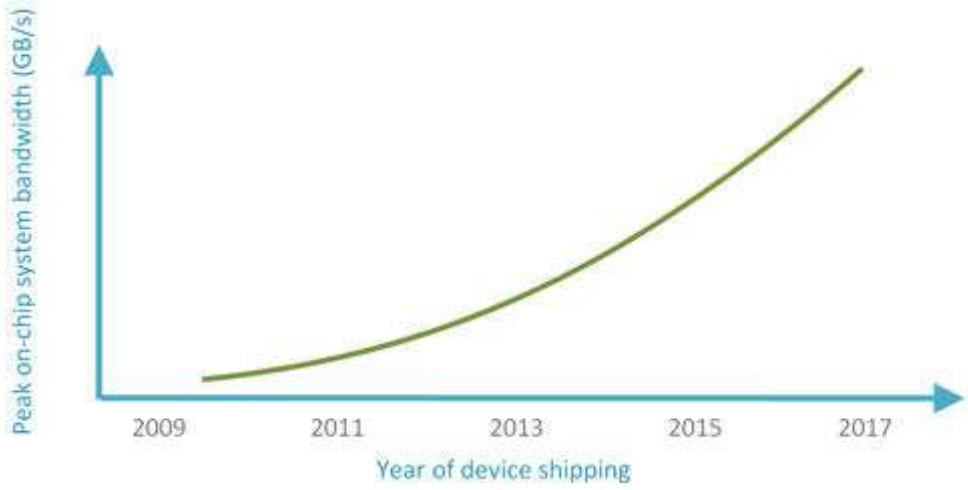
- You always have hardware floating point with 64-bit architecture there's no need to carry around software emulation for floating point operations. More registers to play with means more opportunity for optimisations like loop unrolling and less stack spillage to main memory. Function calls are cheaper in terms of memory usage and can pass twice as many 64-bit points in registers.
- The ability to handle small bursts of crypto also saves power, as there is no need to keep external crypto accelerators powered up for longer than necessary. It can process incredibly large numbers allowing users to better encrypt data against unauthorized access
- And finally where the 64-bit part really comes in, is that larger memory devices for complex and large datasets are becoming a reality. While 32-bit CPU's can only handle 4GB of RAM, 64-bit is virtually limitless (it can handle up to 16 exabytes, or more than 16 billion GB).

In short, there are plenty of reasons for designers to move to 64-bit now than ever before.

**Conflicting Requirements Bring Design Challenges**

Bandwidth requirements for premium mobile devices are expected to soar over the next few years and there are several key use cases supporting this trend.

Screen sizes and resolutions have increased across a wide range of devices, and frames per second have increased - not only for consuming content but also for capturing it. As more people capture content via their mobile' s camera, there is greater demand on higher resolution for stills and video capture:




One of the largest users of memory bandwidth in a SoC is the media subsystem components - GPU, video and display. Nobody wants the annoyance of having his or her screen freeze when capturing that crucial moment on camera, so it is vital that the bandwidth efficiency is optimal here.

Whilst we are making advances in frame-buffer compression technology such as AFBC, peak bandwidth requirements continue to grow.

As our mobile devices become central to our digital lives, those capabilities must be paired with the power efficiency required to work through a full day of heavy use on a single charge. Modern mobile design requires a commitment to getting the most out of every milliwatt and every millimetre of silicon.

As engineers and technologists in this market, we have the challenge of delivering this mobile experience within tight energy and thermal constraints. You also have to combine the trade-offs that exist between maximising the SoC performance and making sure that it reaches tapeout on schedule. The current trend is for handset OEMs to release at least one new product each year to keep up with the voracious appetite of consumers for devices that are

thinner, lighter, and more capable of doing complex task. These desires can be conflicting as release schedule pressures often carry more weight than design improvements.

Time to market limitations often force the hand of system architects as they need to focus on the important deliverables and automate as many tasks as possible.

**Automating the System Design Flow**

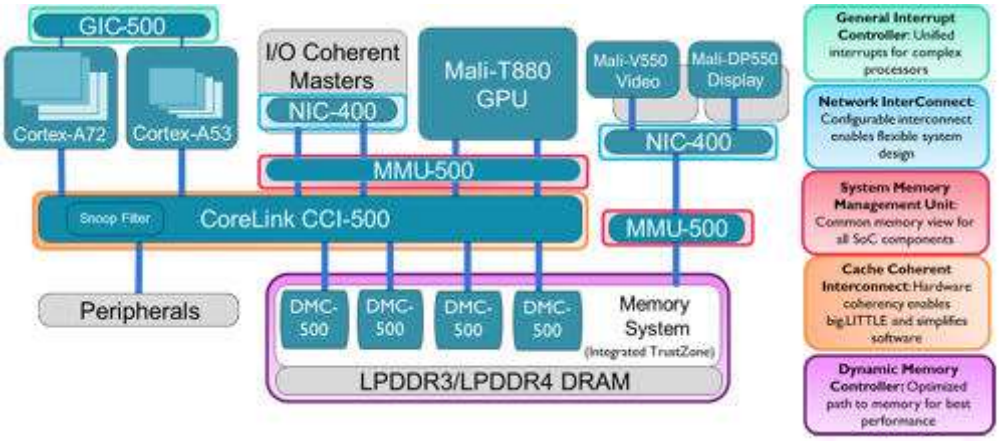
An area where automation can make a big difference is in system configuration and assembly. Modern, multi-core 64-bit SoCs contain a lot of complexity from different IP blocks and traditional methods of configuring and stitching by hand take an excessive amount of time and can be error-prone. Automation in this sphere can not only free up designers to focus on higher value tasks, but a rules-based connection methodology will also reduce the chance of bugs in the design flow.

The recently announced Socrates IP tooling suite gives acceleration in system design. What previously would have taken months to assemble by hand now only takes a matter of days, making a huge difference in the tapeout schedules of SoC designers. It does this through an IP-XACT standardization process of each IP block's interfaces and registers. Then, the user interface takes advantage of built-in ARM engineering intelligence to automatically synthesize the micro-architecture and make the SoC connections. Let’ s take a look at some of the ARM System IP components that are integrated with Socrates:

The system interconnect fabric in modern SoCs is a highly configurable IP block that is the artery of the chip, providing connections to the processor clusters, GPU and memory channels. This level of connectivity means there are a lot of permutations for how it can be configured depending on design requirements, which is where doing it by hand become complicated. Using rules to manage the configuration of the interconnect, such as a CoreLink CCI-500 or NIC-400, actually makes a significant reduction to the time it takes to integrate each IP block together and assemble the system.

**System IP is Central to ARM Systems**

Given that we have CoreLink CCI-500 at the core of our system, we can now look at the other System IP components that work in concert with the CCI to help partners build 64-bit systems. When you look at this example representation of a Premium Mobile SoC you can see there is a significant amount of System IP performing multiple tasks.




CoreLink GIC-500 Generic Interrupt Controller manages migration of interrupts between CPUs and allows for virtualization of interrupts in a hypervisor controlled system.  Compared with the previous generation GIC-400, the GIC-500 supports more than eight CPUs and also supports message-based interrupts as well as directly connecting to ARMv8 Cortex-A72 and Cortex-A53 system register interfaces instead of ARMv7 IRQ and FIQ inputs.

CoreLink MMU-500 System Memory Management Unit supports a common physical memory view for IO devices by sharing the same page tables as the CPUs.

CoreLink TZC-400 TrustZone Address Space Controller and CoreLink DMC-400 Dynamic memory controller are used for efficient DRAM memory access supporting TrustZone memory protection and end-to-end QoS.

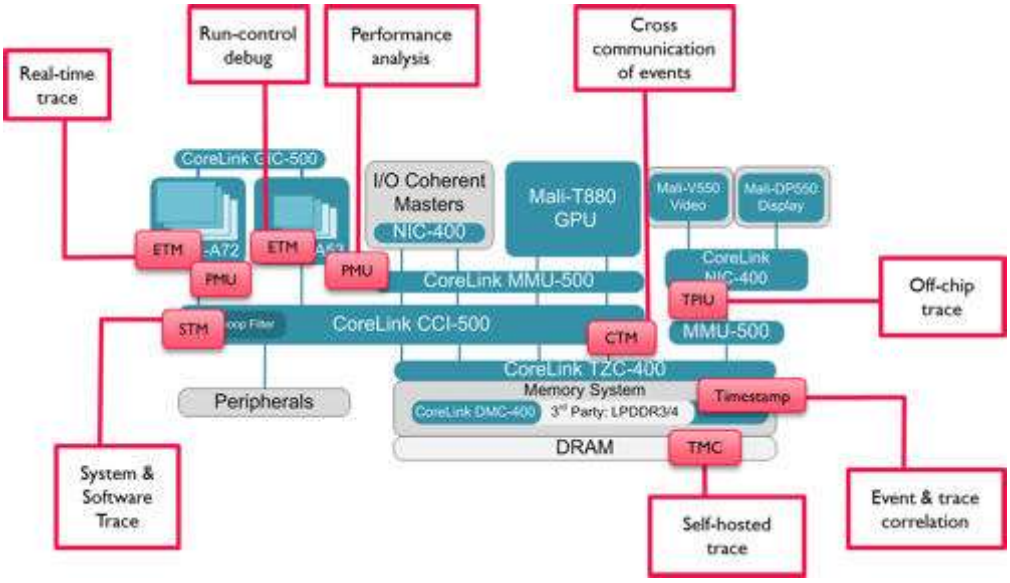
Rest of SoC connectivity is serviced by CoreLink NIC-400 which provides a fully configurable interconnect solution to connect sub-systems such as video, display and peripherals. NIC-400 configurability enables partners to build

hierarchical, low latency, low power connectivity for AMBA® 4 AXI4™, AMBA 3 AXI3™, AHB™-Lite and APB™ components.

The fact that all of these System IP components are designed, implemented and validated with ARM Cortex processors and the Mali Media library reduces overall system latency. These enhancements play a key role in the performance uplift that 64-bit computing brings to mobile. They are all supported by the Socrates Design Environment that makes their configuration and integration as simple as clicking a button.

**Debug & Trace for 64-bit**

The increased processing throughput in 64-bit system impacts debugging solutions as well, particularly the increase in output bandwidth from the trace macrocell. Debug and trace System IP is also critical for helping ARM partners to debug and optimise software for 64-bit systems comprising:




ETM and PMU for real time trace and software performance analysis

System Trace Macrocell for unobtrusive tracing of Systems and Software

Trace Memory Controller for directing trace data for self-hosted trace

Trace point interface unit for directing trace data off-chip

Cross trigger matrix for cross communication of system events whilst debugging

And finally, Timestamp for event correlation

CoreSight SoC-400 currently provides the most complete on-chip debug and real-time trace solution for the entire system-on-chip (SoC), making ARM processor-based SoCs the easiest to debug and optimize. A colleague has explained how to build customised debug and trace solutions for multi-core SoCs using CoreSight SoC-400, showing the value that a well-thought out debug & trace system can offer to all stages of SoC development. The new CoreSight Creator also enables partners to easily configure and generate a CoreSight debug and trace subsystem in days with minimal engineering interaction.

**64-bit in 2015**

We' ve discussed for 64-bit mobile devices, consumers expect something new every year with better and better performance. What I' ve done in this blog is introduce some of the key IP components that all contribute to the premium devices that are faster and more power-efficient each year. 2015 will be a year where we see the 64-bit mobile device reach a wide audience thanks to the outstanding work of our ARM partners! Mobile OEMs are currently in an annual loop of delivering greater advancements to the market. SoC manufacturers are part of that supply chain and hence feel the same pressures. Building a 64-bit SoC has never been easier owing to all of the IP that has been designed and optimized for the purpose. ARM System IP and tooling enable optimised SoCs to be designed and built much faster, allowing architects to beat deadlines and focus on more precise performance improvements.

As system performance increases, so does the need to tightly control the thermal and energy envelope of the system. Whether it is lowest latency or highest bandwidth demanded by the processors, ARM System IP delivers outstanding efficiency to achieve the performance required with the lowest power and smallest area.

For more information on the System IP portfolio please visit: System IP - ARM

**Explore ARM IP here**

- **CoreLink NIC-301 Network Interconnect**
- **CoreLink GIC-390 General Interrupt Controller**
- **CoreSight ETM 10 Embedded Trace Macrocell**