JEDEC STANDARD

Addendum No. 1 to JESD79-3 - 1.35 V DDR3L-800, DDR3L-1066, DDR3L-1333, DDR3L-1600, and DDR3L-1866

JESD79-3-1A.01

(Minor Editorial Revision of JESD79-3-1A, January 2013)

MAY 2013

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or call (703) 907-7559 or www.jedec.org

Published by
©JEDEC Solid State Technology Association 2013
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

PRICE: Please refer to www.jedec.org

PLEASE!

DON'T VIOLATE
THE
LAW!

JEDEC Solid State Technology Association
3103 North 10th Street, Suite 240S
Arlington, Virginia 22201
or call (703) 907-7559

1.35 V DDR3-800, DDR3L-1066, DDR3L-1333, DDR3L-1600, and DDR3L-1866

(From JEDEC Board Ballot, JCB-10-12 and JCB-11-95, formulated under the cognizance of the JC-42.3 Subcommittee on Volatile RAM.)

1 Scope

The JESD79-3 document defines DDR3L SDRAM, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments with the exception of what is stated within this standard.

The purpose of this standard is to define the DDR3L specifications that supersede the DDR3 specifications as defined in JESD79-3. The use of DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600, and DDR3-1866 titles in JESD79-3 are to be interpreted as DDR3L-800, DDR3L-1066, DDR3L-1333, DDR3L-1600,and DDR3L-1866, respectively, when applying towards DDR3L definition; unless specifically stated otherwise.

2 DDR3L VDD/VDDQ requirements

Table 1 — Input/output functional description

Symbol	Type	Function
V_{DD}	Supply	Power Supply: DDR3L operation = 1.283 V to 1.45 V; DDR3 operation = 1.425 V to 1.575 V
V_{DDQ}	Supply	DQ Power Supply: DDR3L operation = 1.283 V to 1.45 V; DDR3 operation = 1.425 V to 1.575 V

Table 2 — Recommended DC Operating Conditions - DDR3L (1.35 V) operation

Symbol	Parameter/Condition	min	Typ	max	Units	Notes
V_{DD}	Supply voltage	1.283	1.35	1.45	V	1,2,3,4
V_{DDQ}	Supply voltage for Output	1.283	1.35	1.45	V	1,2,3,4

NOTE 1 Maximum DC value may not be greater than 1.425V. The DC value is the linear average of $V_{DD}/V_{DDQ}(t)$ over a very long period of time (e.g., 1 sec).
NOTE 2 If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
NOTE 3 Under these supply voltages, the device operates to this DDR3L specifcation.
NOTE 4 Once initialized for DDR3L operation, DDR3 operation may only be used if the device is in reset while V_{DD} and $V_{DD}Q$ are changed for DDR3 operation (see Figure 1).

2 DDR3L VDD/VDDQ requirements (cont'd)

Table 3 — Recommended DC Operating Conditions - DDR3 (1.5 V) operation

Symbol	Parameter/Condition	min	Typ	max	Units	Notes
V_{DD}	Supply voltage	1.425	1.5	1.575	V	1,2,3
V_{DDQ}	Supply voltage for Output	1.425	1.5	1.575	V	1,2,3

NOTE 1 If minimum limit is exceeded, input levels shall be governed by DDR3L specifications.
NOTE 2 Under 1.5 V operation, this DDR3L device operates to the DDR3 specifcations under the same speed timings as defined for this device.
NOTE 3 Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while V_{DD} and V_{DDQ} are changed for DDR3L operation (see Figure 1).

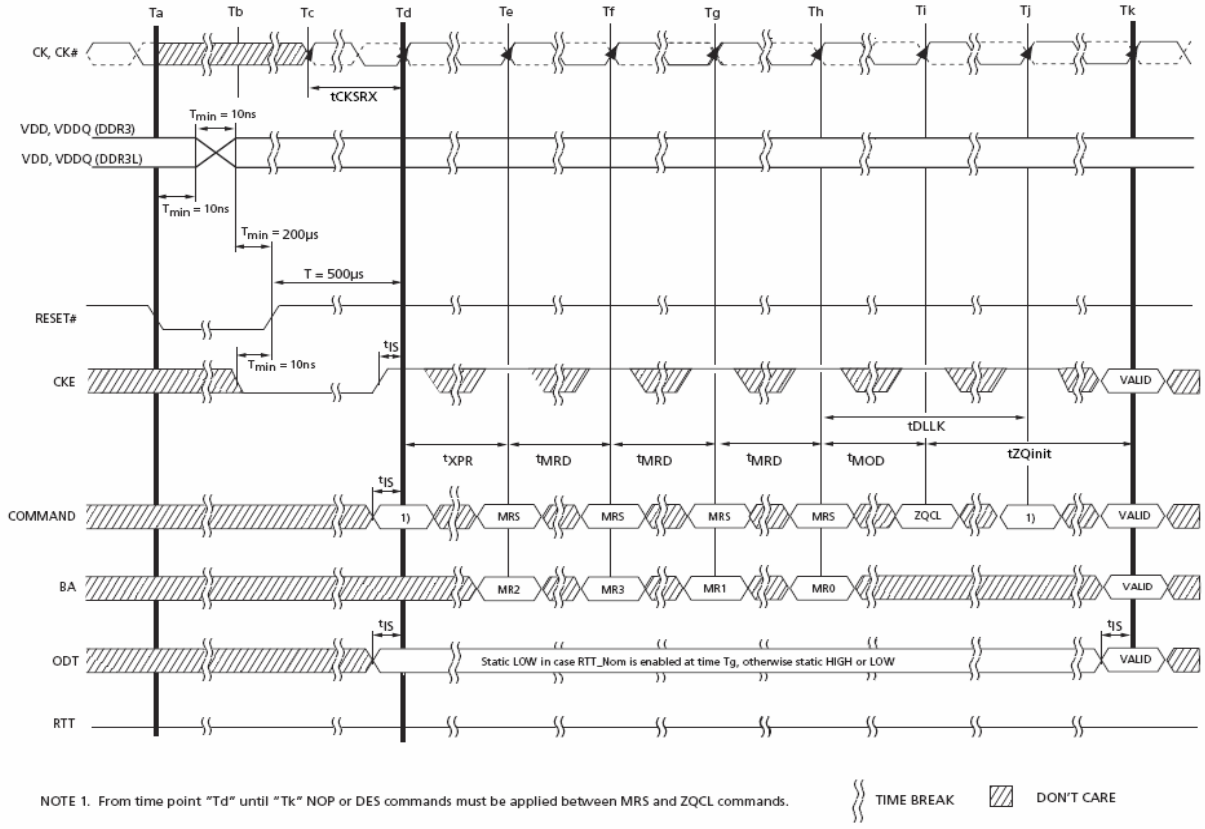

Figure 1 — V_{DDQ}/V_{DDQ} Voltage Switch Between DDR3L and DDR3

3 1.35 V DDR3L AC and DC Logic Input Levels for Single-Ended Signals

3.1 AC and DC Input Levels for Single-Ended Command and Address Signals

Table 4 — Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3L-800, DDR3L-1066		DDR3L-1333, DDR3L-1600		DDR3L-1866		Unit	Notes
		min	max	min	max	min	max		
VIH.CA(DC90)	DC input logic high	Vref + 0.09	V_{DD}	Vref + 0.09	V_{DD}	Vref + 0.09	V_{DD}	V	1
VIL.CA(DC90)	DC input logic low	V_{SS}	Vref - 0.09	V_{SS}	Vref - 0.09	V_{SS}	Vref - 0.09	V	1
VIH.CA(AC160)	AC input logic high	Vref + 0.160	Note 2	Vref + 0.160	Note 2	-	-	V	1, 2, 5
VIL.CA(AC160)	AC input logic low	Note 2	Vref - 0.160	Note 2	Vref - 0.160	-	-	V	1, 2, 5
VIH.CA(AC135)	AC input logic high	Vref + 0.135	Note 2	Vref + 0.135	Note 2	Vref + 0.135	Note 2	V	1, 2, 5
VIL.CA(AC135)	AC input logic low	Note 2	Vref - 0.135	Note 2	Vref - 0.135	Note 2	Vref - 0.135	V	1, 2, 5
VIH.CA(AC125)	AC input logic high	-	-	-	-	Vref + 0.125	Note 2	V	1, 2, 5
VIL.CA(AC125)	AC input logic low	-	-	-	-	Note 2	Vref - 0.125	V	1, 2, 5
VRefCA(DC)	Reference Voltage for ADD, CMD inputs	0.49 * V_{DD}	0.51 * V_{DD}	0.49 * V_{DD}	0.51 * V_{DD}	0.49 * V_{DD}	0.51 * V_{DD}	V	3, 4

NOTE 1 For input only pins except RESET#. Vref = VrefCA(DC).
NOTE 2 See JESD79-3E, 9.6 “Overshoot and Undershoot Specifications”, 9.6.1.
NOTE 3 The AC peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{RefDQ(DC)}$ by more than +/-1% V_{DD} (for reference: approx. +/- 13.5 mV).
NOTE 4 For reference: approx. $V_{DD}/2$ +/- 13.5 mV
NOTE 5 These levels apply for 1.35 Volt (see Table 4) operation only. If the device is operated at 1.5 V (see Table 23), the respective levels in JESD79-3 (VIH/L.CA(DC100), VIH/L.CA(AC175), VIH/L.CA(AC150), VIH/L.CA(AC135), VIH/L.CA(AC125), etc.) apply. The 1.5 V levels (VIH/L.CA(DC100), VIH/L.CA(AC175), VIH/L.CA(AC150), VIH/L.CA(AC135), VIH/L.CA(AC125), etc.) do not apply when the device is operated in the 1.35 voltage range.

3.2 AC and DC Input Levels for Single-Ended Data Signals

Table 5 — Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3L-800, DDR3L-1066		DDR3L-1333, DDR3L-1600		DDR3L-1866		Unit	Notes
		min	max	min	max	min	max		
VIH.DQ(DC90)	DC input logic high	Vref + 0.09	V_{DD}	Vref + 0.09	V_{DD}	Vref + 0.09	V_{DD}	V	1
VIL.DQ(DC90)	DC input logic low	V_{SS}	Vref - 0.09	V_{SS}	Vref - 0.09	V_{SS}	Vref - 0.09	V	1
VIH.DQ(AC160)	AC input logic high	Vref + 0.160	Note 2	-	-	-	-	V	1, 2, 5
VIL.DQ(AC160)	AC input logic low	Note 2	Vref - 0.160	-	-	-	-	V	1, 2, 5
VIH.DQ(AC135)	AC input logic high	Vref + 0.135	Note 2	Vref + 0.135	Note 2	-	-	V	1, 2, 5
VIL.DQ(AC135)	AC input logic low	Note 2	Vref - 0.135	Note 2	Vref - 0.135	-	-	V	1, 2, 5
VIH.DQ(AC130)	AC input logic high	-	-	-	-	Vref + 0.130	Note 2	V	1, 2, 5
VIL.DQ(AC130)	AC input logic low	-	-	-	-	Note 2	Vref - 0.130	V	1, 2, 5
VRefDQ(DC)	Reference Voltage for DQ, DM inputs	0.49 * V_{DD}	0.51 * V_{DD}	0.49 * V_{DD}	0.51 * V_{DD}	0.49 * V_{DD}	0.51 * V_{DD}	V	3, 4

NOTE 1 For input only pins except RESET#. Vref = VrefDQ(DC).
NOTE 2 See JESD79-3E, 9.6 “Overshoot and Undershoot Specifications”, 9.6.2.
NOTE 3 The AC peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{RefDQ(DC)}$ by more than +/-1% V_{DD} (for reference: approx. **+/- 13.5 mV**).
NOTE 4 For reference: approx. **$V_{DD}/2$ +/- 13.5 mV**.
NOTE 5 These levels apply for 1.35 Volt (see Table 5) operation only. If the device is operated at 1.5 V (see Table 24), the respective levels in JESD79-3 (VIH/L.DQ(DC100), VIH/L.DQ(AC175), VIH/L.DQ(AC150), VIH/L.DQ(AC135), etc.) apply. The 1.5 V levels (VIH/L.DQ(DC100), VIH/L.DQ(AC175), VIH/L.DQ(AC150), VIH/L.DQ(AC135), etc.) do not apply when the device is operated in the 1.35 voltage range.

4 1.35 V DDR3L Electrical Characteristics and AC Timing

Table 6 — Timing Parameters by Speed Bin[a]

Parameter	Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units	Notes
		min	max	min	max	min	max	min	max	min	max		
Data Timing													
Data setup time to DQS, DQS# referenced to Vih.DQ(ac) / Vil.DQ(ac) levels	tDS(base) AC160 SR = 1V/ns	90	-	40	-	-	-	-	-	-	-	ps	Refer to JESD79-3 d, 17
	tDS(base) AC135 SR = 1V/ns	140	-	90	-	45	-	25	-	-	-	ps	Refer to JESD79-3 d, 17
	tDS(base) AC130 SR = 2V/ns	-	-	-	-	-	-	-	-	70	-	ps	Refer to JESD79-3 d
Data hold time from DQS, DQS# referenced to Vih.DQ(dc) / Vil.DQ(dc) levels	tDH(base) DC90 SR = 1V/ns	160	-	110	-	75	-	55	-	-	-	ps	Refer to JESD79-3 d, 17
	tDH(base) DC90 SR = 2V/ns	-	-	-	-	-	-	-	-	75	-	ps	Refer to JESD79-3 d
Command and Address Timing													
Command and Address setup time to CK, CK# referenced to Vih.CA(ac) / Vil.CA(ac) levels	tIS(base) AC160 SR = 1V/ns	215	-	140	-	80	-	60	-	-	-	ps	Refer to JESD79-3 b, 16
	tIS(base) AC135 SR = 1V/ns	365	-	290	-	205	-	185	-	65	-	ps	Refer to JESD79-3 b, 16
	tIS(base) AC125 SR = 1V/ns	-	-	-	-	-	-	-	-	150	-	ps	Refer to JESD79-3 b, 16
Command and Address hold time from CK, CK# referenced to Vih.CA(dc) / Vil.CA(dc) levels	tIH(base) DC90 SR = 1V/ns	285	-	210	-	150	-	130	-	110	-	ps	Refer to JESD79-3 b, 16

[a] The setup and hold parameters in this table apply for 1.35 V (see Table 2) operation only. If the device is operated at 1.5 V (see Table 3), the respective parameters in JESD79-3 (tIS(base, AC175), tIS(base, AC150), tIH(base, DC100), tDS(base, AC175), tDS(base, AC150), tDH(base, DC100), etc.) apply. The 1.5 V setup/hold parameters (tIS(base, AC175), tIS(base, AC150), tIH(base, DC100), tDS(base, AC175), tDS(base, AC150), tDH(base, DC100), etc.) do not apply when the device is operated in the 1.35 voltage range.

NOTE 1 The general notes from JESD79-3E, 13.4, apply to Table 6.
NOTE 2 V_{DD} =V_{DD}Q = 1.35 V +0.100/- 0.067V

Table 7 — ADD/CMD Setup and Hold Base-Values for 1 V/ns

Symbol	Reference	DDR3L-800	DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	Units	Note
tIS(base) AC160	$V_{IH/L(AC)}$: SR=1 V/ns	215	140	80	60	-	ps	1
tIS(base) AC135	$V_{IH/L(AC)}$: SR=1 V/ns	365	290	205	185	65	ps	1, 2
tIS(base) AC125	$V_{IH/L(AC)}$: SR=1 V/ns	-	-	-	-	150	ps	1, 3
tIH(base) DC90	$V_{IH/L(DC)}$: SR=1 V/ns	285	210	150	130	110	ps	1

NOTE 1 (AC/DC referenced for 1 V/ns Address/Command slew rate and 2 V/ns differential CK-CK# slew rate)
NOTE 2 The tIS(base) AC135 specifications are adjusted from the tIS(base) AC160 specification by adding an additional 125 ps for DDR3L-800/1066 or 100 ps for DDR3L-1333/1600 of derating to accommodate for the lower alternate threshold of 135 mV and another 25 ps to account for the earlier reference point [(160 mV - 135 mV) / 1 V/ns].
NOTE 3 The tIS(base) AC125 specifications are adjusted from the tIS(base) AC135 specification by adding an additional 75 ps for DDR3L-1866 of derating to accommodate for the lower alternate threshold of 135 mV and another 10 ps to account for the earlier reference point [(135 mV - 125 mV) / 1 V/ns].

4.1 Address / Command Setup, Hold and Derating

Table 8 — Derating values DDR3L-800/1066/1333/1600 tIS/tIH - AC/DC based

ΔtIS, ΔtIH derating in [ps] AC/DC based AC160 Threshold -> VIH(ACAC)=VREF(DC)+160 mV, VIL(AC)=VREF(DC)-160 mV																	
		CK,CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ ADD Slew rate V/ns	2.0	80	45	80	45	80	45	88	53	96	61	104	69	112	79	120	95
	1.5	53	30	53	30	53	30	61	38	69	46	77	54	85	64	93	80
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-1	-3	-1	-3	-1	-3	7	5	15	13	23	21	31	31	39	47
	0.8	-3	-8	-3	-8	-3	-8	5	1	13	9	21	17	29	27	37	43
	0.7	-5	-13	-5	-13	-5	-13	3	-5	11	3	19	11	27	21	35	37
	0.6	-8	-20	-8	-20	-8	-20	0	-12	8	-4	16	4	24	14	32	30
	0.5	-20	-30	-20	-30	-20	-30	-12	-22	-4	-14	4	-6	12	4	20	20
	0.4	-40	-45	-40	-45	-40	-45	-32	-37	-24	-29	-16	-21	-8	-11	0	5

Table 9 — Derating values DDR3L-800/1066/1333/1600 tIS/tIH - AC/DC based Alternate AC135 Threshold

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC135 Threshold -> VIH(AC)=VREF(DC)+135 mV, VIL(AC)=VREF(DC)-135 mV																	
		CK,CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ ADD Slew rate V/ns	2.0	68	45	68	45	68	45	76	53	84	61	92	69	100	79	108	95
	1.5	45	30	45	30	45	30	53	38	61	46	69	54	77	64	85	80
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	2	-3	2	-3	2	-3	10	5	18	13	26	21	34	31	42	47
	0.8	3	-8	3	-8	3	-8	11	1	19	9	27	17	35	27	43	43
	0.7	6	-13	6	-13	6	-13	14	-5	22	3	30	11	38	21	46	37
	0.6	9	-20	9	-20	9	-20	17	-12	25	-4	33	4	41	14	49	30
	0.5	5	-30	5	-30	5	-30	13	-22	21	-14	29	-6	37	4	45	20
	0.4	-3	-45	-3	-45	-3	-45	6	-37	14	-29	22	-21	30	-11	38	5

4.1 Address / Command Setup, Hold and Derating (cont'd)

Table 10 — Derating values DDR3L-1866 tIS/tIH - AC/DC based Alternate AC125 Threshold

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC125 Threshold -> VIH(AC)=VREF(DC)+125 mV, VIL(AC)=VREF(DC)-125 mV																
		CK,CK# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD/ ADD Slew rate V/ns	**2.0**	63	45	63	45	63	45	71	53	79	61	87	69	95	79	103	95
	1.5	42	30	42	30	42	30	50	38	58	46	66	54	74	64	82	80
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	3	-3	3	-3	3	-3	11	5	19	13	27	21	35	31	43	47
	0.8	6	-8	6	-8	6	-8	14	1	22	9	30	17	38	27	46	43
	0.7	10	-13	10	-13	10	-13	18	-5	26	3	34	11	42	21	50	37
	0.6	16	-20	16	-20	16	-20	24	-12	32	4	40	-4	48	14	56	30
	0.5	15	-30	15	-30	15	-30	23	-22	31	-14	39	-6	47	4	55	20
	0.4	13	-45	13	-45	13	-45	21	-37	29	-29	37	-21	45	-11	53	5

Table 11 — Required time t_{VAC} above VIH(AC) {below VIL(AC)} for valid ADD/CMD transition

	DDR3L-800/1066/1333/1600				DDR3L-1866			
Slew Rate [V/ns]	t_{VAC} @ 160 mV [ps]		t_{VAC} @ 135 mV [ps]		t_{VAC} @ 135 mV [ps]		t_{VAC} @ 125 mV [ps]	
	min	max	min	max	min	max	min	max
> 2.0	200	-	213	-	200	-	205	-
2.0	200	-	213	-	200	-	205	-
1.5	173	-	190	-	178	-	184	-
1.0	120	-	145	-	133	-	143	-
0.9	102	-	130	-	118	-	129	-
0.8	80	-	111	-	99	-	111	-
0.7	51	-	87	-	75	-	89	-
0.6	13	-	55	-	43	-	59	-
0.5	Note	-	10	-	Note	-	18	-
< 0.5	Note	-	10	-	Note	-	18	-

NOTE Rising input signal shall become equal to or greater than VIH(ac) level and falling input signal shall become equal to or less than VIL(ac) level.

4.2 Data Setup, Hold and Slew Rate Derating

t_{DS}(base) and t_{DH}(base) of DDR3L-1866 are referenced for 2 V/ns DQ-slew-rate and 4 V/ns DQS slew-rate. Derating values Dt_{DS} and Dt_{DH} with DQ base slew rate 2 V/ns shall be used to calculate total tDS and tDH of DDR3L-1866. This means that for data input signal above 1600 Mbps the reference slew rate for setup/hold specification shall be set to 2 V/ns. When DDR3L-1866 devices are used at or below 1600 Mbps they shall meet an associated data setup/hold specification (including reference slew rate, levels and derating table) of the speed grade associated with that data rate.

EXAMPLE A 1866 device operating at 1600 Mbps shall require t_{DS}(AC135) = 25 ps and t_{DH}(DC90) = 55 ps at 1 V/ns (and the respective derating table.) Note that the AC levels of 130 mV also do not apply if the device is not operated at highest data rate.

Table 12 — Data Setup and Hold Base-Values

Symbol	Reference	DDR3L-800	DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	Units	Note
tDS(base) AC160	$V_{IH/L(AC)}$: SR=1 V/ns	90	40	-	-	-	ps	1
tDS(base) AC135	$V_{IH/L(AC)}$: SR=1 V/ns	140	90	45	25	-	ps	1
tDS(base) AC130	$V_{IH/L(AC)}$: SR=2 V/ns	-	-	-	-	70	ps	2
tDH(base) DC90	$V_{IH/L(DC)}$: SR=2 V/ns	-	-	-	-	75	ps	2
tDH(base) DC90	$V_{IH/L(DC)}$: SR=1 V/ns	160	110	75	55	-	ps	1

NOTE 1 (AC/DC referenced for 1 V/ns DQ-slew rate and 2 V/ns DQS slew rate)
NOTE 2 (AC/DC referenced for 2 V/ns DQ-slew rate and 4 V/ns DQS slew rate)

Table 13 — Derating values DDR3L-800/1066 tDS/tDH - AC/DC based

ΔtDS, ΔtDH derating in [ps] AC/DC based[a] AC160 Threshold -> VIH(AC)=VREF(DC)+160mV, VIL(AC)=VREF(DC)-160mV																	
		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	80	45	80	45	80	45	-	-	-	-	-	-	-	-	-	-
	1.5	53	30	53	30	53	30	61	38	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-1	-3	-1	-3	7	5	15	13	23	21	-	-	-	-
	0.8	-	-	-	-	-3	-8	5	1	13	9	21	17	29	27	-	-
	0.7	-	-	-	-	-	-	3	-5	11	3	19	11	27	21	35	37
	0.6	-	-	-	-	-	-	-	-	8	-4	16	4	24	14	32	30
	0.5	-	-	-	-	-	-	-	-	-	-	4	-6	12	4	20	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-8	-11	0	5

a. Cell contents shaded in red are defined as ‘not supported’.

4.2 Data Setup, Hold and Slew Rate Derating (cont'd)

Table 14 — Derating values for DDR3L-800/1066/1333/1600 tDS/tDH - (AC135)

ΔtDS, ΔtDH derating in [ps] AC/DC based [a] Alternate AC135 Threshold -> VIH(AC)=VREF(DC)+135mV, VIL(AC)=VREF(DC)-135mV																	
		DQS, DQS# Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	68	45	68	45	68	45	-	-	-	-	-	-	-	-	-	-
	1.5	45	30	45	30	45	30	53	38	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	2	-3	2	-3	10	5	18	13	26	21	-	-	-	-
	0.8	-	-	-	-	3	-8	11	1	19	9	27	17	35	27	-	-
	0.7	-	-	-	-	-	-	14	-5	22	3	30	11	38	21	46	37
	0.6	-	-	-	-	-	-	-	-	25	-4	33	4	41	14	49	30
	0.5	-	-	-	-	-	-	-	-	-	-	29	-6	37	4	45	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	30	-11	38	5

a. Cell contents shaded in red are defined as 'not supported'.

Table 15 — Required time t_{VAC} above VIH(AC) {below VIL(AC)} for valid transition

ΔtDS, ΔDH derating in [ps] AC/DC based [a] Alternate AC130 Threshold -> VIH(AC)=VREF(DC)+130mV, VIL(AC)=VREF(DC)-130mV																									
		DQS, DQS# Differential Slew Rate																							
		8.0 V/ns		7.0 V/ns		6.0 V/ns		5.0 V/ns		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	4.0	33	23	33	23	33	23	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.5	28	19	28	19	28	19	28	19	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	3.0	22	15	22	15	22	15	22	15	22	15	-	-	-	-	-	-	-	-	-	-	-	-	-	-
	2.5	-	-	13	9	13	9	13	9	13	9	13	9	-	-	-	-	-	-	-	-	-	-	-	-
	2.0	-	-	-	-	0	0	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-
	1.5	-	-	-	-	-	-	-22	-15	-22	-15	-22	-15	-22	-15	-14	-7	-	-	-	-	-	-	-	-
	1.0	-	-	-	-	-	-	-	-	-65	-45	-65	-45	-65	-45	-57	-37	-49	-29	-	-	-	-	-	-
	0.9	-	-	-	-	-	-	-	-	-	-	-62	-48	-62	-48	-54	-40	-46	-32	-38	-24	-	-	-	-
	0.8	-	-	-	-	-	-	-	-	-	-	-	-	-61	-53	-53	-45	-45	-37	-37	-29	-29	-19	-	-
	0.7	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-49	-50	-41	-42	-33	-34	-25	-24	-17	-8
	0.6	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-37	-49	-29	-41	-21	-31	-13	-15
	0.5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-31	-51	-23	-41	-15	-25
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-28	-56	-20	-40

a. Cell contents shaded in red are defined as 'not supported'.

4.2 Data Setup, Hold and Slew Rate Derating (cont'd)

Table 16 — Required time t_{VAC} above VIH(AC) {below VIL(AC)} for valid transition

Slew Rate [V/ns]	DDR3L-800/1066 (AC160)		DDR3L-800/1066/1333/ 1600 (AC135)		DDR3L-1866 (AC130)	
	t_{VAC} [ps]		t_{VAC} [ps]		t_{VAC} [ps]	
	min	max	min	max	min	max
> 2.0	165	-	113	-	95	-
2.0	165	-	113	-	95	-
1.5	138	-	90	-	73	-
1.0	85	-	45	-	30	-
0.9	67	-	30	-	16	-
0.8	45	-	11	-	Note	-
0.7	16	-	Note	-	-	-
0.6	Note	-	Note	-	-	-
0.5	Note	-	Note	-	-	-
< 0.5	Note	-	Note	-	-	-

NOTE Rising input signal shall become equal to or greater than VIH(AC) level and falling input signal shall become equal to or less than VIL(AC) level.

5 1.35 V DDR3L Input/Output Capacitance

Table 17 — Input / Output Capacitance

		DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units	Notes
Parameter	Symbol	min	max	min	max	min	max	min	max	min	max		
Input/output capacitance (DQ,DM,DQS,DQS#, TDQS,TDQS#)	C_{IO}	1.4	2.5	1.4	2.5	1.4	2.3	1.4	2.2	1.4	2.1	pF	1,2,3
Input capacitance, (CTRL, ADD, CMD input-only pins)	C_I	0.75	1.3	0.75	1.3	0.75	1.3	0.75	1.2	0.75	1.2	pF	2,3,4

NOTE 1 Although the DM, TDQS and TDQS# pins have different functions, the loading matches DQ and DQS

NOTE 2 This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147, Procedure for Measring Input Capacitance Using a Vector Network Analyzer (VNA), with V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} applied and all other pins floating (except the pin under test, CKE, RESET# and ODT as necessary). V_{DD}=V_{DDQ}=1.35V, VBIAS=V_{DD}/2 and on-die termination off.

NOTE 3 This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here

NOTE 4 C_I applies to ODT, CS#, CKE, A0-A15, BA0-BA2, RAS#, CAS#, WE#.

6 1.35 V DDR3L Output Driver DC Electrical Characteristics

Table 18 — Output Driver DC Electrical Characteristics, assuming R_{ZQ} = 240 Ω; entire operating temperature range; after proper ZQ calibration

RON_{Nom}	Resistor	V_{Out}	min	nom	max	Unit	Notes
34 Ω	RON_{34Pd}	$V_{OLdc} = 0.2 \times V_{DDQ}$	0.6	1.0	1.15	$R_{ZQ}/7$	1, 2, 3
		$V_{OMdc} = 0.5 \times V_{DDQ}$	0.9	1.0	1.15	$R_{ZQ}/7$	1, 2, 3
		$V_{OHdc} = 0.8 \times V_{DDQ}$	0.9	1.0	1.45	$R_{ZQ}/7$	1, 2, 3
	RON_{34Pu}	$V_{OLdc} = 0.2 \times V_{DDQ}$	0.9	1.0	1.45	$R_{ZQ}/7$	1, 2, 3
		$V_{OMdc} = 0.5 \times V_{DDQ}$	0.9	1.0	1.15	$R_{ZQ}/7$	1, 2, 3
		$V_{OHdc} = 0.8 \times V_{DDQ}$	0.6	1.0	1.15	$R_{ZQ}/7$	1, 2, 3
40 Ω	RON_{40Pd}	$V_{OLdc} = 0.2 \times V_{DDQ}$	0.6	1.0	1.15	$R_{ZQ}/6$	1, 2, 3
		$V_{OMdc} = 0.5 \times V_{DDQ}$	0.9	1.0	1.15	$R_{ZQ}/6$	1, 2, 3
		$V_{OHdc} = 0.8 \times V_{DDQ}$	0.9	1.0	1.45	$R_{ZQ}/6$	1, 2, 3
	RON_{40Pu}	$V_{OLdc} = 0.2 \times V_{DDQ}$	0.9	1.0	1.45	$R_{ZQ}/6$	1, 2, 3
		$V_{OMdc} = 0.5 \times V_{DDQ}$	0.9	1.0	1.15	$R_{ZQ}/6$	1, 2, 3
		$V_{OHdc} = 0.8 \times V_{DDQ}$	0.6	1.0	1.15	$R_{ZQ}/6$	1, 2, 3
Mismatch between pull-up and pull-down, MM_{PuPd}		$V_{OMdc} = 0.5 \times V_{DDQ}$	-10		+10	%	1, 2, 4

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

NOTE 2 The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$.

NOTE 3 Pull-down and pull-up output driver impedances are recommended to be calibrated at $0.5 \times V_{DDQ}$. Other calibration schemes may be used to achieve the linearity spec shown above, e.g., calibration at $0.2 \times V_{DDQ}$ and $0.8 \times V_{DDQ}$.

NOTE 4 Measurement definition for mismatch between pull-up and pull-down, MM_{PuPd}:
Measure RON_{Pu} and RON_{Pd}, both at $0.5 \times V_{DDQ}$:

$$MM_{PuPd} = \frac{RON_{Pu} - RON_{Pd}}{RON_{Nom}} \times 100$$

7 1.35 V DDR3L On-Die Termination (ODT) Levels and I-V Characteristics

Table 19 — ODT DC Electrical Characteristics, assuming R_{ZQ} = 240 Ω +/- 1% entire operating temperature range; after proper ZQ calibration

MR1 A9, A6, A2	*RTT*	Resistor	V_{Out}	min	nom	max	Unit	Notes
0, 1, 0	120 Ω	$RTT_{120Pd240}$	V_{OLdc} 0.2 × V_{DDQ}	0.6	1.00	1.15	R_{ZQ}	1, 2, 3, 4
			0.5 × V_{DDQ}	0.9	1.00	1.15	R_{ZQ}	1, 2, 3, 4
			V_{OHdc} 0.8 × V_{DDQ}	0.9	1.00	1.45	R_{ZQ}	1, 2, 3, 4
		$RTT_{120Pu240}$	V_{OLdc} 0.2 × V_{DDQ}	0.9	1.00	1.45	R_{ZQ}	1, 2, 3, 4
			0.5 × V_{DDQ}	0.9	1.00	1.15	R_{ZQ}	1, 2, 3, 4
			V_{OHdc} 0.8 × V_{DDQ}	0.6	1.00	1.15	R_{ZQ}	1, 2, 3, 4
		RTT_{120}	$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.00	1.65	R_{ZQ}/2	1, 2, 5
0, 0, 1	60 Ω	$RTT_{60Pd120}$	V_{OLdc} 0.2 × V_{DDQ}	0.6	1.00	1.15	R_{ZQ}/2	1, 2, 3, 4
			0.5 × V_{DDQ}	0.9	1.00	1.15	R_{ZQ}/2	1, 2, 3, 4
			V_{OHdc} 0.8 × V_{DDQ}	0.9	1.00	1.45	R_{ZQ}/2	1, 2, 3, 4
		$RTT_{60Pu120}$	V_{OLdc} 0.2 × V_{DDQ}	0.9	1.00	1.45	R_{ZQ}/2	1, 2, 3, 4
			0.5 × V_{DDQ}	0.9	1.00	1.15	R_{ZQ}/2	1, 2, 3, 4
			V_{OHdc} 0.8 × V_{DDQ}	0.6	1.00	1.15	R_{ZQ}/2	1, 2, 3, 4
		RTT_{60}	$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.00	1.65	R_{ZQ}/4	1, 2, 5
0, 1, 1	40 Ω	RTT_{40Pd80}	V_{OLdc} 0.2 × V_{DDQ}	0.6	1.00	1.15	R_{ZQ}/3	1, 2, 3, 4
			0.5 × V_{DDQ}	0.9	1.00	1.15	R_{ZQ}/3	1, 2, 3, 4
			V_{OHdc} 0.8 × V_{DDQ}	0.9	1.00	1.45	R_{ZQ}/3	1, 2, 3, 4
		RTT_{40Pu80}	V_{OLdc} 0.2 × V_{DDQ}	0.9	1.00	1.45	R_{ZQ}/3	1, 2, 3, 4
			0.5 × V_{DDQ}	0.9	1.00	1.15	R_{ZQ}/3	1, 2, 3, 4
			V_{OHdc} 0.8 × V_{DDQ}	0.6	1.00	1.15	R_{ZQ}/3	1, 2, 3, 4
		RTT_{40}	$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.00	1.65	R_{ZQ}/6	1, 2, 5

Table 19 — ODT DC Electrical Characteristics, assuming R_{ZQ} = 240 Ω +/- 1% entire operating temperature range; after proper ZQ calibration

MR1 A9, A6, A2	*RTT*	Resistor	V_{Out}	min	nom	max	Unit	Notes
1, 0, 1	30 Ω	RTT_{30Pd60}	V_{OLdc} 0.2 × V_{DDQ}	0.6	1.00	1.15	$R_{ZQ}/4$	1, 2, 3, 4
			0.5 × V_{DDQ}	0.9	1.00	1.15	$R_{ZQ}/4$	1, 2, 3, 4
			V_{OHdc} 0.8 × V_{DDQ}	0.9	1.00	1.45	$R_{ZQ}/4$	1, 2, 3, 4
		RTT_{30Pu60}	V_{OLdc} 0.2 × V_{DDQ}	0.9	1.00	1.45	$R_{ZQ}/4$	1, 2, 3, 4
			0.5 × V_{DDQ}	0.9	1.00	1.15	$R_{ZQ}/4$	1, 2, 3, 4
			V_{OHdc} 0.8 × V_{DDQ}	0.6	1.00	1.15	$R_{ZQ}/4$	1, 2, 3, 4
		RTT_{30}	$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.00	1.65	$R_{ZQ}/8$	1, 2, 5
1, 0, 0	20 Ω	RTT_{20Pd40}	V_{OLdc} 0.2 × V_{DDQ}	0.6	1.00	1.15	$R_{ZQ}/6$	1, 2, 3, 4
			0.5 × V_{DDQ}	0.9	1.00	1.15	$R_{ZQ}/6$	1, 2, 3, 4
			V_{OHdc} 0.8 × V_{DDQ}	0.9	1.00	1.45	$R_{ZQ}/6$	1, 2, 3, 4
		RTT_{20Pu40}	V_{OLdc} 0.2 × V_{DDQ}	0.9	1.00	1.45	$R_{ZQ}/6$	1, 2, 3, 4
			0.5 × V_{DDQ}	0.9	1.00	1.15	$R_{ZQ}/6$	1, 2, 3, 4
			V_{OHdc} 0.8 × V_{DDQ}	0.6	1.00	1.15	$R_{ZQ}/6$	1, 2, 3, 4
		RTT_{20}	$V_{IL(AC)}$ to $V_{IH(AC)}$	0.9	1.00	1.65	$R_{ZQ}/12$	1, 2, 5
Deviation of V_M w.r.t. $V_{DDQ}/2$, DV_M				-5		+5	%	1, 2, 5, 6

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

NOTE 2 The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$.

NOTE 3 Pull-down and pull-up ODT resistors are recommended to be calibrated at 0.5 × V_{DDQ}. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 × V_{DDQ} and 0.8 × V_{DDQ}.

NOTE 4 Not a specification requirement, but a design guide line.

NOTE 5 Measurement definition for *RTT*:

Apply $V_{IH(AC)}$ to pin under test and measure current $I(V_{IH(AC)})$, then apply $V_{IL(AC)}$ to pin under test and measure current $I(V_{IL(AC)})$ respectively.

$$RTT = \frac{V_{IH(ac)} - V_{IL(ac)}}{I(VIH(ac)) - I(VIL(ac))}$$

NOTE 6 Measurement definition for V_M and DV_M:

Measure voltage (V_M) at test pin (midpoint) with no load:

$$\Delta V_M = \left(\frac{2 \times V_M}{V_{DDQ}} - 1\right) \times 100$$

7 1.35 V DDR3L On-Die Termination (ODT) Levels and I-V Characteristics (cont'd)

Table 20 — Reference Settings for ODT Timing Measurements

Measured Parameter	RTT_Nom Setting	RTT_Wr Setting	V_{SW1} [V]	V_{SW2} [V]	Note
t_{AON}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AONPD}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AOF}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AOFPD}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{ADC}	$R_{ZQ}/12$	$R_{ZQ}/2$	0.20	0.25	

8 1.35 V DDR3L Single Ended Output Slew Rate

Table 21 — Output Slew Rate (single-ended)

Parameter	Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units
		min	max	min	max	min	max	min	max	min	max	
Single-ended Output Slew Rate	SRQse†	1.75	5[1)]	1.75	5[1)]	1.75	5[1)]	1.75	5[1)]	1.75	5[1)]	V/ns

† Description: SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), se: Single-ended Signals, For Ron = RZQ/7 setting

NOTE 1 In two cases, a maximum slew rate of 6 V/ns applies for a single DQ signal within a byte lane.
Case_1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e., they stay at either high or low).
Case_2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e., from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5 V/ns applies.

9 1.35 V Differential Output Slew Rate

Table 22 — Differential Output Slew Rate

Parameter	Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units
		min	max	min	max	min	max	min	max	min	max	
Differential Output Slew Rate	SRQdiff†	3.5	12	3.5	12	3.5	12	3.5	12	3.5	12	V/ns

† Description: SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), diff: Differential Signals
For Ron = RZQ/7 setting

10 1.35 V DDR3L AC and DC Logic Input Levels for Differential Signals

10.1 Differential swing requirements for clock (CK - CK#) and strobe (DQS - DQS#)

Table 23 — Differential AC and DC Input Levels

Symbol	Parameter	DDR3L-800, 1066, 1333, 1600 & 1866		Unit	Notes
		min	max		
V_{IHdiff}	Differential input high	+ 0.180	Note 3	V	1
V_{ILdiff}	Differential input logic low	Note 3	- 0.180	V	1
$V_{IHdiff(AC)}$	Differential input high AC	2 x (VIH(AC) - Vref)	Note 3	V	2
$V_{ILdiff(AC)}$	Differential input low AC	Note 3	2 x (VIL(AC) - Vref)	V	2

NOTE 1 Used to define a differential signal slew-rate.
NOTE 2 For CK - CK# use VIH/VIL(AC) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU , DQSU# use VIH/VIL(AC) of DQs and VREFDQ; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
NOTE 3 These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to JESD79-3E, 9.6 “Overshoot and Undershoot Specifications”.

Table 24 — Allowed time before ringback (tDVAC) for CK - CK# and DQS - DQS#

Slew Rate [V/ns]	DDR3L-800/1066/1333/1600				DDR3L-1866					
	tDVAC [ps] @ |VIH/Ldiff(AC)| = 320 mV		tDVAC [ps] @ |VIH/Ldiff(AC)| = 270 mV		tDVAC [ps] @ |VIH/Ldiff(AC)| = 270 mV		tDVAC [ps] @ |VIH/Ldiff(AC)| = 250 mV		tDVAC [ps] @ |VIH/Ldiff(AC)| = 260 mV	
	min	max	min	max	min	max	min	max	min	max
> 4.0	189	-	201	-	163		168		176	
4.0	189	-	201	-	163		168		176	
3.0	162	-	179	-	140		147		154	
2.0	109	-	134	-	95		105		111	
1.8	91	-	119	-	80		91		97	
1.6	69	-	100	-	62		74		78	
1.4	40	-	76	-	37		52		56	
1.2	NOTE	-	44	-	5		22		24	
1.0	NOTE	-	NOTE	-	NOTE		NOTE		NOTE	
< 1.0	NOTE	-	NOTE	-	NOTE		NOTE		NOTE	

NOTE Rising input signal shall become equal to or greater than VIH(AC) level and Falling input signal shall become equal to or less than VIL(AC) level.

11 Differential Input Cross point voltage

The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the midlevel between of V_{DD} and V_{SS}.

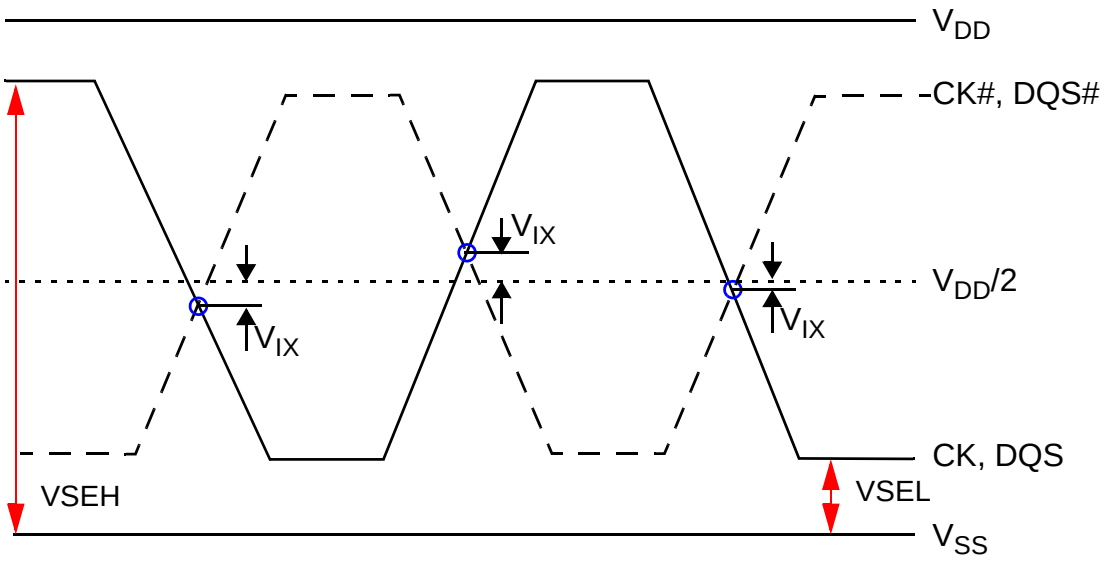

Figure 2 — V_{IX} Definition

Table 25 — Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	DDR3L-800, 1066, 1333, 1600 & 1866		Unit	Notes
		min	max		
V_{IX}	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK, CK#	- 150	150	mV	1
V_{IX}	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for DQS, DQS#	- 150	150	mV	
NOTE 1 The relation between Vix Min/Max and VSEL/VSEH should satisfy following. $(V_{DD}/2) + V_{IX}$ (min) - VSEL ≥ 25 mV VSEH - $((V_{DD}/2) + V_{IX}$ (max)) ≥ 25 mV					

12 DQS Output Cross point voltage

Table 26 — DDR3L-800/1066/1333 V_{OX}

Symbol	Parameter		DQS/DQS# Differential Slew Rate									Unit
			3.5V/ns	4V/ns	5V/ns	6V/ns	7V/ns	8V/ns	9V/ns	10V/ns	12V/ns	
V_{OX}	Deviation of DQS/DQS# output cross point voltage from 0.5 * VDDQ	max	+115	+130	+160	+195	+205	+205	+205	+205	+205	mV
		min	-115	-130	-160	-195	-205	-205	-205	-205	-205	mV

NOTE 1 Measured using an effective test load of 25 Ω to 0.5*V_{DDQ} at each of the differential outputs.
NOTE 2 For a differential slew rate in between the listed values, the V_{OX} value may be obtained by linear interploation.
NOTE 3 Refer to Figure Y for reference drawing, DQS/DQS# shown single-ended for measurement point.
NOTE 4 The DQS/DQS# pins under test are not required to be able to drive each of the slew rates listed in the table; the pins under test will provide one V_{OX} value when tested with specified test condition. The DQS and DQS# differential slewrate when measuring V_{OX} determines which V_{OX} limits to use.

Table 27 — DDR3L-1600/1866 V_{OX}

Symbol	Parameter		DQS/DQS# Differential Slew Rate									Unit
			3.5V/ns	4V/ns	5V/ns	6V/ns	7V/ns	8V/ns	9V/ns	10V/ns	12V/ns	
V_{OX}	Deviation of DQS/DQS# output cross point voltage from 0.5 * VDDQ	Max	+90	+105	+130	+155	+180	+205	+205	+205	+205	mV
		Min	-90	-105	-130	-155	-180	-205	-205	-205	-205	mV

NOTE 1 Measured using an effective test load of 25 Ω to 0.5*V_{DDQ} at each of the differential outputs.
NOTE 2 For a differential slew rate in between the listed values, the V_{OX} value may be obtained by linear interploation.
NOTE 3 Refer to Figure Y for reference drawing, DQS/DQS# shown single-ended for measurement point.
NOTE 4 The DQS/DQS# pins under test are not required to be able to drive each of the slew rates listed in the table; the pins under test will provide one V_{OX} value when tested with specified test condition. The DQS and DQS# differential slewrate when measuring V_{OX} determines which V_{OX} limits to use.

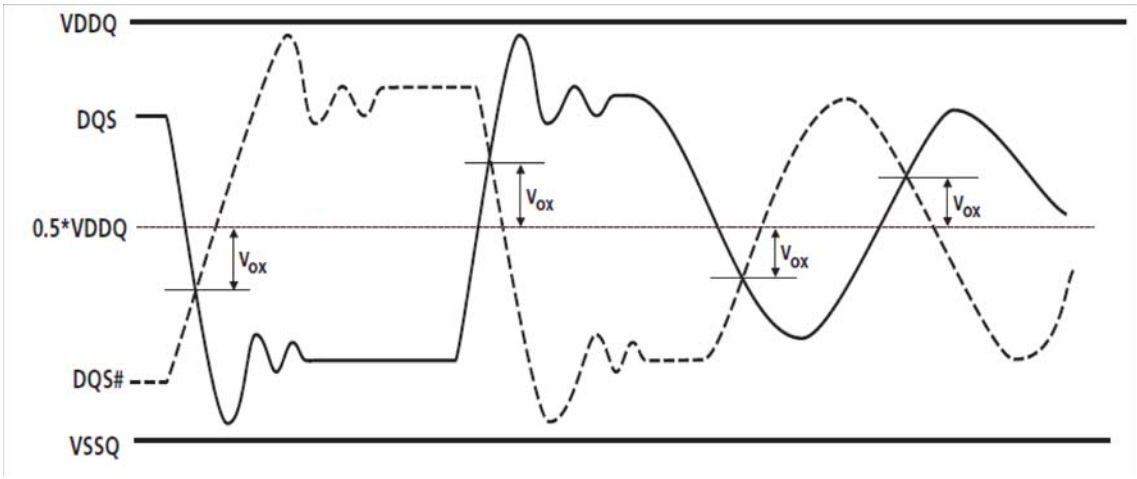

Figure 3 — Definition of Output cross point voltage for DQS and DQS#

Annex A (Informative) Differences between JESD79-3-1A.01 and JESD79-3-1A

This annex briefly describes most of the changes made to entries that appear in this standard, JESD79-3-1A.01, compared to its predecessor, JESD79-3-1A (January 2013).

Item	Description of change
Table 5	For VIH.DQ(AC130) and VIL.DQ(AC130), these items were added to the table at time of ballot without min/max for DDR3L-800, DDR3L-1066, DDR3L-1333, and DRDR3L-1600, min/max values were removed.
Table 7	For tIS(base) AC125, this item was added to the table at time of ballot without values for DDR3L-800, DDR3L-1066, DDR3L-1333, and DRDR3L-1600, values were removed.

A.1 Differences between JESD79-3-1A, compared to its predecessor, JESD79-3-1 (July 2010)

Item	Description of change
Throughout	Document updated to include DDR3L-1866
Table 10	Table 10 renumbered to Table 11, new Table 10 added
Tables	Table 11, Table 12, and Table 13 renumbered, now Table 12, Table 13, and Table 14
Table 14	Table 14 renumbered to Table 16, new Table 15 added
Tables	Table 15, Table 16, Table 17, Table 18, Table 19, Table 20, Table 21, Table 22, and Table 23, renumbered, now Table 17, Table 18, Table 19, Table 20, Table 21, Table 22, Table 23, Table 24, and Table 25
Table 11[10]	The min values have been incorporated [previously TBD]
Clause 4.2	New paragraph and example added
Table 16[14]	The min values have been incorporated [previously TBD]
Table 17[15]	The min values for DDR3L-800/1066/1333 (C_{IO}) changed from 1.5 to 1.4
Table 17[15]	The min and max value for DDR3L-1600 (C_{IO}) changed from 1.5 to 1.4 (min) and 2.3 to 2.2 (max). The max value for DDR3L-1600 (C_I) changed from 1.3 to 1.2.
Clause 12	This clause is new(Table 26, Table 27, and Figure 3)

Standard Improvement Form

JEDEC _____

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC
Attn: Publications Department
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

Fax: 703.907.7583

1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

Address: _____

City/State/Zip: _____ Date: _____


JEDEC