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# IEEE Standard for Ethernet

## Amendment 1: Physical Layer Specifications and Management Parameters for 100 Mb/s Operation over a Single Balanced Twisted Pair Cable (100BASE-T1)

IEEE Computer Society

Sponsored by the
LAN/MAN Standards Committee

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3 Park Avenue
New York, NY 10016-5997
USA

**IEEE Std 802.3bw™-2015**
(Amendment to
IEEE Std 802.3™-2015)

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**LAN/MAN Standards Committee**
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Approved 26 October 2015

**IEEE-SA Standards Board**

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**Abstract:** The 100BASE-T1 Physical Layer (PHY) specifications and management parameters for point-to-point full duplex 100 Mb/s operation over single twisted pair balanced cabling is defined in this amendment.

This specification provides fully functional and electrical specifications for the type 100BASE-T1 PHY. This specification also specifies the baseband medium used with 100BASE-T1.

**Keywords:** 100BASE-T1; copper; Ethernet; IEEE 802.3bw™; MASTER-SLAVE; Medium Dependent Interface; Physical Coding Sublayer; physical layer; Physical Medium Attachment

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# Introduction

This introduction is not part of IEEE Std 802.3bw™-2015, IEEE Standard for Ethernet—Amendment 1: Physical Layer Specifications and Management Parameters for 100 Mb/s Operation over a Single Balanced Twisted Pair

IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added functionality or provided maintenance updates to the specifications and text included in the standard. Each IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010).

The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and Xerox in 1980. Ethernet at 10 Mb/s was approved as an IEEE standard by the IEEE Standards Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC protocol was added in 1997.

Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. This is most common for projects adding higher speeds of operation or new protocols. For example, IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z added 1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae added 10 Gb/s operation (also called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are superseded by IEEE Std 802.3-2012 and are not maintained as separate documents.

At the date of IEEE Std 802.3-2015 publication, IEEE Std 802.3 is composed of the following documents:

IEEE Std 802.3-2012

Section One—Includes Clause 1 through Clause 20 and Annex A through Annex H and Annex 4A. Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service interfaces used for all speeds of operation.

Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33E. Section Two includes management attributes for multiple protocols and speed of operation as well as specifications for providing power over twisted pair cabling for multiple operational speeds. It also includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer specifications.

Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical Layer specifications.

Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer specifications.

Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines

services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical backplanes at speeds of 1000 Mb/s and 10 Gb/s.

Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 through Clause 95 and associated annexes includes general information on 40 Gb/s and 100 Gb/s operation as well the 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet support for time synchronization protocols.

A companion document IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

IEEE Std 802.3bw™-2015

This amendment includes changes to IEEE Std 802.3-2015 and adds Clause 96. This amendment adds 100 Mb/s Physical Layer (PHY) specifications and management parameters for operation on a single balanced twisted-pair copper cable.

A companion document IEEE Std 802.3.1 describes Ethernet management information base (MIB) modules for use with the Simple Network Management Protocol (SNMP). IEEE Std 802.3.1 is updated to add management capability for enhancements to IEEE Std 802.3 after approval of the enhancements.

IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the next few years as amendments to this standard.

# Contents

# IEEE Standard for Ethernet

## Amendment 1: Physical Layer Specifications and Management Parameters for 100 Mb/s Operation over a Single Balanced Twisted Pair Cable (100BASE-T1)



NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard.[1]

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are highlighted in green.

[1]Notes in text, tables, and figures of a standard are given for information only and do not contain requirements needed to implement this standard.

# 1. Introduction

## 1.3 Normative references

***Insert the following references in alphanumerical order:***

ASTM D4728, Standard Test Method for Random Vibration Testing of Shipping Containers.[2]

CISPR 25 Edition 3.0 2008-03, Vehicles, boats and internal combustion engines—Radio disturbance characteristics—Limits and methods of measurement for the protection of on-board receivers.[3]

IEC 60068-2-1/27/30/38/52/64/78, Environmental testing.[4]

IEC 61000-4-2, Electromagnetic compatibility (EMC)—Part 4-2: Testing and measurement techniques—Electrostatic discharge immunity test.

IEC 61000-4-3, Electromagnetic compatibility (EMC)—Part 4-3: Testing and measurement techniques—Radiated, radio-frequency, electromagnetic field immunity test.

IEC 61000-4-21, Electromagnetic compatibility (EMC)—Part 4-21: Testing and measurement techniques—Reverberation chamber test methods.

IEC 61967-1, Integrated circuits—Measurement of electromagnetic emissions, 150 kHz to 1 GHz—Part 1 : General conditions and definitions.

IEC 61967-4, Integrated circuits—Measurement of electromagnetic emissions, 150 kHz to 1 GHz—Part 4: Measurement of conducted emissions—1 Ω/150 Ω direct coupling method.

IEC 62132-1, Integrated circuits—Measurement of electromagnetic immunity, 150 kHz to 1 GHz—Part 1: General conditions and definitions.

IEC 62132-4, Integrated circuits—Measurements of electromagnetic immunity 150 kHz to 1 GHz—Part 4: Direct RF power injection method.

IEC 62215-3, Integrated circuits—Measurement of impulse immunity—Part 3: Non-synchronous transient injection method.

ISO 7637-2:2008, Road vehicles—Electrical disturbances from conduction and coupling—Part 2: Electrical transient conduction along supply lines only.

ISO 7637-3:2007, Road vehicles—Electrical disturbances from conduction and coupling—Part 3: Electrical transient transmission by capacitive and inductive coupling via lines other than supply lines.

ISO 8820-1:2014, Road vehicles—Fuse-links - Part 1: Definitions and general test requirements.

ISO 10605:2008, Road vehicles—Test methods for electrical disturbances from electrostatic discharge.

[2]ASTM publications are available from the American Society for Testing and Materials (http://www.astm.org/).
[3]CISPR documents are available from the International Electrotechnical Commission (http://www.iec.ch/). They are also available in the United States from the American National Standards Institute (http://www.ansi.org/).
[4]IEC publications are available from the International Electrotechnical Commission (http://www.iec.ch/). IEC publications are also available in the United States from the American National Standards Institute (http://www.ansi.org/).

ISO 11452, Road vehicles—Component test methods for electrical disturbances from narrowband radiated electromagnetic energy.

ISO 12103-1:1997, Road vehicles—Test dust for filter evaluation—Part 1: Arizona test dust.

ISO 16750-1:2006, Road vehicles—Environmental conditions and testing for electrical and electronic equipment—Part 1: General.

ISO 16750-2:2012, Road vehicles—Environmental conditions and testing for electrical and electronic equipment—Part 2: Electrical loads.

ISO 16750-3:2012, Road vehicles—Environmental conditions and testing for electrical and electronic equipment—Part 3: Mechanical loads.

ISO 16750-4:2010, Road vehicles—Environmental conditions and testing for electrical and electronic equipment—Part 4: Climatic loads.

ISO 16750-5: 2010, Road vehicles—Environmental conditions and testing for electrical and electronic equipment - Part 5: Chemical loads.

ISO 20653:2013, Road vehicles—Degrees of protection (IP code)—Protection of electrical equipment against foreign objects, water and access.

ISO 26262, Road vehicles—Functional safety.

## 1.4 Definitions

***Change the following existing definitions:***

**1.4.150 code-group:** For IEEE 802.3, a set of encoded symbols representing encoded data or control information. For 100BASE-T4, a set of six ternary symbols that, when representing data, conveys an octet. For 100BASE-TX and 100BASE-FX, a set of five code-bits that, when representing data, conveys a nibble. For 100BASE-T2, a pair of PAM5×5 symbols that, when representing data, conveys a nibble. For 1000BASE-X, a set of ten bits that, when representing data, conveys an octet. For 1000BASE-T, a vector of four 8B1Q4 coded quinary symbols that, when representing data, conveys an octet. For 100BASE-T1, a set of ternary symbols that, when representing data, conveys three bits, as defined in 96.3. (See IEEE Std 802.3, Clause 23, Clause 24, Clause 32, Clause 36, ~~and~~ Clause 40, and Clause 96.)

**1.4.166 Control mode:** In 1000BASE-T, the period of operation in which the PHY is transmitting code-groups that represent control information. The end of a frame is accompanied by a transition to the Control mode, which immediately follows the Data mode and precedes the Idle mode. This occurs when the GMII signal TX_EN is set FALSE. During this time, several control fields are transmitted as code-groups to complete a stream. These include two convolutional encoder reset code-groups, two End-of-Stream delimiter (ESD) code-groups and, possibly, carrier extend code-groups. In 100BASE-T1, the period of operation in which the PHY is transmitting code-groups that represent control information. The end of a frame is accompanied by a transition to the Control mode, which immediately follows the Data mode and precedes the Idle mode. This occurs when the MII signal TX_EN is set FALSE. During this time, several control fields are transmitted as code-groups to complete a stream. (See IEEE Std 802.3, Clause 40 and Clause 96.)

**1.4.172 Data mode:** In 1000BASE-T, the period of operation in which the PHY is transmitting code-groups that represent data. This mode is preceded by a start of a frame during which the GMII signal TX_EN is set TRUE for data transmission. This mode begins with transmission of two Start-of-Stream delimiter code-groups followed by code-groups encoded from the data octets arriving on TXD<7:0> via the GMII. In

100BASE-T1, the period of operation in which the PHY is transmitting code-groups that represent data. This mode is preceded by a start of a frame during which the MII signal TX_EN is set TRUE for data transmission. This mode begins with transmission of three Start-of-Stream delimiter code-groups followed by code-groups encoded from the data nibbles arriving on TXD<3:0> via the MII. (See IEEE Std 802.3, Clause 40 and Clause 96.)

**1.4.193 End-of-Stream Delimiter (ESD):** Within IEEE 802.3, a code-group pattern used to terminate a normal data transmission. For 100BASE-T4, the ESD is indicated by the transmission of five predefined ternary code-groups named eop1-5. For 100BASE-X, the ESD is indicated by the transmission of the code-group/T/R. For 100BASE-T2, the ESD is indicated by two consecutive pairs of predefined PAM5×5 symbols (see Table 32–15), which are generated using unique Start-of-Stream Delimiter (SSD)/ESD coding rules. For 1000BASE-T, the ESD is indicated by two consecutive vectors of four quinary symbols as specified in Table 40–1. For 100BASE-T1, the ESD consists of three code-groups as defined in 96.3.3.3.5. (See IEEE Std 802.3, Clause 22, Clause 23, Clause 32, ~~and~~ Clause 40, and Clause 96.)

**1.4.326 Physical Coding Sublayer (PCS):** Within IEEE 802.3, a sublayer used in certain port types to couple the Media Independent Interface (MII), Gigabit Media Independent Interface (GMII) or 10 Gigabit Media Independent Interface (XGMII) and the Physical Medium Attachment (PMA). The PCS contains the functions to encode data bits for transmission via the PMA and to decode the received conditioned signal from the PMA. There are several PCS structures. (For example, See IEEE Std 802.3, Clause 23, Clause 24, Clause 32, Clause 36, Clause 40, Clause 48, Clause 49, ~~and~~ Clause 82, and Clause 96.)

**1.4.327 Physical Layer entity (PHY):** Within IEEE 802.3, the portion of the Physical Layer between the Medium Dependent Interface (MDI) and the Media Independent Interface (MII), Gigabit Media Independent Interface (GMII) or 10 Gigabit Media Independent Interface (XGMII), consisting of the Physical Coding Sublayer (PCS), the Physical Medium Attachment (PMA), and, if present, the WAN Interface Sublayer (WIS) and Physical Medium Dependent (PMD) sublayers. The PHY contains the functions that transmit, receive, and manage the encoded signals that are impressed on and recovered from the physical medium. (For example, See Clauses 23 to 26, Clause 32, Clause 36, Clause 40, Clauses 48 to 54, Clauses 58 to 63, Clause 65, Clause 66, ~~and~~ Clauses 82 to 89, and Clause 96.)

**1.4.328 Physical Medium Attachment (PMA) sublayer:** Within 802.3, that portion of the Physical Layer that contains the functions for transmission, reception, and (depending on the PHY) collision detection, clock recovery and skew alignment. (For example, See IEEE Std 802.3, Clauses 7, 12, 14, 16, 17, 18, 23, 24, 32, 36, 40, 51, 62, 63, 66, ~~and~~ 83, and Clause 96.)

**1.4.353 receiver training:** Within IEEE 802.3, a start-up routine in 100BASE-T2, ~~and~~ 1000BASE-T, and 100BASE-T1 used to acquire receiver parameters and synchronize the scramblers of two connected Physical Layers (PHYs).

**1.4.363 retraining:** Within IEEE 802.3, the process of re-acquiring receiver parameters and synchronizing the scramblers of two connected 100BASE-T2, ~~PHYs or~~ 1000BASE-T, or 100BASE-T1 PHYs. *See:* **receiver training, blind mode.**

**1.4.390 Start-of-Stream Delimiter (SSD):** Within IEEE 802.3, a pattern of defined codewords used to delineate the boundary of a data transmission sequence on the Physical Layer stream. The SSD is unique in that it may be recognized independent of previously defined code-group boundaries and it defines subsequent code-group boundaries for the stream it delimits. For 100BASE-T4, SSD is a pattern of three predefined sosb code-groups (one per wire pair) indicating the positions of the first data code-group on each wire pair. For 100BASE-X, SSD consists of the code-group sequence /J/K/. For 100BASE-T2, the SSD is indicated by two consecutive pairs of predefined PAM5×5 symbols (±2, ±2) (±2, 0) which are generated using unique SSD/ESD coding rules. For 1000BASE-T, the SSD is indicated by two consecutive vectors of four quinary symbols as specified in Table 40–1. For 100BASE-T1, the SSD consists of three code-groups, as defined in 96.3.3.3.5.

**1.4.393 symbol:** Within IEEE 802.3, the smallest unit of data transmission on the medium. Symbols are unique to the coding system employed. For example, 100BASE-T4 and 100BASE-T1 use ~~uses~~ ternary symbols; 10BASE-T uses Manchester symbols; 100BASE-X uses binary symbols or code-bits; 100BASE-T2 and 1000BASE-T uses quinary symbols. For 1000BASE-X PMDs operating at 1.25 GBd, a symbol corresponds to a code-bit after the 8B/10B encoding operation i.e. has the duration of 0.8 ns. For 10GBASE-R PMDs operating at 10.3125 GBd, a symbol corresponds to a code-bit after the 64B/66B encoding operation i.e. has the duration of approximately 0.097 ns.

**1.4.394 symbol period:** In 1000BASE-T, the time interval for transmission of one code-group. This is equivalent to 8 ns. In 100BASE-T1, this is equivalent to 15 ns with a code-group of 30 ns. (See IEEE Std 802.3, Clause 40 and Clause 96.)

**1.4.395 symbol rate (SR):** Within IEEE 802.3, the total number of symbols per second transferred to or from the Medium Dependent Interface (MDI) on a single wire pair. For 100BASE-T4, the symbol rate is 25 MBd; for 100BASE-X, the symbol rate is 125 MBd; for 100BASE-T2, the symbol rate is 25 MBd; for 1000BASE-T, the symbol rate is 125 MBd; for 100BASE-T1, the symbol rate is $66.66\overline{6}$ MBd.

**1.4.398 ternary symbol:** In 100BASE-T4 and 100BASE-T1, a ternary data element. A ternary symbol can have one of three values: –1, 0, or +1. (See IEEE Std 802.3, Clause 23 and Clause 96.)

***Insert the following new definition into the list after 1.4.16 100BASE-T:***

**1.4.16a 100BASE-T1**: IEEE 802.3 Physical Layer specification for a 100 Mb/s Ethernet full duplex local area network over a single balanced twisted-pair. (See IEEE Std 802.3, Clause 96.)

***Insert the following new definition into the list after 1.4.87 2 Event classification:***

**1.4.87a 4B/3B:** For IEEE 802.3, the data encoding technique used by 100BASE-T1 when converting 4-bit (4B) MII data with 25 MHz clock to 3-bit (3B) data with $33.33\overline{3}$ MHz clock. (See IEEE Std 802.3, 96.3.3.1.2.)

***Insert the following new definition into the list after 1.4.221 FOMAU:***

**1.4.221a FORCE mode:** FORCE mode is a PHY initialization procedure used for manual configuration of MASTER-SLAVE assignment to achieve link acquisition between two link partners. (See IEEE Std 802.3, 96.4.4.)

## 1.5 Abbreviations

***Insert the following new abbreviations into the list, in alphabetical order:***

| | |
|---|---|
| AFEXT | alien FEXT |
| ANEXT | alien NEXT |
| DPI | direct power injection |
| DUT | device under test |
| EMC | electromagnetic compatibility |
| LCL | longitudinal conversion loss Sdc11/Sdc22 |
| LCTL | longitudinal conversion transmission loss Sdc12/Sdc21 |
| PSAACRF | power sum alien attenuation to crosstalk ratio far-end |
| PSANEXT | power sum alien near-end crosstalk |
| RMS | root mean square |

| | |
|---|---|
| TCL | transverse conversion loss Scd11/Scd22 |
| TCTL | transverse conversion transmission loss Scd12/Scd21 |
| XTALK | crosstalk |

# 30. Management

## 30.3 Layer management for DTEs

### 30.3.2 PHY devicePHY device managed object class

#### 30.3.2.1 PHY device attributes

#### 30.3.2.1.2 aPhyType

***Insert the following new entry in APPROPRIATE SYNTAX after the entry for 100BASE-T2:***

APPROPRIATE SYNTAX:

...

| | |
|---|---|
| 100BASE-T1 | Clause 96 100 Mb/s PAM3 |

#### 30.3.2.1.3 aPhyTypeList

***Insert the following new entry in APPROPRIATE SYNTAX after the entry for 100BASE-T2:***

APPROPRIATE SYNTAX:

...

| | |
|---|---|
| 100BASE-T1 | Clause 96 100 Mb/s PAM3 |

## 30.5 Layer management for medium attachment units (MAUs)

### 30.5.1 MAU managed object class

#### 30.5.1.1 MAU attributes

#### 30.5.1.1.2 aMAUType

***Insert the following new entry in APPROPRIATE SYNTAX after the entry for 100BASE-T2FD:***

APPROPRIATE SYNTAX:

...

| | |
|---|---|
| 100BASE-T1 | Single balanced twisted-pair copper cabling PHY as specified in Clause 96 |

#### 30.5.1.1.4 aMediaAvailable

***Insert into the third paragraph in BEHAVIOUR DEFINED AS section of 30.5.1.1.4 after the second sentence as follows:***

BEHAVIOUR DEFINED AS:

For 100BASE-T1, a link_status of OK maps to the enumeration “available”. All other states of link_status map to the enumeration “not available”.

# 45. Management Data Input/Output (MDIO) Interface

## 45.2 MDIO Interface Registers

### 45.2.1 PMA/PMD registers

***Replace the reserved row for 1.17 through 1.29 in Table 45–3 with the following three rows (unchanged rows not shown):***

**Table 45–3—PMA/PMD registers**

| Register address | Register name | Subclause |
|---|---|---|
| 1.17 | Reserved | |
| 1.18 | BASE-T1 PMA/PMD extended ability | 45.2.1.14a |
| 1.19 through 1.29 | Reserved | |

***Change the identified reserved row in Table 45-3 and insert four new rows immediately above the changed row as follows (unchanged rows not shown):***

**Table 45–3—PMA/PMD registers**

| Register address | Register name | Subclause |
|---|---|---|
| 1.1809 through 1.2099 | Reserved | |
| 1.2100 | BASE-T1 PMA/PMD control | 45.2.1.131 |
| 1.2101 | Reserved | |
| 1.2102 | 100BASE-T1 PMA/PMD test control | 45.2.1.132 |
| 1.~~1809~~2103 through 1.32767 | Reserved | |

### 45.2.1.6 PMA/PMD control 2 register (Register 1.7)

***Replace indicated line in the 1.7.5:0 row of Table 45-7 with five new lines, as follows (unchanged lines not shown):***

**Table 45–7—PMA/PMD control 2 register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 1.7.5:0 | PMA/PMD type selection | 5 4 3 2 1 0<br>~~1 1 x x x x = reserved for future use~~<br>1 1 1 1 1 x = reserved for future use<br>1 1 1 1 0 1 = 100BASE-T1 PMA/PMD<br>1 1 1 1 0 0 = reserved for future use<br>1 1 1 0 x x = reserved for future use<br>1 1 0 x x x = reserved for future use | R/W |

[a]R/W = Read/Write

### 45.2.1.7.4 Transmit fault (1.8.11)

***Insert the following row below the header row of Table 45-9 (unchanged rows not shown):***

**Table 45–9—Transmit fault description location**

| PMA/PMD | Description location |
|---|---|
| 100BASE-T1 | 96.4.2 |

### 45.2.1.7.5 Receive fault (1.8.10)

***Insert the following row below the header row of Table 45-10 (unchanged rows not shown):***

**Table 45–10—Receive fault description location**

| PMA/PMD | Description location |
|---|---|
| 100BASE-T1 | 96.4.3 |

### 45.2.1.10 PMA/PMD extended ability register (Register 1.11)

***Change the reserved row in Table 45-14 and insert a new row immediately below the changed row as follows (unchanged rows not shown):***

**Table 45–14—PMA/PMD extended ability register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 1.11.15:~~11~~ 12 | Reserved | Value always 0 | RO |
| 1.11.11 | BASE-T1 extended abilities | 1 = PMA/PMD has BASE-T1 extended abilities listed in register 1.18<br>0 = PMA/PMD does not have BASE-T1 extended abilities | RO |

[a]RO = Read only

***Insert 45.2.1.10.a before 45.2.1.10.1 as follows:***

### 45.2.1.10.a BASE-T1 extended abilities (1.11.11)

When read as a one, bit 1.11.11 indicates that the PMA/PMD has BASE-T1 extended abilities listed in register 1.18. When read as a zero, bit 1.11.11 indicates that the PMA/PMD does not have BASE-T1 extended abilities.

***Insert 45.2.1.14a and Table 45-17a after 45.2.1.14 as follows:***

### 45.2.1.14a BASE-T1 PMA/PMD extended ability register (1.18)

The assignment of bits in the BASE-T1 PMA/PMD extended ability register is shown in Table 45–17a. All of the bits in the PMA/PMD extended ability register are read only; a write to the PMA/PMD extended ability register shall have no effect.

**Table 45–17a PMA/PMD extended ability register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 1.18.15:1 | Reserved | Value always 0 | RO |
| 1.18.0 | 100BASE-T1 ability | 1 = PMA/PMD is able to perform 100BASE-T1<br>0 = PMA/PMD is not able to perform 100BASE-T1 | RO |

[a]RO = Read only

***Insert the following new subclauses before 45.2.2:***

### 45.2.1.131 BASE-T1 PMA/PMD control register (Register 1.2100)

The assignment of bits in the BASE-T1 PMA/PMD control register is shown in Table 45–98a.

**Table 45–98a—BASE-T1 PMA/PMD control register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 1.2100.15 | MASTER-SLAVE manual config enable | Value always 1 | RO |
| 1.2100.14 | MASTER-SLAVE config value | 1 = Configure PHY as MASTER<br>0 = Configure PHY as SLAVE | R/W |
| 1.2100.13:4 | Reserved | Value always 0 | RO |
| 1.2100.3:0 | Type Selection | 3 2 1 0<br>1 x x x = Reserved for future use<br>0 1 x x = Reserved for future use<br>0 0 1 x = Reserved for future use<br>0 0 0 1 = Reserved for future use<br>0 0 0 0 = 100BASE-T1 | R/W |

[a]RO = Read only, R/W = Read/Write

### 45.2.1.131.1 BASE-T1 MASTER-SLAVE manual config enable (1.2100.15)

Bit 1.2100.15 returns a one to indicate that MASTER or SLAVE configuration is set manually.

#### 45.2.1.131.2 BASE-T1 MASTER-SLAVE config value (1.2100.14)

Bit 1.2100.14 is used to select MASTER or SLAVE operation when MASTER-SLAVE manual config enable bit 1.2100.15 is set to one. If bit 1.2100.14 is set to one the PHY shall operate as MASTER. If bit 1.2100.14 is set to zero the PHY shall operate as SLAVE.

#### 45.2.1.131.3 BASE-T1 type selection (1.2100.3:0)

Bits 1.2100.3:0 are used to set the mode of operation. When these bits are set to 0000, the mode of operation is 100BASE-T1.

#### 45.2.1.132 100BASE-T1 PMA/PMD test control register (Register 1.2102)

The assignment of bits in the 100BASE-T1 PMA/PMD test control register is shown in Table 45–98b.

**Table 45–98b—100BASE-T1 PMA/PMD test control register bit definitions**

| Bit(s) | Name | Description | R/W[a] |
|---|---|---|---|
| 1.2102.15:13 | 100BASE-T1 test mode control | 15 14 13<br>1 1 1 = Reserved<br>1 1 0 = Reserved<br>1 0 1 = Test mode 5<br>1 0 0 = Test mode 4<br>0 1 1 = Reserved<br>0 1 0 = Test mode 2<br>0 0 1 = Test mode 1<br>0 0 0 = Normal operation | R/W |
| 1.2102.12:0 | Reserved | Value always 0 | RO |

[a]RO = Read only, R/W = Read/Write

#### 45.2.1.132.1 100BASE-T1 test mode control (1.2102.15:13)

100BASE-T1 test mode control operations are selected using bits 1.2102.15:13. The default value for bits 1.2102.15:13 is 000.

### 45.2.3 PCS registers

#### 45.2.3.1 PCS control 1 register (Register 3.0)

#### 45.2.3.1.2 Loopback (3.0.14)

***Change 45.2.3.1.2 Loopback (3.0.14) as follows:***

When the 100BASE-T1, 10GBASE-T, or the 10GBASE-R mode of operation is selected for the PCS using the PCS type selection field (3.7.1:0), the PCS shall be placed in a loopback mode of operation when bit 3.0.14 is set to a one. When bit 3.0.14 is set to a one, the 100BASE-T1, 10GBASE-R, or 10GBASE-T PCS shall accept data on the transmit path and return it on the receive path. The specific behavior of the 100BASE-T1 PCS during loopback is specified in 96.3.5. The specific behavior of the 10GBASE-R PCS during loopback is specified in 49.2. The specific behavior for the 10GBASE-T PCS during loopback is specified in 55.3.6.3. For all other port types, the PCS loopback functionality is not applicable and writes to this bit shall be ignored and reads from this bit shall return a value of zero.

## 45.5 Protocol implementation conformance statement (PICS) proforma for Clause 45, MDIO interface

### 45.5.3 PICS proforma tables for the Management Data Input Output (MDIO) interface

#### 45.5.3.2 PMA/PMD MMD options

***Insert the following row at the end of table 45.5.3.2 PMA/PMD MMD options:***

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| *BTC | Implementation of BASE-T1 PMA/PMD | 45.2.1.131.2 | | PMA:O | Yes [ ]<br>No [ ]<br>N/A[ ] |

#### 45.5.3.3 PMA/PMD management functions

***Insert the following row at the end of table 45.5.3.3 PMA/PMD management functions:***

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| MM126 | Writes to the BASE-T1 PMA/PMD extended ability register have no effect | 45.2.1.14a | | PMA:M | Yes [ ]<br>N/A[ ] |
| MM127 | BASE-T1 MASTER config | 45.2.1.131.2 | PHY operates as MASTER when bit 1.2100.14 is set to one | BTC:M | Yes [ ]<br>N/A[ ] |
| MM128 | BASE-T1 SLAVE config | 45.2.1.131.2 | PHY operates as SLAVE when bit 1.2100.14 is set to zero | BTC:M | Yes [ ]<br>N/A[ ] |

#### 45.5.3.7 PCS management functions

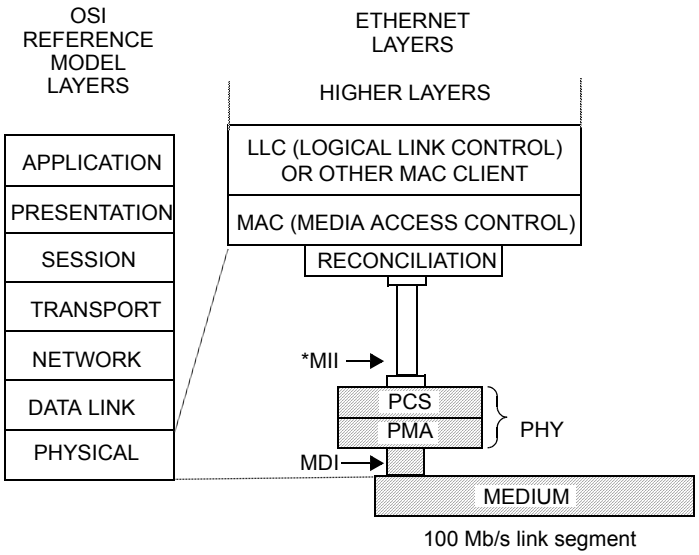
***Change the identified rows in table 45.5.3.7 (unchanged rows not shown):***

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| RM15 | Writes to loopback bit are ignored ~~when operating at 10 Gb/s~~ with port type selections other than 100BASE-T1, 10GBASE-R, or 10GBASE-T | 45.2.3.1.2 | | PCS:M | Yes [ ]<br>N/A[ ] |
| RM16 | Loopback bit returns zero ~~when operating at 10 Gb/s~~ with port type selections other than 100BASE-T1, 10GBASE-R, or 10GBASE-T | 45.2.3.1.2 | | PCS:M | Yes [ ]<br>N/A[ ] |

# 96. Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T1

## 96.1 Overview

The 100BASE-T1 Physical Layer supports standard media access controller (MAC) interfaces via the MII defined in Clause 22 with the exception of the MII Management interface defined in 22.2.4. The 100BASE-T1 management functions are optionally accessible through the management interface defined in Clause 45. Each copper port supports a single balanced twisted-pair link segment connection up to 15 m in length. 100BASE-T1 provides data rate of 100 Mb/s at the MAC interface over a single balanced twisted-pair cable as defined in 96.7. The architectural positioning of the 100BASE-T1 Physical Layer is depicted in Figure 96–1.




MDI = MEDIUM DEPENDENT INTERFACE
MII = MEDIA INDEPENDENT INTERFACE
* Physical instantiation of MII is optional.
PCS = PHYSICAL CODING SUBLAYER
PMA = PHYSICAL MEDIUM ATTACHMENT
PHY = PHYSICAL LAYER DEVICE
PMD = PHYSICAL MEDIUM DEPENDENT

**Figure 96–1—Architectural positioning of 100BASE-T1**

This clause defines the PCS and PMA sublayers of the 100BASE-T1 PHY. A functional block diagram of the 100BASE-T1 PHY is provided in Figure 96–3.

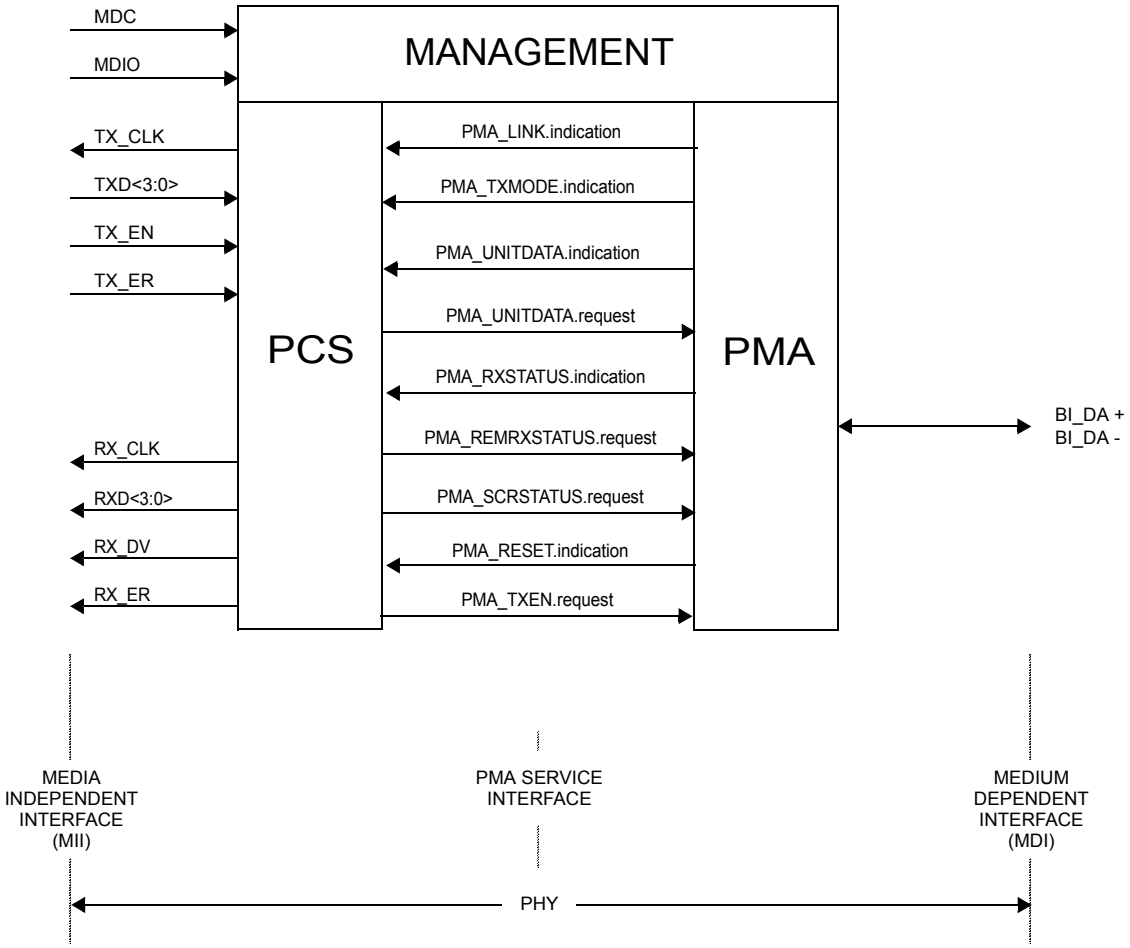



**Figure 96–2—100BASE-T1 PHY interfaces**

### 96.1.1 100BASE-T1 architecture

The 100BASE-T1 PHY operates using full-duplex communications (using echo cancellation) over a single balanced twisted-pair. This PHY uses ternary signaling and interfaces to the Clause 22 MII.

The 100BASE-T1 PHY interfaces to a Clause 22 MII. The PMA is similar to Clause 40. The PCS (specified in 96.3) is different from the PCS defined in Clause 40.

PMA functionality is defined in 96.4 with reference to Clause 40. The PMA functions are illustrated in Figure 96–3.

The 100BASE-T1 PHY leverages 1000BASE-T and 100BASE-TX PHY technologies in operation at 100 Mb/s, and introduces new PCS, PMA, and other modifications in support of the 100BASE-T1 PHY.

The specification features that enable operation over a single balanced twisted-pair are as follows:

a) Full-duplex communication with Ethernet MAC compatibility.

b) Adopt Pulse Amplitude Modulation 3 (PAM3) to provide trade-off between bandwidth and EMI performance.

#### 96.1.1.1 Physical Coding Sublayer (PCS)

The 100BASE-T1 PCS transmits/receives signals to/from a Media Independent Interface (MII) as described in Clause 22, to/from signals on a 100BASE-T1 PMA, which supports a single balanced twisted-pair medium.

#### 96.1.1.2 Physical Medium Attachment (PMA) sublayer

The 100BASE-T1 PMA transmits/receives signals to/from the PCS onto the single balanced twisted-pair cable medium and supports the link management and the 100BASE-T1 PHY Control function. The PMA provides full duplex communications at $66.66\overline{6}$ MBd over a single balanced twisted-pair cable up to 15 m in length.

#### 96.1.1.3 Signaling

100BASE-T1 signaling is performed by the PCS generating continuous code-group sequences that the PMA transmits over the single balanced twisted-pair. The signaling scheme achieves a number of objectives including the following:

a) Algorithm mapping and inverse mapping from nibble data to ternary symbols and back.
b) Uncorrelated symbols in the transmitted symbol stream.
c) No correlation between symbol streams traveling both directions.
d) Ability to rapidly or immediately determine if a symbol stream represents data or idle.
e) Robust delimiters for Start-of-Stream delimiter (SSD), End-of-Stream delimiter (ESD), and other control signals.
f) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.

### 96.1.2 Conventions in this clause

The body of this clause contains state diagrams, including definitions of variables, constants, and functions. Should there be a discrepancy between a state diagram and a descriptive text, the state diagram prevails.

#### 96.1.2.1 State Diagram Notation

The notation used in the state diagrams follows the conventions of 21.5.

#### 96.1.2.2 State Diagram Timer specifications

All timers operate in the manner described in 40.4.5.2.

#### 96.1.2.3 Service specifications

The method and notation used in the service specification follows the conventions of 1.2.2.

## 96.2 100BASE-T1 service primitives and interfaces

The 100BASE-T1 PHY shall use the service primitives and interfaces in 40.2, with exception of the following clarifications and differences noted in this section, in support of 100 Mb/s operations over a single

balanced twisted-pair channel. Figure 96–2 shows the relationship of the service primitives and interfaces used by the 100BASE-T1 PHY.

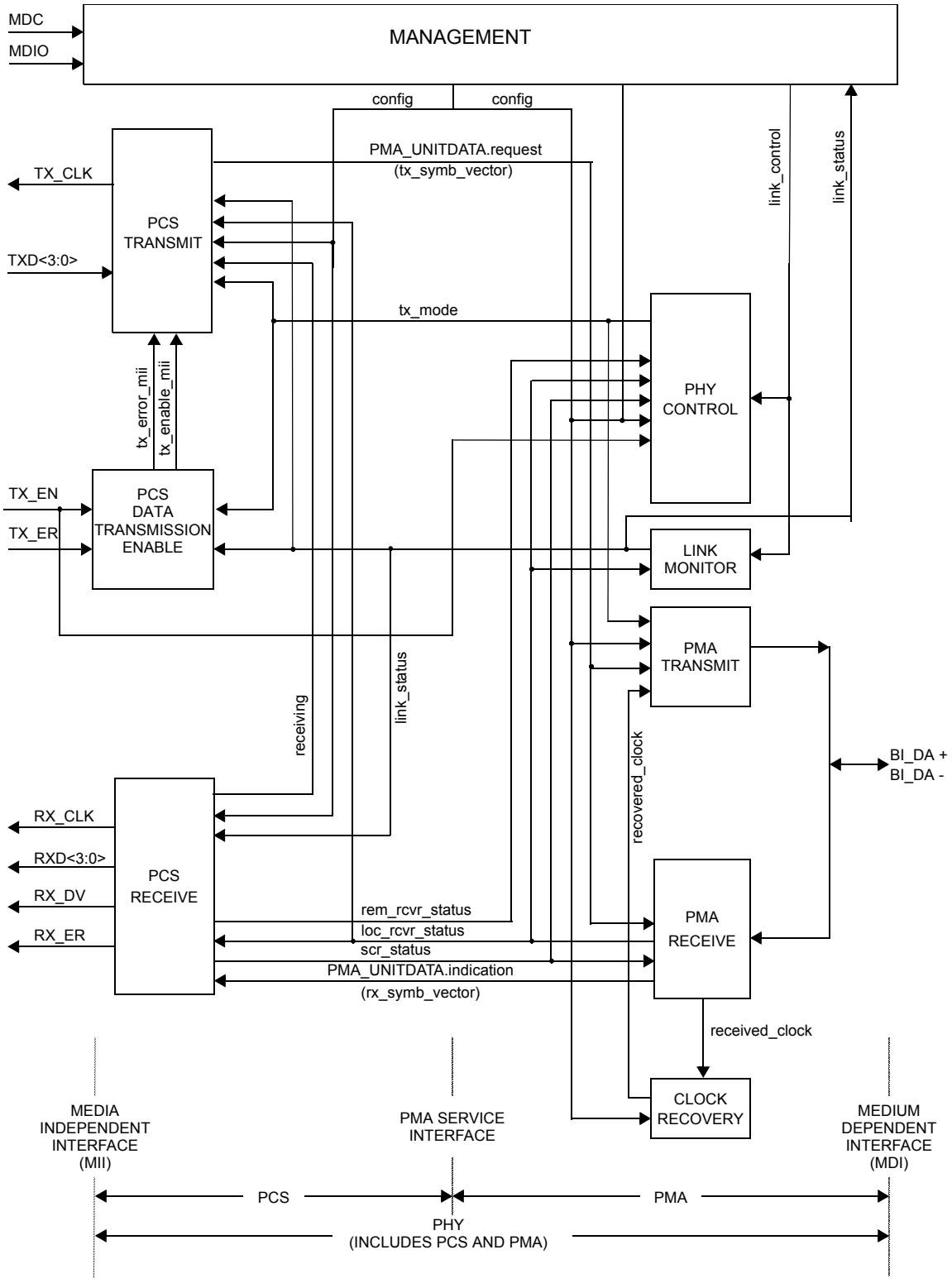
Differences from the 40.2 service interface:

a) The 100BASE-T1 PHY uses the Media Independent Interface (MII) as specified in Clause 22.
b) The 100BASE-T1 PHY does not use 40.2 support of LPI (Low Power Idle) related functions.
c) The 100BASE-T1 PHY MASTER-SLAVE relationship is set by FORCE mode (see 96.4.4).

### 96.2.1 PMA service interface

As shown in Figure 96–2, 100BASE-T1 uses the following service primitives to exchange symbol vectors, status indications, and control signals across the PMA service interface:

PMA_LINK.indications (link_status)
PMA_TXMODE.indication (tx_mode)
PMA_UNITDATA.request (tx_symb_vector)
PMA_UNITDATA.indication (rx_symb_vector)
PMA_SCRSTATUS.request (scr_status)
PMA_RXSTATUS.indication (loc_rcvr_status)
PMA_REMRXSTATUS.request (rem_rcvr_status)
PMA_TXEN.request (TX_EN)




NOTE—The recovered_clock arc is shown to indicate delivery of the received clock signal back to the PMA TRANSMIT for loop timing

**Figure 96–3—Functional block diagram**

### 96.2.2 PMA_LINK.indication

This primitive is generated by the PMA to indicate the status of the underlying medium as specified in 96.4.5. This primitive informs the PCS about the status of the underlying link.

#### 96.2.2.1 Semantics of the primitive

PMA_LINK.indication (link_status)

The link_status parameter can take on one of two values: FAIL or OK

| | |
|---|---|
| FAIL | No valid link established |
| OK | The Link Monitor function indicates that a valid 100BASE-T1 link is established. Reliable reception of signals transmitted from the remote PHY is possible. |

#### 96.2.2.2 When generated

The PMA generates this primitive continuously to indicate the value of the link_status in compliance with the state diagram given in 96.4.5.

#### 96.2.2.3 Effect of receipt

The effect of receipt of this primitive is specified in 96.4.5.

### 96.2.3 PMA_TXMODE.indication

The 100BASE-T1 transmitter sends code-groups that represent an MII data stream, control information, idles, or zeros.

#### 96.2.3.1 Semantics of the primitive

PMA_TXMODE.indication (tx_mode)

PMA_TXMODE.indication specifies to PCS Transmit via the parameter tx_mode what sequence of code-groups the PCS should be transmitting. The parameter tx_mode can take on one of the following three values:

| | |
|---|---|
| SEND_N | This value is continuously asserted when transmission of sequences of code-groups representing a MII data stream (data mode), control mode or idle mode is to take place. |
| SEND_I | This value is continuously asserted in case transmission of sequences of code-groups representing the idle mode is to take place. |
| SEND_Z | This value is continuously asserted in case transmission of zeros is required. |

#### 96.2.3.2 When generated

The PMA PHY Control function generates PMA_TXMODE.indication messages continuously.

#### 96.2.3.3 Effect of receipt

Upon receipt of this primitive, the PCS performs its Transmit function as described in 96.3.3.

### 96.2.4 PMA_UNITDATA.request

This primitive defines the transfer of code-groups in the form of the tx_symb_vector parameter from the PCS to the PMA. The code-groups are obtained in the PCS Transmit function using the encoding rules defined in 96.3.3 to represent MII data streams, an idle mode, or other sequences.

#### 96.2.4.1 Semantics of the primitive

PMA_UNITDATA.request (tx_symb_vector)

During transmission, the PMA_UNITDATA.request simultaneously conveys to the PMA via the parameter tx_symb_vector the value of the symbols to be sent over the transmit pair BI_DA. The tx_symb_vector parameter takes on the form:

SYMB_1D: A vector of one ternary symbol for a single transmit pair BI_DA. Each ternary symbol may take on one of the values {–1, 0, or +1}.

The ternary symbols that are elements of tx_symb_vector are called tx_symb_vector[BI_DA].

#### 96.2.4.2 When generated

The PCS continuously generates PMA_UNITDATA.request (SYMB_1D) synchronously with every TX_TCLK cycle.

#### 96.2.4.3 Effect of receipt

Upon receipt of this primitive the PMA transmits on the MDI the signals corresponding to the indicated ternary symbols. The parameter tx_symb_vector is also used by the PMA Receive function to process the signals received on pair BI_DA.

### 96.2.5 PMA_UNITDATA.indication

This primitive defines the transfer of code-groups in the form of the rx_symb_vector parameter from the PMA to the PCS.

#### 96.2.5.1 Semantics of the primitive

PMA_UNITDATA.indication (rx_symb_vector)

During reception, the PMA_UNITDATA.indication simultaneously conveys to the PCS via the parameter rx_symb_vector the values of the symbols detected on the receive pair BI_DA. The rx_symb_vector parameter takes on the following form:

SYMB_1D A vector of ternary symbols for the receive pair BI_DA. Each ternary symbol may take on one of the values {–1, 0, or +1}.

The ternary symbols that are elements of rx_symb_vector are called rx_symb_vector[BI_DA].

#### 96.2.5.2 When generated

The PMA generates PMA_UNITDATA.indication (SYMB_1D) messages synchronously with signals received at the MDI. The nominal rate of the PMA_UNITDATA.indication primitive is $66.66\overline{6}$ MHz, as governed by the recovered clock.

#### 96.2.5.3 Effect of receipt

The effect of receipt of this primitive is unspecified.

### 96.2.6 PMA_SCRSTATUS.request

This primitive is generated by PCS Receive to communicate the status of the descrambler for the local PHY. The parameter scr_status conveys to the PMA Receive function the information that the descrambler has achieved synchronization.

#### 96.2.6.1 Semantics of the primitive

PMA_SCRSTATUS.request (scr_status)

The scr_status parameter can take on one of two values:

| | |
|---|---|
| OK | The descrambler has achieved synchronization. |
| NOT_OK | The descrambler is not synchronized. |

#### 96.2.6.2 When generated

PCS Receive generates PMA_SCRSTATUS.request messages continuously.

#### 96.2.6.3 Effect of receipt

The effect of receipt of this primitive is specified in 96.4.3 and 96.4.4.

### 96.2.7 PMA_RXSTATUS.indication

This primitive is generated by PMA Receive to indicate the status of the receive link at the local PHY. The parameter loc_rcvr_status conveys to the PCS Transmit, PCS Receive, PMA PHY Control function, and Link Monitor the information on whether the status of the overall receive link is satisfactory or not. Note that loc_rcvr_status is used by the PCS Receive decoding functions. The criterion for setting the parameter loc_rcvr_status is left to the implementor. It can be based, for example, on observing the mean-square error at the decision point of the receiver and detecting errors during reception of symbol streams that represent the idle mode.

#### 96.2.7.1 Semantics of the primitive

PMA_RXSTATUS.indication (loc_rcvr_status)

The loc_rcvr_status parameter can take on one of two values:

| | |
|---|---|
| OK | This value is asserted and remains true during reliable operation of the receive link for the local PHY. |
| NOT_OK | This value is asserted whenever operation of the link for the local PHY is unreliable. |

#### 96.2.7.2 When generated

PMA Receive generates PMA_RXSTATUS.indication messages continuously on the basis of signals received at the MDI.

#### 96.2.7.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 96–18, 96.4.4, and 96.4.5.

### 96.2.8 PMA_REMRXSTATUS.request

This primitive is generated by PCS Receive to indicate the status of the receive link at the remote PHY as communicated by the remote PHY via its encoding of its loc_rcvr_status parameter. The parameter rem_rcvr_status conveys to the PMA PHY Control function the information on whether reliable operation of the remote PHY is detected or not. The criterion for setting the parameter rem_rcvr_status is left to the implementor. It can be based, for example, on asserting rem_rcvr_status is NOT_OK until loc_rcvr_status is OK and then asserting the detected value of rem_rcvr_status after proper PCS receive decoding is achieved.

#### 96.2.8.1 Semantics of the primitive

PMA_REMRXSTATUS.request (rem_rcvr_status)

The rem_rcvr_status parameter can take on one of two values:

| | |
|---|---|
| OK | The receive link for the remote PHY is operating reliably. |
| NOT_OK | Reliable operation of the receive link for the remote PHY is not detected. |

#### 96.2.8.2 When generated

The PCS generates PMA_REMRXSTATUS.request messages continuously on the basis of signals received at the MDI.

#### 96.2.8.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 96–18.

### 96.2.9 PMA_RESET.indication

This primitive is used to pass the PMA Reset function to the PCS (pcs_reset=ON) when reset is enabled.

The PMA_RESET.indication primitive can take on one of two values:

| | |
|---|---|
| TRUE | Reset is enabled. |
| FALSE | Reset is not enabled. |

#### 96.2.9.1 When generated

This primitive is generated under the conditions described in 40.4.2.1.

#### 96.2.9.2 Effect of receipt

The effect of receipt of this primitive is specified in 40.4.2.1.

### 96.2.10 PMA_TXEN.request

This primitive indicates the presence of data on MII for transmission.

#### 96.2.10.1 Semantic of the primitive

PMA_TXEN.request

The TX_EN parameter can take on one of two values:

| | |
|---|---|
| TRUE | The data transmission on MII is enabled. |
| FALSE | The data transmission on MII is not enabled. |

#### 96.2.10.2 When generated

PCS generates the PMA_TXEN.request messages continuously based on TX_EN signal received from MII.

#### 96.2.10.3 Effect of receipt

The effect of receipt of this primitive is specified in Figure 96–18.

## 96.3 100BASE-T1 Physical Coding Sublayer (PCS) functions

The Physical Coding Sublayer (PCS) consists of PCS Reset, the PCS Data Transmission Enable, PCS Transmit, and PCS Receive functions as shown in Figure 96–4. The PCS Transmit function is explained in 96.3.3, and the PCS Receive function is explained in 96.3.4.

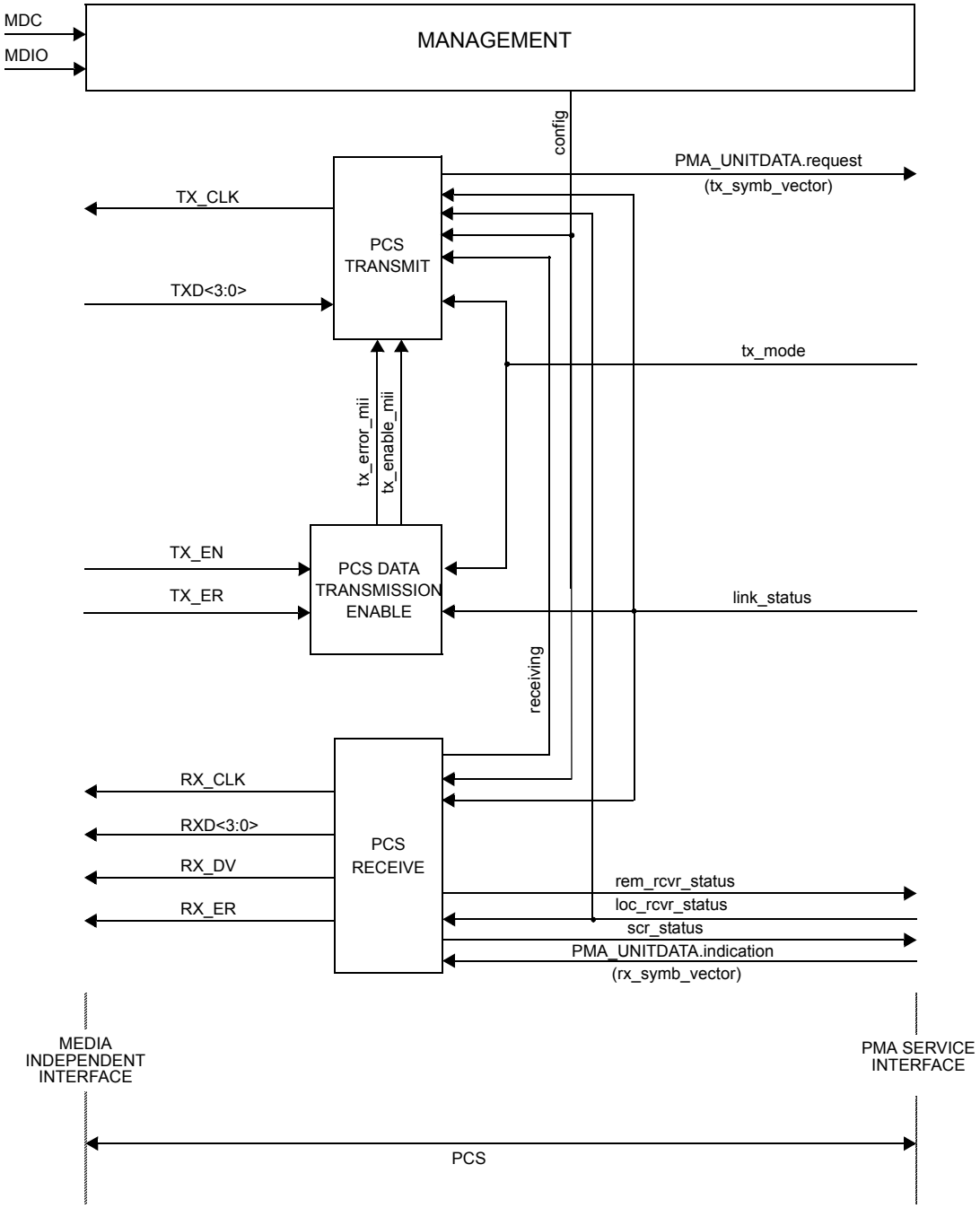



**Figure 96–4—PCS reference diagram**

### 96.3.1 PCS Reset function

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever one of the following conditions occur:

a) Power on (see 36.2.5.1.3).
b) The receipt of a request for reset from the management entity.

PCS Reset sets pcs_reset=ON while any of the above reset conditions hold true. All state diagrams take the open-ended pcs_reset branch upon execution of PCS Reset. The reference diagrams do not explicitly show the PCS Reset function.

### 96.3.2 PCS data transmission enabling

The PCS data transmission enabling function shall conform to the PCS data transmission enabling state diagram in Figure 96–5. When tx_mode is equal to SEND_N, the signals tx_enable_mii and tx_error_mii are equal to the value of the MII signals TX_EN and TX_ER respectively, otherwise tx_enable_mii and tx_error_mii are set to the value FALSE.

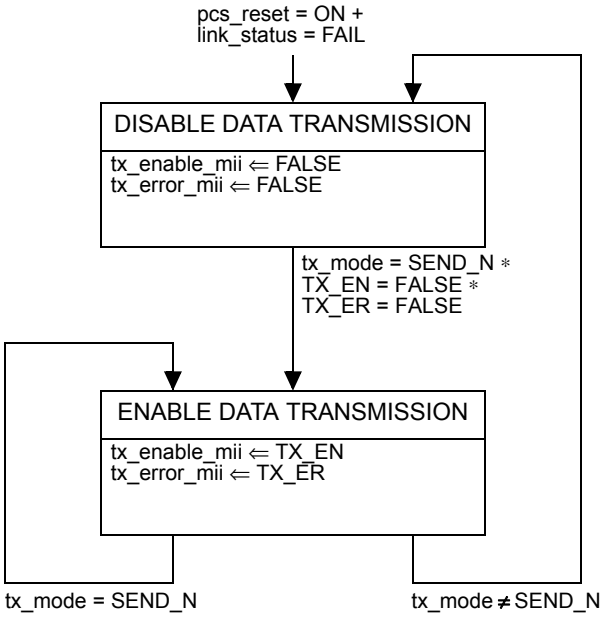



**Figure 96–5—PCS data transmission enabling state diagram**

#### 96.3.2.1 Variables

link_status
: The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive.
Values: OK or FAIL

pcs_reset
: The pcs_reset parameter set by the PCS Reset function.
Values: ON or OFF

tx_enable_mii
: The tx_enable_mii variable is generated in the PCS data transmission enabling state diagram as specified in Figure 96–5. When set to FALSE transmission is disabled, when set to TRUE transmission is enabled.
Values: TRUE or FALSE

tx_error_mii
The tx_error_mii variable is generated in the PCS data transmission enabling state diagram as specified in Figure 96–5.When this variable is set to FALSE it indicates a non-errored transmission, when set to TRUE it indicates an errored transmission.
Values: TRUE or FALSE

TX_EN
The TX_EN signal of the MII as specified in 22.2.2.3.

TX_ER
The TX_ER signal of the MII as specified in 22.2.2.5.

tx_mode
The tx_mode parameter set by the PMA PHY Control function and passed to the PCS via the PMA_TXMODE.indication primitive.
Values: SEND_Z, SEND_N, or SEND_I

### 96.3.3 PCS Transmit

#### 96.3.3.1 4B/3B conversion

The PCS performs a 4B/3B conversion of the nibbles received at the MII, creates the ternary symbols, and then sends the symbols to the PMA for further processing. It receives 4 bits at the MII using TX_CLK, and converts the stream of 4-bit words at 25 MBd to a stream of 3-bit words at $33.33\overline{3}$ MBd. The bits are then scrambled and converted through PCS encoding to a stream of code-groups (pairs of ternary symbols). These ternary symbol pairs are then multiplexed to a serialized stream of ternary symbols at $66.66\overline{6}$ MBd

##### 96.3.3.1.1 Control signals in 4B/3B conversion

Signals tx_enable_mii, tx_error_mii and TXD<3:0>, synchronized to MII TX_CLK are the input of 4B/3B conversion. After 4B/3B conversion, the transmit signals tx_data<2:0>, tx_enable and tx_error shall be synchronized with PCS transmit clock pcs_txclk. The frequencies of MII TX_CLK and pcs_txclk are 25 MHz and $33.33\overline{3}$ MHz respectively to keep the same bitwise throughput with 4B/3B conversion. TX_TCLK shall be derived from a local source in MASTER mode. TX_TCLK shall be derived from the recovered clock in SLAVE mode. The pcs_txclk is derived from the same clock source as TX_TCLK, with the proper clock division factor to get to the required frequency.

##### 96.3.3.1.2 4B/3B conversion for MII data

The transmit data (TXD<3:0>) at the MII shall first be converted into 3 bits as a group (tx_data<2:0>). As shown in Figure 96–6b and Figure 96–6c, when the number of bits of a packet is not a multiple of three, the 4B/3B conversion shall append stuff bits to the end of a packet (1 or 2 bits), and correspondingly, the tx_enable signal remains TRUE until all the bits in a packet (appended with stuff bits if applicable) are rate converted. Note, a packet includes preamble, SFD, and a MAC Frame as specified in 1.4.312. Those stuff bits may be padded randomly, which is left to implementer, and will be discarded at the receiver upon the boundary of the last nibble at the MII RX domain. The minimum 12 byte IPG period between packets enables flushing the extra stuff bits to prevent FIFO overflow.

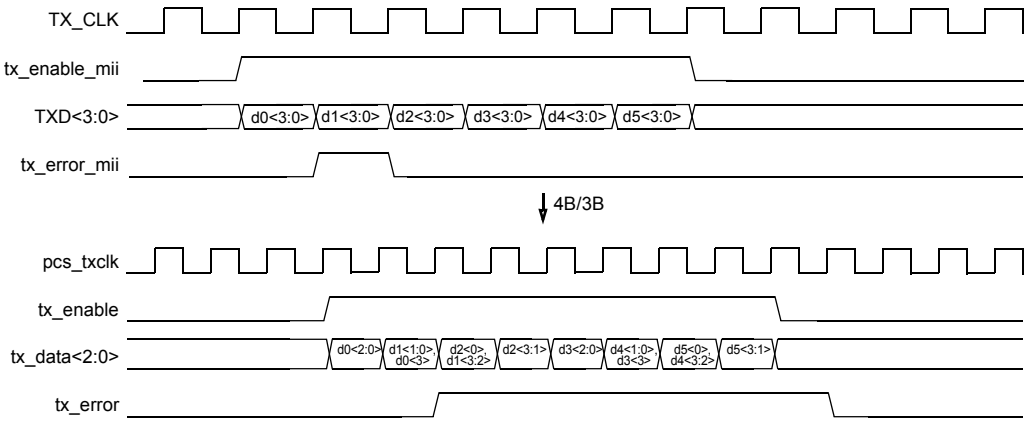



**Figure 96–6a—4B/3B MII signal conversion (3*n*-bit data, no stuff bit appended)**

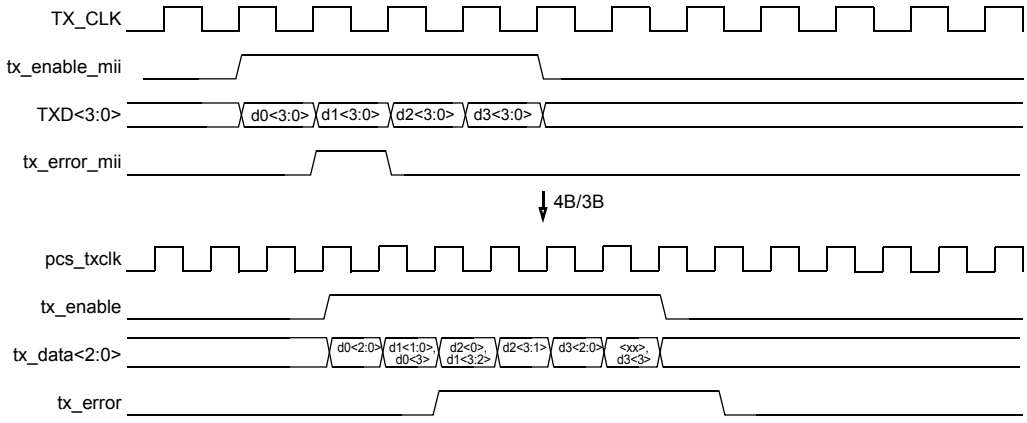



**Figure 96–6b—4B/3B MII signal conversion ((3*n*+1)-bit data, 2 stuff bits appended)**

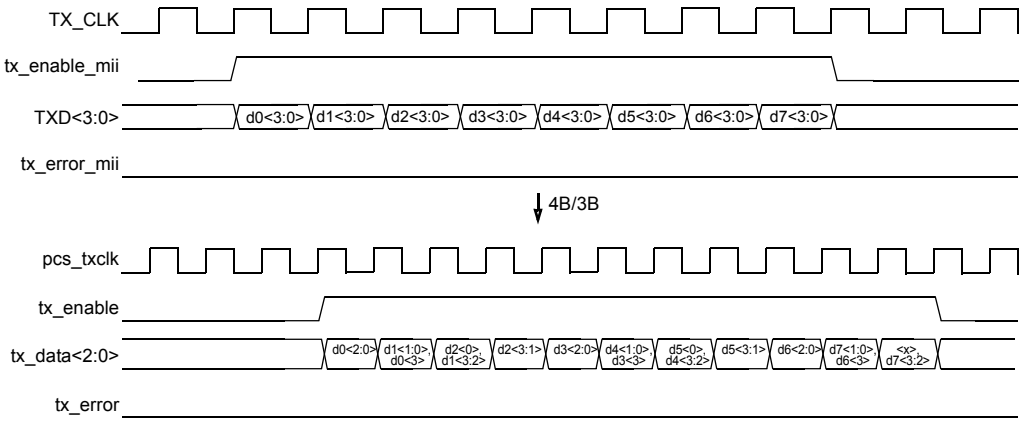



**Figure 96–6c—4B/3B MII signal conversion ((3*n*+2)-bit data, 1 stuff bit appended)**

### 96.3.3.2 PCS Transmit state diagram

The PCS Transmit function shall conform to the PCS Transmit state diagram in Figure 96–7, and the associated state variables, functions, timers and messages.

In each symbol period, PCS Transmit generates a sequence of symbols $A_n$ to the PMA, operating in one of three different modes (tx_mode), where symbol $A_n$ is a ternary code that can take values of {–1, 0, or +1}. The PMA transmits symbol $A_n$ over the wire pair BI_DA. The integer, $n$, is a time index, introduced to establish a temporal relationship between different symbol periods. A symbol period, $T$, is nominally equal to 15 ns. In the normal mode of operation, the PCS Transmit generates sequences of vectors using the encoding rules defined for SEND_N in 96.3.3.3.7 and 96.3.3.3.8, according to the value of tx_enable. Upon the assertion of tx_enable, the PCS Transmit function passes an SSD of 6 consecutive symbols to the PMA, which replaces the first 9 bits of preamble. Following SSD, tx_data<2:0> is encoded into ternary symbols as specified in 96.3.3.3, until tx_enable is de-asserted. Following the de-assertion of tx_enable, a special code ESD (or ERR_ESD when transmit error is encountered) of 6 consecutive symbols is generated, after which the transmission of idle mode is resumed. As shown in Figure 96–6a and Figure 96–6b, if tx_error_mii is ever asserted (due to MII TX_ER assertion) during the data frame period, tx_error is set as TRUE and stays TRUE till the end of frame to record such an occurrence. 100BASE-T1 only has one special symbol pair (0, 0) that is not used by Idle or Data symbols. Therefore, at the end of a frame, tx_error is examined to determine whether ESD3 or ERR_ESD3 are to be transmitted following ESD1 and ESD2, as shown in Figure 96–7.

The 100BASE-T1 PHY supports normal operation and link training operation. In training operation, the PCS ignores signals from MII and sends only the idle signals to the PMA until training process is complete (signaled by the link partner). The training process usually includes descrambler lock, timing acquisition, echo cancellation and equalizer convergence, etc.

If tx_mode has the value SEND_Z, PCS Transmit passes a vector of zeros at each symbol period to the PMA.

If tx_mode has the value SEND_I, PCS Transmit generates sequences of symbols according to the encoding rule in training mode as described in 96.3.3.3.6.

If tx_mode has the value SEND_N, PCS Transmit generates symbols $A_n$ at each symbol period representing data, special control symbols like SSD/ESD or IDLE symbols as defined in 96.3.3.3.5. The transition from idle to data is signaled by an SSD, and the end of transmission of data is signaled by an ESD.

During training operation (when tx_mode is SEND_I), knowledge of the transmitted symbols may be used at receiver side to perform any signal conditioning neccesary for meeting the required performance during normal operation. When the link is up, the PHY enters SEND_N mode and the transmitted PAM3 symbols are used at receiver PHY for continued clock frequency/phase tracking.

#### 96.3.3.2.1 Variables

DATA
: A vector of two ternary symbols corresponding to the code-group indicating valid data, as specified in 96.3.

ERR_ESD3
: A vector of two ternary symbols in the third code-group of ESD in case of tx_error (–1, –1) as specified in 96.3.3.3.5.

ESD1
: A vector of two ternary symbols in the first code-group of ESD (0, 0) as specified in 96.3.3.3.5.

ESD2
: A vector of two ternary symbols in the second code-group of ESD (0, 0) as specified in 96.3.3.3.5.

ESD3
: A vector of two ternary symbols in the third code-group of ESD (1, 1) as specified in 96.3.3.3.5.

IDLE
: A sequence of vectors of ternary symbols representing the special code-group generated in Idle mode, as specified in 96.3.3.3.6.

link_status
: The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive.
Values: OK or FAIL

loc_rcvr_status
: The loc_rcvr_status parameter set by the PMA Receive function and passed to the PCS via the PMA_RXSTATUS.indication primitive.
Values: OK or NOT_OK

pcs_reset
: The pcs_reset parameter set by the PCS Reset function.
Values: ON or OFF

SSD1
: A vector of two ternary symbols in the first code-group of SSD (0, 0) as specified in 96.3.3.3.5.

SSD2
: A vector of two ternary symbols in the second code-group of SSD (0, 0) as specified in 96.3.3.3.5.

SSD3
: A vector of two ternary symbols in the third code-group of SSD (0, 0) as specified in 96.3.3.3.5.

TXD<3:0>
The TXD<3:0> signal of the MII as specified in 22.2.2.4.

tx_enable
The tx_enable parameter generated by PCS Transmit as specified in Figure 96–7.
Values: TRUE or FALSE

tx_data<2:0>
Generated by PCS Transmit, transmit data is synchronous to pcs_txclk (33.33$\overline{3}$ MHz clock).

tx_error
The tx_error parameter generated by PCS Transmit as specified in Figure 96–7.
Values: TRUE or FALSE

TX_EN
The TX_EN signal of the MII as specified in 22.2.2.3.

TX_ER
The TX_ER signal of the MII as specified in 22.2.2.5.

tx_mode
The tx_mode parameter set by the PMA PHY Control function and passed to the PCS via the PMA_TXMODE.indication primitive.
Values: SEND_Z, SEND_N, or SEND_I

$Tx_n$
Alias for tx_symb_vector at time *n*.

tx_symb_pair
A pair of ternary symbols generated by the PCS Transmit function after ternary pair encoding.
Value: A pair of ternary transmit symbols. Each of the ternary symbols may take on one of the values {–1, 0, or +1}

#### 96.3.3.2.2 Functions

| | |
|---|---|
| ENCODE | In the PCS Transmit process, this function takes as its argument tx_data<2:0> and returns the corresponding tx_symb_pair. ENCODE follows the rules defined in 96.3.3.3. |

#### 96.3.3.2.3 Timers

| | | |
|---|---|---|
| symb_timer | The symb_timer shall be generated synchronously with TX_TCLK. In the PCS Transmit state diagram, the message PMA_UNITDATA.request is issued concurrently with symb_timer_done. | |
| | Continuous timer: | The condition symb_timer_done becomes true upon timer expiration. |
| | Restart time: | Immediately after expiration; timer restart resets the condition symb_timer_done. |
| | Duration: | 15 ns nominal. (See clock tolerance in 96.5.4.5) |
| symb_pair_timer | The symb_pair_timer shall be generated synchronously with PCS transmit clock pcs_txclk. | |
| | Continuous timer: | The condition symb_pair_timer_done becomes true upon timer expiration. |

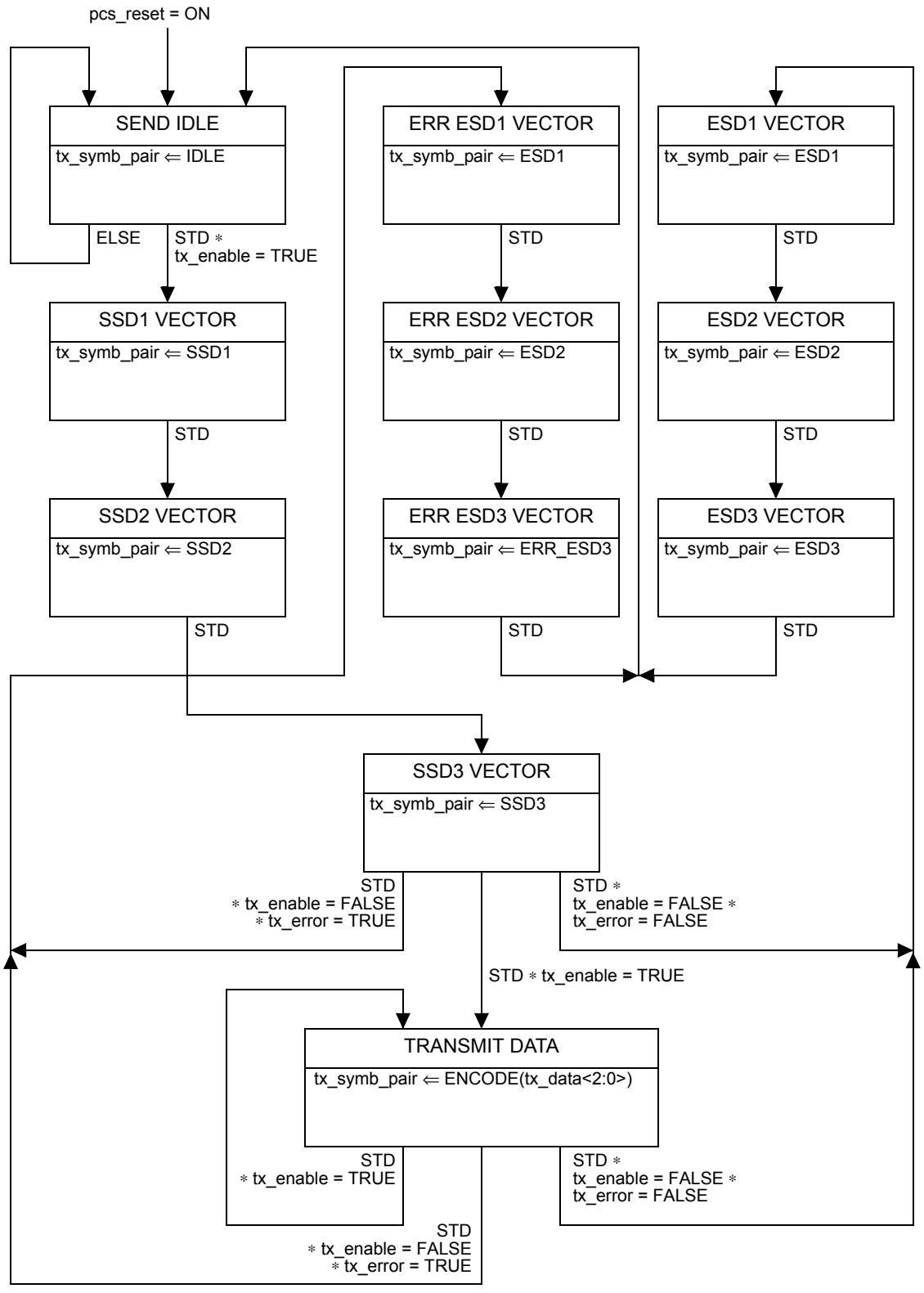



**Figure 96–7—PCS Transmit state diagram**

| | |
|---|---|
| Restart time: | Immediately after expiration; timer restart resets the condition symb_pair_timer_done. |
| Duration: | 30 ns nominal. |

#### 96.3.3.2.4 Messages

| | |
|---|---|
| STD | Alias for symb_pair_timer_done. |

### 96.3.3.3 PCS transmit symbol generation

The reference diagram of PCS transmit symbol generation is indicated in Figure 96–8. The tx_symb_pair is the ternary pair ($TA_n$, $TB_n$).

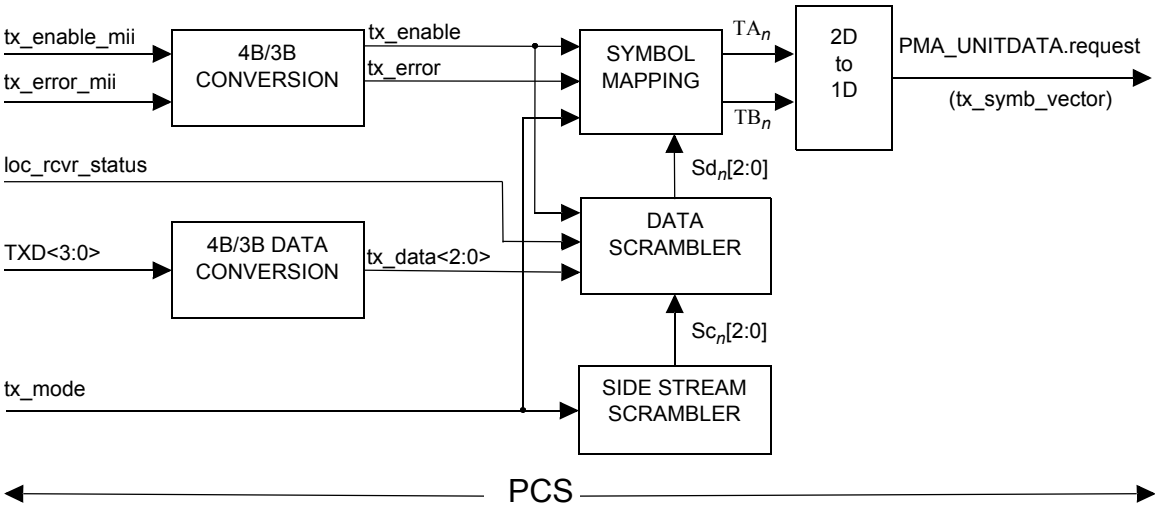



**Figure 96–8—PCS transmit symbol generation**

#### 96.3.3.3.1 Side-stream scrambler polynomial

The scrambler function shall conform to 40.3.1.3.1 and associated Figure 40-6 without any exceptions.

#### 96.3.3.3.2 Generation of Sy$_n$[2:0]

Generation of Sy$_n$[2:0] and Sc$_n$[2:0] shall conform to and be generated in accordance with the encoding rules in 40.3.1.3.2 and 40.3.1.3.3. Sy$_n$[2:0] vector in this specification is three bits, while the 40.3.1.3.2 vector is four bits.The PCS Transmit encoding of Sy$_n$[2:0] and then Sc$_n$[2:0] are performed, at time $n$, and used to eliminate the correlation of transmit data tx_data<2:0> and to generate idle and training symbols. Sy$_n$[3] is not used by definition.

#### 96.3.3.3.3 Generation of $Sc_n[2:0]$

Bits $Sc_n[2:0]$ shall be generated as follows:

$$Sc_n[2:0] = \begin{cases} [0\ 0\ 0] & \text{if ( tx\_mode = SEND\_Z )} \\ Sy_n[2:0] & \text{else} \end{cases}$$

#### 96.3.3.3.4 Generation of scrambled bits $Sd_n[2:0]$

The $tx\_data_n<2:0>$ is a three bit vector after 4B/3B conversion.

From scrambler bits $Sc_n[2:0]$ and $tx\_data_n<2:0>$, bits $Sd_n[2:0]$ shall be generated as follows:

$$Sd_n[2] = \begin{cases} Sc_n[2] \wedge tx\_data_n<2> & \text{if ( } tx\_enable_{n-3} = 1) \\ Sc_n[2] \wedge 1 & \text{else if ( loc\_rcvr\_status = OK)} \\ Sc_n[2] & \text{else} \end{cases}$$

$$Sd_n[1:0] = \begin{cases} Sc_n[1:0] \wedge tx\_data_n<1:0> & \text{if ( } tx\_enable_{n-3} = 1) \\ Sc_n[1:0] & \text{else} \end{cases}$$

Where ^ denotes the XOR logic operator.

#### 96.3.3.3.5 Generation of ternary pair ($TA_n$, $TB_n$)

The bits $Sd_n[2:0]$ are used to generate ternary pair ($TA_n$, $TB_n$). The ternary symbol pair (0, 0) is used in the special codes of SSD, ESD, and ESD with tx_error. Sequences of (0, 0), (0, 0), (0, 0) represent SSD, (0, 0), (0, 0), (1, 1) represent ESD and (0, 0), (0, 0), (–1, –1) represent ESD with tx_error.

#### 96.3.3.3.6 Generation of ($TA_n$, $TB_n$) when tx_mode = SEND_I

Among the nine possible values for the ternary pair ($TA_n$, $TB_n$) only six values are used in the training sequence as indicated in Table 96–1. The ternary pairs used to encode SSD and ESD are not used during training.

#### 96.3.3.3.7 Generation of ($TA_n$, $TB_n$) when tx_mode = SEND_N, tx_enable = 1

The mapping from $Sd_n[2:0]$ to ternary pairs in data mode is indicated in Table 96–2.

#### 96.3.3.3.8 Generation of ($TA_n$, $TB_n$) for idle sequence when tx_mode=SEND_N

The extra scrambling bit $Sx_n$ is introduced to balance the power density for ternary pair ($TA_n$, $TB_n$). $Sx_n$ shall be generated as follows:

$$Sx_n = Scr_n[7] \wedge Scr_n[9] \wedge Scr_n[12] \wedge Scr_n[14]$$

**Table 96–1—Idle symbol mapping in training**

| $Sd_n[2:0]$ | $TA_n$ | $TB_n$ |
|---|---|---|
| 000 | –1 | 0 |
| 001 | 0 | 1 |
| 010 | –1 | 1 |
| 011 | 0 | 1 |
| 100 | 1 | 0 |
| 101 | 0 | –1 |
| 110 | 1 | –1 |
| 111 | 0 | –1 |

**Table 96–2—Data symbols when tx_mode=SEND_N**

| $Sd_n[2:0]$ | $TA_n$ | $TB_n$ |
|---|---|---|
| 000 | –1 | –1 |
| 001 | –1 | 0 |
| 010 | –1 | 1 |
| 011 | 0 | –1 |
| Used for SSD/ESD | 0 | 0 |
| 100 | 0 | 1 |
| 101 | 1 | –1 |
| 110 | 1 | 0 |
| 111 | 1 | 1 |

where ^ denotes the XOR logic operator. The ternary pair ($TA_n$, $TB_n$) is generated according to Table 96–3.

#### 96.3.3.3.9 Generation of ($TA_n$, $TB_n$) when tx_mode=SEND_Z

The ternary pair ($TA_n$, $TB_n$) simply shows as zero vector (0, 0) when tx_mode=SEND_Z.

**Table 96–3—Idle symbols when tx_mode=SEND_N**

| | tx_mode = SEND_N | | | |
|---|---|---|---|---|
| | $Sx_n = 0$ | | $Sx_n = 1$ | |
| $Sd_n[2:0]$ | $TA_n$ | $TB_n$ | $TA_n$ | $TB_n$ |
| 000 | –1 | 0 | –1 | 0 |
| 001 | 0 | 1 | 1 | 1 |
| 010 | –1 | 1 | –1 | 1 |
| 011 | 0 | 1 | 1 | 1 |
| 100 | 1 | 0 | 1 | 0 |
| 101 | 0 | –1 | –1 | –1 |
| 110 | 1 | –1 | 1 | –1 |
| 111 | 0 | –1 | –1 | –1 |

### 96.3.3.3.10 Generation of symbol sequence

The generation of one-dimensional symbol sequence from ternary pair ($TA_n$, $TB_n$) is illustrated in Figure 96–9.

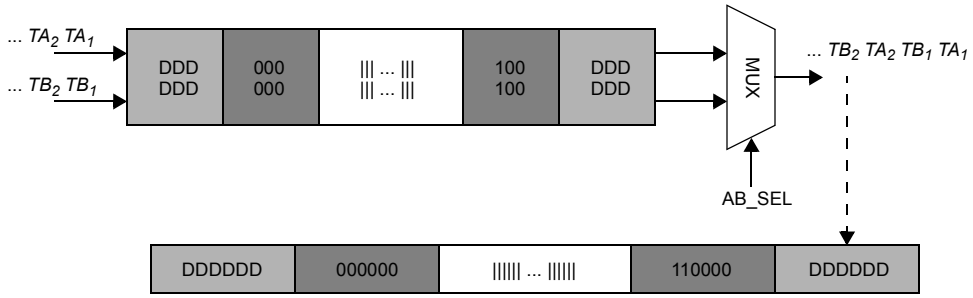



**Figure 96–9—2-D symbol to 1-D symbol conversion**

The symbol is sent to one sequence in the form of interleave in the order from right to left. AB_SEL signal defines the interleave selection for code-groups. The serial stream is created by interleaving either ($TA_n$, $TB_n$) with $TA_n$ followed by $TB_n$ or ($TB_n$, $TA_n$) with $TB_n$ followed by $TA_n$. The ESD (after a packet) is followed by IDLE symbols, then SSD, and then by DATA. The symbol rate is twice as fast as pcs_txclk.

### 96.3.4 PCS Receive

### 96.3.4.1 PCS Receive overview

The PCS Receive function shall conform to the PCS Receive state diagram in Figure 96–10a and Figure 96–10b, and associated state variables.

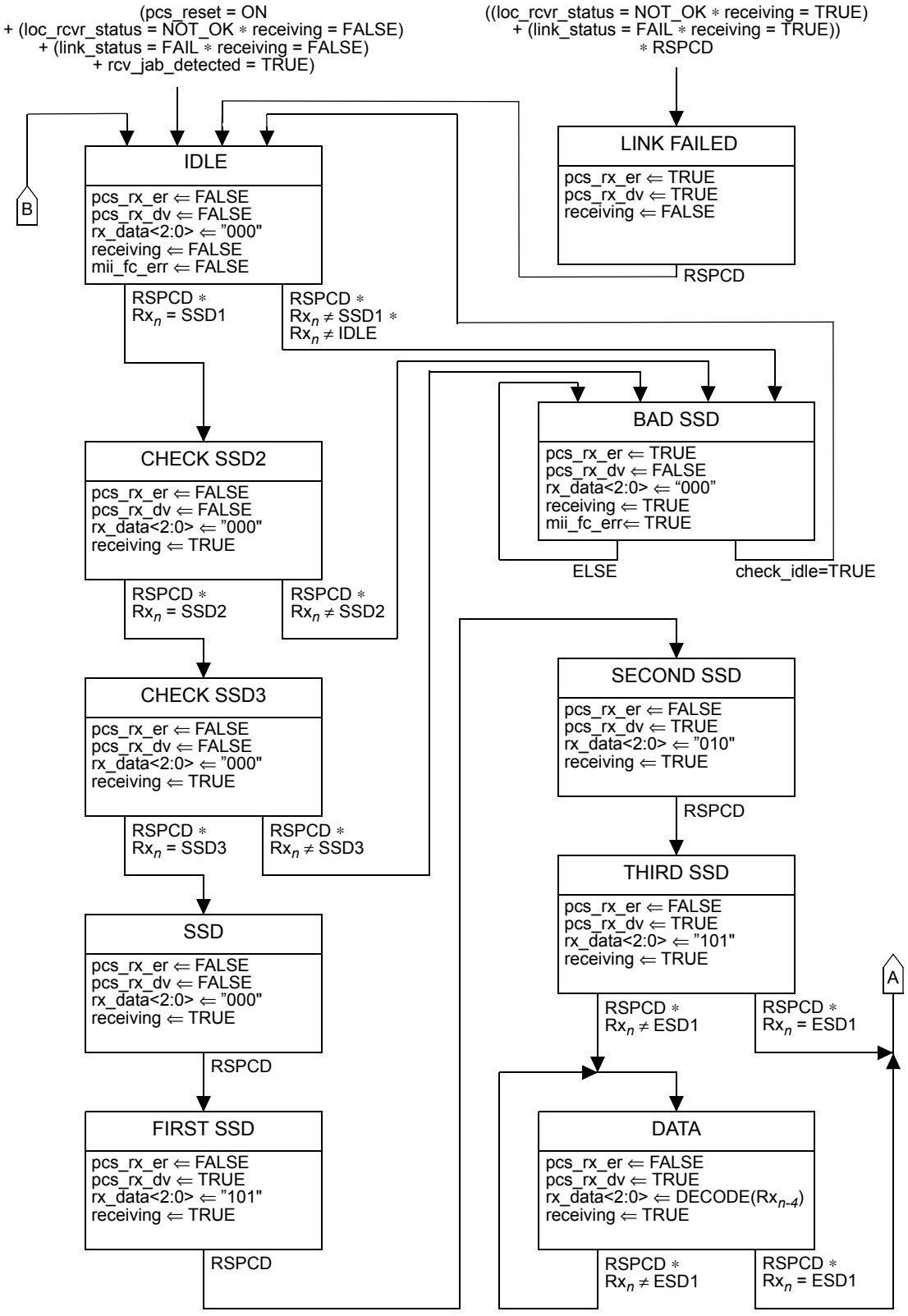



**Figure 96–10a—PCS Receive state diagram**

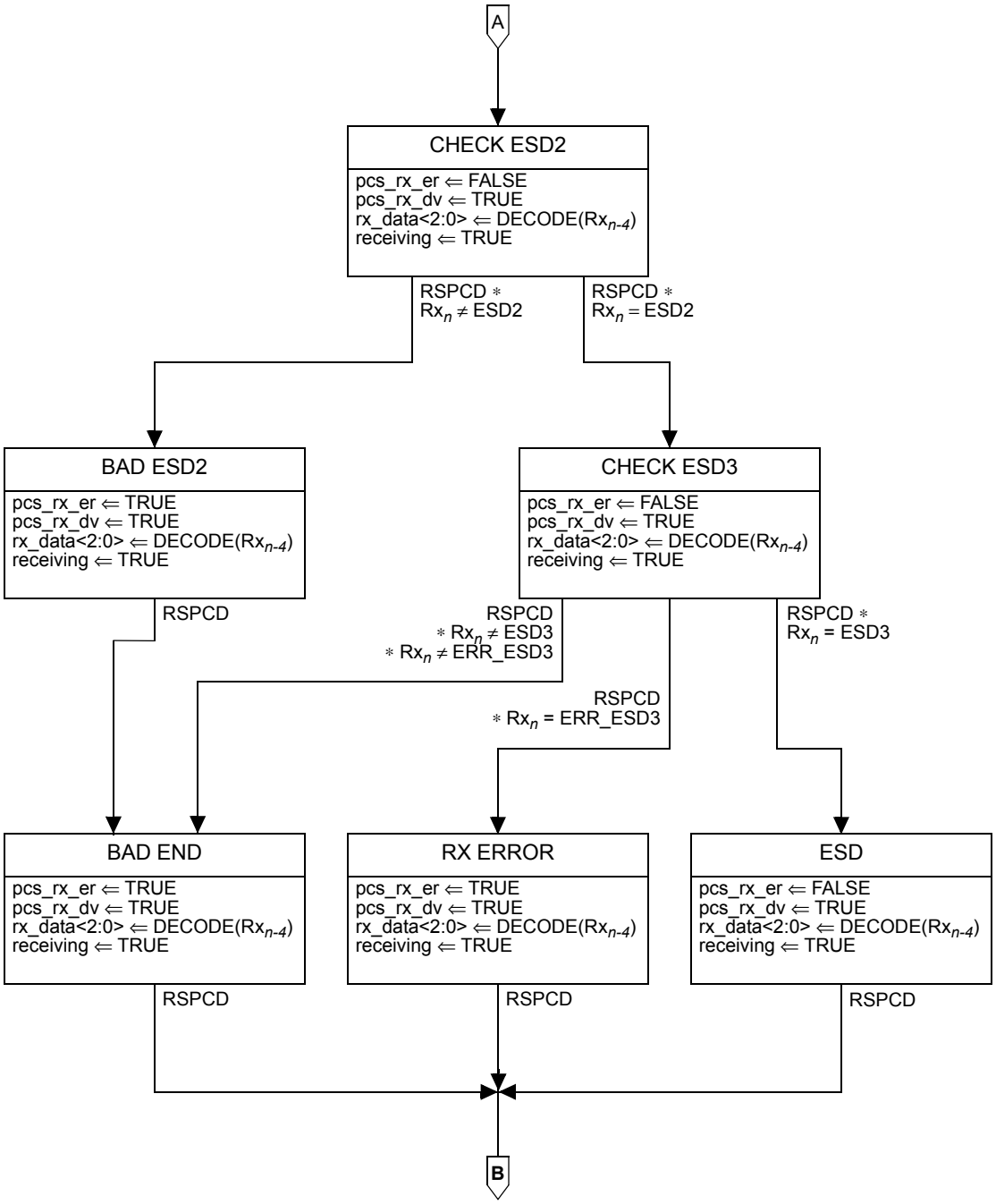



**Figure 96–10b—PCS Receive state diagram (continued)**

A JAB state machine as shown in Figure 96–11, is implemented to prevent any mis-detection of ESD1 and ESD2 that would make the PCS Receive state machine lock up in the DATA state. The maximum dwelling time in DATA state shall be less than the period specified for rcv_max_timer. When rcv_max_timer expires, the PCS Receive state machine is reset and transition to IDLE state is forced.

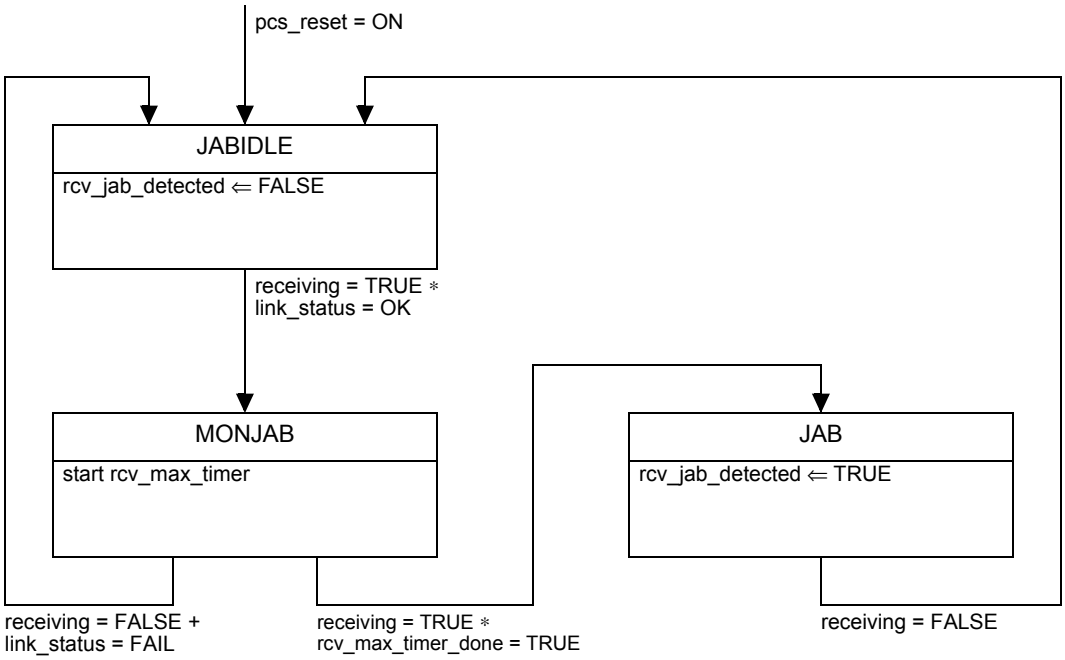



**Figure 96–11—JAB state diagram**

In Figure 96–10a, there are a total of four states after SSD3 detection before the DATA state; meanwhile, there are also four states before the IDLE state (including the DATA state) that perform DATA decoding. As a result, the depth of data flush-in delay line is the same as the flush-out delay line ensuring correct packet reception at the MII.

The variables, functions, and timers used in Figure 96–10a, Figure 96–10b and Figure 96–11 are defined as below. For the definition of IDLE, SSD1, SSD2, SSD3, ESD1, ESD2, ESD3 and ERR_ESD3, see 96.3.3.2.1.

#### 96.3.4.1.1 Variables

link_status
: The link_status parameter set by PMA Link Monitor and passed to the PCS via the PMA_LINK.indication primitive.
Values: OK or FAIL

loc_rcvr_status
: The loc_rcvr_status parameter set by the PMA Receive function and passed to the PCS via the PMA_RXSTATUS.indication primitive.
Values: OK or NOT_OK

mii_fc_err
: Indicates that a false carrier error has occurred.
Values: TRUE or FALSE

pcs_reset
: The pcs_reset parameter set by the PCS Reset function.
Values: ON or OFF

pcs_rx_er
PCS receive error indication signal synchronous to pcs_rxclk.
Values: TRUE or FALSE

pcs_rx_dv
PCS receive data link indication signal synchronous to pcs_rxclk.
Values: TRUE or FALSE

receiving
Generated by the PCS Receive function; if set as TRUE, it indicates that the PCS is in Data mode.
Values: TRUE or FALSE

rcv_jab_detected
Variable set as TRUE when in JAB state as shown in JAB state diagram in Figure 96–11 else it is set FALSE.
Values: TRUE or FALSE

$Rx_n$
Received symbol pair generated by PCS Receive at time *n*.

rx_data<2:0>
PCS decoded data synchronous to pcs_rxclk.

rx_symb_pair
A pair of ternary symbols generated by the PCS Receive function before ternary pair decoding.
Value: A pair of ternary receive symbols. Each of the ternary symbols may take on one of the values {–1, 0, or +1}.

rx_symb_vector
A vector of ternary symbols received by the PMA and passed to the PCS via the PMA_UNITDATA.indication primitive.
Value: SYMB_1D

#### 96.3.4.1.2 Functions

| | |
|---|---|
| check_idle | A function used by the PCS Receive process to detect the reception of valid idle code-groups after an error condition during the process. The check_idle function operates on six consecutive code-groups after de-interleaving rx_symb_vectors. The check_idle function then returns a Boolean value indicating whether or not all six consecutive code-groups after de-interleaving rx_symb_vectors are valid in idle mode encoding, as specified in 96.3.3.3.5. |
| DECODE | In the PCS Receive process, this function takes as its argument the value of rx_symb_pair and returns the corresponding rx_data<2:0>. DECODE follows the rules outlined in 96.3.4.2. |

#### 96.3.4.1.3 Timer

| | |
|---|---|
| RSPCD | Receive Symbol Pair Converted Done, synchronized with PCS receive clock pcs_rxclk of frequency 33.33$\overline{3}$ MHz. |
| rcv_max_timer | A timer used to determine the maximum amount of time the PHY Receive state machine stays in DATA state. The timer shall expire 1.08 ms ± 54 μs after being started. The condition rcv_max_timer_done becomes true upon timer expiration. |

### 96.3.4.2 PCS Receive symbol decoding

When PMA Receive indicates normal operation and sets loc_rcvr_status = OK, the PCS Receive function checks the symbol sequences and searches for SSD or receive error indicator. The receiver de-interleaves the sequences of rx_symb_vector to rx_symb_pair accordingly.

The received symbols, rx_symb_vector, are de-interleaved to generate rx_symb_pair ($RA_n$, $RB_n$). To achieve correct operation, PCS Receive uses the knowledge of the encoding rules that are employed in the idle mode. PCS Receive generates the sequence of symbols and indicates the reliable acquisition of the descrambler state by setting the parameter scr_status to OK. The received ternary pairs ($RA_n$, $RB_n$) are decoded to generate signals rx_data<2:0>, pcs_rx_dv, and pcs_rx_error. These signals are processed through 3B/4B conversion to generate signals RXD<3:0>, RX_DV and RX_ER at the MII.

PCS Receive sets pcs_rx_dv=TRUE when it receives SSD, and sets pcs_rx_dv=FALSE when it receives ESD or ESD with error. The number of bits received in a packet is always a multiple of 3 that shall go through the process of 3B/4B conversion, discarding the residual 1 bit or 2 bits of data.

PCS Receive shall set pcs_rx_er = TRUE when it receives bad ESDs, ERR_ESD, or bad SSDs. When the state machine reaches the IDLE state, pcs_rx_er gets reset to FALSE.

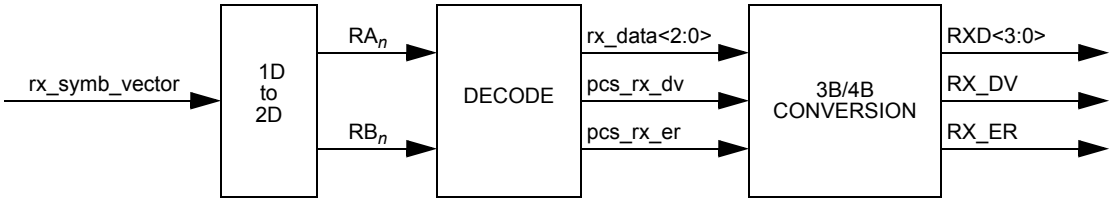



**Figure 96–12—PCS Data receive symbol decoding**

### 96.3.4.3 PCS Receive descrambler polynomial

This function shall conform to 40.3.1.4.2, with the exception that it applies to rx_data<2:0>.

### 96.3.4.4 PCS Receive automatic polarity detection (Optional)

During training, automatic polarity detection may be done in PCS Receive with proper decoding procedures. In the IDLE mode, $Sd_n[2:0]$ are generated by side-stream scrambler with $Sd_n[0]=Scr_n[0]$. According to Table 96–1, when $Sd_n[0]$ is 0, $TA_n$ is either +1 or –1; otherwise, $TA_n$ is 0. Based on this rule, $Scr_n[0]$ should be decoded solely depending on the value of $RA_n$, then fed back to the shift registers of side-stream descrambler to achieve reliable state acquisition. After that, in every symbol cycle, $Scr_n[0]$ should be compared with the processed $RA_n$ value. Continuous consistency within a certain period means the scrambler has been successfully locked. Polarity can also be automatically detected with similar techniques in a recursive process: one assumption of polarity is made first and the descrambler synchronization is monitored within a certain period to determine whether such an assumption is correct; if not, the same procedure is repeated with a different polarity assumption.

Polarity detection and correction can be done simultaneously at the earliest link up stages. Link up starts with the MASTER PHY sending symbols to the SLAVE PHY. During this initial stage, all hand-shaking signal status, such as rem_rcvr_status, are known as FALSE. With this a priori knowledge, polarity should be accurately detected by the SLAVE side. If a polarity flip is detected, the SLAVE changes the sign of its received signals ($RA_n$, $RB_n$) to correct the polarity. Furthermore, it shall invert its transmitted signals ($TA_n$, $TB_n$). Since polarity correction has been taken care of by the SLAVE PHY, the polarity would always be observed as correct by the MASTER PHY.

### 96.3.4.5 PCS Receive MII signal 3B/4B conversion

The MII receive signals RXD<3:0>, RX_DV and RX_ER are synchronized with clock RX_CLK ; while PCS Receive generated signals rx_data<2:0>, rx_dv, and rx_error shall be synchronized with pcs_rxclk to keep the same bitwise throughput after 3B/4B conversion. Generation of pcs_rxclk is implementation dependent. RX_CLK may be derived from the same clock source as TX_CLK if the PHY is in MASTER mode or from the recovered clock if the PHY is in SLAVE mode. The pcs_rxclk is derived from the same clock source as RX_CLK, with the proper clock division factor to get to the required frequency.

The conversion from pcs_rxclk domain signals to MII signals is shown in Figure 96–13. If the number of bits from the received data packet in pcs_rxclk domain is not a multiple of four, the residual bits are actually the stuff bits appended during 4B/3B conversion at the transmitter side. With 3B/4B conversion, those bits shall be discarded. RX_DV shall be deasserted right after the last nibble is converted.

If the BAD SSD state occurred in Figure 96–10a PCS Receive state diagram, the false carrier error shall be indicated on the MII after conversion.

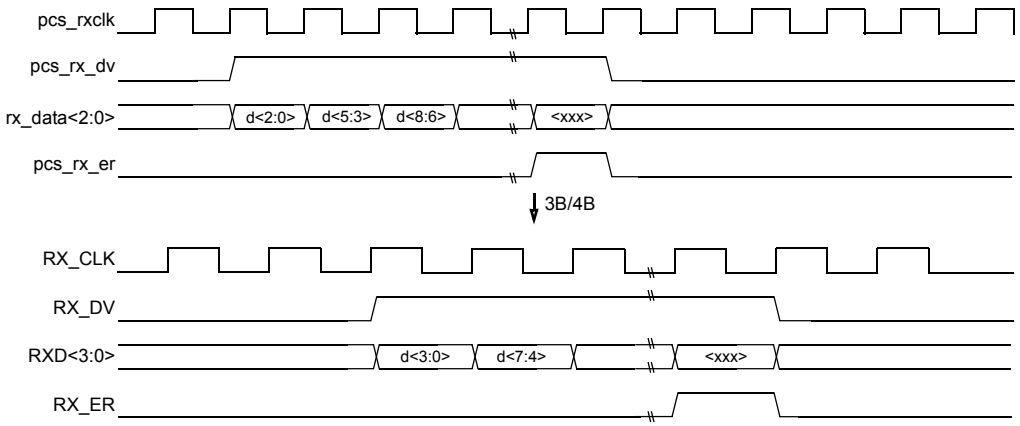



**Figure 96–13—PCS Receive 3B/4B conversion reference diagram**

### 96.3.5 PCS Loopback

The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14, defined in 45.2.3.1.2, is set to a one. In this mode, the PCS shall accept data on the transmit path from the MII and return it on the receive path to the MII. Additionally, the PHY receive circuitry shall be isolated from the network medium, and the assertion of TX_EN at the MII shall not result in the transmission of data on the network medium. The PCS loopback data flow is illustrated in Figure 96–14.

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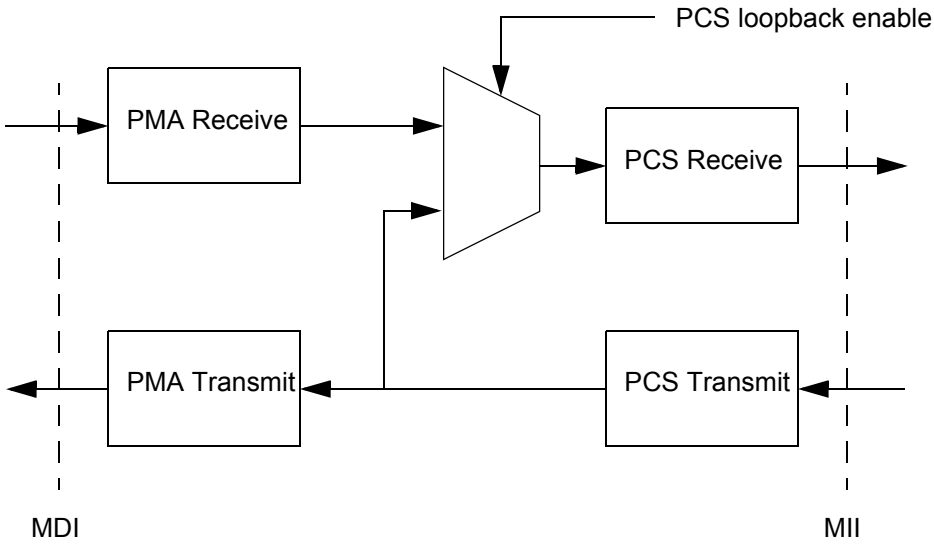



**Figure 96–14—PCS loopback data flow**

The MAC compares the packets sent through the MII Transmit function to the packets received from the MII Receive function to validate the functionality of 100BASE-T1 PCS functions.

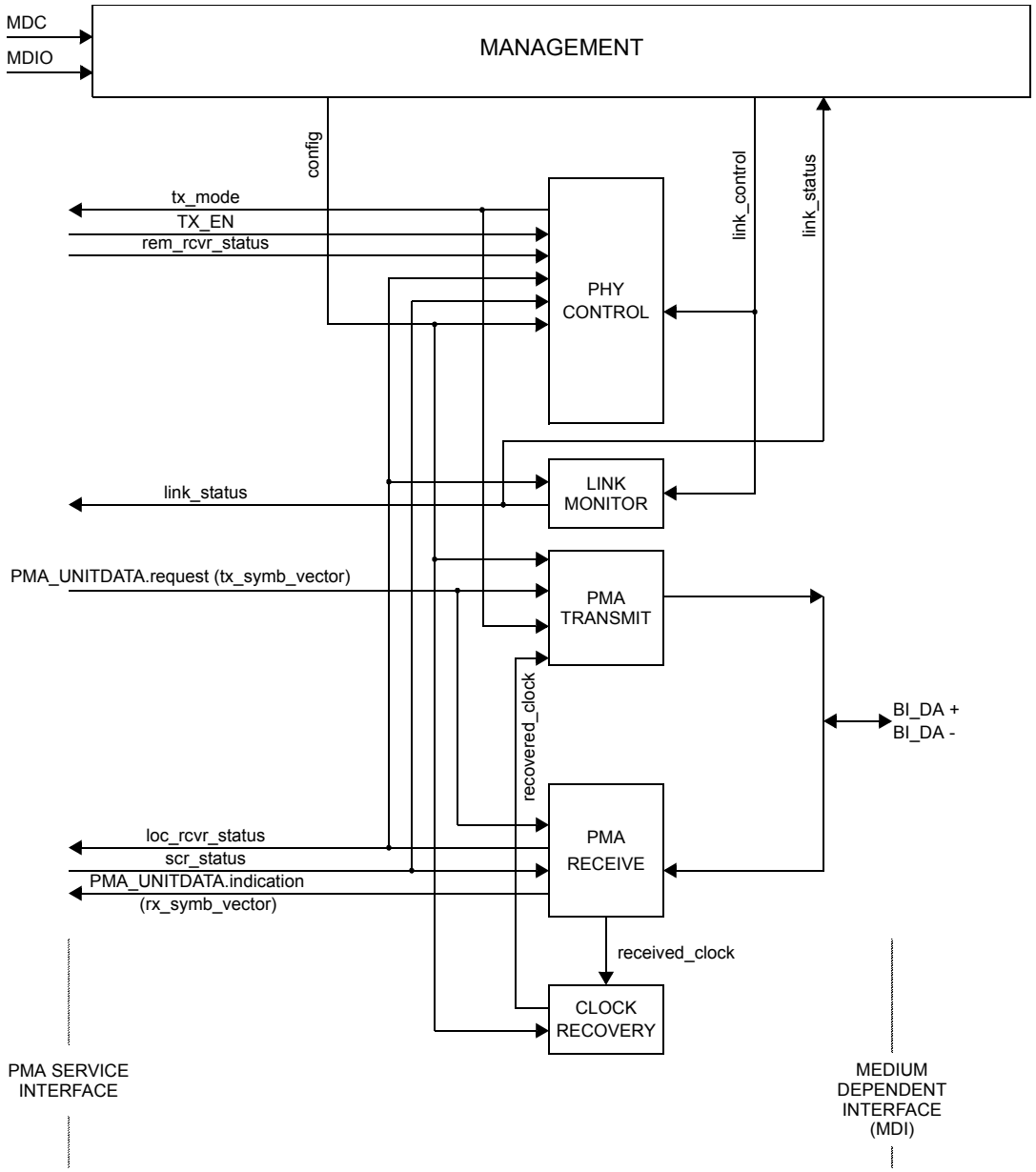
## 96.4 Physical Medium Attachment (PMA) Sublayer

The PMA couples messages from the PMA service interface specified in 96.2.1 onto the 100BASE-T1 physical medium, and provides the link management and PHY Control functions. The PMA provides full duplex communications to and from medium employing 3-level Pulse Amplitude Modulation (PAM3). The interface between PMA and the baseband medium is the Medium Dependent Interface (MDI), which is specified in 96.8.

PMA functions are illustrated in Figure 96–15.

### 96.4.1 PMA Reset function

This function shall conform to 40.4.2.1. The optional low power mode referenced in 36.2.5.1.3 is not supported.




NOTE: The recovered_clock arc shown indicates delivery of the recovered clock back to PMA TRANSMIT for loop timing.

**Figure 96–15—PMA functional block diagram**

### 96.4.2 PMA Transmit function

Figure 96–16 illustrates the signal flow of the 100BASE-T1 PMA Transmit function. During transmission, PMA_UNITDATA.request conveys to the PMA using tx_symb_vector the value of the symbols to be sent over the single transmit pair.

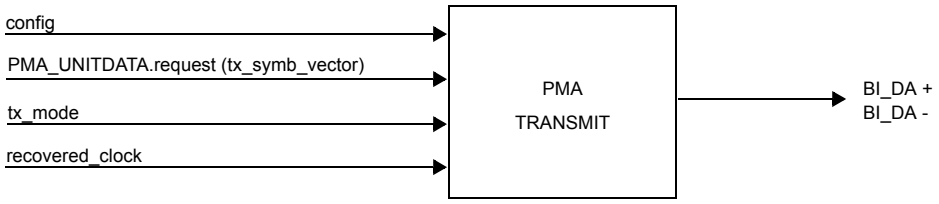



**Figure 96–16—PMA Transmit**

A single transmitter is used to generate the PAM3 signal BI_DA on the wire, using the transmit clock, TX_TCLK of 66.66$\overline{6}$ MHz, that is the reference clock for the MASTER. When the config parameter is set to MASTER, the PMA Transmit Function derives the TX_TCLK from a local clock source. When the config parameter is set to SLAVE, the PMA Transmit Function derives the TX_TCLK from the recovered clock.

The PMA Transmit fault function is optional. The faults detected by this function are implementation specific. If the MDIO interface is implemented, then this function shall be mapped to the transmit fault bit as specified in 45.2.1.7.4.

### 96.4.3 PMA Receive function

Figure 96–17 illustrates the signal flow of the 100BASE-T1 PMA Receive function. There are three primary PMA Receive characteristics: Receivers, Abilities, and Sub-Functions.

The 100BASE-T1 PMA Receive function comprises a single receiver (PMA Receive) for PAM3 modulated signals on a single balanced twisted-pair, BI_DA. PMA Receive has the ability to translate the received signals on the single pair into the PMA_UNITDATA.indication parameter rx_symb_vector. It detects ternary symbol sequences from the signals received at the MDI over one channel and presents these sequences to the PCS Receive function. PMA Receive has Signal Equalization and Echo Cancellation sub-functions. These sub-functions are used to determine the receiver performance and generate loc_rcvr_status. The parameter loc_rcvr_status is generated by PMA Receive to indicate the status of the receive link at the local PHY. This variable indicates to the PCS Transmitter, PCS Receiver, PMA PHY Control function and Link Monitor whether the status of the overall received link is ok or not. scr_status is generated by the PCS Receiver to indicate the status of the descrambler to the local PHY. It conveys the information on whether the scrambler has achieved synchronization or not to the PMA receive function.

The PMA Receive fault function is optional. The PMA Receive fault function is the logical OR of the link_status = Fail and any implementation specific fault. If the MDIO interface is implemented, then this function shall contribute to the receive fault bit specified in 45.2.1.7.5.

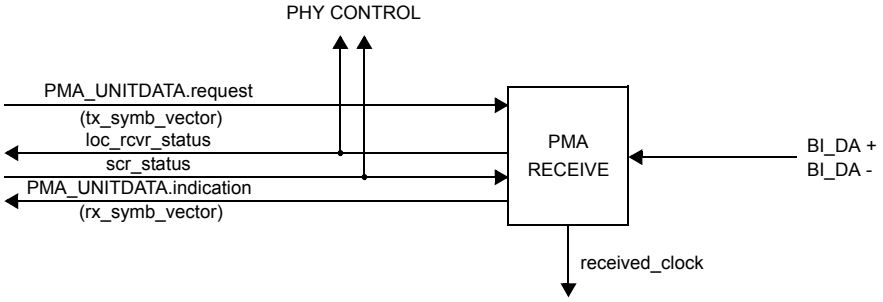



**Figure 96–17—PMA Receive**

### 96.4.4 PHY Control function

For the 100BASE-T1 PHY, FORCE mode is used to achieve link acquisition between two 100BASE-T1 link partners. Using FORCE mode, PMA_CONFIG is pre-determined to be MASTER or SLAVE via management control during initialization or via default hardware set-up. It governs the control actions needed to bring the PHY into the 100BASE-T1 mode of operation so that frames can be exchanged with the link partner. PMA PHY Control also generates the signals that control PCS and PMA sublayer operations. It determines whether the PHY operates in the normal mode, enabling data transmission over the link segment, or whether the PHY sends special code-groups that represent the idle mode. PHY Control shall comply with the state diagram shown in Figure 96–18. PHY Control sets tx_mode to SEND_N (transmission of normal MII Data Stream, Control Information, or idle), SEND_I (transmission of IDLE code-groups), or SEND_Z (transmission of zero code-groups).

### 96.4.5 Link Monitor function

Link Monitor operation, as shown in state diagram of Figure 96–19, shall be provided to support PHY Control. FORCE mode is used to set link_control to ENABLE through management control during the PHY initialization. In all cases, the time from power_on = FALSE, transitioning to power_on = TRUE, to link_status=OK shall be less than 100 ms.

### 96.4.6 PMA clock recovery

This PMA function recovers the clock from the received stream. It is coupled to the receiver in order to provide the clock for optimum sampling of the channel. PMA clock recovery outputs are also used as input variables for other PMA functions.

### 96.4.7 State variables

#### 96.4.7.1 State diagram variables

config
: The config parameter is set by management and passed to the PMA and PCS.
Values: MASTER or SLAVE.

link_control
: This variable is generated by management or set by default.
Values: ENABLE or DISABLE.

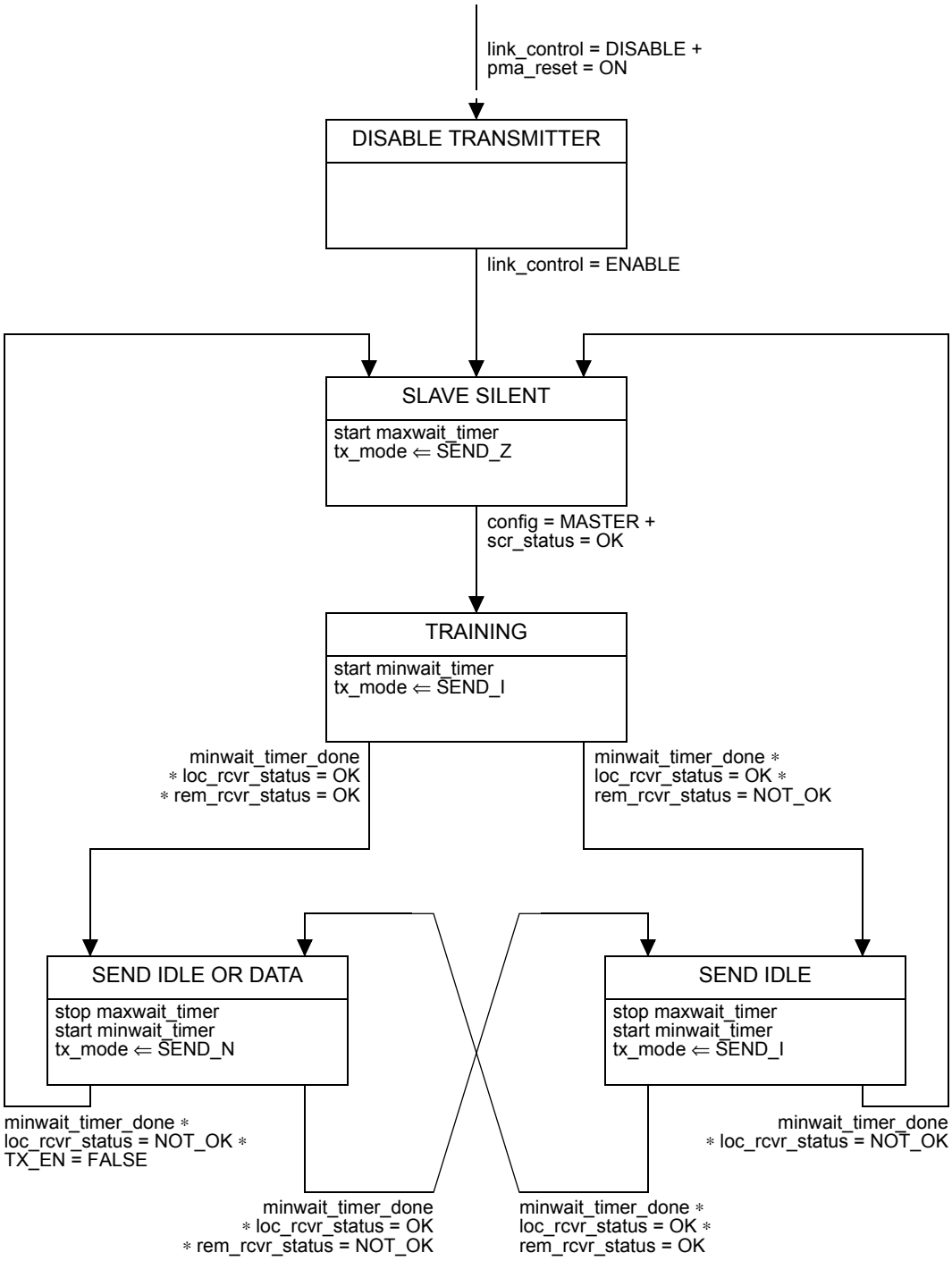



**Figure 96–18—PHY Control state diagram**

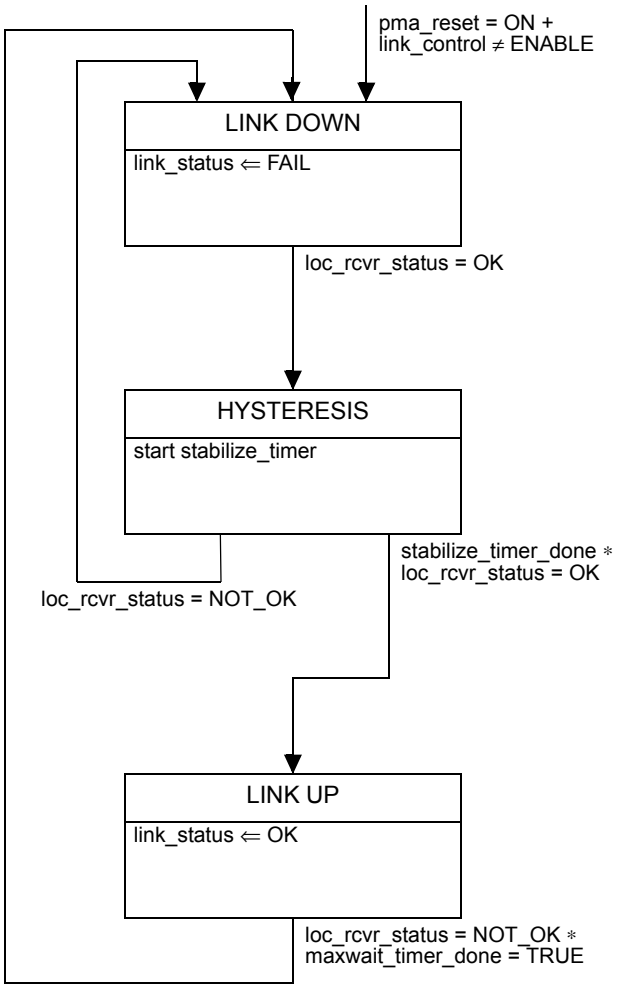



**Figure 96–19—Link Monitor state diagram**

link_status

This variable is generated by the PMA to indicate the status of the link.

Values: OK or FAIL.

loc_rcvr_status

Variable set by the PMA Receive function to indicate correct or incorrect operation of the receive function for the local PHY.

Values: OK: The receive function for the local PHY is operating reliably.
NOT_OK: Operation of the receive function for the local PHY is unreliable.

pma_reset

Allows reset of all PMA functions.

Values: ON or OFF

Set by: PMA Reset

rem_rcvr_status

Variable set by the PCS Receive function to indicate whether correct operation of the receive function for the remote PHY is detected or not.

Values: OK: The receive function for the remote PHY is operating reliably.
NOT_OK: Reliable operation of the receive function for the remote PHY is not detected.

scr_status
: The scr_status parameter as communicated by the PMA_SCRSTATUS.request primitive.
Values: OK: The descrambler has achieved synchronization.
NOT_OK: The descrambler is not synchronized.

tx_mode
: PCS Transmit sends code-groups according to the value assumed by this variable.
Values: SEND_N: This value is continuously asserted when code-group sequences representing a PCS code-group in PCS Transmit function, control information, or idle mode are transmitted.
SEND_I: This value is continuously asserted when transmission of sequences of code-groups representing the idle mode is to take place.
SEND_Z: This value is asserted when transmission of zero code-groups is to take place.

tx_enable
: The tx_enable parameter generated by PCS Transmit as specified in Figure 96–8.
Values: TRUE or FALSE.

#### 96.4.7.2 Timers

| | |
|---|---|
| maxwait_timer | A timer used to limit the amount of time during which a receiver dwells in the SLAVE SILENT and TRAINING states. The timer shall expire 200 ms ± 2 ms. This timer is used jointly in the PHY Control and Link Monitor state diagrams. The maxwait_timer is tested by the Link Monitor to force link_status to be set to FAIL if the timer expires and loc_rcvr_status is NOT_OK. See Figure 96–18. |
| minwait_timer | A timer used to determine the minimum amount of time the PHY Control stays in the TRAINING, SEND IDLE, or DATA states. The timer shall expire 1.8 µs ± 0.18 µs after being started. |
| stabilize_timer | A timer used to control the minimum time that loc_rcvr_status must be OK before a transition to Link Up can occur. The timer shall expire 1.8 µs ± 0.18 µs after being started. |

## 96.5 PMA electrical specifications

This subclause defines the electrical characteristics of the PMA for a 100BASE-T1 Ethernet PHY.

### 96.5.1 EMC tests

Direct Power Injection (DPI) and 150 Ω emission tests for noise immunity and emission as per 96.5.1.1 and 96.5.1.2 may be used to establish a baseline for PHY EMC performance. These tests provide a high degree of repeatability and a good correlation to immunity and emission measurements. Additional tests may be needed to verify EMC performance in various configurations, applications, and conditions.

#### 96.5.1.1 Immunity—DPI test

In a real application radio frequency (RF) common mode (CM) noise at the PHY is the result of electromagnetic interference coupling to the cabling system. Additional differential mode (DM) noise at the PHY is generated from the CM noise by mode conversion of all parts of the cabling system and the MDI. The sensitivity of the PMA's receiver to RF CM noise may be tested according to the DPI method of IEC 62132-4, and may need to comply with more stringent requirements as agreed upon between customer and supplier.

#### 96.5.1.2 Emission—Conducted emission test

The emission of the PMA transmitter to its electrical environment may be tested according to the 150 Ω direct coupling method of IEC 61967-4, and may need to comply with more stringent requirements as agreed upon between customer and supplier.

### 96.5.2 Test modes

The test modes described in this subclause shall be provided to allow testing of the transmitter waveform, transmitter distortion, transmitter jitter, and transmitter droop. The test modes can be enabled by setting bits 1.2102.15:13 (100BASE-T1 PMA/PMD test control register) of the PHY Management register set as described in 45.2.1.132. These test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation.

a) Test mode 1—Transmit droop test mode
b) Test mode 2—Transmit jitter test in MASTER mode
c) Test mode 4—Transmit distortion test
d) Test mode 5—Normal operation at full power (for the PSD mask)

When test mode 1 is enabled, the PHY shall transmit N "+1" symbols followed by N "–1" symbols. The value of N shall be a minimum of 34 symbol periods to achieve a symbol period greater than 500 ns. This sequence is repeated continually. For example, a PHY with test mode 1 enabled and N = 40 symbols (symbol period of 600 ns) would transmit a pattern sufficiently long enough for a 500 ns droop measurement.

When test mode 2 is enabled, the PHY shall transmit the data symbol sequence {+1, –1} repeatedly on its channel. The transmitter shall time the transmitted symbols from a $66.66\overline{6}$ MHz ± 100 ppm clock in the MASTER timing mode.

When test mode 4 is enabled, the PHY shall transmit the sequence of symbols generated by the following scrambler generator polynomial, bit generation, and level mappings:

$$g(x) = 1 + x^{9} + x^{11} \tag{96–1}$$

The maximum-length shift register used to generate the sequences defined by this polynomial shall be updated once per symbol interval (15 ns). The bits stored in the shift register delay line at a particular time n are denoted by $Scr_n[10:0]$. At each symbol period the shift register is advanced by one bit and one new bit represented by $Scr_n[0]$ is generated. Bits $Scr_n[8]$ and $Scr_n[10]$ are exclusive OR'd together to generate the next $Scr_n[0]$ bit. The bit sequences, $x0_n$, and $x1_n$, generated from combinations of the scrambler bits as shown in the following equations, shall be used to generate the ternary symbols, $s_n$, as shown in Table 96–4. The transmitter shall time the transmitted symbols from a $66.66\overline{6}$ MHz ± 100 ppm clock in the MASTER timing mode.

$$x0_n = Scr_n[0] \tag{96–2}$$

$$x1_n = Scr_n[1] \wedge Scr_n[4] \tag{96–3}$$

**Table 96–4—Transmitter test mode 4 symbol mapping**

| $x1_n$ | $x0_n$ | Transmit PAM3 symbol |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | –1 |

Test mode 5 is for checking whether the transmitter is compliant with the transmit PSD mask. When test mode 5 is enabled, the PHY shall transmit a pseudo-random sequence of PAM3 symbols, generated by the scrambling function described in 96.3.3.3.1.

### 96.5.3 Test fixtures

The fixtures shown in Figure 96–20, Figure 96–21, and Figure 96–22, or their equivalents, are used in the stated respective tests for measuring the transmitter specifications. The tolerance of resistors shall be ± 0.1%. All the transmitter tests are defined at the MDI.

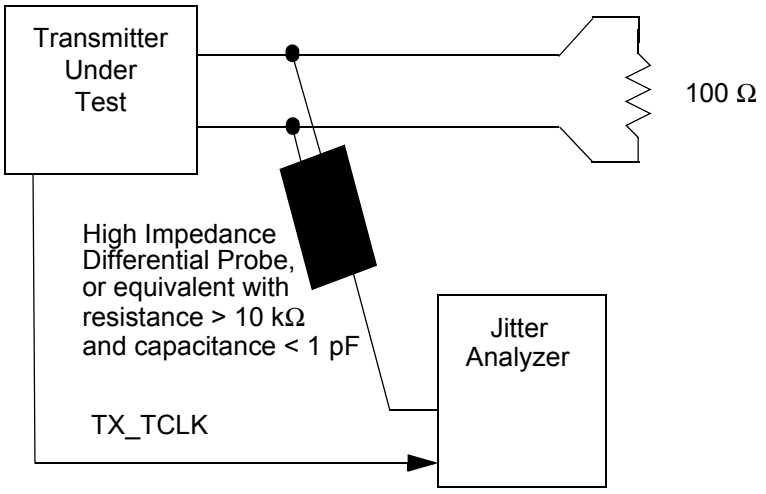



**Figure 96–20—Transmitter test fixture 1: Droop, Jitter**

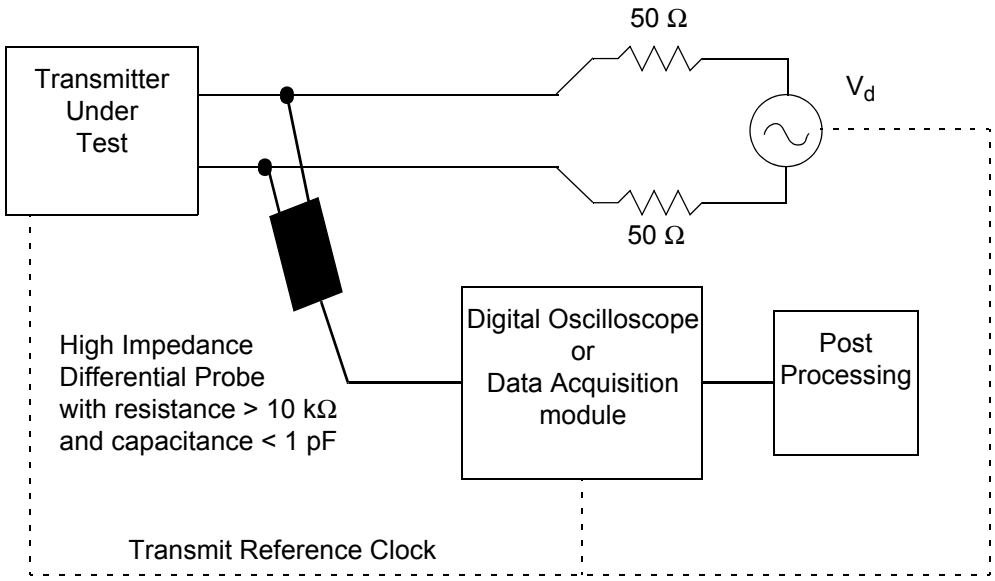



**Figure 96–21—Transmitter test fixture 2: Distortion**

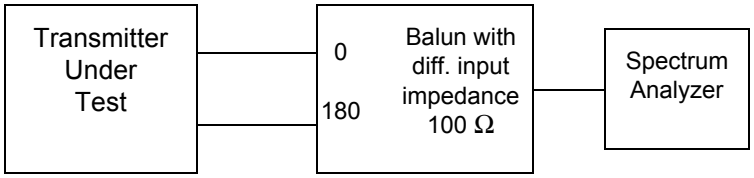



**Figure 96–22—Transmitter test fixture 3: PSD mask**

To allow for measurement of transmitted jitter in SLAVE modes, the PHY shall provide access to the symbol rate clock, TX_TCLK of 66.66$\overline{6}$ MHz, that times the transmitted symbols. The PHY shall provide a means to enable this clock output if it is not normally enabled.

In Figure 96–21, the disturbing signal, $V_d$, shall be a sine wave, synchronous with the transmit reference clock, with frequency given by one-sixth of the symbol rate and differential peak-to-peak voltage of 5.4 V.

The generator of the disturbing signal must have sufficient linearity and range so it does not introduce any appreciable distortion when connected to the transmitter output.

### 96.5.4 Transmitter electrical specifications

The PMA shall operate with AC coupling to the MDI. Where a load is not specified, the transmitter shall meet the requirements of this section with a 100 Ω (the value can vary within ±1% range) resistive differential load connected to the transmitter output.

### 96.5.4.1 Transmitter output droop

The test mode 1 output droop is illustrated in Figure 96–23. With the transmitter in test mode 1 and using the transmitter test fixture 1, the magnitude of both the positive and negative droop measured with respect to an initial peak value after the zero crossing and the value 500 ns after the initial peak, shall be less than 45%.

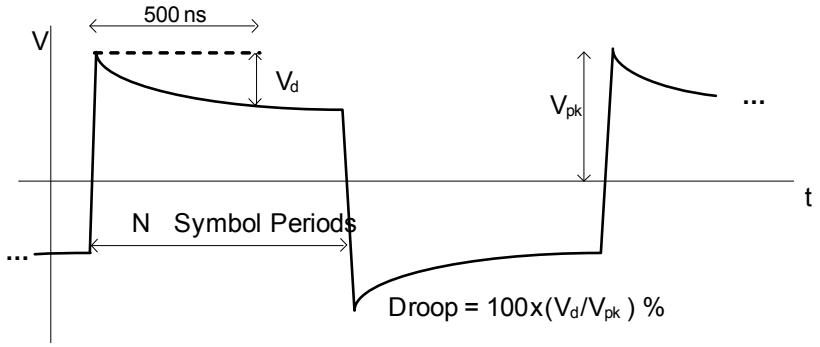



**Figure 96–23—Test mode 1 output (not to scale)**

### 96.5.4.2 Transmitter distortion

The transmitter distortion is measured by capturing the test mode 4 waveform using transmitter test fixture 2. The peak distortion is determined by sampling the differential signal output with the symbol rate clock at an arbitrary phase and processing a block of consecutive samples with MATLAB[5,6] code given below or equivalent. The peak distortion values, measured at a minimum of 10 equally-spaced phases of a single symbol period, shall be less than 15 mV.

The MATLAB code removes the disturbing signal from the measured data and computes the peak distortion. The code assumes the disturber signal and the data acquisition clock are frequency locked to the DUT transmit clock.

```
% 100BASE-T1 100 Mb/s single pair Ethernet PHY
% Test mode4: TX Distortion Post Processing
% Assumes frequency lock for PHY, data capturing clock and disturber

clear
Ns=2047; % Scrambler length
Nc=70;  % Canceller length

% Generate scrambler sequence
scr=ones(Ns,1);
for i=12:Ns
        scr(i)=mod(scr(i-11) + scr(i-9),2);
end
```

[5]Copyright release for MATLAB code: Users of this standard may freely reproduce the MATLAB code in this subclause so it can be used for its intended purpose.

[6]MATLAB is a registered trademark of The Mathworks, Inc.

```
% PAM3 assignment
tm4=scr.*(1-2*mod(circshift(scr,1) + circshift(scr,4),2));

% Test mode4 matrix
for i=1:Nc
        X0(i,:)=circshift(tm4,1-i);
end

% Read captured data file
% 200us long, 2GSample/sec, 8bits or more accuracy
fid=fopen('RawData.bin','r');
tx = fread(fid,inf,'int16');
fclose(fid);

% LPF 33 1/3 MHz, not required if data capture accuracy is 10 bits or more
[A,B]=butter(3,1/30,'low');
tx=filter(A,B,tx);
tx=tx(1:3:end); % decimate to 10x oversampling

% HPF 1.07 MHz
tx = filter([1,-1],[1,-exp(-2*pi/625)],tx);

% Select six periods, 10x oversampling, a row vector
tx=tx((1:6*Ns*10)+2e3)'; % removes HPF transient

% Disturber removal and integration (average) of six periods
TX=fft(tx);
tx=ifft(TX(1:6:end)); % averaged and disturber frequency rejected

% Level normalization
tx=tx/(max(tx)-min(tx))*2;

% Compute distortion for 10 phases
for n=1:10
        tx1=tx(n:10:end);

        % Align data and test pattern
        temp=xcorr(tx1,tm4);
        index=find(abs(temp)==max(abs(temp)));
        X=circshift(X0, [0, mod(index(1)+Nc-10,Ns)]);

        % Compute coefficients that minimize squared error in cyclic block
        coef=tx1/X;

        % Linear canceller
        err=tx1-coef*X;

        % Peak distortion
        dist(n) = max(abs(err));
end

% Print results in mV for 10 sampling phases
format bank
peakDistortion_mV = 1000*dist'
```

### 96.5.4.3 Transmitter timing jitter

When in test mode 2, the RMS (Root Mean Square) value of the MDI output jitter, $J_{TXOUT}$, relative to an unjittered reference shall be less than 50 ps. No high-pass filter is defined here for jitter measurement. The very low frequency components are expected to be filtered out in the setup via the memory size of the oscilloscope. For example, a digital sampling oscilloscope with 20 GSample/s with a 20 Mbytes sample memory size can only capture down to 1 kHz frequency.

When in the normal mode of operation as the SLAVE, jitter on the received signal reflects jitter on the TX_TCLK for SLAVE. Receiving valid signals from a compliant PHY operating as the MASTER with test port connected to the SLAVE, the RMS value of the SLAVE TX_TCLK jitter relative to an unjittered reference shall be less than 0.01 UI (Unit Interval) after the receiver is properly receiving the data. The test setup is shown in Figure 96–24.

For all jitter measurements, the RMS value is defined over an interval of not less than 1 ms and unjittered reference is a constant clock frequency extracted from each record of captured periodic wave. It is based on linear regression of frequency and phase that produces minimum Time Interval Error.

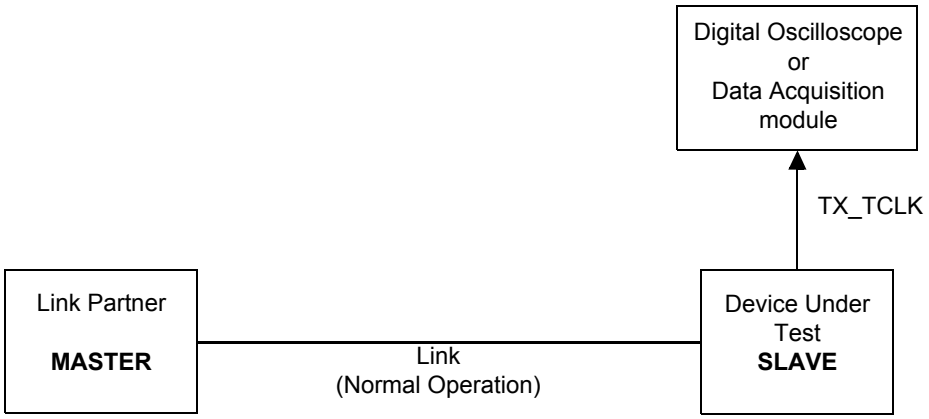



**Figure 96–24—Setup for slave transmit timing jitter in normal mode**

### 96.5.4.4 Transmitter power spectral density (PSD)

When test mode 5 is enabled, the PHY is forced to MASTER mode. In this mode, a pseudo-random sequence of ternary codes {–1, 0, +1}, which are mapped to 3 discrete differential signal levels, is transmitted.

In test mode 5, the power spectral density (PSD) of the transmitter, using the test fixture shown in Figure 96–22, shall be between the upper and lower bounds specified in the table below. The upper and lower limits are given in Equation (96–4) and Equation (96–5), and shown in Figure 96–25. The spectrum analyzer settings used for the PSD measurement should be: resolution bandwidth = 10 kHz, video bandwidth = 30 kHz, sweep time > 60 s, and RMS detector.

$$\text{Upper PSD}(f) = \begin{cases} -63.3 - 1.5 \times \frac{f-1}{19} \text{ dBm/Hz} & \text{for } 1 \text{ MHz} \le f < 20 \text{ MHz} \\ -64.8 - 3.7 \times \frac{f-20}{20} \text{ dBm/Hz} & \text{for } 20 \text{ MHz} \le f < 40 \text{ MHz} \\ -68.5 - 8.0 \times \frac{f-40}{17} \text{ dBm/Hz} & \text{for } 40 \text{ MHz} \le f < 57 \text{ MHz} \\ -76.5 \text{ dBm/Hz} & \text{for } 57 \text{ MHz} \le f \le 200 \text{ MHz} \end{cases} \quad (96\text{–}4)$$

$$\text{Lower PSD}(f) = \begin{cases} -70.9 - 4.9 \times \frac{f-1}{19} \text{ dBm/Hz} & \text{for } 1 \text{ MHz} \le f < 20 \text{ MHz} \\ -75.8 - 13.4 \times \frac{f-20}{20} \text{ dBm/Hz} & \text{for } 20 \text{ MHz} \le f < 40 \text{ MHz} \end{cases} \quad (96\text{–}5)$$

where

| | |
|---|---|
| Upper PSD($f$) | is the upper limit of the PSD of the transmitted signal frequency $f$ |
| Lower PSD($f$) | is the lower limit of the PSD of the transmitted signal frequency $f$ |
| $f$ | is the frequency in MHz |

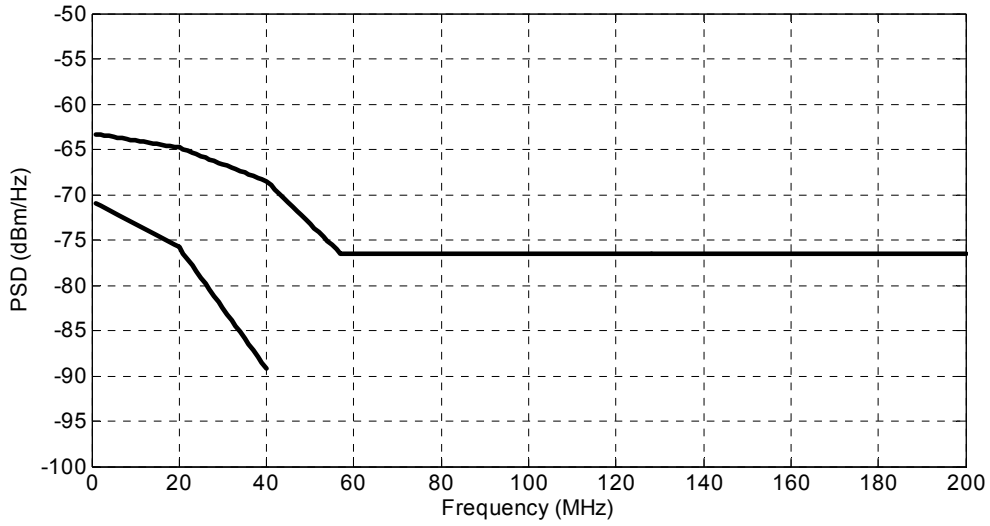



**Figure 96–25—PSD upper and lower limits**

### 96.5.4.5 Transmit clock frequency

The symbol transmission rate of the MASTER PHY shall be within the range 66.66$\overline{6}$ MBd ±100 ppm.

### 96.5.5 Receiver electrical specifications

The PMA shall meet the Receive function specified in PMA Receive function and the electrical specifications of this section. The single balanced twisted-pair cabling system used in test configurations shall be within the limits specified in 96.7.

#### 96.5.5.1 Receiver differential input signals

Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of Transmitter Electrical Specifications and have passed through a link specified in 96.7, shall be received with a bit error ratio less than $10^{-10}$.

#### 96.5.5.2 Receiver frequency tolerance

The receiver feature shall properly receive incoming data with a symbol rate within the range 66.66$\overline{6}$ MBd ±100 ppm

#### 96.5.5.3 Alien crosstalk noise rejection

This specification is provided to verify the DUT's tolerance to alien crosstalk noise using two separate tests. The first test is performed with a noise source consisting of a 100BASE-T1 compliant transmitter sending idle symbols. The level of the noise at the MDI is nominally 100 mV peak-to-peak. The second test is performed with a noise source consisting of a signal generator with Gaussian distribution, bandwith of 50 MHz and magnitude of –85 dBm/Hz. The receive DUT is connected to these noise sources through a resistive network, as shown in Figure 96–26, with a link segment as defined in 96.7. The noise is added at the MDI of the DUT. The BER shall be less than $10^{-10}$, and to satisfy this specification the frame error ratio is less than $10^{-7}$ for 125 octet packets measured at MAC/PLS service interface.

.

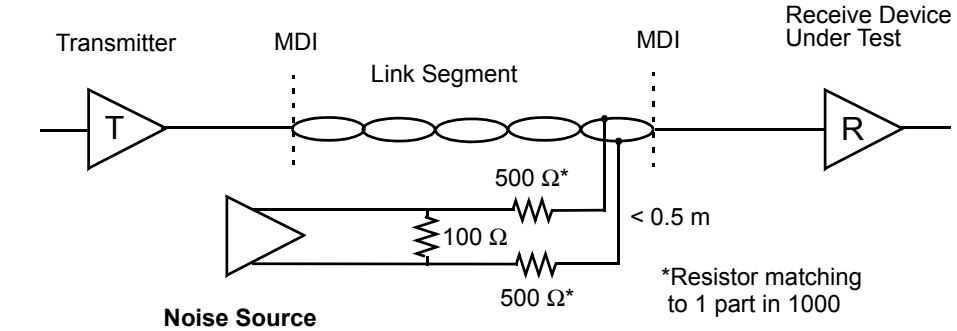



**Figure 96–26—Alien crosstalk noise rejection test setup**

### 96.5.6 Transmitter peak differential output

When measured with 100 Ω termination, transmit differential signal at MDI shall be less than 2.2 V peak-to-peak. This limit applies to all transmit modes including SEND_I and SEND_N modes.

### 96.5.7 PMA Local Loopback

The PMA local loopback function is optional. If supported, the PMA shall be placed in local loopback mode when the PMA local loopback bit in MDIO register 1.0.0, defined in 45.2.1.1, is set to a one. When the PHY is in the PMA local loopback mode the PMA Receive function utilizes the echo signals from the unterminated MDI and decodes these signals to pass the data back to the MII Receive interface. The data flow of the external loopback is shown in Figure 96–27.

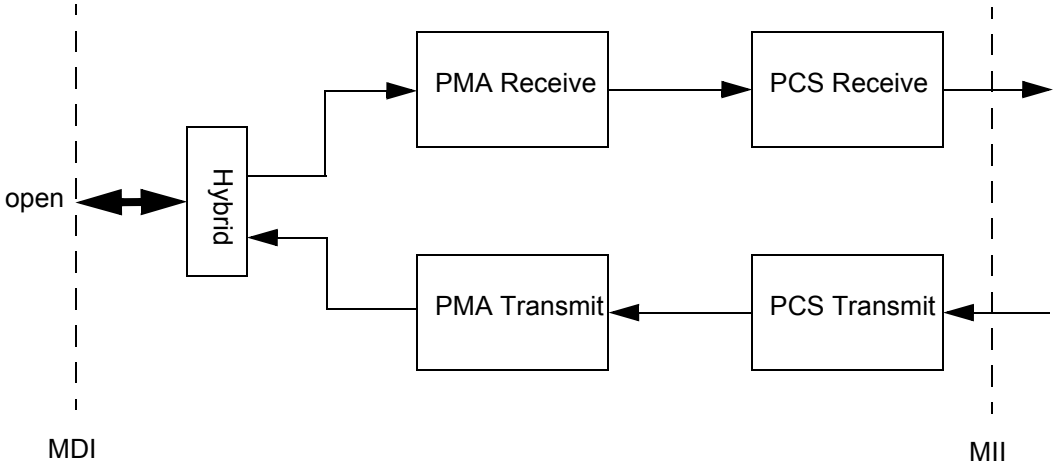



**Figure 96–27—PMA loopback data flow**

A MAC Client may compare the packets sent through the MII Transmit function to the packets received from the MII Receive function to validate the 100BASE-T1 PCS and PMA functions.

## 96.6 Management interface

100BASE-T1 uses the management interface as specified in Clause 45. The Clause 45 MDIO electrical interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent mechanism to access the registers is recommended.

### 96.6.1 MASTER-SLAVE configuration

MASTER-SLAVE assignment for each link configuration is necessary for establishing the timing control of each PHY. In 100BASE-T1, one PHY shall be configured as MASTER and one PHY shall be configured as SLAVE to operate. In the case where both PHYs are configured to be MASTER or both to be SLAVE, operation is undefined.

### 96.6.2 PHY-initialization

Both PHYs sharing a link segment are capable of being MASTER or SLAVE. A forced assignment scheme is employed depending on the physical deployment of the PHY within the application (e.g., at a multi-port bridge versus an end point). This process is conducted at the power-up or reset condition. The station management system manually configures the 100BASE-T1 PHY to be MASTER (before the link acquisition process starts) while the link partner defaults to SLAVE (un-managed).

### 96.6.3 PMA and PCS MDIO function mapping

The MDIO capability described in Clause 45 defines several variables that provide control and status information for and about the PMA and PCS. Mapping of MDIO register bits to PMA and PCS control/status variables is shown in Table 96–5.

**Table 96–5—MDIO register bit mapping reset and loopback control and link status variables**

| Register name | Register/bit number | Controls/status variable |
|---|---|---|
| PMA/PMD control 1 | 1.0.15 | pma_reset |
| PMA/PMD control 1 | 1.0.0 | PMA loopback |
| PCS control 1 | 3.0.15 | pcs_reset |
| PCS control 1 | 3.0.14 | PCS loopback |
| PMA/PMD status 1 | 1.1.2 | link_status |

## 96.7 Link segment characteristics

The 100BASE-T1 PHY is designed to operate over a single balanced twisted-pair cabling system. The single balanced twisted-pair cable supports an effective data rate of 100 Mb/s in each direction simultaneously. The link segment for a 100BASE-T1 PHY system is defined as in Figure 96–28, which consists of up to 15 m of single balanced twisted-pair cabling, with up to four in-line connectors and two mating connectors.

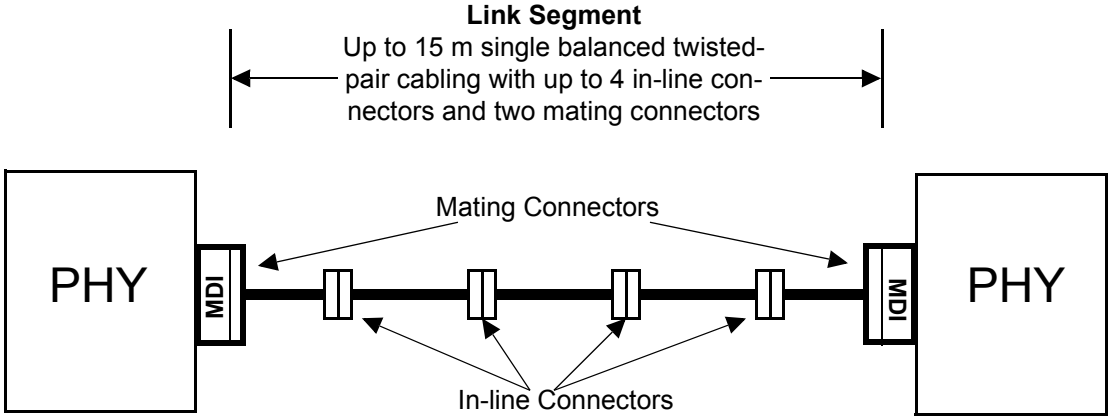



**Figure 96–28—Link segment definition**

### 96.7.1 Cabling system characteristics

The cabling system used in Figure 96–28 to support the 100BASE-T1 PHY is comprised of a single balanced twisted-pair cable up to 15 m in length with associated connectors, and with impedance in the range of 90 Ω to 110 Ω (nominal 100 Ω) to support a data rate of 100 Mb/s in each direction simultaneously.

The transmission parameters contained in this specification are chosen to enable reliable operation over a single balanced twisted-pair cable link segment. The transmission parameters of the link segment include

insertion loss, return loss, mode conversion loss, characteristic impedance, power sum alien near-end cross-talk, and power sum alien attenuation to crosstalk ratio far-end.

#### 96.7.1.1 Characteristic impedance

The characteristic impedance of the cable and any mated MDI connector shall be 100 Ω ±10% measured with TDR and rise-time set not slower than 700 ps.

#### 96.7.1.2 Insertion loss

The insertion loss of the link segment shown in Figure 96–28 when measured with a 100 Ω termination shall be less than that contained in Equation (96–6).

$$\text{Insertion loss}\ (f) < \begin{cases} 1.0 + 1.6 \times \sqrt{\frac{f-1}{9}} \ \text{dB} & \text{for} \ \ 1\ \text{MHz} \le f < 10\ \text{MHz} \\ 2.6 + 2.3 \times \sqrt{\frac{f-10}{23}} \ \text{dB} & \text{for} \ \ 10\ \text{MHz} \le f < 33\ \text{MHz} \\ 4.9 + 2.3 \times \sqrt{\frac{f-33}{33}} \ \text{dB} & \text{for} \ \ 33\ \text{MHz} \le f \le 66\ \text{MHz} \end{cases} \tag{96–6}$$

where

Insertion loss($f$) is the Insertion loss of the link segment at frequency $f$
$f$ is the frequency in MHz

#### 96.7.1.3 Return loss

The return loss of the link segment in Figure 96–28 shall meet or exceed Equation (96–7) for all frequencies from 1 MHz to 66 MHz (with 100 Ω reference impedance).

$$\text{Return loss}\ (f) \ge \begin{cases} 18 \ \text{dB} & \text{for} \ \ 1\ \text{MHz} \le f \le 20\ \text{MHz} \\ 18 - 10 \times \log_{10}\left(\frac{f}{20}\right) \ \text{dB} & \text{for} \ \ 20\ \text{MHz} \le f \le 66\ \text{MHz} \end{cases} \tag{96–7}$$

where

Return loss($f$) is the return loss of the link segment at frequency $f$
$f$ is the frequency in MHz

#### 96.7.1.4 Mode conversion loss

Mode conversion LCL and LCTL (Sdc11, Sdc22 and Sdc21, Sdc12) of the link segment defined in 96.7 shall meet or exceed the limit defined in Equation (96–8) for all frequencies from 1 MHz to 200 MHz.

$$\text{Mode conversion loss}(f) \geq \begin{cases} 43 \text{ dB} & \text{for } 1 \text{ MHz} \leq f \leq 33 \text{ MHz} \\ 43 - 20 \times \log_{10}\left(\frac{f}{33}\right) \text{ dB} & \text{for } 33 \text{ MHz} \leq f \leq 200 \text{ MHz} \end{cases} \quad (96\text{–}8)$$

where

Mode conversion loss($f$) is the common mode to differential mode conversion at frequency $f$
$f$ is the frequency in MHz

Alternatively, TCL and TCTL (Scd11, Scd22 and Scd21, Scd12) may be measured to pass the limit line.

### 96.7.1.5 Power sum alien near-end crosstalk (PSANEXT)

There is no FEXT or NEXT as 100BASE-T1 is a single pair solution. When multiple cable pairs are bundled, the alien XTALK (ANEXT and AFEXT) become interference sources. Since the transmitted symbols from the alien noise source in one cable are not available to another cable, cancellation cannot be done. When there are multiple pairs of cables bundled together, where all pairs carry 100 Mb/s links, then each duplex link is disturbed by neighboring links, degrading the signal quality on the victim pair. In order to limit the near-end crosstalk noise for a 5-around-1 cable bundle (up to 15 m length and up to four in-line connectors, equally spaced), the Power sum alien near-end crosstalk (PSANEXT) loss shall meet Equation (96–9).

$$\text{PSANEXT}\ (f) \geq 31.5 - 10 \times \log_{10}\left(\frac{f}{100}\right) \text{ dB} \quad \text{for } 1 \text{ MHz} \leq f \leq 100 \text{ MHz} \quad (96\text{–}9)$$

where

PSANEXT($f$) is the power sum alien near-end crosstalk loss at frequency $f$
$f$ is the frequency in MHz

### 96.7.1.6 Power sum alien attenuation to crosstalk ratio far-end (PSAACRF)

The Power sum alien attenuation to crosstalk ratio far-end (PSAACRF) for a 5-around-1 cable bundle (up to 15 m length and up to four in-line connectors, equally spaced) shall meet Equation (96–10).

$$\text{PSAACRF}(f) \geq 16.5 - 20 \times \log_{10}\left(\frac{f}{100}\right) \text{ dB} \quad \text{for } 1 \text{ MHz} \leq f \leq 100 \text{ MHz} \quad (96\text{–}10)$$

where

PSAACRF($f$) is the power sum alien attenuation to crosstalk ratio far-end at frequency $f$
$f$ is the frequency in MHz

### 96.7.2 Noise environment

In the 100BASE-T1 automotive environment, there are several types of noise sources:

a) Echo from the local transmitter on the same cable pair is caused by the hybrid function for bidirectional data transmission in the 100BASE-T1 duplex channel and by the impedance discontinuities in the link segment. Echo cancellation techniques, up to each PHY implementer, are generally used to achieve the objective BER level.

b) The typical background noise is mainly due to thermal noise. Thermal noise, with level roughly at –140 dBm/Hz, is not a critical contributor that would impact performance. 100BASE-T1 signaling allows a robust margin over a 15 m single balanced twisted-pair cabling channel to combat thermal noise.

c) PSANEXT as described in 96.7.1.5.

d) PSAACRF as described in 96.7.1.6.

## 96.8 MDI specification

This section defines the MDI for 100BASE-T1.

### 96.8.1 MDI connectors

The mechanical interface to the balanced cabling is a 2-pin connector or 2 pins of a multi-pin connector.

### 96.8.2 MDI electrical specification

The MDI connector mated with a specified single balanced twisted-pair cable connector shall meet the electrical requirements specified in 96.7.1, except for return loss, and 96.7.2.

#### 96.8.2.1 MDI return loss

The MDI return loss (RL) shall meet or exceed Equation (96–11) for all frequencies from 1 MHz to 66 MHz (with 100 Ω reference impedance) at all times when the PHY is transmitting data or control symbols.

$$\text{MDI return loss}\ (f) \geq \begin{cases} 20\ \text{dB} & \text{for}\ \ 1\ \text{MHz} \leq f \leq 30\ \text{MHz} \\ 20 - 20 \times \log_{10}\left(\frac{f}{30}\right)\ \text{dB} & \text{for}\ \ 30\ \text{MHz} \leq f \leq 66\ \text{MHz} \end{cases} \tag{96–11}$$

where

MDI return loss($f$) is the MDI return loss at frequency $f$
$f$ is the frequency in MHz

#### 96.8.2.2 MDI mode conversion loss

Mode conversion LCL (Sdc11) of the PHY measured at MDI shall meet or exceed the limit defined in Equation (96–12) for all frequencies from 1 MHz to 200 MHz.

$$\text{MDI mode conversion loss}(f) \geq \begin{cases} 50 \text{ dB} & \text{for } 1 \text{ MHz} \leq f \leq 33 \text{ MHz} \\ 50 - 20 \times \log_{10}\left(\frac{f}{33}\right) \text{ dB} & \text{for } 33 \text{ MHz} \leq f \leq 200 \text{ MHz} \end{cases} \quad (96\text{–}12)$$

where
MDI mode conversion loss($f$) is the MDI mode conversion loss at frequency $f$
$f$ is the frequency in MHz

Alternatively, TCL (Scd11) may be measured to pass the limit line.

### 96.8.3 MDI fault tolerance

The wire pair of the MDI shall, under all operating conditions, withstand without damage the application of short circuits of any wire to the other wire of the same pair or ground potential or positive voltages of up to 50 V dc with the source current limited to 150 mA, as per Table 96–6, for an indefinite period of time. Normal operation shall resume after the short circuit(s) is(are) removed.

The wire pair of the MDI shall also withstand without damage high-voltage transient noises and ESD per application requirements.

**Table 96–6—Connection fault**

| BI_DA+ | BI_DA- |
|---|---|
| No fault | No fault |
| BI_DA- | BI_DA+ |
| Ground | No fault |
| No fault | Ground |
| +50 V dc | No fault |
| No fault | +50 V dc |
| Ground | +50 V dc |
| +50 V dc | Ground |

## 96.9 Environmental specifications

### 96.9.1 General safety

All equipment subject to this clause shall conform to IEC 60950-1 (for IT and motor vehicle applications) and to ISO 26262 (for motor vehicle applications only, if required by the given application). All equipment subject to this clause may be additionally required to conform to any applicable local, state, or national standards or as agreed to between the customer and supplier.

### 96.9.2 Network safety

All cabling and equipment subject to this clause is expected to be mechanically and electrically secure in a professional manner. In automotive applications, all 100BASE-T1 cabling shall be routed in way to provide maximum protection by the motor vehicle sheet metal and structural components, following SAE J1292, ISO 14229, and ISO 15764.

#### 96.9.2.1 Environmental safety

In automotive applications, all equipment subject to this clause shall conform to the potential environmental stresses with respect to their mounting location, as defined in the following specifications:

a) General loads: ISO 16750-1
b) Electrical loads: ISO 16750-2, ISO 7637-2:2008, and ISO 8820-1
c) Mechanical loads: ISO 16750-3, ASTM D4728, and ISO 12103-1
d) Climatic loads: ISO 16750-4 and IEC 60068-2-1/27/30/38/52/64/78
e) Chemical loads: ISO 167540-5 and ISO 20653

Automotive environmental conditions are generally more severe than those found in many commercial environments. The targeted application environment(s) require careful analysis prior to implementation.

#### 96.9.2.2 Electromagnetic compatibility

A system integrating the 100BASE-T1 PHY shall comply with all applicable local and national codes. In addition, the system may need to comply with more stringent requirements as agreed upon between customer and supplier, for the limitation of electromagnetic interference. In automotive applications, a 100BASE-T1 PHY shall be tested according to CISPR 25 test methods, and shall meet the following motor vehicle EMC requirements:

a) Radiated/Conducted Emissions: IEC CISPR 25, IEC 61967-1/4, and IEC 61000-4-21
b) Radiated/Conducted Immunity: ISO 11452, IEC 62132-1/4, and IEC 61000-4-21
c) Electrostatic Discharge: ISO 10605 and IEC 61000-4-2/3
d) Electrical Disturbances: IEC 62215-3 and ISO 7637-2/3

Exact test setup and test limit values may be adapted to each specific application, subject to agreement between the customer and the supplier.

## 96.10 Delay constraints

Every 100BASE-T1 PHY associated with MII shall comply with the bit delay constraints for full duplex operation. The delay for the transmit path, from the MII input to the MDI, shall be less than 360 ns. The delay for the receive path, from the MDI to the MII output, shall be less than 960 ns.

## 96.11 Protocol implementation conformance statement (PICS) proforma for Clause 96, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T1[7]

### 96.11.1 Introduction

The supplier of a protocol implementation that is claimed to conform to Clause 96, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) and baseband medium, type 100BASE-T1, shall complete the following protocol implementation conformance statement (PICS) proforma.

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the PICS proforma, can be found in Clause 21.

### 96.11.2 Identification

#### 96.11.2.1 Implementation identification

| | |
|---|---|
| Supplier[1] | |
| Contact point for enquiries about the PICS[1] | |
| Implementation Name(s) and Version(s)[1,3] | |
| Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)[2] | |
| NOTE 1—Required for all implementations.<br>NOTE 2—May be completed as appropriate in meeting the requirements for the identification.<br>NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier's terminology (e.g., Type, Series, Model). | |

#### 96.11.2.2 Protocol summary

| | |
|---|---|
| Identification of protocol standard | IEEE Std 802.3bw-2015, Clause 96, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T1 |
| Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS | |
| Have any Exception items been required? No [ ] Yes [ ]<br>(See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3bw-2015.) | |

| | |
|---|---|
| Date of Statement | |

[7] *Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can be used for its intended purpose and may further publish the completed PICS.

### 96.11.3 Major capabilities/options

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| MII | PHY associated with MII | 96.1 | Interface is supported | O | Yes [ ]<br>No [ ] |
| PCS | 100BASE-T1 PCS | 96.3 | | M | Yes [ ] |
| PMA | 100BASE-T1 PMA | 96.4 | | M | Yes [ ] |
| *CHNL | Channel | 96.7 | Channel specification not applicable to a PHY manufacturer | O | Yes [ ]<br>No [ ] |
| *MD | MDIO Capability | 96.1 | Register and Interface supported | O | Yes [ ]<br>No [ ] |
| *AUTO | Automotive environment installation | | | O | Yes [ ]<br>No [ ] |

### 96.11.4 PICS proforma tables for Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 100BASE-T1

#### 96.11.4.1 Physical Coding Sublayer (PCS)

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| PCT1 | PCS Transmit state diagram | 96.3.3.2 | See Figure 96–7 | M | Yes [ ] |
| PCT2 | PCS data transmission enabling state diagram | 96.3.2 | See Figure 96–5 | M | Yes [ ] |
| PCT3 | tx_data<2:0>, tx_enable and tx_error | 96.3.3.1.1 | Be synchronized with PCS transmit clock pcs_txclk | M | Yes [ ] |
| PCT4 | TX_TCLK in MASTER mode | 96.3.3.1.1 | Derived from a local source in MASTER mode | M | Yes [ ] |
| PCT5 | TX_TCLK in SLAVE mode | 96.3.3.1.1 | Derived from the recovered clock in SLAVE mode. | M | Yes [ ] |
| PCT6 | Transmit data | 96.3.3.1.2 | Be converted into 3 bits (tx_data<2:0>) | M | Yes [ ] |
| PCT7 | Stuff bits | 96.3.3.1.2 | Append stuff bits to the end of a packet (1 or 2 bits) when the number of bits in a packet is not a multiple of 3 | M | Yes [ ] |
| PCT8 | symb_pair_timer | 96.3.3.2.3 | Generated synchronously with PCS transmit clock pcs_txclk | M | Yes [ ] |
| PCT9 | symb_timer | 96.3.3.2.3 | Generated synchronously with TX_TCLK. | M | Yes [ ] |

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| PCT10 | scrambler function | 96.3.3.3.1 | Conform to 40.3.1.3.1 and associated Figure 40-6 | M | Yes [ ] |
| PCT11 | $Sy_n$[2:0] | 96.3.3.3.2 | Conform to and be generated in accordance with the encoding rules in 40.3.1.3.2 and 40.3.1.3.3 | M | Yes [ ] |
| PCT12 | $Sc_n$[2:0] | 96.3.3.3.2 | Conform to and be generated in accordance with the encoding rules in 40.3.1.3.2 and 40.3.1.3.3 | M | Yes [ ] |
| PCT13 | $Sd_n$[2:0] | 96.3.3.3.4 | Generated as defined in 96.3.3.3.4 | M | Yes [ ] |
| PCT14 | $Sx_n$ | 96.3.3.3.8 | Generated as defined in 96.3.3.3.8 | M | Yes [ ] |

### 96.11.4.2 PCS Receive functions

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| PCR1 | PCS Receive state diagram | 96.3.4.1 | See Figure 96–10a and Figure 96–10b | M | Yes [ ] |
| PCR2 | rcv_max_timer | 96.3.4.1.3 | Expire 1.08 ms ±54 µs after being started | M | Yes [ ] |
| PCR3 | 3B/4B conversion in PCS Receive | 96.3.4.2 | The number of bits recevied in a packet is always a multiple of 3 that shall go through the process of 3B/4B conversion, discarding the residual 1 bit or 2 bits of data | M | Yes [ ] |
| PCR4 | PCS Receive | 96.3.4.2 | Set pcs_rx_er = TRUE when it receives bad ESDs, ERR_ESD, or bad SSDs | M | Yes [ ] |
| PCR5 | PCS receive descrambler polynomial | 96.3.4.3 | Conform to 40.3.1.4.2, with the exception that it applies to rx_data<2:0> | M | Yes [ ] |
| PCR6 | PCS receive automatic polarity detection | 96.3.4.4 | Invert its transmitted signals (TAn, TBn) | O | Yes [ ]<br>No [ ] |
| PCR7 | rx_data<2:0>, rx_enable and rx_error | 96.3.4.5 | Be synchronized with pcs_rx-clk | M | Yes [ ] |
| PCR8 | Residual bits | 96.3.4.5 | When the number of bits from the received data packet is not a multiple of four, those extra bits are discarded | M | Yes [ ] |
| PCR9 | RX_DV | 96.3.4.5 | Deasserted right after the last nibble is converted | M | Yes [ ] |
| PCR10 | False carrier error | 96.3.4.5 | Indicated on the MII after conversion | M | Yes [ ] |

### 96.11.4.3 PCS Loopback

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| PCL1 | PCS Loopback | 96.3.5 | The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14, defined in 45.2.3.1.2, is set to a one. | M | Yes [ ] |
| PCL2 | PCS Loopback function | 96.3.5 | The PCS shall accept data on the transmit path from the MII and return it on the receive path to the MII. | M | Yes [ ] |
| PCL3 | PHY receive circuitry isolation | 96.3.5 | The PHY receive circuitry shall be isolated from the network medium. | M | Yes [ ] |
| PCL4 | PHY transmit circuity isolation | 96.3.5 | The assertion of TX_EN at the MII shall not result in the transmission of data on the network medium. | M | Yes [ ] |

### 96.11.4.4 Physical Medium Attachment (PMA)

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| PMF1 | PMA reset function | 96.4.1 | Conform to 40.4.2.1, optional low power mode referenced in 36.2.5.1.3 not supported. | M | Yes [ ] |
| PMF2 | PMA transmit fault function | 96.4.2 | Be mapped to the transmit fault bit as specified in 45.2.1.7.4. | MDIO:M | Yes [ ]<br>N/A [ ] |
| PMF3 | PMA receive function | 96.4.3 | Contribute to the receive fault bit specified in 45.2.1.7.5. | MDIO:M | Yes [ ]<br>N/A [ ] |
| PMF4 | PHY Control function | 96.4.4 | See Figure 96–18. | M | Yes [ ] |
| PMF5 | Link Monitor function | 96.4.5 | See Figure 96–19. | M | Yes [ ] |
| PMF6 | Time from power_on = FALSE, transitioning to power_on = TRUE, to link_status=OK | 96.4.5 | Less than 100 ms. | M | Yes [ ] |
| PMF7 | maxwait_timer | 96.4.7.2 | Expire 200 ms ± 2 ms. | M | Yes [ ] |
| PMF8 | minwait_timer | 96.4.7.2 | Expire 1.8 µs ± 0.18 µs after being started. | M | Yes [ ] |
| PMF9 | stabilize_timer | 96.4.7.2 | Expire 1.8 µs ± 0.18 µs after being started. | M | Yes [ ] |

### 96.11.4.5 PMA electrical specifications

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| PME1 | Test modes | 96.5.2 | Provided to allow testing of the transmitter waveform, transmitter distortion, transmitter jitter, and transmitter droop | M | Yes [ ] |
| PME2 | These test modes shall only change the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation. | 96.5.2 | | M | Yes [ ] |
| PME3 | When test mode 1 is enabled, the PHY shall | 96.5.2 | Transmit N "+1" symbols followed by N "–1" symbols. The value of N (minimum of 34) shall be chosen such that N symbol period is greater than 500 ns | M | Yes [ ] |
| PME4 | When test mode 2 is enabled, the PHY shall | 96.5.2 | Transmit the data symbol sequence {+1, –1} repeatedly on its channel. The transmitter shall time the transmitted symbols from a $66.66\overline{6}$ MHz ± 100 ppm clock in the MASTER timing mode | M | Yes [ ] |
| PME5 | When test mode 4 is enabled, the PHY shall | 96.5.2 | Transmit the sequence of symbols generated by the scrambler generator polynomial, bit generation, and level mappings as defined in 96.5.2 | M | Yes [ ] |
| PME6 | The maximum-length shift register used to generate the sequences defined by this polynomial shall | 96.5.2 | Be updated once per symbol interval (15 ns) | M | Yes [ ] |
| PME7 | The transmitter shall | 96.5.2 | Time the transmitted symbols from a $66.66\overline{6}$ MHz ± 100 ppm clock in the MASTER timing mode | M | Yes [ ] |
| PME8 | When test mode 5 is enabled, the PHY shall | 96.5.2 | Transmit a pseudo-random sequence of PAM3 symbols, generated by the scrambling function described in 96.3.3.3 | M | Yes [ ] |
| PME9 | The tolerance of resistors shall be ± 0.1%. | 96.5.3 | | M | Yes [ ] |
| PME10 | The PHY shall provide access to the symbol rate clock, TX_TCLK of $66.66\overline{6}$ MHz, that times the transmitted symbols. | 96.5.3 | | M | Yes [ ] |

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| PME11 | The PHY shall provide a means to enable TX_TCLK output if it is not normally enabled. | 96.5.3 | | M | Yes [ ] |
| PME12 | The disturbing signal, $V_d$ | 96.5.3 | Be a sine wave, synchronous with the transmit reference clock, with frequency given by one-sixth of the symbol rate and differential peak-to-peak voltage of 5.4 V | M | Yes [ ] |
| PME13 | PMA | 96.5.4 | Operate with AC coupling to the MDI | M | Yes [ ] |
| PME14 | The positive and negative droop | 96.5.4.1 | Be less than 45% with respect to an initial peakvalue after the zero crossing and the value 500 ns after the initial peak | M | Yes [ ] |
| PME15 | The peak distortion values, measured at a minimum of 10 equally-spaced phases of a single symbol period | 96.5.4.2 | Be less than 15 mV | M | Yes [ ] |
| PME16 | When in test mode 2, the RMS value of the MDI output jitter, $J_{TXOUT}$, relative to an unjittered reference | 96.5.4.3 | Be less than 50 ps | M | Yes [ ] |
| PME17 | When in the normal mode of operation as the SLAVE, the RMS value of the SLAVE TX_TCLK jitter relative to an unjittered reference | 96.5.4.3 | Be less than 0.01 UI | M | Yes [ ] |
| PME18 | For all jitter measurements, the RMS value shall be measured over an interval of not less than 1 ms and unjittered reference is a constant clock frequency extracted from each record of captured periodic wave. | 96.5.4.3 | | M | Yes [ ] |
| PME19 | In test mode 5, PSD of the transmitter | 96.5.4.4 | Be between the upper and lower bounds given in Equation (96–4) and Equation (96–5), and shown in Figure 96–25 | M | Yes [ ] |
| PME20 | The symbol transmission rate of the MASTER PHY | 96.5.4.5 | Be within the range $66.66\overline{6}$ MBd ±100 ppm | M | Yes [ ] |

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| PME21 | Differential signals received at the MDI that were transmitted from a remote transmitter within the specifications of Transmitter Electrical Specifications and have passed through a link specified in 96.7, shall be received with a bit error ratio less than $10^{-10}$. | 96.5.5.1 | | M | Yes [ ] |
| PME22 | The receiver feature | 96.5.5.2 | Properly receive incoming data with a symbol rate within the range 66.66$\overline{6}$ MBd ±100 ppm | M | Yes [ ] |
| PME23 | The alien crosstalk test specified in 96.5.5.3 shall be satisfied by | 96.5.5.3 | A bit error ratio of less than $10^{-10}$ that is derived from a measured packet error ratio less than $10^{-7}$ for 125 octet packets. | M | Yes [ ] |
| PME24 | Transmit differential signal | 96.5.6 | Less than 2.2 V peak-to-peak when measured with a 100 Ω termination | M | Yes [ ] |
| PME25 | PMA Local Loopback | 96.5.7 | The PMA is placed in local loopback mode when the PMA local loopback bit in MDIO register 1.0.0, defined in 45.2.1.1, is set to a one | O | Yes [ ] No [ ] |

### 96.11.4.6 Management interface

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| MI1 | MASTER-SLAVE configuration | 96.6.1 | Each link configuration will have one PHY as MASTER one PHY configured as SLAVE | M | Yes [ ] |

### 96.11.4.7 Characteristics of the Link Segment

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| LKS1 | The characteristic impedance of the cable and any mated MDI connector | 96.7.1.1 | Be 100 Ω ±10% measured with TDR and rise-time set not slower than 700 ps | M | Yes [ ] |
| LKS2 | The insertion loss when measured with a 100 Ω termination | 96.7.1.2 | Be less than that contained in Equation (96–6) | M | Yes [ ] |
| LKS3 | The return loss (with 100 Ω reference impedance) | 96.7.1.3 | Meet or exceed Equation (96–7) for all frequencies from 1 MHz to 66 MHz | M | Yes [ ] |
| LKS4 | Mode conversion LCL and LCTL | 96.7.1.4 | Meet or exceed the limit defined in Equation (96–8) for all frequencies from 1 MHz to 200 MHz | M | Yes [ ] |
| LKS5 | The PSANEXT defined in 96.7.1.5 | 96.7.1.5 | Meet Equation (96–9) | M | Yes [ ] |
| LKS6 | The PSAACRF defined in 96.7.1.6 | 96.7.1.6 | Meet Equation (96–10) | M | Yes [ ] |

### 96.11.4.8 MDI Requirements

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| MDI1 | The MDI connector mated with a specified single balanced twisted-pair cable connector | 96.8.2 | Meet the electrical requirements specified in 96.7.1, except for return loss, and 96.7.2 | M | Yes [ ] |

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| MDI2 | The MDI return loss | 96.8.2.1 | Meet or exceed Equation (96–11) for all frequencies from 1 MHz to 66 MHz (with 100 Ω reference impedance) at all times when the PHY is transmitting data or control symbols | M | Yes [ ] |
| MDI3 | Mode conversion LCL | 96.8.2.2 | Meet or exceed the limit defined in Equation (96–12) for all frequencies from 1 MHz to 200 MHz | M | Yes [ ] |
| MDI4 | MDI wire pair short circuit | 96.8.3 | Under all operating conditions withstand without damage the application of short circuits of any wire to the other wire of the same pair or ground potential or positive voltages of up to 50 V dc with the source current limited to 150 mA, as per Table 96–6, for an indefinite period of time | M | Yes [ ] |
| MDI5 | Operation after short circuit | 96.8.3 | Resume normal operation | M | Yes [ ] |
| MDI6 | MDI wire pair transients and ESD | 96.8.3 | Under all operating conditions, withstand without damage high voltage transient noise and ESD per application requirements | M | Yes [ ] |

### 96.11.4.9 Environmental specifications

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| ES1 | Conformance to IEC 60950-1 | 96.9 | | M | Yes [ ] |
| ES2 | Application requires conformance to ISO 26262 | 96.9 | | AUTO:O | Yes [ ]<br>N/A[ ] |
| ES3 | Conformance to ISO 26262 | 96.9 | | AUTO*<br>ES2:M | Yes [ ]<br>N/A[ ] |
| ES4 | All 100BASE-T1 cabling | 96.9 | Be routed in way to provide maximum protection by the motor vehicle sheet metal and structural components, following SAE J1292, ISO 14229, and ISO 15764 | AUTO:<br>M | Yes [ ]<br>N/A[ ] |
| ES5 | Conform to the potential environmental stresses to their mounting locations, as defined in ISO 16750-1, ISO 16750-2, ISO 7637-2-2008, ISO 8820-1, ISO 16750-3, ASTM D4728, ISO 12103-1, ISO 16750-4, IEC 60068-2-1/27/30/38/52/64/78, ISO 167540-5, and ISO 20653 | 96.9 | | AUTO:<br>M | Yes [ ]<br>N/A[ ] |
| ES6 | Compliance with applicable local and national codes for the limitation of electromagnetic interference, or as agreed to between the customer and the supplier | 96.9 | | M | Yes [ ] |
| ES7 | Tested according to IEC CISPR 25 test methods defined to measure the PHY's EMC performance | 96.9 | | AUTO:<br>M | Yes [ ]<br>N/A[ ] |
| ES8 | Meet the following motor vehicle EMC requirements: CISPR 25, IEC 61967-1/4, IEC 61000-4-21, ISO 11452, IEC 62132-1/4, IEC 61000-4-21, ISO 10605, IEC 61000-4-2/3, IEC 62215-3, ISO 7637-2/3 | 96.9 | | AUTO:<br>M | Yes [ ]<br>N/A[ ] |

### 96.11.4.10 Delay constraints

| Item | Feature | Subclause | Value/Comment | Status | Support |
|---|---|---|---|---|---|
| DC1 | 100BASE-T1 PHY associated with MII | 96.10 | Comply with the bit delay constraints of full duplex operation | M | Yes [ ] |
| DC2 | Delay for the transmit path | 96.10 | Less than 360 ns | M | Yes [ ] |
| DC3 | Delay for the receive path | 96.10 | Less than 960 ns | M | Yes [ ] |

# Consensus

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