



6.976

High Speed Communication Circuits and Systems

Lecture 6

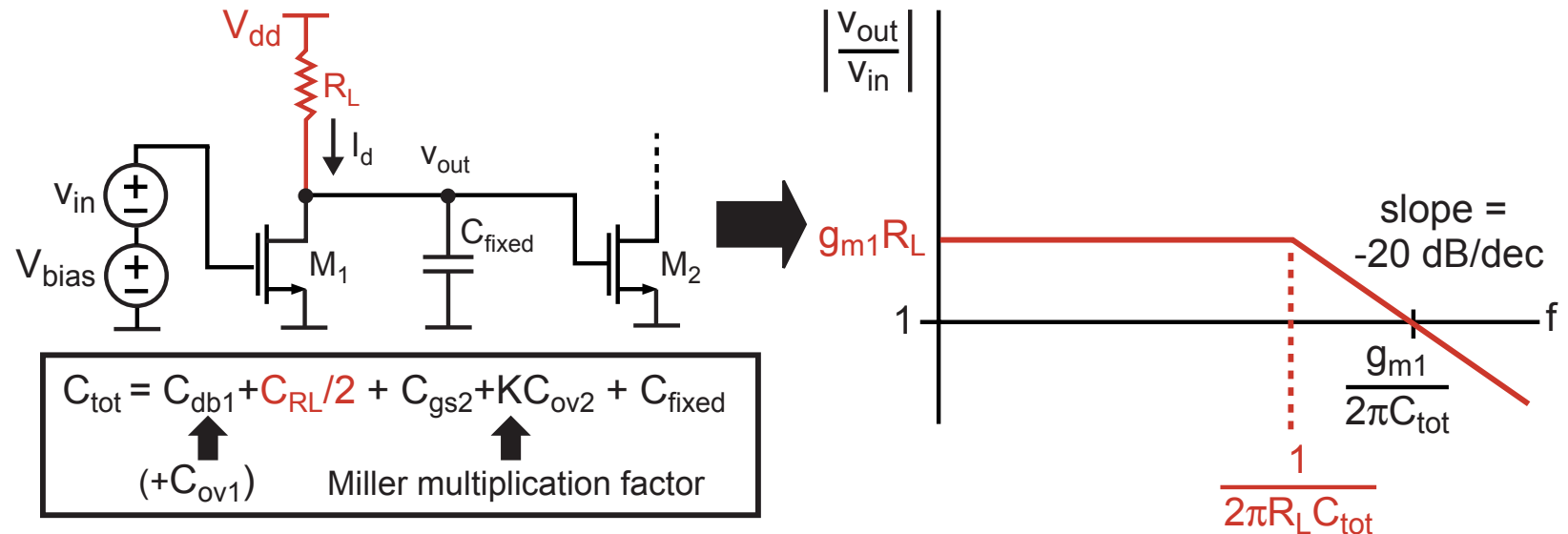
***Enhancement Techniques for Broadband Amplifiers,
Narrowband Amplifiers***

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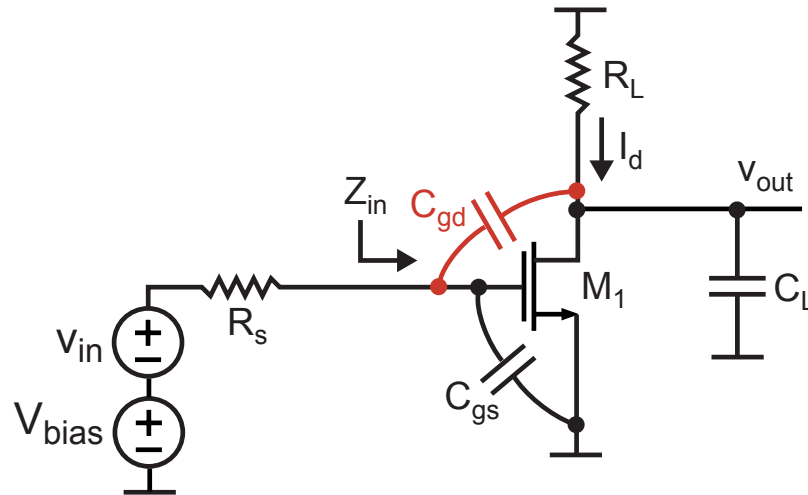
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Resistor Loaded Amplifier (Unsilicided Poly)



- We decided this was the fastest non-enhanced amplifier
 - Can we go faster? (i.e., can we enhance its bandwidth?)
- We will look at the following
 - Reduction of Miller effect on C_{gd}
 - Shunt, series, and zero peaking
 - Distributed amplification

Miller Effect on C_{gd} Is Significant



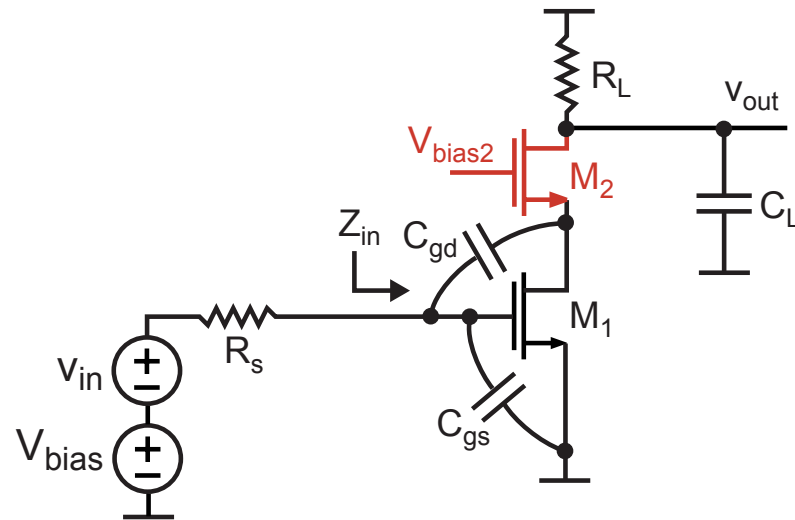
- C_{gd} is quite significant compared to C_{gs}
 - In 0.18μ CMOS, C_{gd} is about 45% the value of C_{gs}
- Input capacitance calculation

$$Z_{in} \approx \frac{1}{s(C_{gs} + C_{gd}(1 - A_v))} = \frac{1}{sC_{gs}(1 + C_{gd}/C_{gs}(1 + g_m R_L))}$$

- For 0.18μ CMOS, gain of 3, input cap is almost tripled over C_{gs} !

$$Z_{in} \approx \frac{1}{sC_{gs}(1 + 0.45(4))} = \frac{1}{sC_{gs}2.8}$$

Reduction of C_{gd} Impact Using a Cascode Device



- The cascode device lowers the gain seen by C_{gd} of M_1

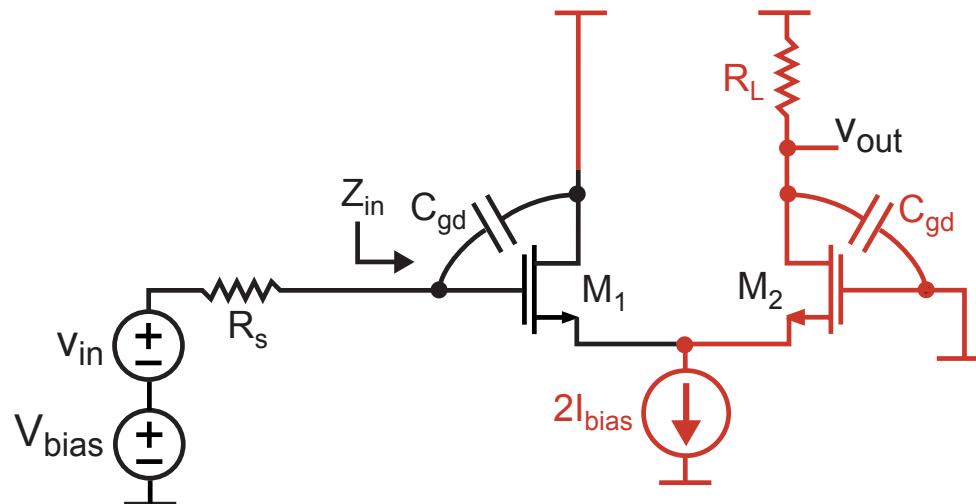
$$A_v \rightarrow g_{m1} \frac{1}{g_{m2}} \approx 1 \Rightarrow Z_{in} \approx \frac{1}{sC_{gs}(1 + C_{gd}/C_{gs}(2))}$$

- For 0.18m CMOS and gain of 3, impact of C_{gd} is reduced by 30%:

$$Z_{in} \approx \frac{1}{sC_{gs}1.9}$$

- Issue: cascoding lowers achievable voltage swing

Source-Coupled Amplifier

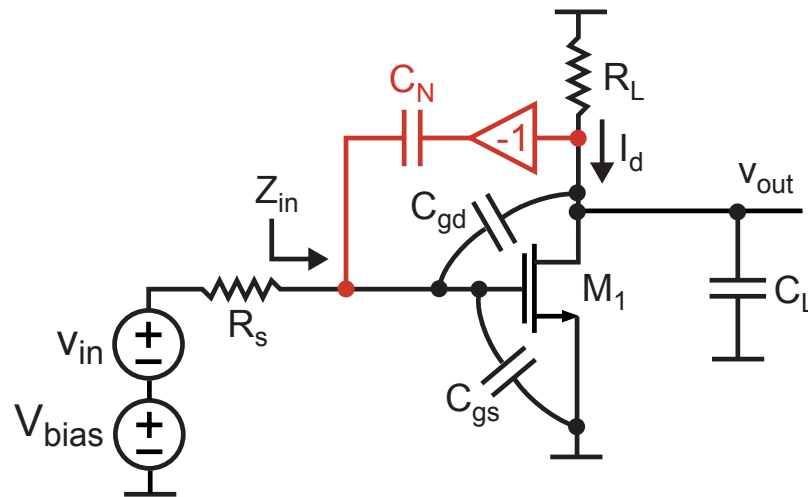


- **Remove impact of Miller effect by sending signal through source node rather than drain node**
 - C_{gd} not Miller multiplied AND impact of C_{gs} cut in half!

$$Z_{in} \approx \frac{1}{s(C_{gs}/2 + C_{gd})} \Rightarrow Z_{in} \approx \frac{1}{sC_{gs}0.95} \quad (0.18\mu \text{ CMOS})$$

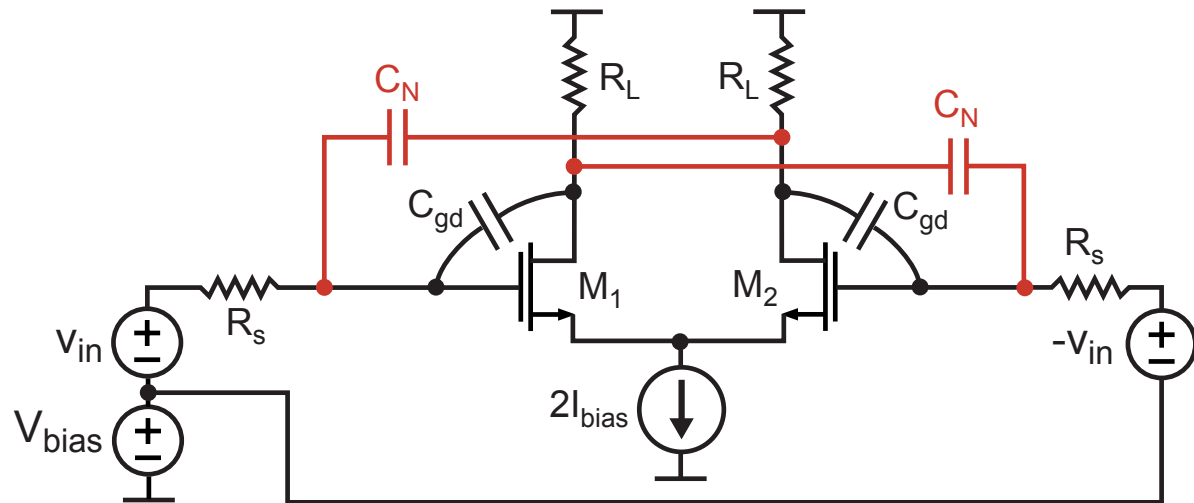
- **The bad news**
 - Signal has to go through source node (C_{sb} significant)
 - Power consumption doubled

Neutralization



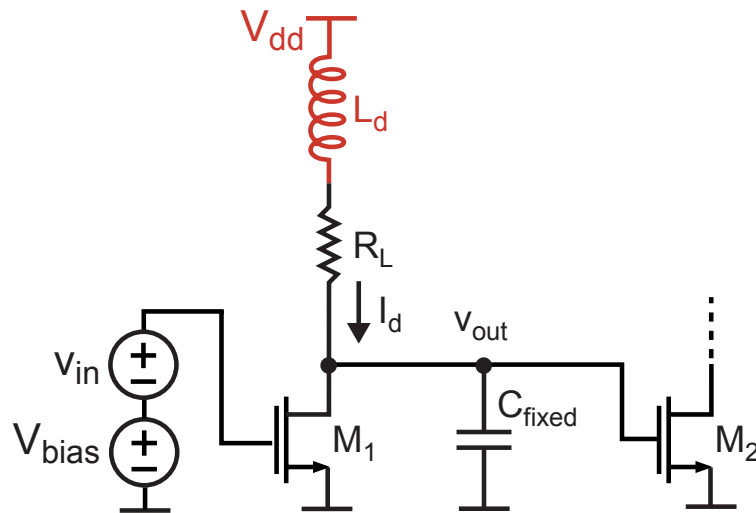
- Consider canceling the effect of C_{gd}
 - Choose $C_N = C_{gd}$
 - Charging of C_{gd} now provided by C_N
- Benefit: Impact of C_{gd} removed $\Rightarrow Z_{in} \approx \frac{1}{sC_{gs}}$
- Issues:
 - How do we create the inverting amplifier?
 - What happens if C_N is not precisely matched to C_{gd} ?

Practical Implementation of Neutralization



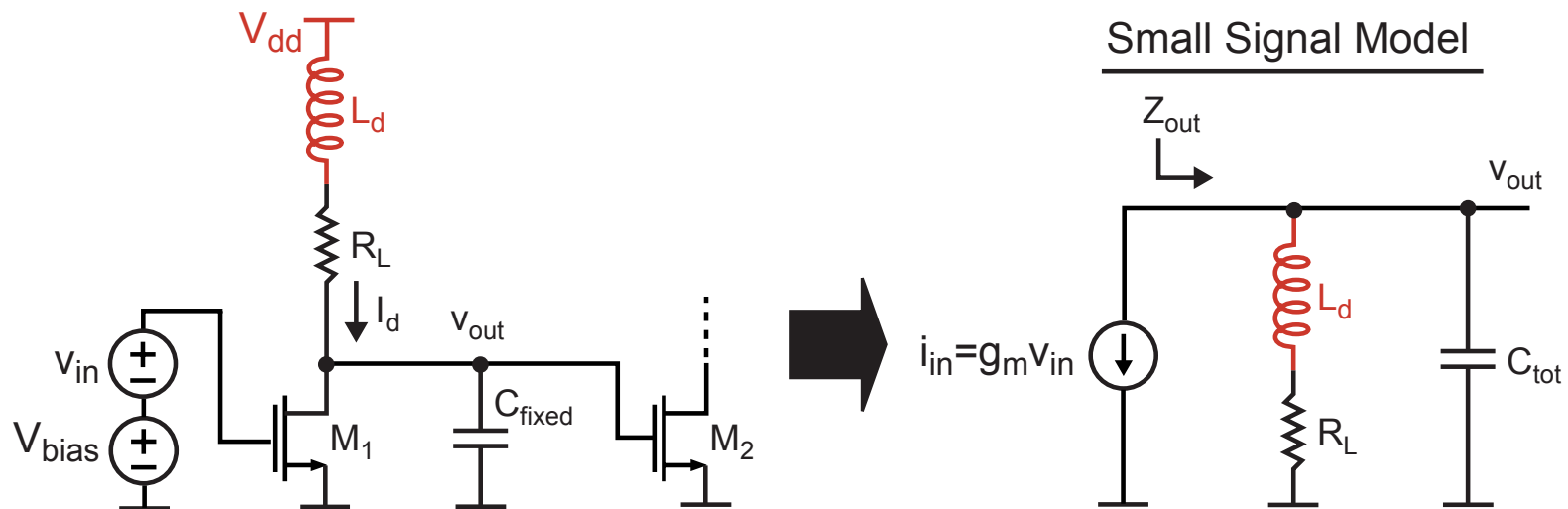
- Leverage differential signaling to create an inverted signal
- Only issue left is matching C_N to C_{gd}
 - Often use lateral metal caps for C_N (or CMOS transistor)
 - If C_N too low, residual influence of C_{gd}
 - If C_N too high, input impedance has inductive component
 - Causes peaking in frequency response
 - Often evaluate acceptable level of peaking using eye diagrams

Shunt-peaked Amplifier



- **Use inductor in load to extend bandwidth**
 - Often implemented as a spiral inductor
- **We can view impact of inductor in both time and frequency**
 - In frequency: peaking of frequency response
 - In time: delay of changing current in R_L
- **Issue – can we extend bandwidth without significant peaking?**

Shunt-peaked Amplifier - Analysis



■ Expression for gain

$$A_v = g_m Z_{out} = g_m [(sL_d + R_L) || 1/(sC_{tot})]$$

■ Parameterize with

$$= g_m R_L \frac{s(L_d/R_L) + 1}{s^2 L_d C_{tot} + s R_L C_{tot} + 1}$$

$$m = \frac{R_L C_{tot}}{\tau}, \quad \text{where } \tau = \frac{L_d}{R_L}$$

- Corresponds to ratio of RC to LR time constants

The Impact of Choosing Different Values of m – Part 1

- Parameterized gain expression

$$A_v = g_m R_L \frac{\tau s + 1}{s^2 \tau^2 m + s \tau m + 1}$$

- Comparison of new and old 3 dB frequencies

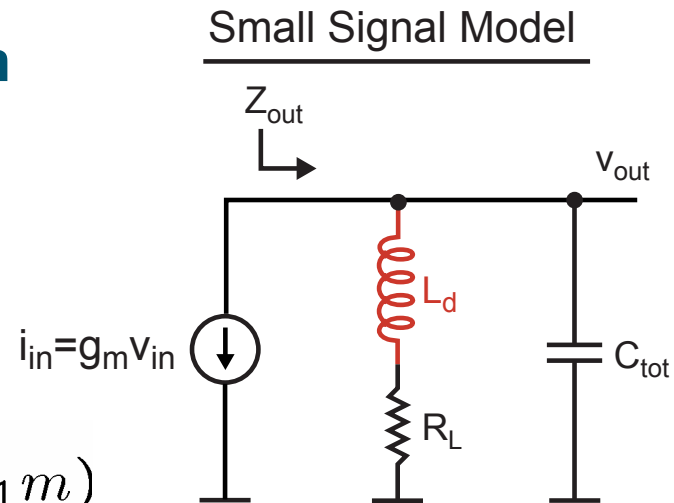
set: $s = j\omega$, $\omega_1 = \frac{1}{RC}$, $\tau = 1/(\omega_1 m)$

$$|A_v| = g_m R_L \left| \frac{j\omega/(\omega_1 m) + 1}{-(\omega/(\omega_1 m))^2 m + j\omega/(\omega_1 m)m + 1} \right|$$

define ω_2 as new 3 dB frequency, note that ω_1 is old one

$$\Rightarrow \left| \frac{j\omega_2/(\omega_1 m) + 1}{-(\omega_2/(\omega_1 m))^2 m + j\omega_2/\omega_1 + 1} \right| = \frac{1}{\sqrt{2}}$$

- Want to solve for ω_2/ω_1



The Impact of Choosing Different Values of m – Part 2

- From previous slide, we have

$$\left| \frac{jw_2/(w_1 m) + 1}{-(w_2/(w_1 m))^2 m + jw_2/w_1 + 1} \right| = \frac{1}{\sqrt{2}}$$

- After much algebra

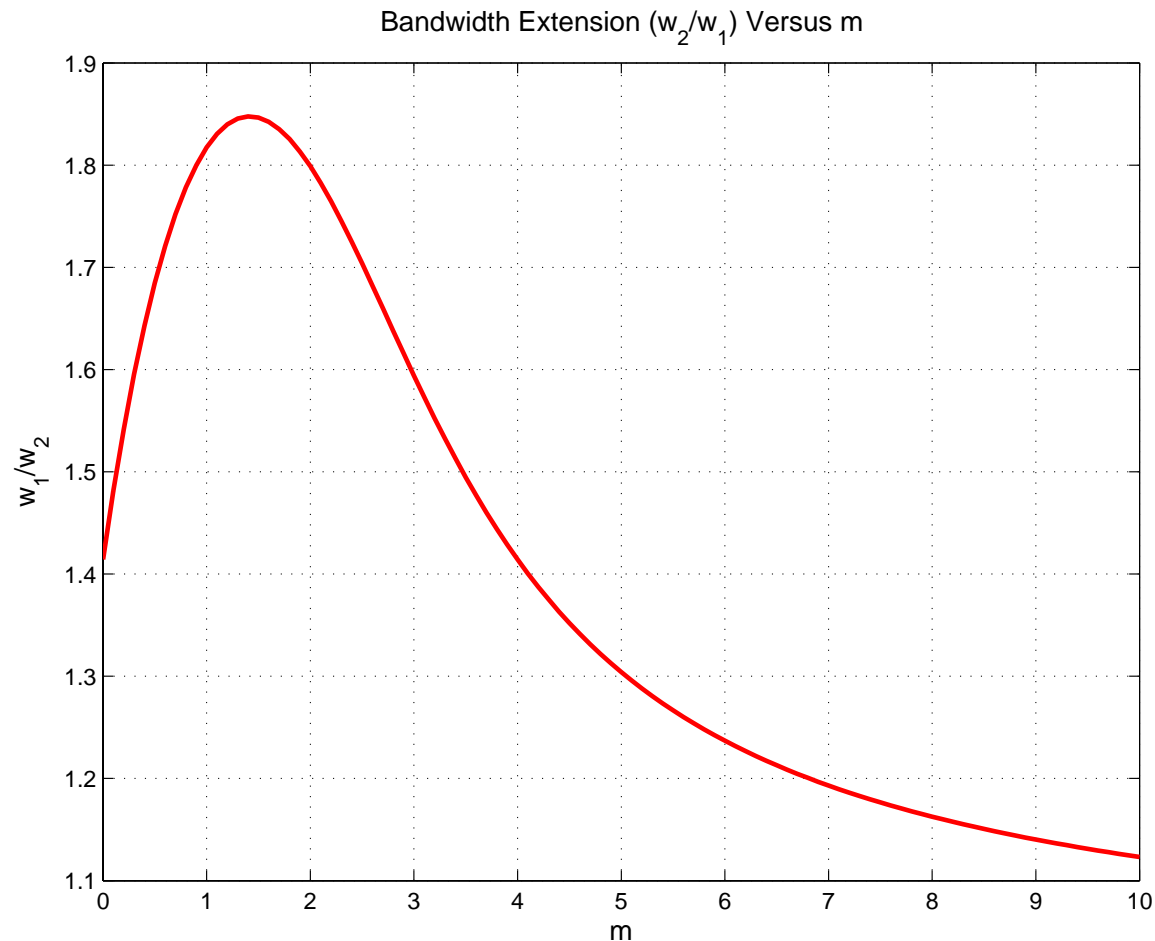
$$\frac{w_2}{w_1} = \sqrt{\left(-\frac{m^2}{2} + m + 1\right)} + \sqrt{\left(-\left(\frac{m^2}{2} + m + 1\right)^2 + m^2\right)}$$

- We see that m directly sets the amount of bandwidth extension!

- Once m is chosen, inductor value is

$$L_d = \frac{R_L^2 C_{tot}}{m}$$

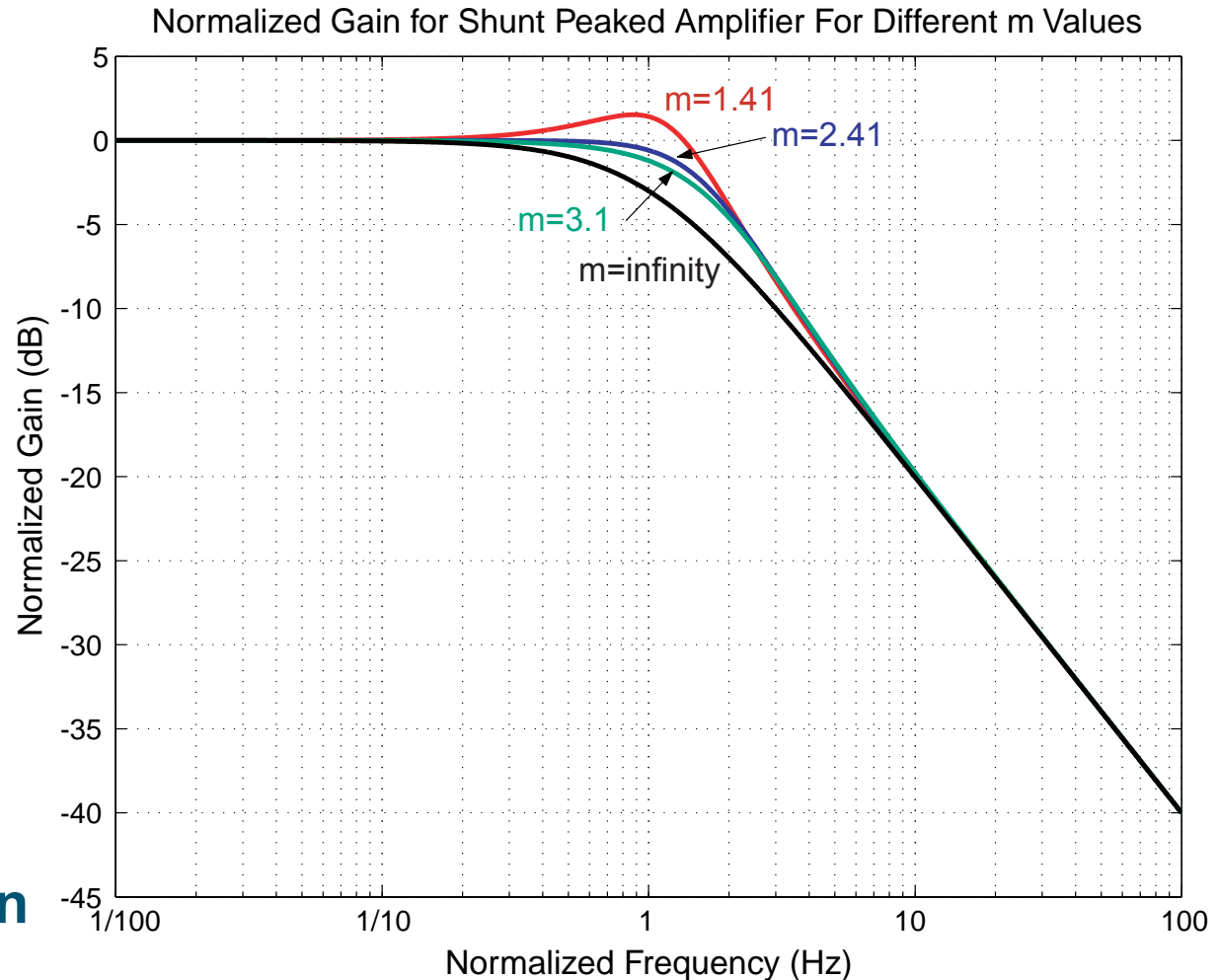
Plot of Bandwidth Extension Versus m



- Highest extension: $w_2/w_1 = 1.85$ at $m \approx 1.41$
 - However, peaking occurs!

Plot of Transfer Function Versus m

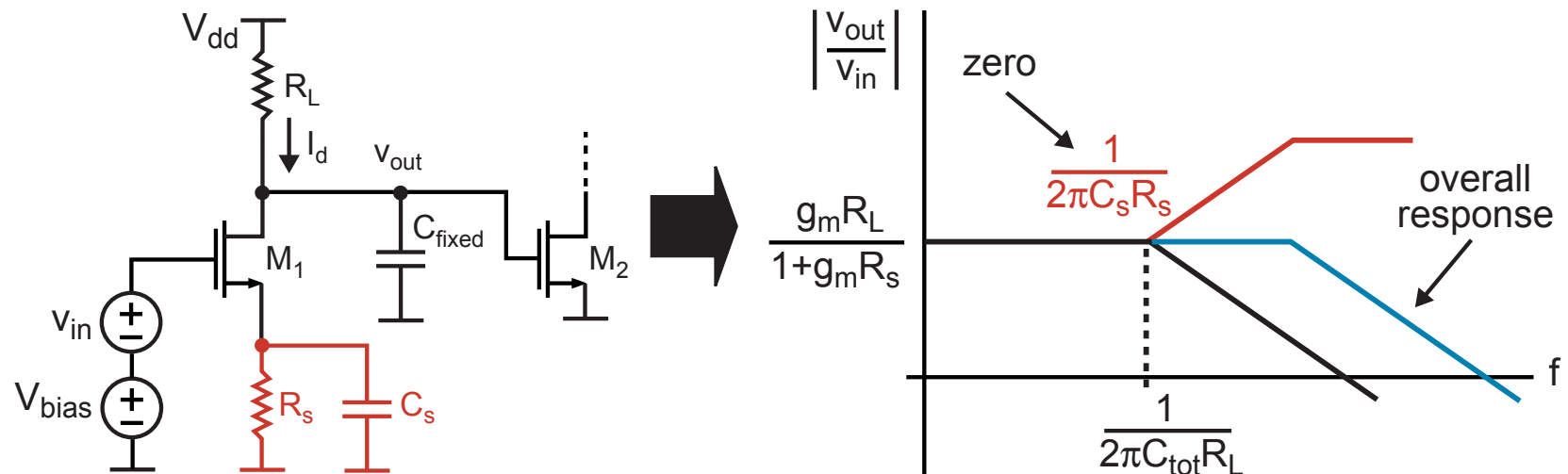
- **Maximum bandwidth:**
 $m = 1.41$
(extension = 1.85)
- **Maximally flat response:**
 $m = 2.41$
(extension = 1.72)
- **Best phase response:**
 $m = 3.1$
(extension = 1.6)
- **No peaking:**
 $m = \text{infinity}$
- **Eye diagrams often used to evaluate best m**



To Do

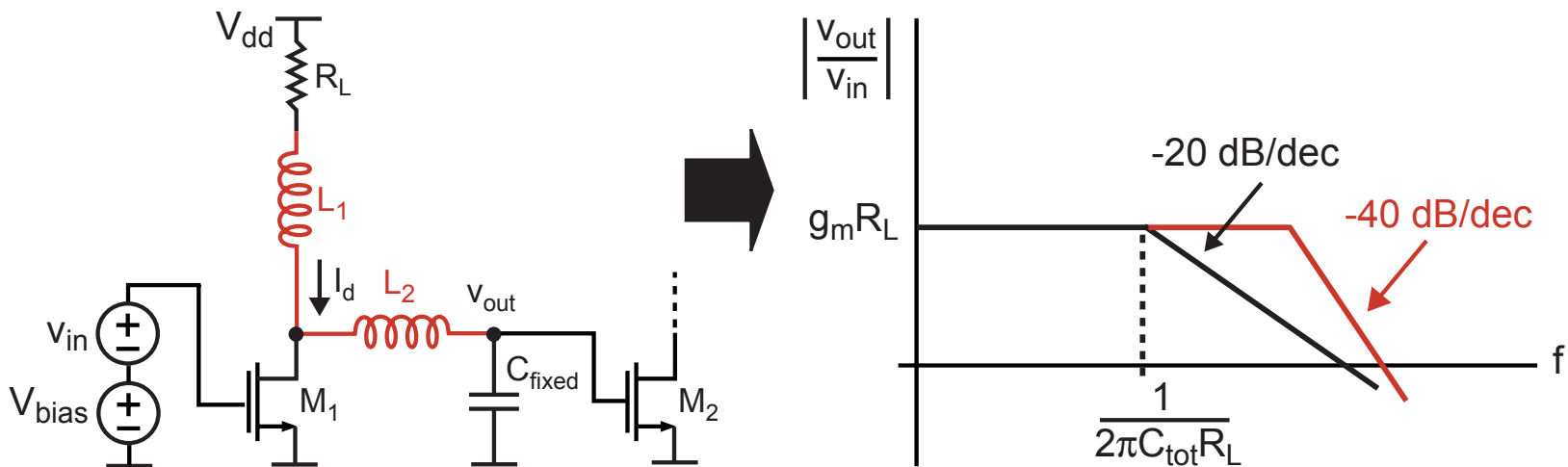
- Add eye diagrams

Zero-peaked Common Source Amplifier



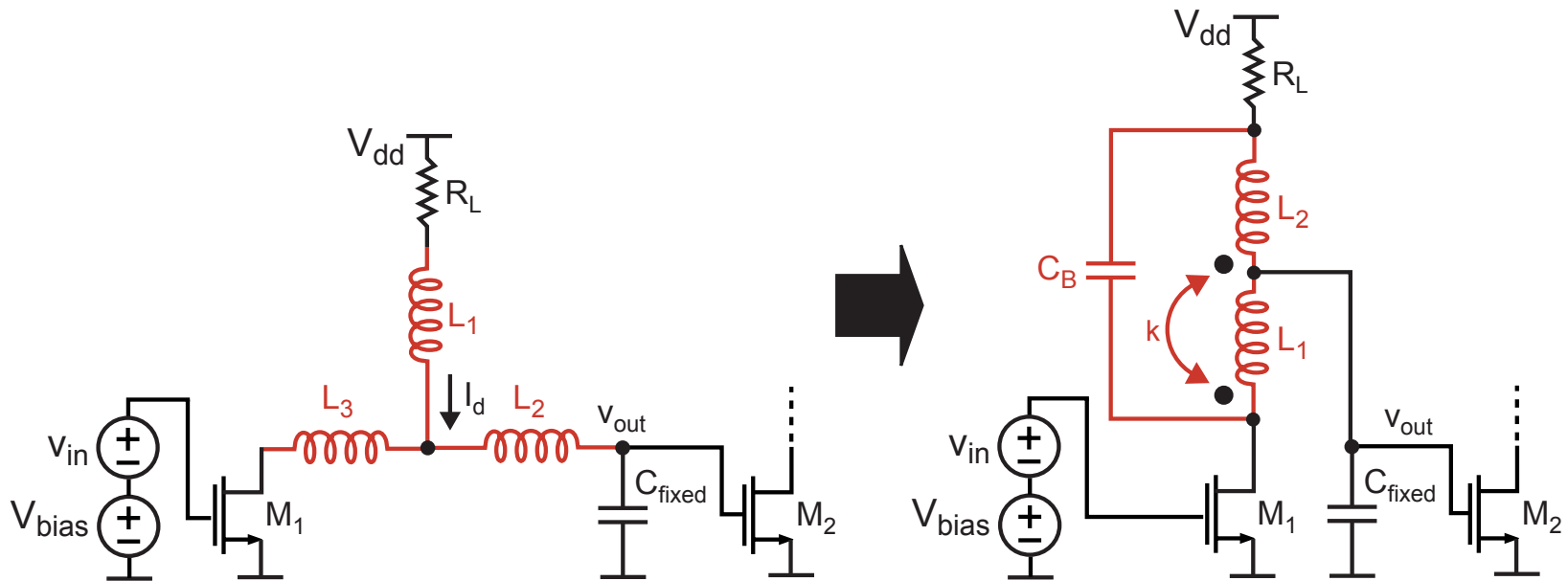
- Inductors are expensive with respect to die area
- We can instead achieve bandwidth extension with capacitor
 - ─ Idea: degenerate gain at low frequencies, remove degeneration at higher frequencies (i.e., create a zero)
- Issues:
 - ─ Must increase R_L to keep same gain (lowers pole)
 - ─ Lowers achievable gate voltage bias (lowers device f_t)

Back to Inductors – Shunt and Series Peaking



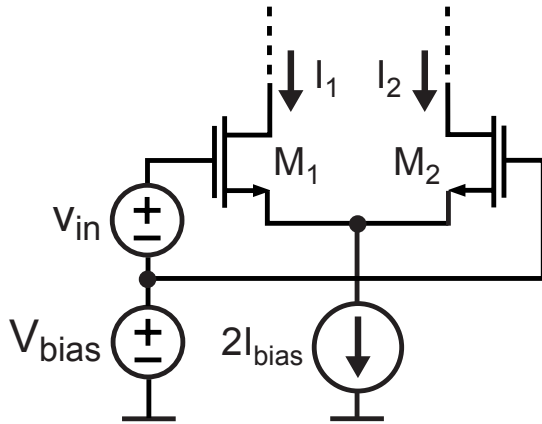
- **Combine shunt peaking with a series inductor**
 - Bandwidth extension by converting to a second order filter response
 - Can be designed for proper peaking
- **Increases delay of amplifier**

T-Coil Bandwidth Enhancement



- **Uses coupled inductors to realize T inductor network**
 - Works best if capacitance at drain of M_1 is much less than the capacitance being driven at the output load
- See Chap. 8 of Tom Lee's book (pp 187-191) for analysis
- See S. Galal, B. Ravazi, "10 Gb/s Limiting Amplifier and Laser/Modulator Driver in 0.18 μ CMOS", ISSCC 2003, pp 188-189 and "Broadband ESD Protection ...", pp. 182-183

Bandwidth Enhancement With f_t Doublers



- A MOS transistor has f_t calculated as

$$2\pi f_t = \frac{g_m}{C_{gs} + C_{gd}} \approx \frac{g_m}{C_{gs}}$$

- f_t doubler amplifiers attempt to increase the ratio of transconductance to capacitance

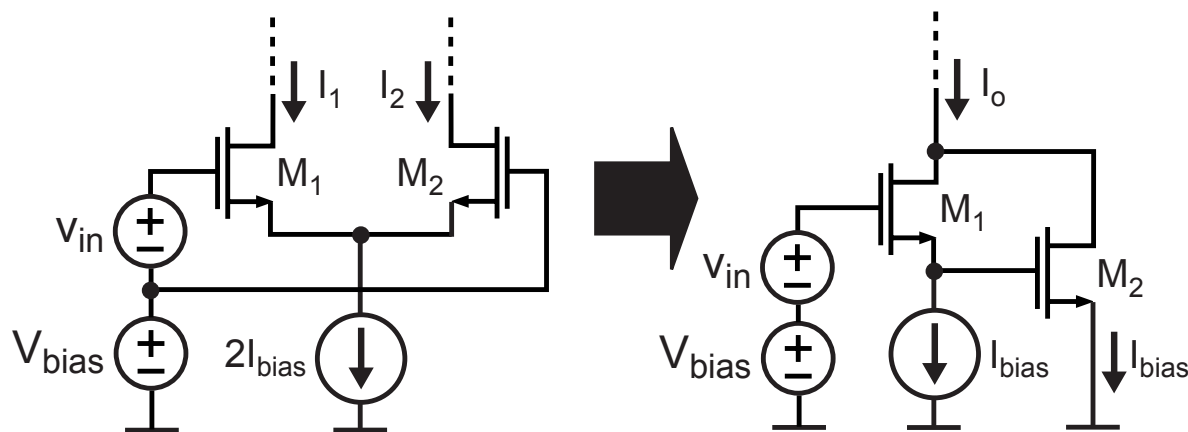
- We can make the argument that differential amplifiers are f_t doublers

- Capacitance seen by V_{in} for single-ended input: $C_{gs}/2$
- Difference in current:

$$i_2 - i_1 = \frac{v_{in}}{2}g_m - \left(-\frac{v_{in}}{2}\right)g_m = v_{in}g_m$$

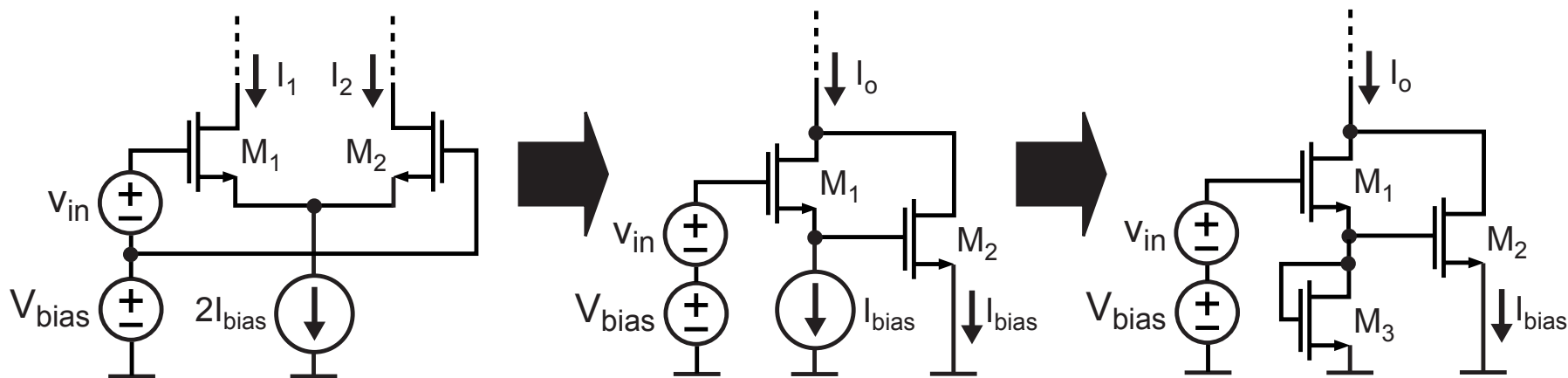
- Transconductance to Cap ratio is doubled: $\frac{2g_m}{C_{gs}}$

Creating a Single-Ended Output



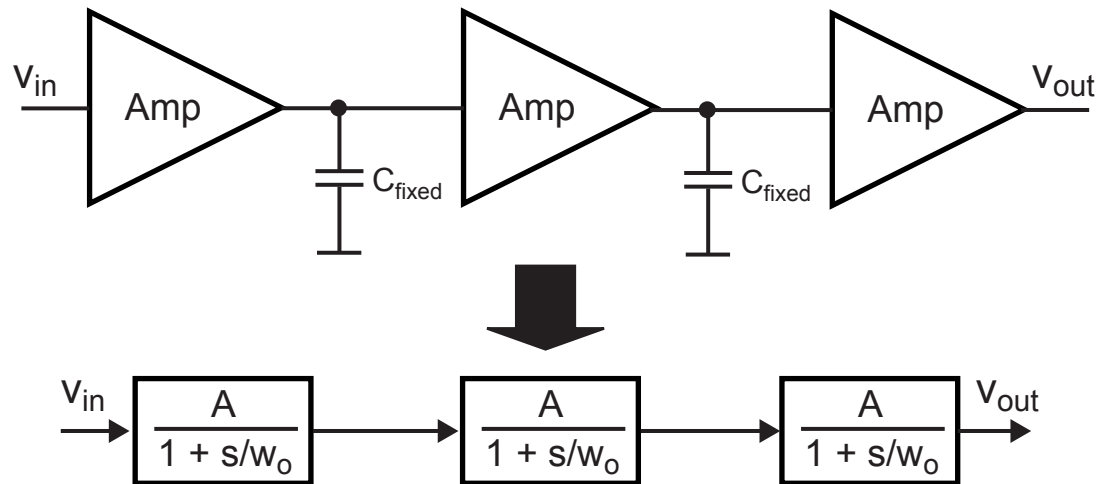
- **Input voltage is again dropped across two transistors**
 - Ratio given by voltage divider in capacitance
 - Ideally is $\frac{1}{2}$ of input voltage on C_{gs} of each device
- **Input voltage source sees the series combination of the capacitances of each device**
 - Ideally sees $\frac{1}{2}$ of the C_{gs} of M_1
- **Currents of each device add to ideally yield ratio:** $\frac{2g_m}{C_{gs}}$

Creating the Bias for M_2



- **Use current mirror for bias**
 - Inspired by bipolar circuits (see Tom Lee's book, page 198)
- **Need to set V_{bias} such that current through M_1 has the desired current of I_{bias}**
 - The current through M_2 will ideally match that of M_1
- **Problem: achievable bias voltage across M_1 (and M_2) is severely reduced (thereby reducing effective f_t of device)**
 - Do f_t doublers have an advantage in CMOS?

Increasing Gain-Bandwidth Product Through Cascading



- We can significantly increase the gain of an amplifier by cascading n stages

$$\Rightarrow \frac{v_{out}}{v_{in}} = \left(\frac{A}{1 + s/w_0} \right)^n = A^n \frac{1}{(1 + s/w_0)^n}$$

- Issue – bandwidth degrades, but by how much?

Analytical Derivation of Overall Bandwidth

- The overall 3-db bandwidth of the amplifier is where

$$\left| \frac{v_{out}}{v_{in}} \right| = \left| \frac{A}{1 + jw_1/w_o} \right|^n = \frac{A^n}{\sqrt{2}}$$

- w_1 is the overall bandwidth
- A and w_o are the gain and bandwidth of each section

$$\Rightarrow \left(\frac{A}{\sqrt{1 + (w_1/w_o)^2}} \right)^n = \frac{A^n}{\sqrt{2}}$$

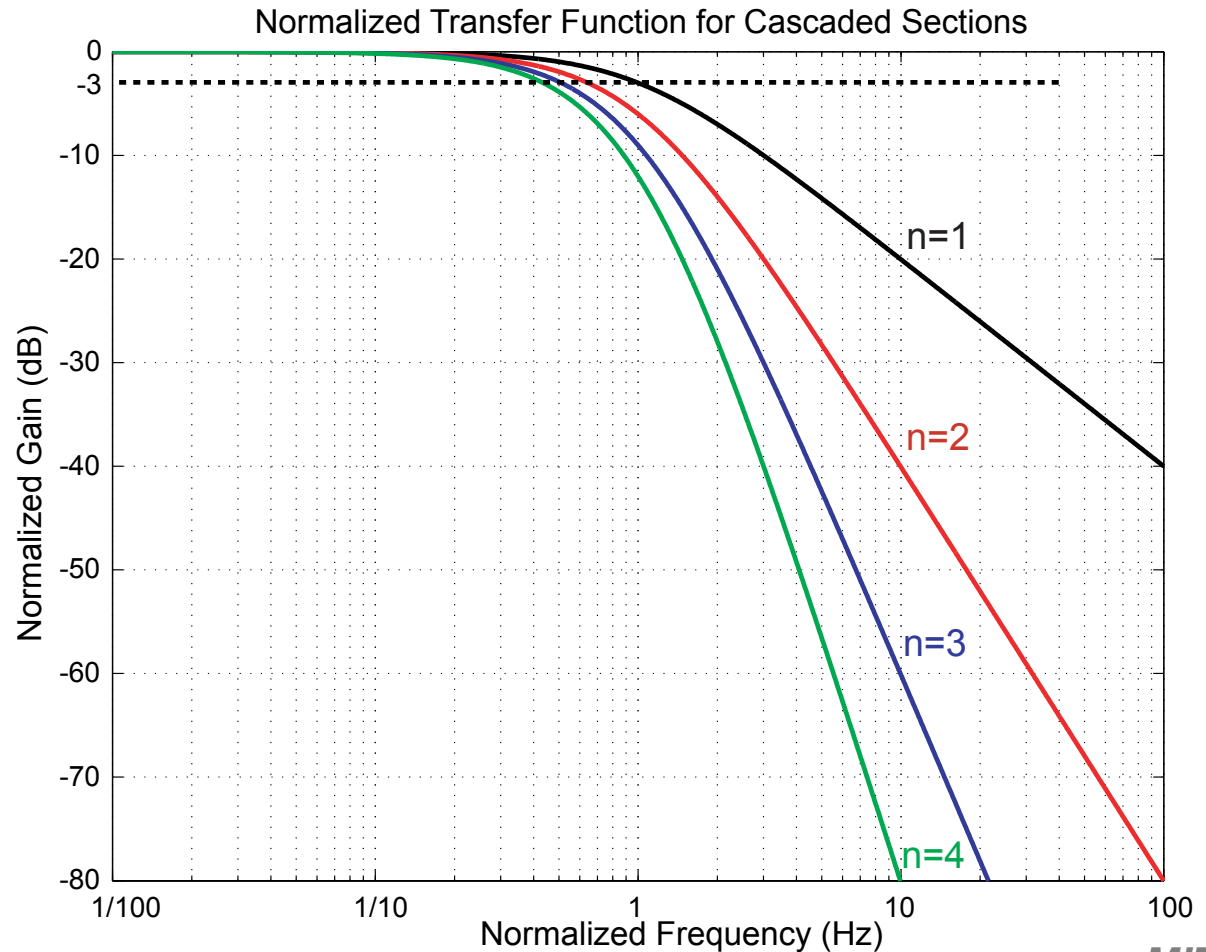
$$\Rightarrow \left(1 + (w_1/w_o)^2 \right)^n = 2$$

$$\Rightarrow w_1 = w_o \sqrt{2^{1/n} - 1}$$

- Bandwidth decreases much slower than gain increases!
 - Overall gain bandwidth product of amp can be increased!

Transfer Function for Cascaded Sections

$$H(f) = \left| \frac{1}{1 + j2\pi f} \right|^n$$



Choosing the Optimal Number of Stages

- To first order, there is a constant gain-bandwidth product for each stage

$$\Rightarrow Aw_o = w_t \Rightarrow w_o = w_t/A$$

- Increasing the bandwidth of each stage requires that we lower its gain
 - Can make up for lost gain by cascading more stages
- We found that the overall bandwidth is calculated as

$$w_1 = w_o \sqrt{2^{1/n} - 1} = \frac{w_t}{A} \sqrt{2^{1/n} - 1}$$

- Assume that we want to achieve gain G with n stages

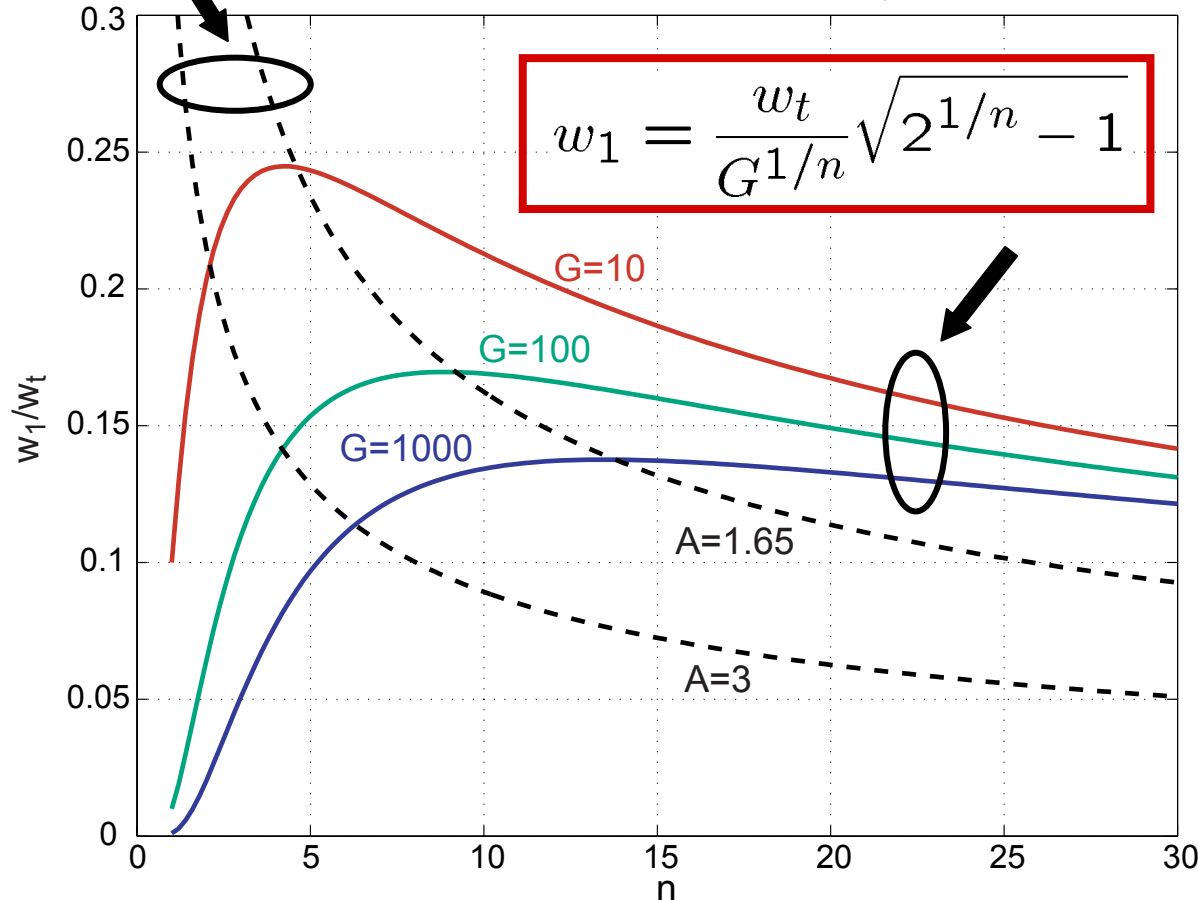
$$\Rightarrow A = G^{1/n} \Rightarrow w_1 = \frac{w_t}{G^{1/n}} \sqrt{2^{1/n} - 1}$$

- From this, Tom Lee finds optimum gain ≈ 1.65
 - See Tom Lee's book, pp 207-211

Achievable Bandwidth Versus G and n

$$\frac{w_t}{A} \sqrt{2^{1/n} - 1}$$

Achievable Bandwidth (Normalized to f_t)
Versus Gain (G) and Number of Stages (n)



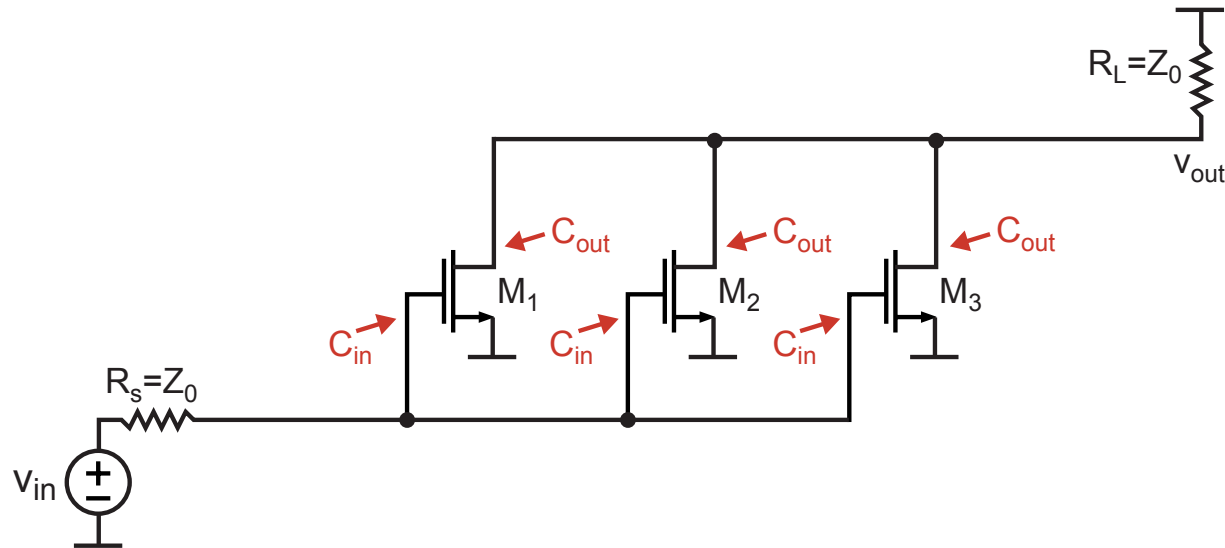
- Optimum gain per stage is about 1.65

- Note that gain per stage derived from plot as

$$A = G^{1/n}$$

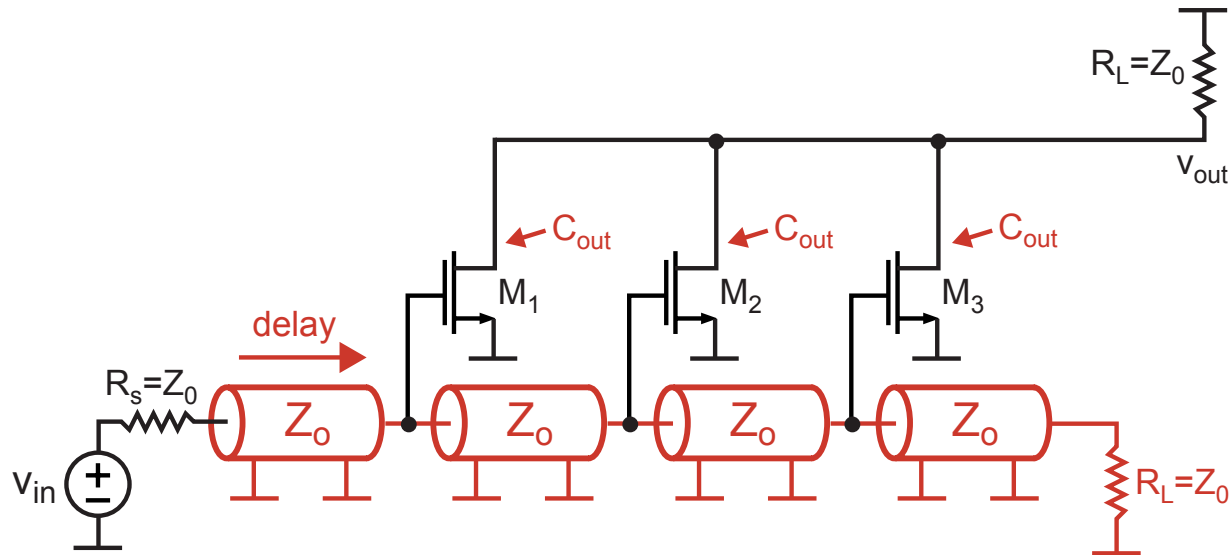
- Maximum is fairly soft, though
- Can dramatically lower power (and improve noise) by using larger gain per stage

Motivation for Distributed Amplifiers



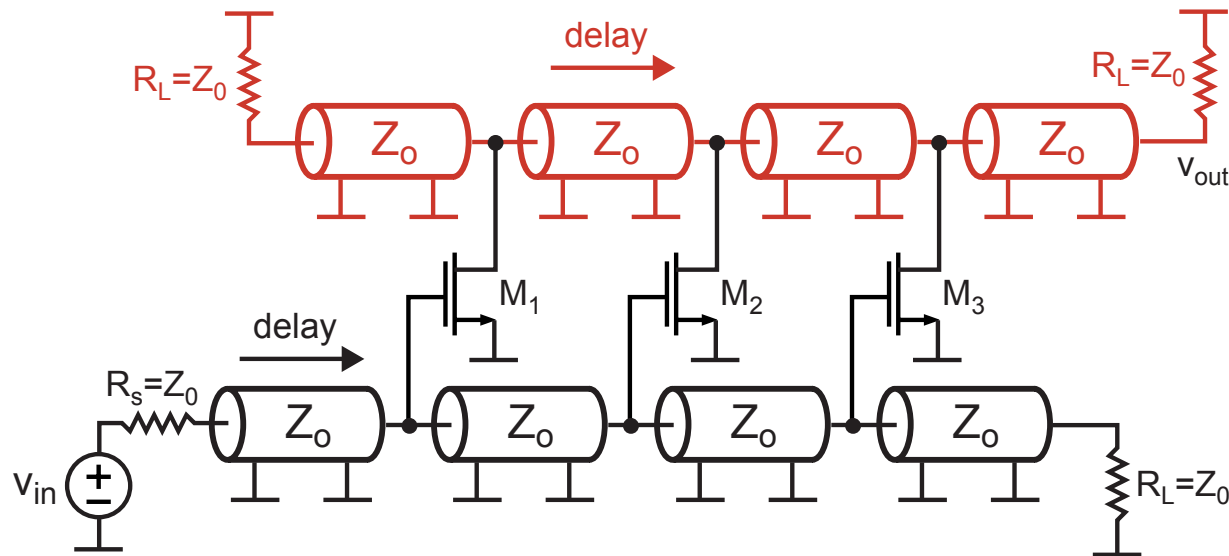
- We achieve higher gain for a given load resistance by increasing the device size (i.e., increase g_m)
 - Increased capacitance lowers bandwidth
 - We therefore get a relatively constant gain-bandwidth product
- We know that transmission lines have (ideally) infinite bandwidth, but can be modeled as LC networks
 - Can we lump device capacitances into transmission line?

Distributing the Input Capacitance



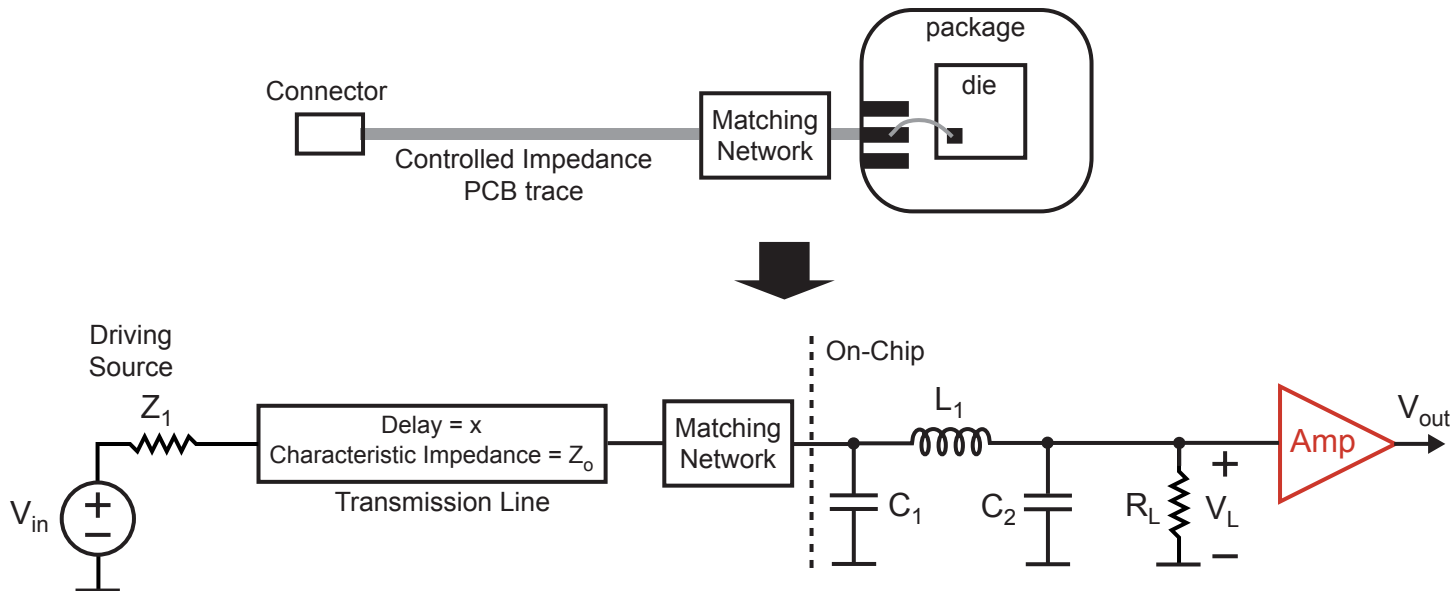
- **Lump input capacitance into LC network corresponding to a transmission line**
 - Signal ideally sees a real impedance rather than an RC lowpass
 - Often implemented as lumped networks such as T-coils
 - We can now trade delay (rather than bandwidth) for gain
- **Issue: outputs are delayed from each other**

Distributing the Output Capacitance



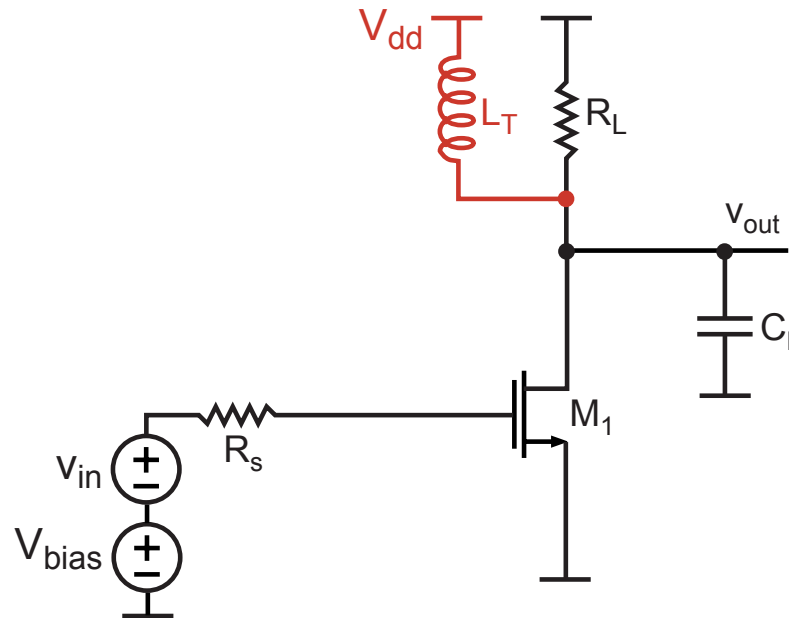
- Delay the outputs same amount as the inputs
 - Now the signals match up
 - We have also distributed the output capacitance!
- Benefit – high bandwidth
- Negatives – high power, poorer noise performance, expensive in terms of chip area
 - Each transistor gain is adding rather than multiplying!

Narrowband Amplifiers



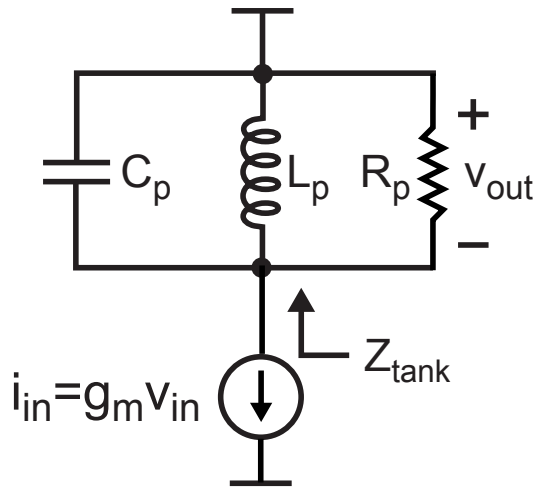
- **For wireless systems, we are interested in conditioning and amplifying the signal over a narrow frequency range centered at a high frequency**
 - Allows us to apply narrowband transformers to create matching networks
- **Can we take advantage of this fact when designing the amplifier?**

Tuned Amplifiers



- Put inductor in parallel across R_L to create bandpass filter
 - It will turn out that the gain-bandwidth product is roughly conserved regardless of the center frequency!
 - Assumes that center frequency (in Hz) $\ll f_t$
- To see this and other design issues, we must look closer at the parallel resonant circuit

Tuned Amp Transfer Function About Resonance



- **Amplifier transfer function**

$$\frac{v_{out}}{v_{in}} = g_m Z_{tank}(s) = \frac{g_m}{Y_{tank}(s)}$$

- **Note that conductances add in parallel**

$$Y_{tank}(s) = \frac{1}{R_p} + \frac{1}{sL_p} + sC_p$$

- **Evaluate at $s = j\omega$**

$$Y_{tank}(\omega) = \frac{1}{R_p} - \frac{j}{\omega L_p} + j\omega C_p = \frac{1}{R_p} + \frac{j}{\omega L_p} (-1 + \omega^2 L_p C_p)$$

- **Look at frequencies about resonance:** $\omega = \omega_o + \Delta\omega$

$$\begin{aligned} \Rightarrow Y_{tank}(\Delta\omega) &= \frac{1}{R_p} + \frac{j}{(\omega_o + \Delta\omega)L_p} (-1 + (\omega_o + \Delta\omega)^2 L_p C_p) \\ &\approx \frac{1}{R_p} + \frac{j}{\omega_o L_p} (-1 + \omega_o^2 L_p C_p + 2\omega_o \Delta\omega L_p C_p) \end{aligned}$$

Tuned Amp Transfer Function About Resonance (Cont.)

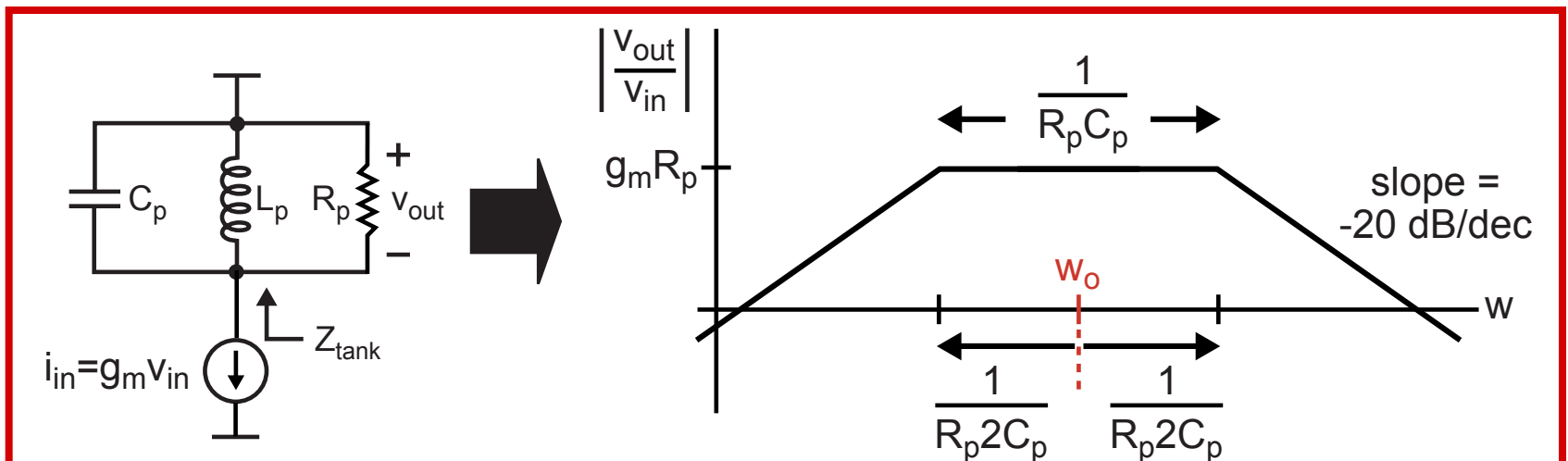
- From previous slide

$$Y_{tank}(\Delta\omega) \approx \frac{1}{R_p} + \frac{j}{\omega_o L_p} \left(\underbrace{-1 + \omega_o^2 L_p C_p}_{=0} + 2\omega_o \Delta\omega L_p C_p \right)$$

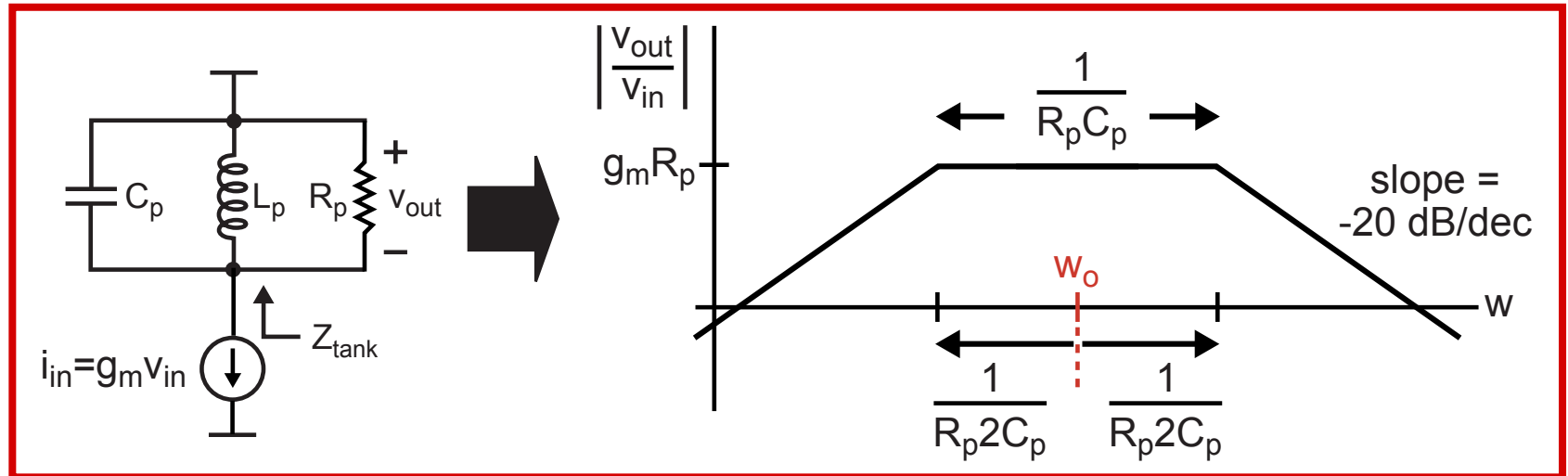
$$\approx \frac{1}{R_p} + \frac{j}{\omega_o L_p} (2\omega_o \Delta\omega L_p C_p) = \frac{1}{R_p} + j\Delta\omega 2C_p$$

- Simplifies to RC circuit for bandwidth calculation!

$$Z_{tank}(\Delta\omega) \approx R_p \parallel \frac{1}{j\Delta\omega 2C_p}$$



Gain-Bandwidth Product for Tuned Amplifiers

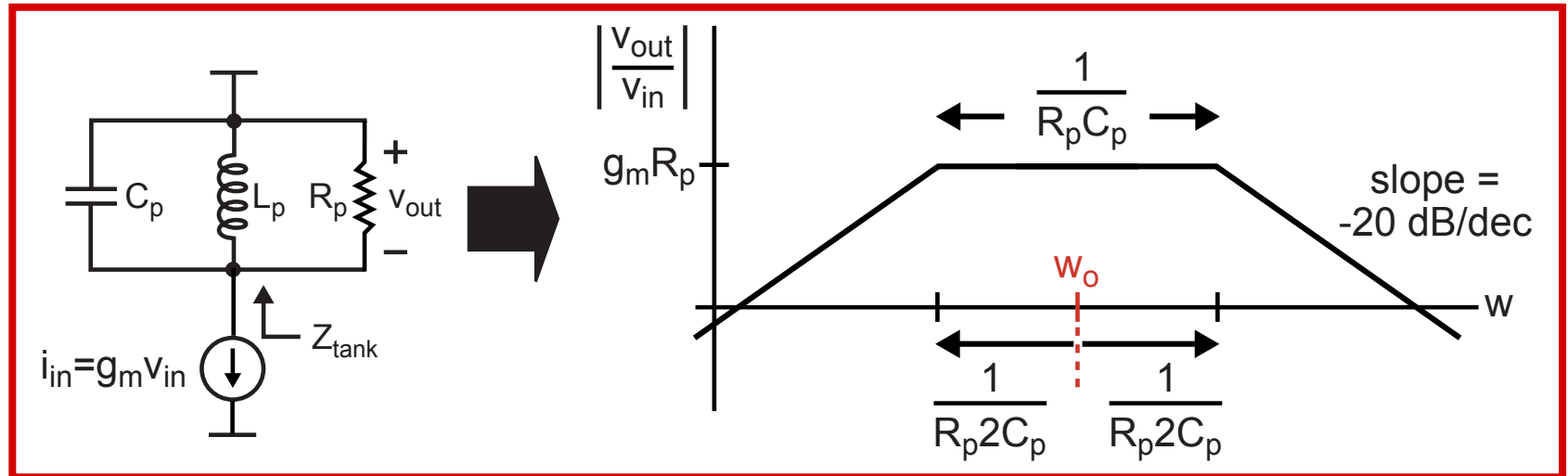


- The gain-bandwidth product:

$$G \cdot BW = g_m R_p \frac{1}{R_p C_p} = \frac{g_m}{C_p}$$

- The above expression is independent of center frequency!
 - In practice, we need to operate at a frequency less than the f_t of the device

The Issue of Q



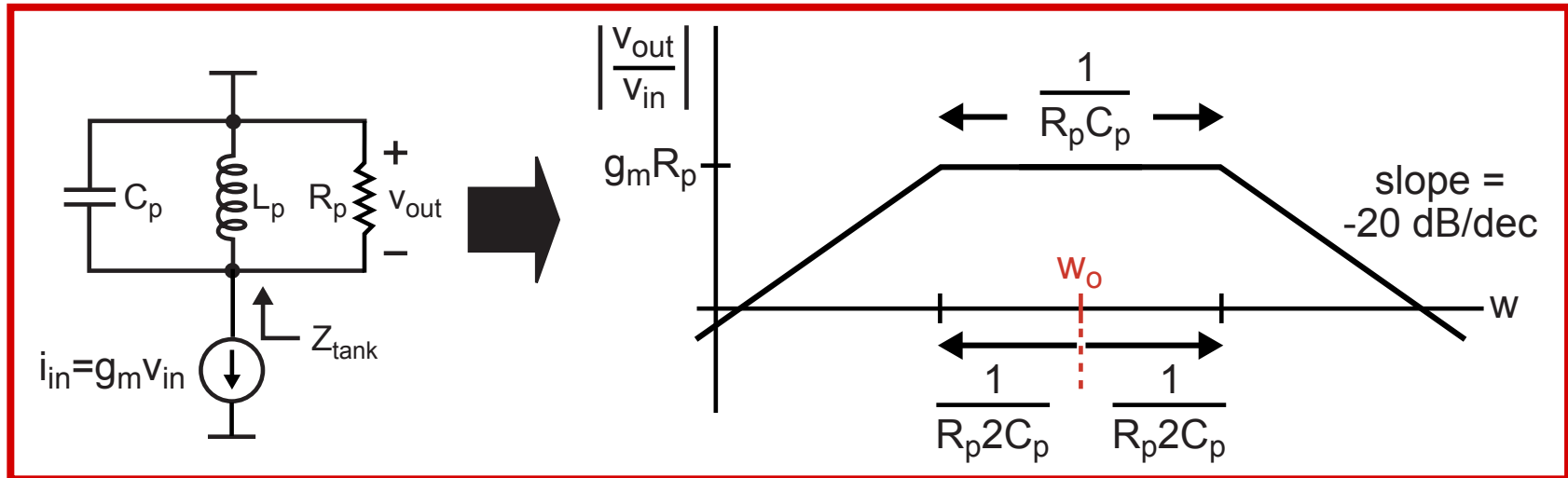
- **By definition** $Q = \omega \frac{\text{energy stored}}{\text{average power dissipated}}$

- **For parallel tank (see Tom Lee's book, pp 88-89)**

at resonance: $Q = \frac{R_p}{\omega_o L_p} = \omega_o R_p C_p$

- **Comparing to above:** $Q = \omega_o R_p C_p = \frac{\omega_o}{1/(R_p C_p)} = \boxed{\frac{\omega_o}{BW}}$

Design of Tuned Amplifiers



■ Three key parameters

- Gain = $g_m R_p$
- Center frequency = ω_o
- $Q = \omega_o / BW$

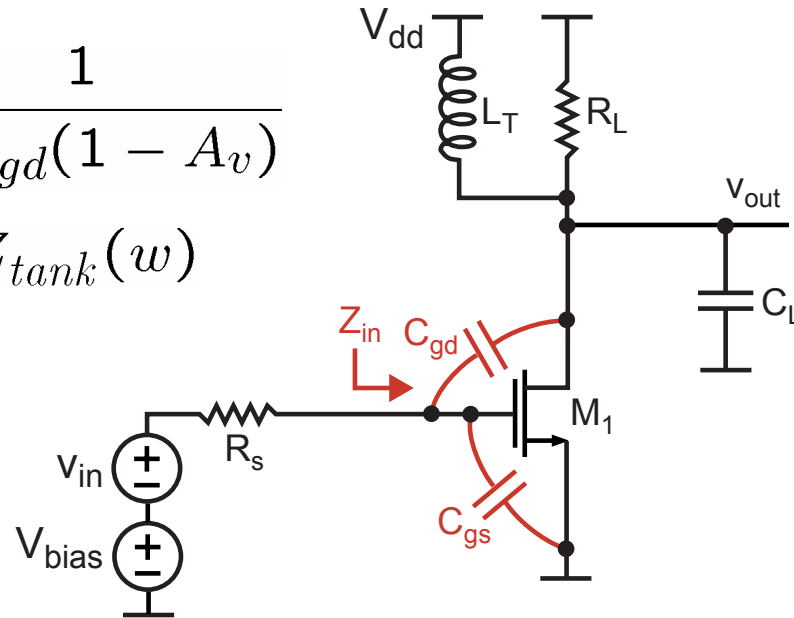
■ Impact of high Q

- Benefit: allows achievement of high gain with low power
- Problem: makes circuit sensitive to process/temp variations

Issue: C_{gd} Can Cause Undesired Oscillation

$$Z_{in}(w) = \frac{1}{jwC_{gs}} \parallel \frac{1}{jwC_{gd}(1 - A_v)}$$

$$\text{where } A_v = -g_m Z_{tank}(w)$$



- At frequencies below resonance, tank looks inductive

$$A_v \approx -g_m(jwL) \Rightarrow Z_{in}(w) \approx \frac{1}{jwC_{gs}} \parallel \frac{1}{jwC_{gd}(1 + g_m(jwL))}$$

$$\Rightarrow Z_{in}(w) \approx \frac{1}{jwC_{gs}} \parallel \frac{1}{jwC_{gd} - w^2 g_m C_{gd} L}$$

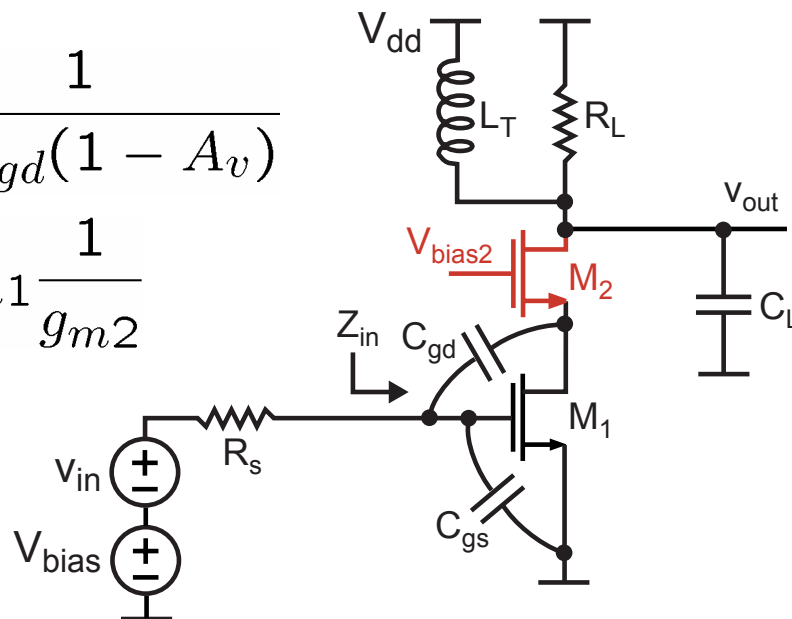
$$\Rightarrow Z_{in}(w) \approx \frac{1}{jwC_{gs}} \parallel \frac{1}{jwC_{gd}} \parallel \frac{-1}{w^2 g_m C_{gd} L}$$

Negative Resistance!

Use Cascode Device to Remove Impact of C_{gd}

$$Z_{in}(w) = \frac{1}{j\omega C_{gs}} \parallel \frac{1}{j\omega C_{gd}(1 - A_v)}$$

$$\text{where } A_v = -g_{m1} \frac{1}{g_{m2}}$$

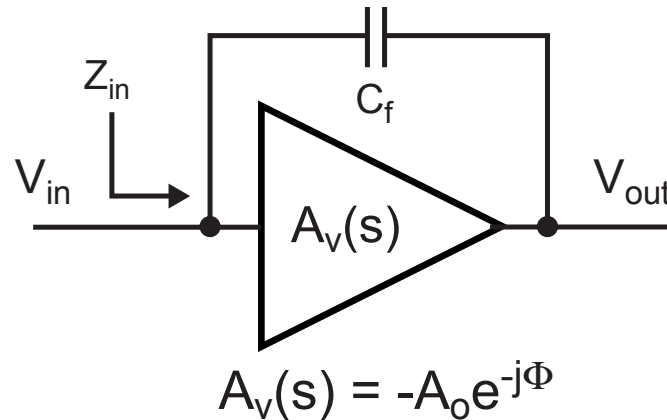


- At frequencies above and below resonance

$$Z_{in}(w) = \frac{1}{j\omega C_{gs}} \parallel \frac{1}{j\omega C_{gd}(1 + g_{m1}/g_{m2})}$$

**Purely
Capacitive!**

Active Real Impedance Generator

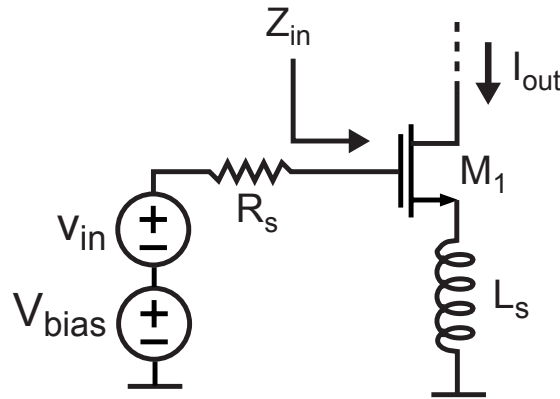


■ Input impedance:

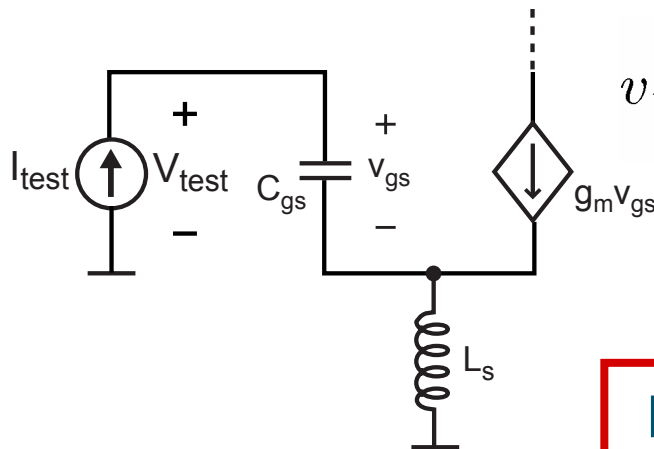
$$\begin{aligned} Z_{in}(w) &= \frac{1}{j\omega C_f(1 - A_v)} = \frac{1}{j\omega C_f(1 + A_o e^{-j\Phi})} \\ &= \frac{1}{j\omega C_f(1 + A_o \cos \Phi) + A_o \omega C \sin \Phi} \\ &= \frac{1}{j\omega C_f(1 + A_o \cos \Phi)} \parallel \frac{1}{A_o \omega C \sin \Phi} \end{aligned}$$

Resistive component!

This Principle Can Be Applied To Impedance Matching



- **We will see that it's advantageous to make Z_{in} real without using resistors**
 - **For the above circuit (ignoring C_{gd})**

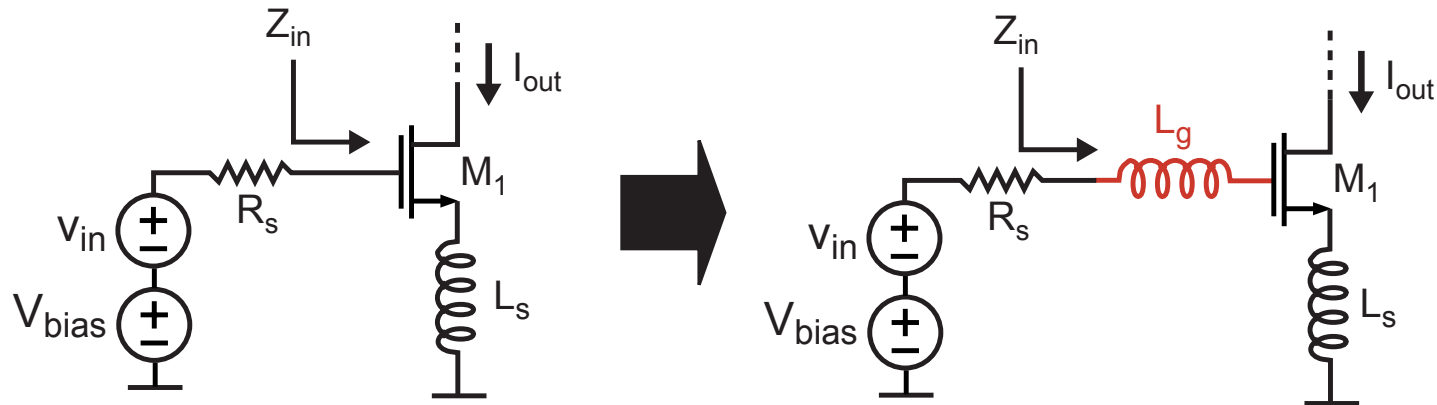


$$v_{test} = i_{test} \left(\frac{1}{sC_{gs}} + \left(1 + g_m \frac{1}{sC_{gs}} \right) sL_s \right)$$

$$\Rightarrow Z_{in}(s) = \frac{1}{sC_{gs}} + sL_s + \frac{g_m}{C_{gs}} L_s$$

Looks like series resonant circuit!

Use A Series Inductor to Tune Resonant Frequency



- Calculate input impedance with added inductor

$$Z_{in}(s) = \frac{1}{sC_{gs}} + s(L_s + L_g) + \frac{g_m}{C_{gs}}L_s$$

- Often want purely resistive component at frequency ω_o
 - Choose L_g such that resonant frequency = ω_o

$$\text{i.e., want } \frac{1}{\sqrt{(L_s + L_g)C_{gs}}} = \omega_o$$