6.976
High Speed Communication Circuits and Systems
Lecture 9
Low Noise Amplifiers

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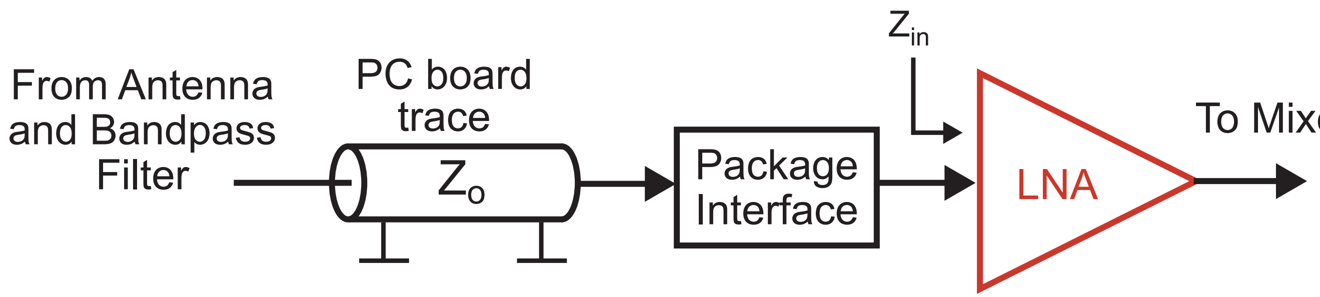
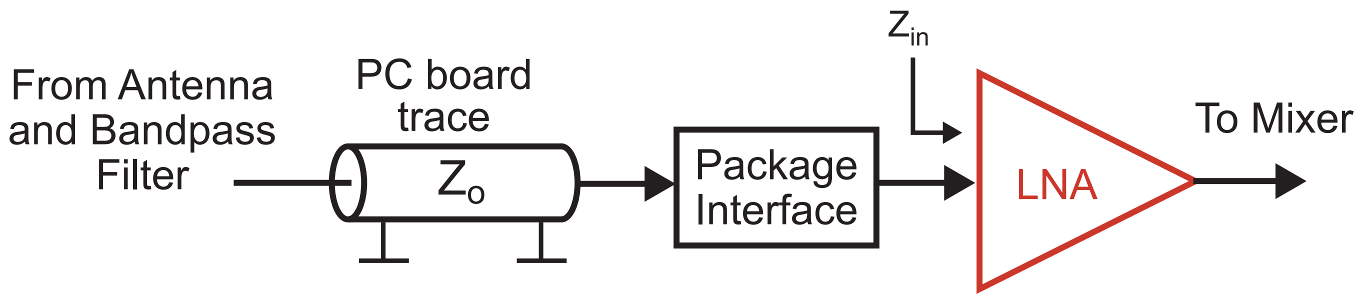
Narrowband LNA Design for Wireless Systems



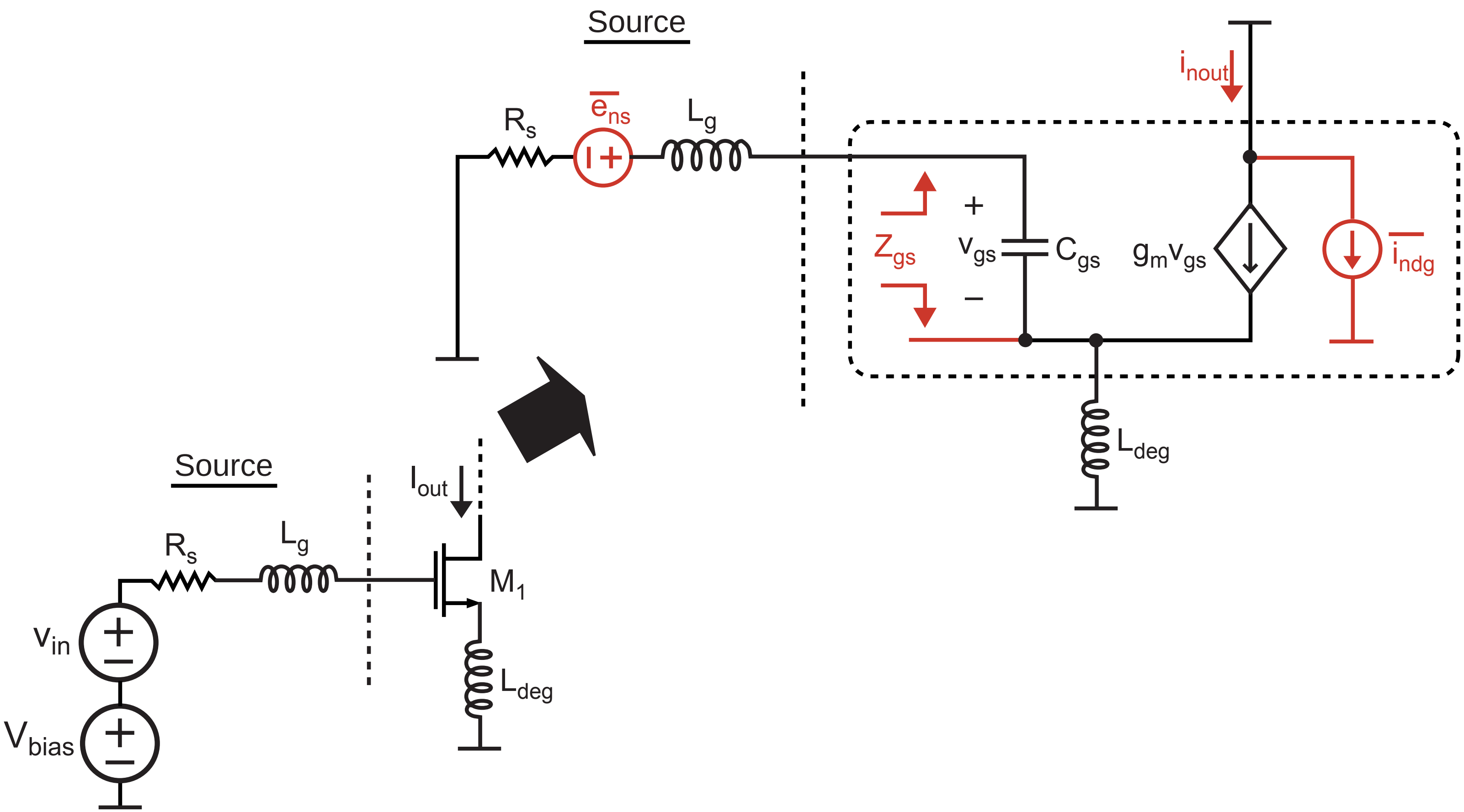
- **Design Issues**
  - **Noise Figure – impacts receiver sensitivity**
  - **Linearity (IIP3) – impacts receiver blocking performance**
  - **Gain – high gain reduces impact of noise from components that follow the LNA (such as the mixer)**
  - **Power match – want $Z_{in} = Z_o$ (usually = 50 Ohms)**
  - **Power – want low power dissipation**
  - **Bandwidth – need to pass the entire RF band for the intended radio application (i.e., all of the relevant channels)**
  - **Sensitivity to process/temp variations – need to make it manufacturable in high volume**

Our Focus in This Lecture



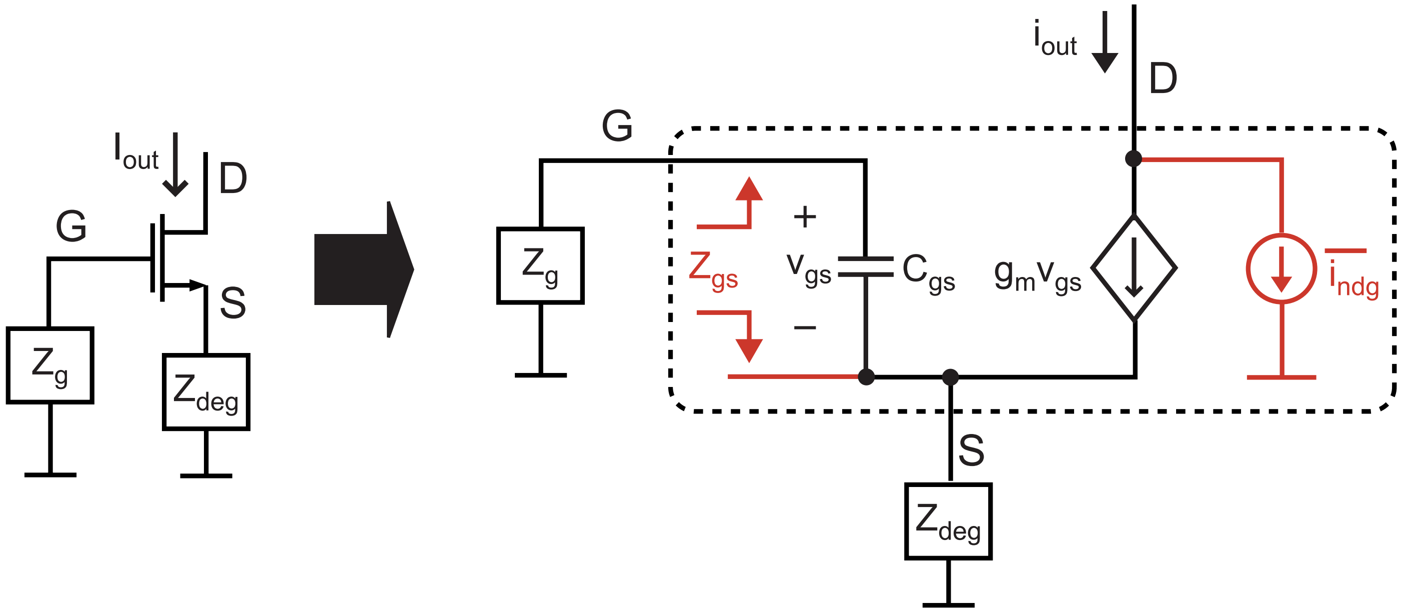
- Designing for low Noise Figure
- Achieving a good power match
- Hints at getting good IIP3
- Impact of power dissipation on design
- Tradeoff in gain versus bandwidth

Our Focus: Inductor Degenerated Amp



- Same as amp in Lecture 7 except for inductor degeneration
  - Note that noise analysis in Tom Lee's book does not include inductor degeneration (i.e., Table 11.1)

Recall Small Signal Model for Noise Calculations

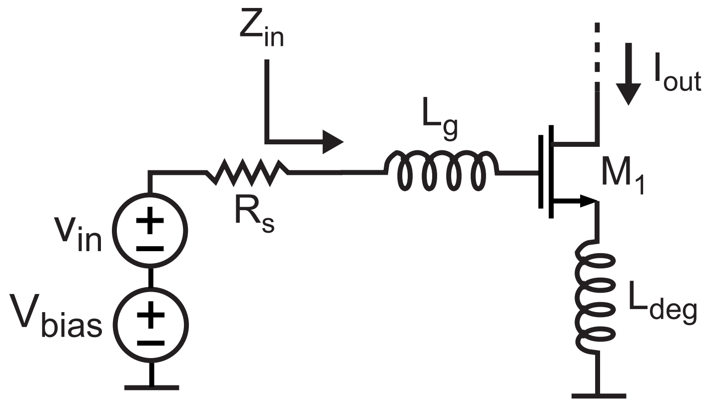


$$\frac{\overline{i_{ndg}^2}}{\Delta f} = \frac{\overline{i_{nd}^2}}{\Delta f}\left(|\eta|^2 + 2Re\left\{c\chi_d\eta^* Z_{gsw}\right\} + \chi_d^2|Z_{gsw}|^2\right)$$

where: $\dfrac{\overline{i_{nd}^2}}{\Delta f} = 4kT\gamma g_{do},\ \chi_d = \dfrac{g_m}{g_{do}}\sqrt{\dfrac{\delta}{5\gamma}},\quad Z_{gsw} = wC_{gs}Z_{gs}$

$$Z_{gs} = \frac{1}{sC_{gs}} \Big|\Big| \frac{Z_{deg}+Z_g}{1+g_mZ_{deg}} \qquad \eta = 1 - \left(\frac{g_mZ_{deg}}{Z_{deg}+Z_g}\right)Z_{gs}$$

Key Assumption: Design for Power Match



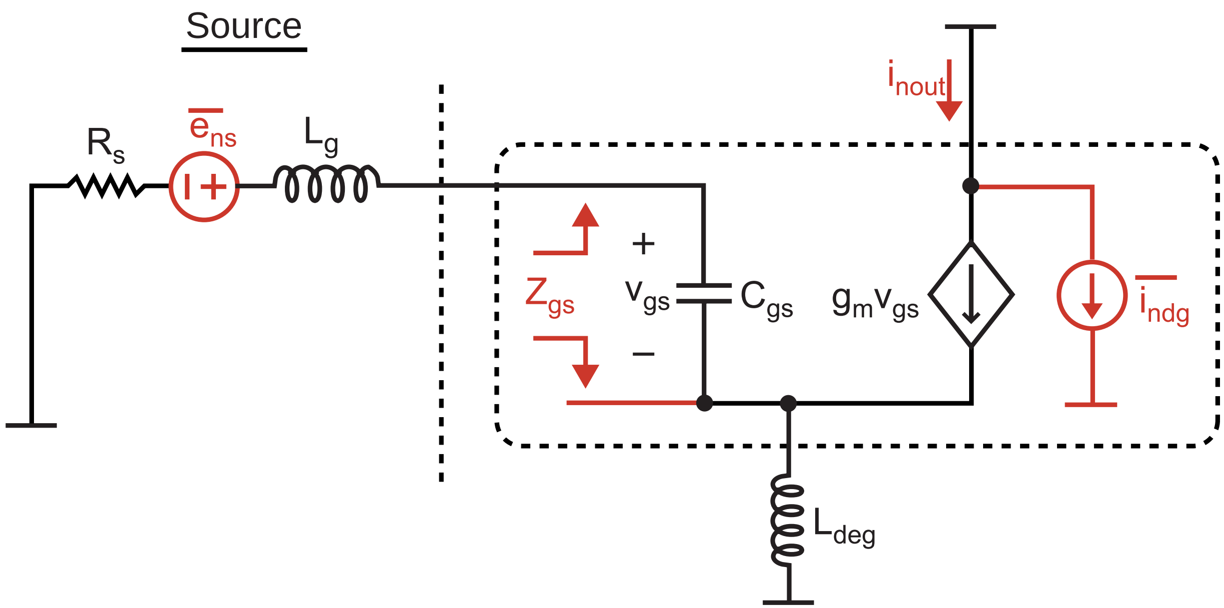
- **Input impedance (from Lec 6)**

$$Z_{in}(s) = \frac{1}{sC_{gs}} + s(L_{deg} + L_g) + \underbrace{\frac{g_m}{C_{gs}} L_{deg}}_{\textbf{Real!}}$$

- **Set to achieve pure resistance = R_s at frequency w_o**

$$\boxed{\Rightarrow \quad \frac{1}{\sqrt{(L_g + L_{deg})C_{gs}}} = w_o, \qquad \frac{g_m}{C_{gs}} L_{deg} = R_s}$$

Process and Topology Parameters for Noise Calculation



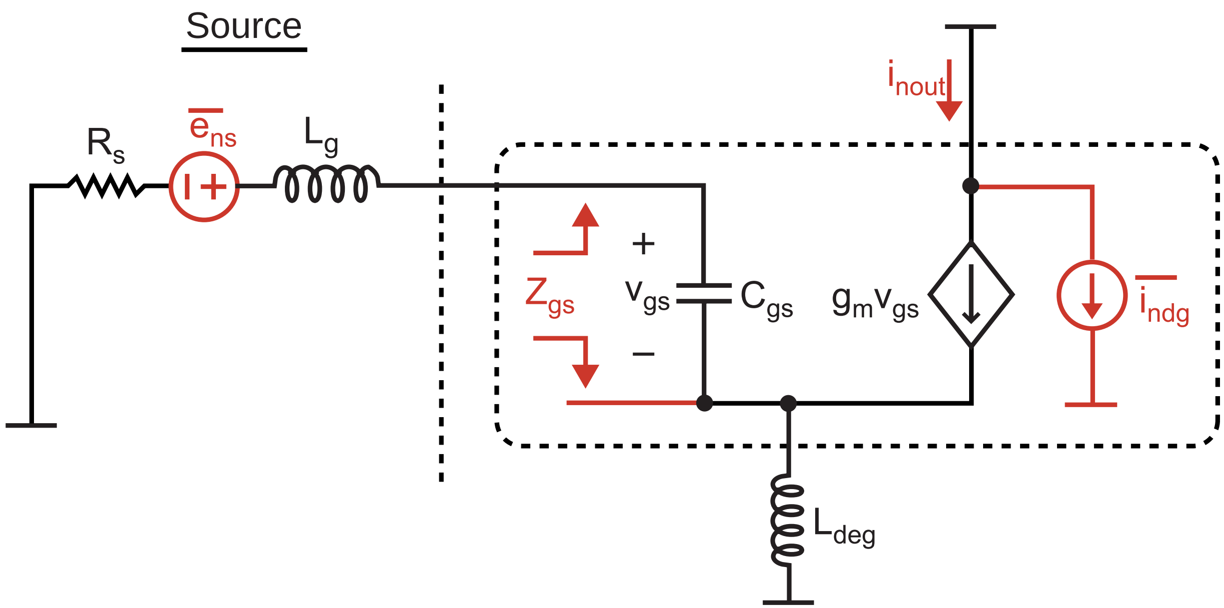
- **Process parameters**
  - **For 0.18μ CMOS, we will assume the following**

$$\boxed{c = -j0.55,} \quad \gamma = 3, \quad \delta = 2\gamma = 6, \quad \frac{g_m}{g_{do}} = \frac{1}{2} \Rightarrow \boxed{\chi_d = 0.32}$$

- **Circuit topology parameters Z_g and Z_{deg}**

$$\boxed{Z_g = R_s + jwL_g, \quad Z_{deg} = jwL_{deg}}$$

Calculation of Z_{gs}

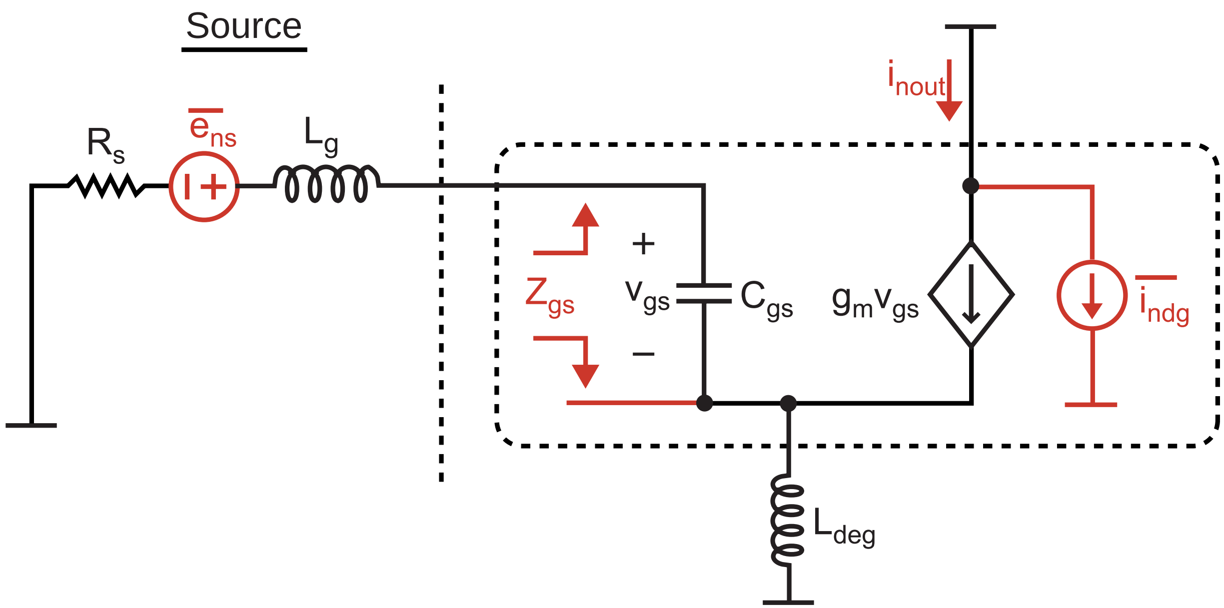


$$Z_{gs} = \frac{1}{sC_{gs}} \Bigg|\Bigg| \frac{Z_{deg} + Z_g}{1 + g_m Z_{deg}} = \frac{1}{jw_o C_{gs}} \Bigg|\Bigg| \frac{jw_o(L_{deg} + L_g) + R_s}{1 + g_m jw_o L_{deg}}$$

$$= \frac{jw_o(L_{deg} + L_g) + R_s}{1 - w_o^2 C_{gs}(L_{deg} + L_s) + jw_o(g_m L_{deg} + R_s C_{gs})}$$

$$\boxed{= \frac{jw_o(L_{deg} + L_g) + R_s}{jw_o(g_m L_{deg} + R_s C_{gs})}}$$

Calculation of η



$$\eta = 1 - \left(\frac{g_m Z_{deg}}{Z_{deg} + Z_g}\right) Z_{gs} = 1 - \frac{g_m j w_o L_{deg}}{j w_o (L_{deg} + L_g) + R_s} Z_{gs}$$

$$= 1 - \frac{g_m j w_o L_{deg}}{j w_o (g_m L_{deg} + R_s C_{gs})} = 1 - \frac{(g_m/C_{gs}) L_{deg}}{\underbrace{(g_m/C_{gs}) L_{deg}}_{= R_s} + R_s}$$

$$= 1 - \frac{R_s}{R_s + R_s} = \boxed{\frac{1}{2}}$$

Calculation of Z_{gsw}

- **By definition**

$$Z_{gsw} = w_o C_{gs} Z_{gs} \qquad \left(Q = \frac{1}{w_o C_{gs} 2R_s} = \frac{w_o(L_g + L_{deg})}{2R_s}\right)$$

- **Calculation**

$$Z_{gsw} = w_o C_{gs} \frac{j w_o (L_{deg} + L_g) + R_s}{j w_o (g_m L_{deg} + R_s C_{gs})}$$

$$= \frac{j w_o^2 C_{gs} (L_{deg} + L_g) + w_o C_{gs} R_s}{j w_o (g_m L_{deg} + R_s C_{gs})}$$

$$= \frac{j1 + 1/(2Q)}{j w_o (g_m L_{deg} + R_s C_{gs})}$$

$$= \frac{j1 + 1/(2Q)}{j w_o C_{gs} ((g_m / C_{gs}) L_{deg} + R_s)}$$

$$= \frac{j1 + 1/(2Q)}{j w_o C_{gs} (R_s + R_s)} = \frac{j1 + 1/(2Q)}{j1/Q} = \boxed{\frac{1}{2}(2Q - j)}$$

Calculation of Output Current Noise

- **Step 3: Plug in values to noise expression for i_{ndg}**

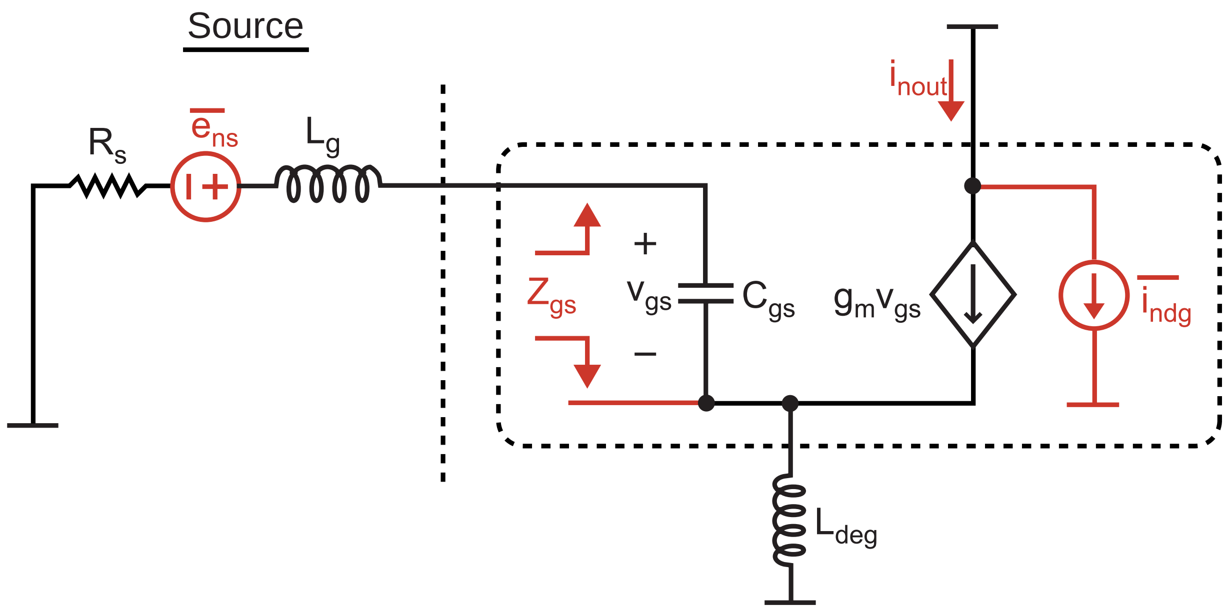
$$\frac{\overline{i_{ndg}^2}}{\Delta f} = \frac{\overline{i_{nd}^2}}{\Delta f}\left(|\eta|^2 + 2Re\{-j|c|\chi_d \eta^* Z_{gsw}\} + \chi_d^2 |Z_{gsw}|^2\right)$$

$$\text{where } \eta = \frac{1}{2}, \qquad Z_{gsw} = \frac{1}{2}(2Q - j)$$

$$\Rightarrow \frac{\overline{i_{ndg}^2}}{\Delta f} = \frac{\overline{i_{nd}^2}}{\Delta f}\left(\frac{1}{4} + 2Re\left\{-j|c|\chi_d \frac{1}{4}(2Q - j)\right\} + \chi_d^2 \frac{1}{4}|2Q - j|^2\right)$$

$$\boxed{= \frac{\overline{i_{nd}^2}}{\Delta f}\frac{1}{4}\left(1 - 2|c|\chi_d + \chi_d^2(4Q^2 + 1)\right)}$$

Compare Noise With and Without Inductor Degeneration



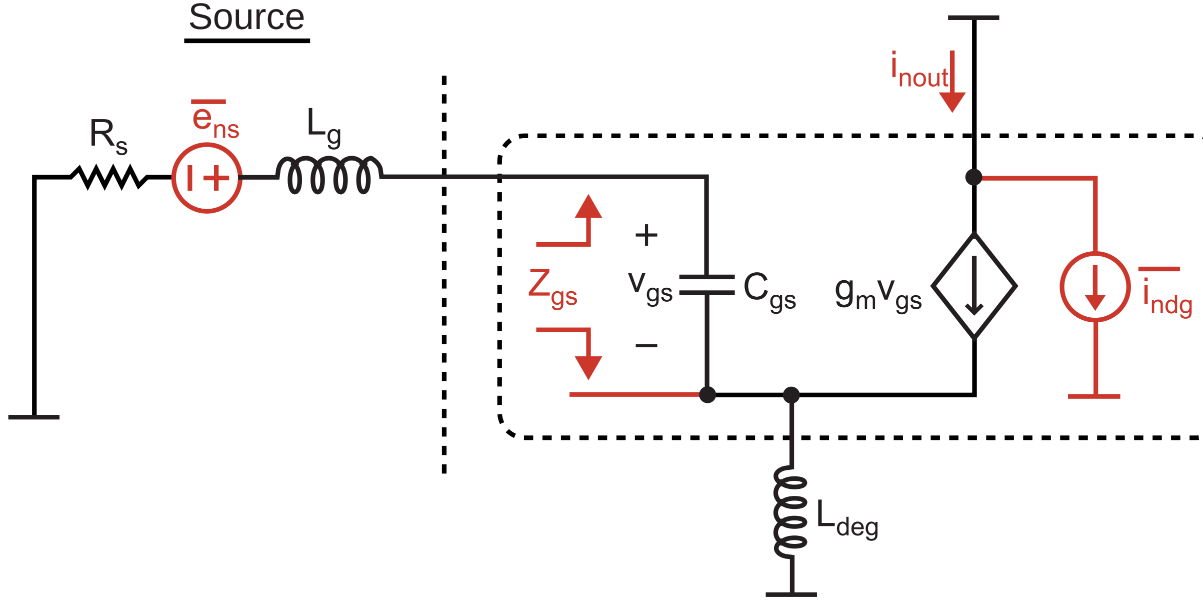
- **From Lecture 7, we derived for $L_{deg} = 0$, $w_o^2 = 1/(L_g C_{gs})$**

$$\frac{\overline{i_{ndg}^2}}{\Delta f} = \frac{\overline{i_{nd}^2}}{\Delta f}\left(1 - 2|c|\chi_d + \chi_d^2(Q^2+1)\right)$$

- **We now have for $(g_m/C_{gs})L_{deg} = R_s$, $w_o^2 = 1/((L_g + L_{deg})C_{gs})$**

$$\frac{\overline{i_{ndg}^2}}{\Delta f} = \frac{\overline{i_{nd}^2}}{\Delta f}\frac{1}{4}\left(1 - 2|c|\chi_d + \chi_d^2(4Q^2+1)\right)$$

Derive Noise Factor for Inductor Degenerated Amp

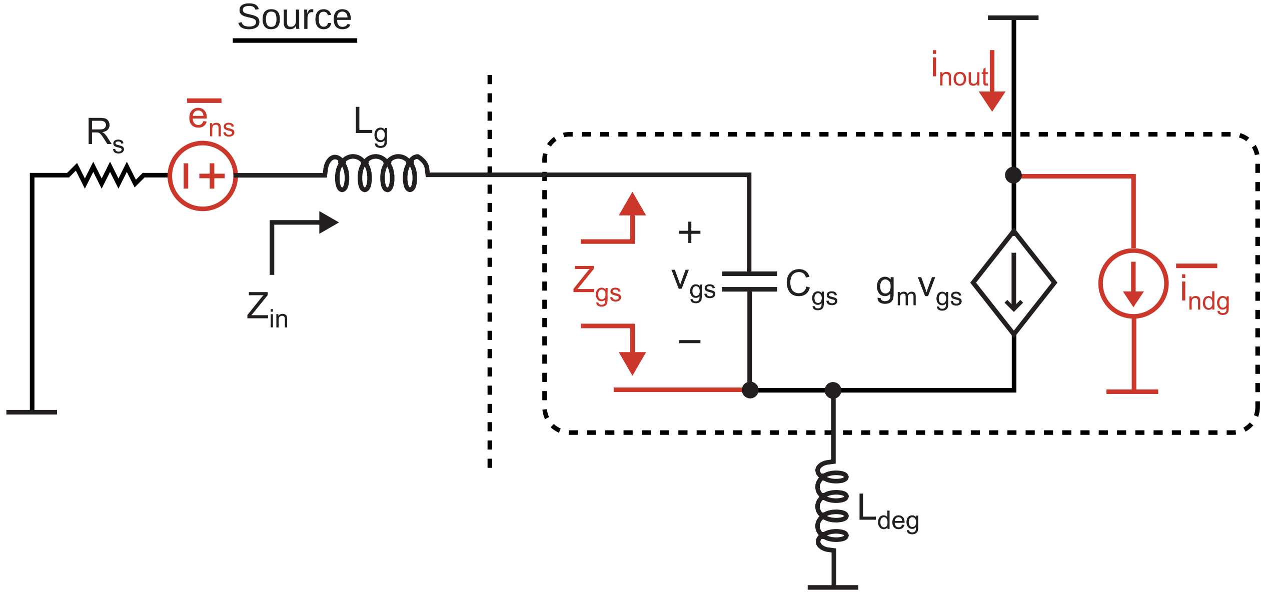


- Recall the alternate expression for Noise Factor derived in Lecture 8

$$F = \frac{\text{total output noise power}}{\text{output noise due to input source}} = \frac{\overline{i^2_{nout(tot)}}}{\overline{i^2_{nout(in)}}}$$

- We now know the output noise due to the transistor noise
  - We need to determine the output noise due to the source resistance

Output Noise Due to Source Resistance



$$Z_{in} = \frac{1}{jw_o C_{gs}} + jw_o(L_{deg} + L_g) + \frac{g_m}{C_{gs}} L_{deg} = R_s$$

$$\Rightarrow \quad v_{gs} = \frac{\overline{e_{ns}}}{R_s + Z_{in}} \left(\frac{1}{jw_o C_{gs}} \right) = \frac{\overline{e_{ns}}}{2R_s} \left(\frac{1}{jw_o C_{gs}} \right) = \left(\frac{Q}{j} \right) \overline{e_{ns}}$$

$$\Rightarrow \quad i_{nout} = g_m \left(\frac{Q}{j} \right) \overline{e_{ns}}$$

$$\boxed{\Rightarrow \quad \overline{i_{nout}^2} = (g_m Q)^2 \overline{e_{ns}^2}}$$

Noise Factor for Inductor Degenerated Amplifier

$$\text{Noise Factor} = \frac{(g_m Q)^2 \overline{e_{ns}^2} + \overline{i_{ndg}^2}/\Delta f}{(g_m Q)^2 \overline{e_{ns}^2}} = 1 + \frac{\overline{i_{ndg}^2}/\Delta f}{(g_m Q)^2 \overline{e_{ns}^2}}$$

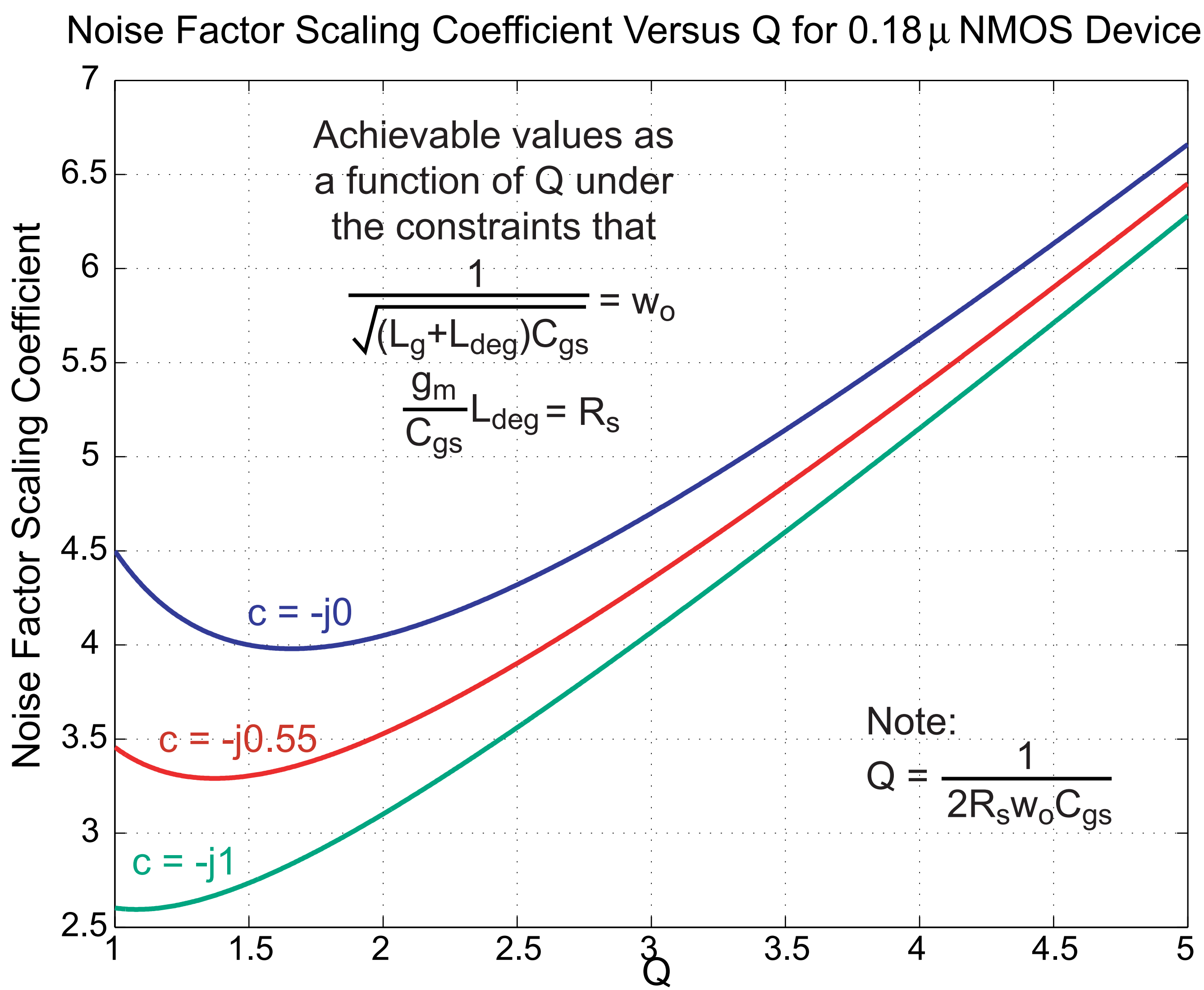
$$= 1 + \frac{4kT\gamma g_{do}(1/4)(1 - 2|c|\chi_d + \chi_d^2(4Q^2 + 1))}{(g_m Q)^2 4kTR_s}$$

$$= 1 + \left(\frac{1}{g_m Q R_s}\right)\gamma\left(\frac{g_{do}}{g_m}\right)\frac{1}{4Q}\left(1 - 2|c|\chi_d + (4Q^2 + 1)\chi_d^2\right)$$

$$= 1 + \left(\frac{2w_o R_s C_{gs}}{g_m R_s}\right)\gamma\left(\frac{g_{do}}{g_m}\right)\frac{1}{4Q}\left(1 - 2|c|\chi_d + (4Q^2 + 1)\chi_d^2\right)$$

$$\boxed{= 1 + \left(\frac{w_o}{w_t}\right)\underbrace{\gamma\left(\frac{g_{do}}{g_m}\right)\frac{1}{2Q}\left(1 - 2|c|\chi_d + (4Q^2 + 1)\chi_d^2\right)}_{\text{Noise Factor scaling coefficient}}}$$

Noise Factor Scaling Coefficient Versus Q



Achievable Noise Figure in 0.18μ with Power Match

- **Suppose we desire to build a narrowband LNA with center frequency of 1.8 GHz in 0.18μ CMOS (c=-j0.55)**
  - **From Hspice – at V_{gs} = 1 V with NMOS (W=1.8μ, L=0.18μ)**
    - measured g_m =871 μS, C_{gs} = 2.9 fF

$$\Rightarrow \quad w_t \approx \frac{g_m}{C_{gs}} = \frac{871 \times 10^{-6}}{2.9 \times 10^{-15}} = 2\pi(47.8GHz)$$

$$\Rightarrow \quad \frac{w_o}{w_t} = \frac{2\pi 1.8e9}{2\pi 47.8e9} \approx \frac{1}{26.6}$$

  - **Looking at previous curve, with Q ≈ 2 we achieve a Noise Factor scaling coefficient ≈ 3.5**

$$\Rightarrow \quad \text{Noise Factor} \approx 1 + \frac{1}{26.6}3.5 \approx 1.13$$

$$\Rightarrow \quad \text{Noise Figure} = 10\log(1.13) \approx 0.53\ dB$$

Component Values for Minimum NF with Power Match

- **Assume R_s = 50 Ohms, Q = 2, f_o = 1.8 GHz, f_t = 47.8 GHz**
  - **C_{gs} calculated as**

$$Q = \frac{1}{2R_s w_o C_{gs}}$$

$$\Rightarrow \quad C_{gs} = \frac{1}{2R_s w_o Q} = \frac{1}{2(50)2\pi 1.8e9(2)} = \boxed{442fF}$$

  - **L_{deg} calculated as**

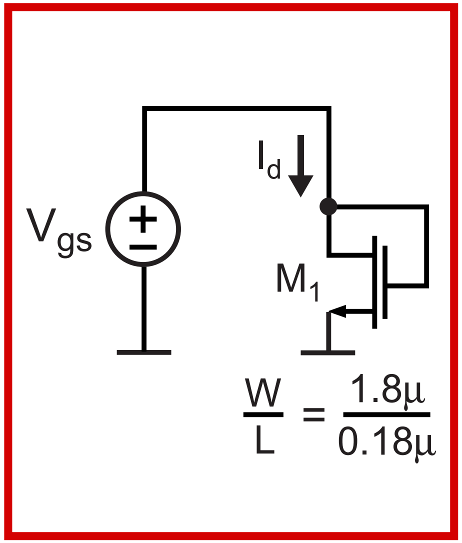
$$\frac{g_m}{C_{gs}} L_{deg} = R_s \quad \Rightarrow \quad L_{deg} = \frac{R_s}{w_t} = \frac{50}{2\pi 47.8e9} = \boxed{0.17nH}$$

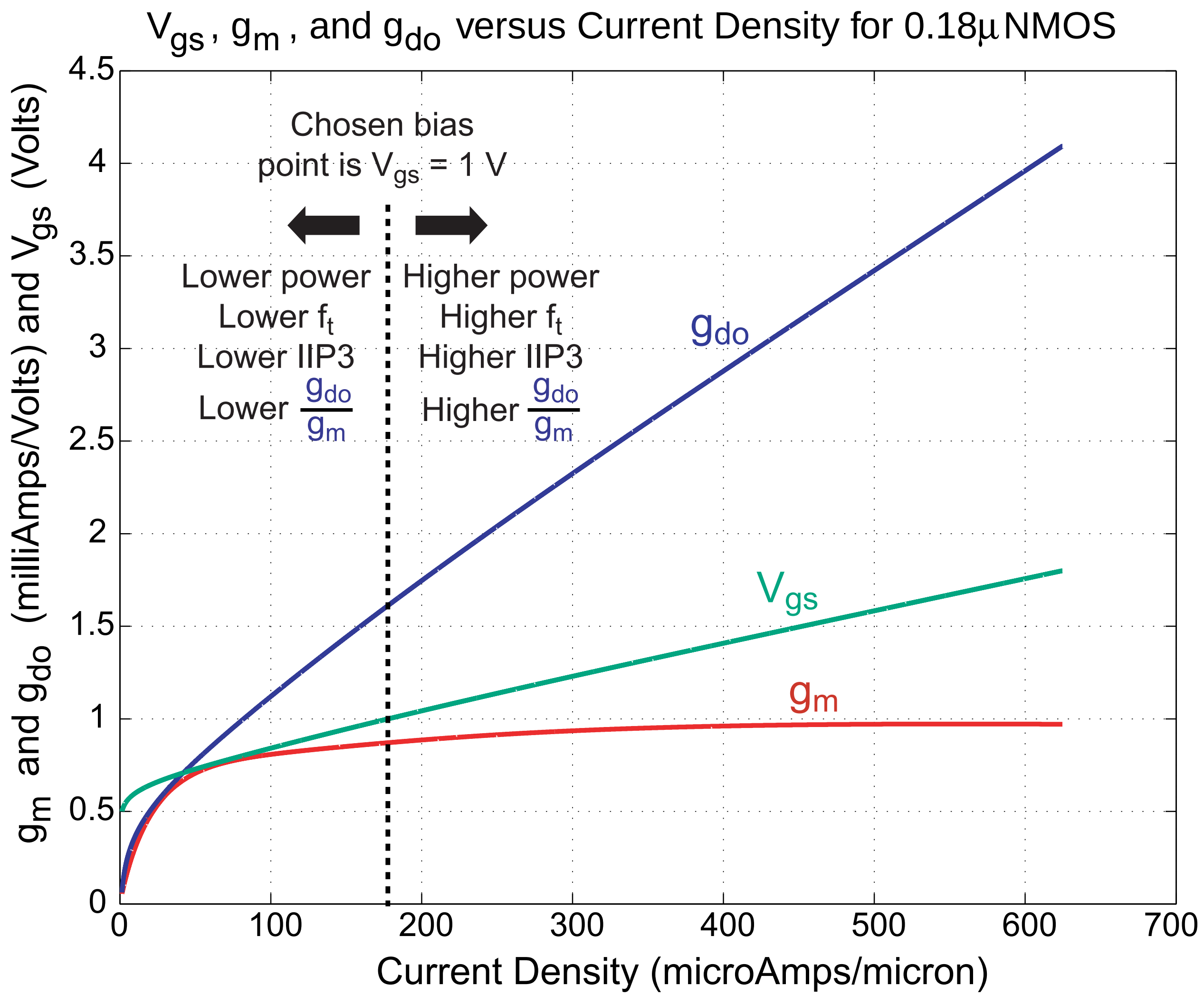
  - **L_g calculated as**

$$\frac{1}{\sqrt{(L_g + L_{deg})C_{gs}}} = w_o \quad \Rightarrow \quad L_g = \frac{1}{w_o^2 C_{gs}} - L_{deg}$$

$$\Rightarrow \quad L_g = \frac{1}{(2\pi 1.8e9)^2 442e\text{-}15} - 0.17e\text{-}9 = \boxed{17.5nH}$$

Have We Chosen the Correct Bias Point? (V_{gs} = 1V)





- **Note: IIP3 is also a function of Q**

Calculation of Bias Current for Example Design

- **Calculate current density from previous plot**

$$V_{gs} = 1V \;\Rightarrow\; I_{dens} \approx 175\mu A/\mu m$$

- **Calculate W from Hspice simulation (assume L=0.18 μm)**

$$C_{gs} = 2.9fF \text{ for } W = 1.8\mu m \;\Rightarrow\; W = \frac{442fF}{2.9fF}1.8\mu m \approx 274\mu m$$

  - **Could also compute this based on C_{ox} value**
- **Calculate bias current**

$$I_{bias} = I_{den}W = (175\mu A/\mu m)(274\mu m) \approx \boxed{48mA}$$

  - **Problem: this is not low power!!**

We Have Two "Handles" to Lower Power Dissipation

- **Key formulas** $$I_{bias} = I_{den} W$$

$$F = 1 + \left(\frac{w_o}{w_t}\right)\gamma\left(\frac{g_{do}}{g_m}\right)\frac{1}{2Q}\left(1 - 2|c|\chi_d + (4Q^2+1)\chi_d^2\right)$$

- **Lower current density, I_{den}**
  - **Benefits**

$$\Rightarrow \text{ lower power, } \text{ lower } \frac{g_{do}}{g_m} \text{ ratio}$$

  - **Negatives**

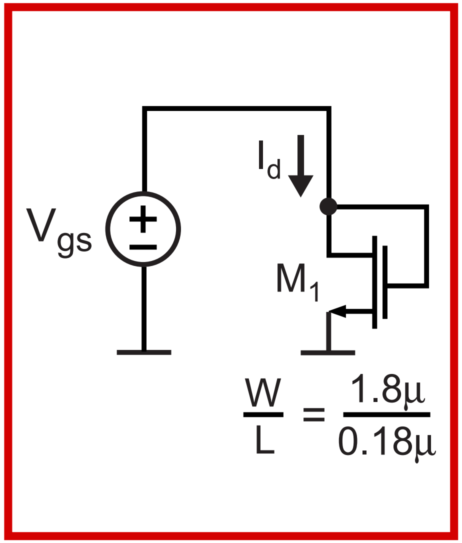
$$\Rightarrow \text{ lower IIP3, } \text{ lower } f_t$$

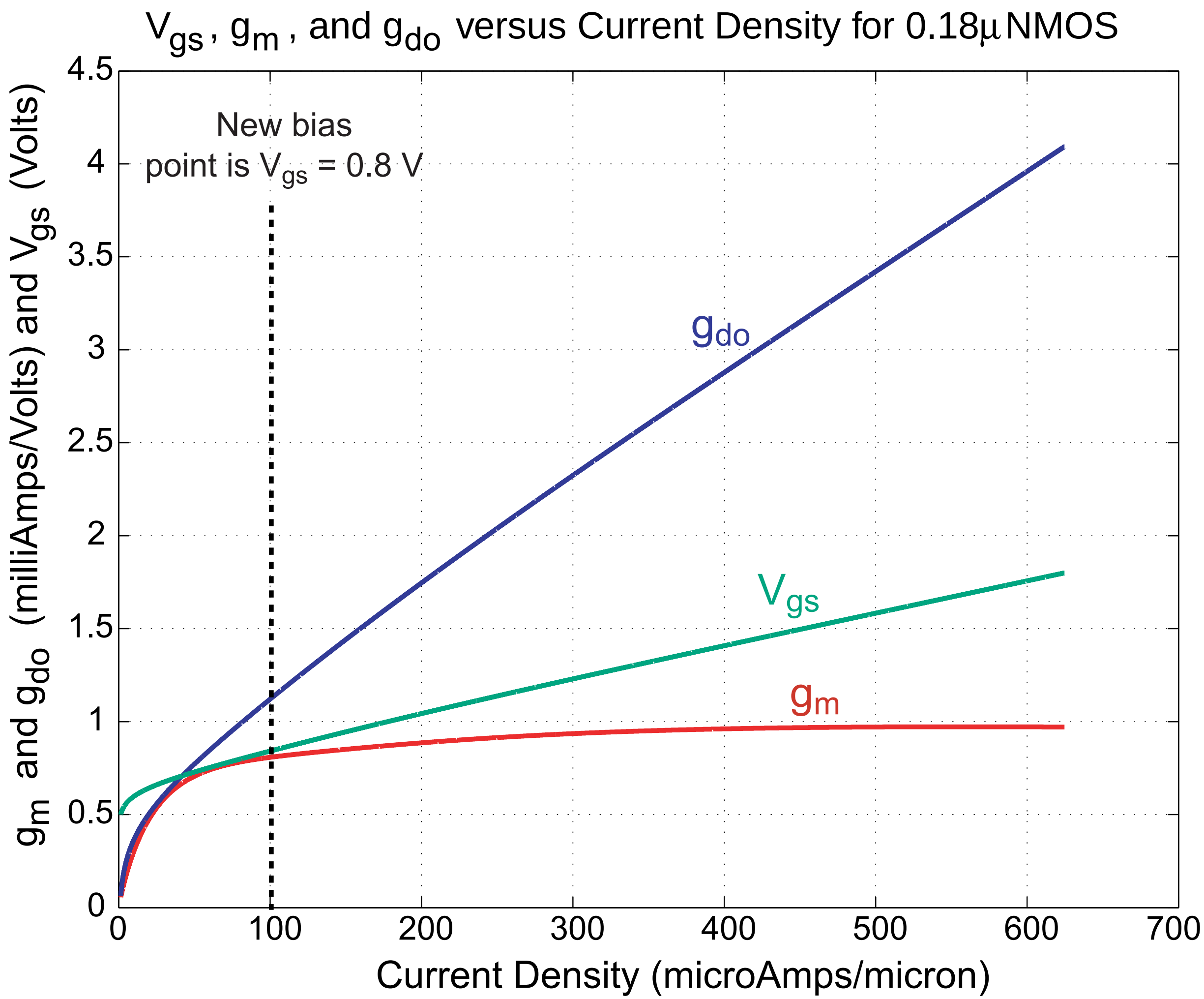
- **Lower W**
  - **Benefit: lower power**
  - **Negatives**

$$\Rightarrow \text{ lower } C_{gs} = \frac{2}{3} W L C_{ox} \Rightarrow \text{ higher } Q = \frac{1}{w_o C_{gs} 2 R_s}$$

$$\Rightarrow \text{ higher } F \quad \text{(and higher inductor values)}$$

First Step in Redesign – Lower Current Density, I_{den}





- Need to verify that IIP3 still OK (once we know Q)

Recalculate Process Parameters

- Assume that the only thing that changes is g_m/g_{do} and f_t
  - From previous graph (I_{den} = 100 μ A/μ m)

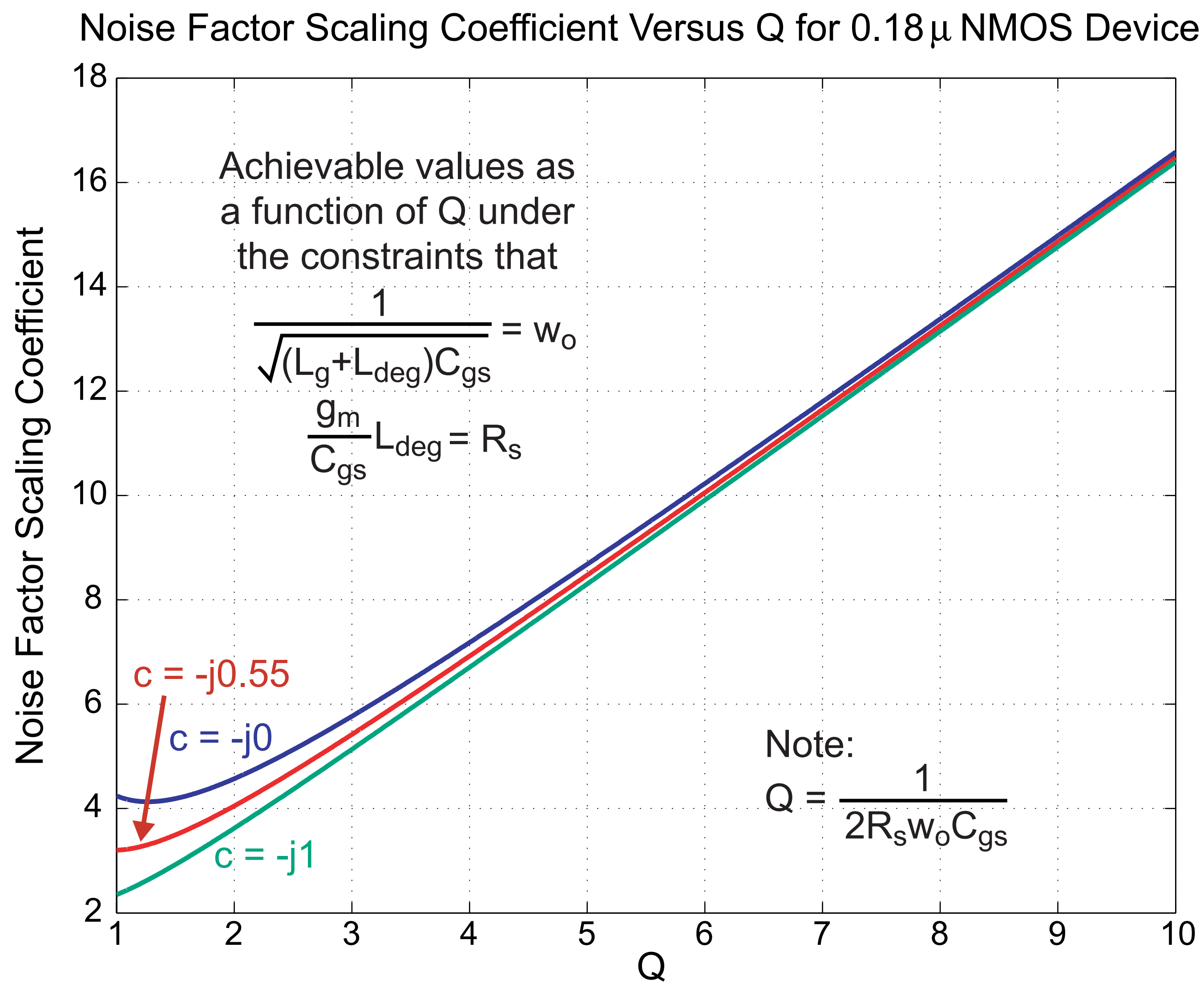
$$\frac{g_m}{g_{do}} \approx \frac{.78}{1.15} \approx 0.68 \;\Rightarrow\; \chi_d = \frac{g_m}{g_{do}}\sqrt{\frac{\delta}{5\gamma}} = 0.63\sqrt{\frac{2}{5}} \approx 0.43$$

$$w_t \approx \frac{g_m}{C_{gs}} \approx \frac{0.78mS}{2.9fF} = (2\pi)42.8GHz$$

- We now need to replot the Noise Factor scaling coefficient
  - Also plot over a wider range of Q

$$F = 1 + \left(\frac{w_o}{w_t}\right)\underbrace{\gamma\left(\frac{g_{do}}{g_m}\right)\frac{1}{2Q}\left(1 - 2|c|\chi_d + (4Q^2+1)\chi_d^2\right)}_{\text{Noise Factor scaling coefficient}}$$

Update Plot of Noise Factor Scaling Coefficient



Second Step in Redesign – Lower W

- **Recall**

$$C_{gs} = \frac{2}{3} W L C_{ox}, \quad Q = \frac{1}{w_o C_{gs} 2 R_s}$$

- **I_{bias} can be related to Q as**

$$I_{bias} = I_{den} W = I_{den} \frac{3}{2 L C_{ox}} C_{gs} = I_{den} \frac{3}{2 L C_{ox}} \frac{1}{w_o 2 R_s Q}$$

$$\Rightarrow \boxed{I_{bias} \propto \frac{1}{Q}}$$

- **We previously chose Q = 2, let's now choose Q = 6**
  - **Cuts power dissipation by a factor of 3!**
  - **New value of W is one third the old one**

$$\Rightarrow W = \frac{274 fF}{3} \approx \boxed{91 \mu m}$$

Power Dissipation and Noise Figure of New Design

- **Power dissipation**

$$I_{bias} = I_{den}W = (100\mu A/\mu m)(91\mu m) = 9.1mA$$

  - **At 1.8 V supply**

$$\Rightarrow \quad \text{Power} = (9.1mA)(1.8V) = \boxed{16.4mW}$$

- **Noise Figure**
  - **f_t previously calculated, get scaling coeff. from plot**

$$\frac{w_o}{w_t} = \frac{2\pi 1.8e9}{2\pi 42.8e9} \approx \frac{1}{23.8}, \quad \text{scaling coeff.} \approx 10$$

$$\Rightarrow \quad \text{Noise Factor} \approx 1 + \frac{1}{23.8}10 \approx 1.42$$

$$\Rightarrow \quad \text{Noise Figure} = 10\log(1.42) \approx \boxed{1.52\ dB}$$

Updated Component Values

- Assume R_s = 50 Ohms, Q = 6, f_o = 1.8 GHz, f_t = 42.8 GHz
  - C_{gs} calculated as

$$Q = \frac{1}{2R_s w_o C_{gs}}$$

$$\Rightarrow \; C_{gs} = \frac{1}{2R_s w_o Q} = \frac{1}{2(50)2\pi 1.8e9(6)} \approx \boxed{147fF}$$

  - L_{deg} calculated as

$$\frac{g_m}{C_{gs}} L_{deg} = R_s \;\; \Rightarrow \;\; L_{deg} = \frac{R_s}{w_t} = \frac{50}{2\pi 42.8e9} = \boxed{0.19nH}$$

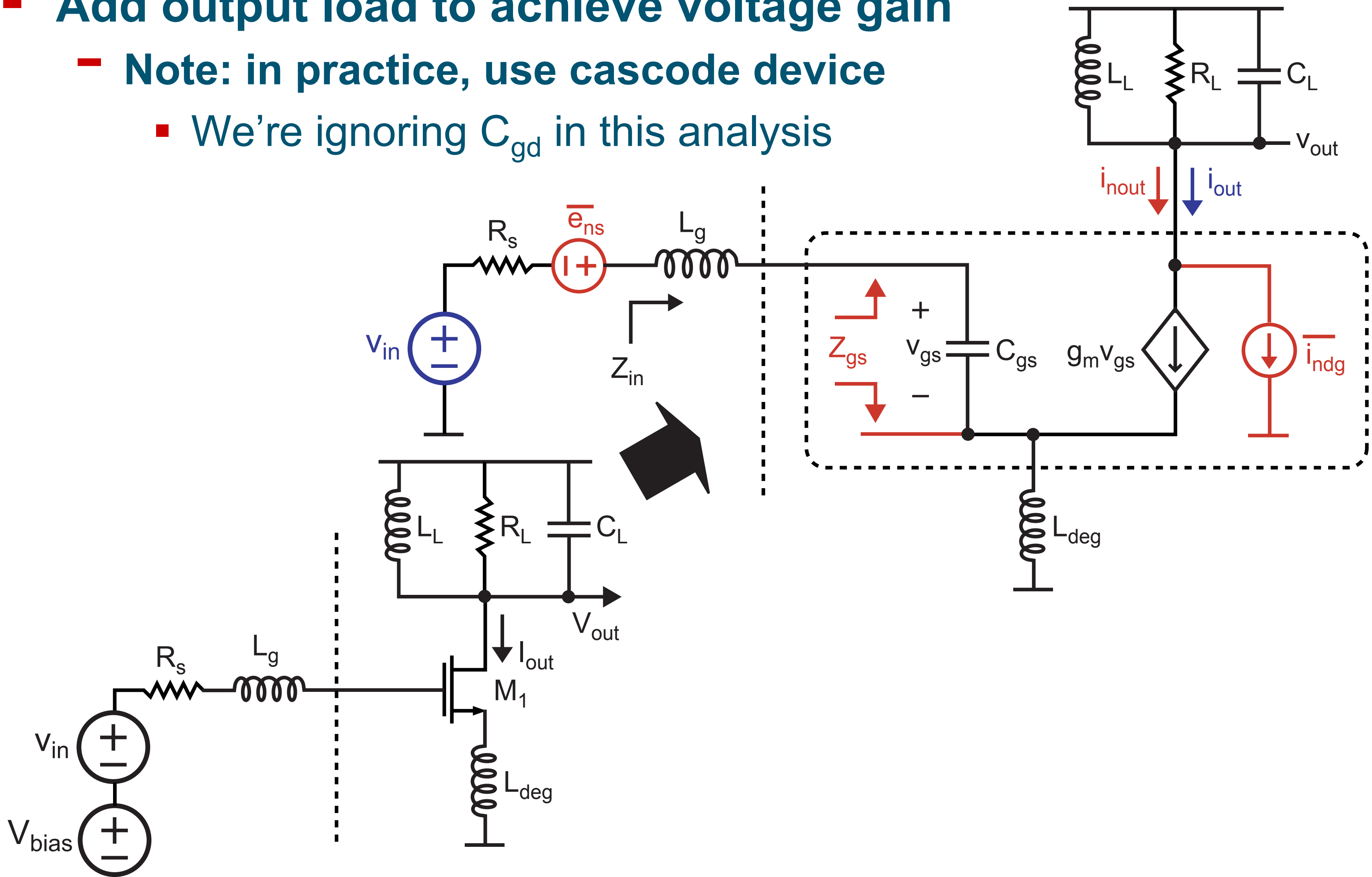
  - L_g calculated as

$$\frac{1}{\sqrt{(L_g + L_{deg})C_{gs}}} = w_o \;\Rightarrow\; L_g = \frac{1}{w_o^2 C_{gs}} - L_{deg}$$

$$\Rightarrow \; L_g = \frac{1}{(2\pi 1.8e9)^2 147e\text{-}15} - 0.19e\text{-}9 = \boxed{53nH}$$

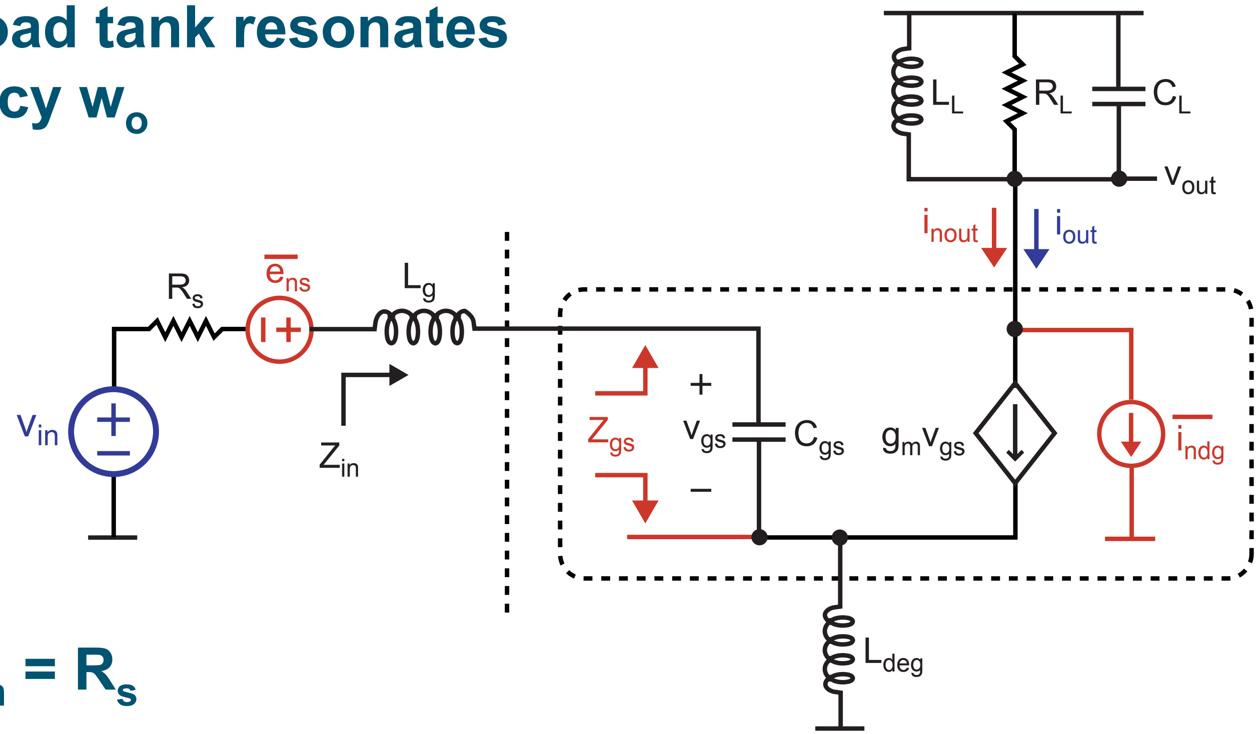
Inclusion of Load (Resonant Tank)

- **Add output load to achieve voltage gain**
  - **Note: in practice, use cascode device**
    - We're ignoring C_{gd} in this analysis



Calculation of Gain

- Assume load tank resonates at frequency w_o



- Assume $Z_{in} = R_s$

$$\Rightarrow \quad v_{gs} = \frac{v_{in}}{2R_s}\left(\frac{1}{jw_oC_{gs}}\right) = \left(\frac{Q}{j}\right)v_{in}$$

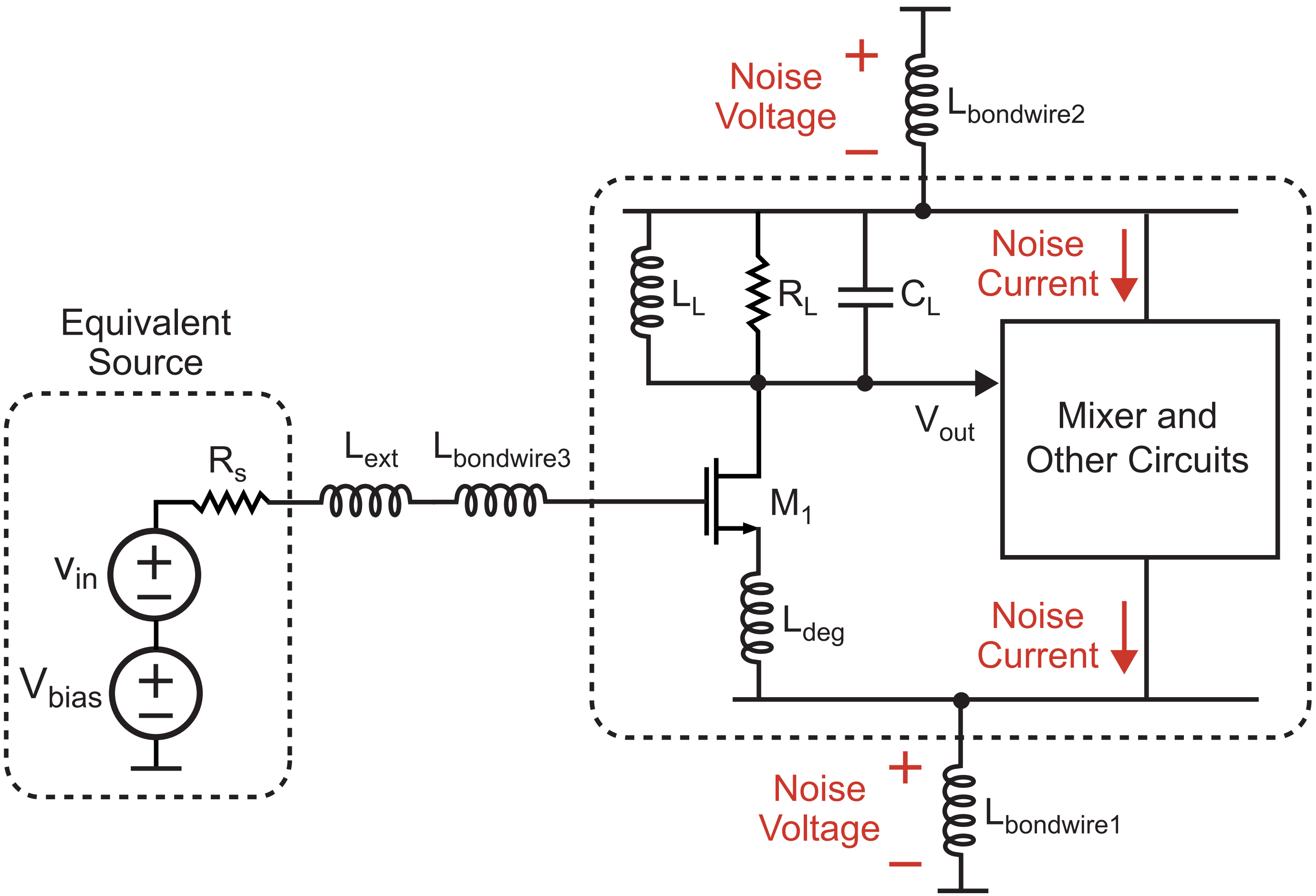
$$\Rightarrow \quad i_{out} = g_m\left(\frac{Q}{j}\right)v_{in} \qquad \Rightarrow \quad \boxed{v_{out} = -g_mR_L\left(\frac{Q}{j}\right)v_{in}}$$

Setting of Gain

$$|\text{Gain}| = g_m R_L Q$$

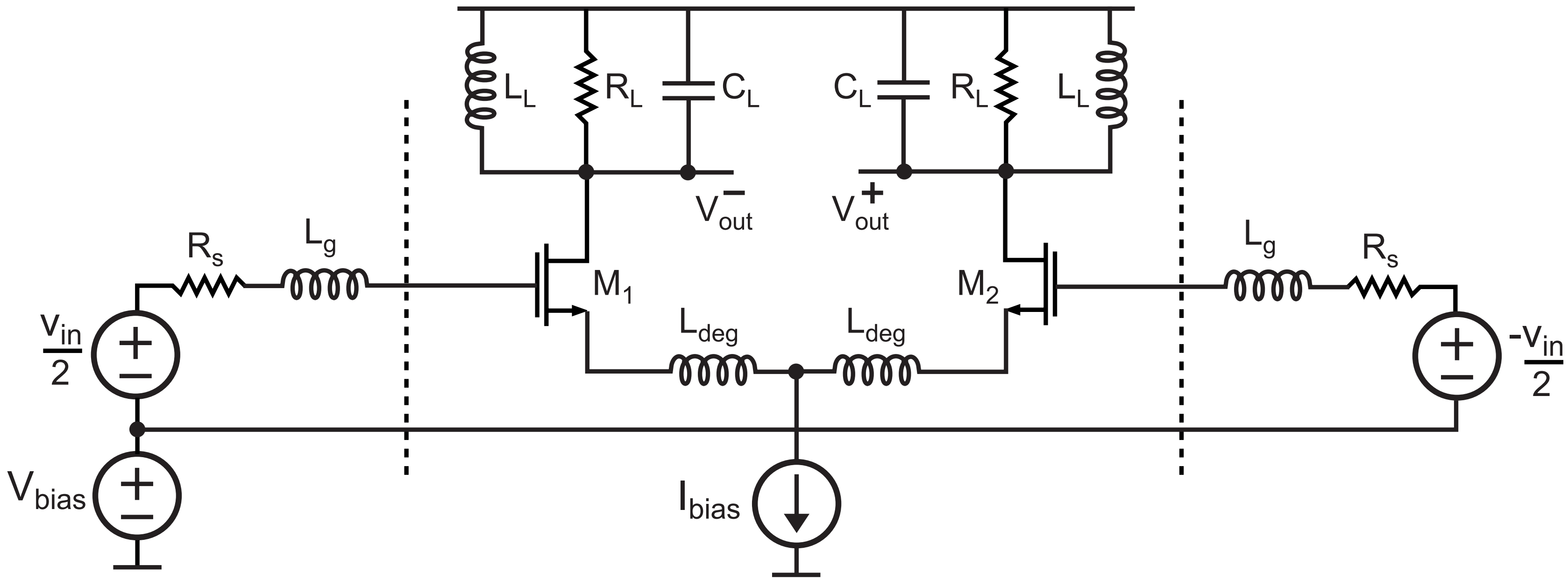
- **Parameters g_m and Q were set by Noise Figure and IIP3 considerations**
  - **Note that Q is of the input matching network, not the amplifier load**
- **R_L is the free parameter – use it to set the desired gain**
  - **Note that higher R_L for a given resonant frequency and capacitive load will increase Q_L (i.e., Q of the amplifier load)**
    - There is a tradeoff between amplifier bandwidth and gain
  - **Generally set R_L according to overall receiver noise and IIP3 requirements (higher gain is better for noise)**
    - Very large gain (i.e., high Q_L) is generally avoided to minimize sensitivity to process/temp variations that will shift the center frequency

The Issue of Package Parasitics



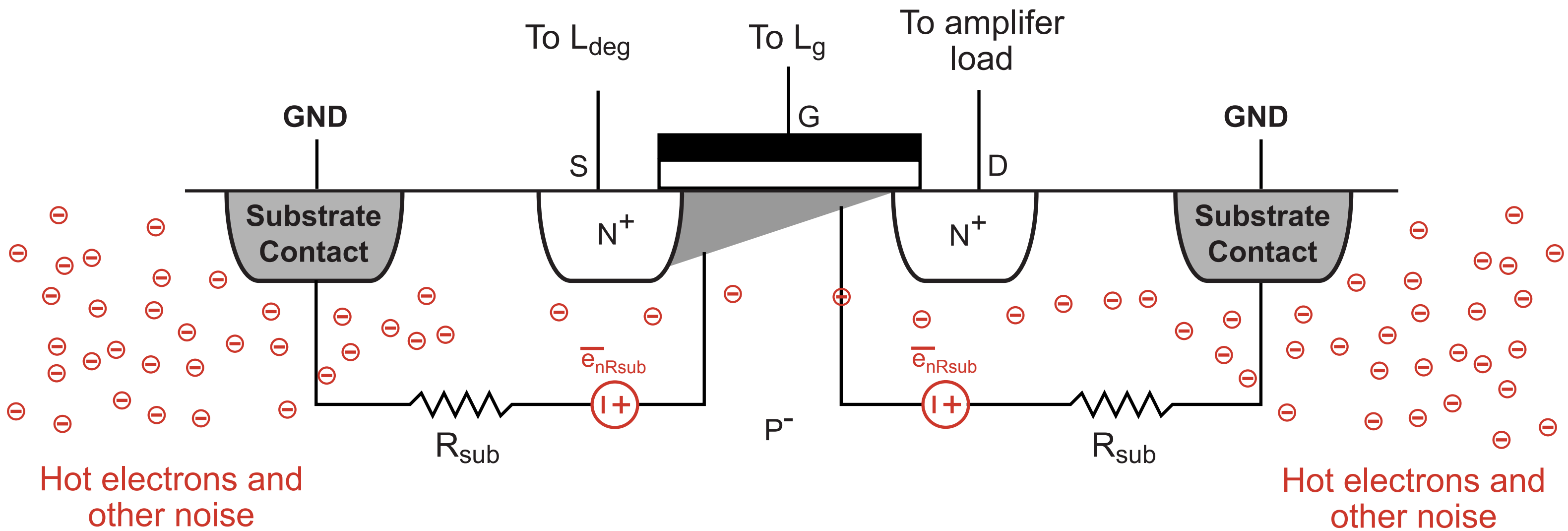
- **Bondwire (and package) inductance causes two issues**
  - **Value of degeneration inductor is altered**
  - **Noise from other circuits couples into LNA**

Differential LNA



- **Advantages**
  - **Value of L_{deg} is now much better controlled**
  - **Much less sensitivity to noise from other circuits**
- **Disadvantages**
  - **Twice the power as the single-ended version**
  - **Requires differential input at the chip**

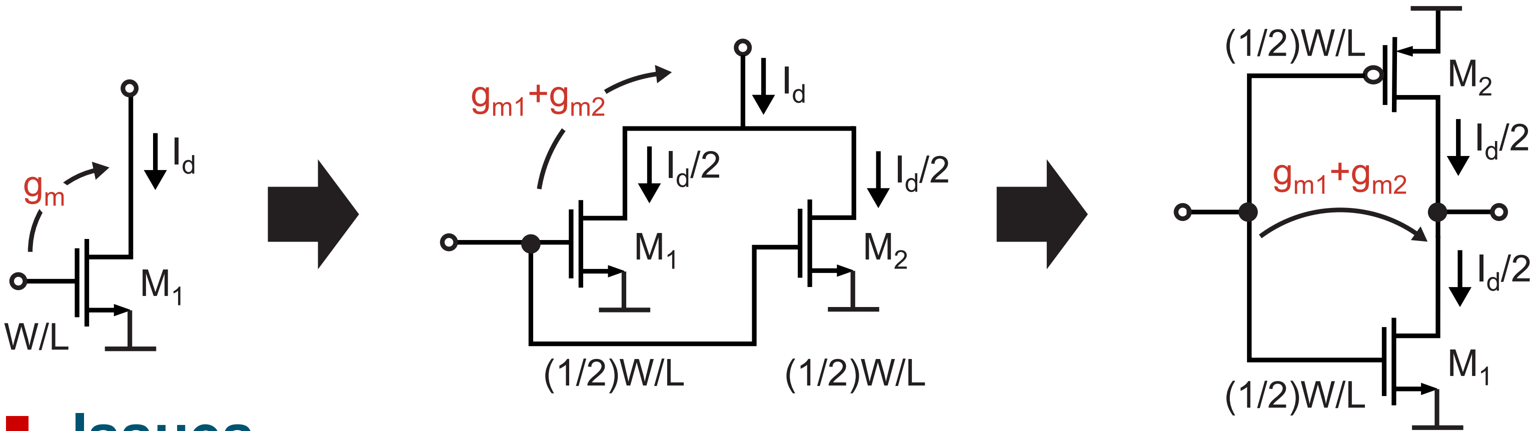
Note: Be Generous with Substrate Contact Placement



- **Having an abundance of nearby substrate contacts helps in three ways**
  - **Reduces possibility of latch up issues**
  - **Lowers R_{sub} and its associated noise**
    - Impacts LNA through backgate effect (g_{mb})
  - **Absorbs stray electrons from other circuits that will otherwise inject noise into the LNA**
- **Negative: takes up a bit extra area**

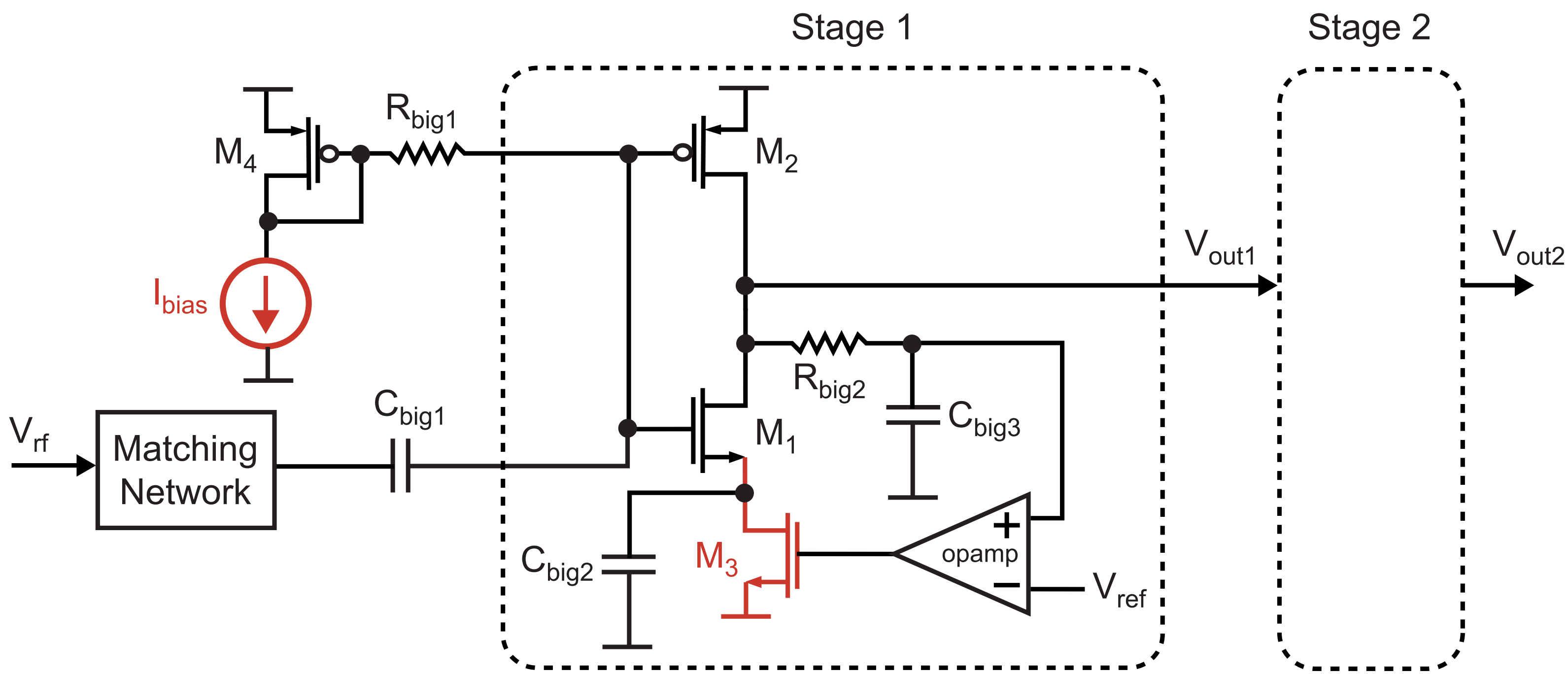
Another CMOS LNA Topology

- **Consider increasing g_m for a given current by using both PMOS and NMOS devices**
  - **Key idea: re-use of current**



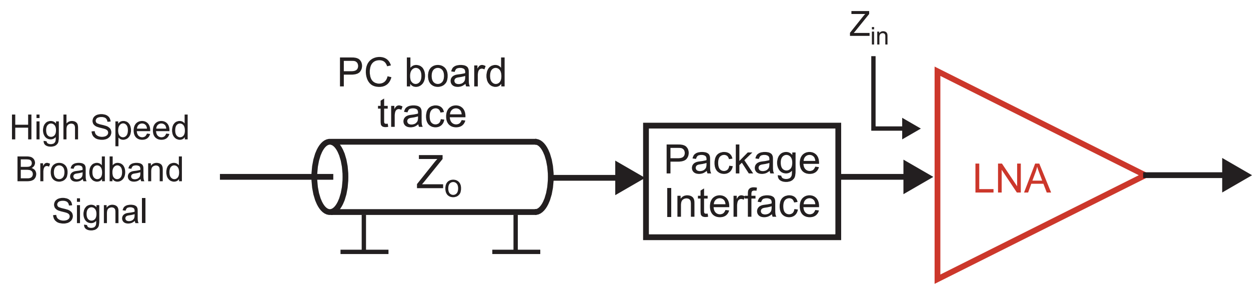
- **Issues**
  - **PMOS device has poorer transconductance than NMOS for a given amount of current, and f_t is lower**
  - **Not completely clear there is an advantage to using this technique, but published results are good**
    - See A. Karanicolas, “A 2.7 V 900-MHz CMOS LNA and Mixer”, JSSC, Dec 1996

Biasing for LNA Employing Current Re-Use



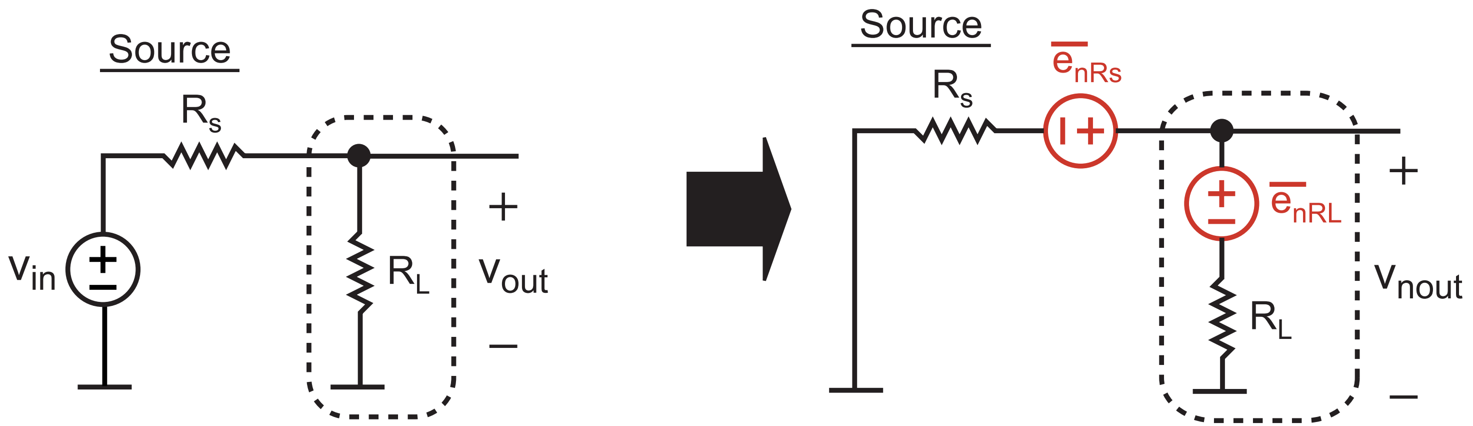
- PMOS is biased using a current mirror
- NMOS current adjusted to match the PMOS current
- Note: not clear how the matching network is achieving a 50 Ohm match
  - Perhaps parasitic bondwire inductance is degenerating the PMOS or NMOS transistors?

Broadband LNA Design



- **Most broadband systems are not as stringent on their noise requirements as wireless counterparts**
- **Equivalent input voltage is often specified rather than a Noise Figure**
- **Typically use a resistor to achieve a broadband match to input source**
  - **We know from Lecture 8 that this will limit the noise figure to be higher than 3 dB**
- **For those cases where low Noise Figure is important, are there alternative ways to achieve a broadband match?**

Recall Noise Factor Calculation for Resistor Load



- **Total output noise**

$$\overline{v^2_{nout(tot)}} = \left(\frac{R_L}{R_s + R_L}\right)^2 \overline{e^2_{nRs}} + \left(\frac{R_s}{R_s + R_L}\right)^2 \overline{e^2_{nRL}}$$

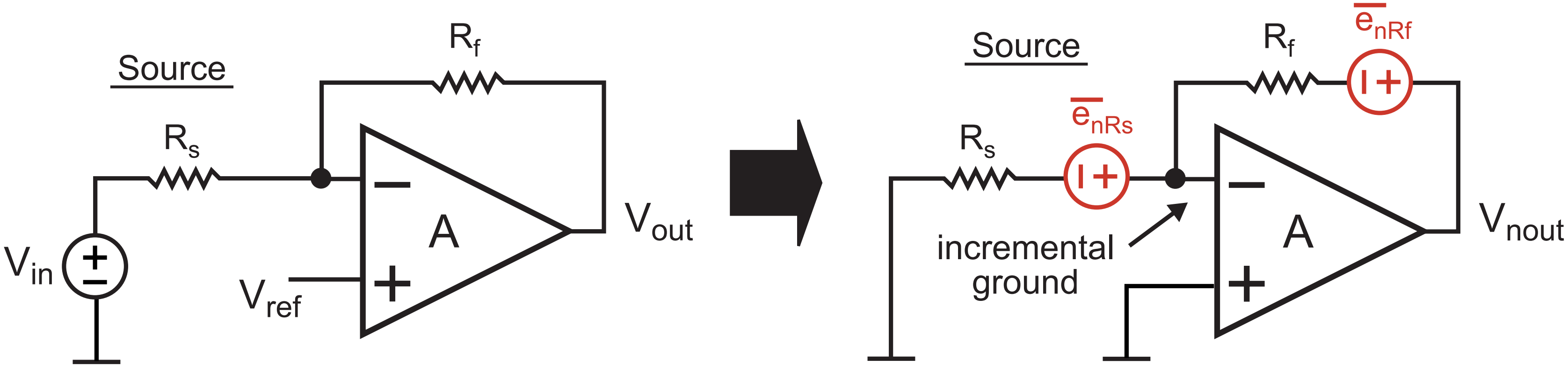
- **Total output noise due to source**

$$\overline{v^2_{nout(in)}} = \left(\frac{R_L}{R_s + R_L}\right)^2 \overline{e^2_{nRs}}$$

- **Noise Factor**

$$F = 1 + \left(\frac{R_s}{R_L}\right)^2 \frac{\overline{e^2_{nRL}}}{\overline{e^2_{nRs}}} = 1 + \left(\frac{R_s}{R_L}\right)^2 \frac{4kTR_L}{4kTR_s} = \boxed{1 + \frac{R_s}{R_L}}$$

Noise Figure For Amp with Resistor in Feedback



- **Total output noise (assume A is large)**

$$\overline{v^2_{nout(tot)}} \approx \left(\frac{-R_f}{R_s}\right)^2 \overline{e^2_{nRs}} + \overline{e^2_{nRf}}$$

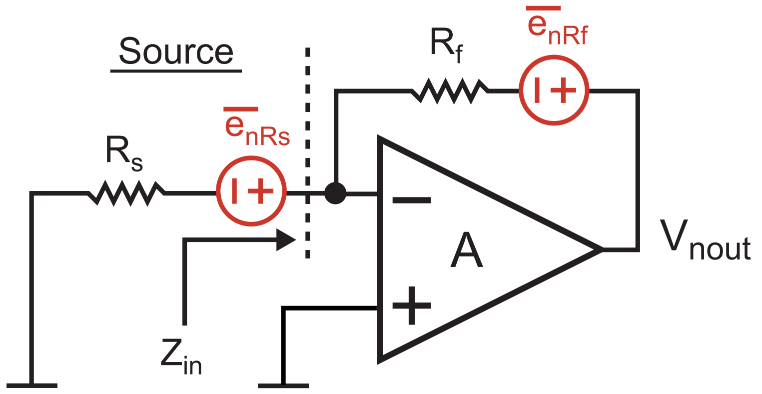
- **Total output noise due to source (assume A is large)**

$$\overline{v^2_{nout(in)}} \approx \left(\frac{-R_f}{R_s}\right)^2 \overline{e^2_{nRs}}$$

- **Noise Factor**

$$F \approx 1 + \left(\frac{R_s}{R_f}\right)^2 \frac{\overline{e^2_{nRf}}}{\overline{e^2_{nRs}}} = 1 + \left(\frac{R_s}{R_f}\right)^2 \frac{4kTR_f}{4kTR_s} = \boxed{1 + \frac{R_s}{R_f}}$$

Input Impedance For Amp with Resistor in Feedback



- **Recall from Miller effect discussion that**

$$Z_{in} = \frac{Z_f}{1 - gain} = \frac{R_f}{1 + A}$$

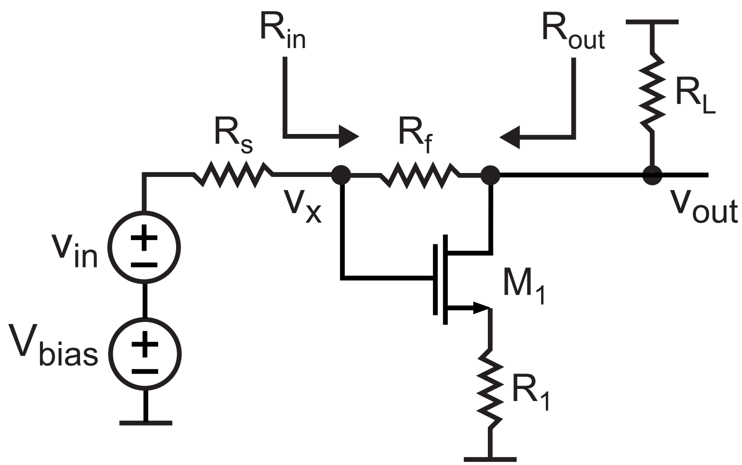
- **If we choose Z_{in} to match R_s, then**

$$R_f = (1 + A)Z_{in} = (1 + A)R_s$$

- **Therefore, Noise Figure lowered by being able to choose a large value for R_f since**

$$F \approx 1 + \frac{R_s}{R_f}$$

Example – Series-Shunt Amplifier



- **Recall that the above amplifier was analyzed in Lecture 5**
- **Tom Lee points out that this amplifier topology is actually used in noise figure measurement systems such as the Hewlett-Packard 8970A**
  - **It is likely to be a much higher performance transistor than a CMOS device, though**