LECTURE 020 –REVIEW OF CMOS TECHNOLOGY

INTRODUCTION

Objective

Provide sufficient background to understand the limits and capabilities of CMOS technology applied to PLLs.

Organization:

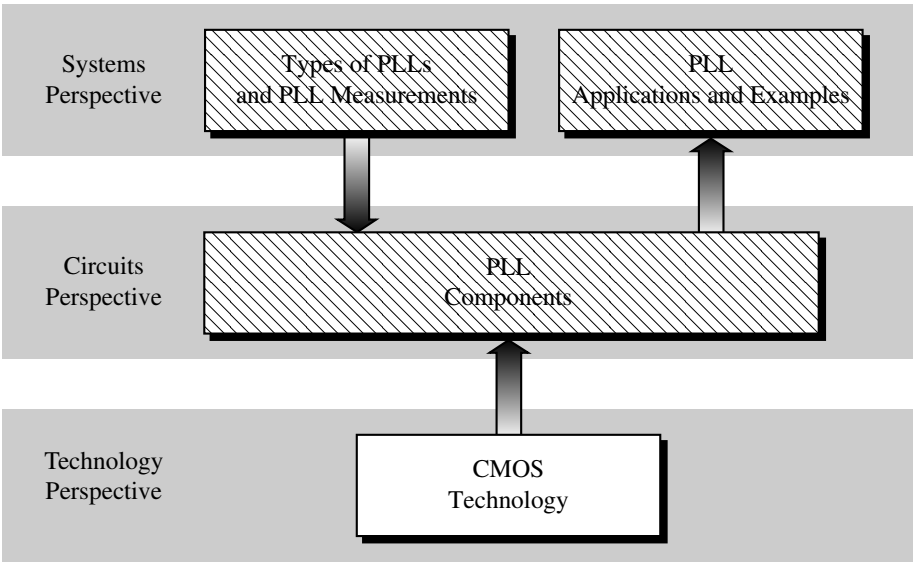
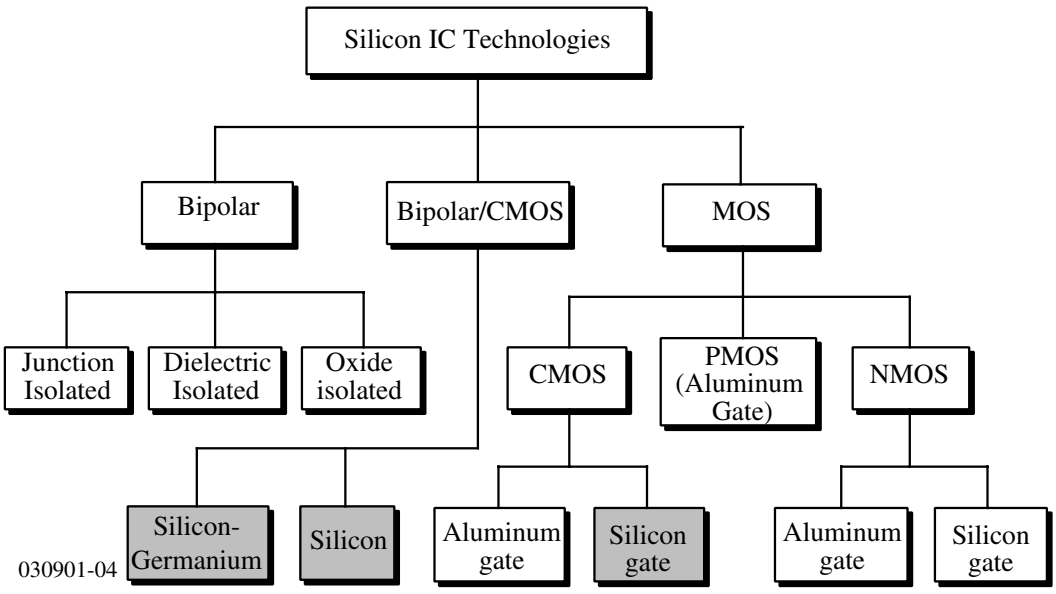


Fig. 030901-02

Classification of Silicon Technology



030901-04

Why CMOS Technology?

Comparison of BJT and MOSFET technology from an analog viewpoint:

Feature	BJT	MOSFET
Cutoff Frequency(f_T)	100 GHz	50 GHz (0.25μm)
Noise (thermal about the same)	Less 1/f	More 1/f
DC Range of Operation	9 decades of exponential current versus v_{BE}	2-3 decades of square law behavior
Small Signal Output Resistance	Slightly larger	Smaller for short channel
Switch Implementation	Poor	Good
Capacitor Implementation	Voltage dependent	Reasonably good

Therefore,

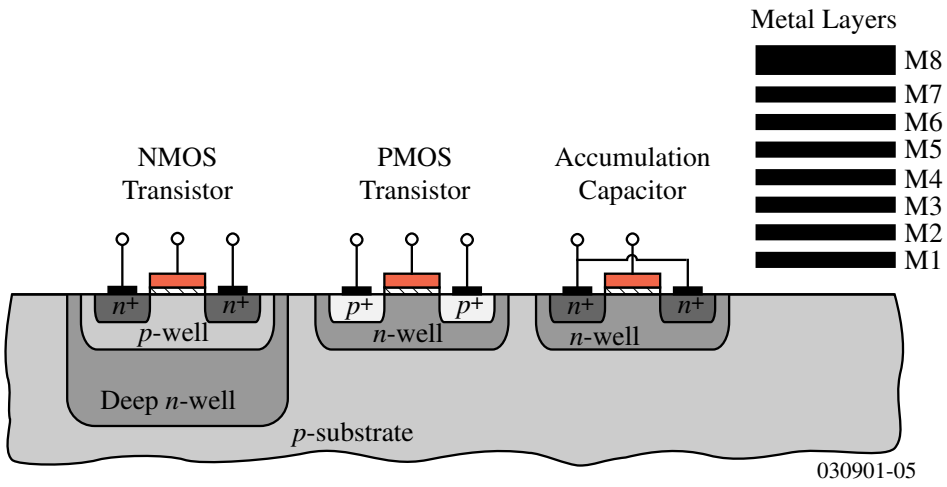
- Almost every comparison favors the BJT, *however* a similar comparison made from a digital viewpoint would come up on the side of CMOS.
- Therefore, since large-volume technology will be driven by digital demands, CMOS is an obvious result as the technology of availability.

Other factors:

- The potential for technology improvement for CMOS is greater than for BJT
- Performance generally increases with decreasing channel length

Components of a Modern CMOS Technology

Illustration of a modern CMOS process:



In addition to NMOS and PMOS transistors, the technology provides:

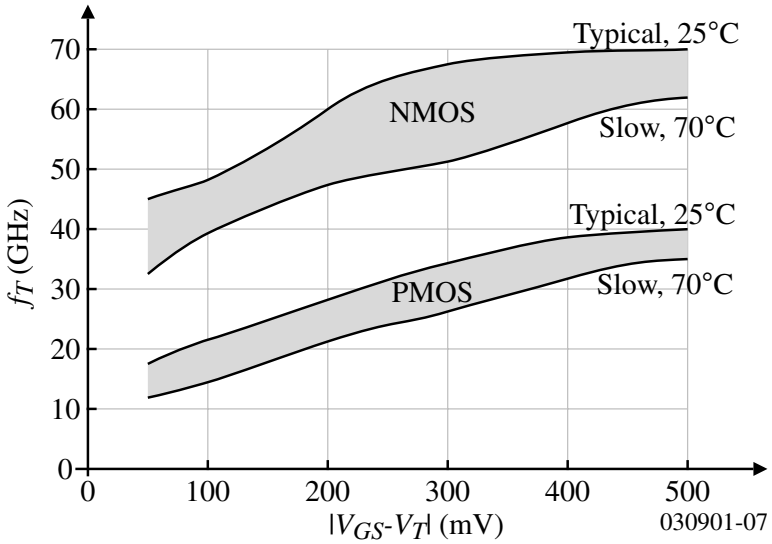
1.) A deep *n*-well that can be utilized to reduce substrate noise coupling.

2.) A MOS varactor that can serve in VCOs

3.) At least 6 levels of metal that can form many useful structures such as inductors, capacitors, and transmission lines.

CMOS Components – Transistors

f_T as a function of gate-source overdrive, V_{GS}-V_T (0.13μm):



The upper frequency limit is probably around 40 GHz for NMOS with an f_T in the vicinity of 60GHz with an overdrive of 0.5V and at the slow-high temperature corner.

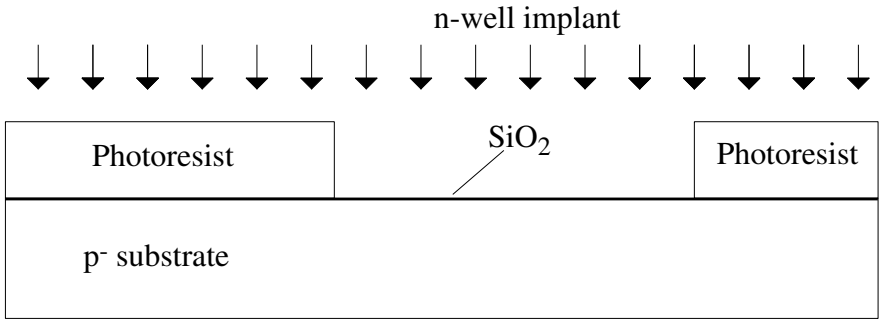
TYPICAL CMOS FABRICATION PROCESS

N-Well CMOS Fabrication Major Steps

1.) Implant and diffuse the n-well
2.) Deposition of silicon nitride
3.) n-type field (channel stop) implant
4.) p-type field (channel stop) implant
5.) Grow a thick field oxide (FOX)
6.) Grow a thin oxide and deposit polysilicon
7.) Remove poly and form LDD spacers
8.) Implantation of NMOS S/D and n-material contacts
9.) Remove spacers and implant NMOS LDDs
10.) Repeat steps 8.) and 9.) for PMOS
11.) Anneal to activate the implanted ions
12.) Deposit a thick oxide layer (BPSG - borophosphosilicate glass)
13.) Open contacts, deposit first level metal and etch unwanted metal
14.) Deposit another interlayer dielectric (CVD SiO_2), open vias, deposit 2nd level metal
15.) Etch unwanted metal, deposit a passivation layer and open over bonding pads

Major CMOS Process Steps

Step 1 - Implantation and diffusion of the n-wells



Step 2 - Growth of thin oxide and deposition of silicon nitride

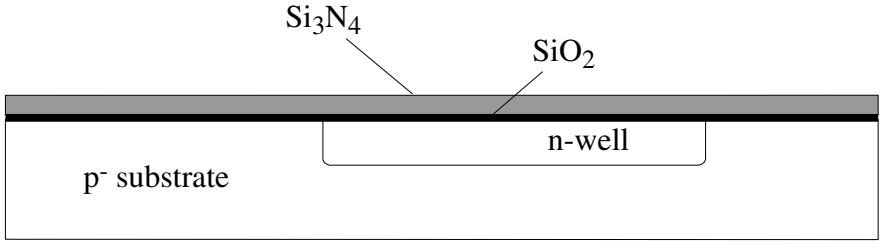
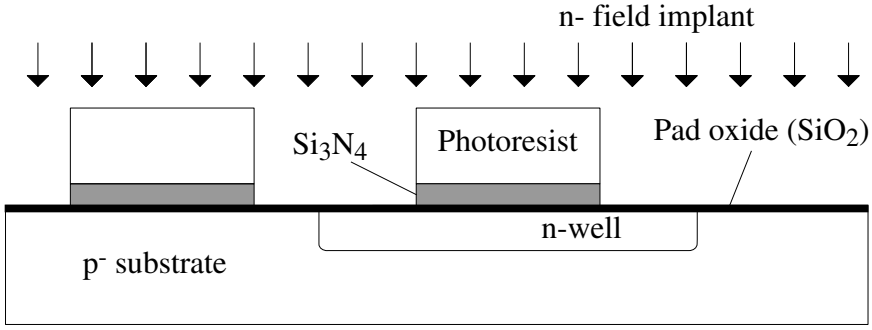


Fig. 180-01

Major CMOS Process Steps - Continued

Step 3.) Implantation of the n-type field channel stop



Step 4.) Implantation of the p-type field channel stop

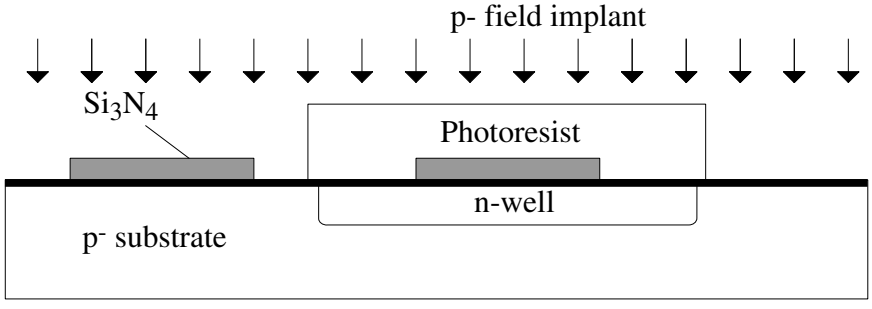
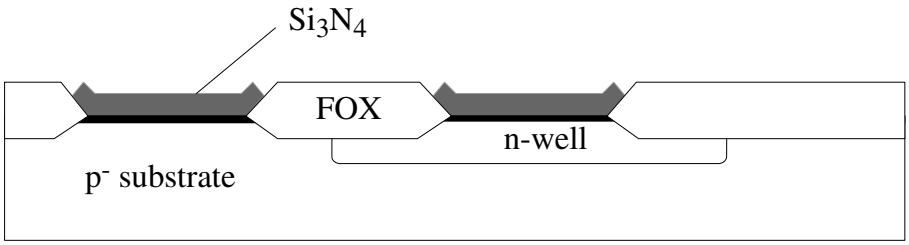


Fig. 180-02

Major CMOS Process Steps – Continued

Step 5.) Growth of the thick field oxide (LOCOS - *loc*alized *o*xidation of *s*ilicon)



Step 6.) Growth of the gate thin oxide and deposition of polysilicon. The thresholds can be shifted by an implantation before the deposition of polysilicon.

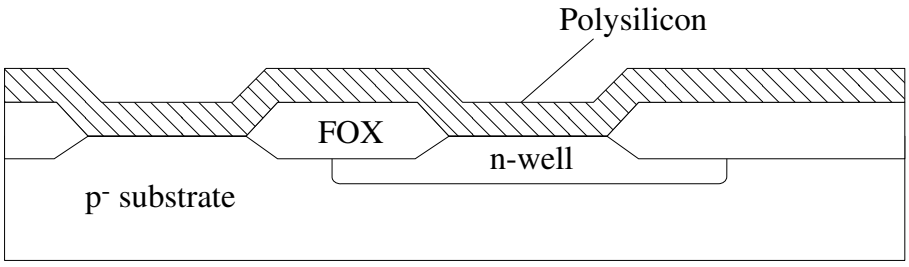
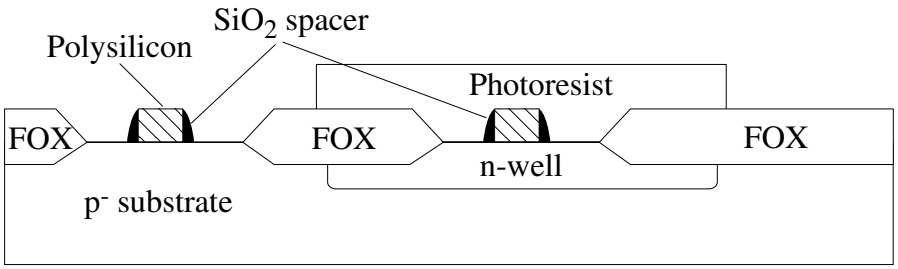


Fig. 180-03

Major CMOS Process Steps - Continued

Step 7.) Removal of polysilicon and formation of the sidewall spacers



Step 8.) Implantation of NMOS source and drain and contact to n-well (not shown)

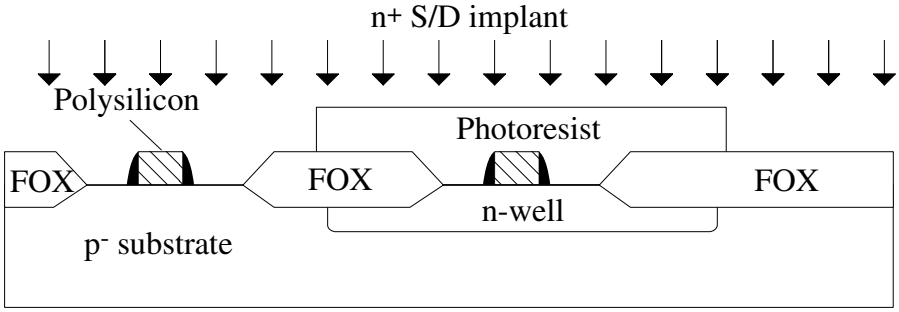
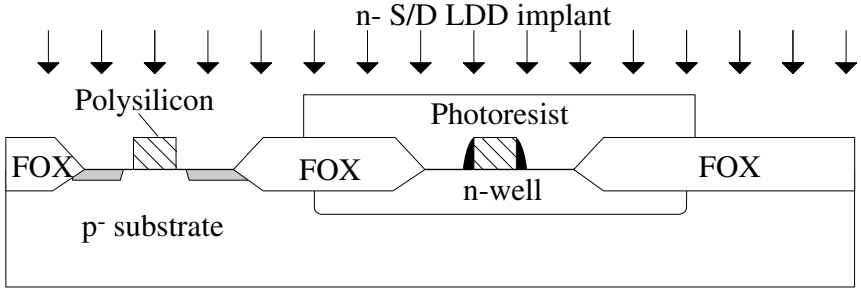


Fig. 180-04

Major CMOS Process Steps - Continued

Step 9.) Remove sidewall spacers and implant the NMOS lightly doped source/drains



Step 10.) Implant the PMOS source/drains and contacts to the p- substrate (not shown), remove the sidewall spacers and implant the PMOS lightly doped source/drains

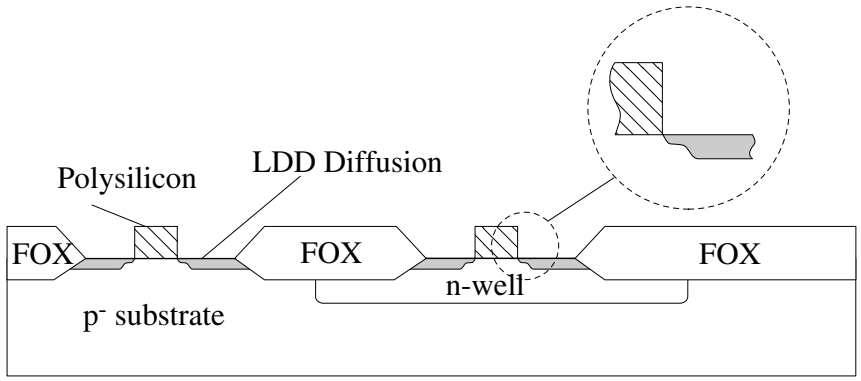
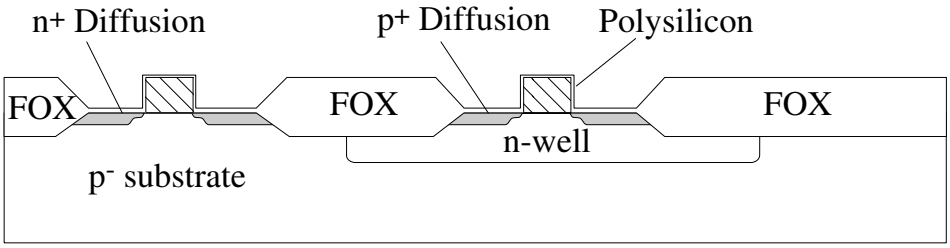


Fig. 180-05

Major CMOS Process Steps – Continued

Step 11.) Anneal to activate the implanted ions



Step 12.) Deposit a thick oxide layer (BPSG - borophosphosilicate glass)

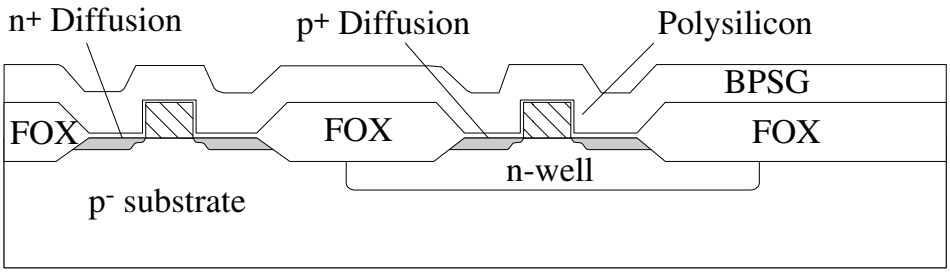
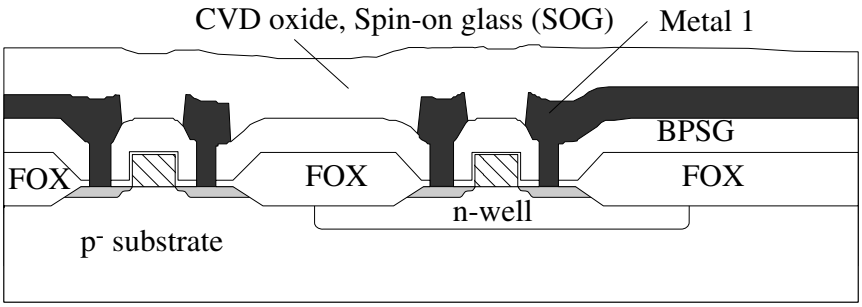


Fig. 180-06

Major CMOS Process Steps - Continued

Step 13.) Open contacts, deposit first level metal and etch unwanted metal



Step 14.) Deposit another interlayer dielectric (CVD SiO_2), open contacts, deposit second level metall

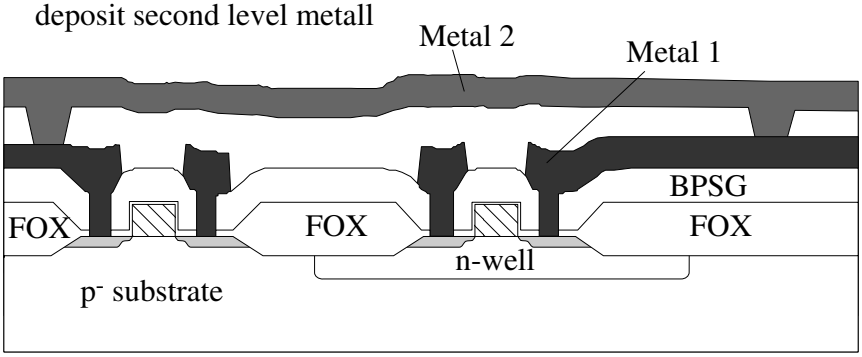


Fig. 180-07

Major CMOS Process Steps – Continued

Step 15.) Etch unwanted metal and deposit a passivation layer and open over bonding pads

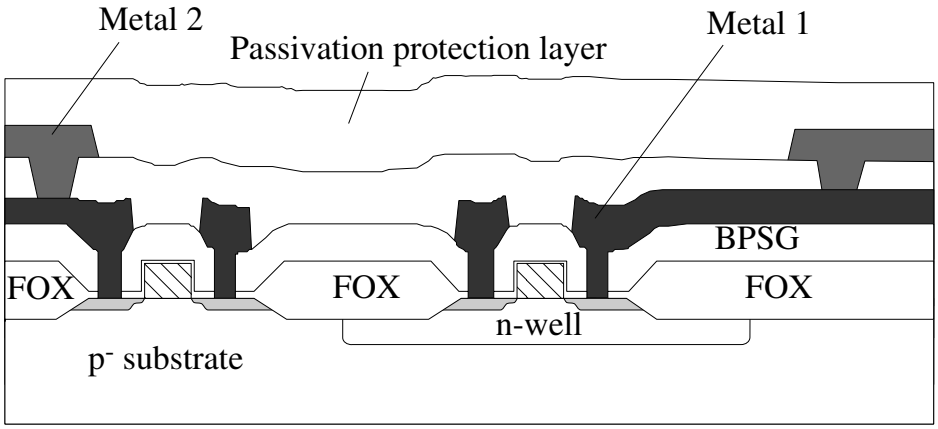


Fig. 180-08

p-well process is similar but starts with a p-well implant rather than an n-well implant.

Approximate Side View of CMOS Fabrication

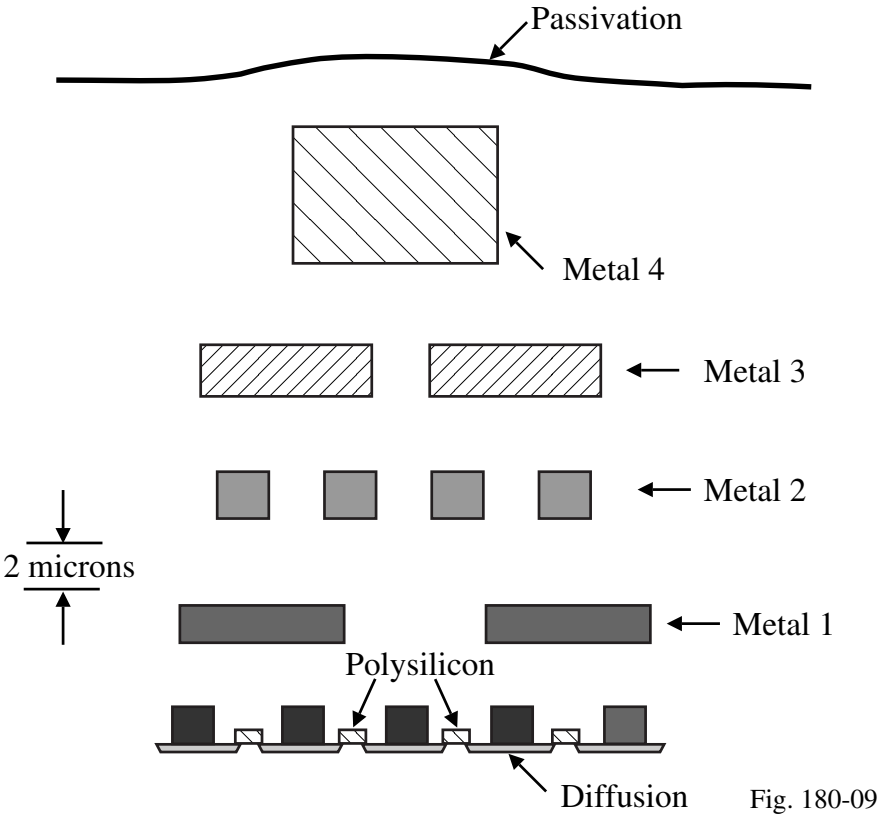
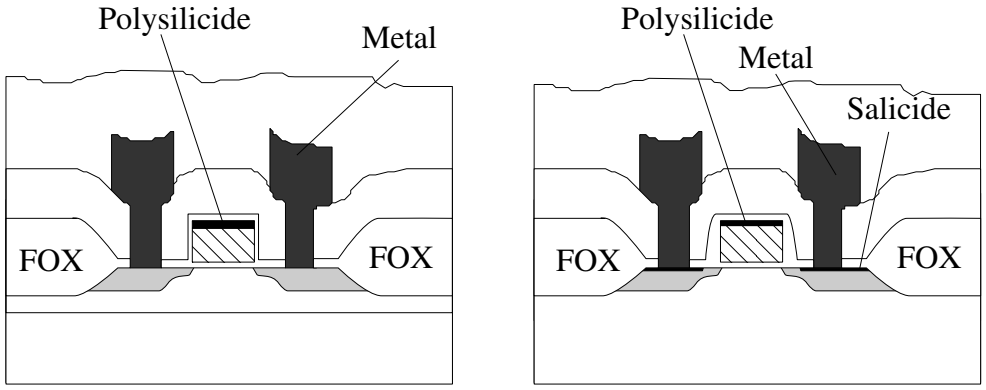


Fig. 180-09

Silicide/Salicide Technology

Used to reduce interconnect resistivity by placing a low-resistance silicide such as $TiSi_2$, WSi_2, $TaSi_2$, etc. on top of polysilicon

Salicide technology (self-aligned silicide) provides low resistance source/drain connections as well as low-resistance polysilicon.



Polycide structure Salicide structure

Fig 180-10

Scanning Electron Microscope of a MOSFET Cross-section

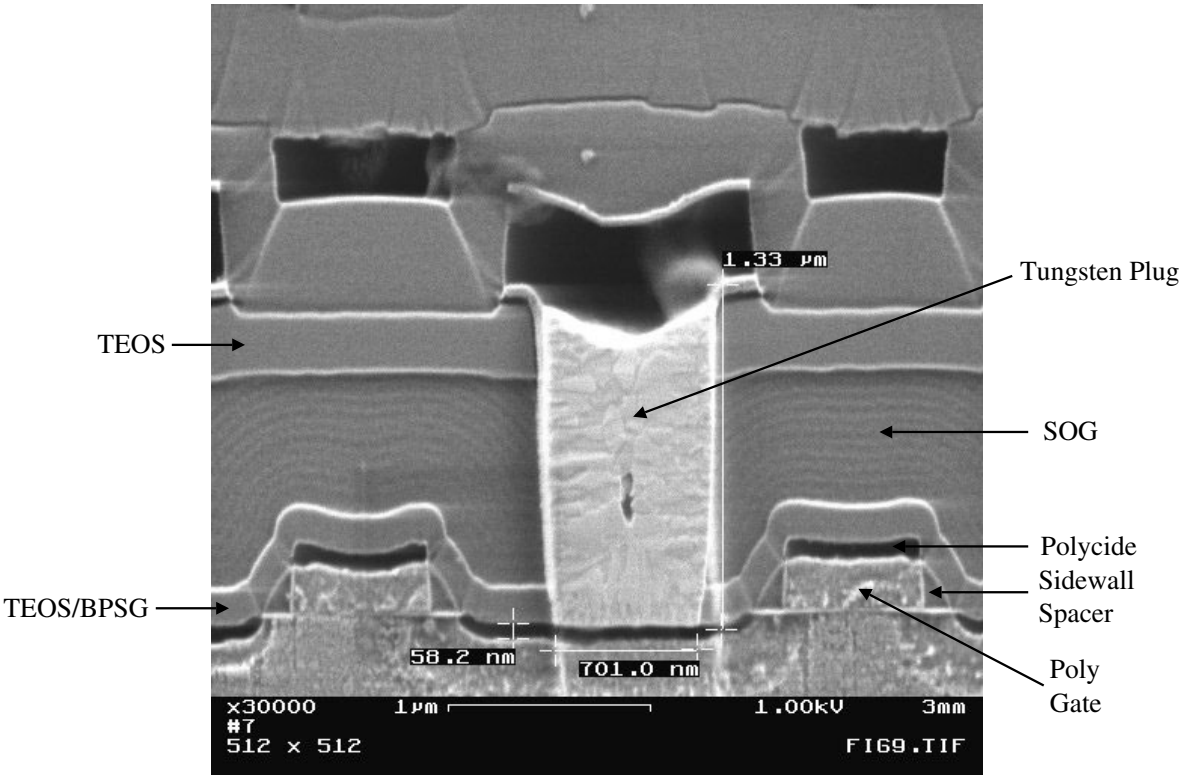


Fig. 2.8-20

Scanning Electron Microscope Showing Metal Levels and Interconnect

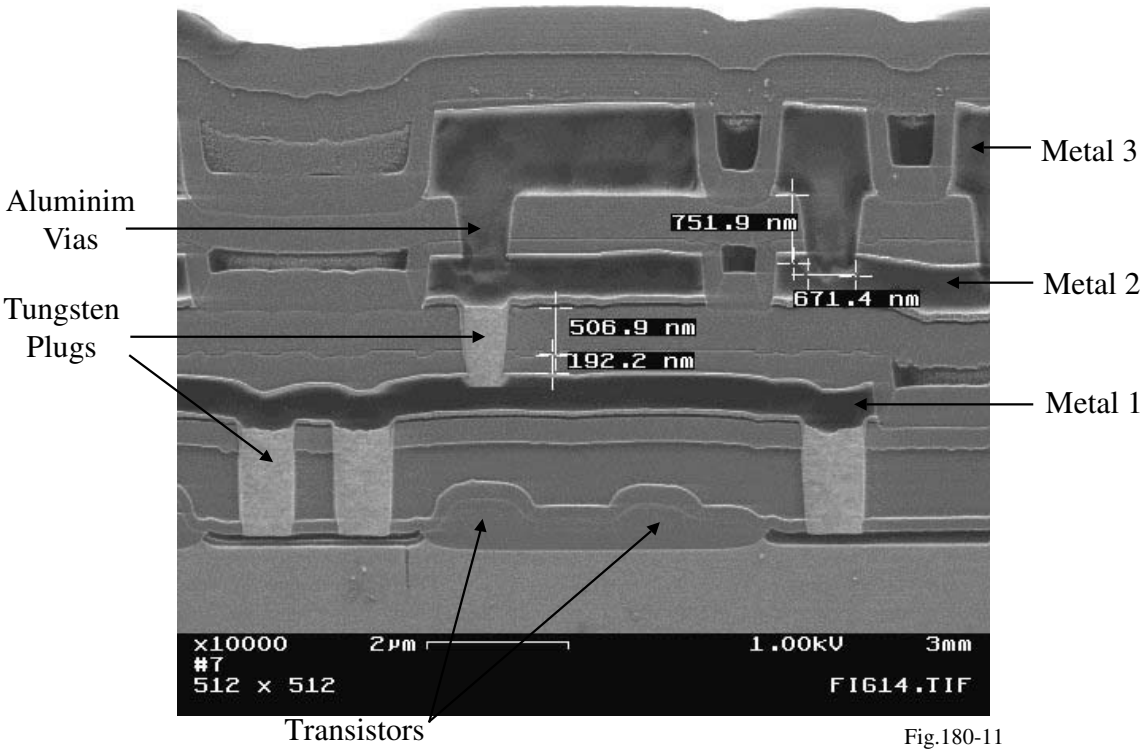


Fig.180-11

RESISTORS COMPATIBLE WITH CMOS TECHNOLOGY

MOS Resistors - Source/Drain Resistor

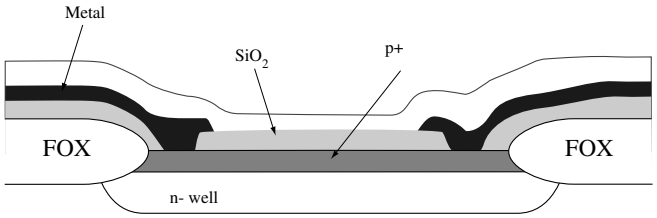


Fig. 2.5-16

Diffusion:

10-100 ohms/square
Absolute accuracy = ±35%
Relative accuracy=2% (5µm), 0.2% (50µm)
Temperature coefficient = +1500 ppm/°C
Voltage coefficient ≈ 200 ppm/V

Ion Implanted:

500-2000 ohms/square
Absolute accuracy = ±15%
Relative accuracy=2% (5µm), 0.15% (50µm
Temperature coefficient = +400 ppm/°C
Voltage coefficient ≈ 800 ppm/V

Comments:

- Parasitic capacitance to substrate is voltage dependent.
- Piezoresistance effects occur due to chip strain from mounting.

Polysilicon Resistor

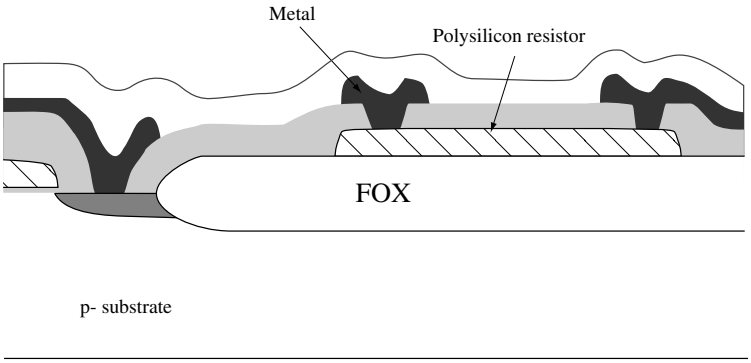


Fig. 2.5-17

30-100 ohms/square (unshielded)
100-500 ohms/square (shielded)
Absolute accuracy = ±30%
Relative accuracy = 2% (5 µm)
Temperature coefficient = 500-1000 ppm/°C
Voltage coefficient ≈ 100 ppm/V

Comments:

- Used for fuzzes and laser trimming
- Good general resistor with low parasitics

N-well Resistor

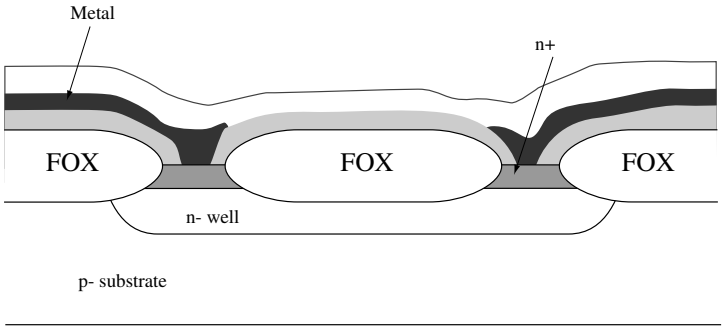


Fig. 2.5-18

1000-5000 ohms/square

Absolute accuracy = ±40%

Relative accuracy ≈ 5%

Temperature coefficient = 4000 ppm/°C

Voltage coefficient is large ≈ 8000 ppm/V

Comments:

- Good when large values of resistance are needed.
- Parasitics are large and resistance is voltage dependent

CAPACITORS COMPATIBLE WITH CMOS TECHNOLOGY

Types of Capacitors Considered

- pn junction capacitors
- Standard MOS capacitors
- Accumulation mode MOS capacitors
- Poly-poly capacitors
- Metal-metal capacitors

Characterization of Capacitors

Assume C is the desired capacitance:

1.) Dissipation (quality factor) of a capacitor is

$$Q = \omega C R_p$$

where R_p is the equivalent resistance in parallel with the capacitor, C.

2.) C_{max}/C_{min} ratio is the ratio of the largest value of capacitance to the smallest when the capacitor is used as a variable capacitor called *varactor*.

3.) Variation of capacitance with the control voltage.

4.) Parasitic capacitors from both terminal of the desired capacitor to ac ground.

Desirable Characteristics of Varactors

1.) A high quality factor

2.) A control voltage range compatible with supply voltage

3.) Good tunability over the available control voltage range

4.) Small silicon area (reduces cost)

5.) Reasonably uniform capacitance variation over the available control voltage range

6.) A high C_{max}/C_{min} ratio

Some References for Further Information

1.) P. Andreani and S. Mattisson, "On the Use of MOS Varactors in RF VCO's," *IEEE J. of Solid-State Circuits*, vol. 35, no. 6, June 2000, pp. 905-910.

2.) A-S Porret, T. Melly, C. Enz, and E. Vittoz, "Design of High-*Q* Varactors for Low-Power Wireless Applications Using a Standard CMOS Process," *IEEE J. of Solid-State Circuits*, vol. 35, no. 3, March 2000, pp. 337-345.

3.) E. Pedersen, "RF CMOS Varactors for 2GHz Applications," *Analog Integrated Circuits and Signal Processing*, vol. 26, pp. 27-36, Jan. 2001

PN Junction Capacitors

Generally made by diffusion into the well.

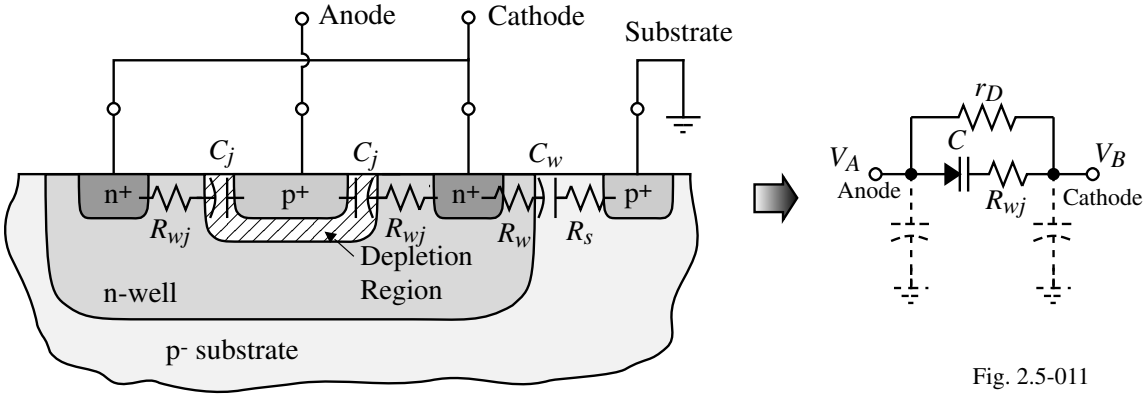


Fig. 2.5-011

Layout:

Minimize the distance between the p^+ and n^+ diffusions.

Two different versions have been tested.

1.) Large islands – 9μm on a side

2.) Small islands – 1.2μm on a side

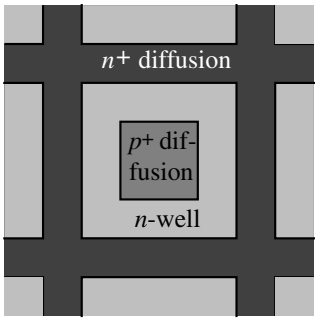


Fig. 2.5-1A

PN-Junction Capacitors – Continued

The anode should be the floating node and the cathode must be connected to ac ground.

Experimental data (Q at 2GHz, 0.5µm CMOS):

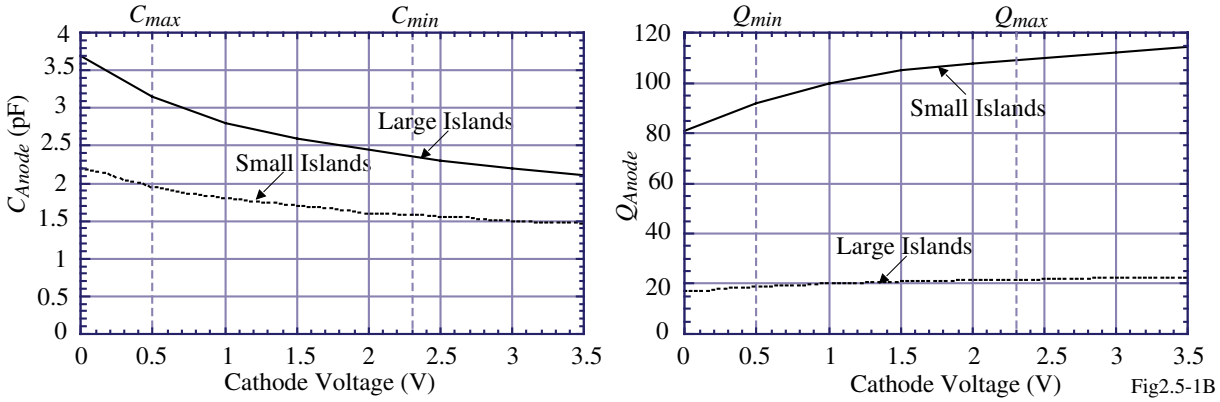


Fig2.5-1B

Summary:

Terminal Under Test	Small Islands (598 1.2µm x1.2µm)			Large Islands (42 9µm x 9µm)		
	C_{max}/C_{min}	Q_{min}	Q_{max}	C_{max}/C_{min}	Q_{min}	Q_{max}
Anode	1.23	94.5	109	1.32	19	22.6
Cathode	1.21	8.4	9.2	1.29	8.6	9.5

Electrons as majority carriers lead to higher Q because of their higher mobility.

The resistance, R_{wj}, is reduced in small islands compared with large islands ⇒ higher Q.

Single-Ended and Differential PN Junction Capacitors

Differential configurations can reduce the bulk resistances and increase the effective Q.

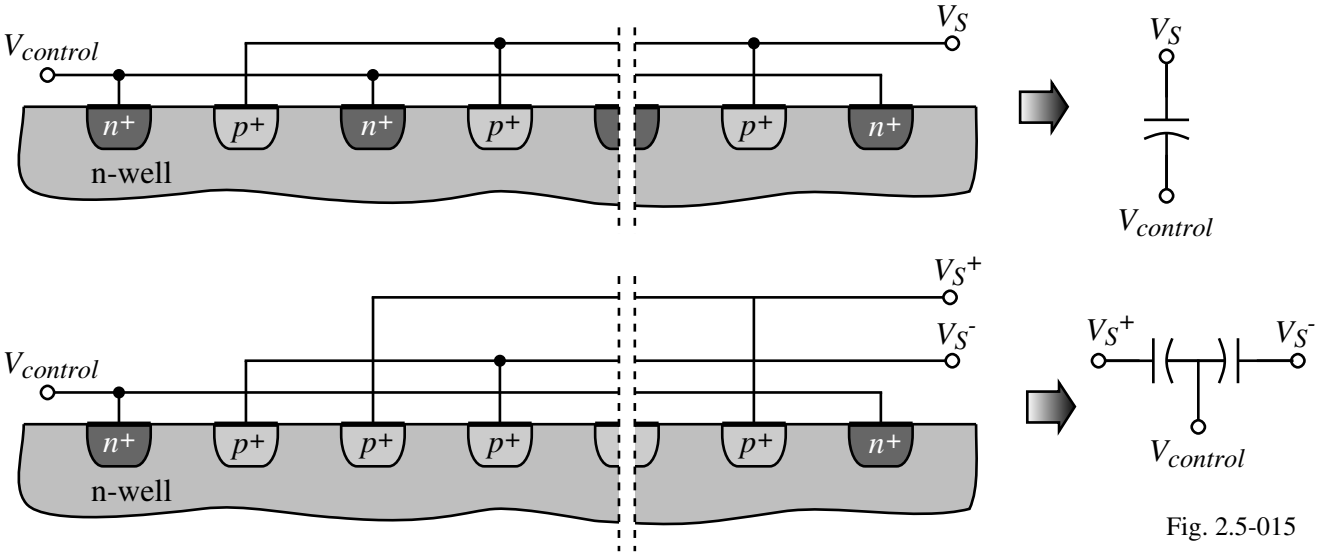


Fig. 2.5-015

An examination of the electric field lines shows that because the symmetry inherent in the differential configuration, the path to the small-signal ground can be shortened if devices with opposite polarity alternate.

Standard MOS Capacitor (D = S = B)

Conditions:

- D = S = B
- Operates from accumulation to inversion
- Nonmonotonic
- Nonlinear

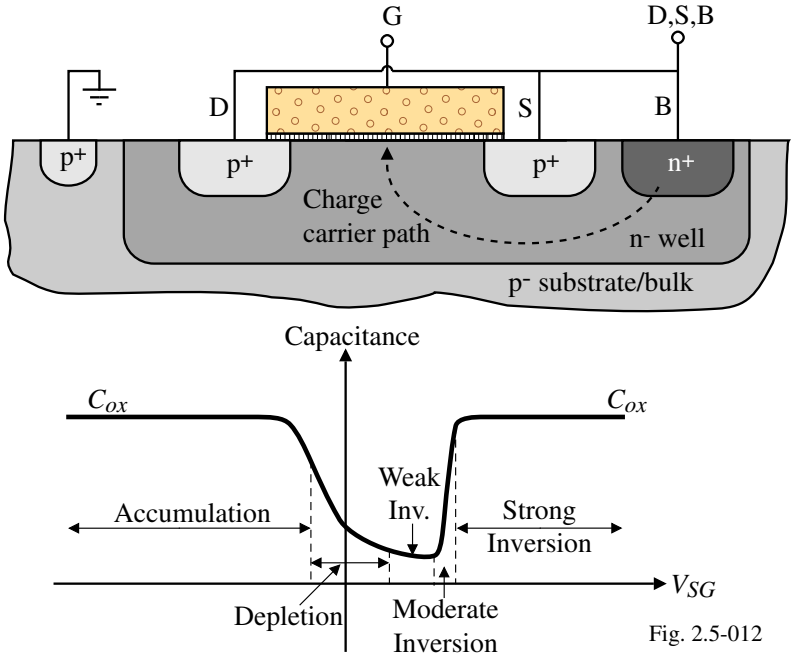


Fig. 2.5-012

Inversion Mode MOS Capacitors

Conditions:

- D = S, B = V_{DD}
- Accumulation region removed by connecting bulk to V_{DD}
- Channel resistance:

$$R_{on} = \frac{L}{12K_P'(V_{BG}-|V_T|)}$$

- LDD transistors will give lower Q because of the increased series resistance

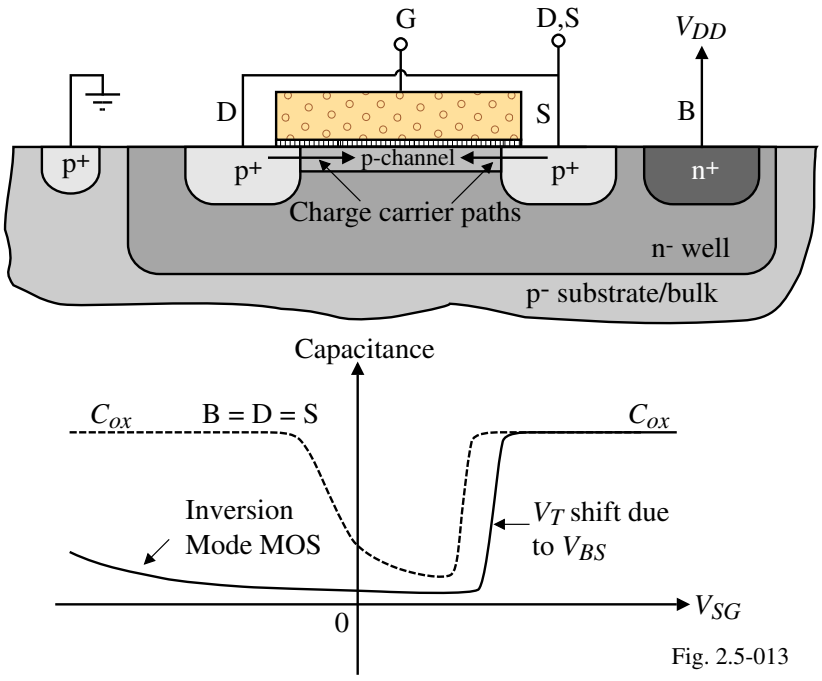
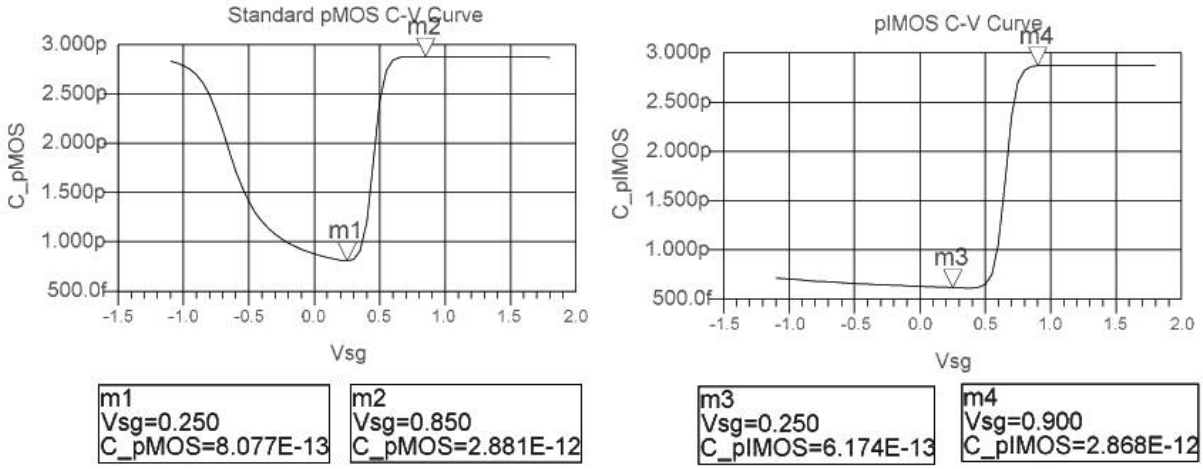


Fig. 2.5-013

Experimental Results for Standard and Inversion Mode 0.25µm CMOS Varactors

n-well:



Inversion Mode MOS Capacitors – Continued

Bulk tuning of the polysilicon-oxide-channel capacitor (0.35µm CMOS)

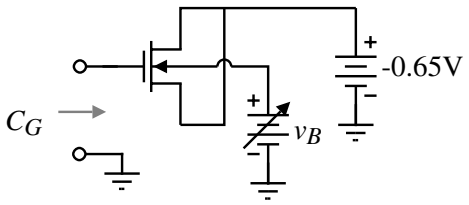
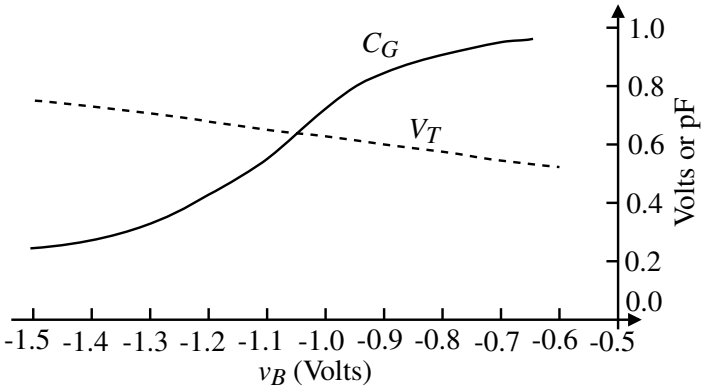


Fig. 2.5-3



$C_{max}/C_{min} \approx 4$

Interpretation:

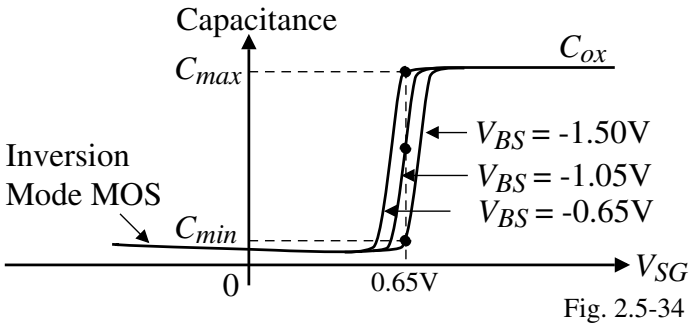


Fig. 2.5-34

Inversion Mode NMOS Varactor – Continued

More Detail - Includes the LDD transistor

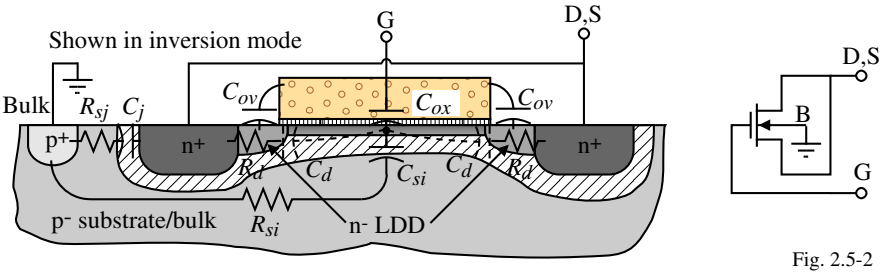


Fig. 2.5-2

Best results are obtained when the drain-source are on ac ground.

Experimental Results (Q at 2GHz, 0.5μm CMOS):

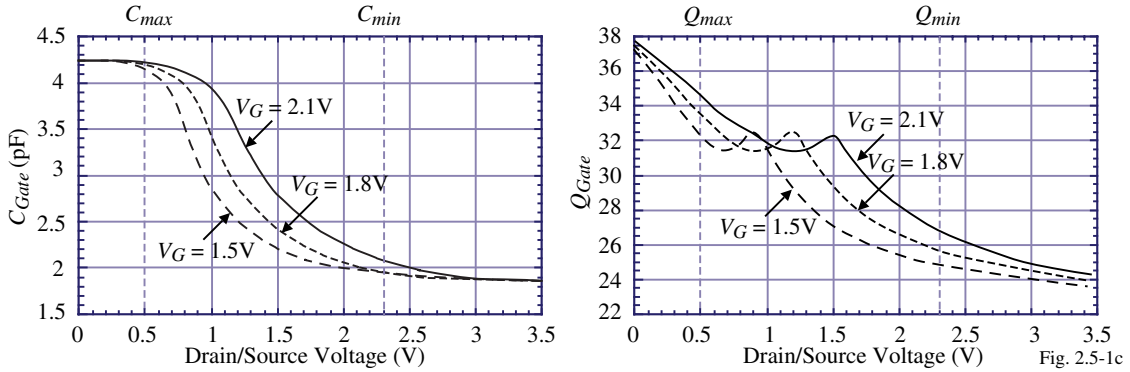


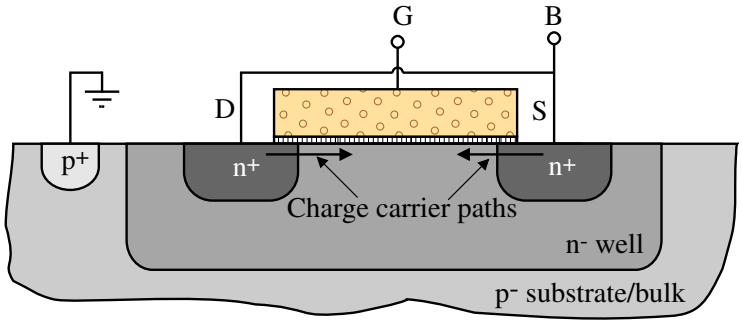
Fig. 2.5-1c

V_G =1.8V: C_{max}/C_{min} ratio = 2.15 (1.91), Q_{max} = 34.3 (5.4), and Q_{min} = 25.8(4.9)

Accumulation Mode MOS Capacitors

Conditions:

- Remove p+ drain and source and put n+ bulk contacts instead
- Generally not supported (yet) in most silicon foundries



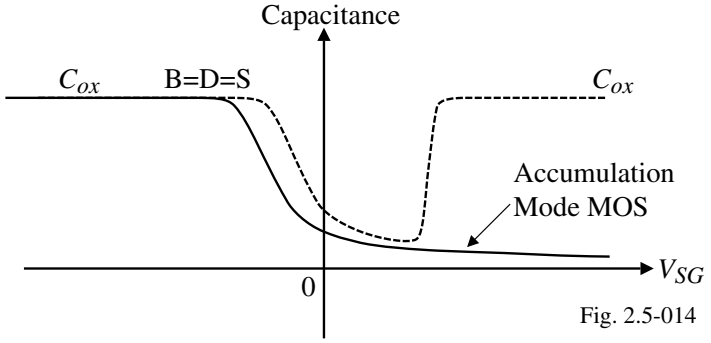


Fig. 2.5-014

Accumulation-Mode Capacitor – More Detail

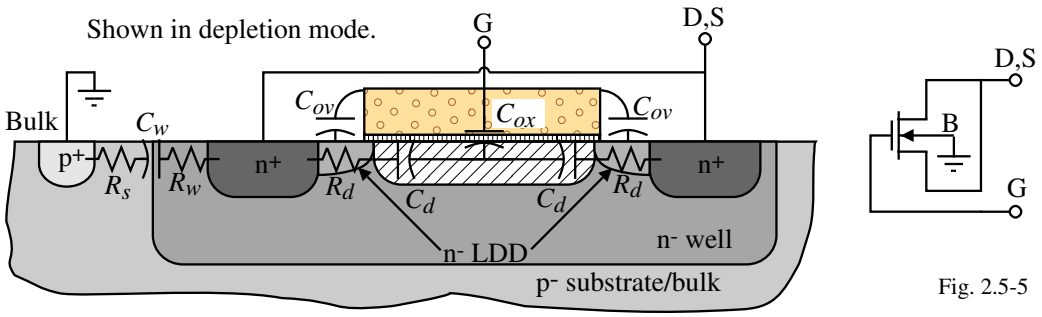


Fig. 2.5-5

Best results are obtained when the drain-source are on ac ground.

Experimental Results (Q at 2GHz, 0.5µm CMOS):

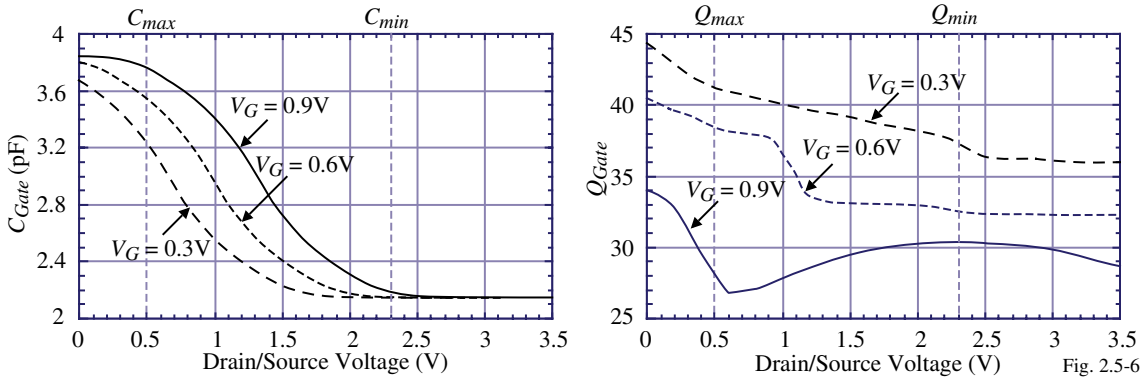


Fig. 2.5-6

$V_G = 0.6$V: C_{max}/C_{min} ratio = 1.69 (1.61), Q_{max} = 38.3 (15.0), and Q_{min} = 33.2(13.6)

Differential Varactors†

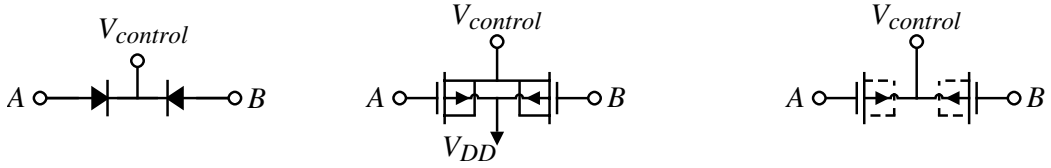
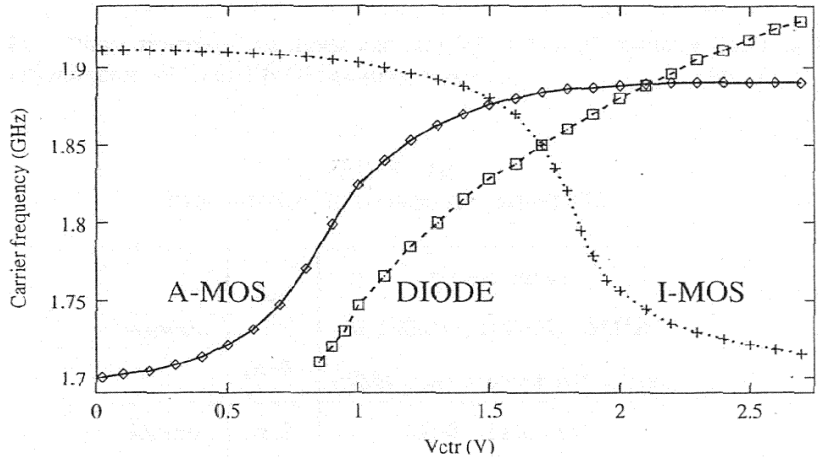


Fig. 040-01



Varactor	$f_L - f_H$ (GHz)	f_C (GHz)	Tuning Range
Diode	1.73-1.93	1.83	10.9%
I-MOS	1.71-1.91	1.81	11.0%
A-MOS	1.70-1.89	1.80	10.6%

† P. Andreani and S. Mattisson, "On the Use of MOS Varactors in RF VCO's," *IEEE J. of Solid-State Circuits*, Vol. 35, No. 6, June 2000, pp. 905-910.

Compensated MOS-Capacitors in Depletion with Substrate Biasing[†]

Substrate biasing keeps the MOS capacitors in a broad depletion region and extends the usable voltage range and achieves a first-order cancellation of the nonlinearity effect.

Principle:

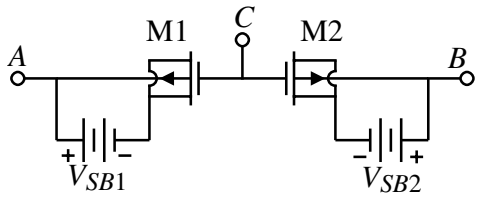
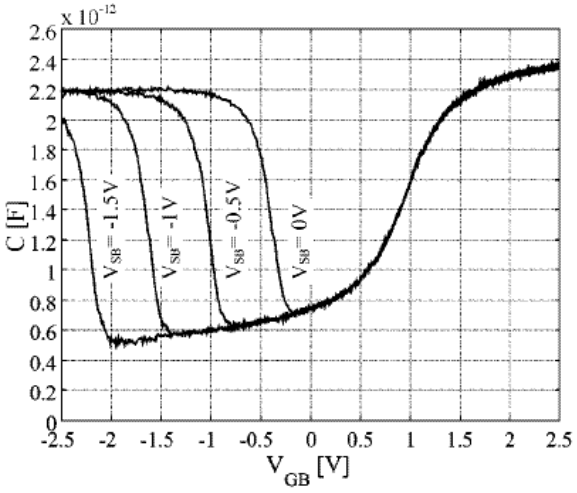


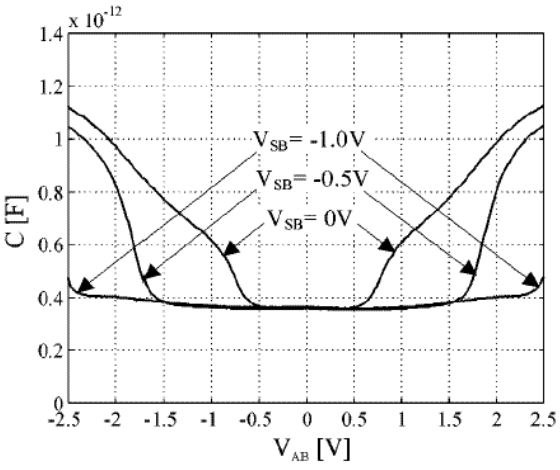
Fig. 040-02



[†] T. Tille, J. Sauerbrey and D. Schmitt-Landsiedel, "A 1.8V MOSFET-Only ΣΔ Modulator Using Substrate Biased Depletion-Mode MOS Capacitors in Series Compensation," *IEEE J. of Solid-State Circuits*, Vol. 36, No. 7, July 2001, pp. 1041-1047.

Compensated MOS-Capacitors in Depletion – Continued

Measured CV plot of a series compensated MOS capacitor with different substrate biases (0.25μm CMOS, t_{ox} = 5nm, W_1=W_2=20μm and L_1=L_2=20μm):



Example of a realization of the series compensation without using floating batteries.

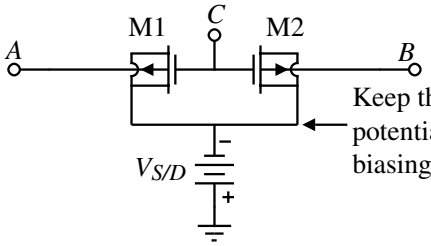
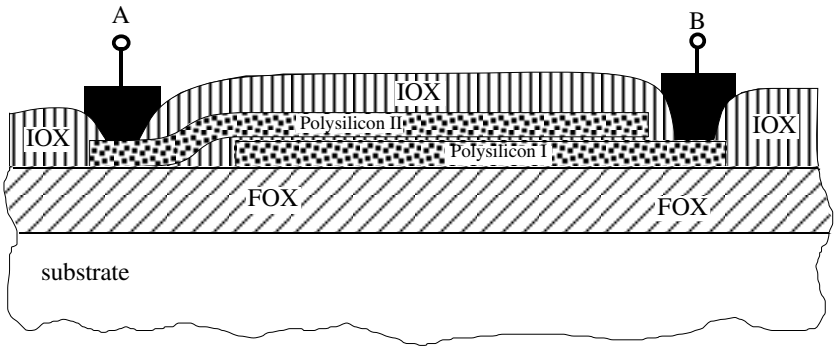


Fig. 040-03

MOS Capacitors - Continued

Polysilicon-Oxide-Polysilicon (Poly-Poly):

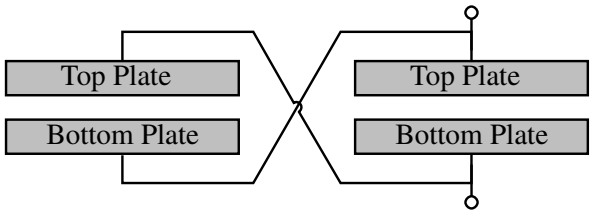


Best possible capacitor for analog circuits

Less parasitics

Voltage independent

Possible approach for increasing the voltage linearity:



Implementation of Capacitors using Available Interconnect Layers

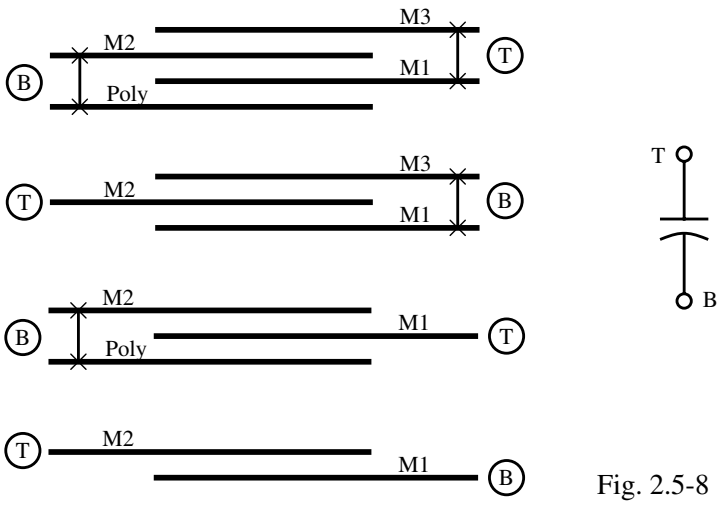
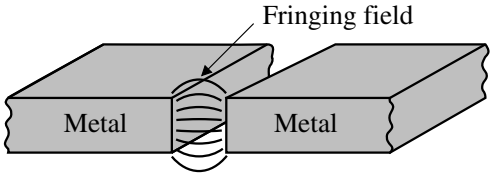


Fig. 2.5-8

Much more information on using metal for capacitance is found in the reference: R. Aparicio and A. Hamimiri, "Capacity Limits and Matching Properties of Integrated Capacitors," *IEEE J. of Solid-State Circuits*, Vol. 37, No. 3, March 2002, pp. 384-393.

Horizontal Metal Capacitors

Capacitance between conductors on the same level and use lateral flux.



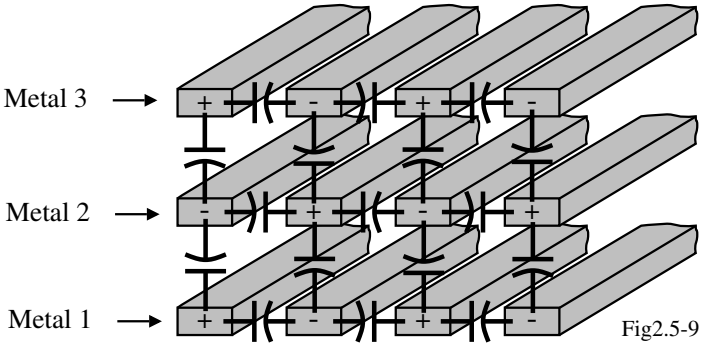
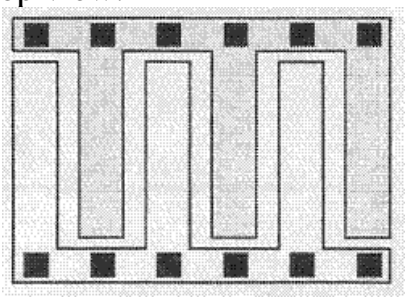
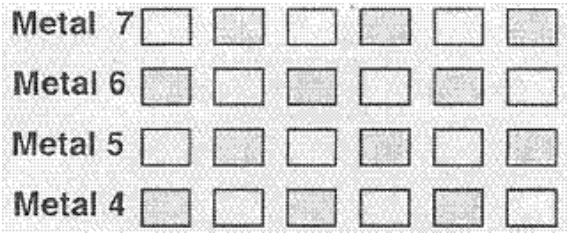


Fig2.5-9

Top view:



Side view:



These capacitors are sometimes called fractal capacitors because the fractal patterns are structures that enclose a finite area with an infinite perimeter.

The capacitor/area can be increased by a factor of 10 over vertical flux capacitors.

MOS Passive RC Component Performance Summary

Component Type	Range of Values	Absolute Accuracy	Relative Accuracy	Temperature Coefficient	Voltage Coefficient
Poly-oxide-semi-conductor Capacitor	0.35-0.5 fF/μm²	10%	0.1%	20ppm/°C	±20ppm/V
Poly-Poly Capacitor	0.3-0.4 fF/μm²	20%	0.1%	25ppm/°C	±50ppm/V
Diffused Resistor	10-100 Ω/sq.	35%	2%	1500ppm/°C	200ppm/V
Ion Implanted Resistor	0.5-2 kΩ/sq.	15%	2%	400ppm/°C	800ppm/V
Poly Resistor	30-200 Ω/sq.	30%	2%	1500ppm/°C	100ppm/V
n-well Resistor	1-10 kΩ/sq.	40%	5%	8000ppm/°C	10kppm/V

INDUCTORS COMPATIBLE WITH CMOS TECHNOLOGY

Inductors

What is the range of values for on-chip inductors?

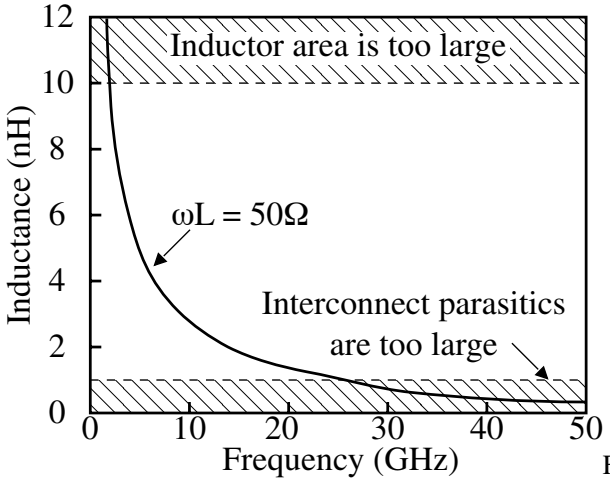


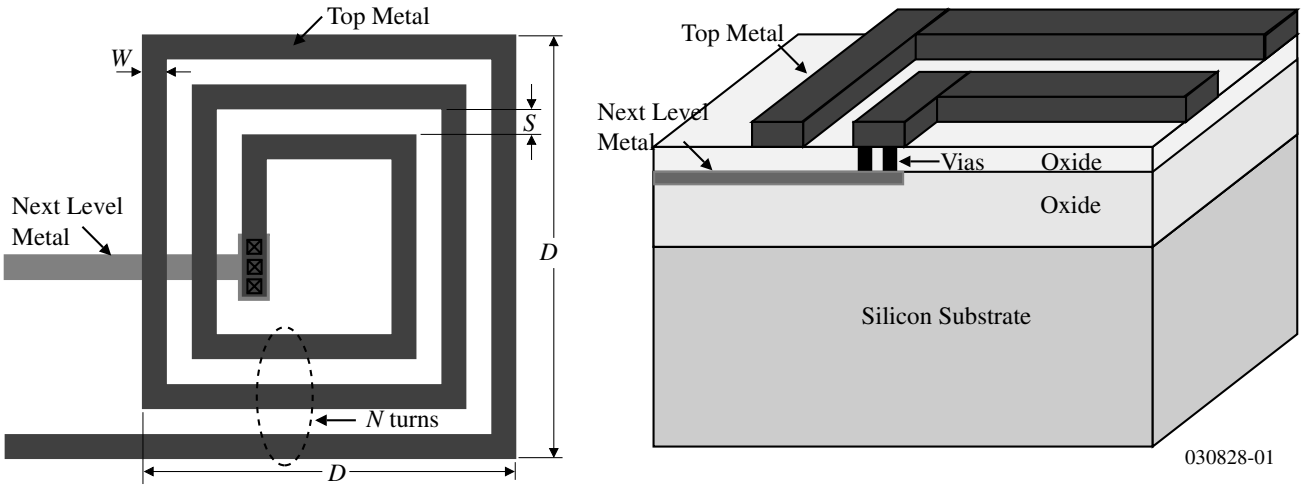
Fig. 6-5

Consider an inductor used to resonate with 5pF at 1000MHz.

$$L = \frac{1}{4\pi^2 f_o^2 C} = \frac{1}{(2\pi \cdot 10^9)^2 \cdot 5\text{x}10^{-12}} = 5\text{nH}$$

Note: Off-chip connections will result in inductance as well.

Spiral Inductors on a Lossy Substrate:



- Spiral inductor is implemented using metal layers in CMOS technology
- Topmost metal is preferred because of its lower resistivity
- More than one metal layer can be connected together to reduce resistance or area
- The accurate analysis of a spiral inductor requires complex electromagnetic simulation methods
- Optimize the values of *W*, *S*, and *N* to get the desired *L*, a high *Q*, and a high self-resonant frequency

Inductor Design

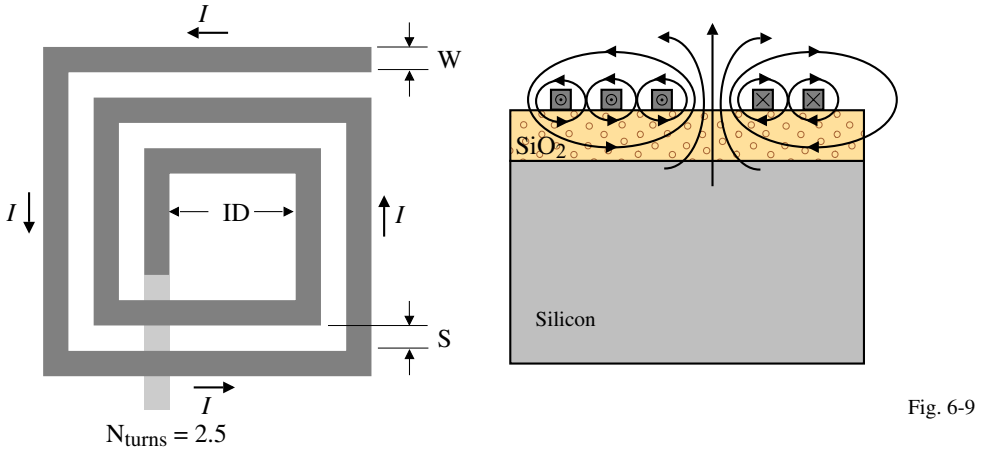


Fig. 6-9

Typically: $3 < N_{turns} < 5$ and $S = S_{min}$ for the given current

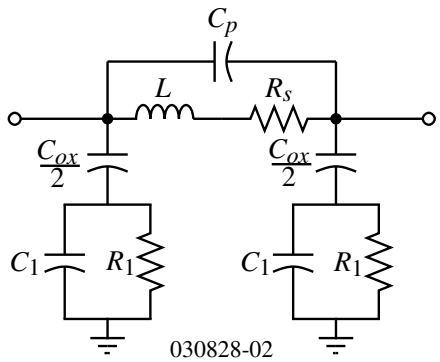
Select the OD, N_{turns}, and W so that ID allows sufficient magnetic flux to flow through the center.

Loss Mechanisms:

- Skin effect
- Capacitive substrate losses
- Eddy currents in the silicon

Inductor Modeling

Model:



$$L \approx \frac{37.5\mu_0 N^2 a^2}{11D\text{-}14a} \qquad C_{ox} = W \cdot L \cdot \frac{\varepsilon_{ox}}{t_{ox}}$$

$$R_s \approx \frac{L}{W\sigma\delta(1\text{-}e^{-t/\delta})} \qquad R_1 \approx \frac{WLC_{sub}}{2}$$

$$C_p = NW^2L \cdot \frac{\varepsilon_{ox}}{t_{ox}} \qquad C_1 \approx \frac{2}{WLC_{sub}}$$

where

$\mu_0 = 4\pi x10^{-7}$ H/m (vacuum permeability)

σ = conductivity of the metal

a = distance from the center of the inductor to the middle of the windings

L = total length of the spiral

t = thickness of the metal

δ = skin depth given by $\delta = \sqrt{2/W\mu_0\sigma}$

$G_{sub}(C_{sub})$ is a process-dependent parameter

Inductor Modeling – Continued

Definition of the previous components:

R_s is the low frequency resistive loss of a metal and the skin effect

C_p arises from the overlap of the cross-under with the rest of the spiral. The lateral capacitance from turn-to-turn is also included.

C_{ox} is the capacitance between the spiral and the substrate

R_1 is the substrate loss due to eddy currents

C_1 is capacitance of the substrate

Design specifications:

L = desired inductance value

Q = quality factor

f_{SR} = self-resonant frequency. The resonant frequency of the LC tank represents the upper useful frequency linmt of the inductor. Inductor operation frequency should be lower than f_{SR}, $f < f_{SR}$.

ASITIC:

A software tool for analysis and simulation of spiral inductors and transformers for CMOS.

http://formosa.eecs.berkeley.edu/~niknejad/asitic.html

Guidelines for Designing CMOS Sprial Inductors[†]

D – Outer diameter:

- As D increases, Q increases but the self-resonant frequency decreases
- A good design generally has $D < 200\mu m$

W – Metal width:

- Metal width should be as wide as possible
- As W increases, Q increases and R_s decreases
- However, as W becomes large, the skin effects become more significant, increasing R_s
- A good value of W is $10\mu m < W < 20\mu m$

S – Spacing between turns:

- The spacing should be as small as possible
- As S and L increase, the mutual inductance, M, decreases
- Use minimum metal spacing allowed in the technology but make sure the inter-winding capacitance between turns is not significant

N – Number of turns:

- Use a value that gives a layout convenient to work with other parts of the circuit

[†] Jaime Aguilera, et. al., "A Guide for On-Chip Inductor Design in a Conventional CMOS Process for RF Applications," *Applied Microwave & Wireless*, pp. 56-65, Oct. 2001.

Design Example

A 2GHz LC tank is to be designed as a part of LC oscillator. The C value is given as 3pF.

(a) Find value of L. (b) Design a spiral inductor with L value (± 5% range) from (a) using ASITIC. Optimize design parameters, W, S, D and N to get a high Q ($Q_{min} = 5$). Show L, Q, f_{SR} value obtained from simulation. (c) Show the layout. (d) Give a lumped circuit model.

Solution

(a) LC tank oscillation frequency is given as 2GHz.

$$\omega_{osc} = \frac{1}{\sqrt{LC}}, \quad L = \frac{1}{\omega_{osc}^{\ 2} \cdot C} = \frac{1}{(2\pi \cdot 2\times 10^{9})^{2} \cdot (3\times 10^{-12})} = 2.11\times 10^{-9}$$

$\therefore$ $L = 2.11$nH is desired.

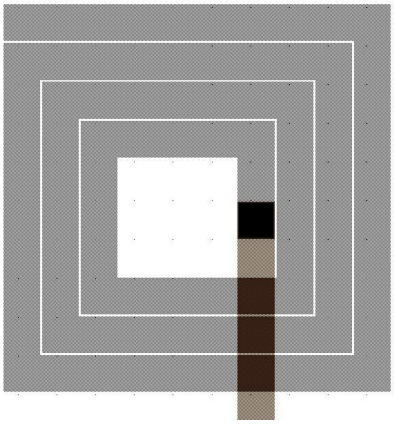
(b) $L = 2.11$nH(± 5%) is used as input parameter. Several design parameters are tried to get high Q and f_{SR} values. Final design has

- Parameters: $W = 19$um, $S = 1$um, $D = 200$um, $N = 3.5$
- Resulting inductor: $L = 2.06$nH, $Q = 7.11$, $f_{SR} = 9.99$GHz @ 2GHz

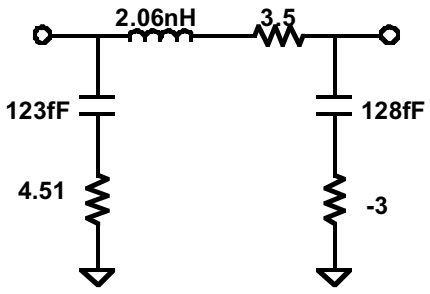
This design is acceptable as $Q > Q_{min}$ and $f < f_{SR}$.

Design Example-Continued

(c.) ASITIC generates a layout automatically. It can be saved and imported to use in other tools such as Cadence, ADS and Sonnet.



(d) Analysis in ASITIC gives the following π model.



The π model is usually not symmetrical and this can be used for differential configuration where none of the two ports is ac-grounded.

Reduction of Capacitance to Ground

Comments concerning implementation:

1.) Put a metal ground shield between the inductor and the silicon to reduce the capacitance.
   - Should be patterned so flux goes through but electric field is grounded
   - Metal strips should be orthogonal to the spiral to avoid induced loop current
   - The resistance of the shield should be low to terminate the electric field

2.) Avoid contact resistance wherever possible to keep the series resistance low.

3.) Use the metal with the lowest resistance and farthest away from the substrate.

4.) Parallel metal strips if other metal levels are available to reduce the resistance.

Example →

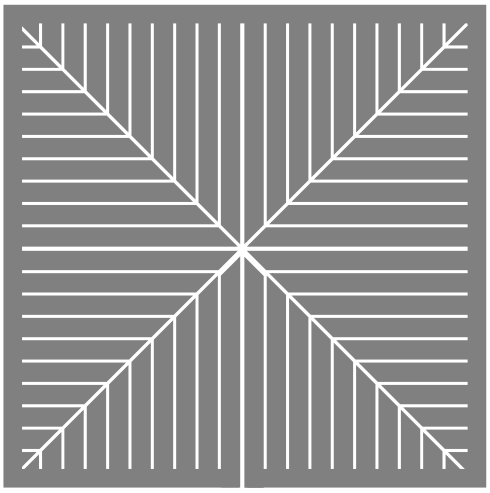
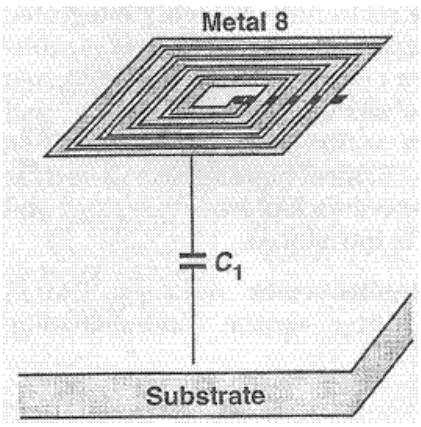


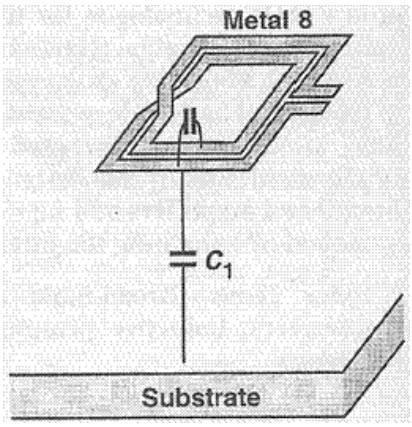
Fig. 2.5-12

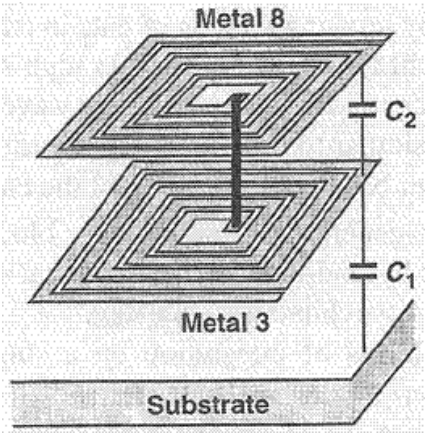
Multi-Level Spiral Inductors

Use of more than one level of metal to make the inductor.

- Can get more inductance per area
- Can increase the interwire capacitance so the different levels are often offset to get minimum overlap.
- Multi-level spiral inductors suffer from contact resistance (must have many parallel contacts to reduce the contact resistance).
- Metal especially designed for inductors is top level approximately 4μm thick.





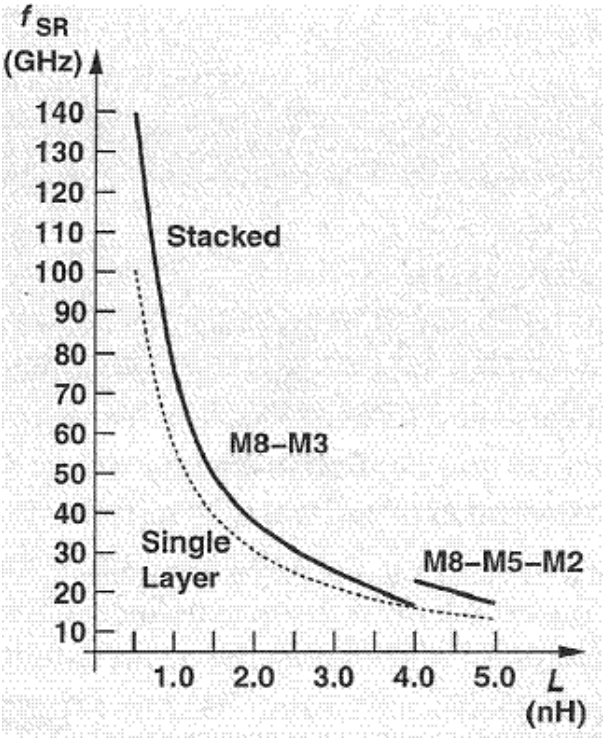


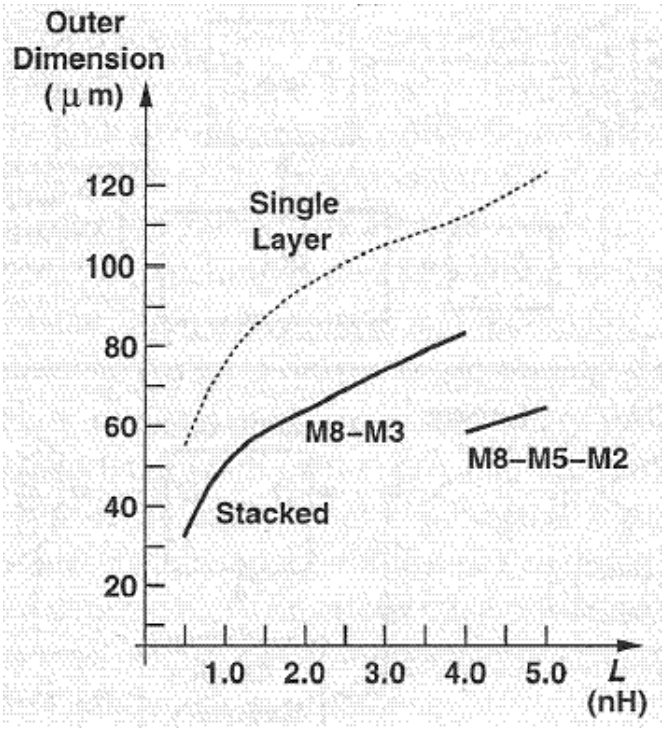
Q = 5-6, f_{SR} = 30-40GHz. Q = 10-11, f_{SR} = 15-30GHz[1]. Good for high L in small area.

[1] The skin effect and substrate loss appear to be the limiting factor at higher frequencies of self-resonance.

Inductors - Continued

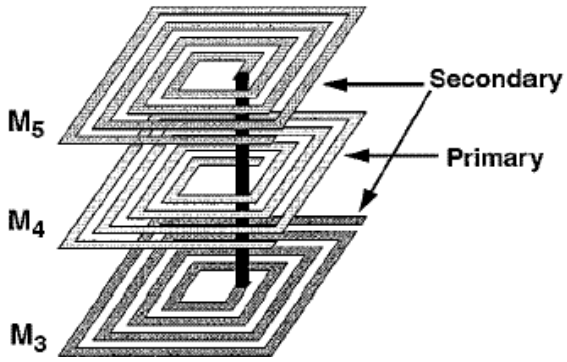
Self-resonance as a function of inductance. Outer dimension of inductors.



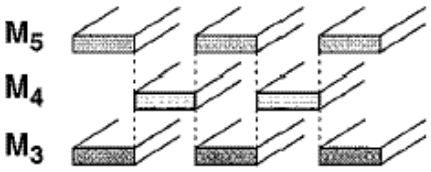


Transformers

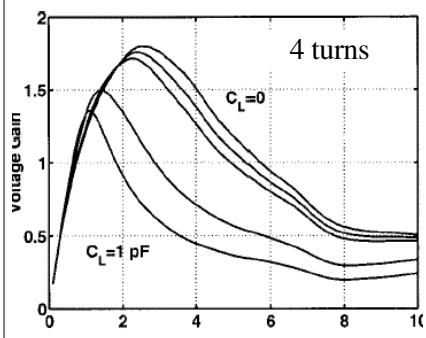
Transformer structures are easily obtained using stacked inductors as shown below for a 1:2 transformer.

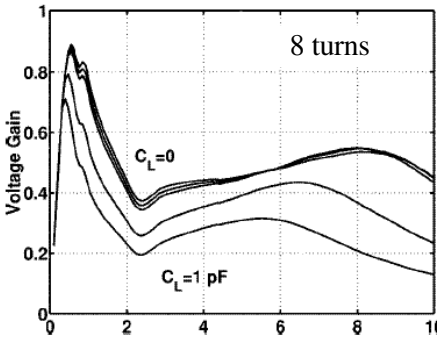


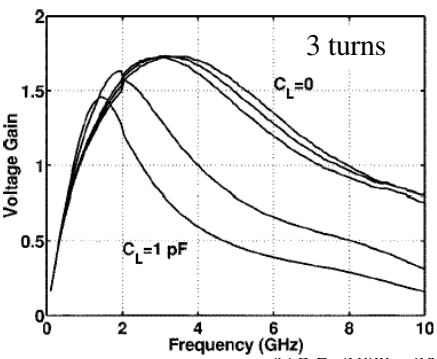
Method of reducing the interwinding capacitances.



Measured 1:2 transformer voltage gains:



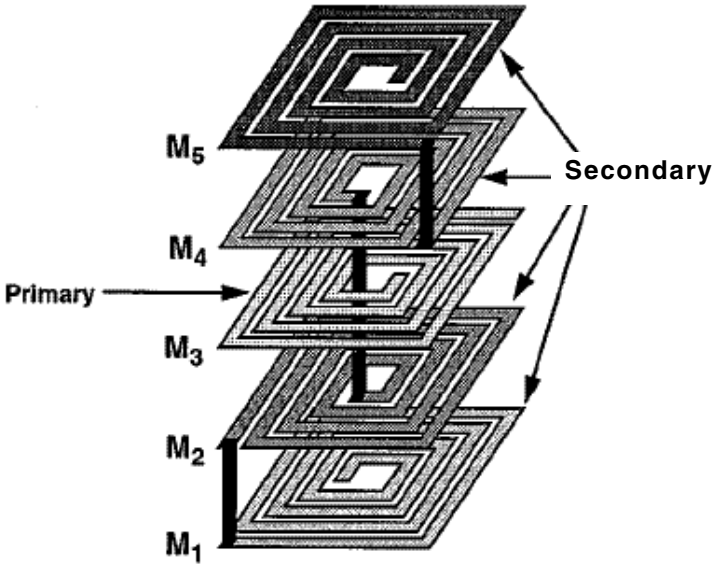




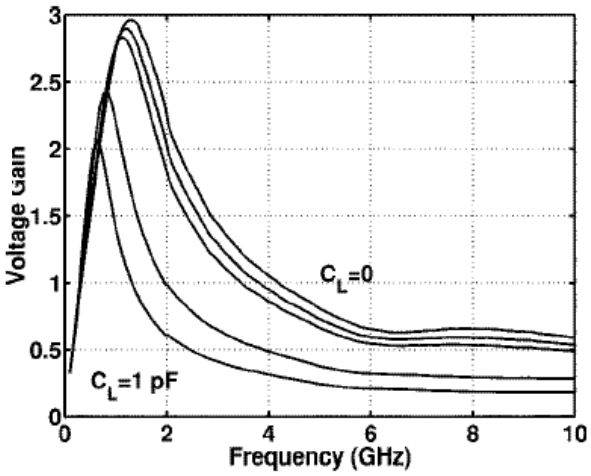
Transformers – Continued

A 1:4 transformer:

Structure-



Measured voltage gain-



(C_L = 0, 50fF, 100fF, 500fF and 1pF. C_L is the capacitive loading on the secondary.)

SUMMARY

- This section has presented and characterized CMOS technology and the passive components suitable for implementation on silicon integrated circuit technologies.
- Resistors
  - Source/drain diffusions, base/emitter diffusions, polysilicon and n-well/collector
- Capacitors
  - pn-junction, MOS capacitors (depletion and accumulation), poly-poly, metal-metal
- Varactors – varied using a voltage and vary from 10% to as much as 100% or more
- Inductors
  - Limited to nanohenrys
  - Very low Q (3-5)
  - Not variable
- Transformers
  - Reasonably easy to build and work using stacked inductors
- Did not cover several important aspects of IC components
  - Errors
  - Matching
  - Physical aspects (layout)