LECTURE 140 –ALL DIGITAL FREQUENCY SYNTHESIZER

Objective

1.) Demonstrate the application of an ADPLL to a frequency synthesizer suitable for 802.15.4 (Bluetooth/ZigBee)

2.) Illustrate the application of 0.18μm CMOS to a PLL application

What is Bluetooth/ZigBee?

- A short-range technology for integration into mobile and handheld devices that is target to replace cable connections.
- Specifications:
  - Frequency range: 2400-2483.5 MHz
  - Spectrum spreading: FHSS (Frequency hopping spectrum spreading)
    - $f_k = 2.402 + k$ MHz, $k = 0, 1, \ldots, 78$ (dwell time = 0.625ms)
    - Channel bandwidth: 1 MHz
  - Modulation: GFSK (BT = 0.5; $0.28 < h < 0.35$)
  - Receiver sensitivity: -70 dBm @ 0.1% BER
  - Coverage area: Up to 10 m
  - Transmit power: 0dBm (up to 20dBm with power control)

Frequency Synthesizer Specification for 802.15.4 Application

- Frequency range: 2.402 – 2.480 GHz
- Settling time ≤ 220 μsecs
- Phase noise:
  - ≤ -89 dBc/Hz at 0.5 MHz offset
  - ≤ -121 dBc/Hz at 2 MHz offset
- Channel bandwidth: 1 MHz, error tolerance: ±20 ppm (96 kHz)

Architecture Selection

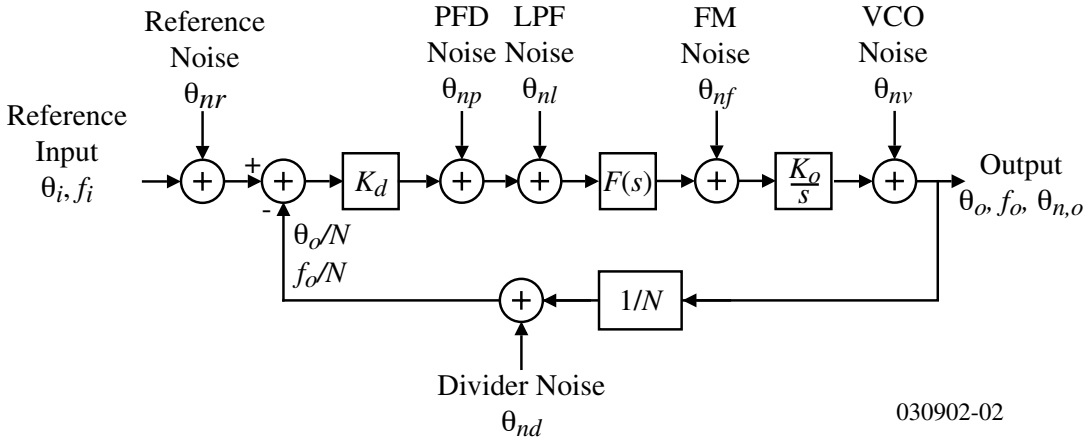
- Direct digital frequency synthesizer – limited in speed by Nyquist sampling requirements
- Integer-N frequency synthesizer – (channel spacing = reference frequency)
  - Small channel spacing ⇒ Large division ratio ⇒ Large in-band phase noise
  - Small channel spacing ⇒ Small loop bandwidth ⇒ Increased switching time
- Fractional-N frequency synthesizer (channel spacing << reference frequency)
  - Lower in-band noise
  - Faster locking time
  - Fractional spurs are eliminated by modulating the division ratio using a high-order delta-sigma modulator

System Level Design using Linear Models

• When the PLL is in locked state, the linear model can be used for analysis

• If the reference frequency >> loop bandwidth, then we can use the continuous model

Therefore,



$$B(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{G(s)}{1 + G(s)H(s)}$$

where

$$G(s) = \frac{K_d K_o F(s)}{s} \qquad \text{and} \qquad H(s) = \frac{1}{N}$$

System Level Analysis – Continued

• Output noise power, θ_{no}:

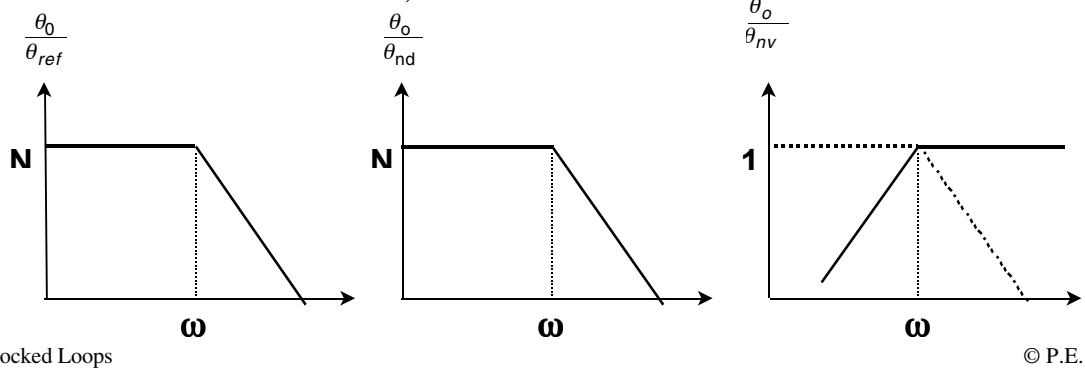
$$\theta_{no}^2 = N^2(\theta_{nr}^2 + \theta_{n,eq}^2)\left(\frac{O(s)}{1 + O(s)}\right)^2 + \theta_{nv}^2\left(\frac{1}{1 + O(s)}\right)^2$$

where

$$\theta_{n,eq}^2 = \frac{1}{K_d^2}(\theta_{np}^2 + \theta_{nl}^2) = \frac{1}{K_d^2 F(s)^2}\theta_{nf}^2 + \theta_{nd}^2 \quad \text{and} \quad O(s) = \frac{K_d K_o F(s)}{Ns} = \frac{K_v F(s)}{Ns}$$

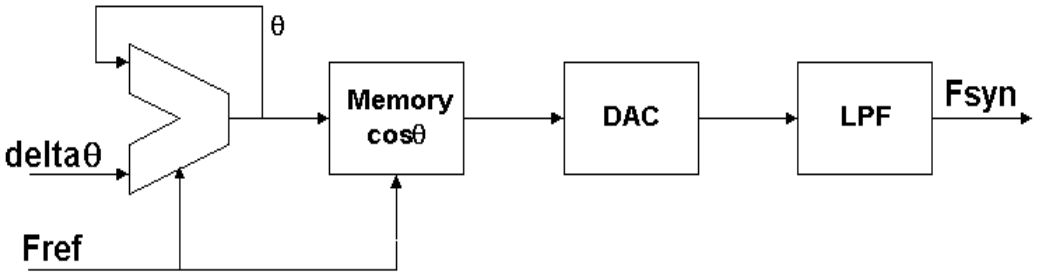
Note that, $\dfrac{O(s)}{1 + O(s)} = \dfrac{\frac{K_d K_o F(s)}{N}}{s + \frac{K_d K_o F(s)}{N}}$ and $\dfrac{1}{1 + O(s)} = \dfrac{s}{s + \frac{K_d K_o F(s)}{N}}$

• Reference noise and the VCO inherent noise are the two major sources of phase noise in a PLL. This is illustrated below as,



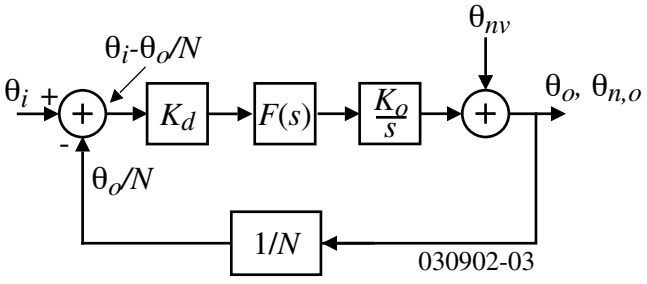
Direct Digital Frequency Synthesizer

- Direct digital frequency synthesizer (DDFS)
  - Advantage: High frequency resolution, fast switching time
  - Disadvantage: High power consumption, limitation of the highest frequency by the Nyquist sampling theorem, discrete narrow band spurious signals
- The DDFS methods are combined with PLLs to achieve fine frequency steps with reasonable phase noise.



PLL Based Frequency Synthesizer

- PLL is a negative feedback system whose output frequency is locked onto an input signal.
  - Phase detector is the error amplifier
  - Lowpass filter supresses the high frequency components of the phase detector
  - VCO
- Low cost and good spurious suppression
- Coarse frequency resolution or frequency steps and poor phase noise
- Slow switching speed for negative feedback loop
- Closed-loop transfer function:

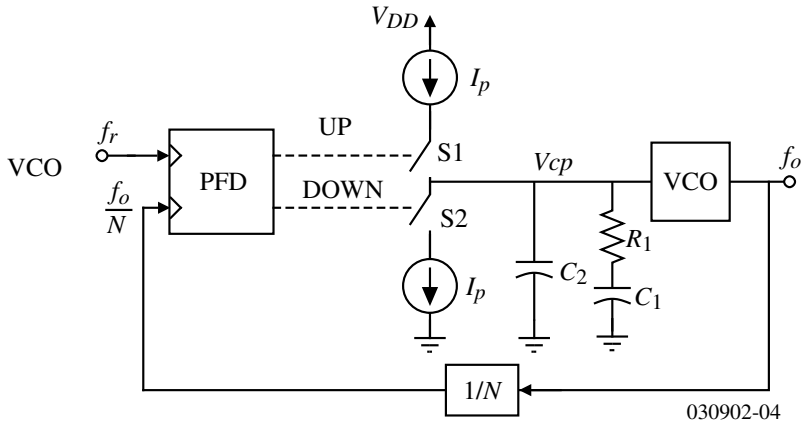


$$B(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{G(s)}{1 + G(s)H(s)} = \frac{\frac{K_d K_o F(s)}{s}}{1 + \frac{K_d K_o F(s)}{Ns}} = \frac{N\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}$$

Charge Pump Frequency Synthesizer

• Charge pump phase locked loop (Type II, 3rd order PLL)

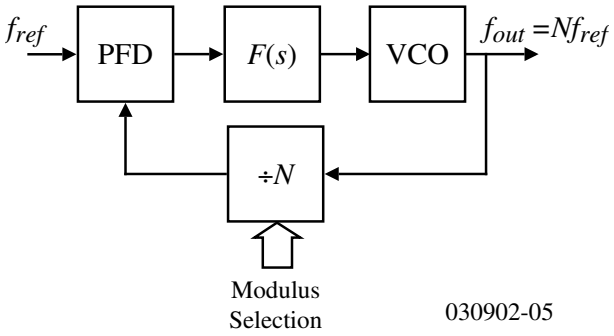
- Advantage: Low phase noise
- Disadvantages: Process depedent, slow locking speed, large passive external elements (*R*s and *C*s)



Integer-N Frequency Synthesizer

• Integer-N frequency synthesizer:

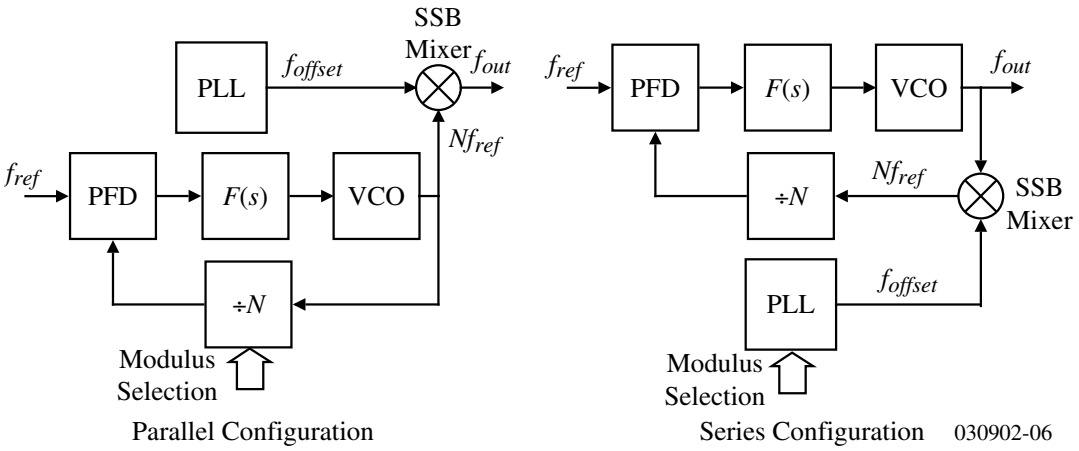
- $f_o = Nf_{ref}$, N = integer number
- Inverse relationship between step size and phase noise
- To achieve small channel spacing, a low f_{ref} is required which means a narrow loop bandwidth resulting in increased settling time and reduced VCO noise supression
- Low f_{ref} means a large integer N, resulting in increased in-band phase noise



Dual Loop Frequency Synthesizer

• Dual loop frequency synthesizer:

- Mixer is incorporated into the PLL altering the relationship between the channel spacing and the reference frequency of the integer *N* synthesizer
- 2 dual loop types: A combination of 2 PLLs by a single sideband mixer in parallel and in series
- Adds a fixed high offset frequency and a low variable frequency



Dual Loop Frequency Synthesizers - Continued

• Architectural comments:

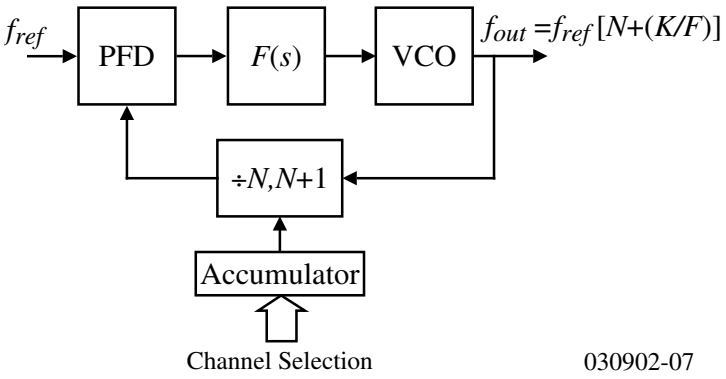
- Parallel configuration: A fixed frequency + varying frequency. Gives large spurs at the output
- Series configuration: Varying frequency is added inside the loop resulting in a larger settling time and a small sideband from the mixer
- The loop bandwidth of the high frequency loop can be large which gives more reduction of phase noise close to the carrier
- The frequency division of the divider can be reduced with the fixed offset frequency
- Sidebands are produced from the non-ideal SSB mixing and larger power consumption is required

Fractional-N Frequency Synthesizer

- Fractional-N frequency synthesizer:
  - Doesn't require more current, complexity or bigger area
  - $f_{ref} >> f_{step}$
  - $f_o = f_{ref}\left(N + \frac{K}{F}\right)$

  $N_{fractional}$: (Divide by N+1 every K VCO cycles out of F cycles and by N for the remaining cycles)

$$\therefore \quad N_{fractional} = (N+1)\frac{K}{F} + N\left(1 - \frac{K}{F}\right) = N + \frac{K}{F}, \text{ where } K \geq K \geq 0$$

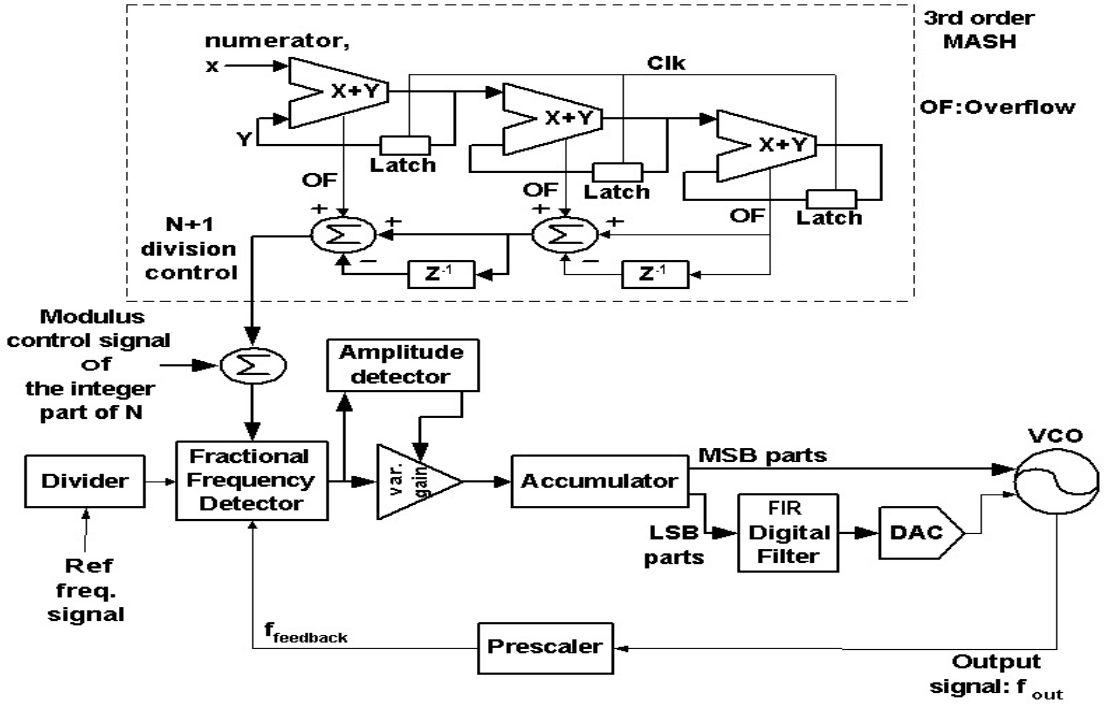


All-Digital Frequency Synthesizer

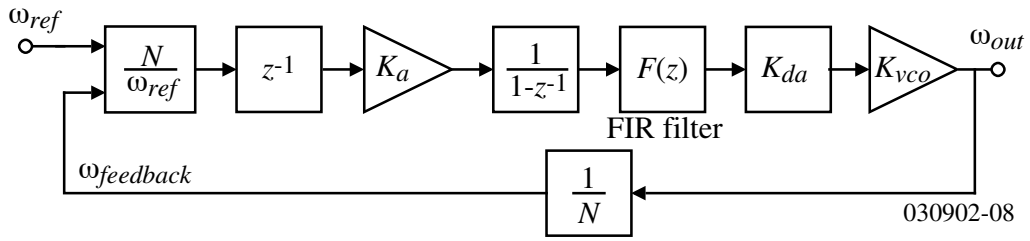
- Apply digital filter to achieve a single-chip frequency synthesizer
  - Fully integrated frequency synthesizer
  - Easy to implement for a multi-mode application (i.e. W-CDMA/GPRS/GSM)
  - Increase design robustness
- Apply MASH delta-sigma modulator
  - Reduced spurs
  - Fast locking time
- Use a switched-current oscillator
  - Wide locking range
  - Fast locking time

All Digital Frequency Synthesizer – Continued

Block diagram:



Linear Model of the ADPLL Frequency Synthesizer

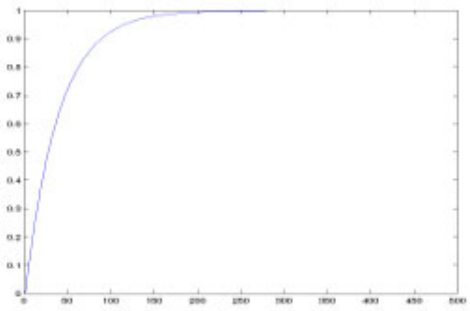


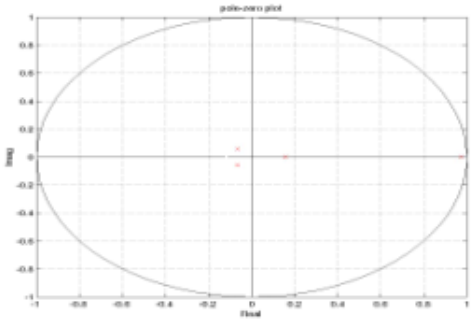
$$H(z) = \frac{\omega_{feedback}}{\omega_{ref}} = \frac{KF(z)z^{-1}}{1 - z^{-1}[1 - KF(z)]}$$

where

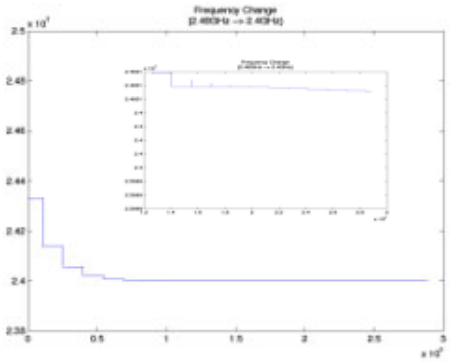
$$K = \frac{K_{da}K_{vco}K_a}{\omega_{ref}}$$

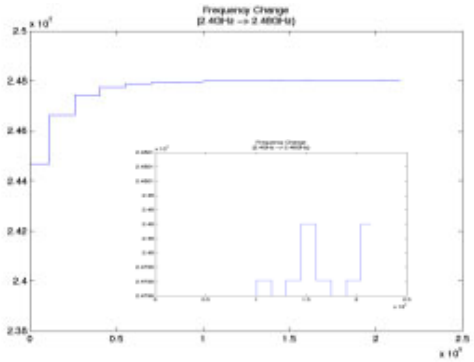
System Level Unit Step Response and Pole-Zero Plot



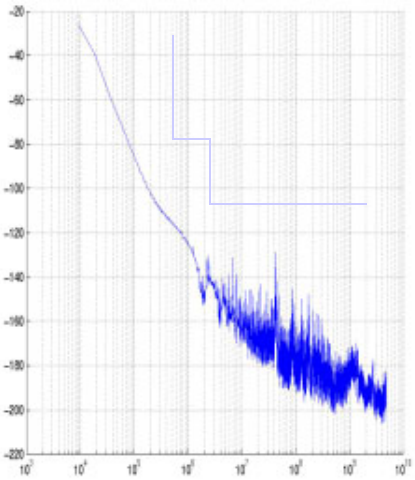


System Level Locking Time Simulation (Bluetooth)

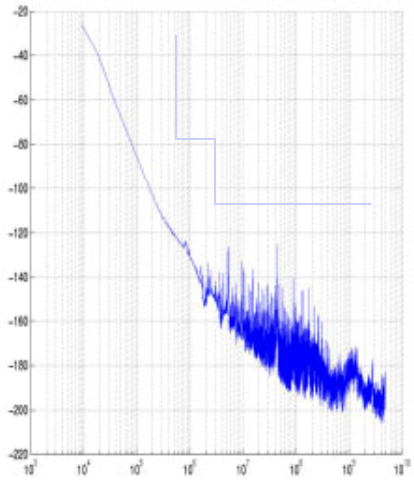




System Level Phase Noise Simulation (Bluetooth)



$$\text{Fractional} = \frac{\text{Numerator}}{\text{Denominator}} = \frac{32}{64}$$

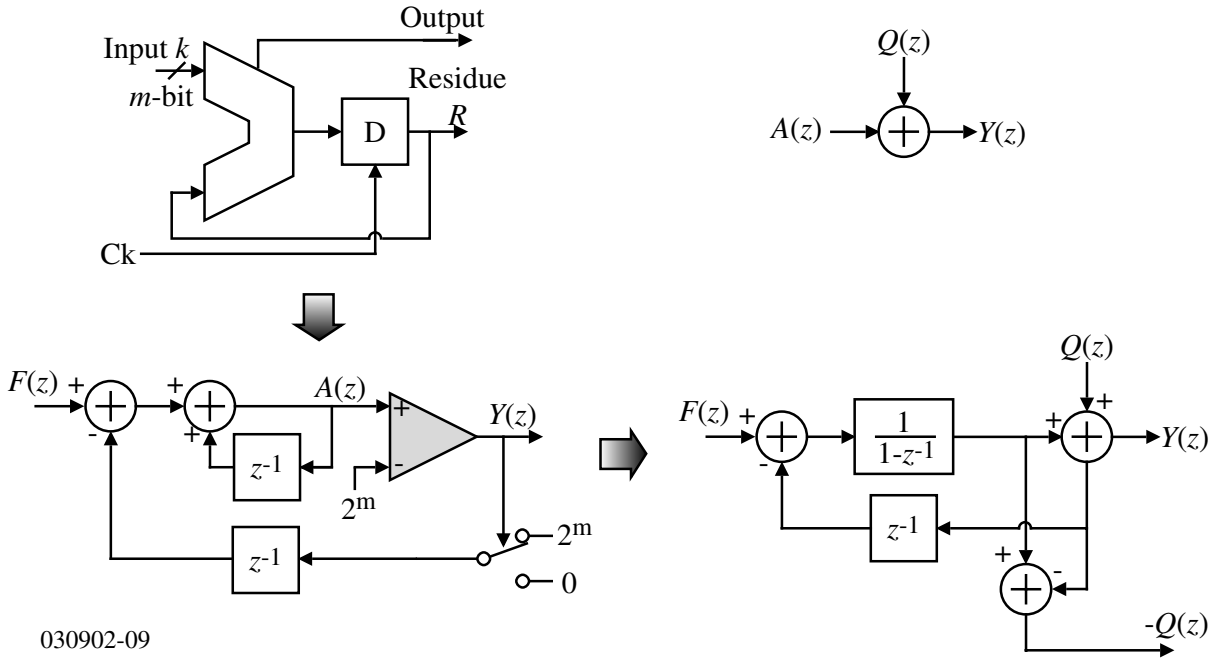


$$\text{Fractional} = \frac{\text{Numerator}}{\text{Denominator}} = \frac{0}{64}$$

Block Design – Third-Order ΔΣ Modulator

- Used to eliminate the fractional spurs by modulating the division ratio
- A third-order modulator is used to meet the higher spurs specification

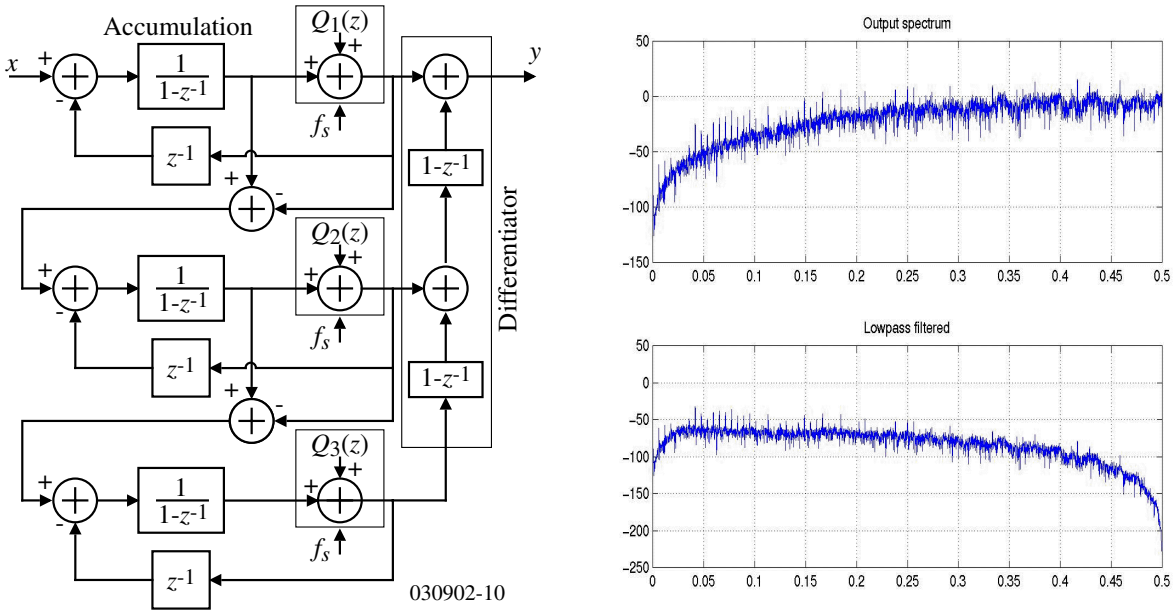
A first-order ΔΣ modulator:



Block Design – Third-Order ΔΣ Modulator – Continued

Third-order MASH block diagram and simulation:

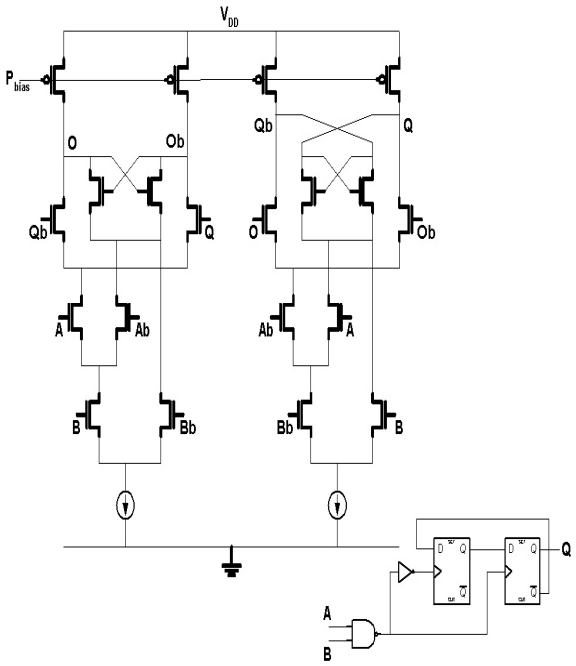
$$y(z) = x(z) + (1-z^{-1})^3 q_3(z) = x(z) + H_{noise}(z) q_3(z)$$



Block Design – Continued

Logic design:

- Conventional CMOS static logic
  - Wide noise margins
  - High packaging density
  - Zero static power dissipation
  - Coupling between the analog blocks and the digital blocks
  - Susceptible to power supply noise
- Current Mode Logic
  - Constant current source
  - Differential input and output



Block Design – Continued

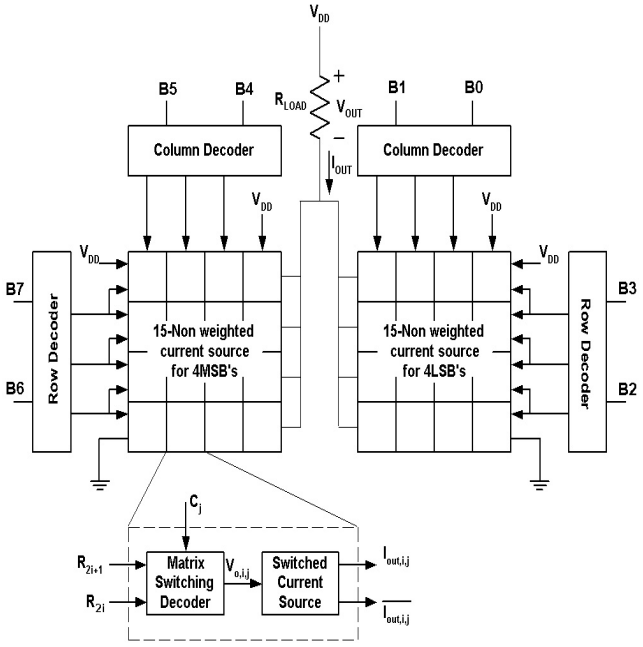
8-bit DAC:

- Symmetric 2-stage current cell matrix architecture
- A 4-bit MSB current cell matrix and a 4-bit LSB current cell matrix
- Uses thermometer code
- Monotonic conversion characteristic

$$I_{out} = I_{MSB}(2^3B_7 + 2^2B_6 + 2^1B_5 + 2^0B_4) + I_{LSB}(2^3B_3 + 2^2B_2 + 2^1B_1 + 2^0B_0)$$

$$I_{MSB} = 16\, I_{LSB}$$

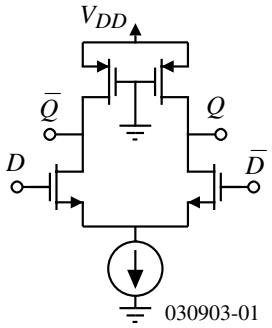
$$V_{out} = I_{out}\, R_{Load}$$



Block Design – Continued

Prescaler:

- Issues – high operating frequency, low power dissipation, low phase-noise
- Conventional Current Mode Logic (CML):



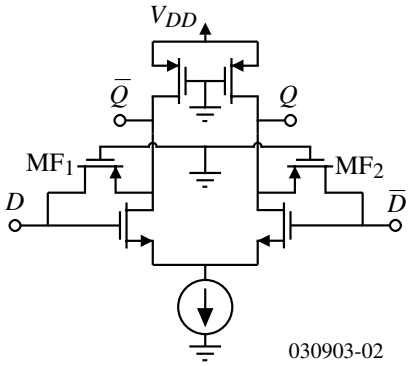
- Feedback CML (Transistors MF_1 and MF_2)

$$A(j\omega) = \frac{A_d(j\omega)}{1 + F_b A_d(j\omega)}$$

$$= \frac{A_d(0)}{1 + F_b A_d(0)} = \frac{1}{1 - j\left(\frac{\omega}{\omega_p}\right)\left(\frac{1}{1+F_b A_d(0)}\right)}$$

where

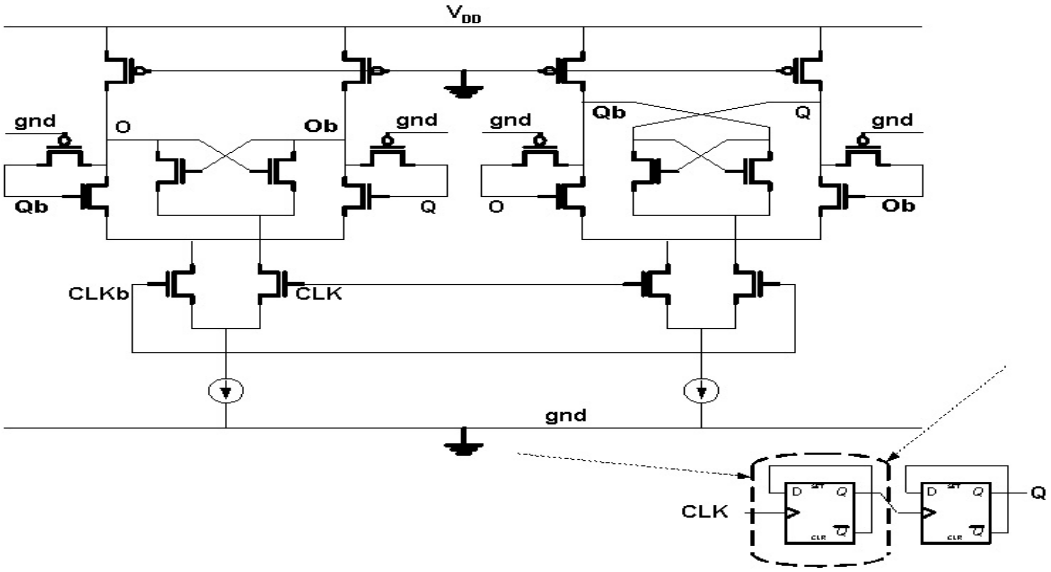
F_b = the gain of the feedback transistors



The bandwidth of the feedback CML >> the bandwidth of the conventional CML.

Block Design – Continued

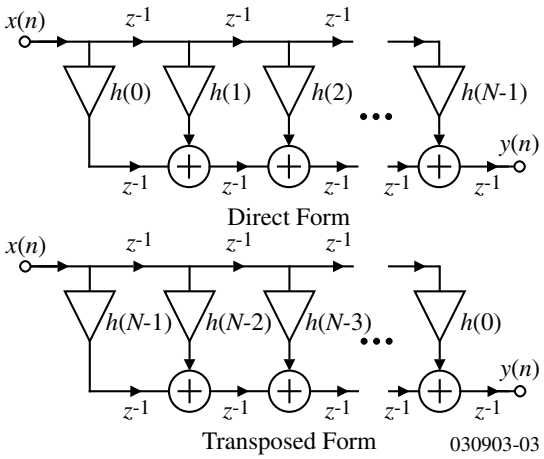
Feedback CML D Flip-flop implementation:



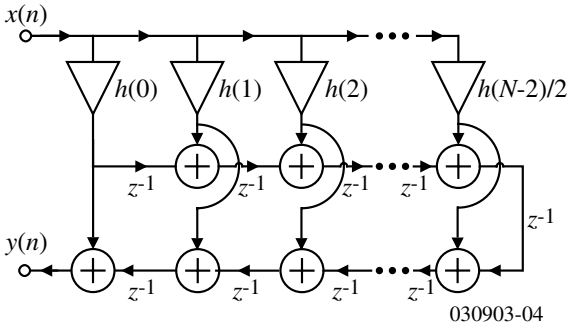
Block Design – Continued

FIR Digital Filter:

(a.) Single flow graph of *n*th order



(b.) Linear phase transpose direct form.



Experimental Results

(In progress)

