LECTURE 150 – CLOCK AND DATA RECOVERY CIRCUITS

INTRODUCTION

Objective

The objective of this presentation is:

1.) Understand the applications of PLLs in clock/data recovery

2.) Examine and characterize CDR circuits

Outline

- Introduction and basics of clock and data recovery circuits
- Clock recovery architectures and issues
- Phase and frequency detectors for random data
- CDR architectures
- Jitter in CDR circuits
- VCOs for CDR applications
- Examples of CDR circuits
- Summary

BASICS OF CLOCK AND DATA RECOVERY CIRCUITS

Why Clock and Data Recovery Circuits?

In many systems, data is transmitted or retrieved without any additional timing reference. For example, in optical communications, a stream of data flows over a single fiber with no accompanying clock, but the receiver is required to process this data synchronously. Therefore, the clock or timing information must be recovered from the data at the receiver.

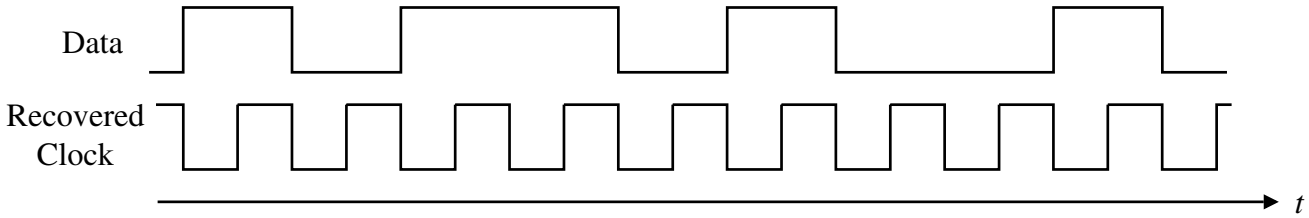


Fig. 4.2-01

Most all clock recovery circuits employ some form of a PLL.

Properties of NRZ Data

Most binary data is transmitted in a "nonreturn-to-zero" (NRZ) format. NRZ data is compared with "return-to-zero" (RZ) data below.

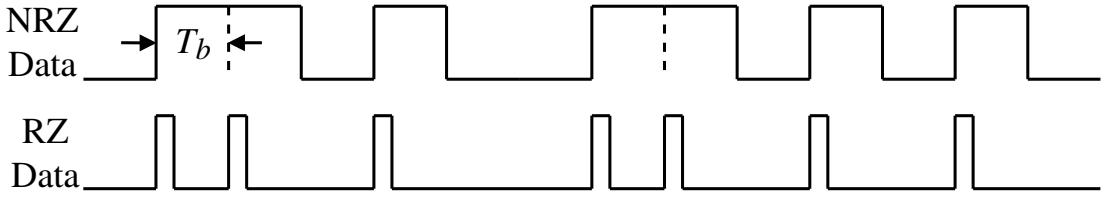


Fig. 4.2-02

The NRZ format has a duration of T_b for each bit period. The bit rate, $r_b = 1/T_b$ in bits/sec.

The bandwidth of RZ data > bandwidth of NRZ data

Maximum bandwidth of NRZ data is determined by a square wave of period $2T_b$.

In general, NRZ data is treated as a random waveform with certain known statistical properties.

The Challenge of Clock Recovery

1.) The data may exhibit long sequences of ONEs or ZEROs requiring the CRC to "remember" the bit rate during such an interval. The CRC must not only continue to produce the clock, but do so without drift or variation in the clock frequency.

2.) The spectrum of the NRZ data has nulls at frequencies which are integer multiples of the bit rate. For example, if r_b = 1Gb/s, the spectrum has no energy at 1GHz.

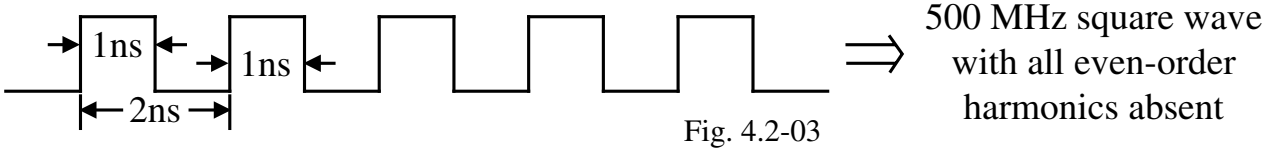


Fig. 4.2-03

NRZ Data Spectrum

The autocorrelation function of a random binary sequence can be written as[†]

$$R_x(\tau) = 1 - \frac{|\tau|}{T_b}, \quad |\tau| < T_b$$
$$= 0, \quad |\tau| = T_b$$

From this, the power spectral density of a random binary sequence is written as,

$$P_x(\omega) = T_b\left[\frac{\sin(\omega T_b/2)}{\omega T_b/2}\right]^2$$

which is illustrated as,

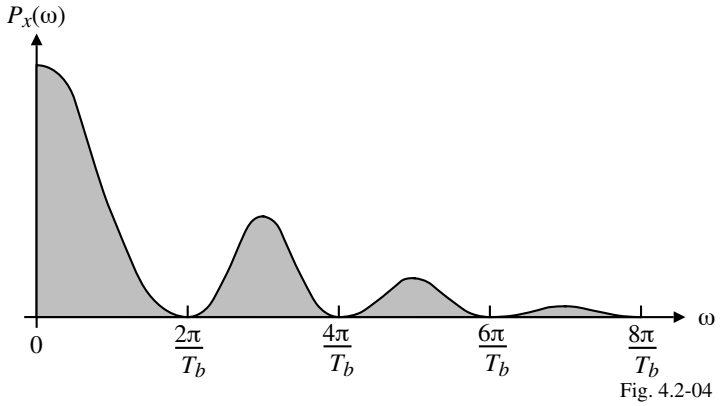


Fig. 4.2-04

[†] S.K.Shanmugam, *Digital and Analog Communication Systems*, New York: Wiley &Sons, 1979.

Edge Detection

CRC circuits require the ability to detect both the positive and negative transitions of the incoming data as illustrated below,

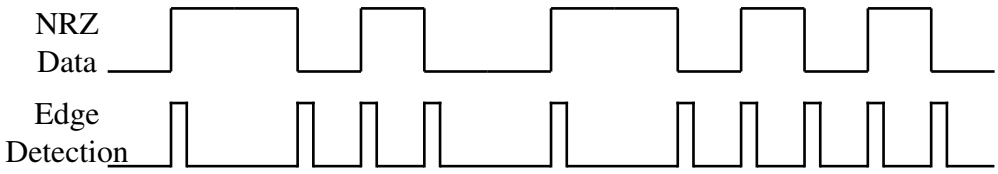


Fig. 4.2-05

Methods of edge detection:

1.) EXOR gate with a delay on one input.

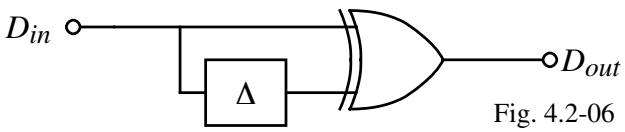


Fig. 4.2-06

2.) A differentiator followed by a full-wave rectifier.

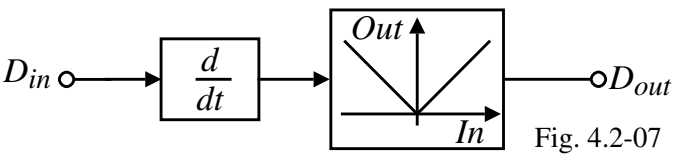


Fig. 4.2-07

Edge Detection and Sampling of NRZ Data - Continued

3.) Use a flipflop that operates on both the rising and falling edges.

This technique takes advantage of the fact that in a phase-locked CRC, the edge-detected data is multiplied by the output of a VCO as shown.

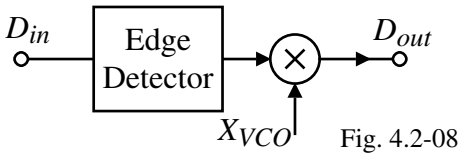


Fig. 4.2-08

In effect, the data transition impulses "sample" points on the VCO output.

a.) Master-slave flipflop consisting of two D latches.

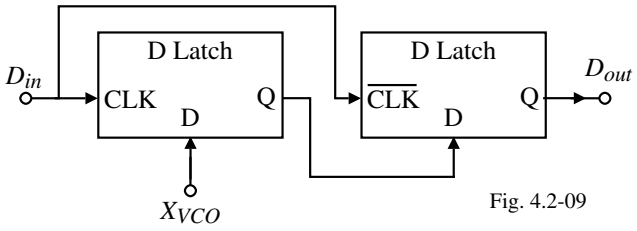


Fig. 4.2-09

b.) Double-edge-triggered flipflop.

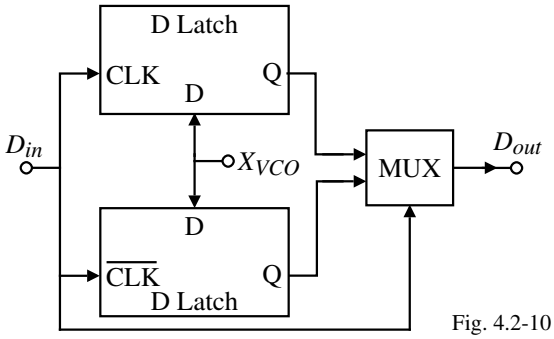


Fig. 4.2-10

CLOCK RECOVERY ARCHITECTURES AND ISSUES

Clock Recovery Architectures

From the previous considerations, we see that clock recovery consists of two basic functions:

1.) Edge detection

2.) Generation of a periodic output that settles to the input data rate but has negligible drift when some data transitions are absent.

Conceptual illustration of these functions:

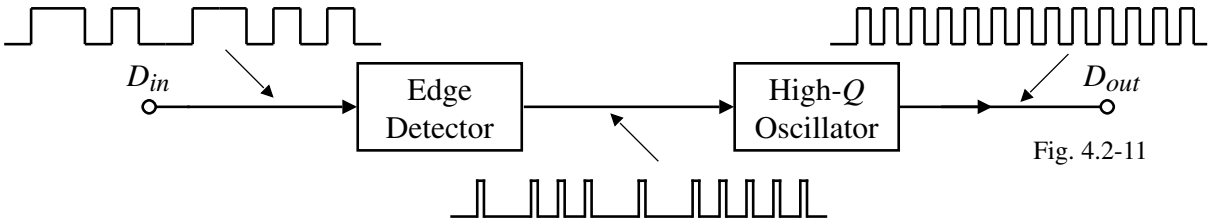


Fig. 4.2-11

In essence, the high-Q oscillator is "synchronized" with the input transitions and oscillates freely in their absence. Synchronization is achieved by means of phase locking.

Phase Locked Clock Recovery Circuit

Circuit:

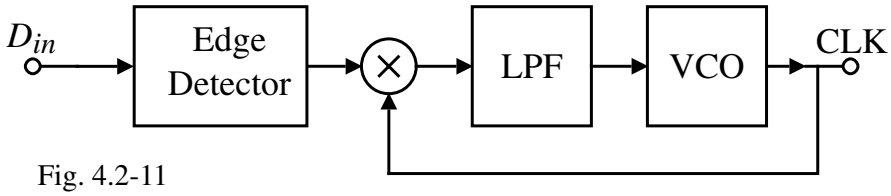


Fig. 4.2-11

Operation:

1.) Assume the input data is periodic with a frequency of $1/T_b$ (Hz).

2.) The edge detector doubles the frequency causing the PLL to lock to $2/T_b$ (Hz).

3.) If a number of transitions are absent, the output of the multiplier is zero and the control voltage applied to the VCO begins to decay causing the oscillator to drift from $1/T_b$ (Hz).

4.) To minimize the drift due to the lack of transitions,

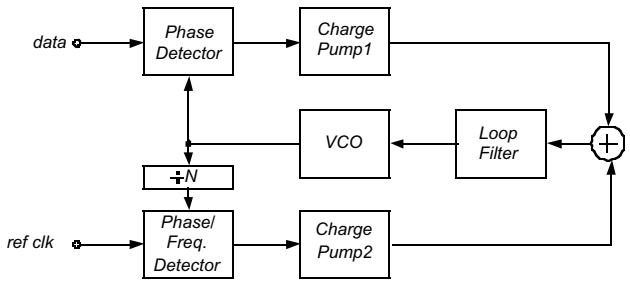
τ_{LPF} >> Maximum allowable interval between consecutive transitions.

5.) The result is a small loop bandwidth and a narrow capture range. Fortunately, most communication systems guarantee an upper bound of the allowable interval between consecutive transitions by encoding the data.

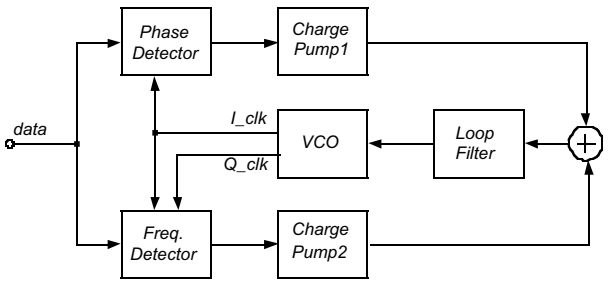
Frequency Aided Acquisition

Frequency acquisition can be accomplished with and without an external reference. If an external reference clock is available, frequency acquisition can be done with a secondary PLL loop having a PFD.

Frequency acquisition with a external reference:



Frequency acquisition with a frequency detector:

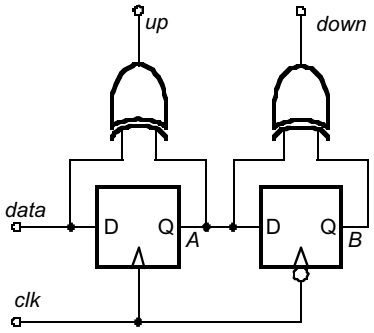


If no reference clock is available, a frequency detector has to be used which requires I and Q clocks and for typical implementations, the VCO frequency cannot be off more that about 25% of the data rate.

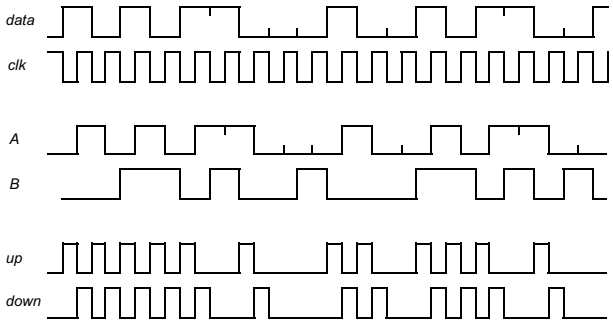
PHASE DETECTORS FOR RANDOM DATA

Linear Phase Detectors

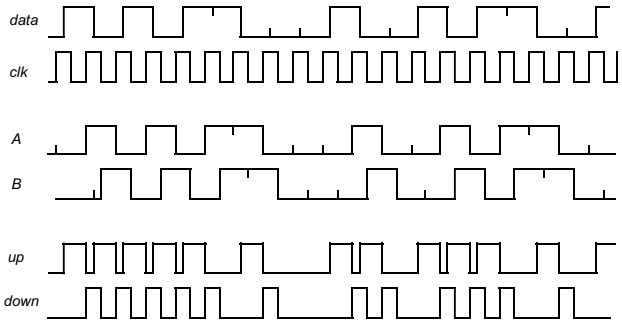
This type of detector is represented by the Hogge detector.[†]



Clock rising edge is at data center:



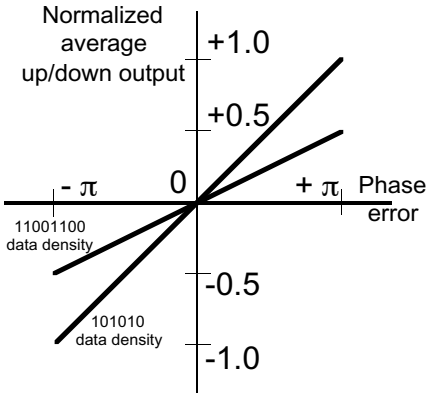
Clock is 0.5 period ahead of data center.



[†] C. R. Hogge, *IEEE J. Lightwave Technology*, pp. 1312-1314, 1985.

Linear Phase Detector – Continued

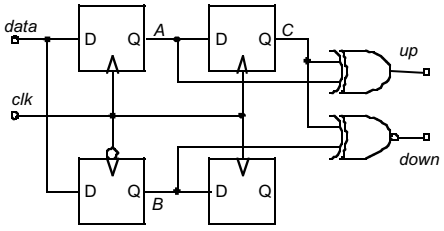
Transfer characteristics of the Hogge phase detector:

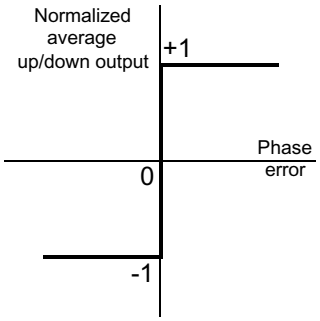


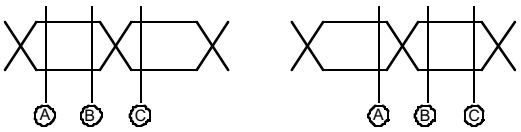
- Linear gain characteristics
- Phase detector gain is 0.5 for 11001100 data transition density
- Small jitter generation due to PD
- Suffers from bandwidth limitations
- Have static phase offset due to mismatch

Binary Phase Detectors

This type of phase detector is represented by the Alexander type of phase detector.†







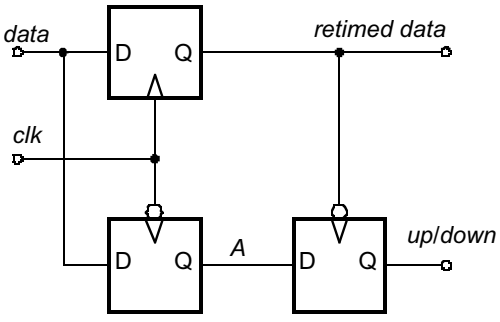
Binary Phase Detector Truth-Table		
ABC	Decision	Output
000	Tri-state	- - - - - - -
001	Clock is ahead	Down
010	Error	- - - - - - -
011	Clock is behind	Up
100	Clock is behind	Up
101	Error	- - - - - - -
110	Clock is ahead	Down
111	Tri-state	- - - - - - -

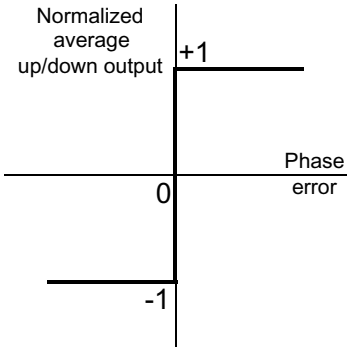
- High phase detector gain
- Causes higher output jitter compared to linear phase detectors
- Static phase offset set by sampling aperture errors
- Widely used in digital PLL and DLL's

† J.D.H. Alexander, *IEE Electronics Letters*, pp. 541-542, 1975.

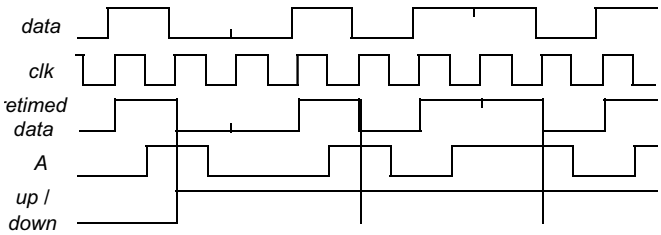
Binary Phase Detectors – Continued

Meghelli Phase Detector†

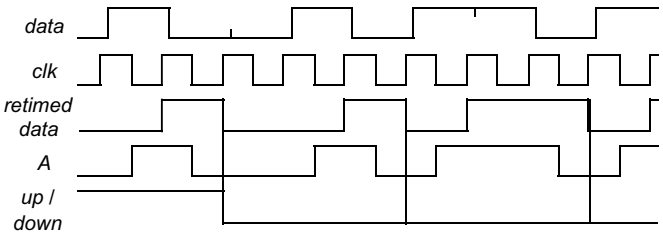




Clock lagging data:



Clock leading data:



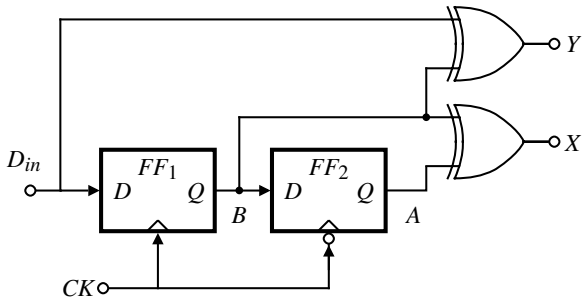
- Similar to the Alexander phase detector
- Simpler implementation

† M. Meghelli, et. al. *ISSCC*'2000, pp. 56-57.

Half-Rate Detectors

- These detectors sense the input random data at full rate but employ a VCO running at half-rate.
- Failure of the Hogge detector:

  A random sequence can be selected such that the half-rate clock continues to sample a high level on the data waveforms.



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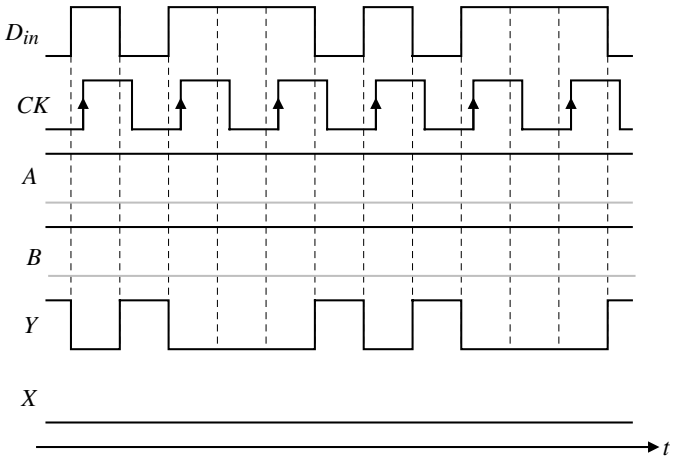
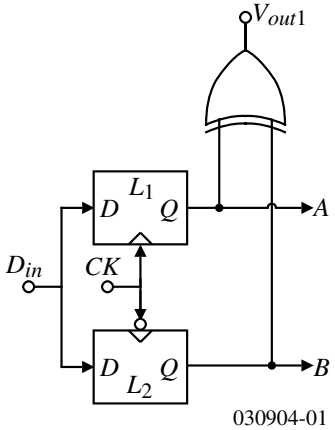


Half-Rate Detectors – Continued

What is required is to use *both* edges of the half-rate clock.

A simple linear half-rate PD using D latches:



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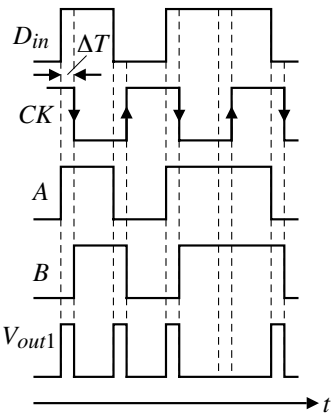


This detector:

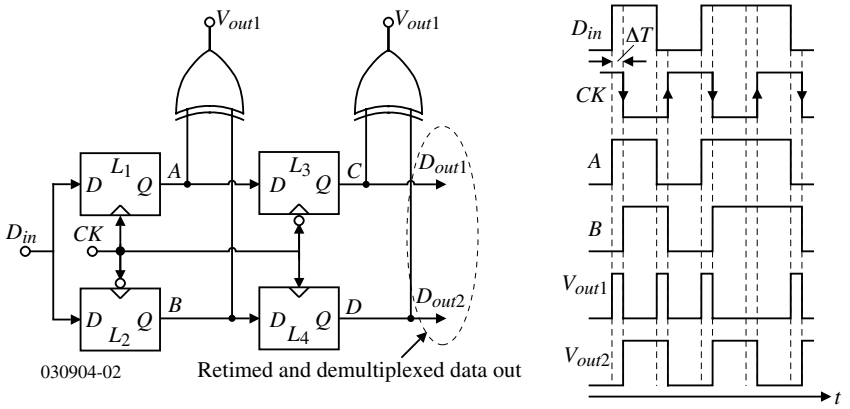
1.) Detects data edges

2.) Produces proportional pulses

However, it must also provide a reference output so as to uniquely represent the phase error for different data transitions.

Complete Linear Half-Rate PD

$C \oplus D$ gives pulses of width $T_{CK}/2$ which serves as the reference output.



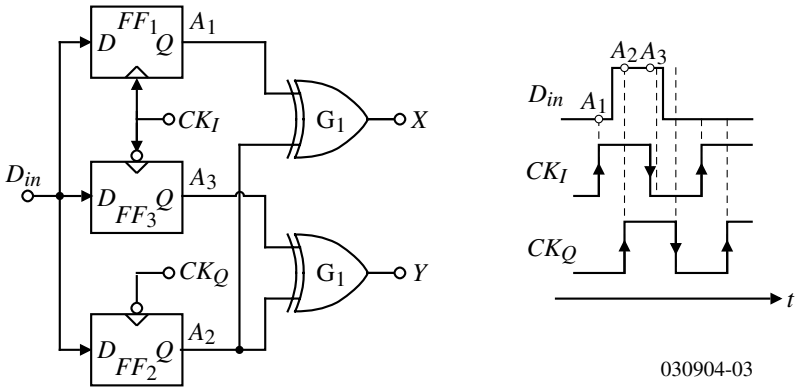
How does the PD lock to random data?

If the clock edge is to strobe the data in the middle of the eye, then the proportional pulses are $T_{CK}/4$ wide. (The disparity between the average values of these outputs is removed by scaling down the effect of the output of the second EXOR by a factor of two (i.e. halving the current in the charge pump.)

Early-Late Circuits as a Half-Rate PD

Since the Alexander PD already requires sampling on both clock edges for full-rate detection, it must employ additional phase of the clock if it is to operate in the half-rate mode.

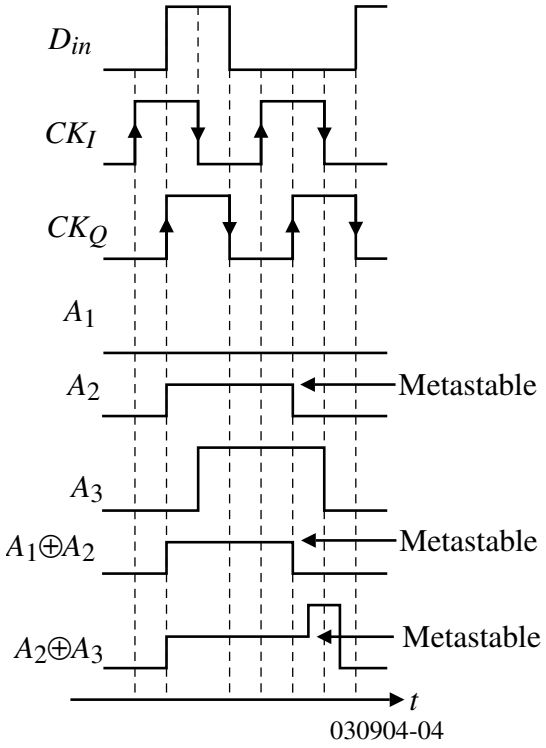
Use of quadrature clocks for binary half-rate detection:



A_1, A_2, and A_3 have the same role as the consecutive samples in a full-rate counterpart. However, the flip-flops generate skewed outputs requiring additional retiming latches before the results can be applied to XOR gates.

Early-Late Circuits as a Half-Rate PD – Continued

Effect of skews under locked condition (when CK_Q samples the data zero crossings driving FF_3 into metastability):



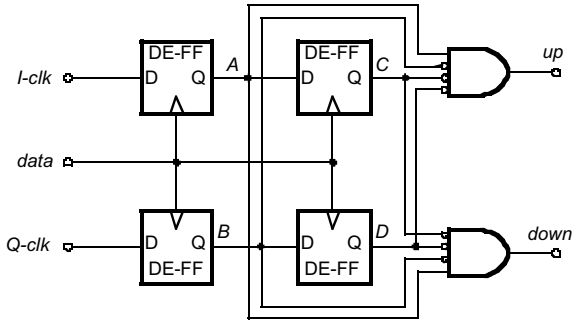
If A_2 is metastable, then $A_1 \oplus A_2$ and $A_2 \oplus A_3$ are metastable. Since A_3 holds its value for $T_{CK}/4$ seconds after A_2 changes, then $A_2 \oplus A_3$ produce an extraneous pulse of width $T_{CK}/4$ causing the VCO to be disturbed.

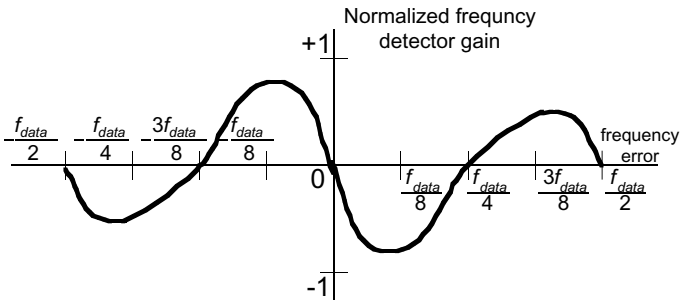
$\therefore$ It desirable to delay A_1 by $T_{CK}/2$ and A_2 by $T_{CK}/4$.

FREQUENCY DETECTORS FOR RANDOM DATA

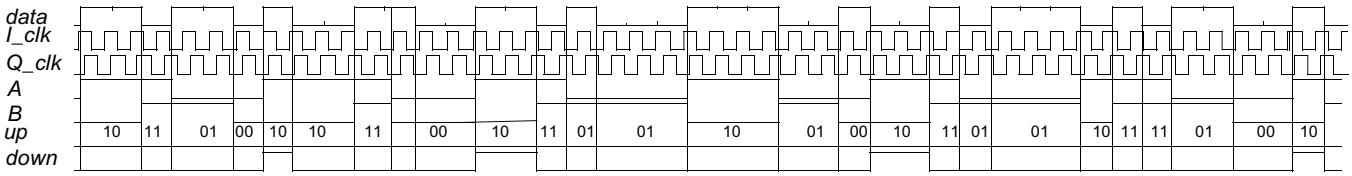
Rotational Frequency Detectors

Block diagram (Richman)[†]





Timing diagram example: (VCO clock is faster than the data rate)

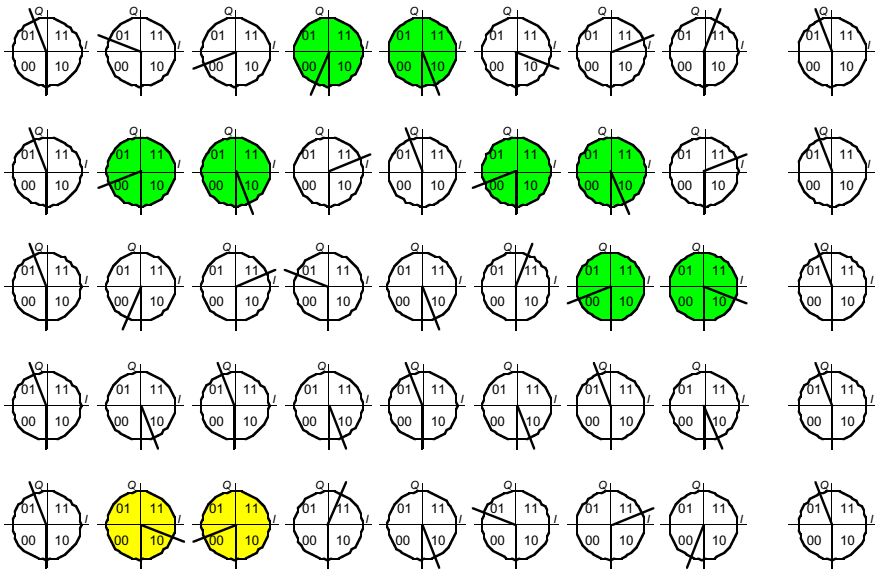


- Pull in range: ±25% of data rate
- Prone to false locking in presence of jitter and/or short data pattern
- AB changing from 00 to 10 → DOWN pulse, AB changing from 10 to 00 → UP pulse

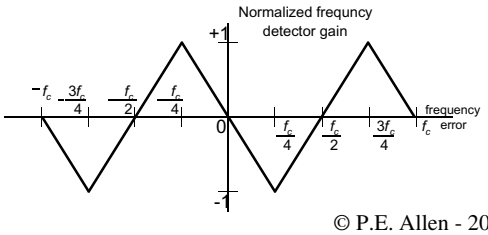
[†] D. Richman, *Proc. of IRE*, pp. 106-133, Jan. 1954.

Phasor DiagramExamples of Rotational Frequency Detectors

Phasor diagrams for a 0101 data pattern:

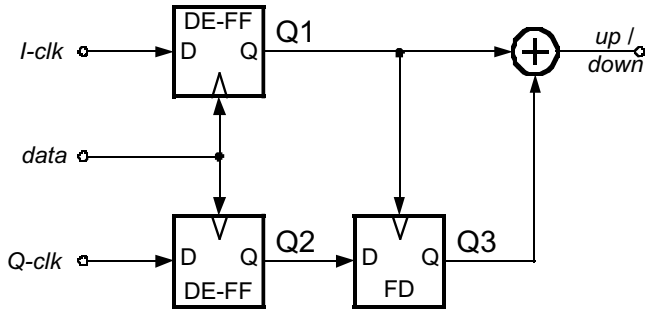


If the VCO frequency is off more than 50%, the frequency is in the wrong direction.



Rotational Frequency Detectors – Continued

A simpler implementation of the Richman frequency detector (Pottbacker)[†]. The data samples the clock.



Logic Table of Pottbacker's Frequency Detector		
Q1	Q2	Q3
X	1	0
Rising	0	-1
Falling	0	+1

- Very similar characteristics to that of Richman's frequency detector, however, the implementation is simpler.
- Pull-in range: ±25% of data rate
- Prone to false locking in the presence of jitter and/or short data patterns

[†] A. Pottbacker, et. al., *IEEE JSSC*, pp. 1747-1751, Dec. 1992.

CDR ARCHITECTURES

Clock Recovery – Spectral Line, Early-Late

Enam, Abidi 1992

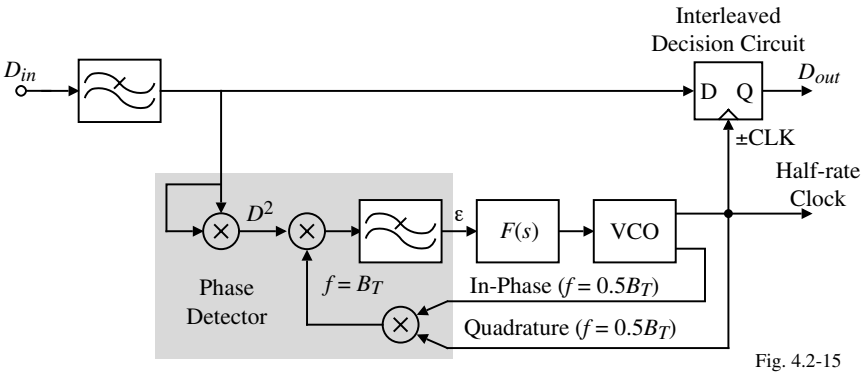


Fig. 4.2-15

Interleaved decision circuit

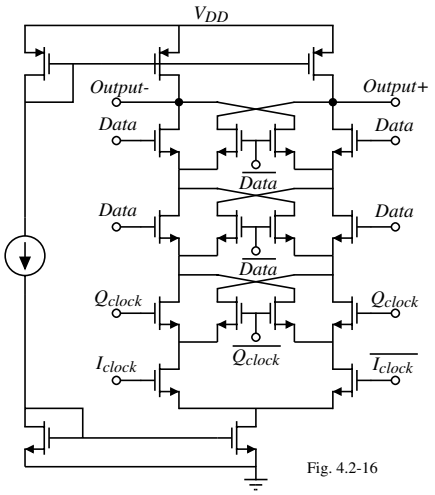


Fig. 4.2-16

Comments:

- Good example of CMOS solution to practical clock recovery circuits
- Circuit can be analyzed as spectral line or as early-late.

Clock Recovery - Quadricorrelator

Analog version has three loops sharing the same VCO.

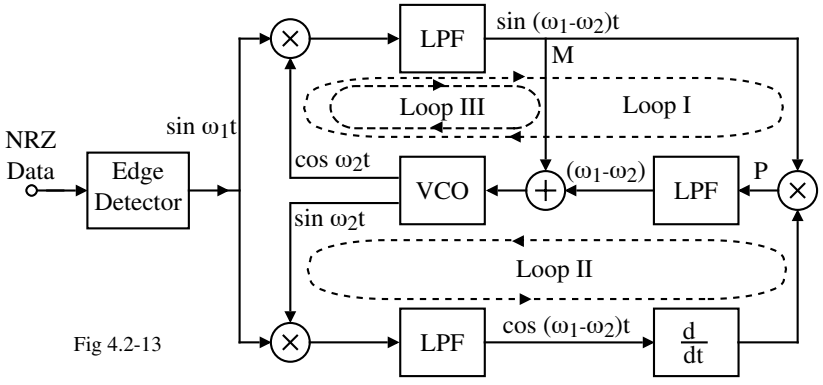


Fig 4.2-13

Edge detector plus three loops-

Loops I and II perform frequency detection

Loop III performs phase detection

Operation:

The signal at P is $(\omega_1-\omega_2)\cos^2(\omega_1-\omega_2) \Rightarrow$ VCO is driven by $\sin(\omega_1-\omega_2)t + (\omega_1-\omega_2)$

Loops I and II drive the VCO to lock when $\omega_1 \neq \omega_2$. As $|\omega_1-\omega_2|$ approaches zero, Loop III begins to generate an asymmetrical signal at node M assisting the lock process. Finally, when $\omega_1 \approx \omega_2$, the dc feedback signal produced by Loops I and II approaches zero and Loop III dominates, locking the VCO output to the input data.

Quadricorrelator – Continued

The use of frequency detection in the quadricorrelator makes the capture range independent of the locked loop bandwidth, allowing a small cutoff frequency in the LPF of Loop III so as to minimize the VCO drift between data transitions.

Because Loops I and II can respond to noise and spurious components, it is desirable to disable these loops once phase lock has been attained.

Since the combination of an edge detector and a mixer can be replaced with a double-edge triggered flipflop, the quadricorrelator can be implemented in a digital form as shown below.

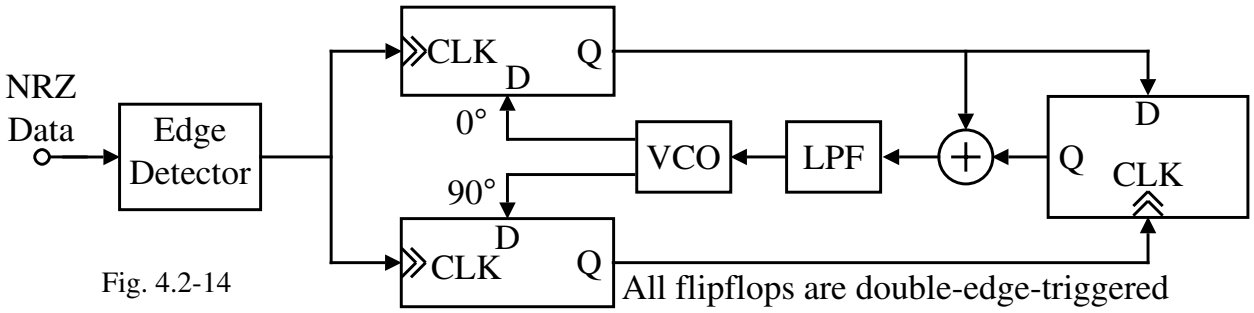


Fig. 4.2-14

JITTER IN CDR CIRCUITS

Jitter Influence on Clock Recovery

Types of jitter:

- Long term jitter

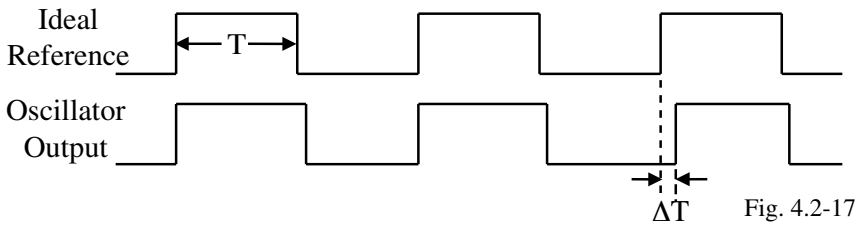


Fig. 4.2-17

  - Diverges for a free-runnng oscillator
  - Meaningful only in a phase-locked system
  - Depends on PLL dynamics

- Cycle-to-cycle jitter

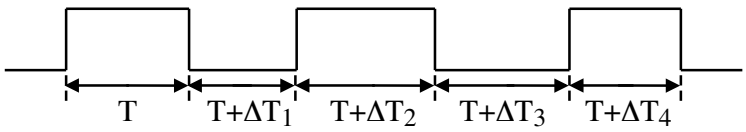


Fig. 4.2-18

  - Of great interest in many timing applications
  - Mostly due to the oscillator
  - Usually too fast for the PLL to correct

Jitter Due to Device Noise

1/f noise:

1/f noise is inversely proportional to frequency and causes the frequency to change very slowly. Easily suppressed by a wide PLL bandwidth.

$$\overline{e_{ni}^2} = \frac{B}{fW_iL_i} \quad (V^2/Hz) \qquad \text{and} \qquad \overline{i_{ni}^2} = \frac{2BK'I_i}{fL_i^2} \quad (A^2/Hz)$$

where

$$B = \frac{KF}{2C_{ox}K'}$$

Thermal noise:

Thermal noise is assumed to be "white" and is modeled in MOSFETs as,

$$\overline{e_{ni}^2} \approx \frac{8kT}{3g_m} \quad (V^2/Hz) \qquad \text{and} \qquad \overline{i_{ni}^2} \approx \frac{8kTg_m}{3} \quad (A^2/Hz)$$

The relationship between phase noise and cycle-to-cycle jitter is,

$$\Delta T^2(\text{rms}) \approx \frac{4\pi}{\omega_o^3} S\phi(\omega)\ (\omega-\omega_o)^2$$

(Razavi: *IEEE Trans. on Circuits and Systems, Part II*, Jan. 99)

Sources of Jitter

- Input jitter

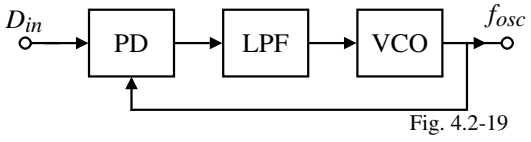


Fig. 4.2-19

- VCO jitter due to device noise

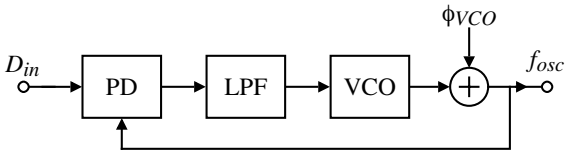


Fig. 4.2-20

- VCO jitter due to ripple on control line

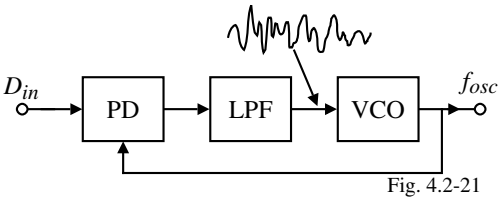


Fig. 4.2-21

- Injection pulling of the VCO by the data

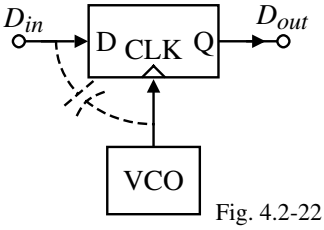


Fig. 4.2-22

- Substrate and supply noise

Substrate and Supply Noise

How Do Carriers Get Injected into the Substrate?

1.) Hot carriers (substrate current)

2.) Electrostatic coupling (across depletion regions and other dielectrics)

3.) Electromagnetic coupling (parallel conductors)

Why is this a Problem?

With decreasing channel lengths, more circuitry is being integrated on the same substrate. The result is that noisy circuits (circuits with rapid transitions) are beginning to adversely influence sensitive circuits (such as analog circuits).

Present Solution:

Keep circuit separate by using multiple substrates and put the multiple substrates in the same package.

Hot Carrier Injection in CMOS Technology without an Epitaxial Region

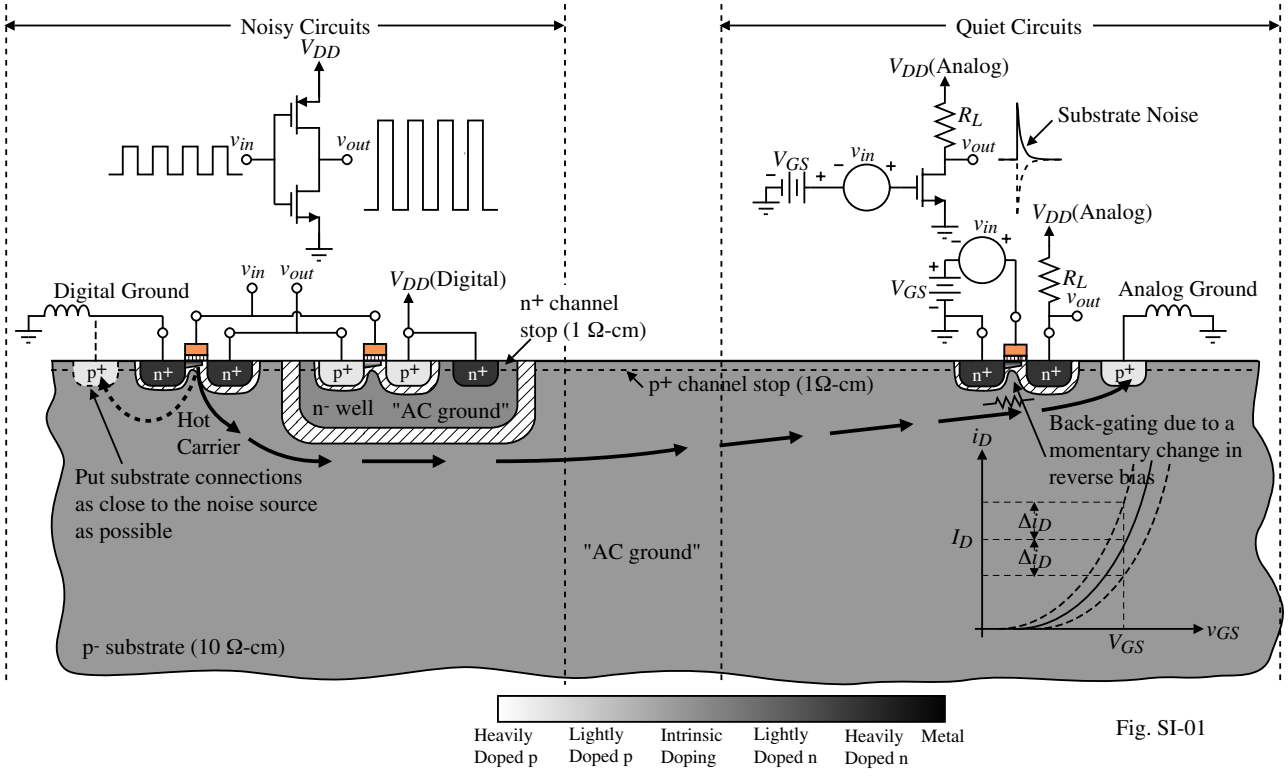


Fig. SI-01

Hot Carrier Injection in CMOS Technology with an Epitaxial Region

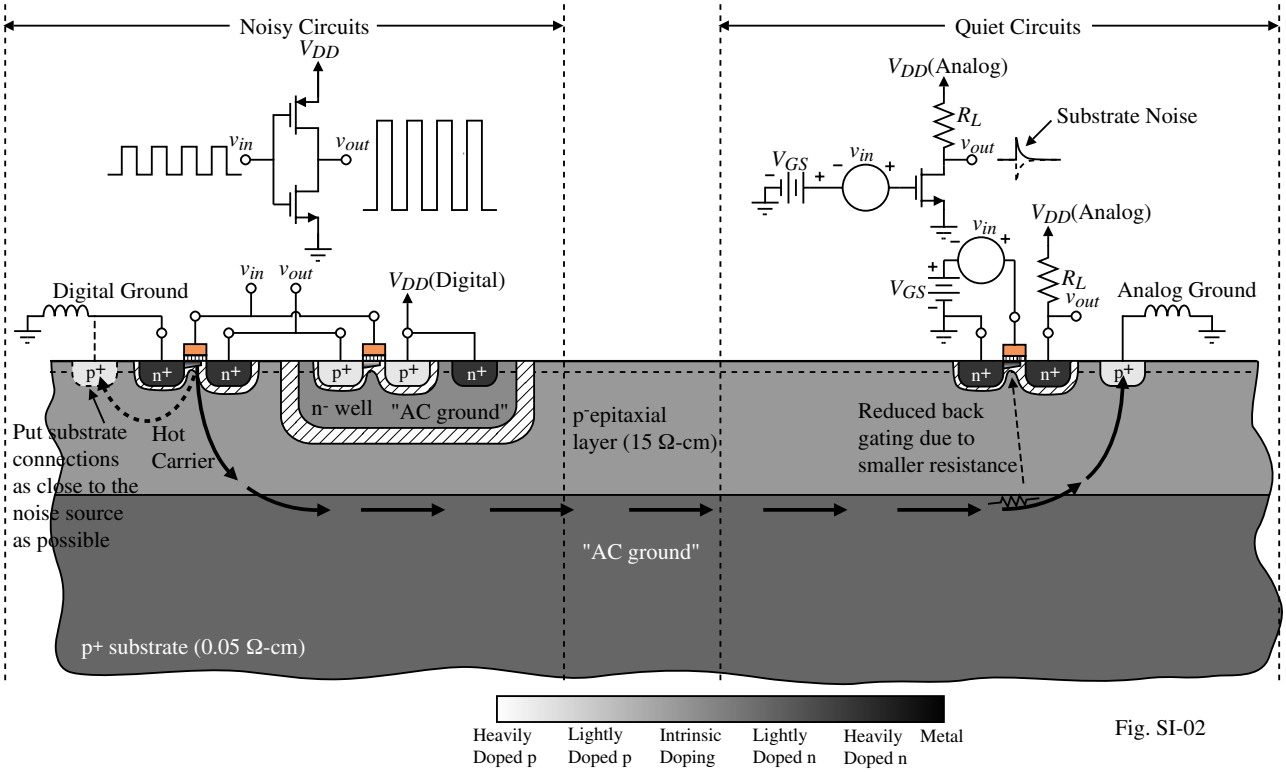
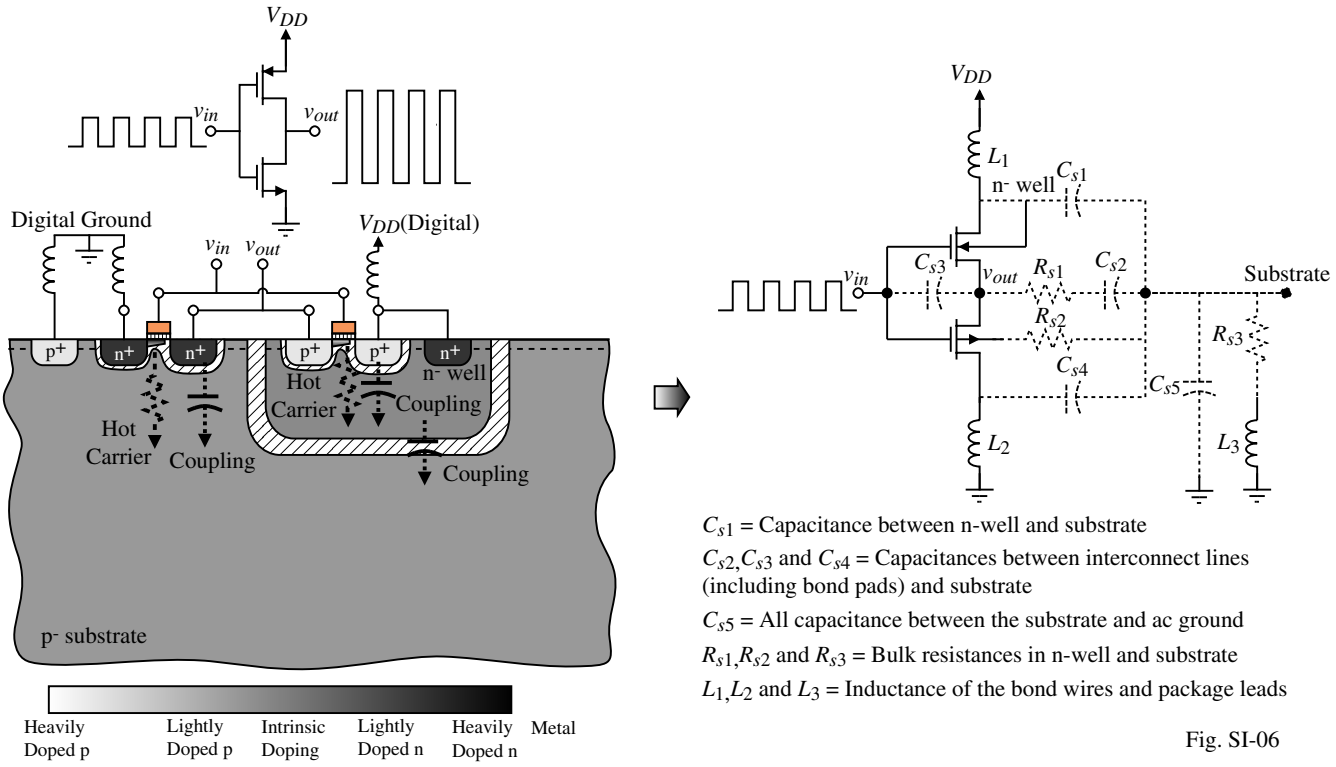


Fig. SI-02

Computer Model for Substrate Interference Using SPICE Primitives

Noise Injection Model:



C_{s1} = Capacitance between n-well and substrate

C_{s2},C_{s3} and C_{s4} = Capacitances between interconnect lines (including bond pads) and substrate

C_{s5} = All capacitance between the substrate and ac ground

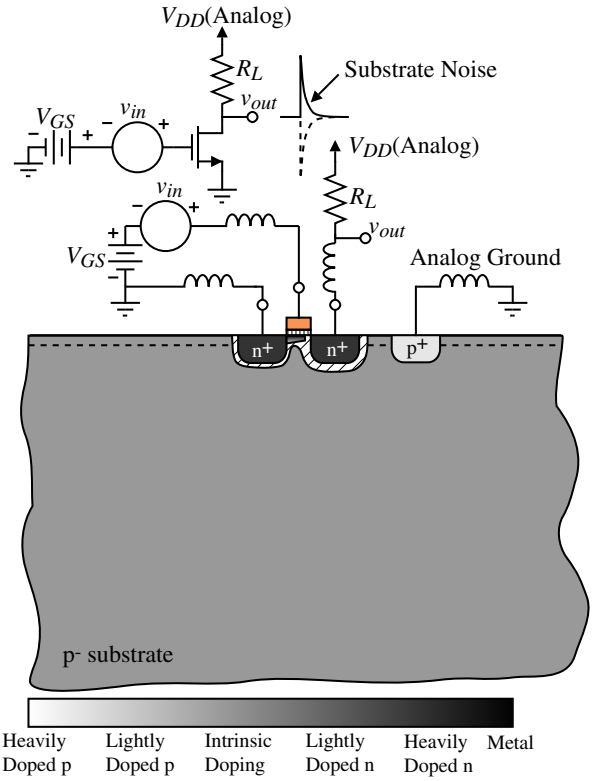
R_{s1},R_{s2} and R_{s3} = Bulk resistances in n-well and substrate

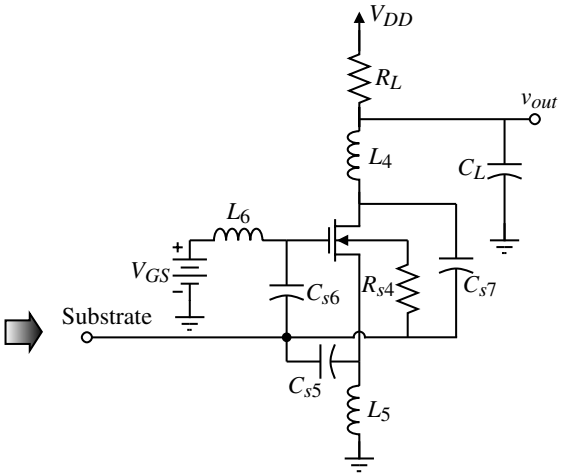
L_1,L_2 and L_3 = Inductance of the bond wires and package leads

Fig. SI-06

Computer Model for Substrate Interference Using SPICE Primitives

Noise Detection Model:





C_{s5},C_{s6} and C_{s7} = Capacitances between interconnect lines (including bond pads) and substrate

R_{s4} = Bulk resistance in the substrate

L_4,L_5 and L_6 = Inductance of the bond wires and package leads

Fig. SI-07

Other Sources of Substrate Injection

(We do it to ourselves and can't blame the digital circuits.)

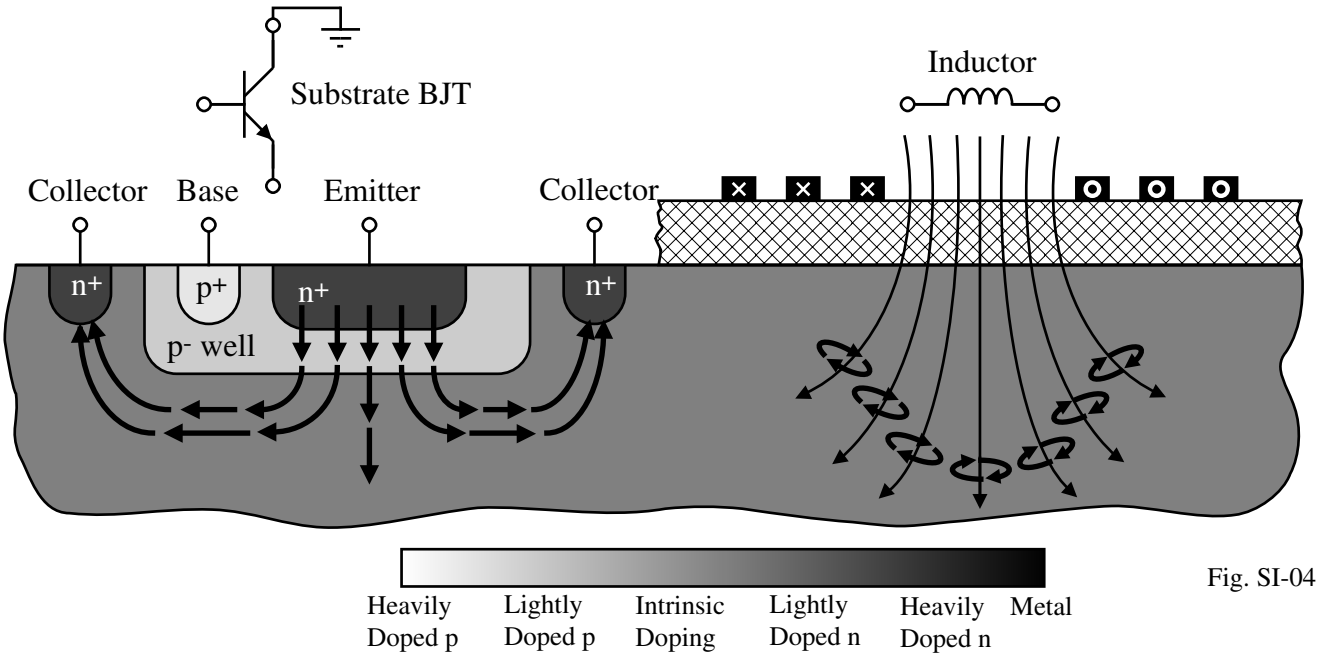


Fig. SI-04

Also, there is coupling from power supplies and clock lines to other adjacent signal lines.

What is a Good Ground?

- On-chip, it is a region with very low bulk resistance.

  It is best accomplished by connecting metal to the region at as many points as possible.

- Off-chip, it is all determined by the connections or bond wires.

  The inductance of the bond wires is large enough to create significant ground potential changes for fast current transients.

  $$v = L\frac{di}{dt}$$

  Use multiple bonding wires to reduce the ground noise caused by inductance.

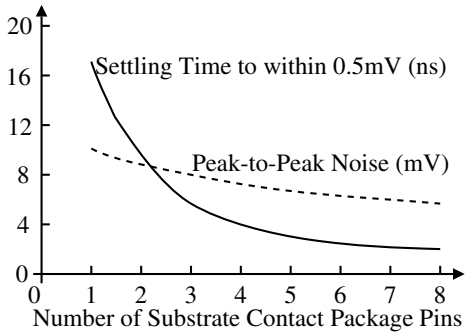


Fig. SI-08

- Fast changing signals have part of their path (circuit through ground and power supplies. Therefore bypass the off-chip power supplies to ground as close to the chip as possible.

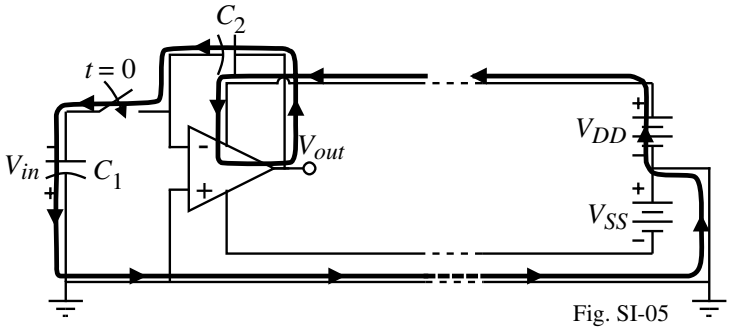


Fig. SI-05

Summary of Substrate Interference

- Methods to reduce substrate noise
  1.) Physical separation
  2.) Guard rings placed close to the sensitive circuits with dedicated package pins.
  3.) Reduce the inductance in power supply and ground leads (best method)
  4.) Connect regions of constant potential (wells and substrate) to metal with as many contacts as possible.
- Noise Insensitive Circuit Design Techniques
  1.) Design for a high power supply rejection ratio (PSRR)
  2.) Use multiple devices spatially distinct and average the signal and noise.
  3.) Use "quiet" digital logic (power supply current remains constant)
  4.) Use differential signal processing techniques.
- Some references

1.) D.K. Su, M.J. Loinaz, S. Masui and B.A. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal IC's," *J. of Solid-State Circuits*, vol. 28, No. 4, April 1993, pp. 420-430.

2.) K.M. Fukuda, T. Anbo, T. Tsukada, T. Matsuura and M. Hotta, "Voltage-Comparator-Based Measurement of Equivalently Sampled Substrate Noise Waveforms in Mixed-Signal ICs," *J. of Solid-State Circuits*, vol. 31, No. 5, May 1996, pp. 726-731.

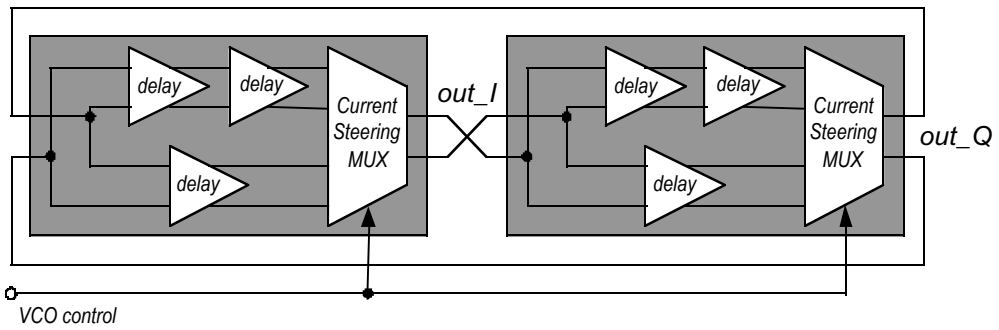
3.) X. Aragones, J. Gonzalez and A. Rubio, *Analysis and Solutions for Switching Noise Coupling in Mixed-Signal ICs*, Kluwer Acadmic Publishers, Boston, MA, 1999.

VOLTAGE CONTROLLED OSCILLATORS FOR CDR APPLICATIONS

Comparison of VCOs

Comparison of VCO Topologies				
	Relaxation	Ring	LC	Quadrature LC
Control Voltage	Differential ↑	Differential ↑	Single-ended ↓	Differential ↑
Phase Noise	High ↓	High ↓	Low ↑	Moderate
Tuning Range	Wide ↑	Wide ↑	Narrow ↓	Medium
VCO Gain	High ↓	High ↓	Low ↑	Medium
PVT Variations	High ↓	High ↓	Low ↑	Low ↑

Ring Oscillator Example†



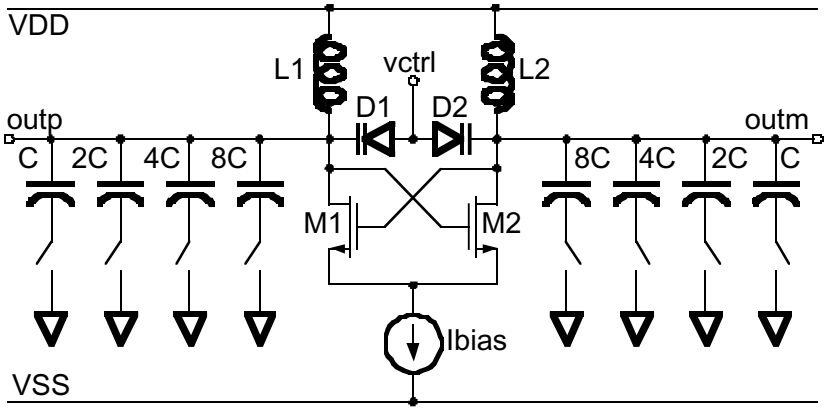
Comments:

- Tuning can be split into fine and coarse control
- Very wide tuning range
- Differential control
- Moderate phase noise

(See also, Y. Eken, "High Frequency Voltage Controlled Ring Oscillators in Standard CMOS," Ph.D. Dissertation, School of ECE, Georgia Tech, Nov. 2003)

† R. Walker, *ISSCC*'1997, pp. 246-247.

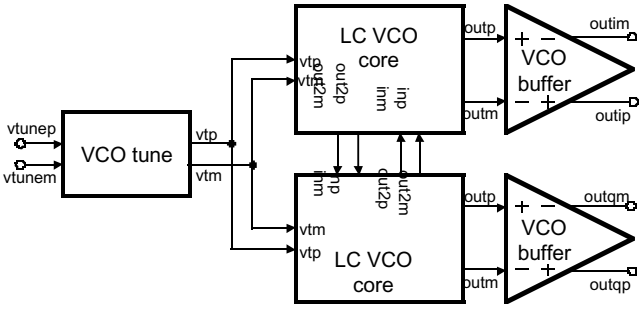
LC VCO Example



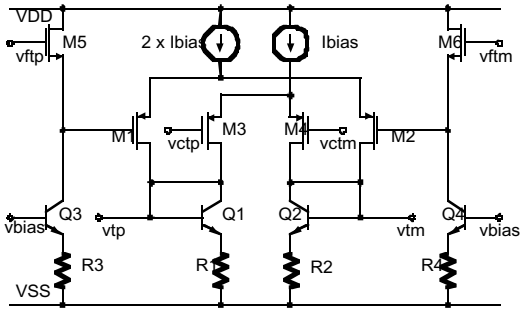
Comments:

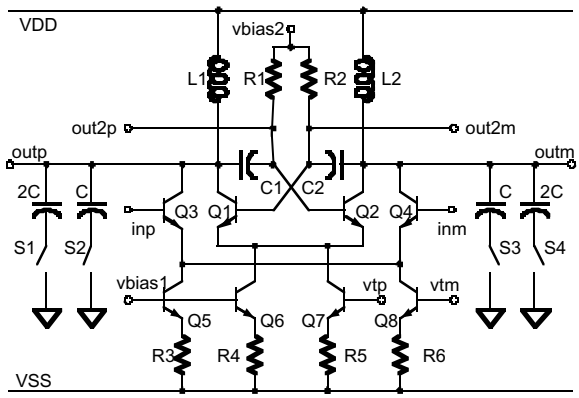
- Fine tuning is through varactor control
- Coarse tuning is achieved by binary weighted capacitor array
- Low tuning range
- Single-ended control
- Very good phase noise characteristics

Quadrature LC VCO Example



T.P. Liu, *IEEE VLSI* 1999, pp. 55-56





A.L. Coban, et. al., *VLSI* 2001, pp. 119-120

- Two identical LC VCOs are coupled in quadrature.
- VCO tuning is achieved through:
  - Adjusting the coupling between the two oscillator cores
  - Changing the LC-tank capacitance

A Design Procedure for VCOs for CDR Applications

The following procedure seeks to maximize the tuning range and minimize the phase noise with the knowledge of four parameters:

- Load capacitance, C_L
- Required output voltage swing
- Center frequency, f_o
- Power

The first two parameters may require a buffer as shown below.

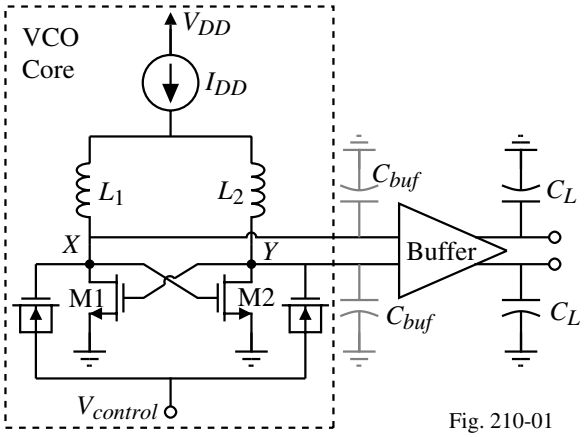


Fig. 210-01

Design Procedure for VCOs – Continued

Other circuits that the VCO may have to drive include a flip-flop in a divider chain, two flipflops in the demultiplexer and a 50Ω output driver:

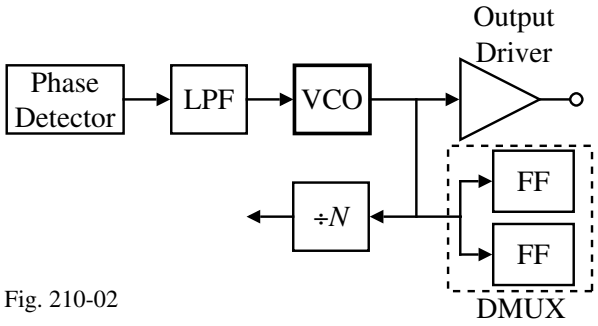


Fig. 210-02

Procedure:

1.) With the power budget and hence the value of I_{DD} the width of M1 and M2 is chosen to yield an average CM level of approximately $0.5V_{DD}$ at the X and Y nodes. Note that when $V_X = V_Y$, that $V_{DG1} = V_{DG2} = 0$.

$$I_D = \frac{K'W}{2L}(V_{GS}\text{-}V_T)^2\text{: } V_{GS} = 0.5V_{DD} \text{ and } I_{DD} \quad \rightarrow \quad \frac{W}{L} \quad \rightarrow \quad g_m$$

2.) Design the inductors, L_1 and L_2. To maximize the tuning range (and Q) the inductance must be minimized. To get the oscillator to start-up, the following must hold:

$$(g_m R_{p,min})^2 = 1$$

However, $R_{p,min}$, is the parallel resistance of the tank and is primarily due to the inductor.

$$R_{p,min} \approx QL_{min}\omega_{osc} \quad \rightarrow \quad (g_m\, QL_{min}\omega_{osc})^2 = 1 \quad \rightarrow \quad L_{min} = \frac{1}{g_m Q \omega_{osc}}$$

The above assumes that the Q is approximately constant with the value of L_{min}.

VCO Design Procedure – Continued

3.) With $L = L_{min}$, the oscillation amplitude is quite small in order to maintain unity loop gain. If the amplitude grows, the transistor nonlinearities reduce the loop gain which may prevent full swing. One must also be careful of the variation of g_m and Q with PVT corners possibly prohibiting oscillation at some corners. Therefore, the values of L and R_p must sufficiently exceed L_{min} and $R_{p,min}$ to provide the required voltage swings and start under worst case conditions.

4.) The value of R_p can be related to the required output swing as follows. M1 and M2 each have an average current of $0.5I_{DD}$. If the drain currents are approximated by sinusoids varying between I_{DD} and zero, the V_X and V_Y swing from $0.5V_{DD}$-$I_{DD}R_p$ and $0.5V_{DD}$+$I_{DD}R_p$. For this voltage sinusoid, the largest peak voltage is $0.5V_{DD}$=$I_{DD}R_p$ giving

$$R_{p,swing} = \frac{V_{DD}}{2I_{DD}} \quad \text{(minimum parallel tank resistance giving maximum swing)}$$

$$\therefore \quad L_{opt} = \frac{V_{DD}}{2I_{DD}} \cdot \frac{1}{Q\omega_{osc}}$$

5.) With W/L and L_{opt} known, the varactor capacitance can be found as

$$C_{tot} = \frac{1}{\omega_{osc}^2 L_{opt}}$$

where $C_{tot} = C_{var} + C_{gs} + C_{bds} + 4C_{gd} + C_{inductor} + C_{buffer}$

Designing a VCO for CDR Applications

Use the above procedure to design a VCO for 5GHz using 0.18μm CMOS technology having $K_N' = 120\mu A/V^2$ and $V_{TN} = 0.5V$. Assume the Q of the inductor is 5, $V_{DD} = 1.8V$ and the power is to be 5mW. Assume that $C_{gs} + C_{bds} + 4C_{gd} = 300fF$, $C_{inductor} = 50fF$, and $C_{buffer} = 200fF$.

Solution

1.) From the specifications we get $I_{DD} = 5mW/1.8V = 2.78mA$. The W/L can be found as,

$$\frac{W}{L} = \frac{I_{DD}}{K_N'(0.5V_{DD}\text{-}V_{TN})^2} = \frac{2.78mA}{0.12mA/V^2\,(0.9\text{-}0.5)^2} = 144.67 \approx 145$$

$$g_m = \sqrt{2K_N'\,(0.5I_{DD})145} = 6.95mS$$

2.) The minimum inductance can be found as

$$L_{min} = \frac{1}{g_m Q\omega_{osc}} = \frac{1}{6.95mS \cdot 5 \cdot 2\pi \cdot 5x10^9} = 0.916nH$$

3.) The value of R_p for maximum swing is

$$R_{p,swing} = \frac{V_{DD}}{2I_{DD}} = \frac{1.8}{2 \cdot 2.78mA} = 323.7\Omega$$

$$\therefore \quad L_{opt} = \frac{V_{DD}}{2I_{DD}} \cdot \frac{1}{Q\omega_{osc}} = 323.7\Omega \left(\frac{1}{5 \cdot 10\pi x10^9}\right) = 2.06nH$$

Example - Continued

4.) The value of C_{tot} is,

$$C_{tot} = \frac{1}{\omega_{osc}^2 L_{opt}} = \frac{1}{(10\pi \text{x} 10^9)^2 (2.06\text{nH})} = 491.6 \text{ fF}$$

Unfortunately, we see that $C_{var} = 491.6\text{fF} - 550\text{fF} = -58\text{fF}$

Our only choices are:

a.) Decrease the inductor size which will reduce the output swing.

b.) Decrease the buffer input capacitance which will degrade the drive capability.

c.) Decrease the W/L of the transistors by decreasing the power dissipation

5.) Since the inductance capacitance is small compared to the buffer input capacitance, we will choose to reduce the buffer input capacitance by a half giving

$C_{var} = 491.6\text{fF} - 450\text{fF} = 42\text{fF}$

SUMMARY

- CDR circuits are used for recovering the clock from NRZ data
- The PLL consists of a phase detector, lowpass filter and VCO
- Phase detectors for random data
  - Linear phase detectors (Hogge)
  - Binary phase detectors (Alexander)
  - Half-rate detectors (linear and binary)
- Frequency detectors for random data
  - Rotational frequency detectors (Richman, Pottbacker))
- Jitter in CDR circuits
  - Long term and short term
  - Sources include input, device noise, ripple on VCO control, injection pulling of the VCO, and substrate and supply noise
- VCOs for CDR circuits
  - LC – lower phase noise, less tuning range
  - Ring oscillator – higher phase noise, wide tuning range, compatible with digital CMOS
  - Design procedure for LC VCOs