Analysis and Design of Phase-Locked Loops

Prof. Shen-Iuan Liu

Depart. of Electrical Engineering

National Taiwan University

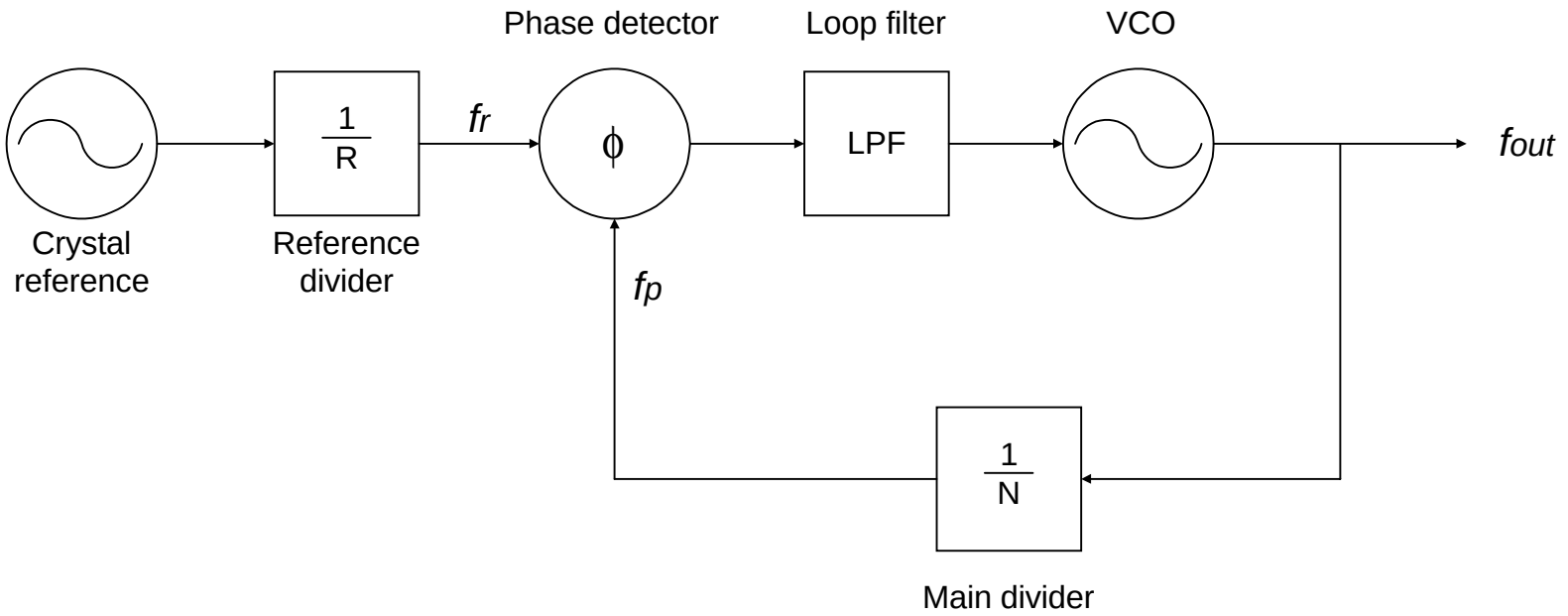
Taipei, Taiwan 10617, R.O.C.

Tel.: (02)23635251 ext. 239

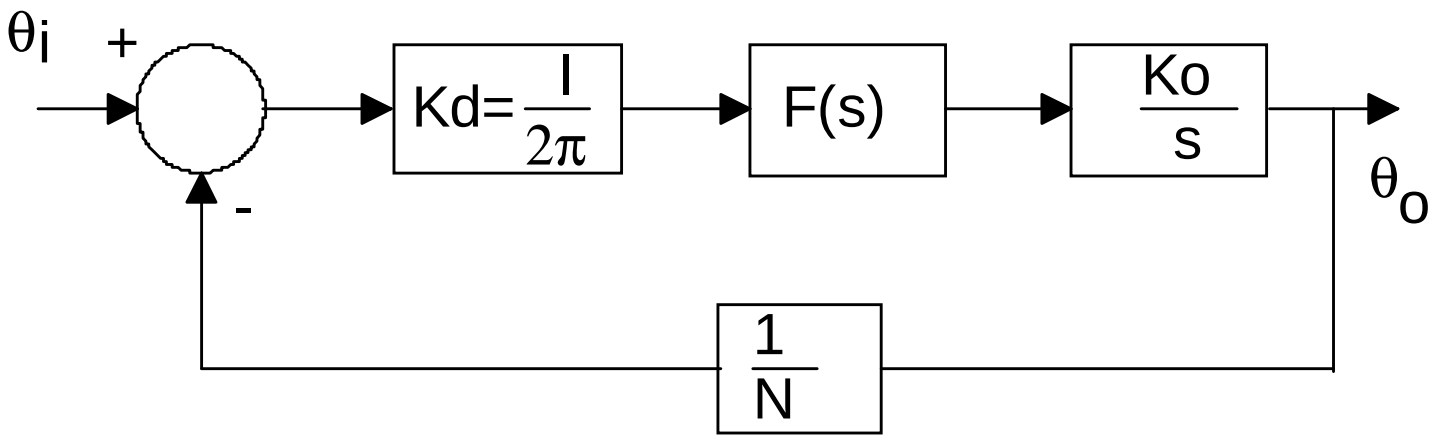
Fax: (02)23671909

Email: lsi@cc.ee.ntu.edu.tw

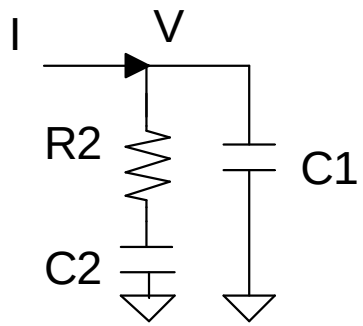
Block diagram of a phase-locked loop



Linear model of a phase-locked loop



Loop Filter (2nd Order)



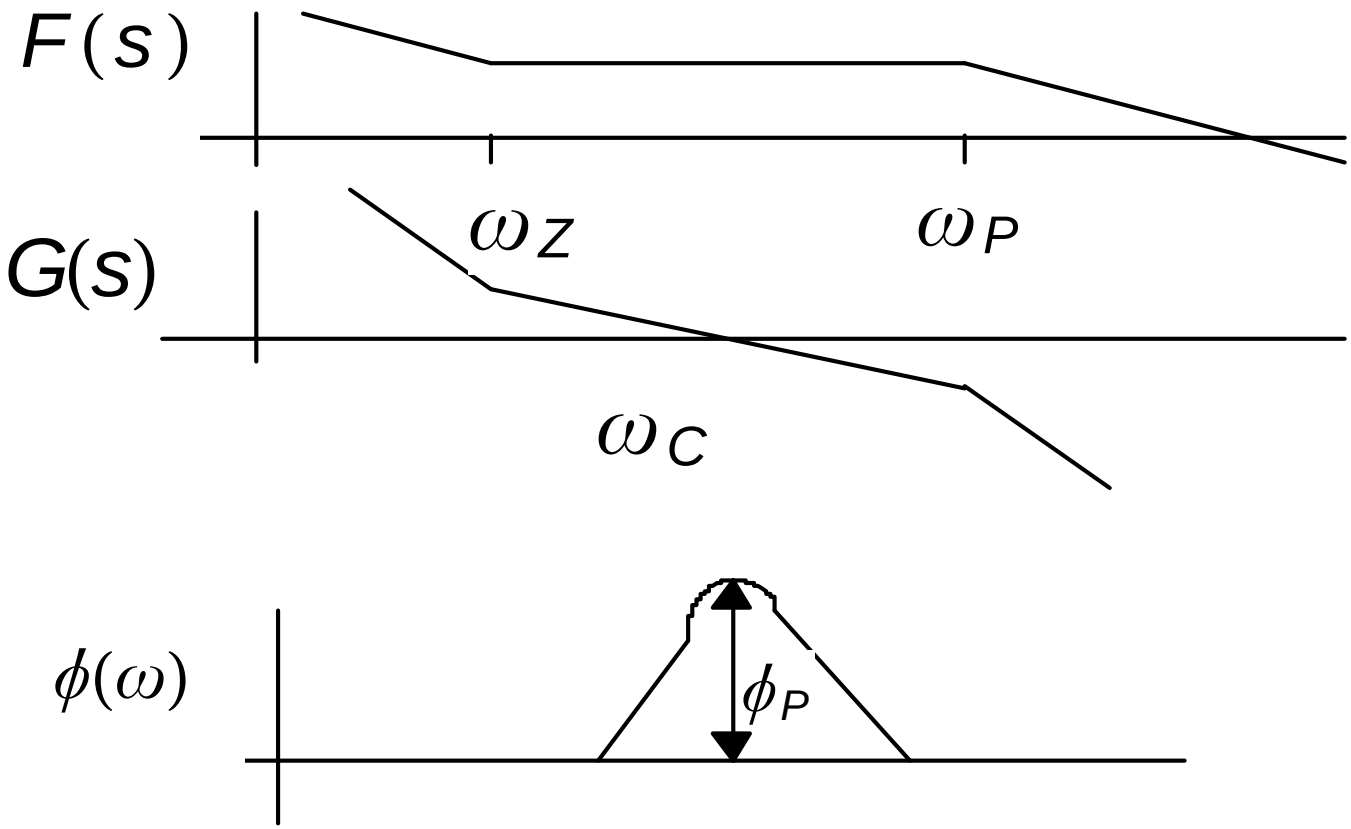
$$\frac{V}{I} = F(s) = (R_2 + \frac{1}{sC_2}) \parallel \frac{1}{sC_1} = \frac{sC_2R_2 + 1}{s(sC_1C_2R_2 + C_1 + C_2)}$$

$$F(s) = \frac{1}{C_1 + C_2} \frac{sT_2 + 1}{s(sT_1 + 1)}$$

$$\text{where } T_1 = R_2 \frac{C_1C_2}{C_1 + C_2}, T_2 = R_2C_2$$

$$\omega_Z = T_2^{-1}, \omega_p = T_1^{-1} = \omega_Z(1 + \frac{C_2}{C_1})$$

Opened-Loop Response



$$Opened-loop\ gain\ G(s) = \frac{K_d K_o F(s)}{sN}$$

Opened-Loop Response

$$Gain: -G(s)|_{s=j\omega} = \frac{-K_d K_o (1 + j\omega T_2)}{\omega^2 C_1 N (1 + j\omega T_1)} \cdot \frac{T_1}{T_2}$$

$$Phase: \phi(\omega) = \tan^{-1}(\omega T_2) - \tan^{-1}(\omega T_1) + 180^o$$

$$Let \frac{d\phi(\omega)}{d\omega} = o \text{ at } \omega = \omega_C$$

$$\omega_C = \frac{1}{\sqrt{T_1 T_2}}$$

Maximum Phase Margin

$$\phi_P = \tan^{-1}(\omega_C T_2) - \tan^{-1}(\omega_C T_1)$$

Opened-Loop Response

$$\omega = \omega_C \rightarrow |G(j\omega_c)| = 1 \rightarrow C_1 = \frac{K_d K_o T_1}{\omega_C^2 N T_2} \cdot \left\| \frac{1 + j\omega_C T_2}{1 + j\omega_C T_1} \right\|$$

$$T_1 = \frac{\sec \phi_P - \tan \phi_p}{\omega_C} \text{ and } T_2 = \frac{1}{\omega_C^2 T_1}$$

Hence, if ωc and ϕp are specified,

$$C_1 = \frac{T_1}{T_2} \cdot \frac{K_d K_o}{\omega_C^2 N} \cdot \sqrt{\frac{1 + (\omega_C T_2)^2}{1 + (\omega_C T_1)^2}}$$

$$C_2 = C_1 \cdot \left(\frac{T_2}{T_1} - 1\right)$$

$$R_2 = \frac{T_2}{C_2}$$

Closed-Loop Response

$$Opened-loop\ gain\ G(s)=\frac{K_dK_oF(s)}{sN}$$

$$Closed-loop\ gain\ H(s)=\frac{NG(s)}{1+G(s)}$$

Third-order system

$$G(s)=\frac{K_dK_oF(s)}{sN} \quad where \quad F(s)=\frac{K_F(s+\omega_z)}{s(\frac{s}{\omega_p}+1)} \quad K_F=\frac{R_2C_2}{C_1+C_2}$$

$$\Rightarrow G(s)=\frac{K(s+\omega_z)}{s^2(\frac{s}{\omega_p}+1)} \quad where \quad K=\frac{K_dK_oK_F}{N}$$

Closed-Loop Response

$$If \quad G(s)\big|_{s=j\omega_c} = 1 \qquad \because \omega_c^{\,2} = \omega_p \omega_z \qquad \Rightarrow \; K = \omega_c$$

$$H(s) = \frac{NG(s)}{1+G(s)} = \frac{NK(s+\omega_z)}{s^2\left(\frac{s}{\omega_p}+1\right)+Ks+K\omega_z}$$

γ	PM
1	0°
2	36.9°
3	53.1°
4	61.9°
5	67.4°
6	71°

$$Let \quad r \equiv \frac{\omega_c}{\omega_z} = \frac{\omega_p}{\omega_c}$$

Closed-Loop Response

$$\Rightarrow H(s) = \frac{N\omega_c{}^2 r(s+\omega_c/r)}{s^3 + s^2\omega_c r + s\omega_c{}^2 r + \omega_c{}^3} = \frac{N\omega_c{}^2 r(s+\omega_c/r)}{(s+\omega_c)[s^2 + s\omega_c(r-1) + \omega_c{}^2]}$$

$$\frac{H(s)}{N} = \frac{\omega_c}{(s+\omega_c)}\frac{r-1}{r-3} - \frac{\omega_c}{r-3}\frac{(r-1)s+2\omega_c}{[s^2 + s\omega_c(r-1) + \omega_c{}^2]}$$

$$Let \quad \omega_{n2} = \omega_c \quad \xi_2 = \frac{r-1}{2}$$

$$\frac{H(s)}{N} = \frac{\omega_{n2}}{\xi_2 - 1}\left[\frac{\xi_2}{s+\omega_{n2}} - \frac{\xi_2 s + \omega_{n2}}{s^2 + s2\xi_2\omega_{n2} + \omega_{n2}{}^2}\right]$$

Design Strategy

- Open loop considerations
  - Set C2 >20 • C1 for 65° phase margin
  - Set $\omega c < \omega ref / 5$
  - Set phase margin to at least 65° or at maximum

$$\phi_P = 2 \cdot \tan^{-1}\left(\sqrt{\frac{C_2}{C_1} + 1}\right) - \frac{\pi}{2}$$

Design Strategy

- Close loop considerations
  - Set C2 >20 • C1 for 65° phase margin
  - Set $\omega n < \omega ref / 10$
  - Set $\zeta >= 1$ and $\omega p / \omega n > 10$
  - Determine optimal values for PM and ωc

$$\phi_P = 2 \cdot \tan^{-1}\left(\sqrt{\frac{C_2}{C_1} + 1}\right) - \frac{\pi}{2}$$

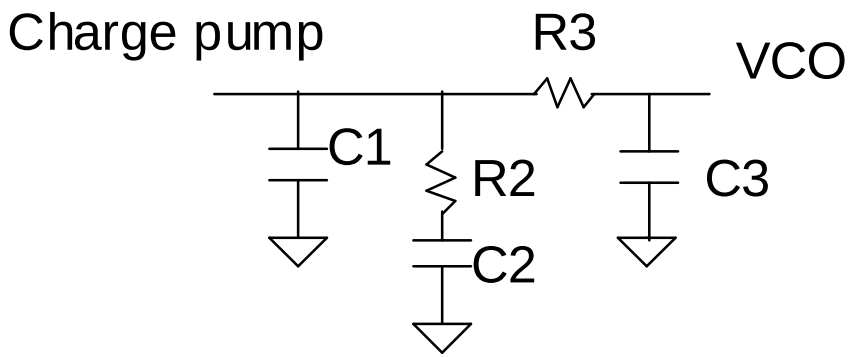
$$\omega_C = \frac{1}{R_2 C_2} \cdot \sqrt{\frac{C_2}{C_1} + 1}$$

  - Determine optimal value for ICH given R2

$$\frac{I_{CH}}{2\pi} = \frac{N}{K_o} \cdot \frac{C_1}{(R_2 C_2)^2} \cdot \left(\frac{C_2}{C_1} + 1\right)^{3/2}$$

Reference Spur Attenuation

- Current switching noise in the dividers and the charge pump circuit at the reference rate, Fref, may cause unwanted FM sidebands at RF output.
- The spurious sidebands can cause noise in adjacent channels. Additional attenuation from the added passive loop filter is required.
- 3rd-order filter



Design of the 3rd-order filter

- The added attenuation from the lowpass filter is

$$Atten = 20\log[(2\pi Fref \cdot R_3 \cdot C_3)^2 + 1]$$

$$where\ T_3 \equiv R_3 \cdot C_3$$

- In terms of the attenuation of the reference spurs added by the lowpass pole, one have

$$T_3 = \sqrt{\frac{10^{(Atten/20)} - 1}{(2\pi \cdot Fref)^2}}$$

- Recommended value of T3 is

$$5\omega_c < \frac{1}{T_3}\ and\ \frac{1}{T_3} < f_{ref}$$

Design of the 3rd-order filter

- The new open loop unity gain frequency (loop bandwidth) can be approximated to be

$$T_2 = \frac{1}{\omega_C^2 \cdot (T_1 + T_3)}$$

$$\omega_C = \frac{\tan\phi \cdot (T_1 + T_3)}{[(T_1 + T_3)^2 + T_1 \cdot T_3]} \times [\sqrt{1 + \frac{(T_1 + T_3)^2 + T_1 \cdot T_3}{[\tan\phi \cdot (T_1 + T_3)]^2}} - 1]$$

$$C_1 = \frac{T_1}{T_2} \cdot \frac{K_d \cdot K_o}{\omega_C{}^2 \cdot N} \times [\frac{1 + \omega_C{}^2 T_2^2}{(1 + \omega_C{}^2 T_1^2)(1 + \omega_C{}^2 T_3^2)}]^{1/2}$$

$$C_2 = C_1 \cdot (\frac{T_2}{T_1} - 1) \text{ and } R_2 = \frac{T_2}{C_2}$$

- The approximation for ωc can be used up to 1/5fref.

Design Example

- As a rule of thumb:

$$C_3 \le \frac{C_1}{10} \text{ and } R_3 > 2R_2$$

- The value of C3 must include the input capacitance of VCO.

$$K_o = 20MHz/v$$
$$I = 5mA$$
$$F_{RF} = 900MHz$$
$$Fref = 200kHz$$
$$N = \frac{F_{RF}}{F_{ref}} = 4500$$
$$\omega_p = 2\pi \cdot 20kHz = 1.256e5$$
$$\phi_P = 45^0$$
$$Atten = 20dB$$

Design Example

$$T_1 = \frac{\sec\phi_P - \tan\phi_p}{\omega_C} = 3.29e^{-6}$$

$$T_3 = \sqrt{\frac{10^{(20/20)} - 1}{(2\pi \cdot 200e^{3})^2}} = 2.387e^{-6}$$

$$\omega_C = \frac{(3.29e^{-6})}{[(3.29e^{-6}+2.387e^{-6})^2+3.29e^{-6}\cdot 2.387e^{-6}]} \times [\sqrt{1+\frac{(3.29e^{-6}+2.387e^{-6})^2+3.29e^{-6}\cdot 2.387e^{-6}}{(3.29e^{-6}+2.387e^{-6})]^2}} - 1]$$

$$\omega_C = 7.045e^{4}$$

$$T_2 = \frac{1}{(7.045e^{4})^2\cdot(3.29e^{-6}+2.387e^{-6})} = 3.549e^{-5}$$

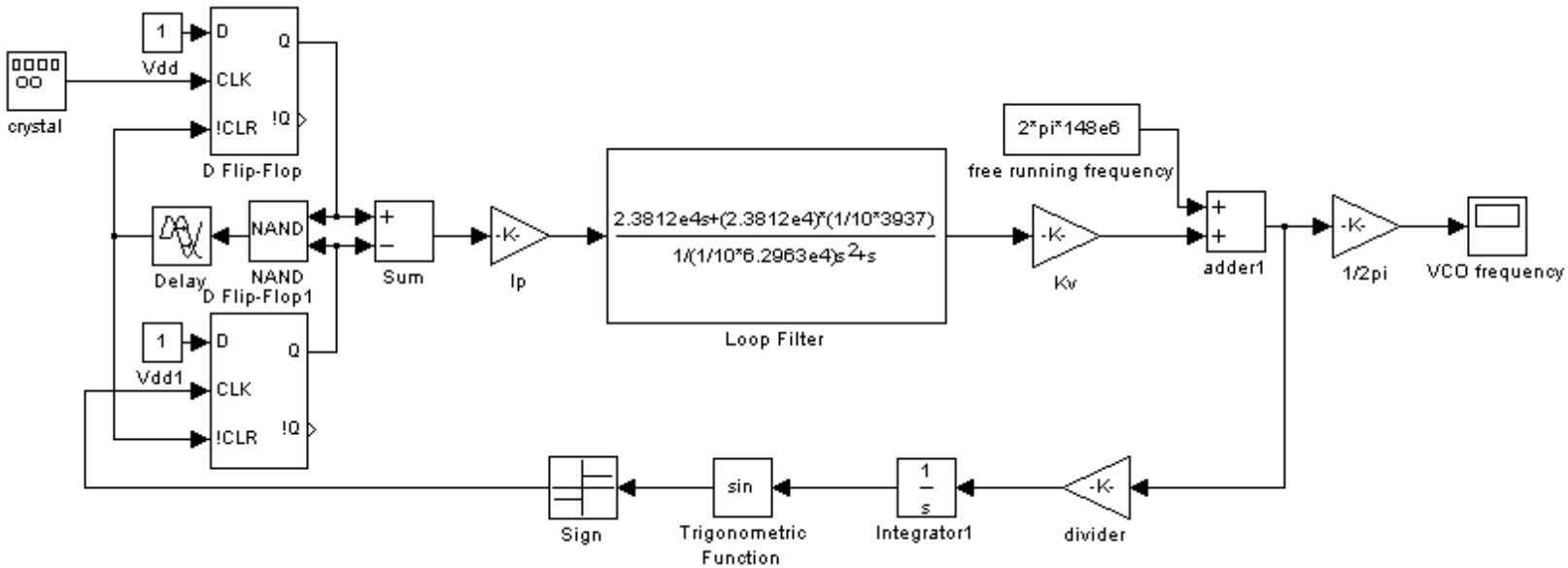
$$C_1 = \frac{3.29e^{-6}}{3.549e^{-5}} \cdot \frac{(5e^{-3})\cdot(20e^{6})}{(7.045e^{4})^2\cdot 4500} \times [\frac{1+(7.045e^{4})^2(3.549e^{-5})^2}{(1+(7.045e^{4})^2(3.29e^{-6})^2)(1+(7.045e^{4})^2(2.387e^{-6})^2)}]^{1/2}$$

$$C_1 = 1.085nF$$

$$C_2 = 10.6nF \text{ and } R_2 = 3.35k\Omega$$

$$\text{If } R_3 = 22k\Omega \text{ then } C_3 = 106pF$$

PLL Behavior Simulation by Simulink



Phase Noise

A typical sinusoidal signal,

$$V_{out}(t) = A(t)\cos(2\pi f_o t + \phi(t))$$

Neglecting amplitude noise,

$$V_{out}(t) = \sqrt{2P}\cos(2\pi f_o t + \phi(t))$$

the instantaneous frquency for $V_{out}(t)$,

$$f(t) = f_o + \frac{d\phi(t)}{dt} \equiv f_o + \Delta f$$

For $|\Delta f| << f_o$, *the power spectrum* $S_{\Delta f} = f^2 S_\phi$

Phase Noise

If $\phi(t) << 1$ *radian, based on the narrowband FM approximation*,

$$V_{out}(t) = \sqrt{2p}\cos(2\pi f_o t + \phi(t))$$

$$\simeq \sqrt{2P}\cos(2\pi f_o t) - \sqrt{2P}\,\phi(t)\sin(2\pi f_o t)$$

The approximated RF spectrum is

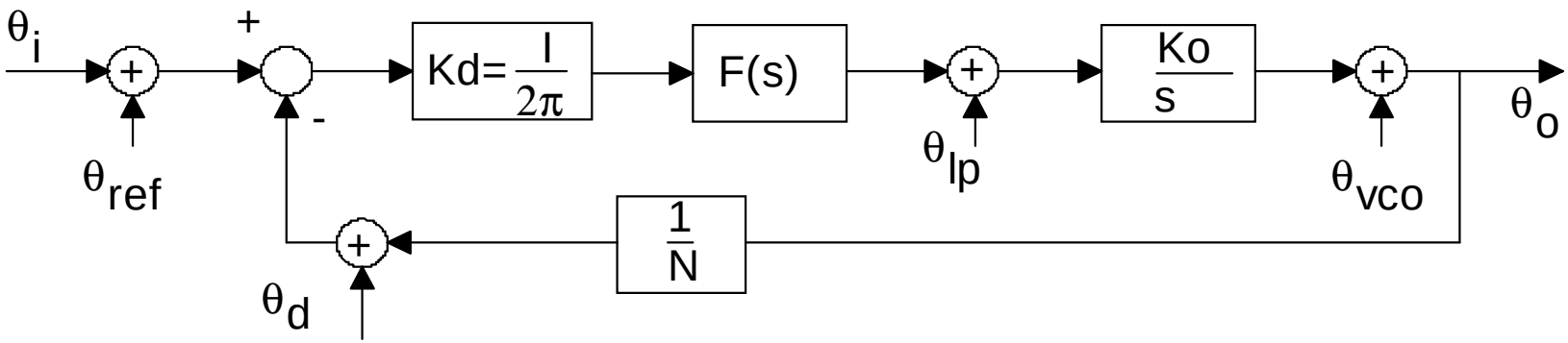
$$S_V(f) \approx \frac{2P}{4}\{\delta(f-f_o) + S_\phi(f-f_o) + \delta(f+f_o) + S_\phi(f+f_o)\}$$

The Single-Sideband Phase Noise Referenced to Carrier, ***L***(f)

$$L(f) \equiv \frac{\int_{f_o+f-\frac{1}{2}}^{f_o+f+\frac{1}{2}} S_V(f')df'}{Carrier\ Power}$$

$$L(f) \approx \frac{1}{2}S_\phi(f)$$

Noise Response



$$\frac{\theta_o}{\theta_{ref}} = \frac{\theta_o}{\theta_d} = \frac{NG(s)}{1+G(s)}$$ Lowpass

$$\frac{\theta_o}{\theta_{lp}} = \frac{NK_o/s}{1+G(s)}$$ Bandpass

$$\frac{\theta_o}{\theta_{vco}} = \frac{N}{1+G(s)}$$ Highpass

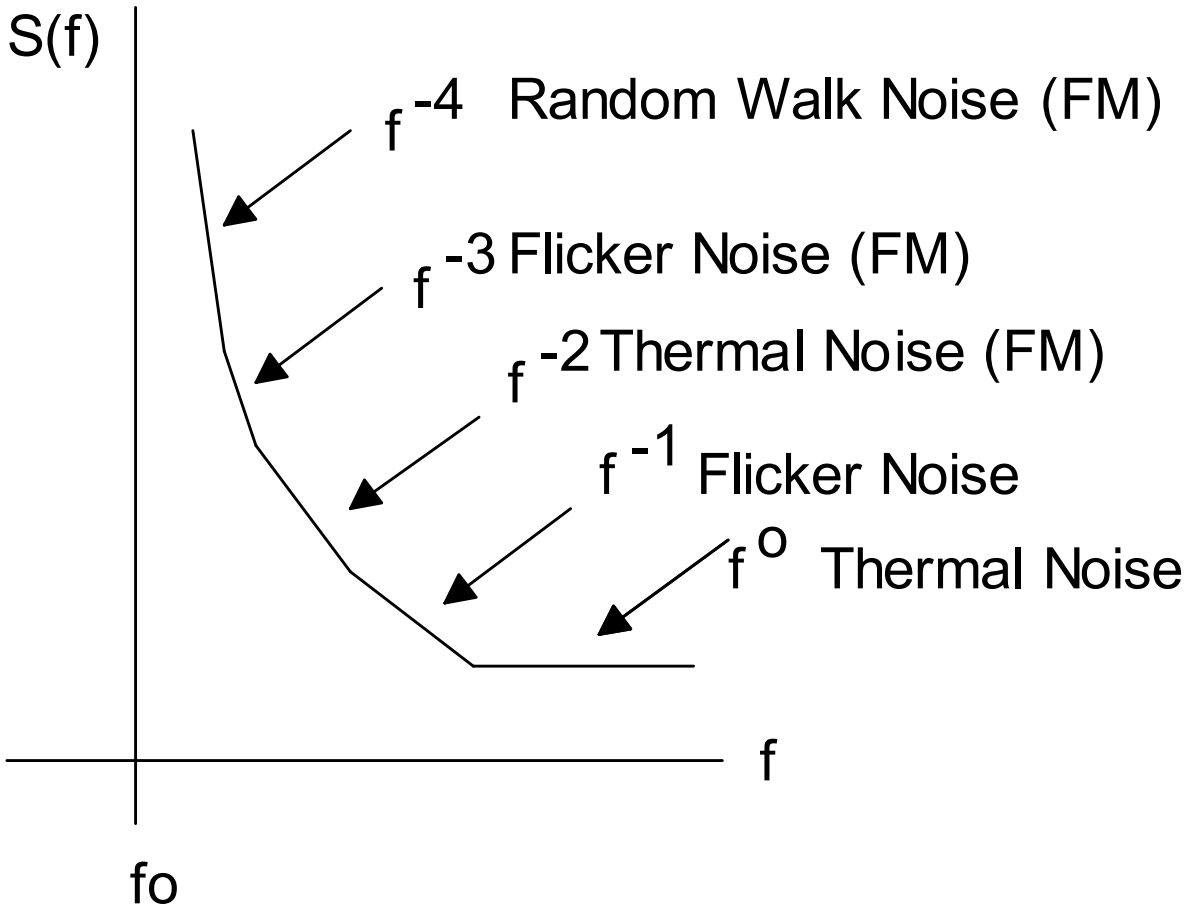
Noise Response

$$S_{\phi}(f) = S_{ref}(f)N^2\left|\frac{G(s)}{1+G(s)}\right|^2 + S_{lp}(f)N^2\left|\frac{K_o/s}{1+G(s)}\right|^2 +$$

$$S_{vco}(f)N^2\left|\frac{1}{1+G(s)}\right|^2 + S_d(f)N^2\left|\frac{G(s)}{1+G(s)}\right|^2, s = j2\pi f$$

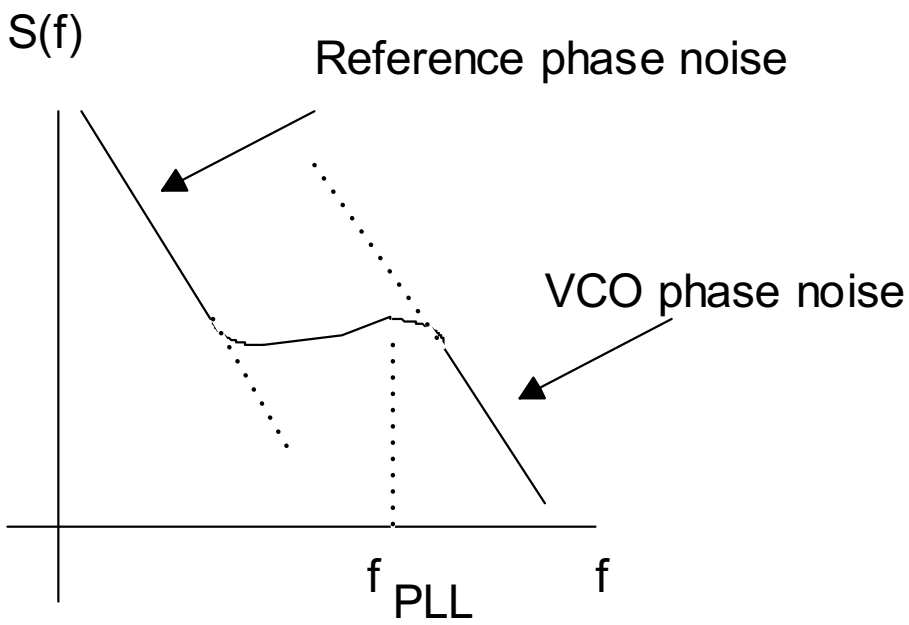
- The power spectrums are multiplied by divider's ratio, N.
- The crystal reference and counter are the only significant contributors in the bandwidth of the PLL.
- At offset frequency greater than the PLL BW, the VCO's phase noise is dominant.

Typical VCO Phase Noise



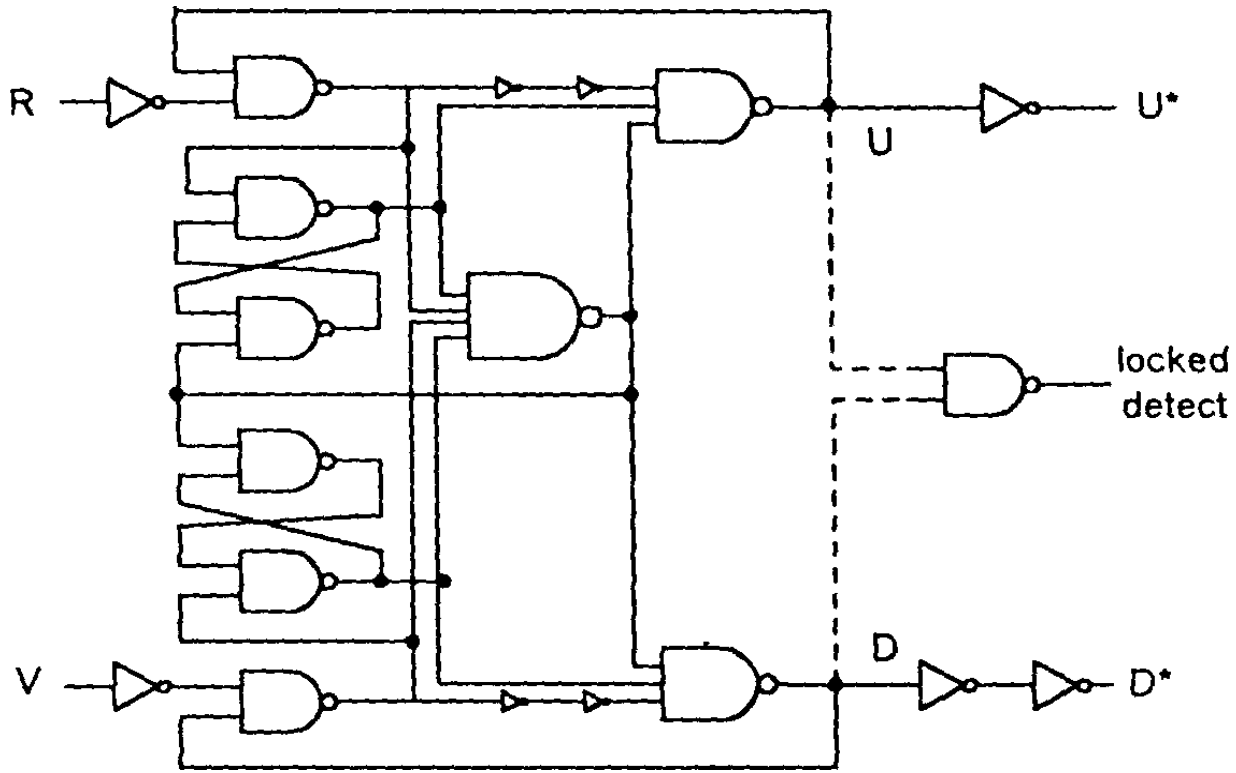
IEEE JSSC-33, pp.179-,Feb. 1998. & IEEE JSSC-33,pp.828,June 1998.

Typical PLL Phase Noise



f_{PLL} is the opened-loop unity-gain bandwidth(~ωc)

Phase Frequency Detector

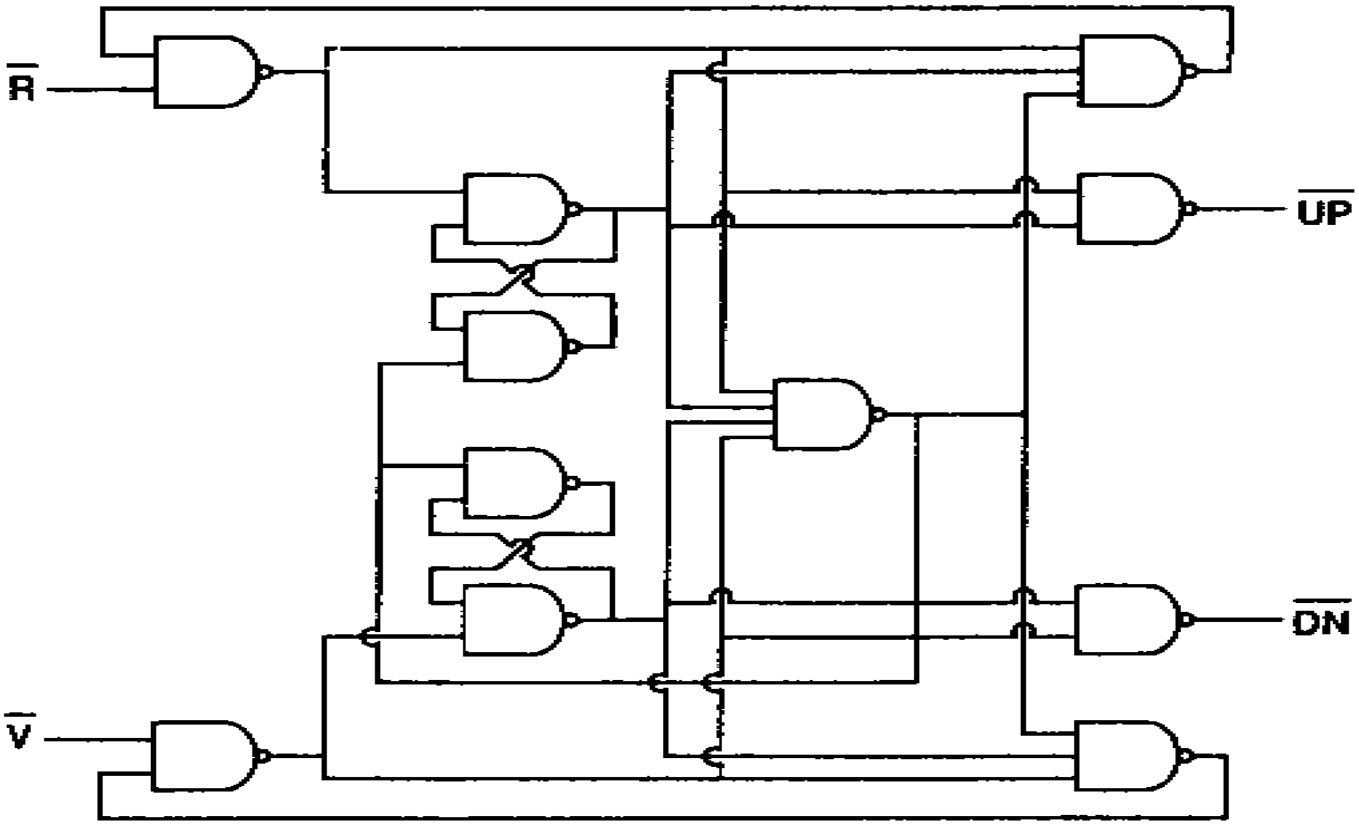


To reduce the dead zone, the delay can be inserted at the output of the 4-input NAND.

Increasing the delay will reduce the maximal frequency of the PFD.

IEEE JSSC-25, pp.1019-,Aug. 1990

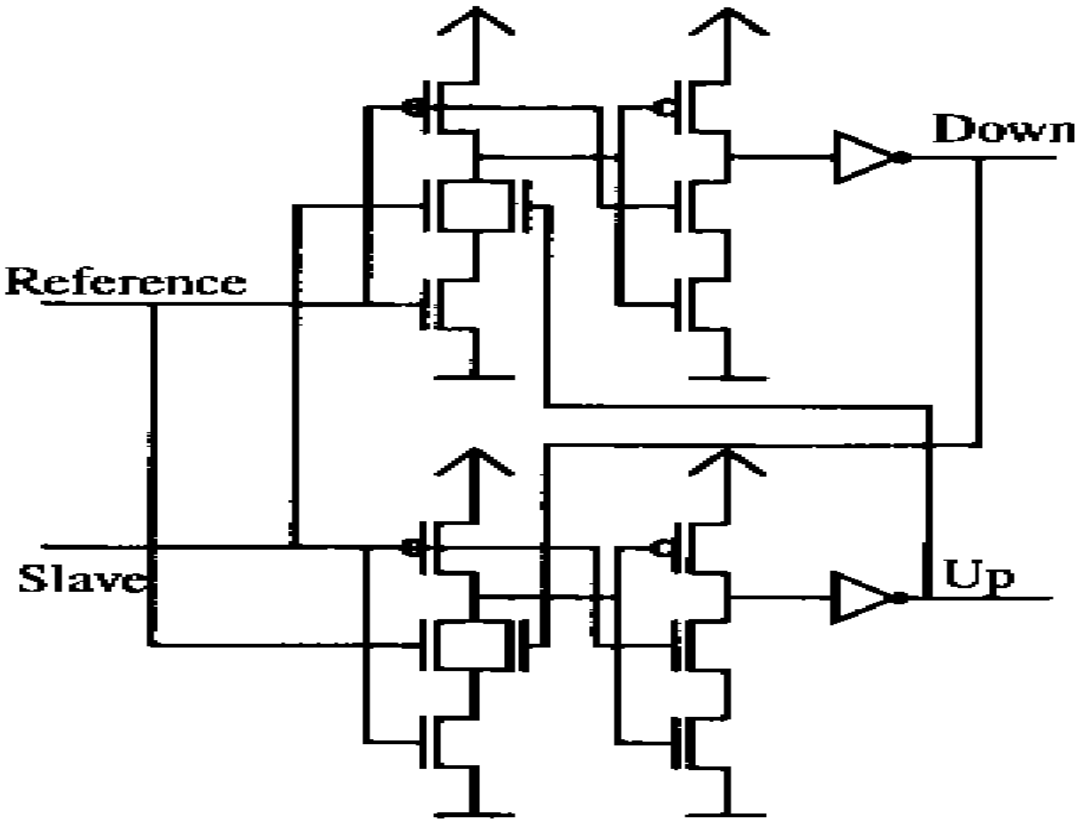
Phase Frequency Detector



Phase-frequency comparator with equal short duration output pulses for in-phase inputs.

IEEE JSSC, SC-31, pp. 1723-, Nov. 1996.

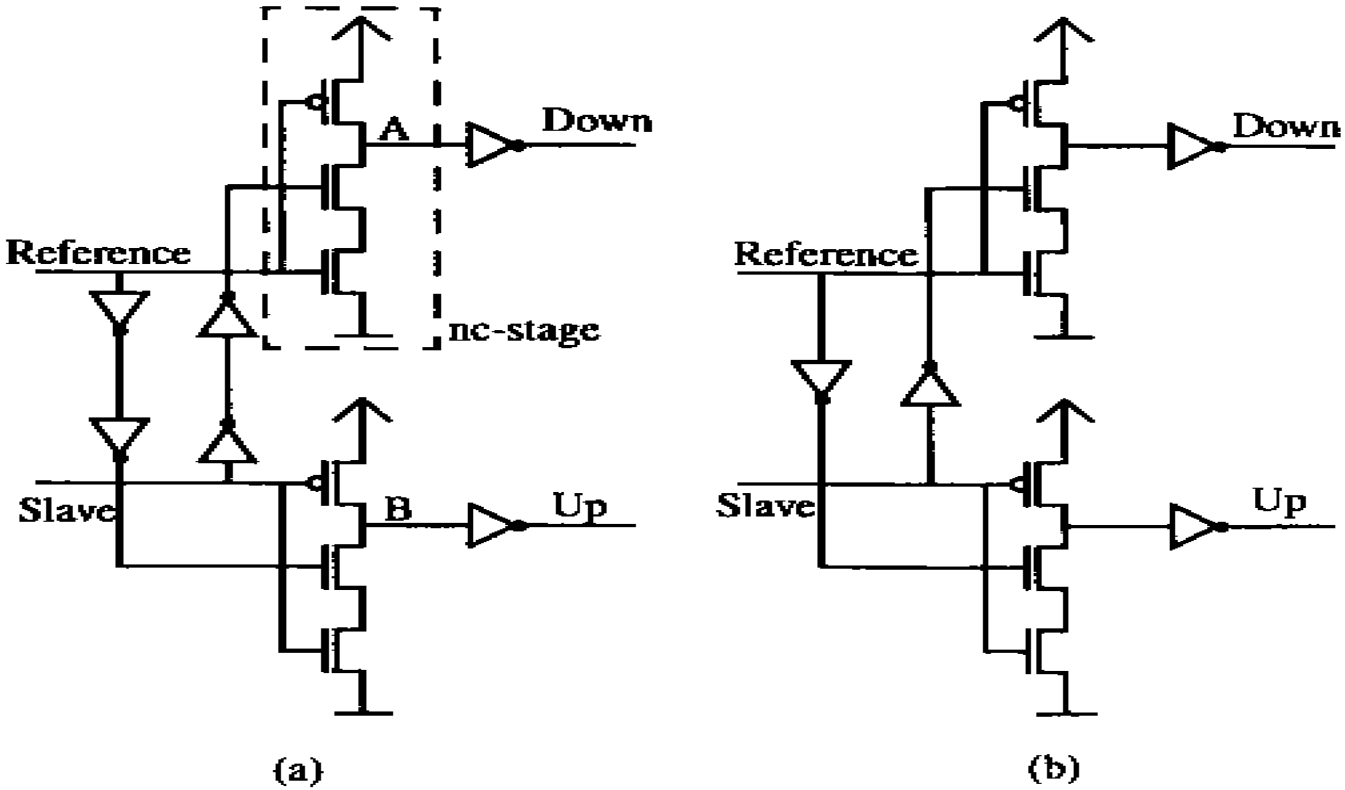
Phase Frequency Detector



Precharge type phase frequency detector (ptPFD)

IEICE Trans. Electronics, E78-C, pp.381-,April 1995.

Phase Frequency Detector

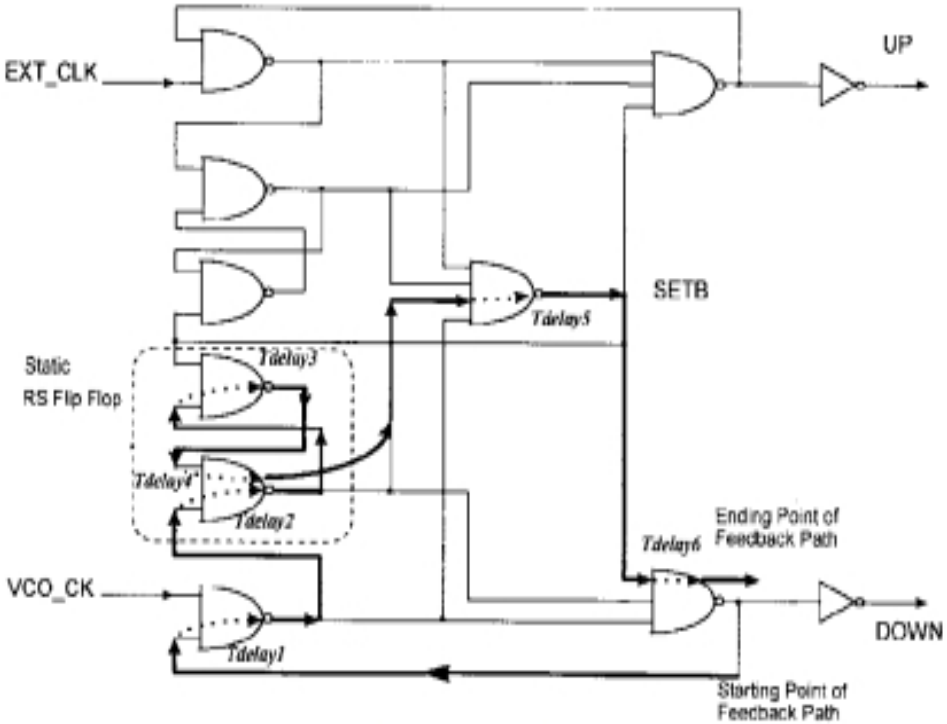


(a) The ncPFD in zero degree phase offset version. (b) Modified version with π rad phase offset.

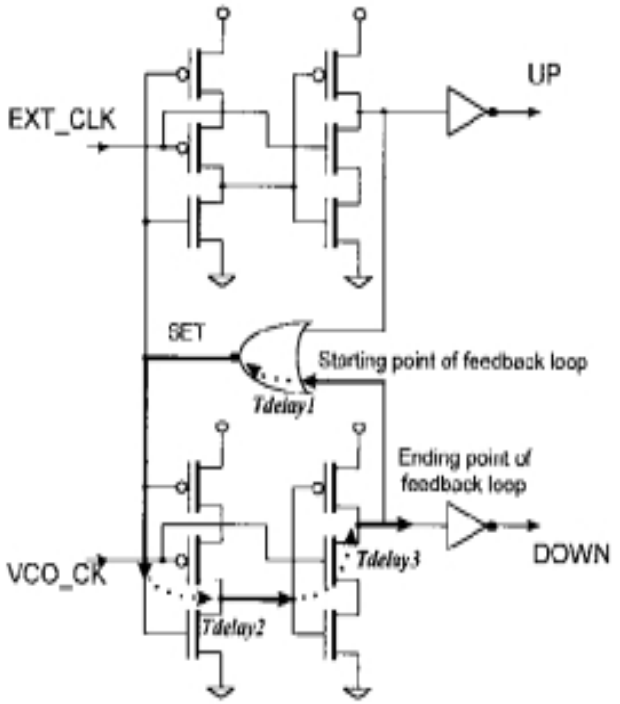
IEEE JSSC, SC-33, pp. 295-, Feb. 1998.

*50% duty required

Phase Frequency Detector



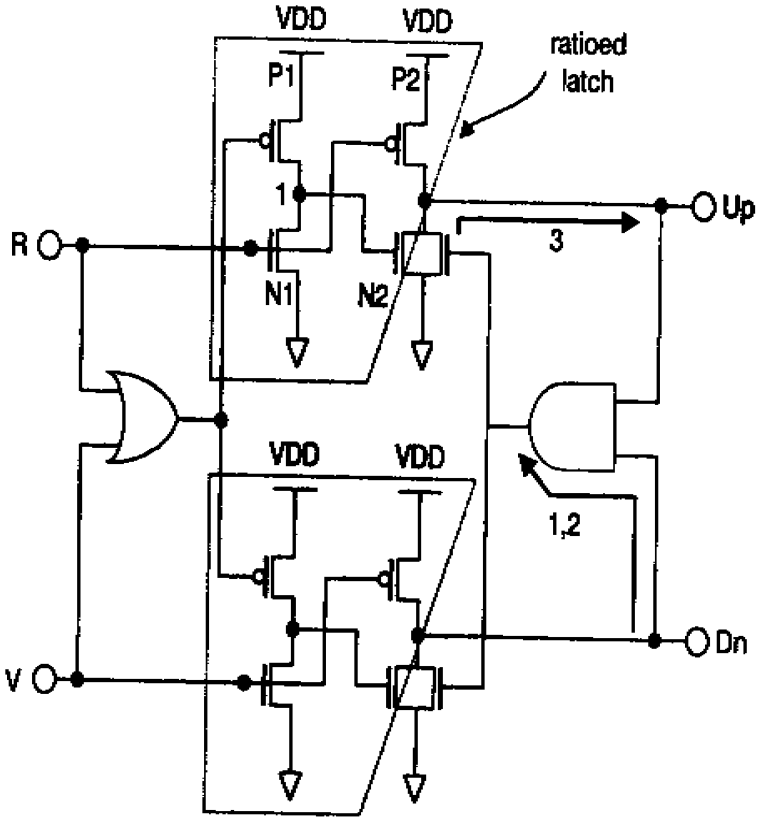
Conventional phase frequency detector.



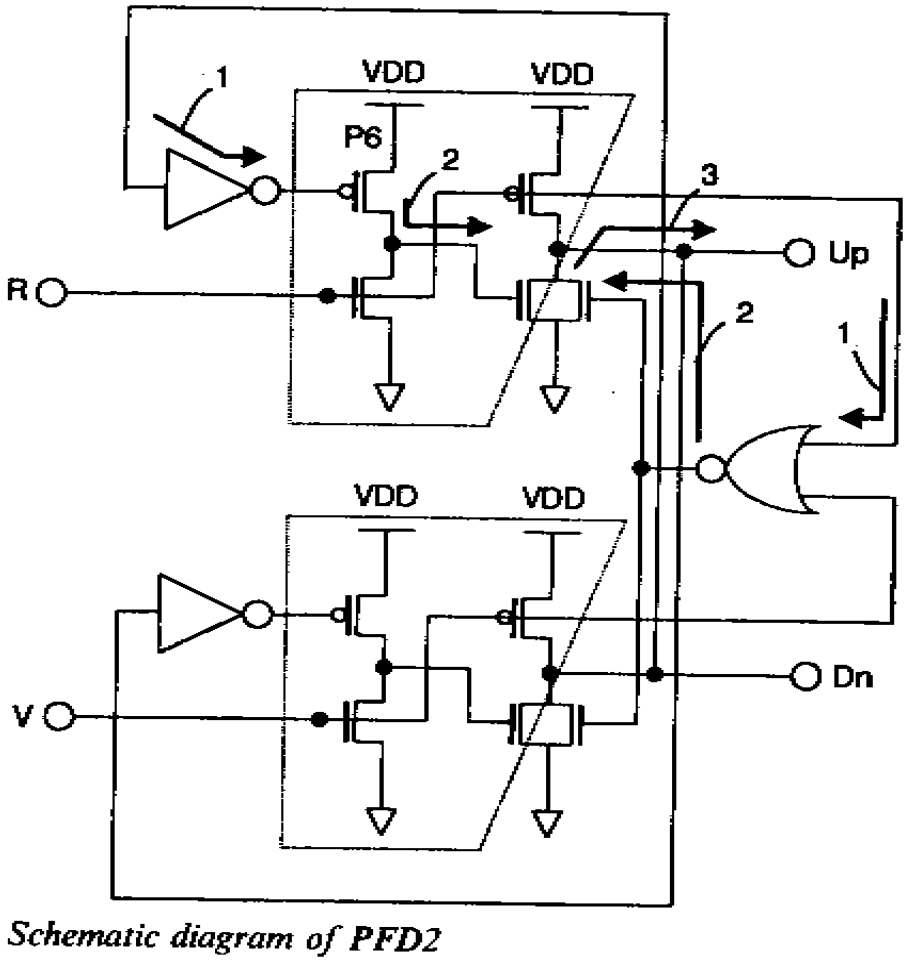
Implemented phase frequency detector.

IEEE JSSC, SC-32, pp. 691-, May 1997.

Phase Frequency Detector



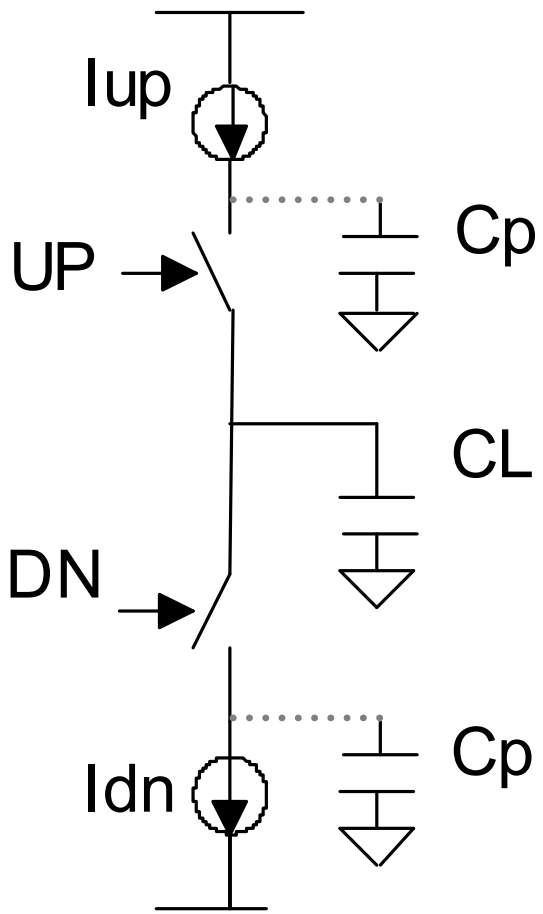
Schematic diagram of PFD1



Schematic diagram of PFD2

IEE E.L., Vol.-34, pp.2121-, Oct. 1998.

Current-Pump Circuit



Problems:

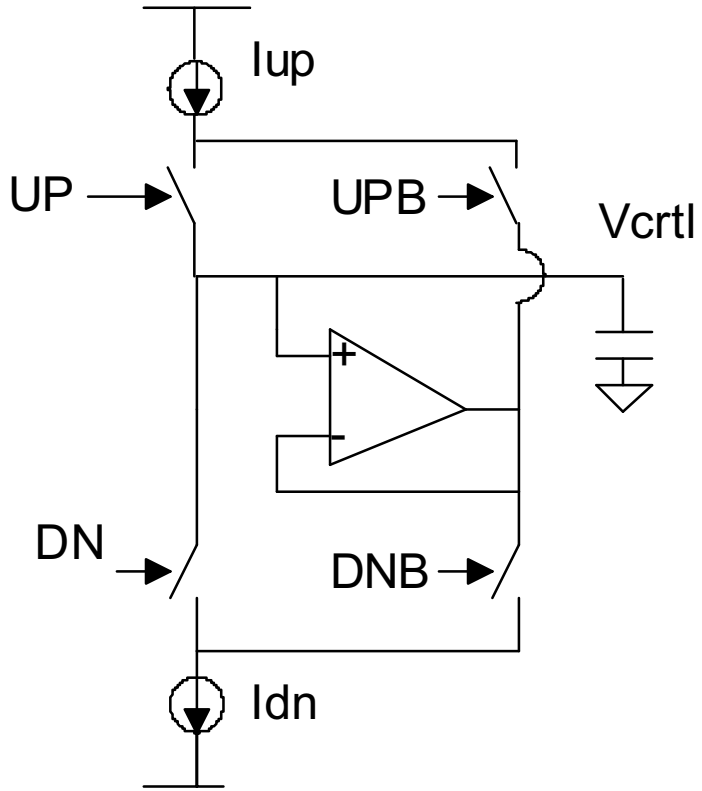
1. Charge Sharing
2. Charge Injection

$\Delta Qcp=Cp\Delta V=50fF*500mV$

$\Delta Q=I*\Delta t=10uA*\Delta t$

Δt=2.5ns static phase offset for PFD's input

Current-Pump Circuit



Problems:

1. Offset of OP AMP
2. Equal delay for UP and DN

IEEE JSSC, SC-27, pp. 1599-, Nov. 1992.

Current-Pump Circuit

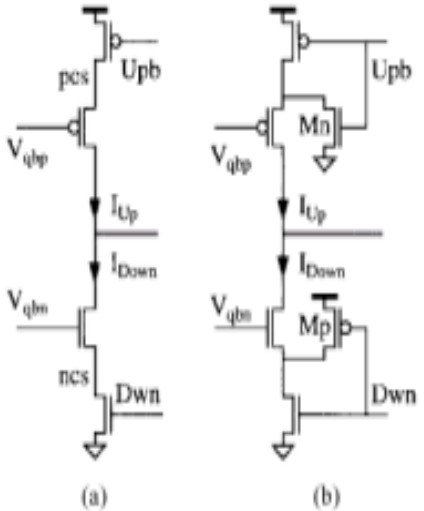


Fig. 9. (a) Charge-pump suffering from charge sharing (Type A). (b) Charge removal transistors eliminate charge sharing (Type B).

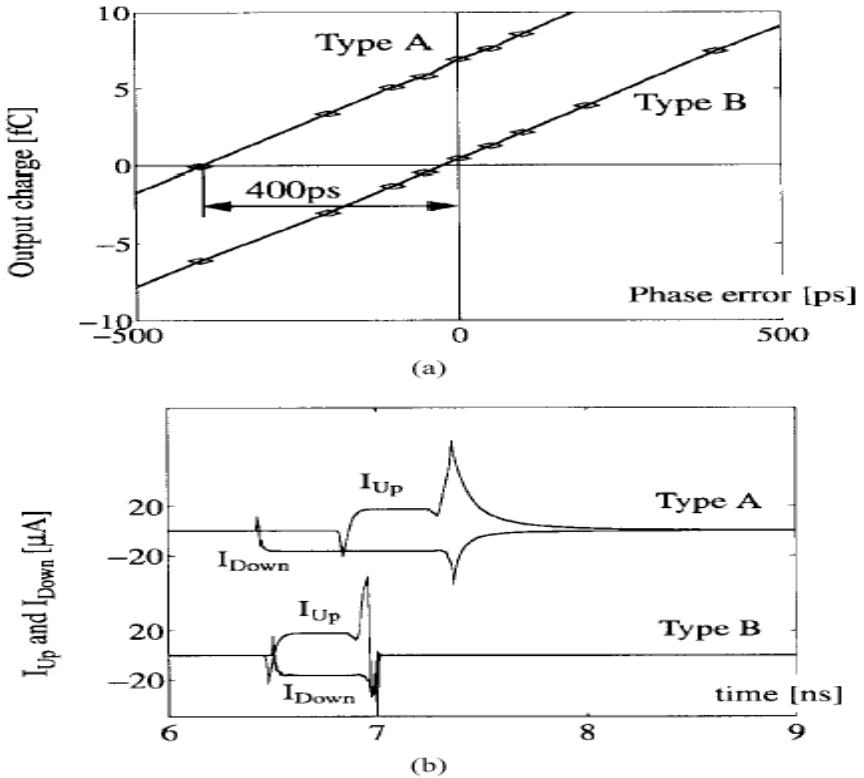


Fig. 10. Characteristics of the Type A and B charge pumps. (a) Transfer function of PFD followed by charge pump. (b) Simulated I_{Up} and I_{Down} when net output charge is zero.

IEEE JSSC, SC-34, pp. 1951-, Dec. 1999.

Current Pump Circuits

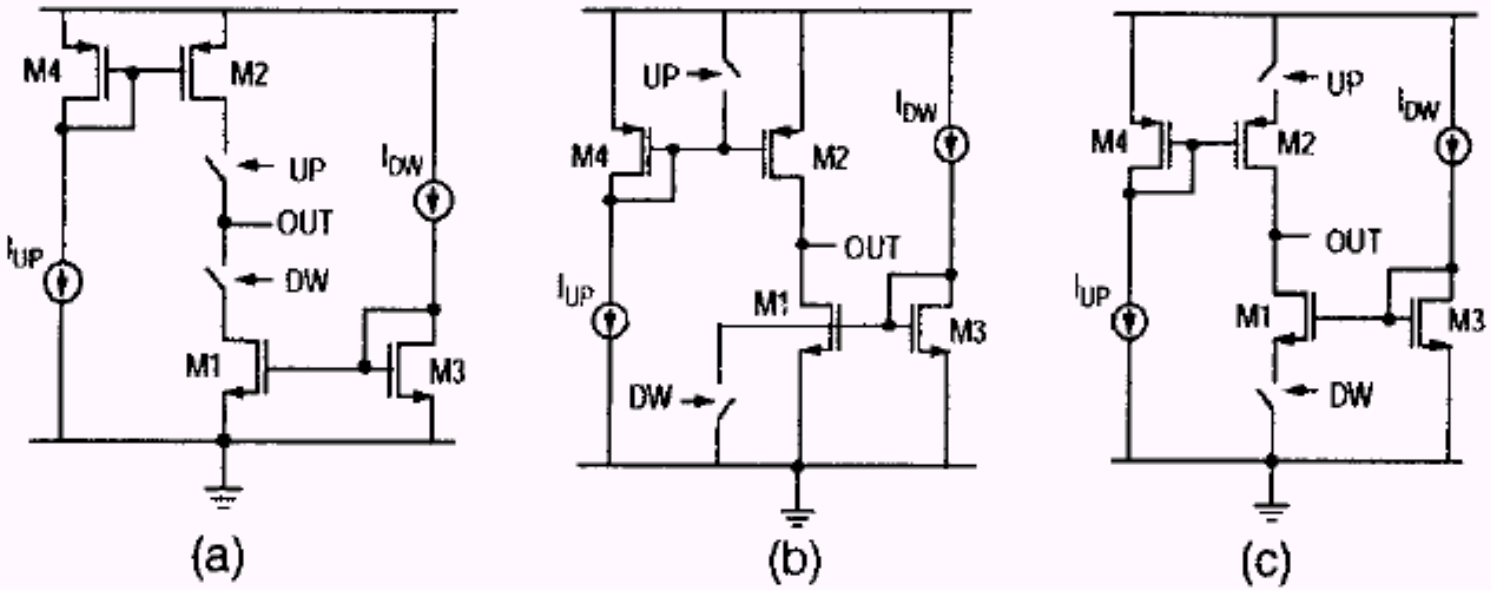


Figure 3. Single-ended charge pumps : (a) switch in drain, (b) switch in gate, and (c) switch in source.

Ref: IEEE ISCAS'99, II-545, 1999

Current Pump Circuits

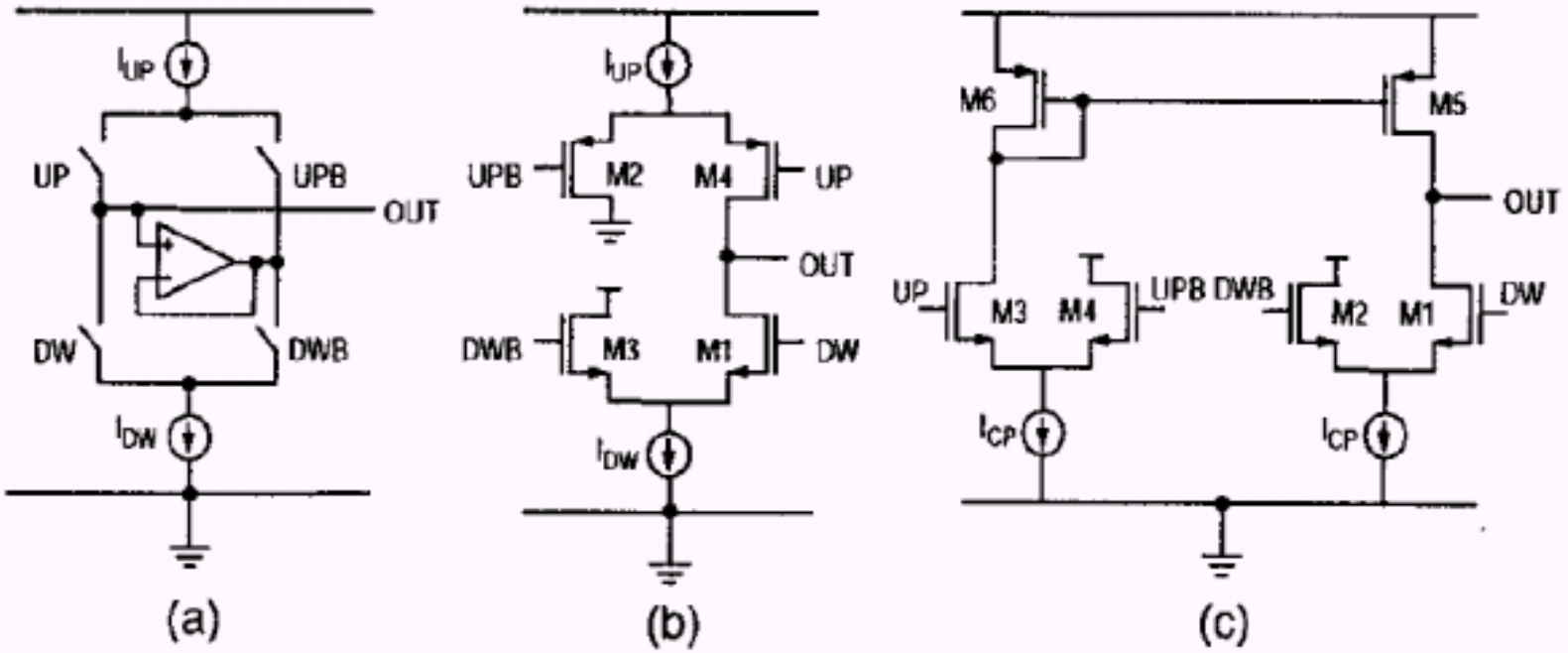


Figure 4. Variations of single-ended charge pumps : (a) with active amplifier, (b) with current steering switch, and (c) with NMOS switches only.

Current Pump Circuits

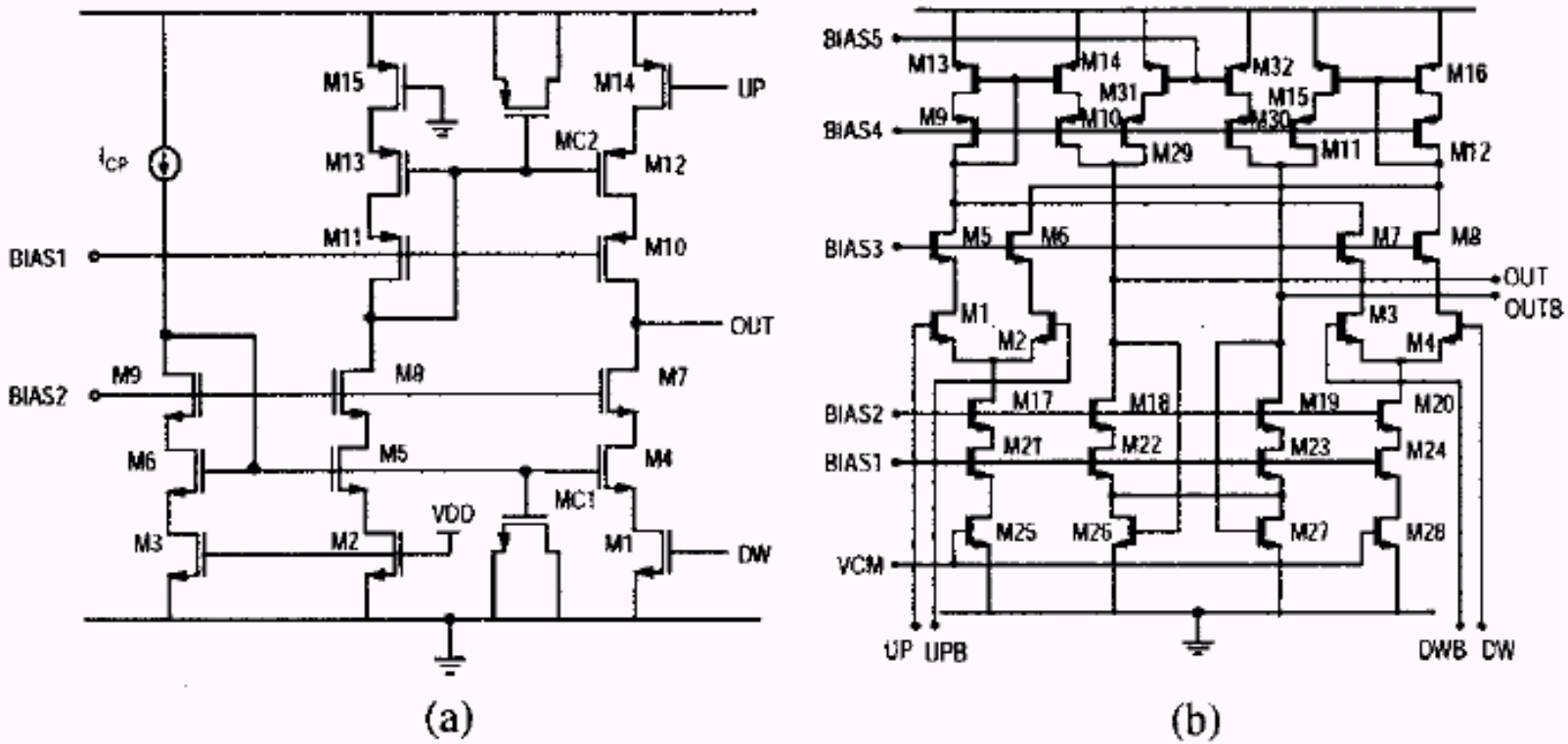
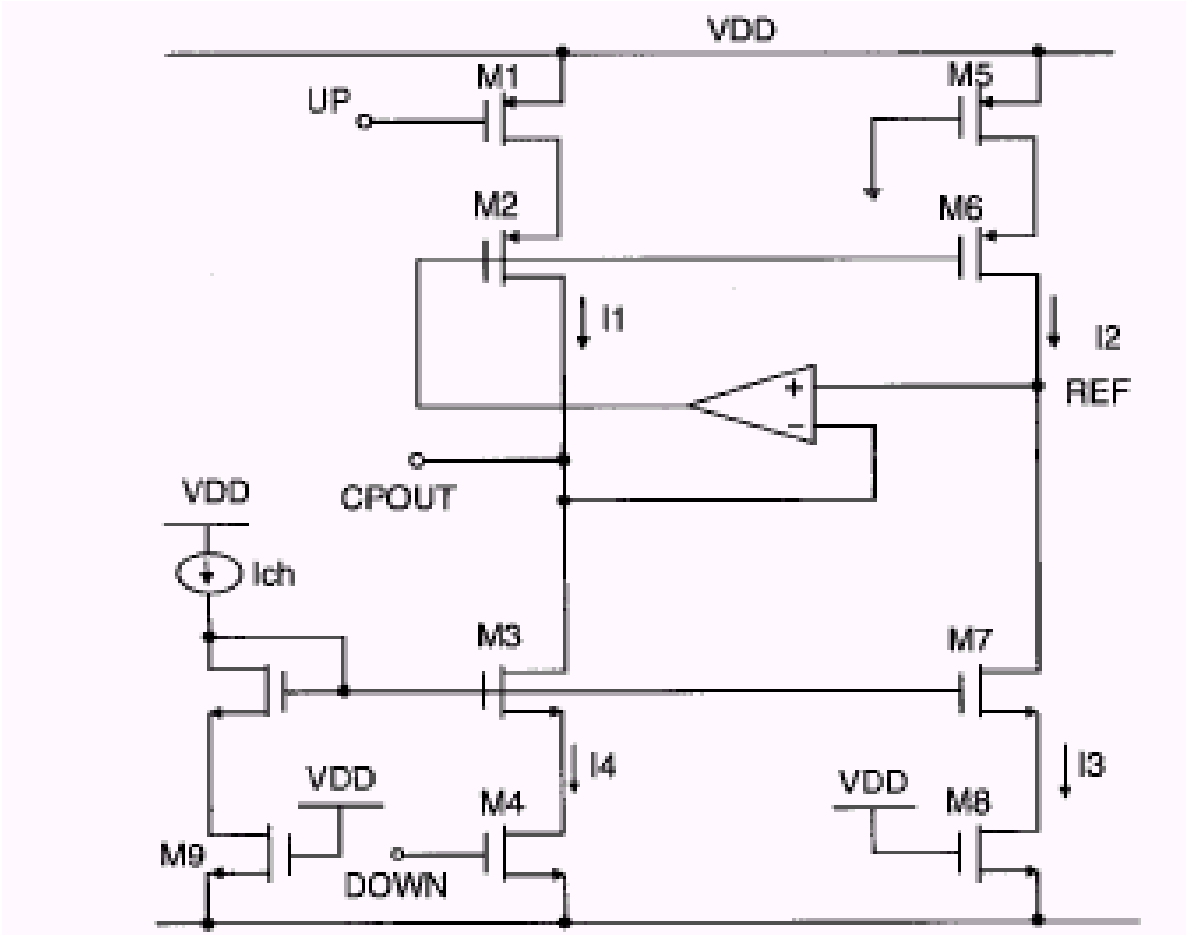


Figure 5. Improved architectures : (a) single-ended, and (b) fully differential.

Current Pump Circuits

- Conventional tri-state - Type 1 (Fig. 3, Fig. 4(a), Fig. 5(a))
  - Low power consumption, moderate speed, moderate clock skew
  - Low power frequency synthesizers, digital clock generators
- Current steering - Type 2 (Fig. 4(b))
  - Static current consumption, high speed, moderate clock skew
  - High speed PLL (f_{ref} > 100MHz), translation loop, digital clock generators
- Differential input with single-ended output - Type 3 (Fig. 4(c))
  - Medium power, moderate speed, low clock skew
  - Low-skew digital clock generators, frequency synthesizers
- Fully differential - Type 4 (Fig. 5(b))
  - Static current consumption, high speed (f_{ref} > 100MHz), high linearity, low clock skew, immune to leakage current, immune to supply/ground noise
  - High-speed fully monolithic PLLs (f_{ref} > 100MHz) - digital clock generators, translation loop, frequency synthesizer (with on-chip loop filter)

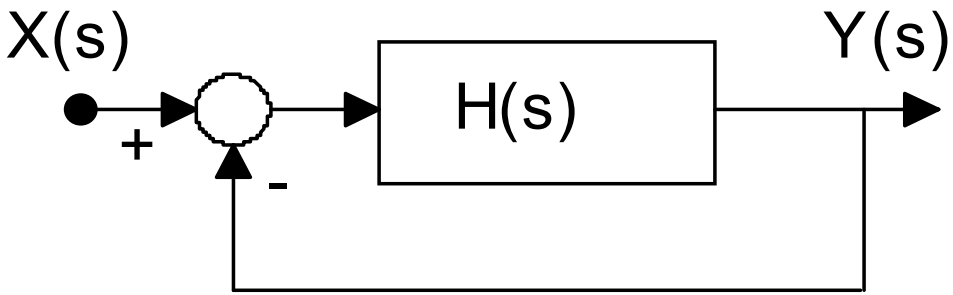
Current Pump Circuits



Ref: IEE EL, pp. 1907-, 2000

Oscillator

Small-Signal Model

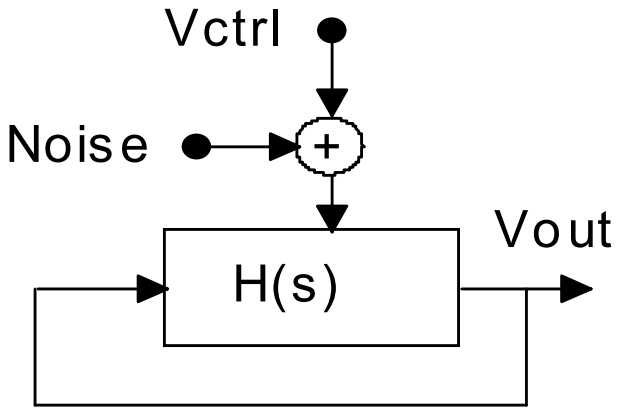


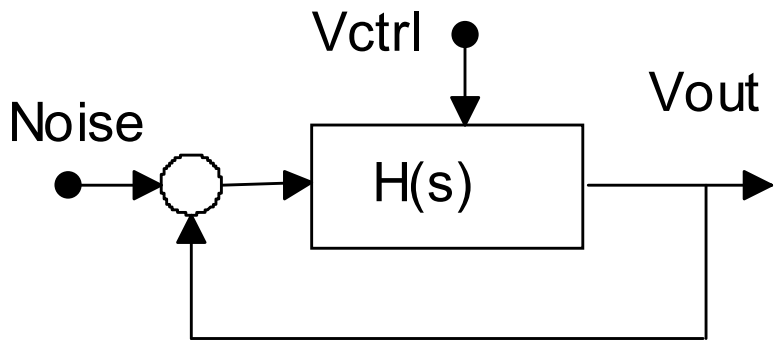
$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1+H(s)}$$

Conditions of Oscillation

* Unity-gain at fo
*Zero Total Phase Shift at fo

Basic Noise Mechanism





Noise in Signal Path

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1-H(s)}$$

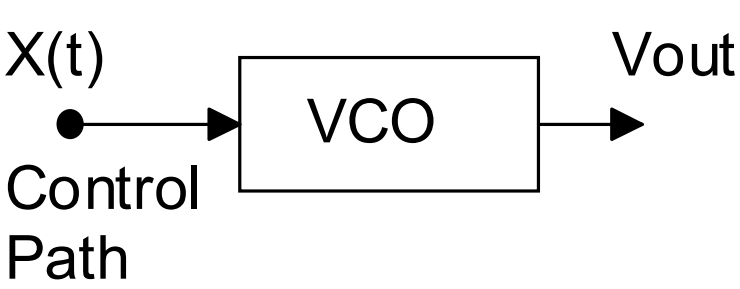
$$\frac{Y}{X}(\omega_o + \Delta\omega) \approx \frac{-1}{\Delta\omega \dfrac{dH(\omega)}{d\omega}} \qquad \text{where } H(\omega) = |H| \exp(j\phi)$$

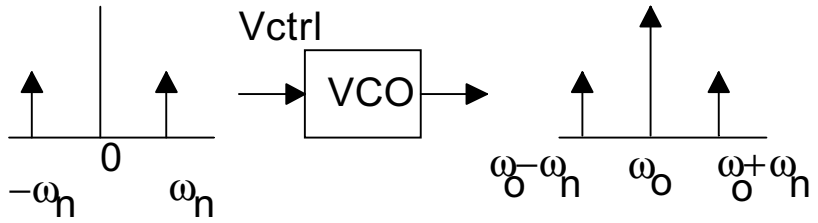
$$\left| \frac{Y}{X}(\omega_o + \Delta\omega) \right|^2 \approx \frac{1}{(\Delta\omega)^2 \left| \dfrac{dH(\omega)}{d\omega} \right|^2} = \frac{1}{(\Delta\omega)^2 \left(\left| \dfrac{d|H|}{d\omega} \right|^2 + \left| \dfrac{d\phi}{d\omega} \right|^2 |H|^2 \right)}$$

$$\left| \frac{Y}{X}(\omega_o + \Delta\omega) \right|^2 \approx \frac{1}{(\Delta\omega)^2 \left| \dfrac{d\phi}{d\omega} \right|^2}$$

For a LC tank osc., $Q = \dfrac{\omega_o}{2} \dfrac{d\phi}{d\omega} \rightarrow\rightarrow\rightarrow \left| \dfrac{Y}{X}(\omega_o + \Delta\omega) \right|^2 \approx \dfrac{1}{4Q^2} \left(\dfrac{\omega_o}{\Delta\omega} \right)^2$

Noise in Control Path





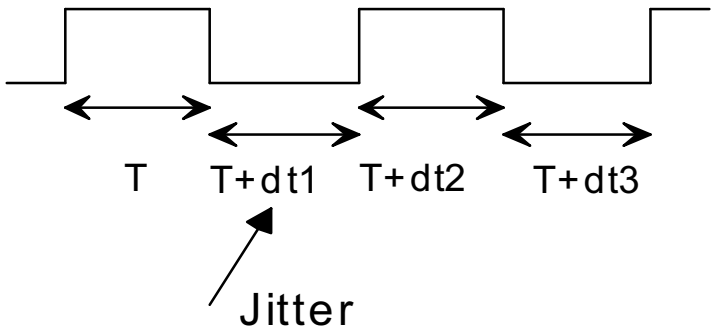
For sinusoidal disturbance:

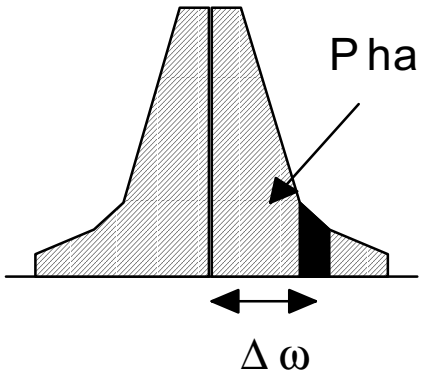
$$V_{out}(t) = A_o \cos(\omega_o t + K_V \int A_m \cos \omega_m t dt)$$

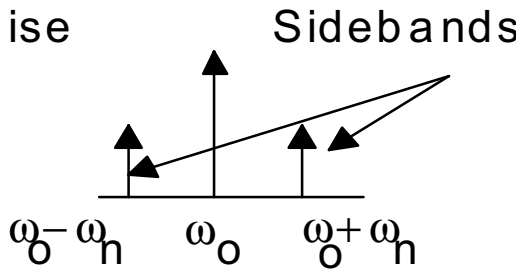
$$\simeq A_o \cos \omega_o t + \frac{A_o A_m K_V}{2\omega_m}[\cos(\omega_o + \omega_m)t - \cos(\omega_o - \omega_m)t]$$

- Mechanism is similar to FM
- Upconverts noise spectrum from LF to the band around carrier
- Flicker noise is important
- All the sources of FM should be considered

Jitter, Phase Noise, and Sidebands





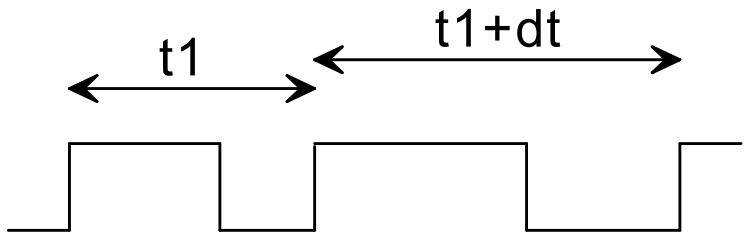


- Jitter may result from phase noise or sidebands
- Random jitter and phase noise originate from:
  - Supply and substrate noise
  - Device noise (e.g. Flicker and Thermal noise)
- Sidebands usually result from periodic disturbance of control path

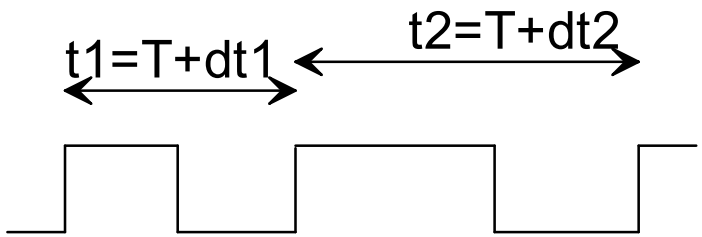
Types of Jitter

Long-Term Jitter: the maximum change in a clock's output transition from its ideal position over many cycles

Cycle-to-Cycle Jitter



Period (Cycle) Jitter



Sources of Jitter

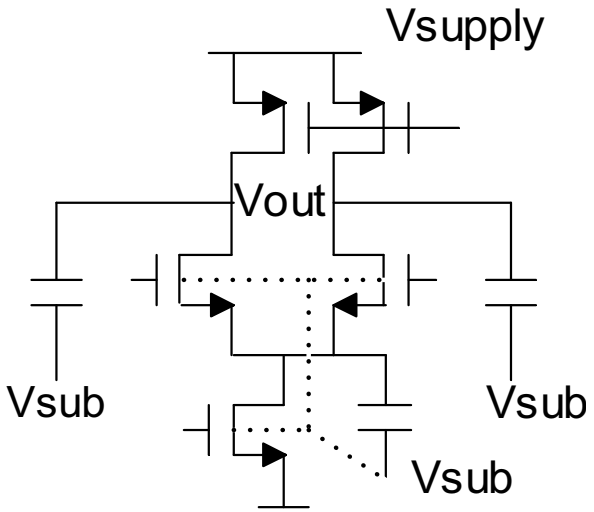
1. Device Noise (Thermal, Flicker)

- Flicker noise varies the oscillation frequency slowly;It can be suppressed by the wide-BW of PLLs.
- Thermal noise generates" white frequency noise".

Relationship between phase noise and cycle-to-cycle jitter

$$\Delta T_{CC}^2 \approx \frac{2\pi}{\omega_o^3} S_\phi(\omega)(\omega - \omega_o)^2$$

Sources of Jitter



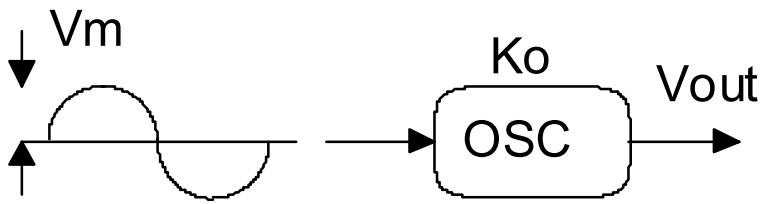
2. Supply Noise

- Supply and substrate noise varies voltage-dependent capacitances.==> modulating the oscillation frequency
- Can view the circuit as a VCO with the supply or substrate acting as control line.

3. Substrate Noise

- Vth modulation

Jitter Due to Supply Noise



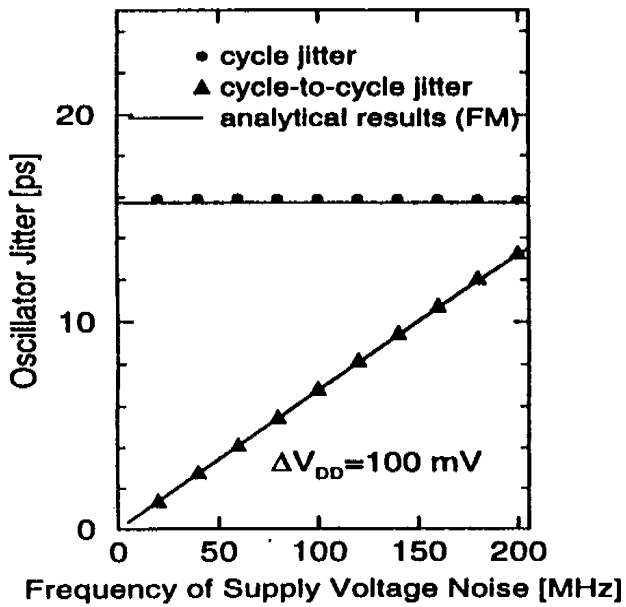
$$\Delta V_m = V_m \cos \omega_m t \rightarrow \Delta f_o = V_m K_o \cos \omega_m t$$

$$\textit{Cycle jitter} : \Delta T(t) = \frac{1}{f_o + \Delta f_o} - \frac{1}{f_o} \approx \frac{-V_m K_o}{f_o^2} \cos \omega_m t$$

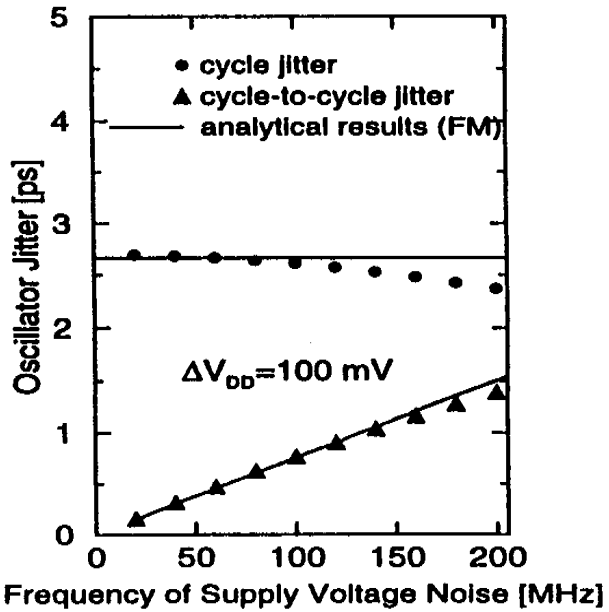
$$\textit{Cycle} - \textit{cycle jitter} : \Delta T_{CC} = \frac{V_m K_o}{f_o^2} \sqrt{1 - \cos(\omega_m / f_o)} \approx \frac{V_m K_o \omega_m}{\sqrt{2}\, f_o^3}$$

Simulation Results

Single–Ended Ring



Differential Ring



Jitter Due to Supply Noise

- Supply noise sensitivities can be minimized by isolating the delay elements from supply.
  - Use buffered control voltage as supply voltage
  - Use buffered control voltage to generate a bias current

  ==> Current source isolation

- Simple Current Source ==>5%/V sensitivity
- Cascode Current Source ==>0.5%/V sensitivity (2Vds needed)
- Replica current source ==> 0.5%/V sensitivity

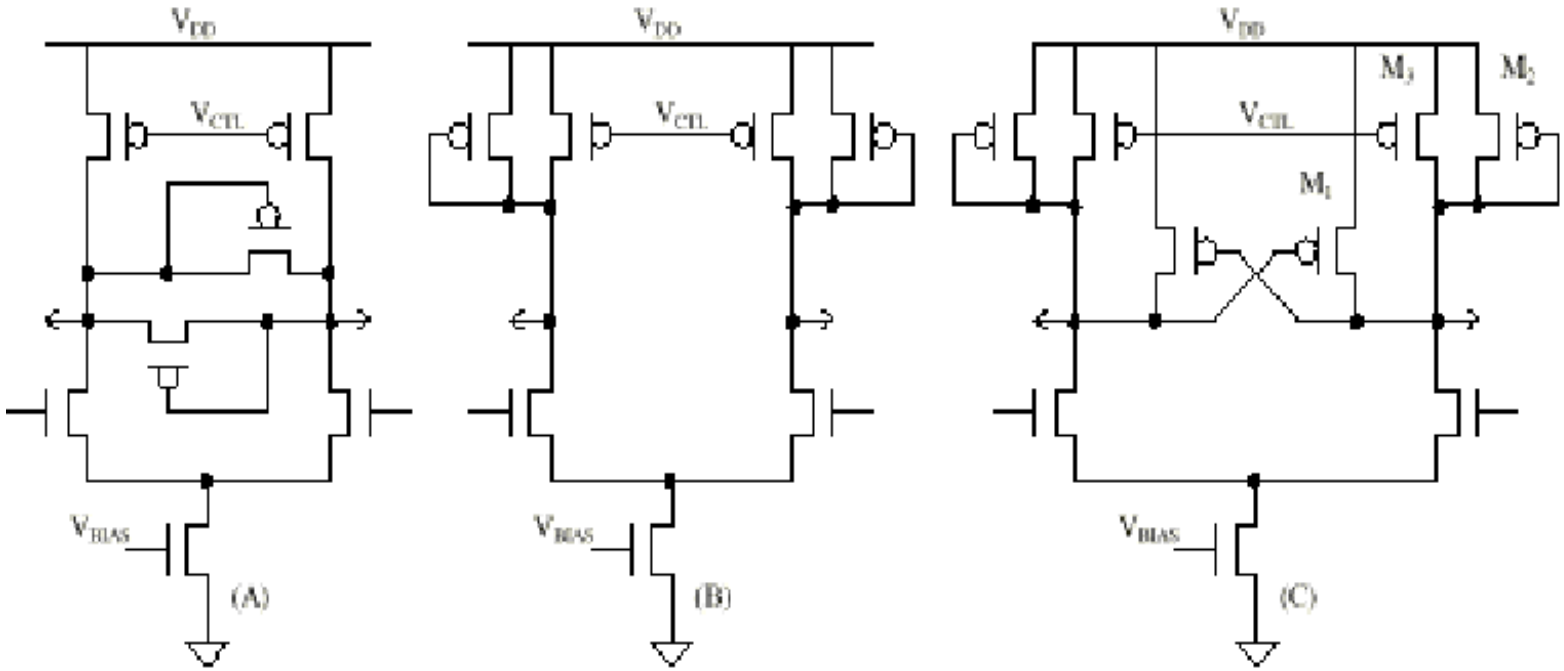
Jitter Due to Substrate Noise

- Substrate noise sensitivities can be minimized by
  - Using well-type devices for current sources
  - Using well-type devices for loop filter capacitor
  - Using well-tap voltage as control voltage reference
  - Only connecting control voltage to well-type devices
  - Don’t connect control voltage to pad directly

Voltage-Controlled Oscillators

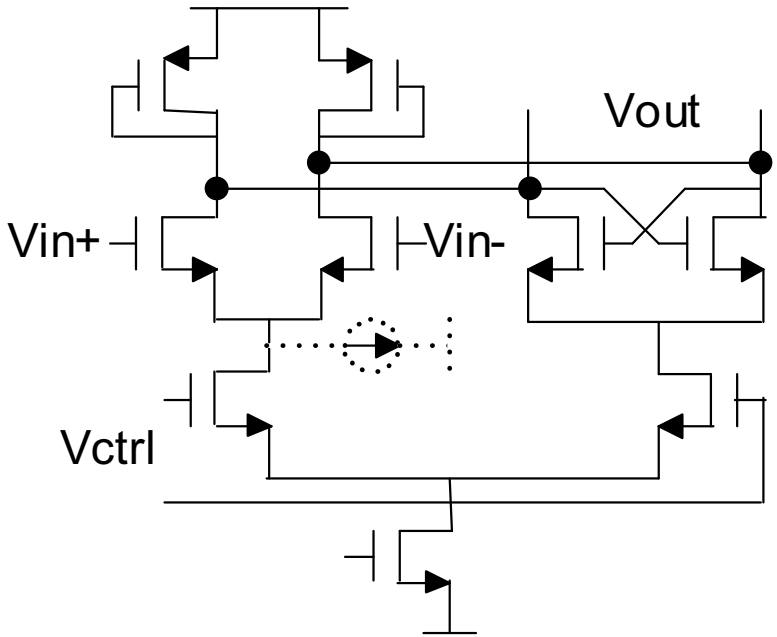
1. Ring Oscillators
2. Multivibrators
3. LC tank Oscillators

Variable Delay Elements

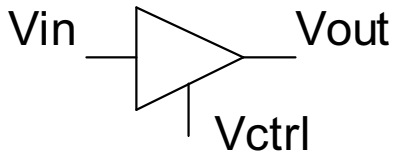


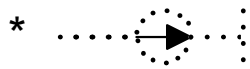
(a) Clamped-load (b) Symmetric-load (c) Cross-coupled-load

Variable Delay Using Local Feedback



Direct Delay Variation

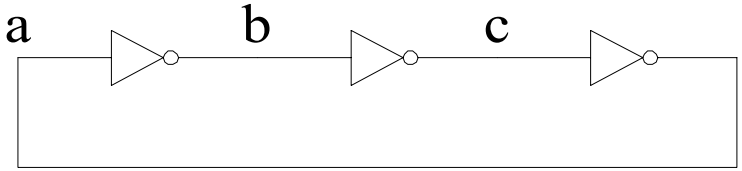


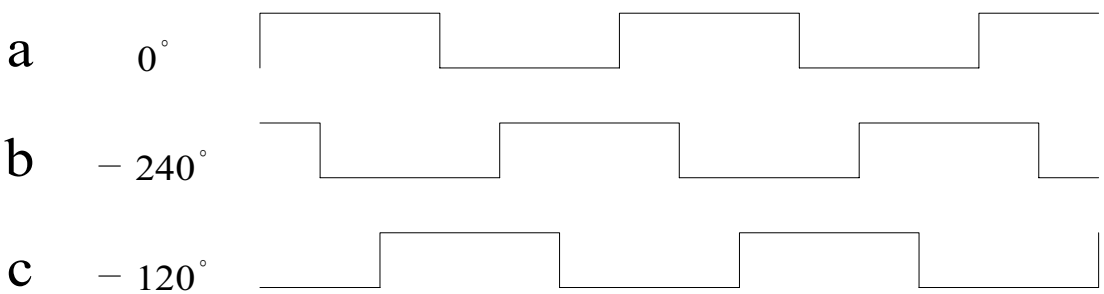


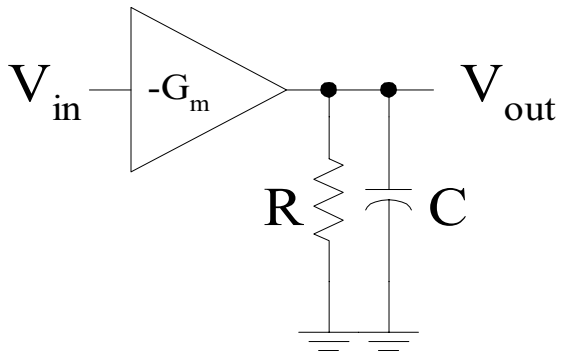
* Supply volatge lim.

Monolithic PLLs and Clock Recovery Circuits, IEEE Press, pp. 1, 1996

Ring Oscillator







$$H(s)=\frac{V_{out}}{V_{in}}=\frac{-G_mR}{1+sRC}=\frac{-A}{1+s/\omega_p}$$

$$A=G_mR \qquad \omega_p=1/RC$$

Ring Oscillator

$$H(S) = \frac{A}{1 + S/\omega_p}$$

$$\angle H(\omega_0) = -\pi - \tan^{-1}\frac{\omega_0}{\omega_p} = -\pi - \frac{\pi}{N}$$

$$\tan^{-1}\frac{\omega_0}{\omega_p} = \frac{\pi}{N}$$

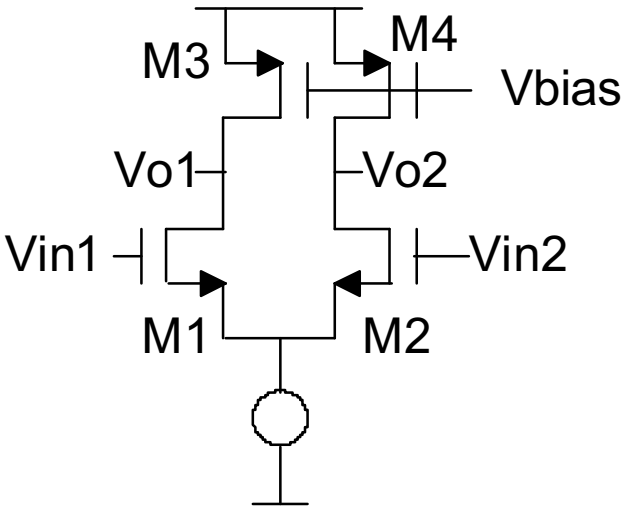
$$\omega_0 = \omega_p \tan\frac{\pi}{N}$$

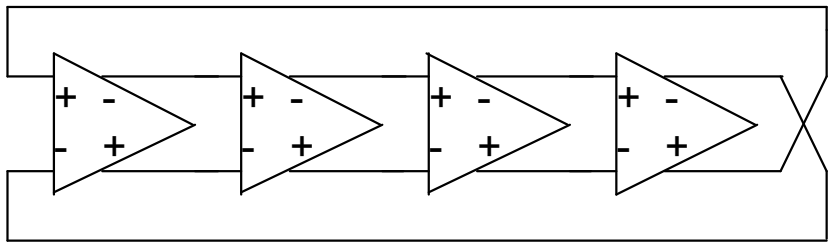
$$|H(\omega_0)| = \left|\frac{A}{1 + j\omega_0/\omega_p}\right| = \frac{A}{\sqrt{1+\left(\frac{\omega_0}{\omega_p}\right)^2}} \geq 1$$

$$A \geq \sqrt{1+\left(\frac{\omega_0}{\omega_p}\right)^2} \qquad A \geq \sqrt{1+\tan^2\frac{\pi}{N}} \Rightarrow A \geq \sec\frac{\pi}{N}$$

- EX: if N=3, A must be larger than 2
- N=4, A must be larger than 1.414

VCO's Phase Noise Calculation





$$\overline{V_{N,in}^2} = \frac{\overline{I_N^2}}{G_m^2} = \frac{\frac{8kTg_{m1}}{3} + \frac{8kTg_{m3}}{3}}{G_m^2} = \frac{8kT}{3} \cdot \frac{g_{m1} + g_{m3}}{G_m^2}$$

VCO's Phase Noise Calculation

Since,

$$\left|\frac{d|H|}{d\omega}\right| = \left|\frac{d\phi}{d\omega}\right| = \frac{2}{\omega_o} \text{ at } \omega = \omega_o \text{ and } |H| = 1$$

Hence,

$$\left|\frac{Y}{X}(\omega_o + \Delta\omega)\right|^2 \approx \frac{1}{(\Delta\omega)^2\left(\left|\frac{d|H|}{d\omega}\right|^2 + \left|\frac{d\phi}{d\omega}\right|^2 |H|^2\right)} = \frac{1}{8}\left(\frac{\omega_o}{\Delta\omega}\right)^2$$

$$\left|\frac{V_{N,out}}{V_{out}}(\omega_o + \Delta\omega)\right|^2 = \frac{\overline{V_{N,in}^2}}{\overline{V_{out}^2}} \cdot \left|\frac{Y}{X}(\omega_o + \Delta\omega)\right|^2$$

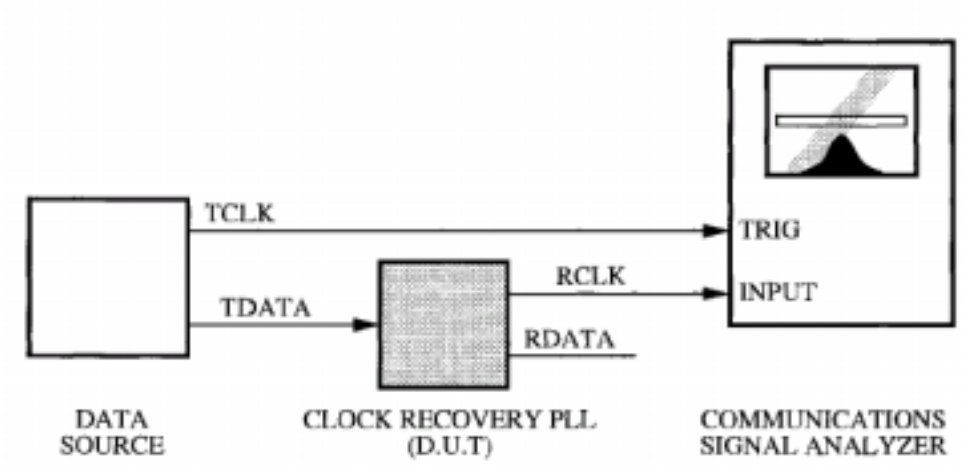
$$\left|\frac{V_{N,out}}{V_{out}}(\omega_o + \Delta\omega)\right|^2 = \frac{1}{\overline{V_{out}^2}} \cdot \frac{kT}{3} \cdot \frac{g_{m1} + g_{m3}}{G_m^2} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2$$

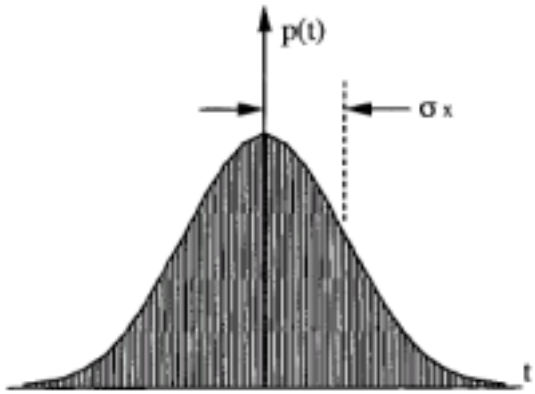
Let ω_o=1.8GHz, $\Delta\omega$=1MHz and $g_{m1}=g_{m2}$=320uS, $g_{m3}=g_{m4}$=1592uS,

==>Phase noise= -100.8dBc/Hz

VCO's Jitter Simulation

- *Closed-Loop, Transmit Clock Referenced*

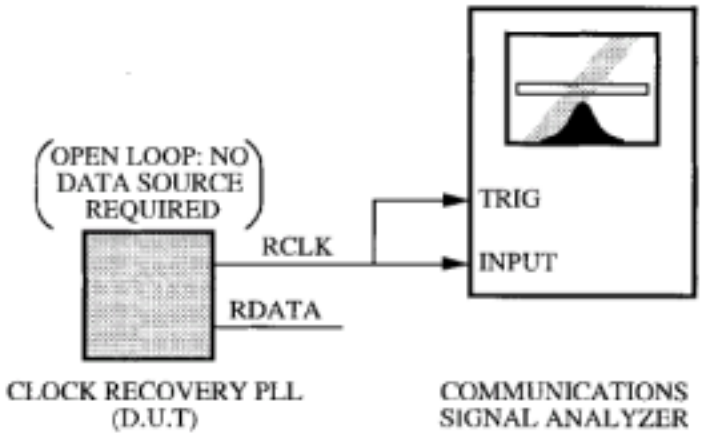


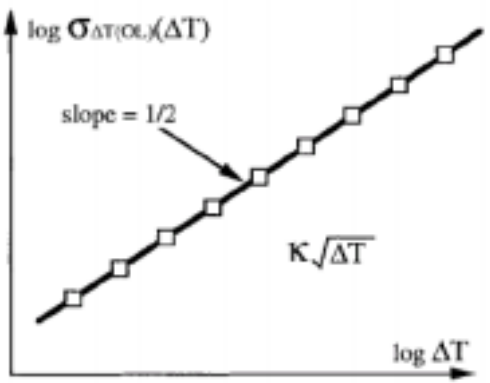


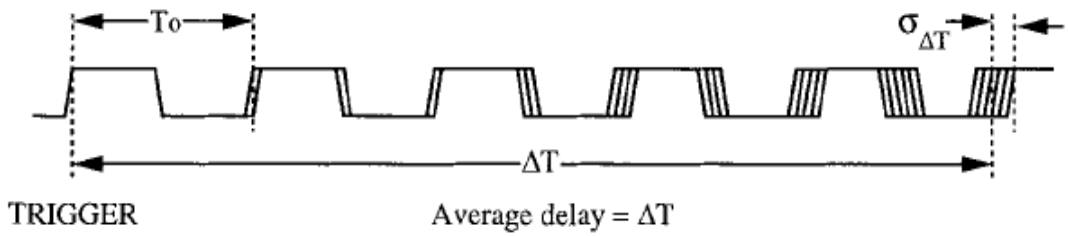
Ref: IEEE JSSC-32, pp.870, June 1997

VCO's Jitter Simulation

- *Open Loop, Self Referenced*





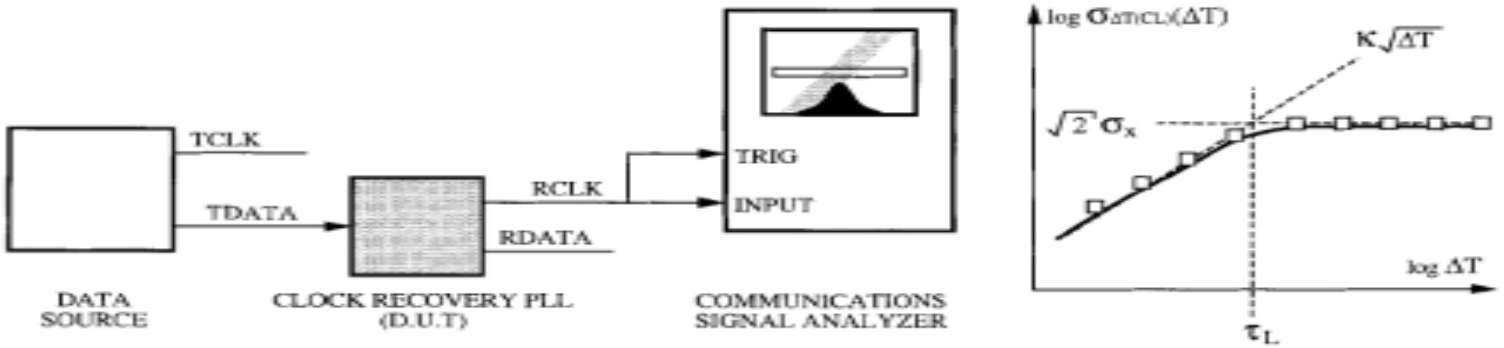


$$\sigma_{\Delta T(OL)}(\Delta T) \approx \kappa\sqrt{\Delta T}$$

If these jitter errors contributions from many individual stage delays are independent, then the standard deviation of the sum increases as the square root of the number of delays being summed.

VCO's Jitter Simulation

- *Closed Loop, Self Referenced*



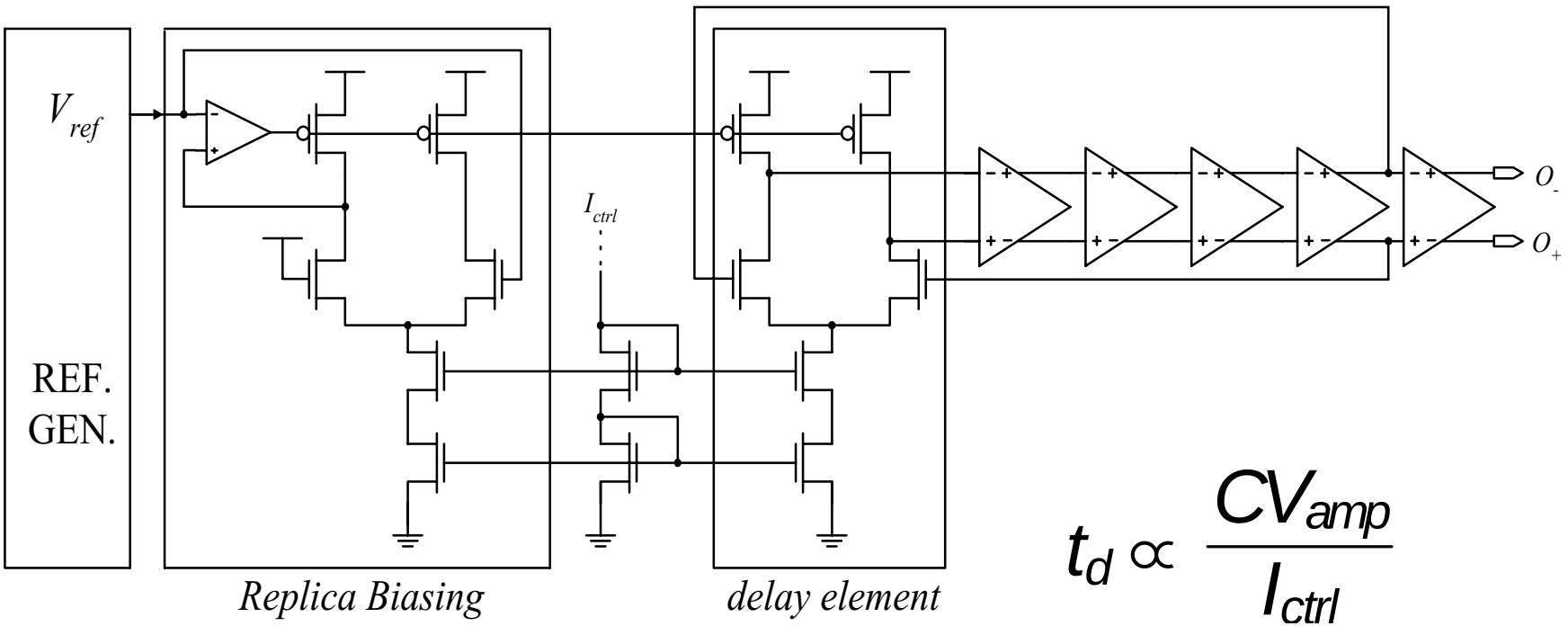
In clock recovery PLL's, however, it is common to overdamp the loop to avoid peaking in the jitter transfer function, and the loop transfer function can be approximated as

$$H(s) = \frac{2\pi f_L}{s + 2\pi f_L} \qquad \tau_L = \frac{1}{2\pi f_L}$$

At very long delays, the jitter over the measurement interval ΔT is due to the σ_x jitter at the beginning and end of the time period. Since the jitter errors of clock edges separated by a long delay are uncorrelated, the total jitter is $\sqrt{2}\sigma_x$.

The closed-loop σ_x in terms of the open-loop figure of merit, κ $\qquad \sigma_x = \kappa\sqrt{\frac{1}{4\pi f_L}}$

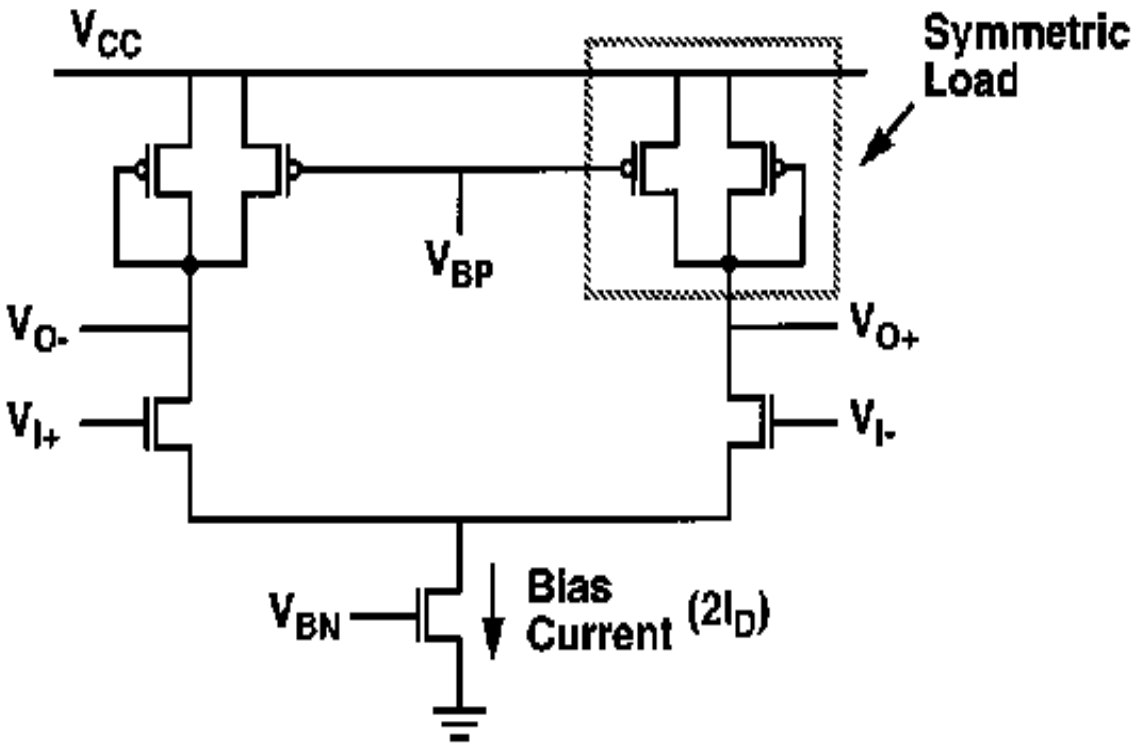
Current Controlled Oscillator



$$t_d \propto \frac{CV_{amp}}{I_{ctrl}}$$

IEEE JSSC, SC-27, pp. 1599-, Nov. 1992.

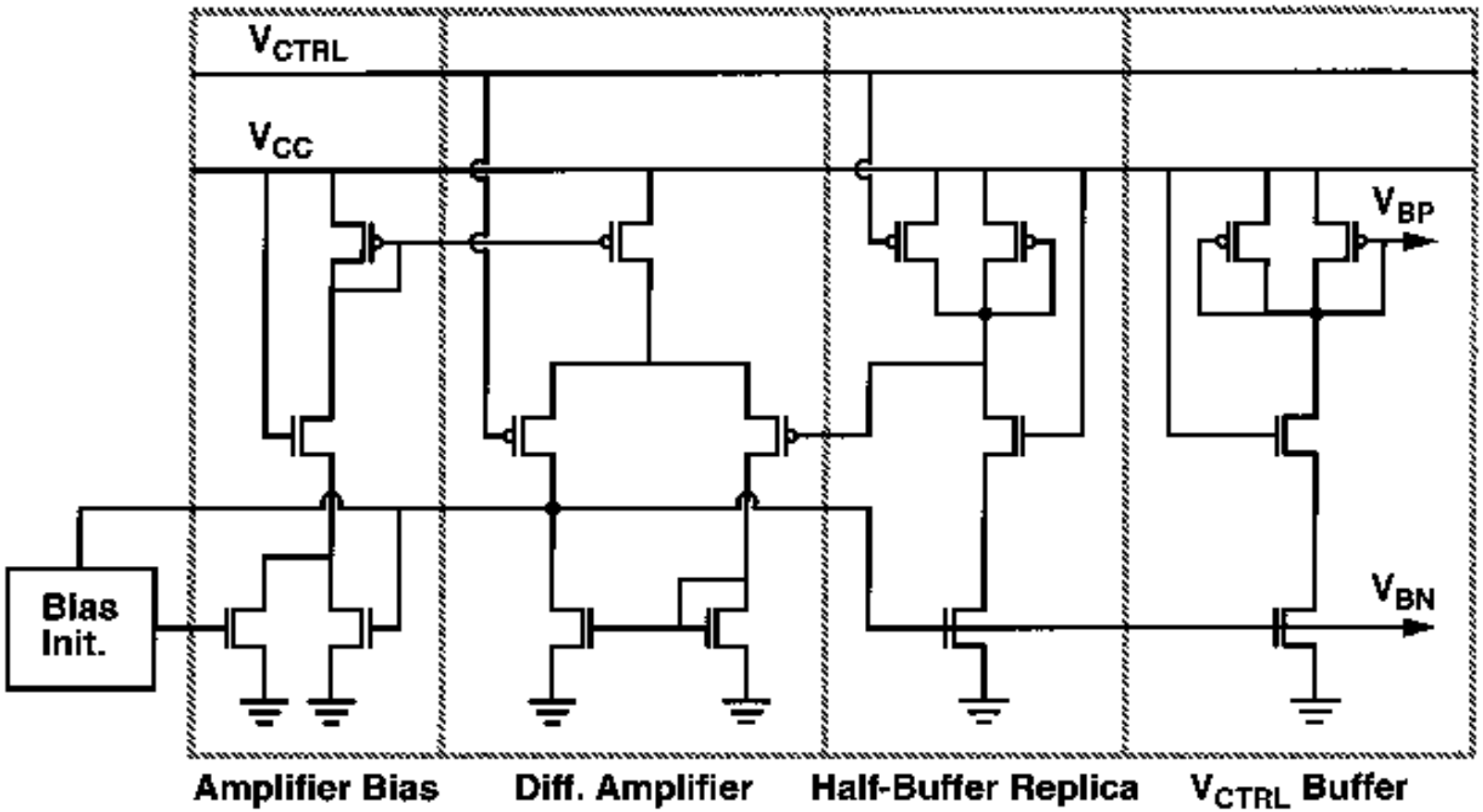
Symmetric Load Amplifier



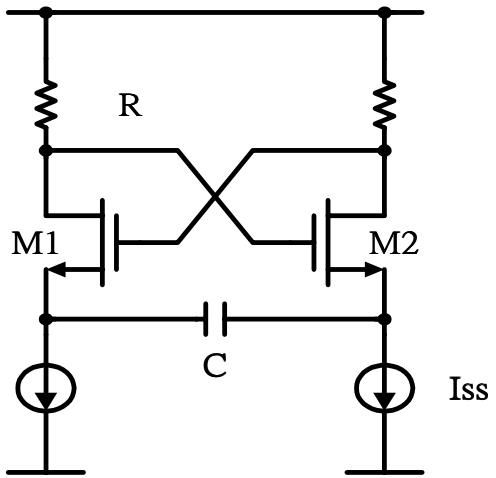
. 1. Differential buffer delay stage with symmetric loads.

IEEE JSSC, SC-31, pp. 1723-, Nov. 1996.

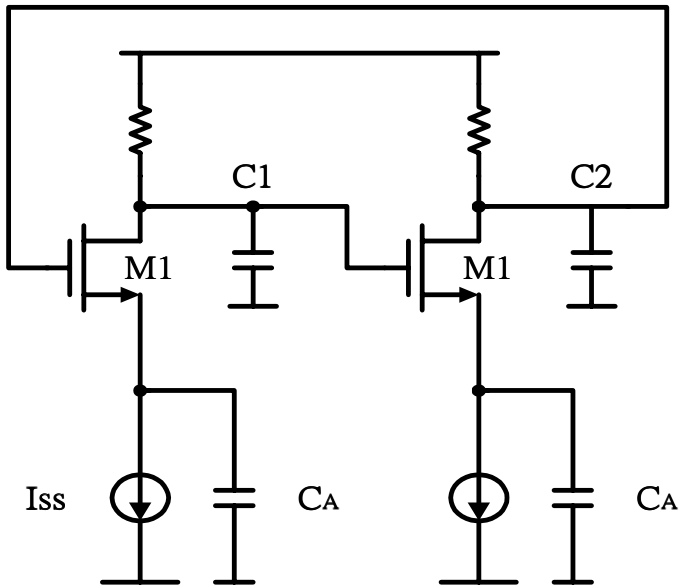
Replica Biasing Circuit



Multivibrator



(a)

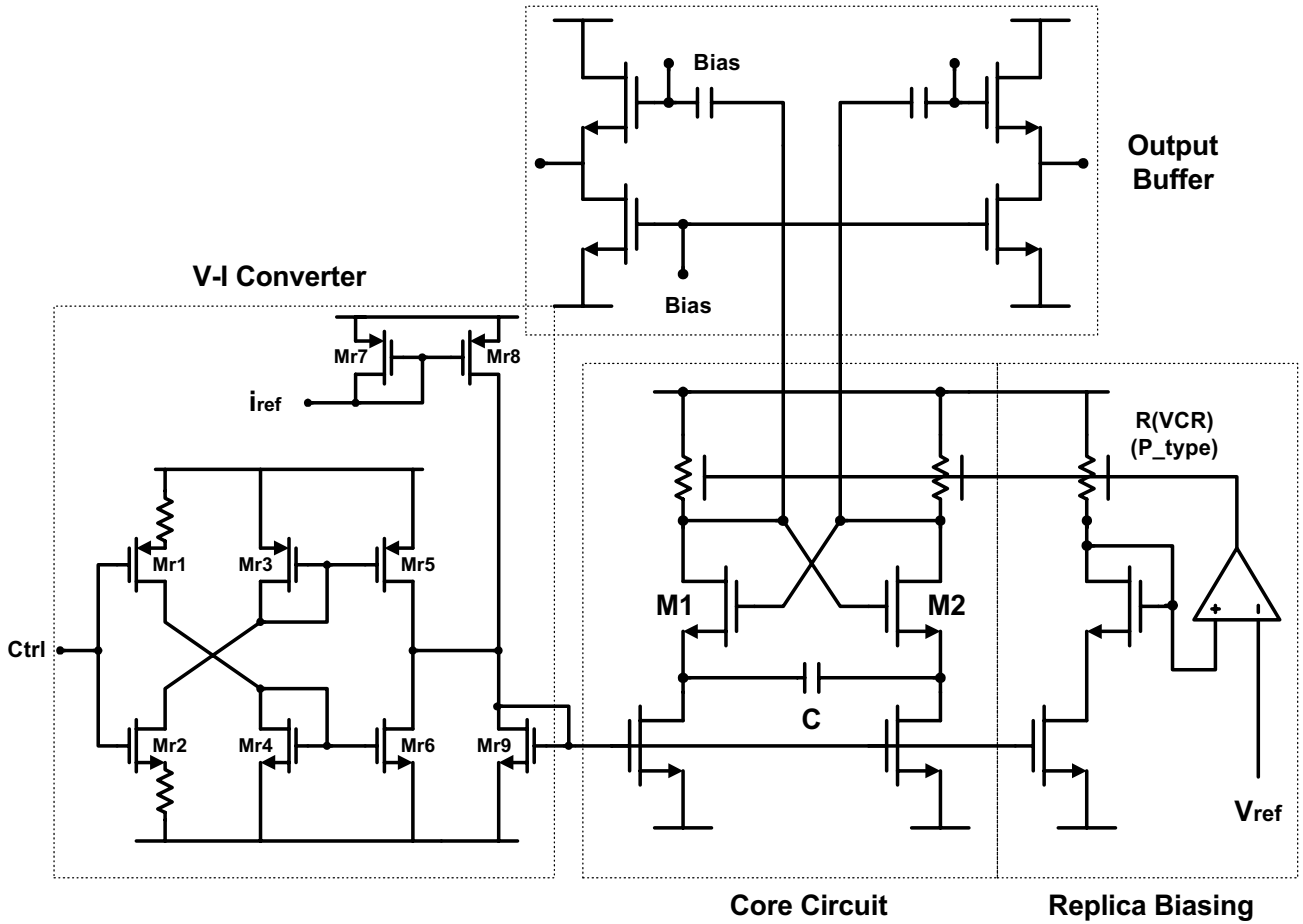


(b)

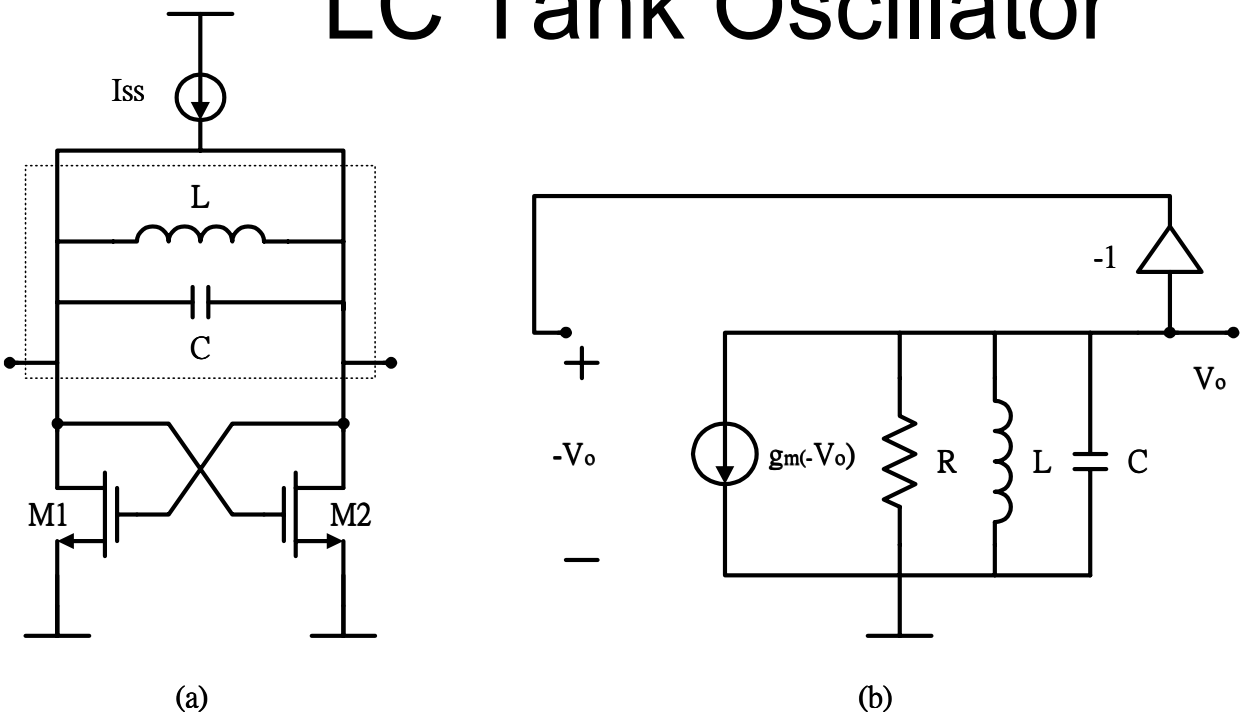
$$H(s)=\left[\frac{-g_m R C_A s}{(g_m+C_A s)(RC_D s+1)}\right]^2 \quad \text{where C1=C2=}C_D$$

If $H(j\omega_o)=1$ and $g_m R=\frac{C_A}{C_A-C_D}$ then $\omega_o=\sqrt{\frac{g_m}{RC_AC_D}}$

Multivibrator



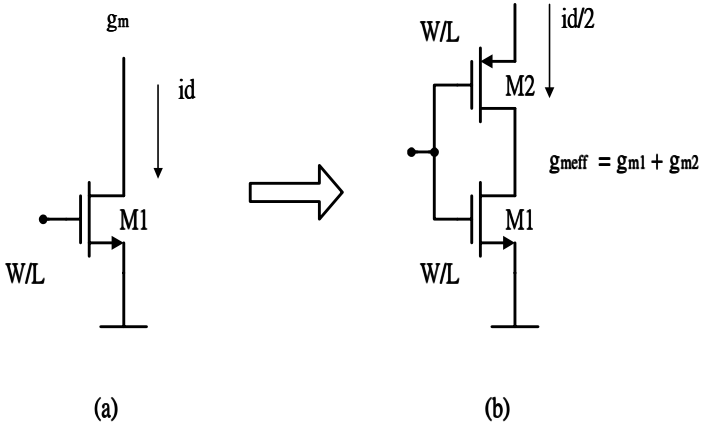
LC Tank Oscillator

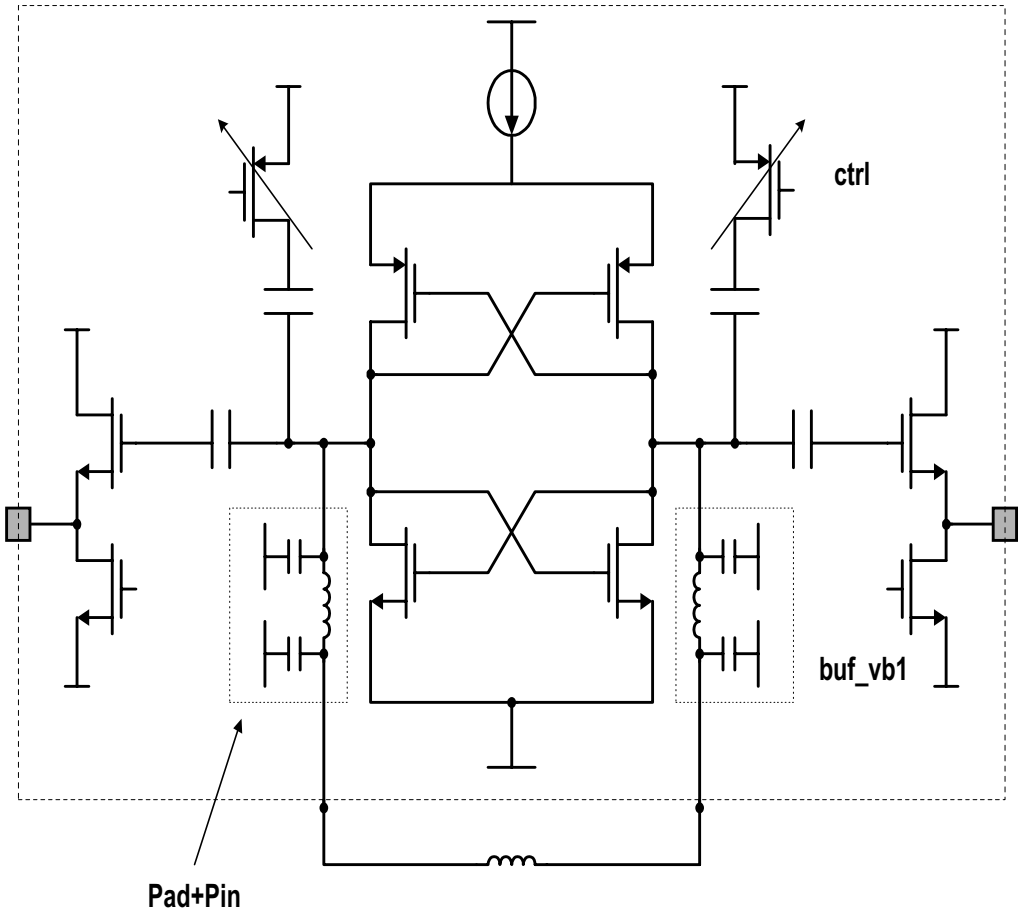


$$V_O = g_m(-V_O)\cdot(R_{eff} // sL // \frac{1}{sC})$$

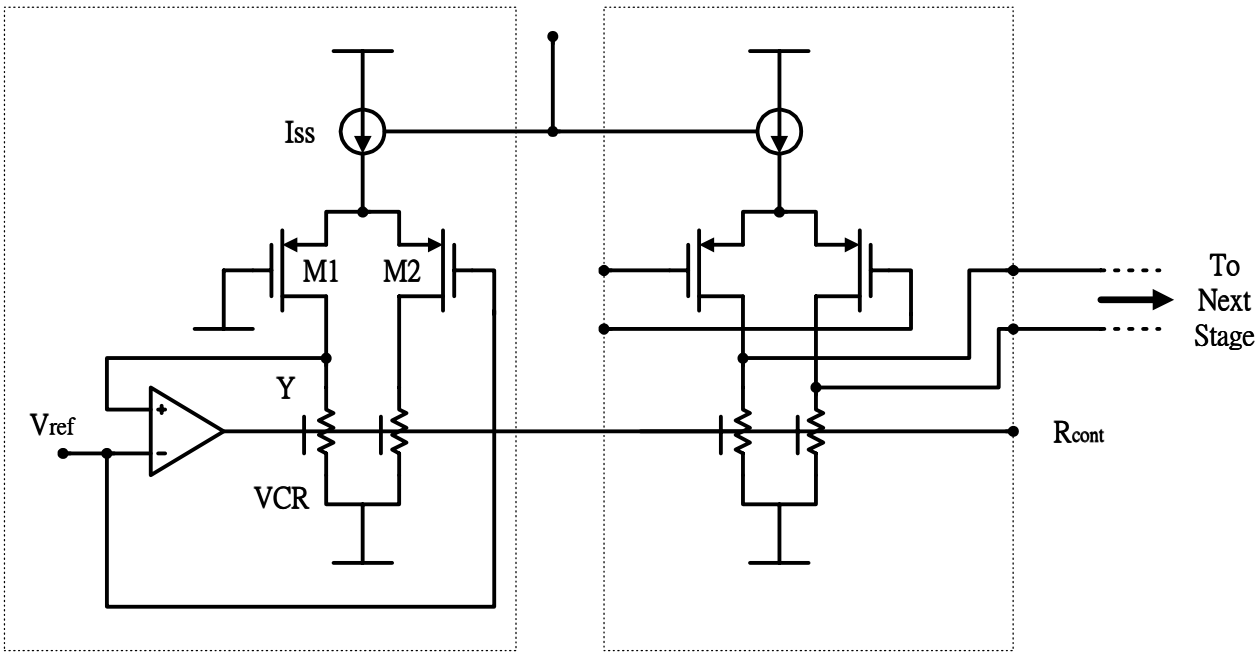
If $\frac{1}{g_m} = R_{eff}$ then $\omega_o = \frac{1}{\sqrt{LC}}$

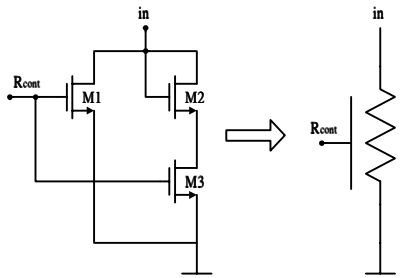
Current Reuse



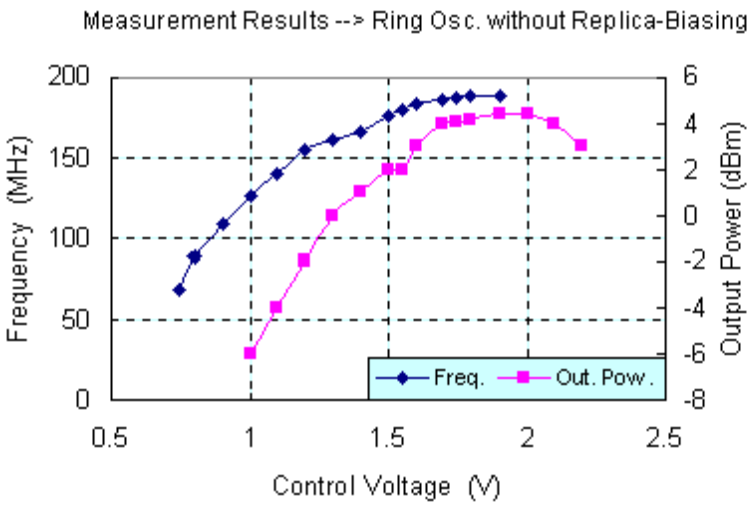


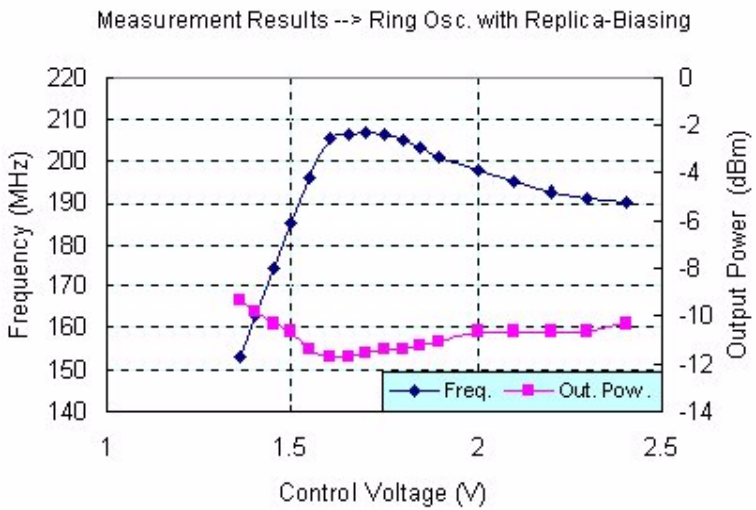
5-satge Ring Oscillator



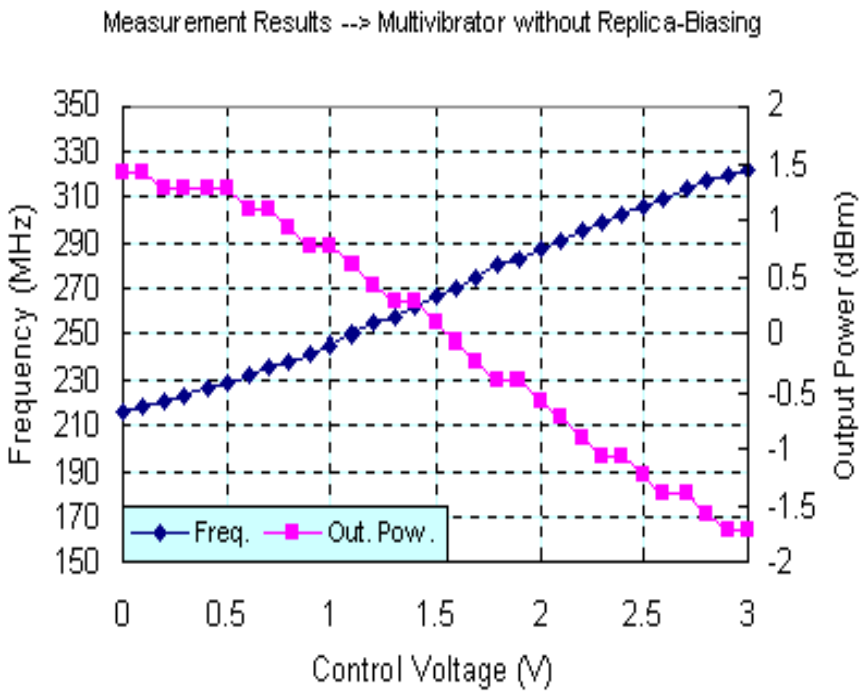


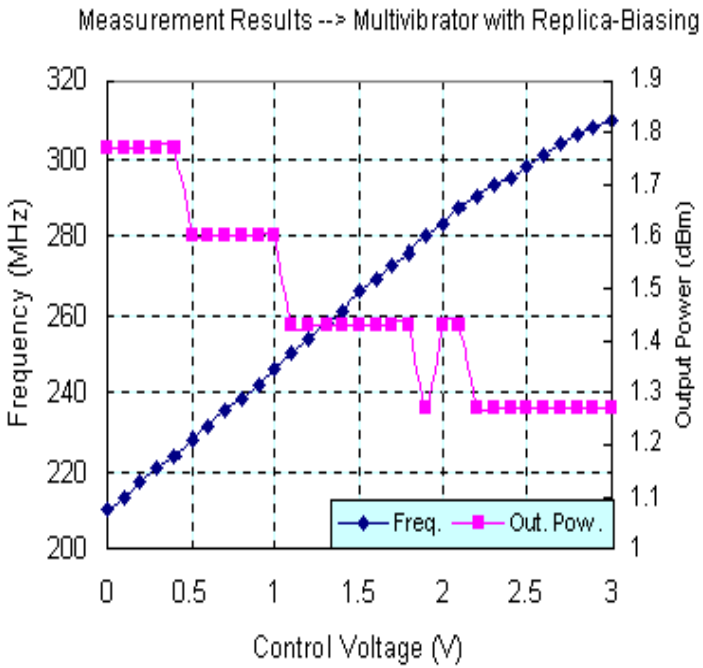
5-satge Ring Oscillator



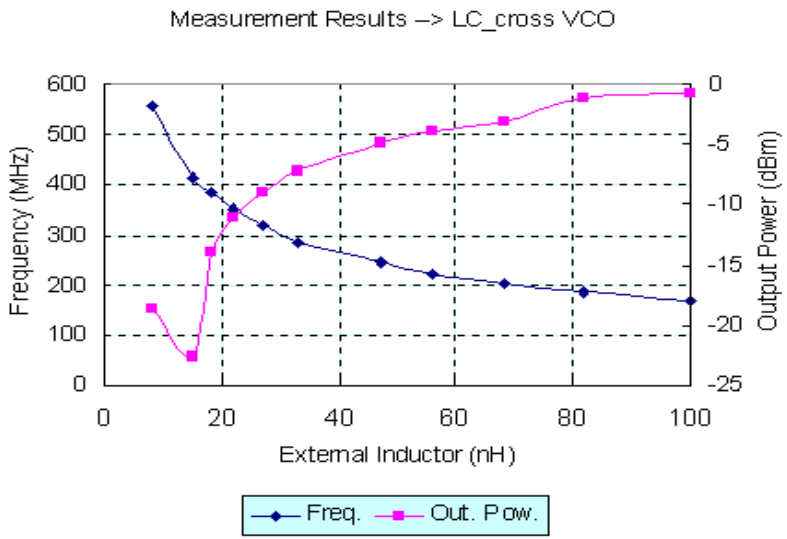


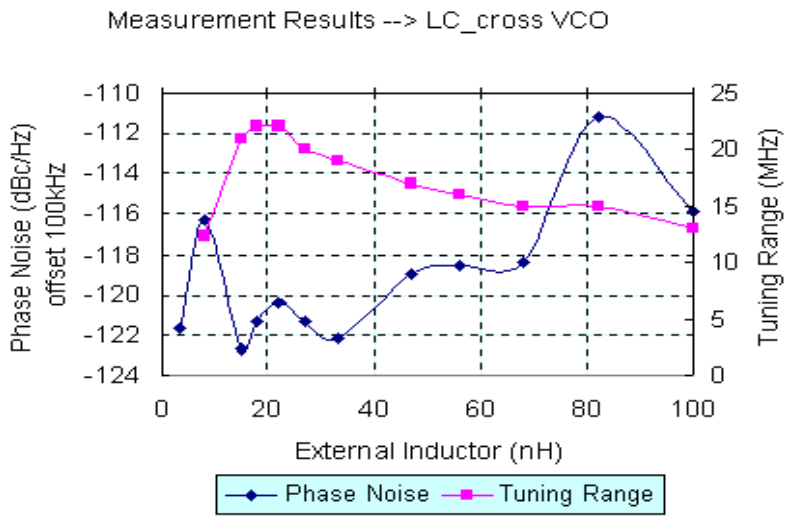
Multivibrator

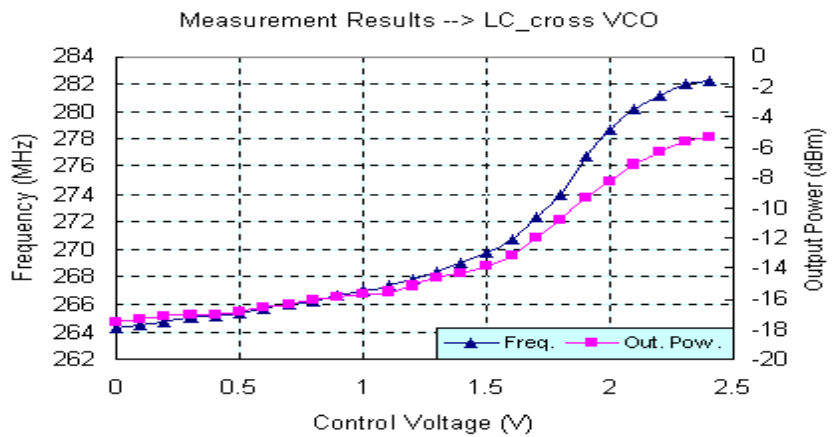




LC Tank Oscillator







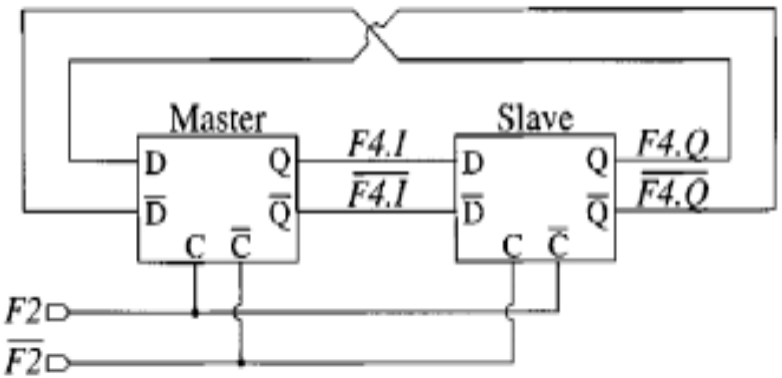
Comparisons of three kinds of Osc.

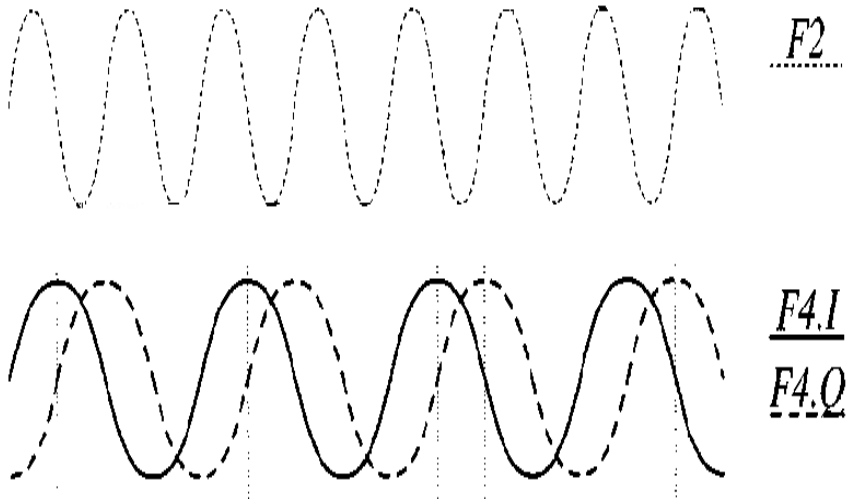
	Power Supply (V)	Tuning Range	Phase Noise (dBc/Hz) offset 100KHz	Power Consumption (mW)	Output Power Range (dBm)
Ring Osc. (without Replica-Biasing)	**3.12**	**0.75~2.2(V)** **23.4~188.6 (MHz)**	**~ -92**	**14.1336**	**-35.67 ~ 3.00**
Ring Osc. (with Replica-Biasing)	**3.12**	**1.36~1.65(V)** **153.4~206.5 (MHz)**	**~ -82** **~ -94 (saturation)**	**18.0336**	**-9.33 ~ -11.67**
Multivibrater (without Replica-Biasing)	**3.12**	**0.00~3.00(V)** **215.8~322.3 (MHz)**	**~ -83**	**21.8400**	**-1.73 ~ 1.43**
Multivibrater(with Replica-Biasing)	**3.12**	**0.00~3.00(V)** **210.0~310.0 (MHz)**	**~ -81**	**23.1504**	**1.27 ~ 1.77**
LC_cross	**3.12**	**0.00~2.40(V)** **264.3~282.3 (MHz)**	**~ -108**	**9.3320**	**-17.5 ~ -5.33**

表 5.1: 五組壓控振盪器電路量測特性列表

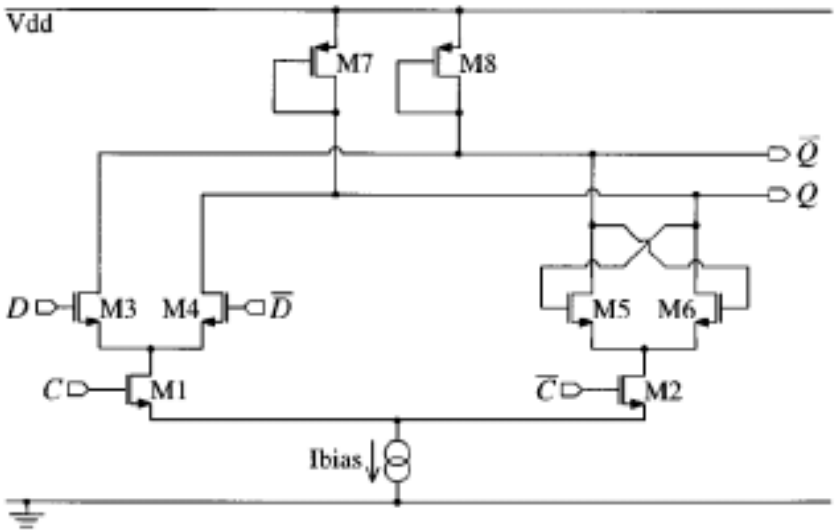
Frequency Divider

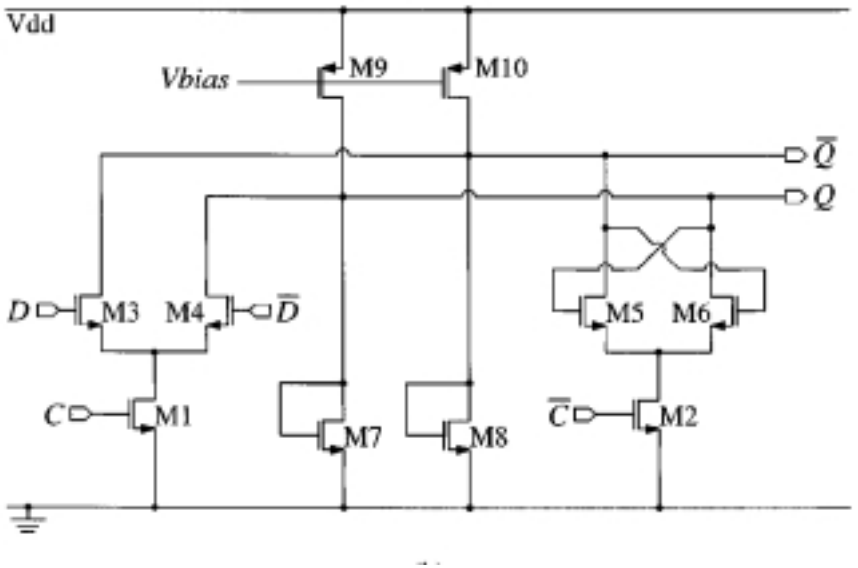
Divide-by-Two





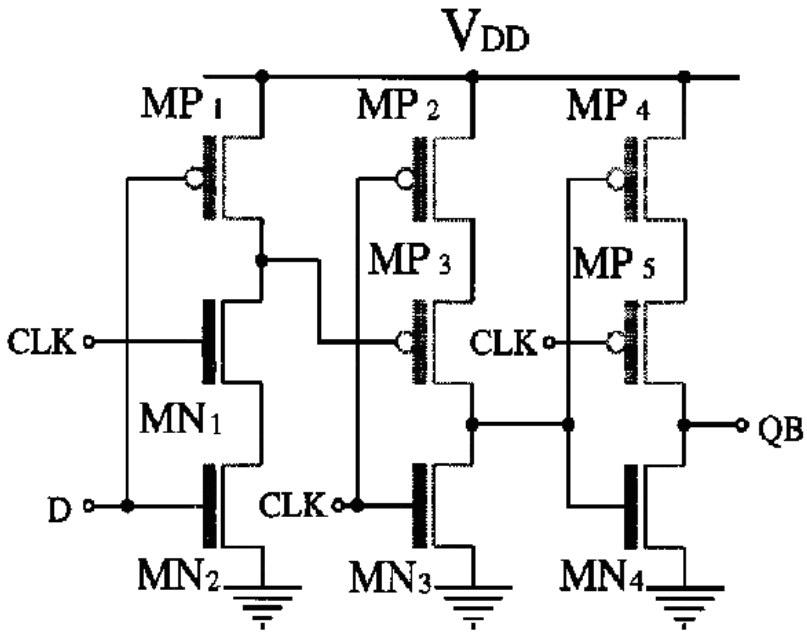
Divide-by-Two Circuits

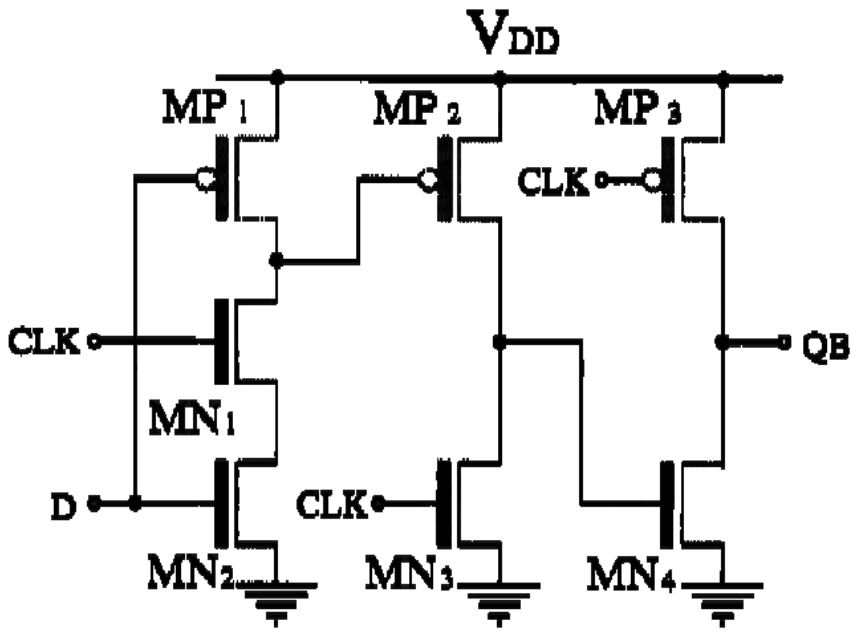




IEEE JSSC, SC-31, pp. 890-, July 1996.

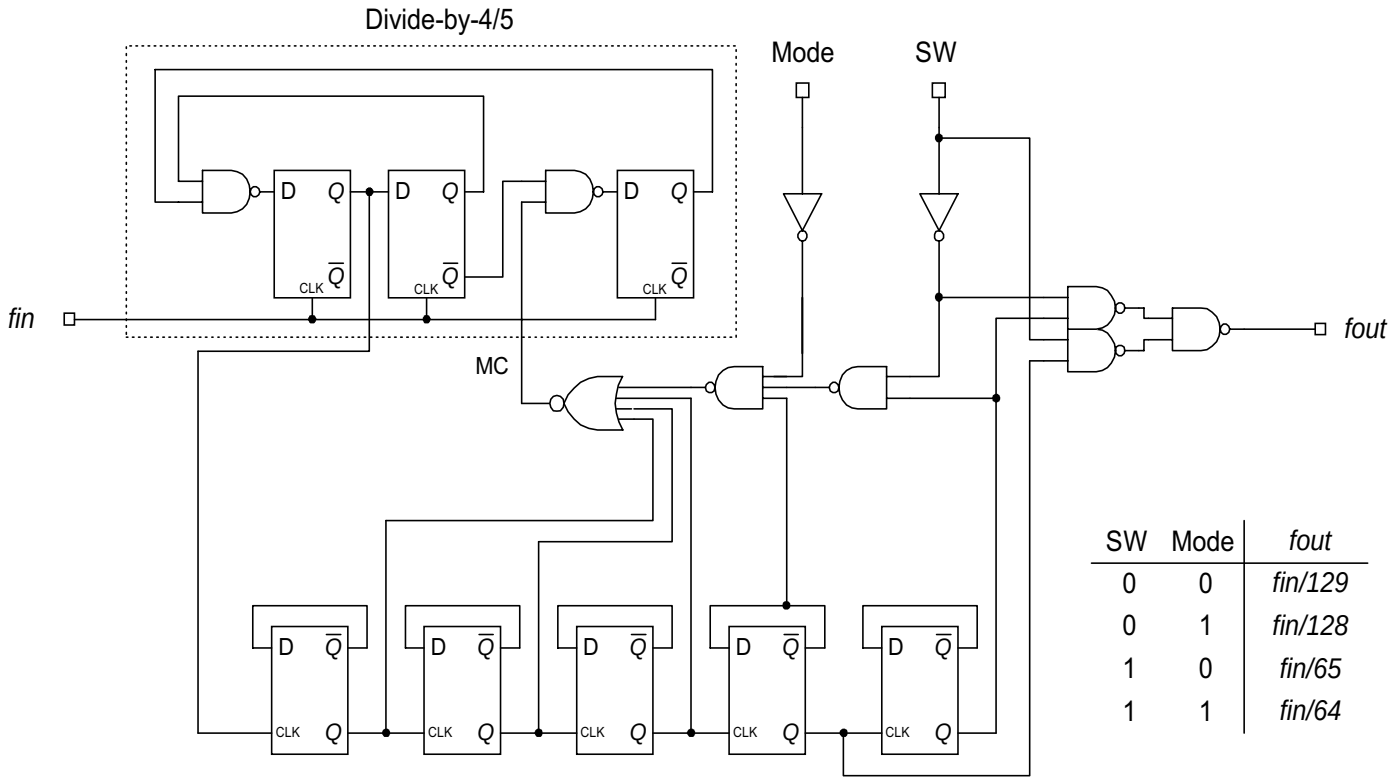
TSPC Dynamic Circuit





IEEE JSSC, SC-31, pp. 749-, May 1996.

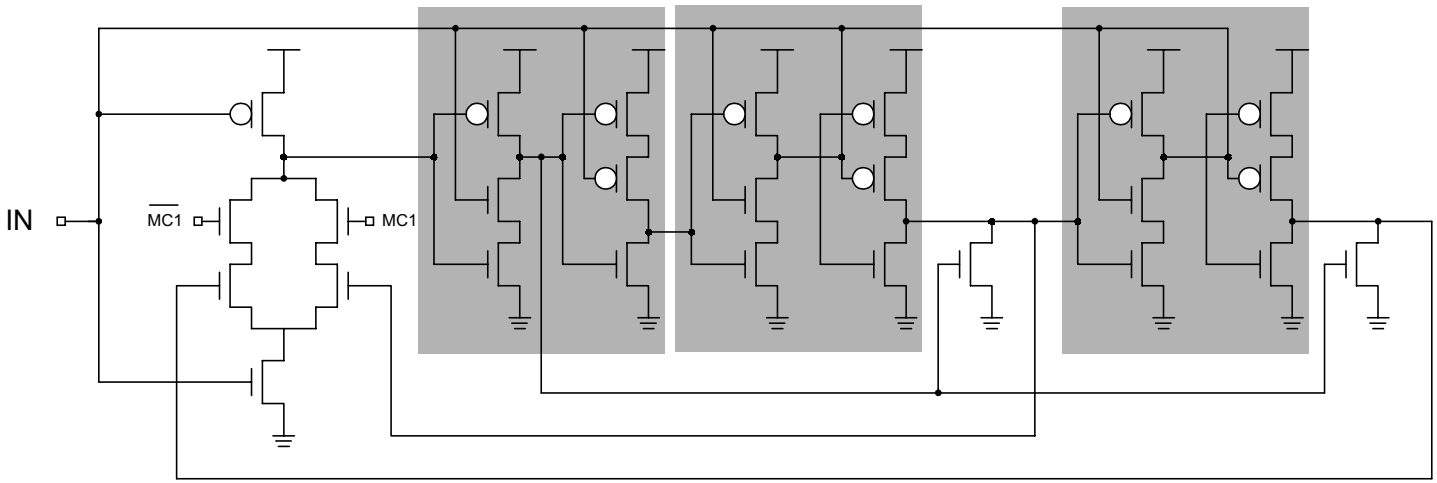
Functional block diagram of the dual-modulus prescaler



SW	Mode	*fout*
0	0	*fin/129*
0	1	*fin/128*
1	0	*fin/65*
1	1	*fin/64*

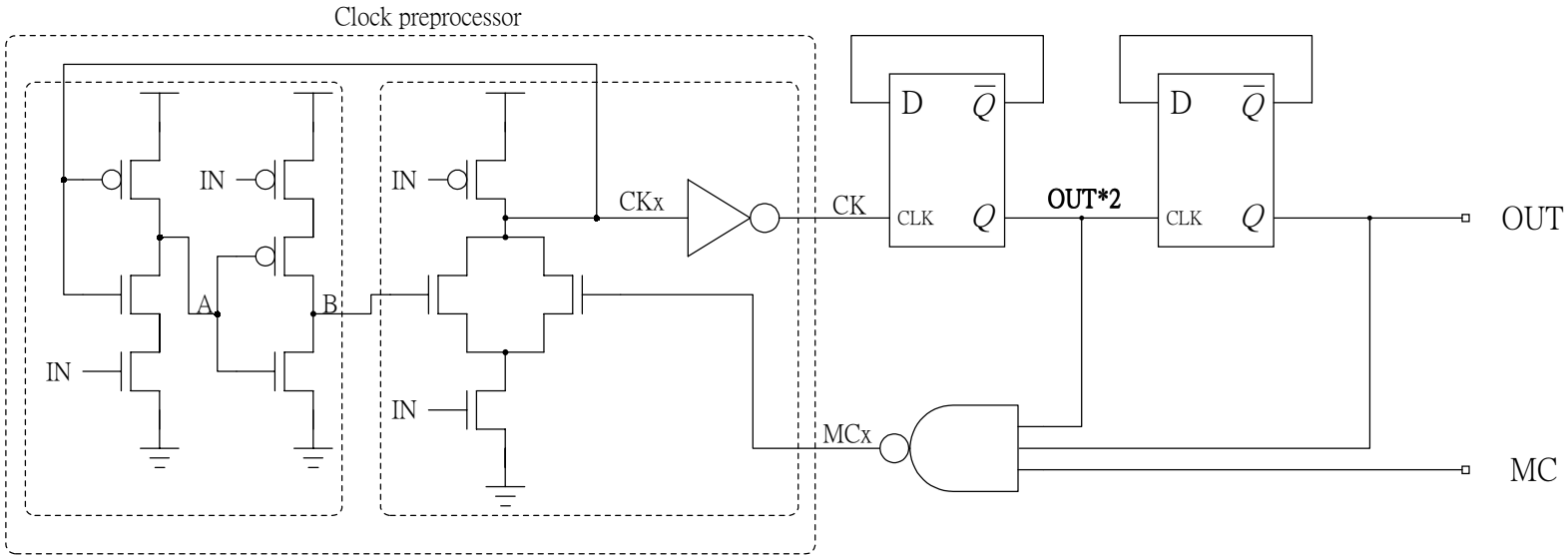
High frequency CMOS dual-modulus prescaler

- Divide-by3/4



- TSMC 0.8-μm SPDM CMOS process
- VDD=5V, Max. operating freq. :1 GHz

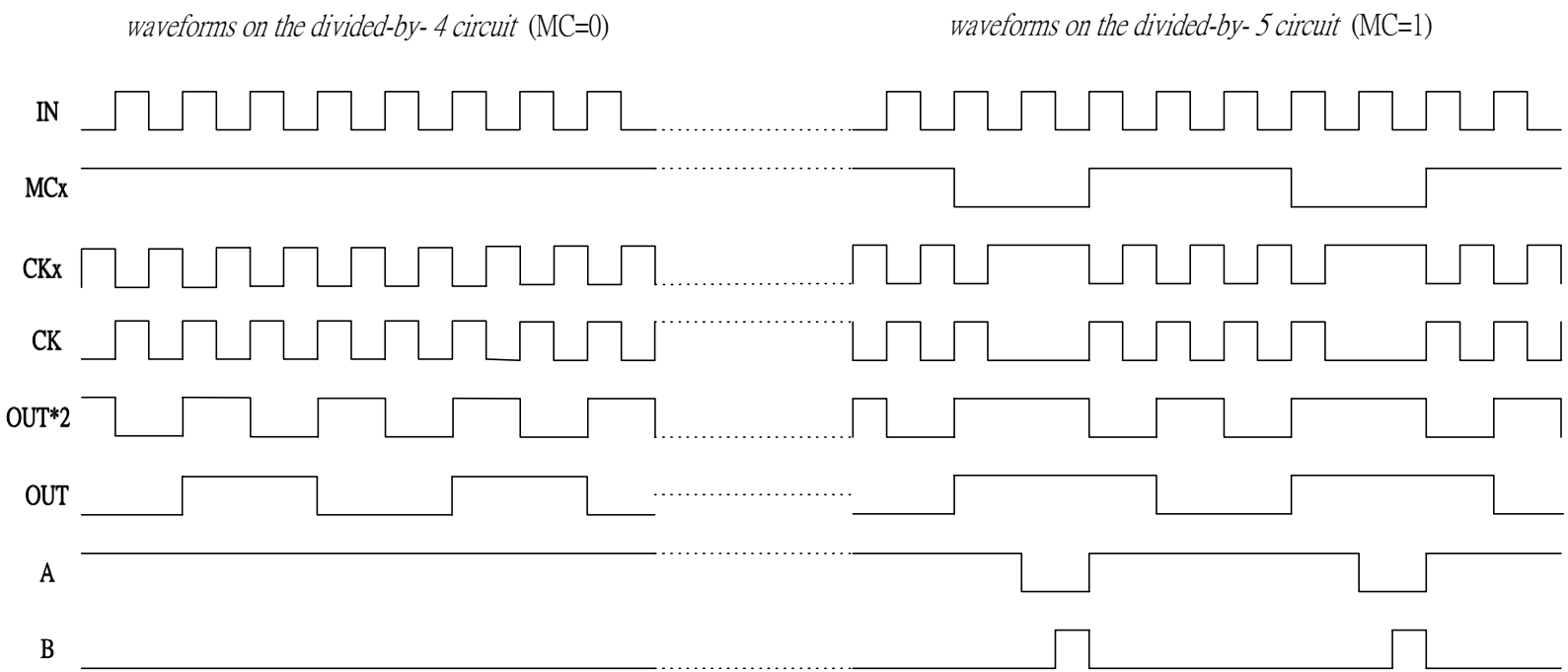
A High-Speed Divide-by-4/5 Counter for a Dual-Modulus Prescaler



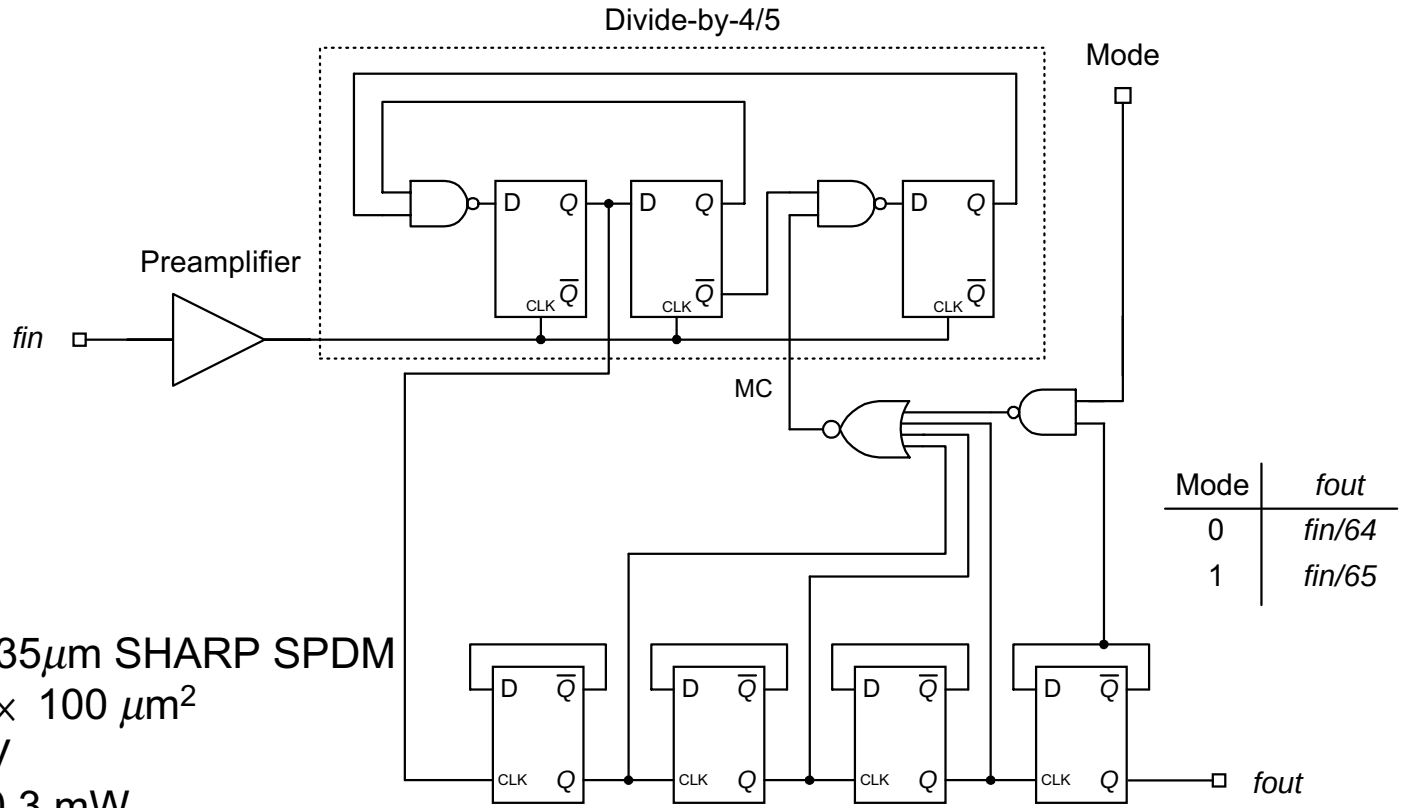
TSMC 0.6- μm SPDM CMOS process

Max. operating freq. : 1.1 GHz , Power : 19.2 mW@ VDD=3V

Timing diagram

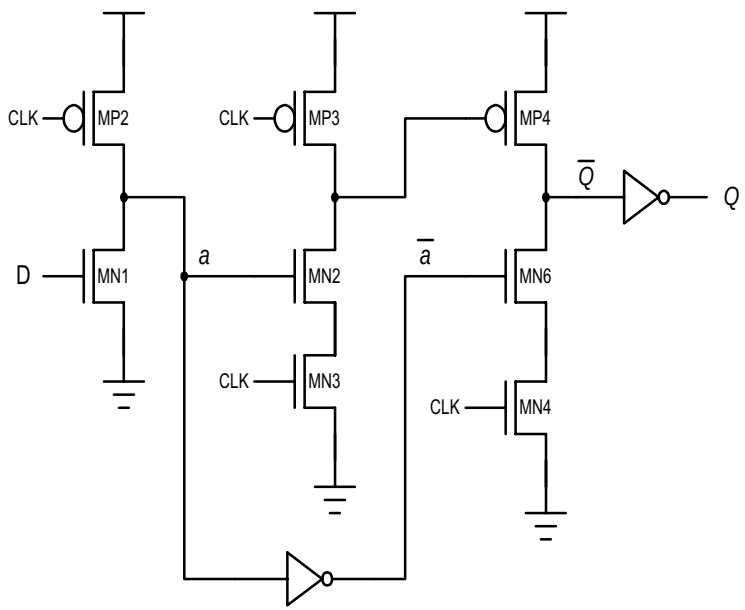


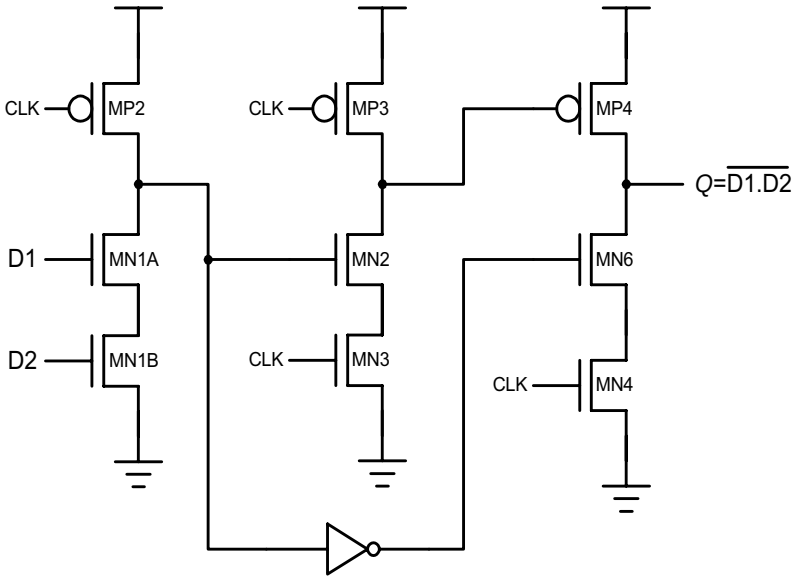
3 V 4 GHz Prescaler with improved DFF



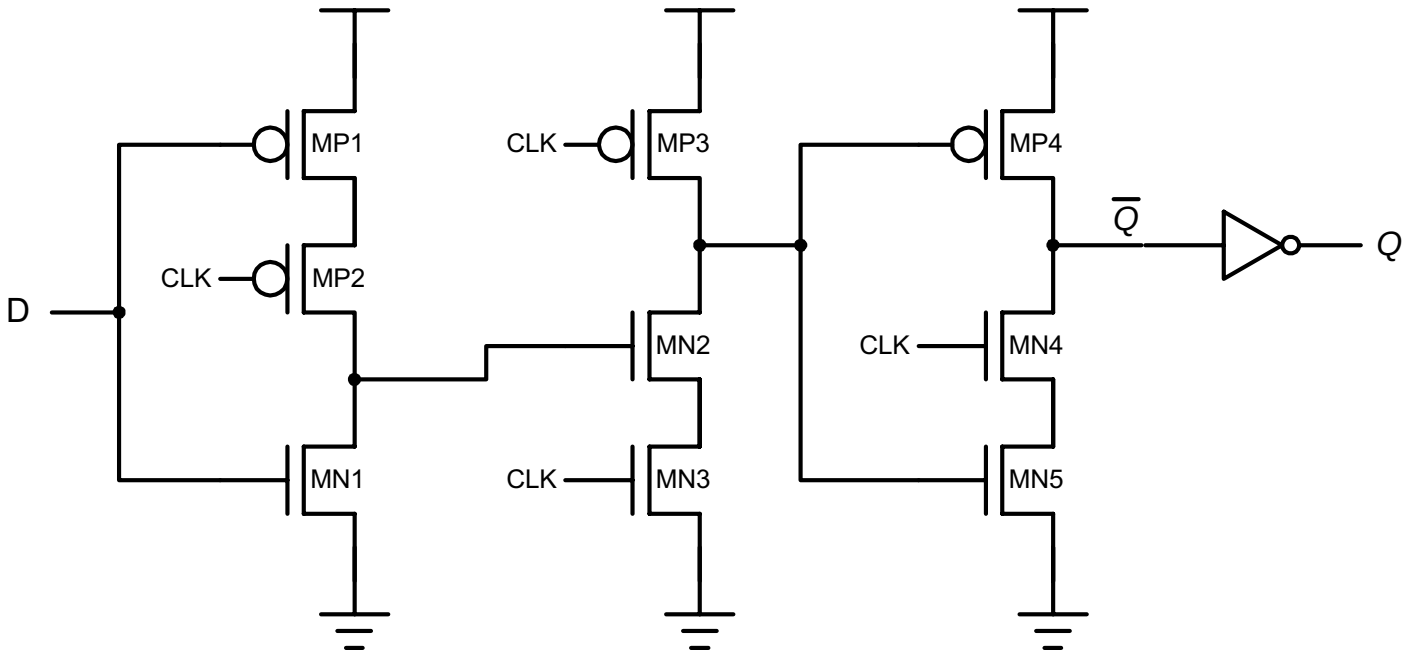
CHIP Features
Technology : 0.35μm SHARP SPDM
Core area : 570× 100 μm^2
Supply voltage : 3V
Power : 90.3 mW
Max. operating freq.: ～4000 MHz

Improved TSPC ratioed DFF

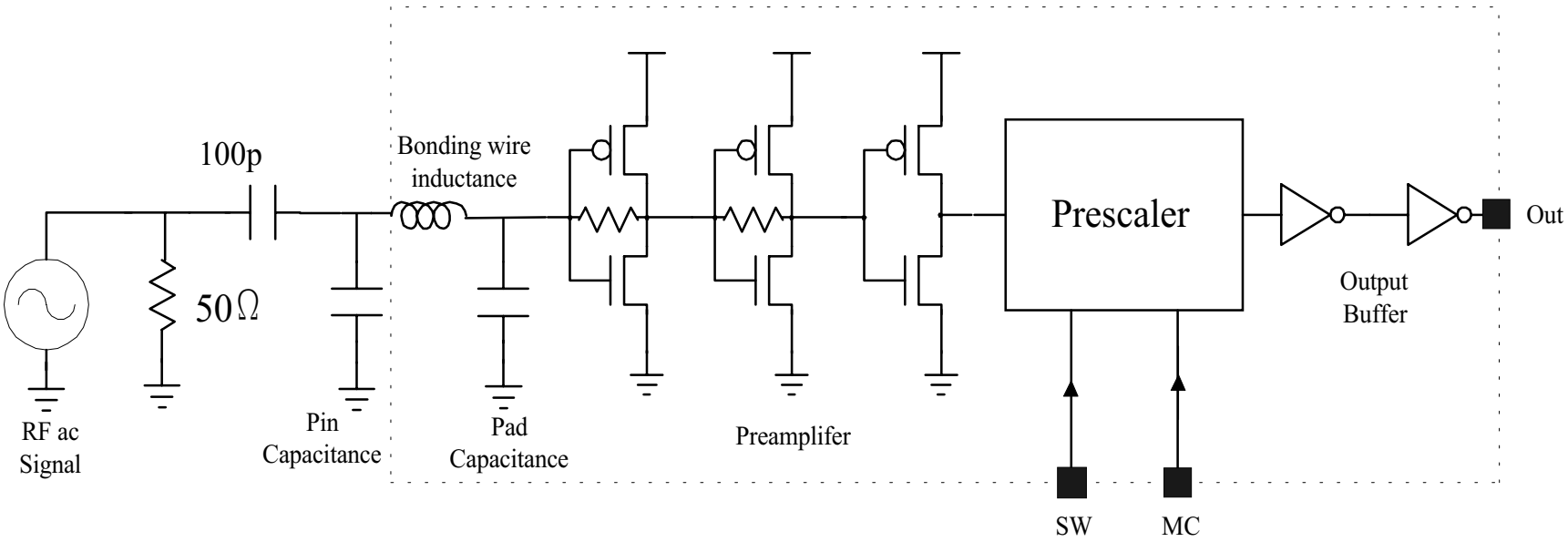




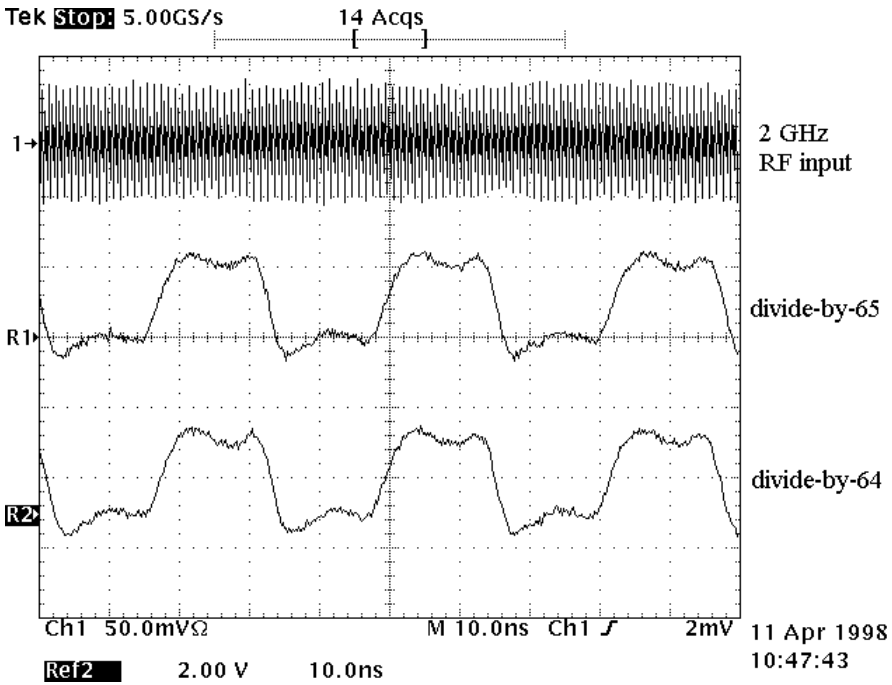
TSPC DFF by Yuan and Svensson

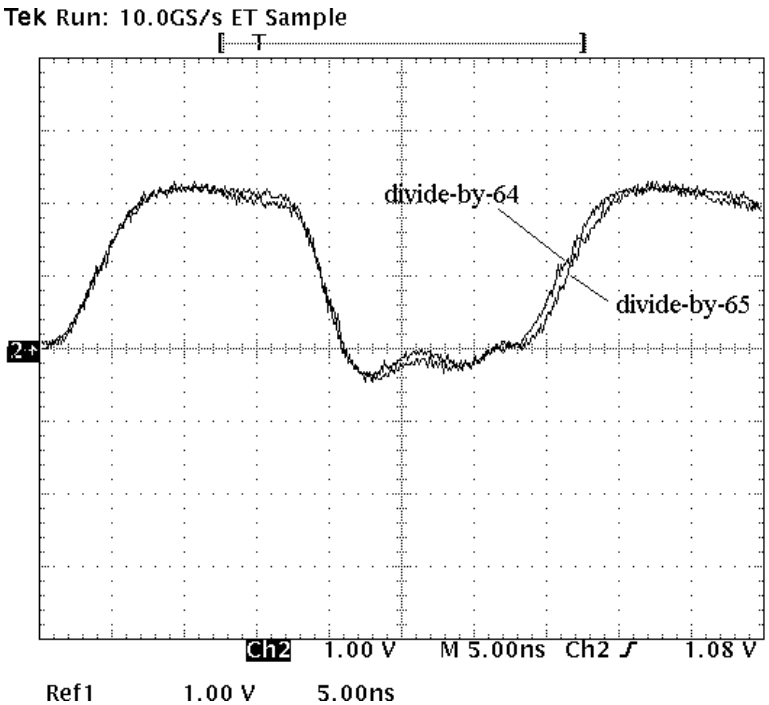


Input Preamplifer Design

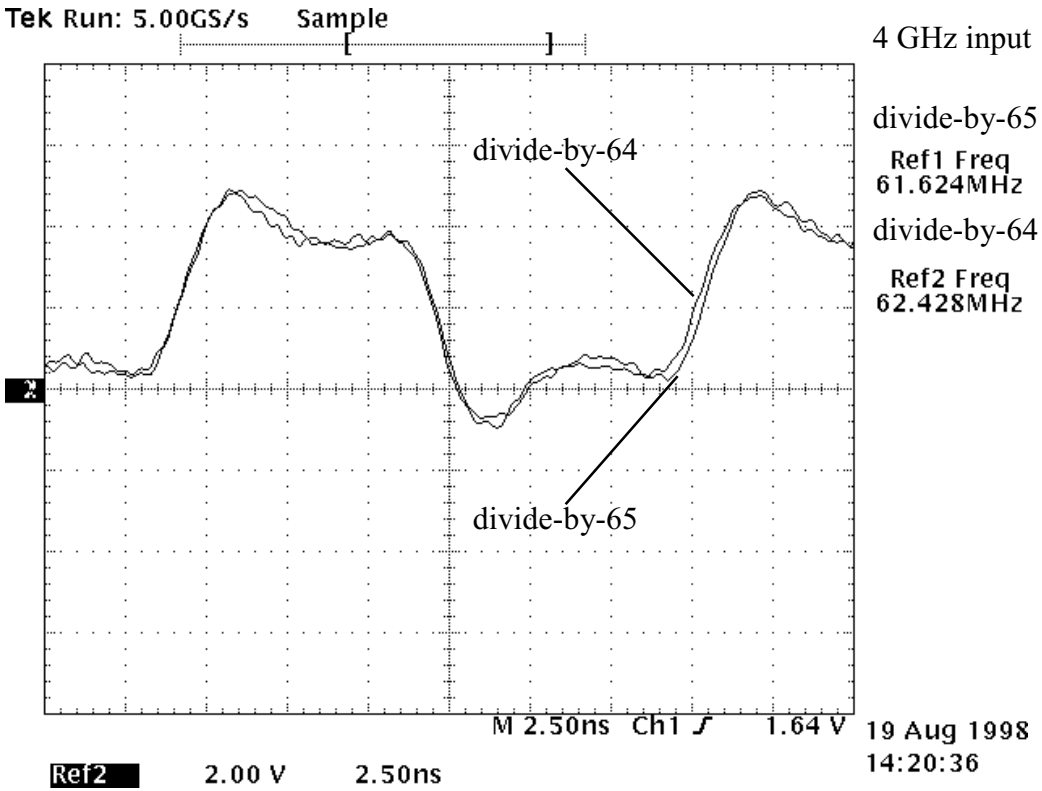


Measured waveforms of the prescaler

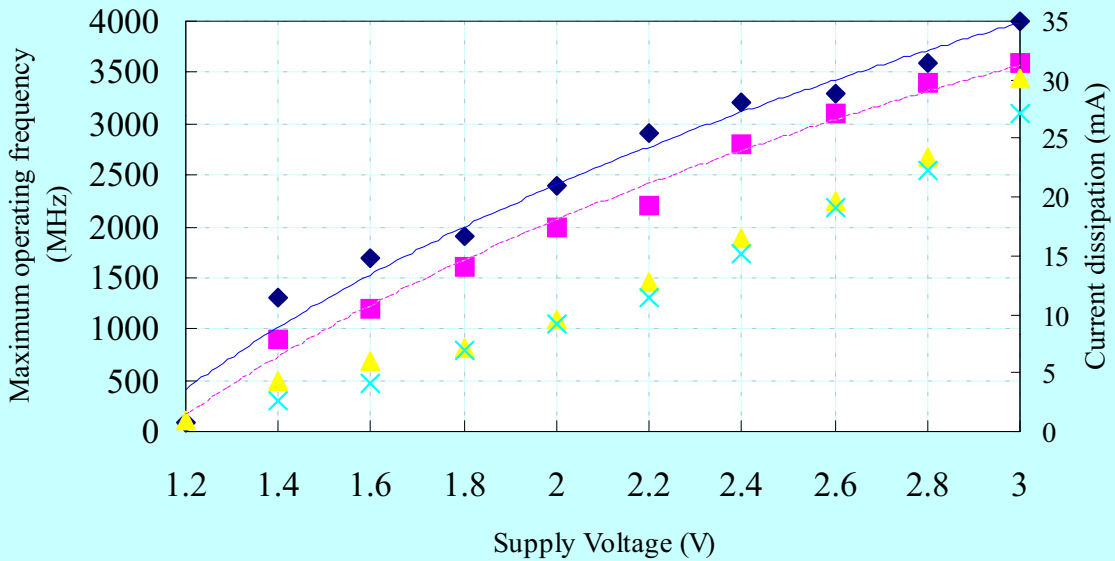




Measured waveforms of the prescaler



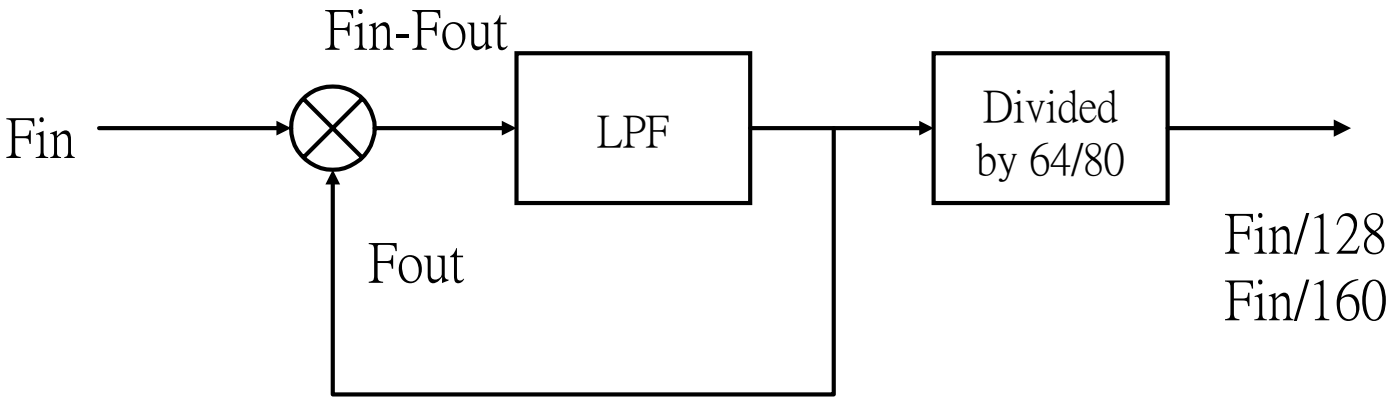
Measured maximum operating frequency and power dissipation



- frequency using LFF
- frequency using only DFF
- current dissipation using LFF
- current dissipation using only DFF

Technology:
0.35*u*m SHARP DPDM CMOS, Sharp. Inc.

Regenerative Frequency Divider



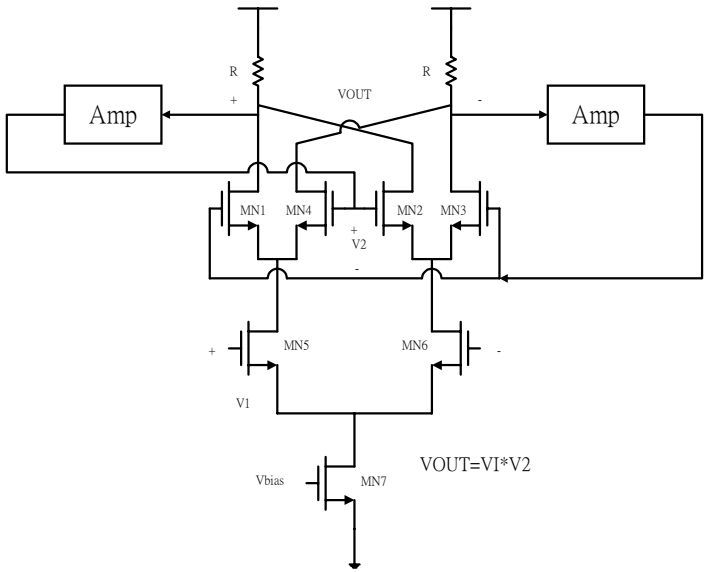
Fin-Fout=Fout

=> Fout=Fin/2

- Low frequency operation limitation
- ***LPF*** is realized by the low-pass characteristic of amplifiers

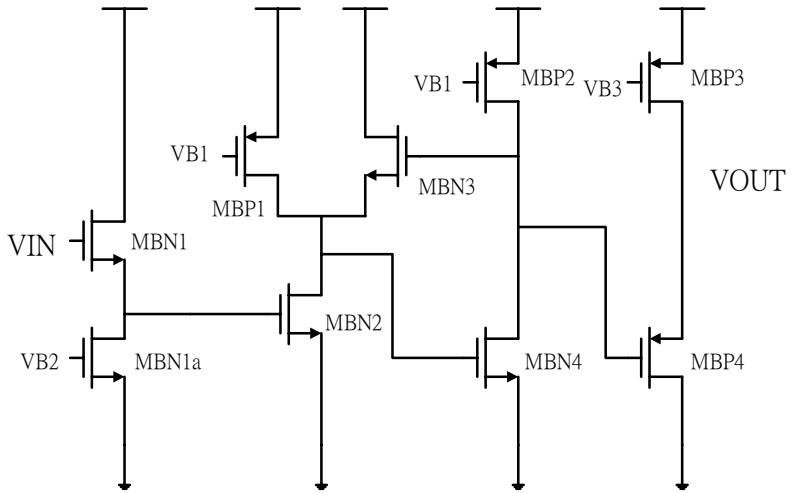
Circuit Implementation

- Mixer



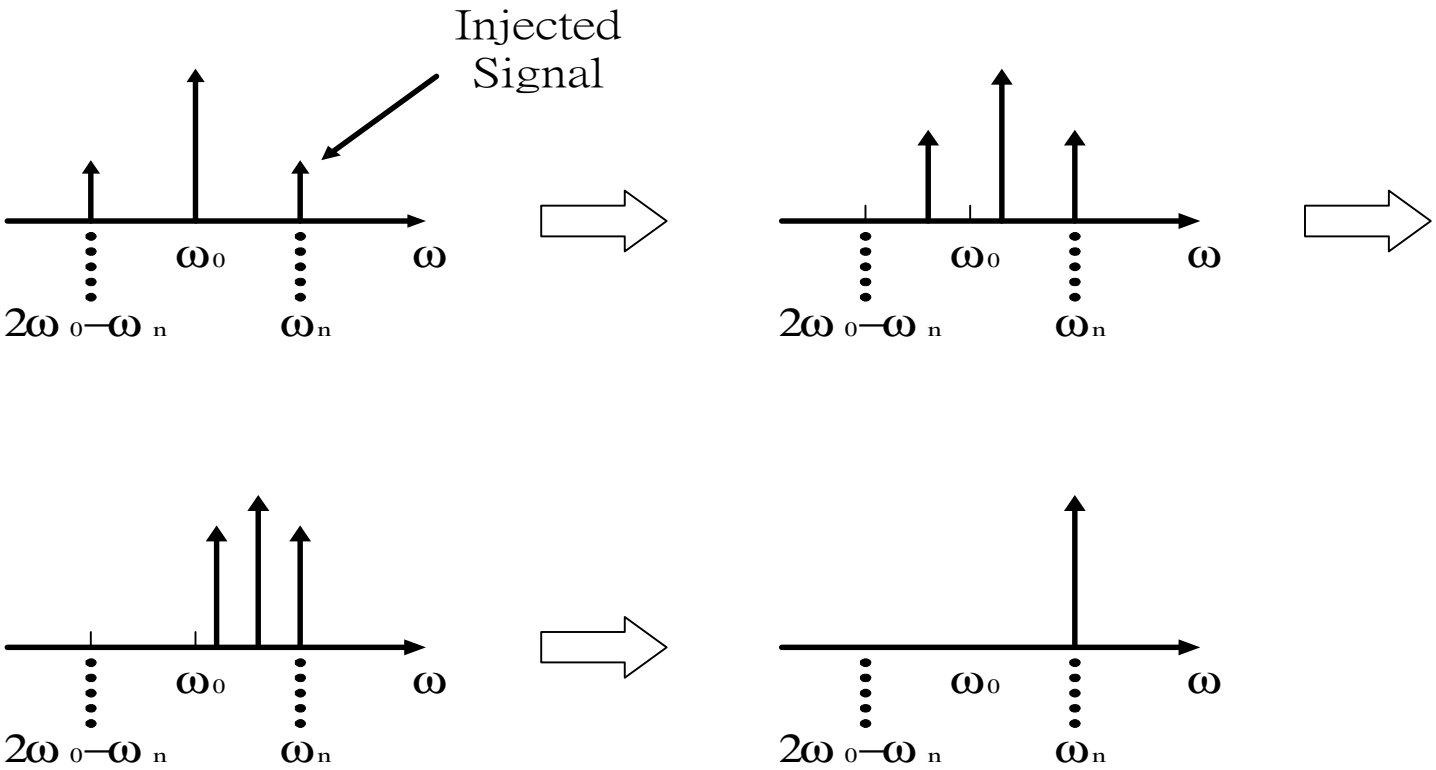
Gilbert's cell

- Amplifier



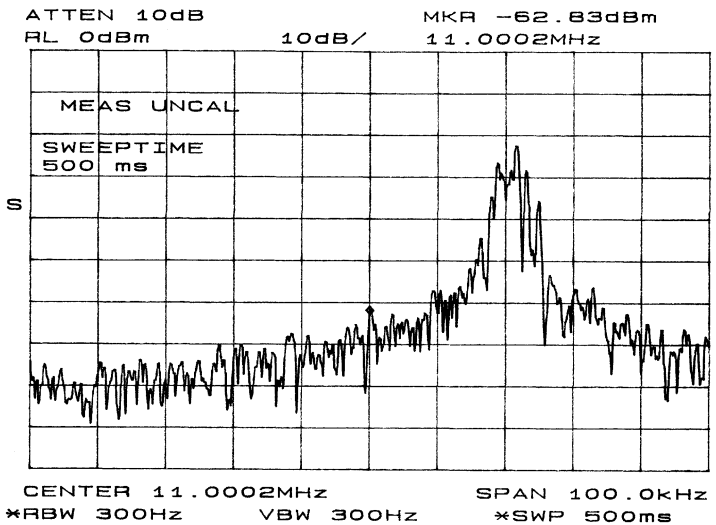
Gain=gm_{MBN2}/gm_{MBN3}

The principle of injection locking

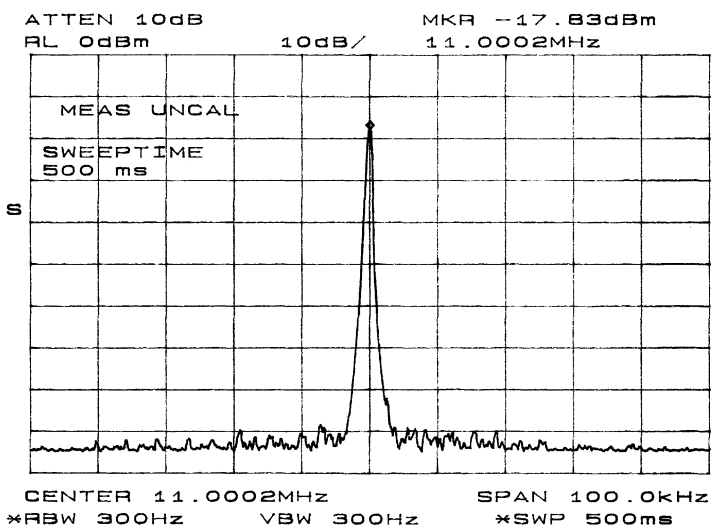


The phenomenon of injection locking

- Without injection

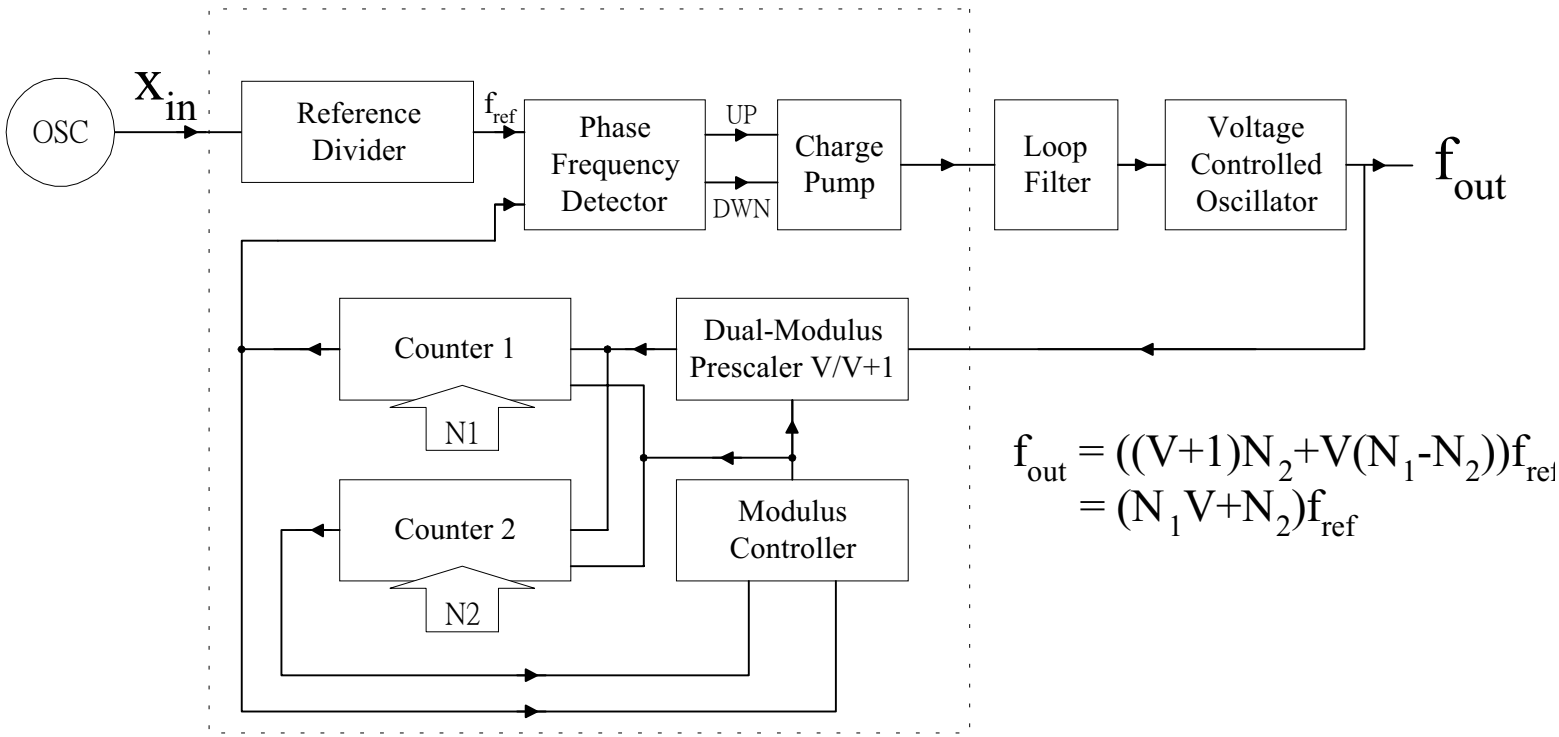


- With injection

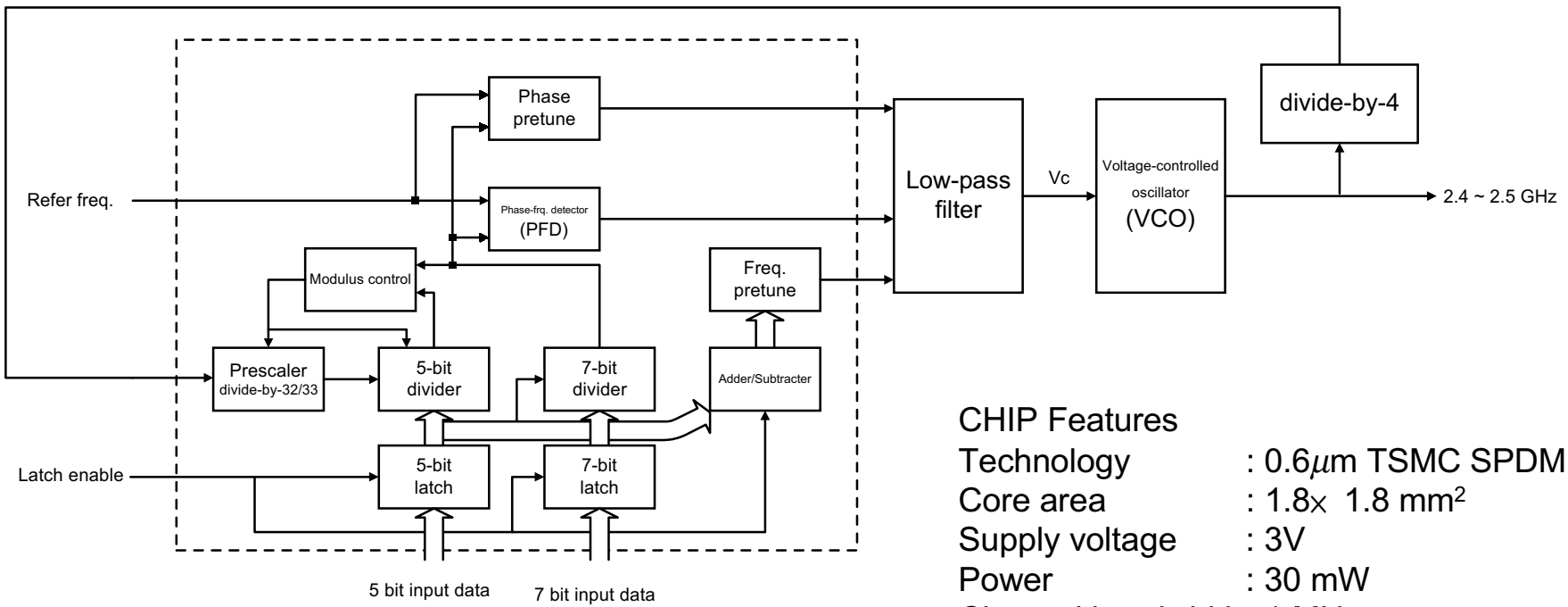


Finj=1408MHz -2.3dBm(165mv)

Frequency Synthesizer



Fast-switching frequency synthesizer

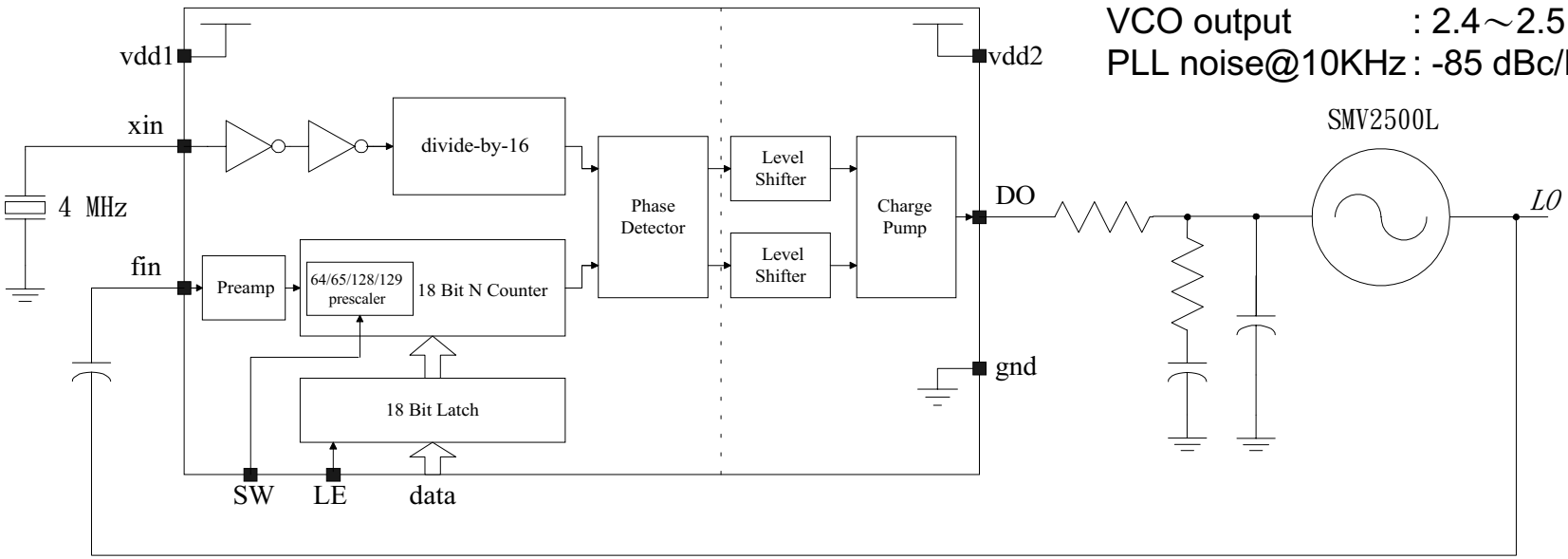


CHIP Features

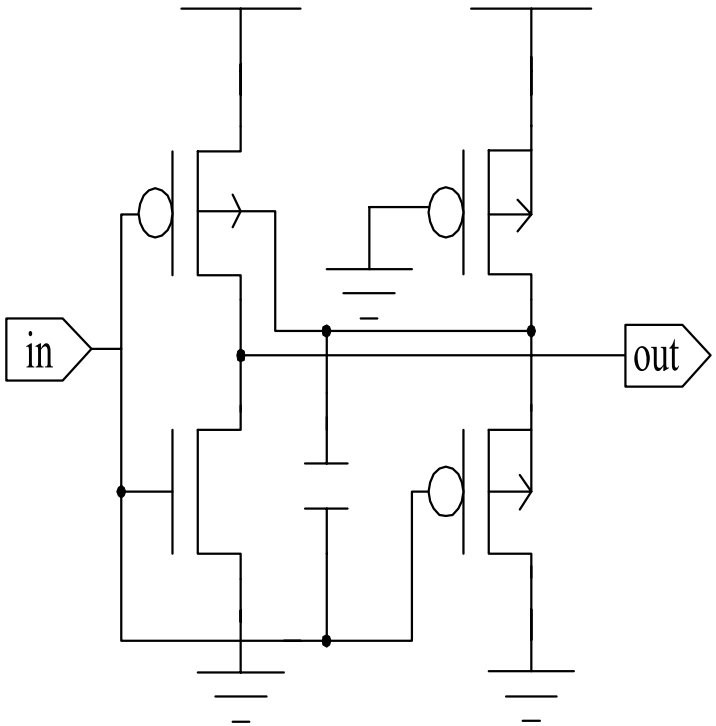
Technology	: 0.6μm TSMC SPDM
Core area	: 1.8× 1.8 mm^2
Supply voltage	: 3V
Power	: 30 mW
Channel bandwidth	: 1 MHz
Max. operating freq.	: ～600 MHz
VCO output	: 2.35～2.45 GHz
PLL noise@100KHz	: -95 dBc/Hz

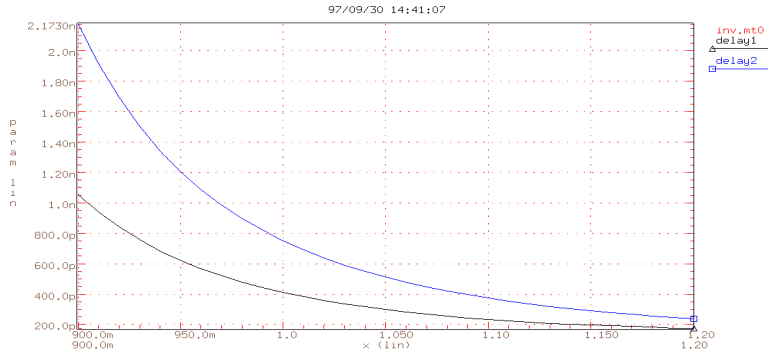
2.4GHz RF Frequency Synthesizer

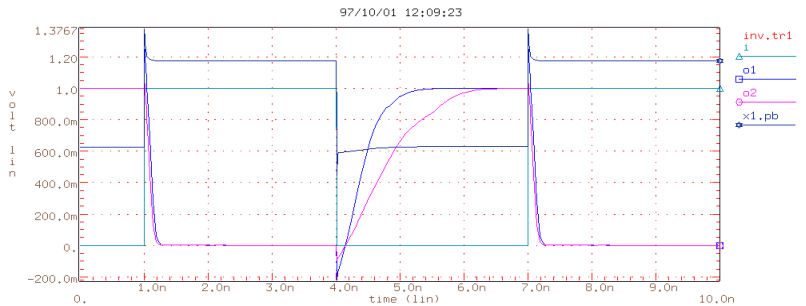
CHIP Features
Technology : 0.35μm DPDM
Core area : 750 × 350 μm^2
Supply voltage : 2.6 V
Channel bandwidth : 250 KHz
Max. operating freq. : ～2.5 GHz
VCO output : 2.4～2.5 GHz
PLL noise@10KHz : -85 dBc/Hz



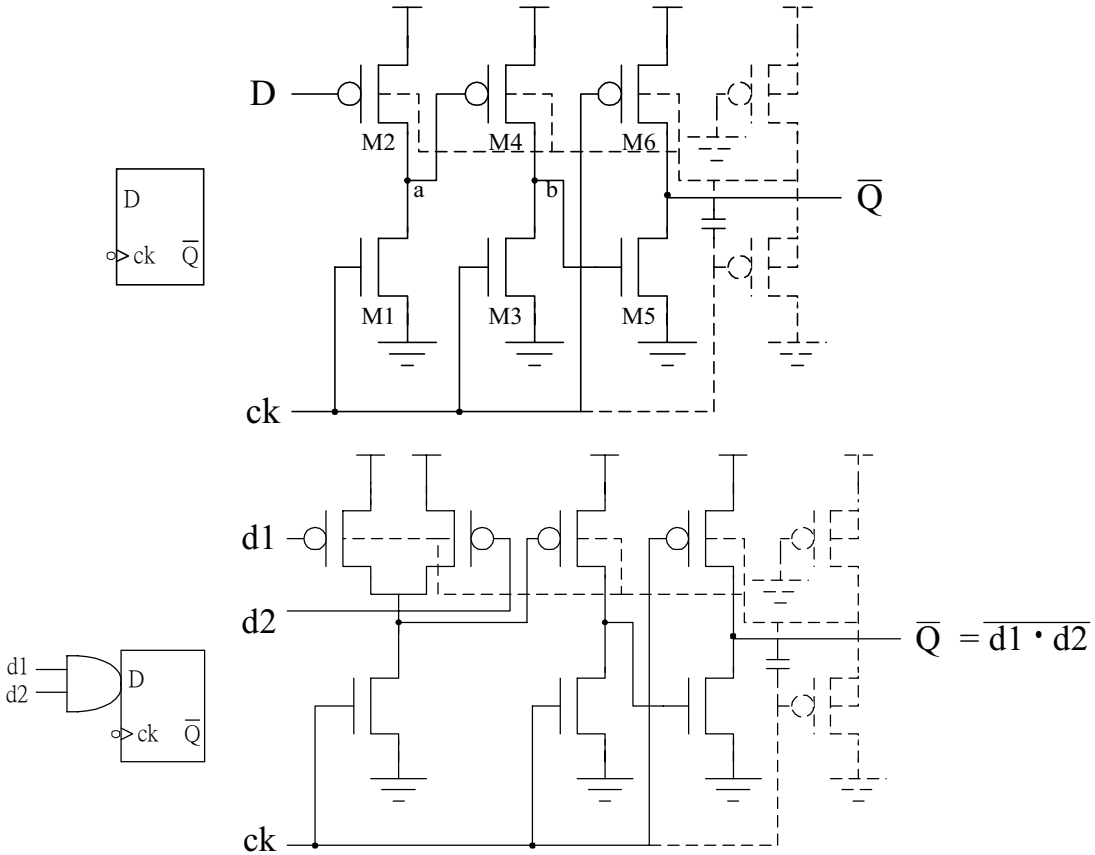
Proposed Dynamic Back Gate Forward Bias Inverter



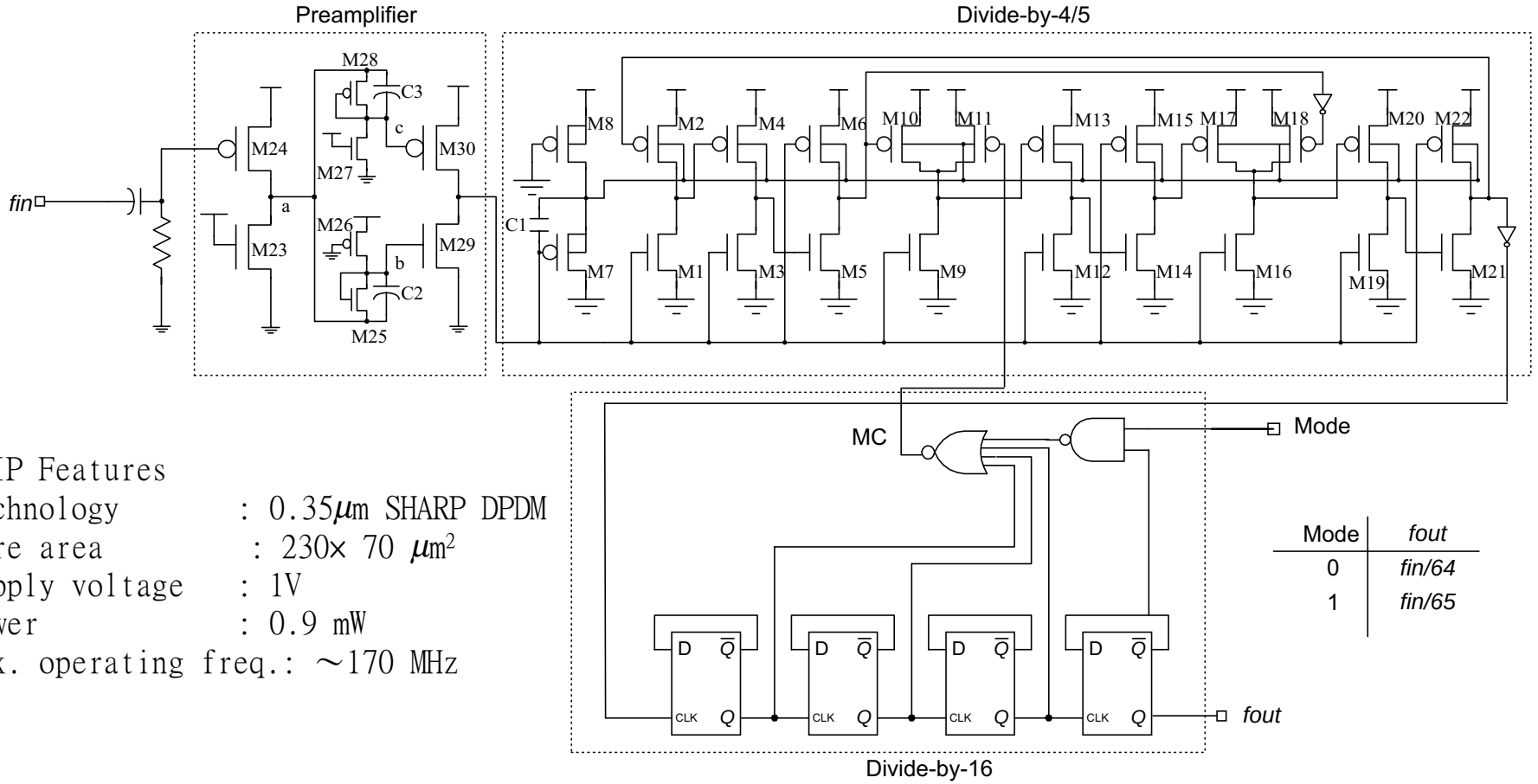




Proposed Dynamic Back Gate Forward Bias DFF and LFF



Dynamic Back Froward Bias Prescaler



CHIP Features

Technology	: 0.35μm SHARP DPDM
Core area	: 230× 70 μm^2
Supply voltage	: 1V
Power	: 0.9 mW
Max. operating freq.:	～170 MHz

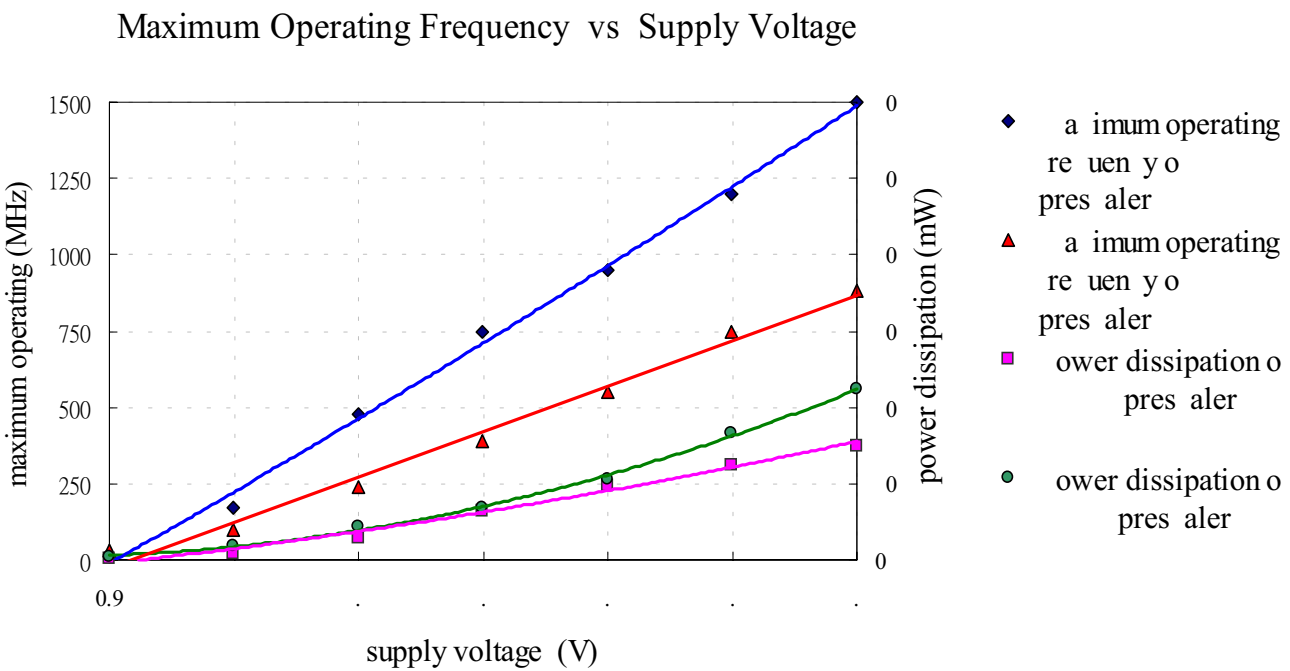
Mode	*fout*
0	*fin/64*
1	*fin/65*

Comparison and Conclusion

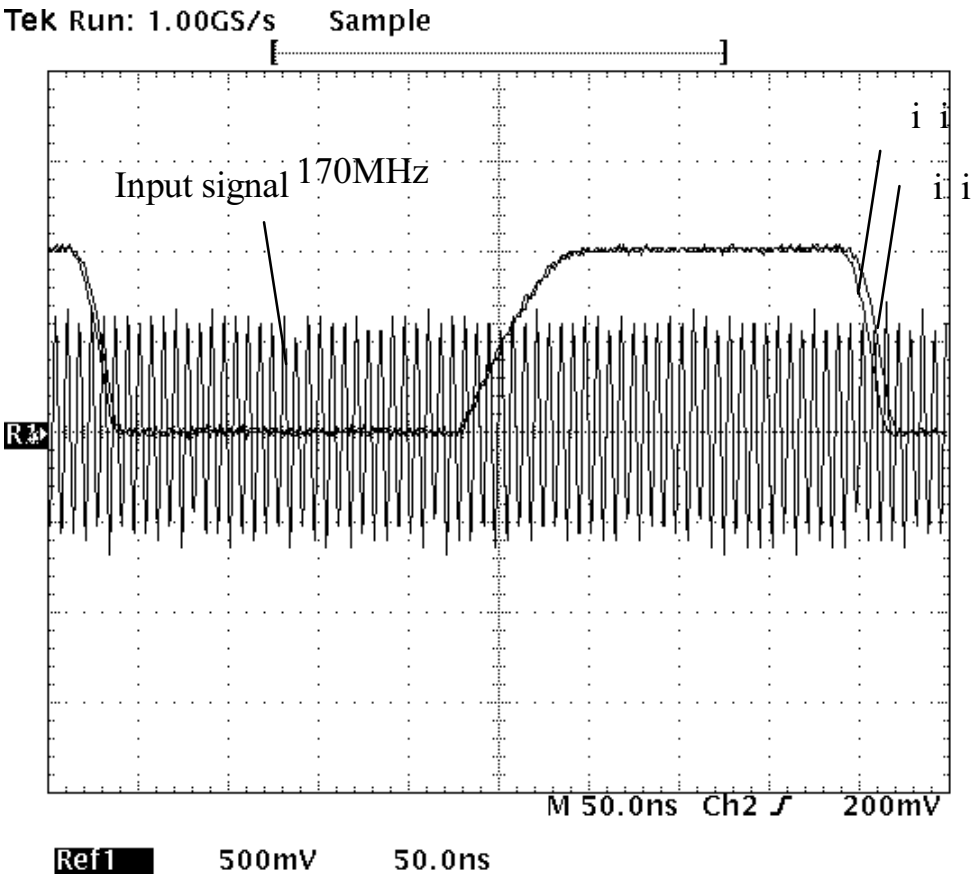
	Max operating freq	*Transistor count*	*Clocked transistor count*	*Total gate width*	*Power at max freq*
TSPC		41	9	580	
new	3 times faster	24+200fF	7+200fF	311+200fF	Equal to TSPC

- Advantage: Low voltage , High frequency
- Disadvantage: sensitive to technology, more static power dissipation

Measured max. operating freq. and power versus supply voltage

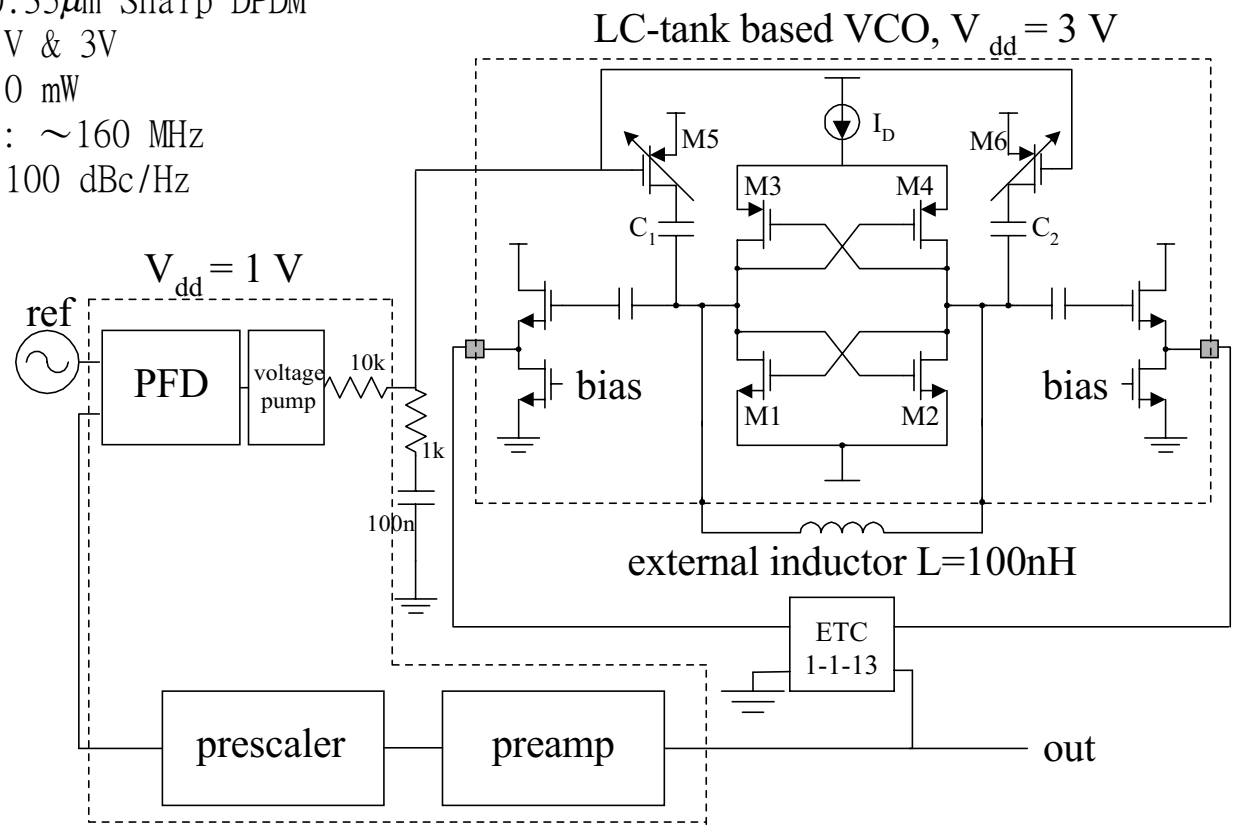


Measured prescaler input and output waveforms



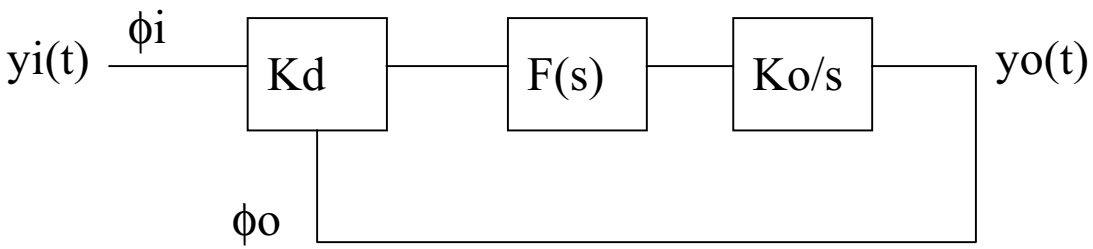
1V CMOS Synthesizer

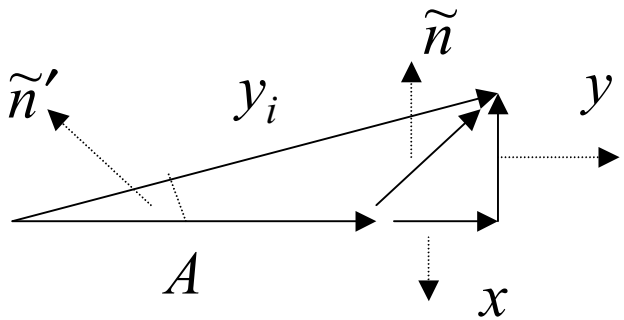
CHIP Features
Technology : 0.35μm Sharp DPDM
Supply voltage : 1V & 3V
Power : 10 mW
Max. operating freq.: ~160 MHz
PLL noise@100KHz : -100 dBc/Hz



Additive Noise Response of the Loop

$$y_i(t) = v_i + \tilde{n} = A\sin(\omega\ t) + \tilde{n}$$





$\tilde{n}$ is a white noise with noise bandwidth Bi and noise power spectral density No

$$\tilde{n} = \tilde{n}_x + \tilde{n}_y$$

$$\tilde{n}_x = x\sin(\omega\ t) \qquad \tilde{n}_y = y\cos(\omega\ t)$$

$$\overline{\tilde{n}}^2 = \overline{\tilde{n}_x}^2 + \overline{\tilde{n}_y}^2 = N_o B_i$$

Ref: A. Blanchard,

"Phase locked loops", 1976

$$\overline{\tilde{n}_x}^2 = \overline{\tilde{n}_y}^2 = N_o B_i / 2 \qquad \bar{x}^2 = \bar{y}^2 = N_o B_i$$

Additive Noise Response of the Loop

$$y_i(t) = A\sin(\omega\ t) + \tilde{n} = (A + x)\sin(\omega\ t) + y\cos(\omega\ t)$$

$$\because\ x << A,\quad y << A$$

$$y_i(t) \cong (A + x)\sin(\omega\ t + \tilde{n}') \quad \text{and} \quad \tilde{n}' = \tan^{-1}\left(\frac{y}{A+x}\right) \approx \tan^{-1}\left(\frac{y}{A}\right) \approx \frac{y}{A}$$

$$\overline{\tilde{n}'^2} = \frac{\overline{y}^2}{\overline{A}^2} = \frac{N_o B_i}{A^2}$$

is a stationary Gaussian noise with noise bandwidth Bi and noise power spectral density $\frac{N_o}{A^2}$

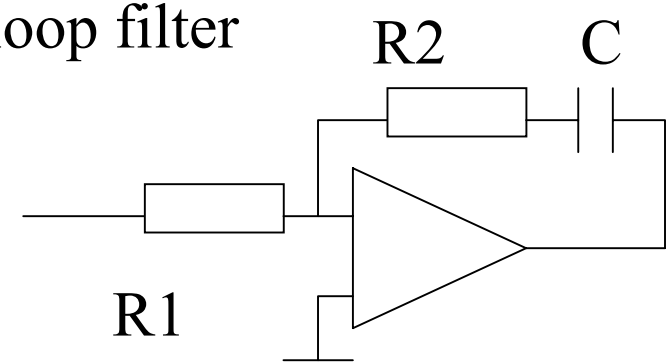
$$S_{\theta_o}(f) = S_{\theta_i}(f)\left|H(j2\pi f)\right|^2 = \frac{N_o}{A^2}\left|H(j2\pi f)\right|^2$$

It is the noise power spectral density of the output

Additive Noise Response of the Loop

$$\sigma_{\phi_o}{}^2 = \frac{N_o}{A^2}\int_{-B_i/2}^{B_i/2}\left|H(j2\pi f)\right|^2 df \approx \frac{N_o}{A^2}\int_{-\infty}^{\infty}\left|H(j2\pi f)\right|^2 df$$

The loop filter (1)



$$H(s) = \frac{KF(s)}{s + KF(s)} = \frac{K\tau_2 s + K}{\tau_1 s^2 + K\tau_2 s + K}$$

$$K = K_d K_o \quad \tau_1 = R_1 C \quad \tau_2 = R_2 C$$

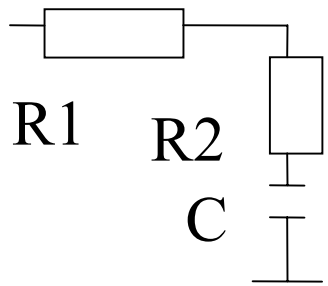
Additive Noise Response of the Loop

$$\omega_n^2 = \frac{K}{\tau_1} \quad 2\zeta\omega_n = \frac{K\tau_2}{\tau_1} \qquad H(s) = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\sigma_{\phi_o}^2 = \frac{N_o}{A^2}\int_{-\infty}^{\infty}\left|H(j2\pi f)\right|^2 df = \frac{N_o}{A^2}\frac{1}{2\pi}\int_{-\infty}^{\infty}\frac{\omega_n^4 + 4\zeta\omega_n^2\omega^2}{(\omega_n^2 - \omega^2)^2 + 4\zeta\omega_n^2\omega^2}d\omega$$

$$\sigma_{\phi_o}^2 = \frac{N_o}{A^2}\frac{\omega_n}{4\zeta}(1 + 4\zeta^2)$$

(2) The loop filter



Additive Noise Response of the Loop

$$H(s)=\frac{K\tau_2 s+K}{\tau_1 s^2+(1+K\tau_2)s+K} \qquad K=K_d K_o \quad \tau_1=(R_1+R_2)C \quad \tau_2=R_2C$$

$$\omega_n{}^2=\frac{K}{\tau_1} \quad 2\zeta\omega_n=\frac{1+K\tau_2}{\tau_1} \qquad H(s)=\frac{(2\zeta\omega_n-\omega_n{}^2/K)s+\omega_n{}^2}{s^2+2\zeta\omega_n s+\omega_n{}^2}$$

$$\sigma_{\phi_o}{}^2=\frac{N_o}{A^2}\frac{1}{2\pi}\int_{-\infty}^{\infty}\frac{\omega_n{}^4+(2\zeta\omega_n-\omega_n{}^2/K)^2\omega^2}{(\omega_n{}^2-\omega^2)^2+4\zeta\omega_n{}^2\omega^2}d\omega$$

$$\sigma_{\phi_o}{}^2=\frac{N_o}{A^2}\frac{\omega_n}{4\zeta}[1+(2\zeta-\frac{\omega_n}{K})^2]$$

Additive Noise Response of the Loop

$$B_n \equiv \int_0^\infty \left|H(j2\pi f)\right|^2 df$$ Noise Bandwidth

The loop filter (1) $$2B_n = \frac{\omega_n}{4\zeta}(1+4\zeta^2)$$

The loop filter (2) $$2B_n = \frac{\omega_n}{4\zeta}[1+(2\zeta - \frac{\omega_n}{K})^2]$$

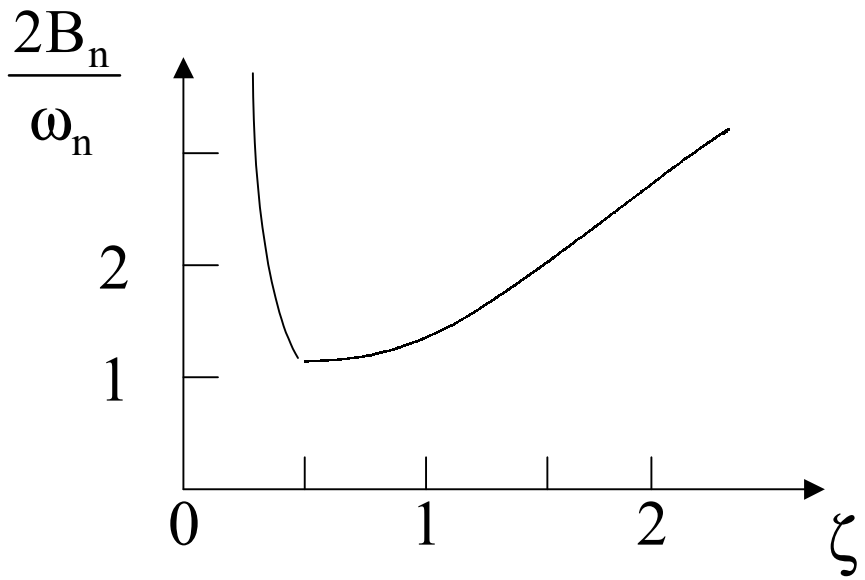
$$\sigma_{\phi_o}{}^2 = \frac{N_o}{A^2}(2B_n) \qquad \sigma_{\phi_i}{}^2 = \bar{\tilde{n}}'^2 = \frac{\bar{y}^2}{\bar{A}^2} = \frac{N_o B_i}{A^2}$$

$$SNR_i = \frac{\bar{v}_i{}^2}{\bar{n}^2} = \frac{A^2}{2N_o B_i} = \frac{1}{2\sigma_{\phi_i}{}^2} \qquad \Rightarrow SNR_o = \frac{1}{2\sigma_{\phi_o}{}^2} \equiv SNR_i \frac{B_i}{2B_n}$$

Additive Noise Response of the Loop

If K>>ωn, both cases give $2B_n \cong \frac{\omega_n}{4\zeta}(1+4\zeta^2)$

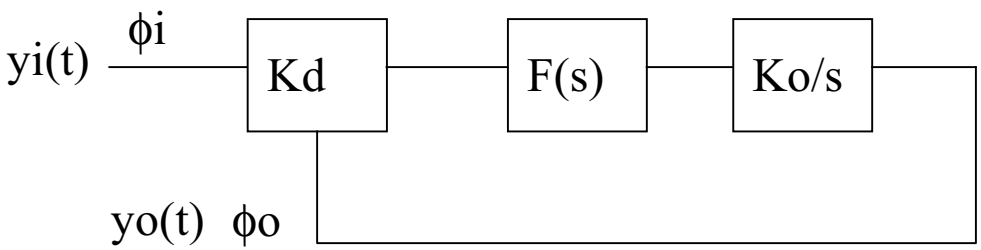
One can find $(2B_n)_{min} \cong \omega_n$ where $(\zeta)_{opt} = 0.5$



If $\zeta \in (0.25, 1)$, $2B_n < 1.25\omega_n$

It corresponds a 1dB loss for optimum $\sigma_{\phi_o}{}^2$

Response to Random Modulations



$$y_i(t) = A\sin(\omega t + \phi_i(t))$$

$$\phi_i(t) = \alpha(t) + \theta_i$$

$\alpha(t)$ is the random process having zero mean and θi is constant

$$y_o(t) = B\sin(\omega t + \theta_i + \phi_o(t))$$

The phase error $\phi(t) = \alpha(t) - \phi_o(t)$

Response to Random Modulations

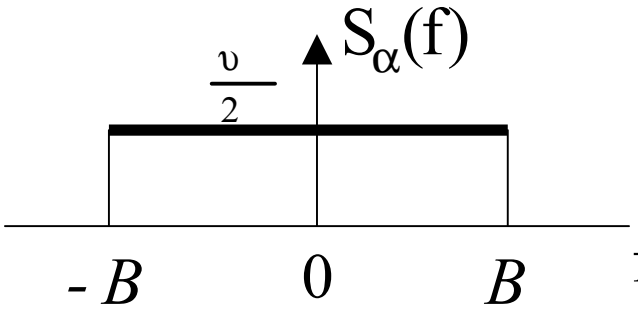
$$S_{\phi_o}(f) = S_\alpha(f)\left|H(j2\pi f)\right|^2 \qquad S_\phi(f) = S_\alpha(f)\left|1 - H(j2\pi f)\right|^2$$

Since H(jω) and 1-H(jω) are linear filters, if α(t) is the stationary Gaussian process, process ϕ(t) and ϕo(t) are also stationary Gaussian processes.

$$\overline{\phi_o(t)} = \overline{\alpha(t)} = \overline{\phi(t)} = 0$$

$$\sigma_{\phi_o}{}^2 = \int_{-\infty}^{\infty} S_\alpha(f)\left|H(j2\pi f)\right|^2 df \qquad \sigma_\phi{}^2 = \int_{-\infty}^{\infty} S_\alpha(f)\left|1 - H(j2\pi f)\right|^2 df$$

Phase Mod. by a Gaussian white noise

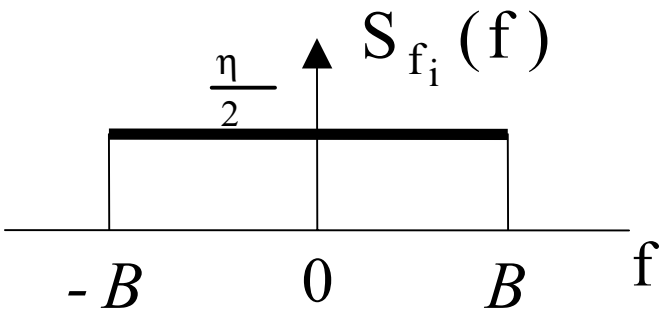


$$S_\alpha(f) = \frac{\upsilon}{2} \quad (\text{rad}^2/\text{Hz})$$

$$\sigma_{\phi_o}{}^2 = \frac{\upsilon}{2}\int_{-\infty}^{\infty}\left|H(j2\pi f)\right|^2 df = \frac{\upsilon}{2}(2B_n) \qquad \sigma_{\phi}{}^2 = \frac{\upsilon}{2}\int_{-\infty}^{\infty}\left|1-H(j2\pi f)\right|^2 df$$

One must choose H(s) so that $\sigma_{\phi_o}{}^2$ is as small as required

Freq. Mod. by a Gaussian white noise



$$S_{f_i}(f) = \frac{\eta}{2} \quad (\text{Hz}^2/\text{Hz})$$

$$S_{\alpha}(f) = \frac{\eta}{2}\frac{1}{f^2} \quad (\text{rad}^2/\text{Hz})$$

If the loop filter is $F(s) = \dfrac{1 + j\omega\tau_2}{1 + j\omega\tau_1}$

$$\sigma_\phi^2 = \frac{\eta}{2}\frac{\pi}{\zeta\omega_n}\left(1 + \frac{\omega_n^2}{K^2}\right) \quad \text{if} \quad 2\pi B >> \omega_n$$

If the condition is not fulfilled, the phase error is smaller than the above quantity

If the loop filter is $F(s) = \dfrac{1 + j\omega\tau_2}{j\omega\tau_1}$

$$\sigma_\phi^2 = \frac{\eta}{2}\frac{\pi^2}{\zeta\omega_n}$$

The conclusion: $\omega_n \nearrow \quad \sigma_\phi^2 \searrow$

Freq. Mod. by a Gaussian flicker noise

The power spectral density of fi(t)

$$S_{f_i}(f) = \frac{\xi}{\varepsilon} \quad |f| < \varepsilon$$
$$= \frac{\xi}{|f|} \quad \varepsilon < |f| < B$$
$$= 0 \quad \text{elsewhere}$$

The power spectral density of input phase α(t)

$$S_{\alpha}(f) = \frac{\xi}{\varepsilon}\frac{1}{f^2} \quad |f| < \varepsilon$$
$$= \frac{\xi}{|f|f^2} \quad \varepsilon < |f| < B$$
$$= 0 \quad \text{elsewhere}$$

The noise power of output phase error ϕ(t)

$$\sigma_{\phi}^2 = 4\pi \int_0^{2\pi\varepsilon} \frac{\xi}{\varepsilon} \frac{|1-H(j\omega)|^2}{\omega^2} d\omega + 8\pi^2 \int_{2\pi\varepsilon}^{\infty} \xi \frac{|1-H(j\omega)|^2}{\omega^3} d\omega$$

Freq. Mod. by a Gaussian flicker noise

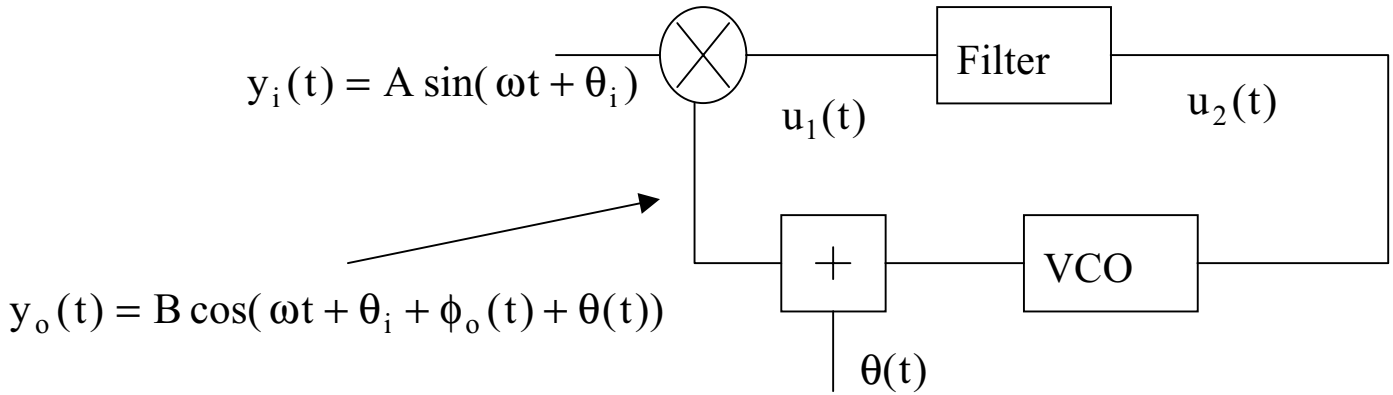
If the loop filter is $F(s) = \dfrac{1 + j\omega\tau_2}{j\omega\tau_1}$ and $\zeta > 1$,

When $2\pi\varepsilon \rightarrow 0$ and $K^2 >> \ln(\omega_n^2 / 2\pi\varepsilon)$,

$$\sigma_\phi^2 = \xi \frac{4\pi^2}{\omega_n^2} f(\zeta) \quad \text{where} \quad f(\zeta) = \begin{cases} \dfrac{\ln(\zeta + \sqrt{\zeta^2 - 1})}{\zeta\sqrt{\zeta^2 - 1}} & \zeta > 1 \\ 1 & \zeta = 1 \\ \dfrac{\text{Arc}\tan(\sqrt{1-\zeta^2}\,/\,\zeta)}{\zeta\sqrt{1-\zeta^2}} & \zeta < 1 \end{cases}$$

The conclusion: $\omega_n \nearrow \quad \sigma_\phi^2 \searrow$

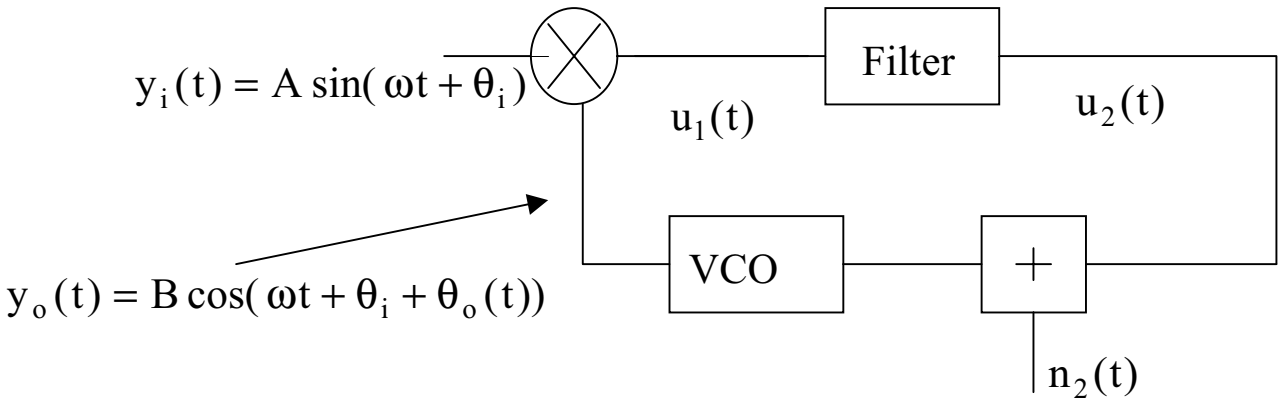
Influence of VCO Modulation



$$\frac{\Phi_o(s)}{\Theta(s)} = \frac{-KF(s)}{s + KF(s)} = -H(s)$$

$$\because \Theta_o(s) = \Phi_o(s) + \Theta(s) \qquad \therefore \frac{\Theta_o(s)}{\Theta(s)} = 1 - H(s)$$

Influence of VCO Modulation



$$\frac{\Theta_o(s)}{N_2(s)} = \frac{K_V}{s + KF(s)}$$ where K_V is the gain of VCO

For the loop being opened, $s\Theta(s) = K_V N_2(s)$

$$\Theta_o(s) = \frac{s\Theta(s)}{s + KF(s)} = (1 - H(s))\Theta(s)$$ Two cases are equivalent

Parameter Optimization

- input signal frequency modulation
- additive noise
- VCO signal frequency modulation

$$\sigma_\phi^2 = \int_{-\infty}^{\infty} S_{\phi_i}(f)\left|1-H(j2\pi f)\right|^2 df + \int_{-\infty}^{\infty} \frac{N_o}{A^2}\left|H(j2\pi f)\right|^2 df + \int_{-\infty}^{\infty} S_\theta(f)\left|1-H(j2\pi f)\right|^2 df$$

- FMs of the input signal and VCO signal can be expressed as

$$S_{f_i}(f) = \frac{\eta}{2} + \frac{\xi}{|f|} \qquad S_{f_\theta}(f) = \frac{\eta'}{2} + \frac{\xi'}{|f|}$$

That implies

$$S_{\varphi_i}(f) = \frac{\eta}{2f^2} + \frac{\xi}{|f|f^2} \qquad S_\theta(f) = \frac{\eta'}{2f^2} + \frac{\xi'}{|f|f^2}$$

Parameter Optimization

$$\sigma_\phi{}^2 = \frac{N_o}{A^2}\frac{\omega_n(1+4\zeta^2)}{4\zeta} + \frac{\eta+\eta'}{2}\frac{\pi^2}{\zeta\omega_n} + (\xi+\xi')\frac{4\pi^2}{\omega_n{}^2}f(\zeta)$$

- If the flicker noise is negligible compared with FM white noise

$$\sigma_\phi{}^2 = \frac{N_o}{A^2}\frac{\omega_n(1+4\zeta^2)}{4\zeta} + \frac{\eta+\eta'}{2}\frac{\pi^2}{\zeta\omega_n}$$

$$\sigma_{\phi\min}{}^2 = 2\frac{N_o}{A^2}\frac{\omega_{n,opt}(1+4\zeta^2)}{4\zeta} = 2\frac{\eta+\eta'}{2}\frac{\pi^2}{\zeta\omega_{n,opt}}$$

$$\omega_{n,opt}{}^2 = \frac{\eta+\eta'}{2}\frac{A^2}{N_o}\frac{4\pi^2}{1+4\zeta^2}$$

Parameter Optimization

- If the parasitic FM of the signals are due to flicker noise

$$\sigma_\phi^{\,2} = \frac{N_o}{A^2}\frac{\omega_n(1+4\zeta^2)}{4\zeta} + (\xi+\xi')\frac{4\pi^2}{\omega_n^{\,2}} f(\zeta)$$

$$\omega_{n,opt}^{\,3} = \frac{2Y}{X} \text{ where } X = \frac{N_o}{A^2}\frac{1+4\zeta^2}{\zeta} \text{ and } Y = 4\pi^2(\xi+\xi')f(\zeta)$$

$$\sigma_{\phi\min}^{\,2} = \frac{3X}{2}\omega_{n,opt} = \frac{3Y}{\omega_{n,opt}^{\,2}}$$

Example

SNR of the second-order PLL is $\frac{A^2}{N_o} = 2x10^4$ with $F(s) = \frac{1 + j\omega\tau_2}{j\omega\tau_1}$ and $\zeta = 1$

For $\omega_n = 40\,\text{rad/s}$, the min. phase error is $\sigma_{\min}{}^2 = 1.4x10^{-2}\,\text{rad}$.

If the input signal is perfectly stable, what kind of the signal frequency modulated the VCO?

- If the noise is white noise,

$$\omega_{n,opt}{}^2 = \frac{\eta'}{2}\frac{A^2}{N_o}\frac{4\pi^2}{1+4\zeta^2}$$

$$\sigma_{\phi\min}{}^2 = 2\frac{\eta'}{2}\frac{\pi^2}{\zeta\omega_{n,opt}}$$

$$\frac{\eta'}{2} = 10^{-2} \text{ and } \sigma_{\phi\min}{}^2 = 5x10^{-3}$$

- If the noise is flicker noise,

$$\xi' = \frac{1}{8\pi^2}\frac{N_o}{A^2}\frac{1+4\zeta^2}{\zeta}\omega_{n,opt}{}^3$$

$$\sigma_{\phi\min}{}^2 = \frac{3}{2}\frac{N_o}{A^2}\frac{1+4\zeta^2}{\zeta}\omega_{n,opt}$$

$$\frac{\xi'}{2} = 0.2 \text{ and } \sigma_{\phi\min}{}^2 = 1.5x10^{-2}$$

$\therefore$ The VCO is frequency-modulated by a flicker noise having a spectral density $S_{f_o}(f) = \frac{0.2}{|f|}(\text{Hz}^2/\text{Hz})$

Self-Calibrating Frequency Synthesizer

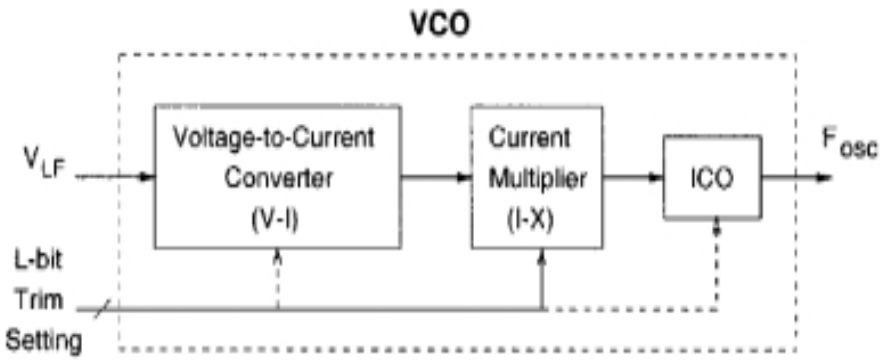


Fig. 3. Digitally programmable VCO.

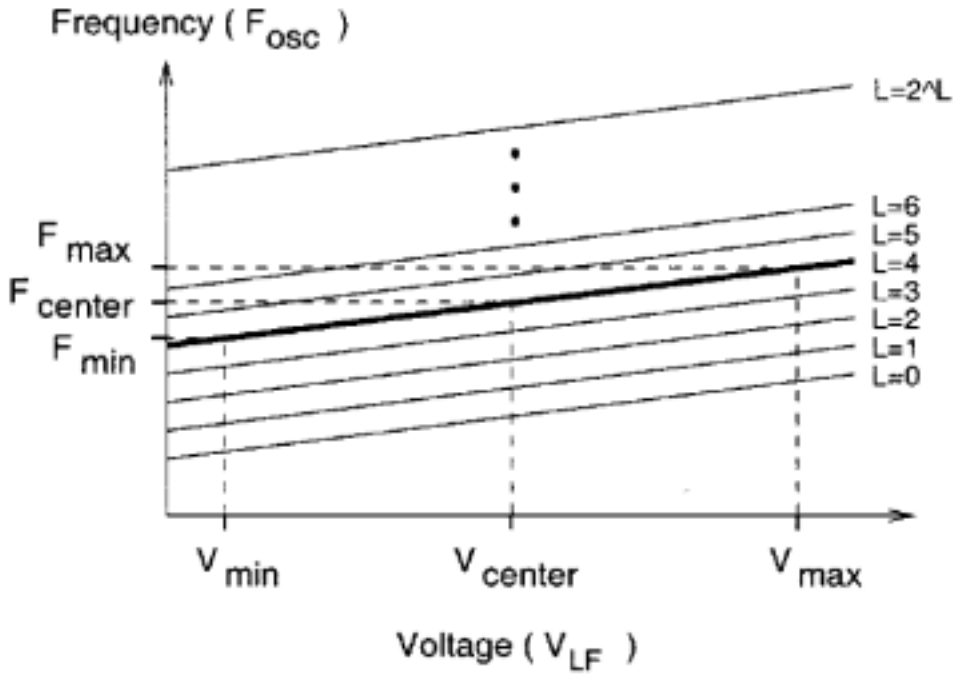
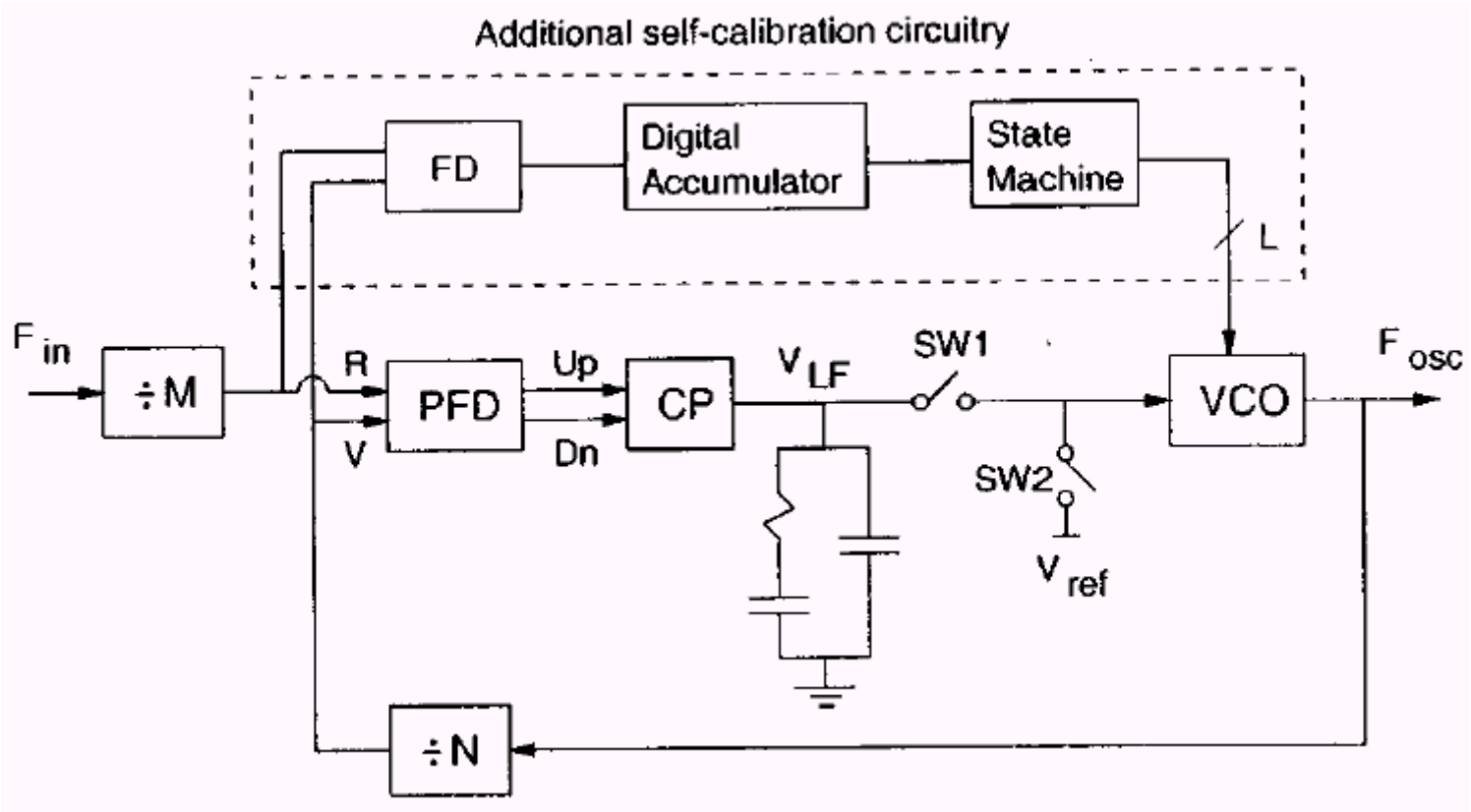


Fig. 4. 2^L operating modes of VCO.

Self-Calibrating Frequency Synthesizer



IEEE JSSC-35, pp. 1437-, Oct. 2000

Adaptive Bandwidth PLLs using Regulated Supply CMOS Buffers

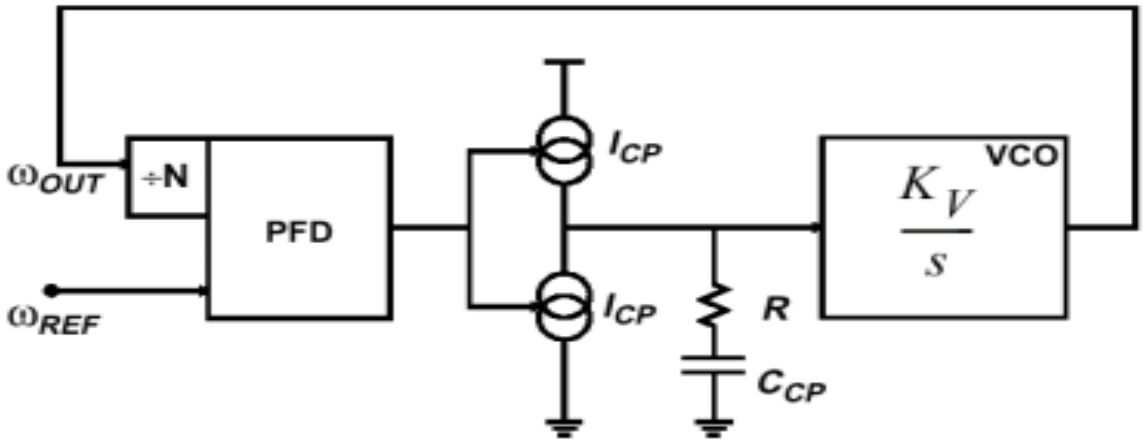


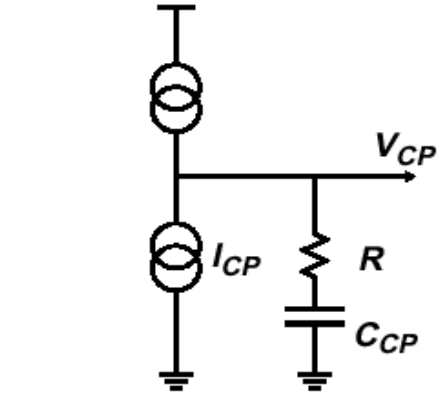
Figure 5: Conventional PLL block diagram

$$H(s) = N \cdot \frac{1 + 2 \cdot \zeta \cdot s/\omega_B}{1 + 2 \cdot \zeta \cdot s/\omega_B + (s/\omega_B)^2}$$

where the loop damping factor ζ and bandwidth ω_B are given by:

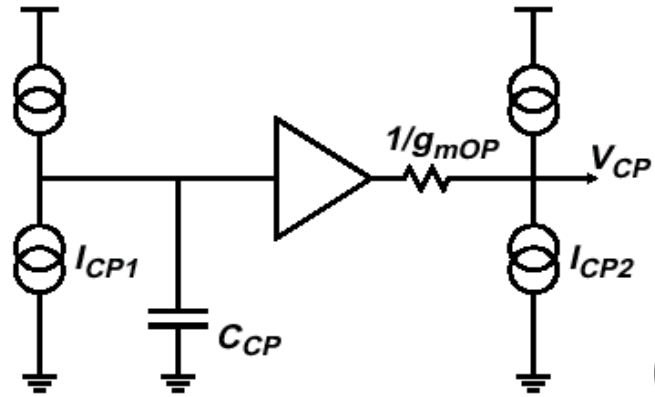
$$\zeta = 0.5 \cdot R \cdot \sqrt{I_{CP} \cdot K_V \cdot C_{CP}/N} \quad \text{and} \quad \omega_B = 2 \cdot \zeta/(R \cdot C_{CP})$$

IEEE Symposium on VLSI Circuits, pp. 124, 2000



$$V_{CP}(t) = \frac{\int_0^t I_{CP}(\tau)d\tau}{C_{CP}} + I_{CP}(t) \cdot R$$

(a)

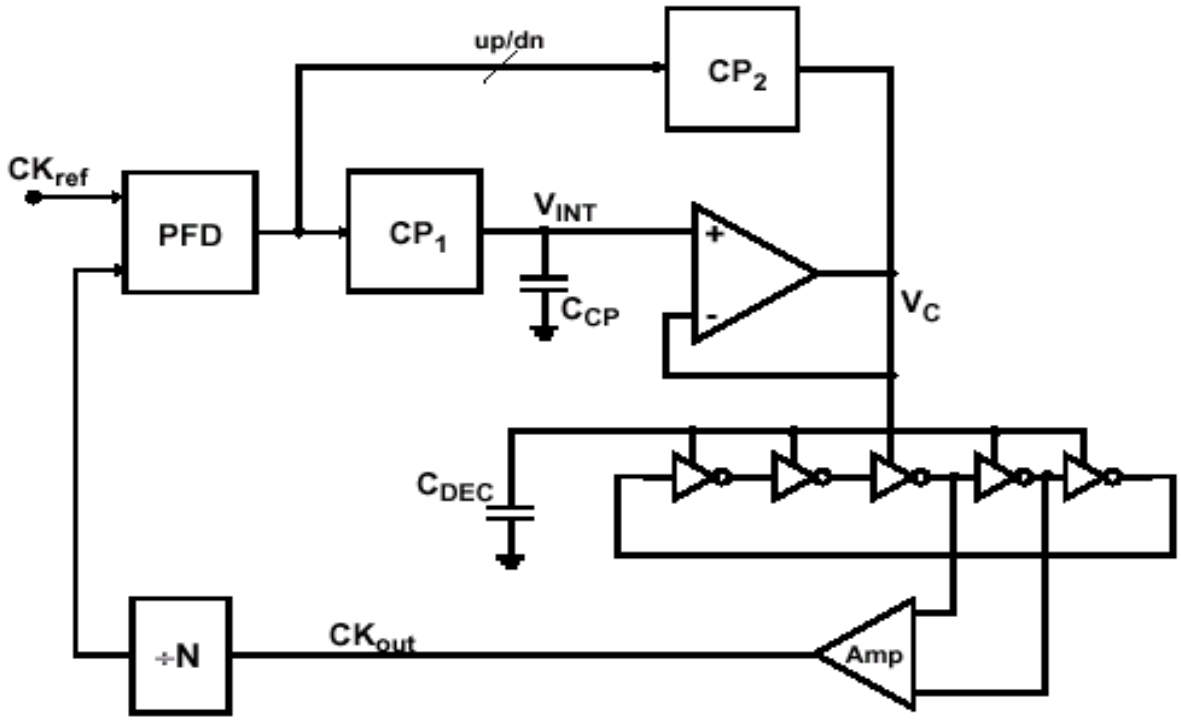


$$V_{CP}(t) = \frac{\int_0^t I_{CP1}(\tau)d\tau}{C_{CP}} + \frac{I_{CP2}(t)}{g_{mOP}}$$

(b)

Figure 6: Implementing the PLL stabilizing zero

Adaptive Bandwidth PLLs using Regulated Supply CMOS Buffers



$$R_{op} = \frac{1}{g_{mop}} = \frac{1}{k_{OP} \cdot g_{mBUF}} \qquad g_{mBUF} \propto \beta(V_C - V_T) \qquad I_{CP} = k_{CP}\beta(V_C - V_T)^2$$

where g_{mBUF} is the transconductance of the buffer biased at Vc

$$Freq = \frac{1}{g_{mop}} = \frac{g_{mBUF}}{2nC_{LD}N} \qquad K_V \propto \frac{\beta}{C_{LD}}$$

where C_{LD} is the load of the buffer *and* K_V is the gain of VCO

N is the divider's vlaue and n is the no. of BUFs to form the VCO

$$\omega_B \propto n \cdot Freq \cdot \sqrt{k_{CP} \cdot N \cdot \frac{C_{LD}}{C_{CP}}} \qquad \zeta \propto \frac{1}{k_{OP}} \cdot \sqrt{\frac{k_{CP}}{N} \cdot \frac{C_{CP}}{C_{LD}}}$$

The process and environmental condition dependent terms *(Vt* , β) cancel, and the loop bandwidth tracks the operating frequency.

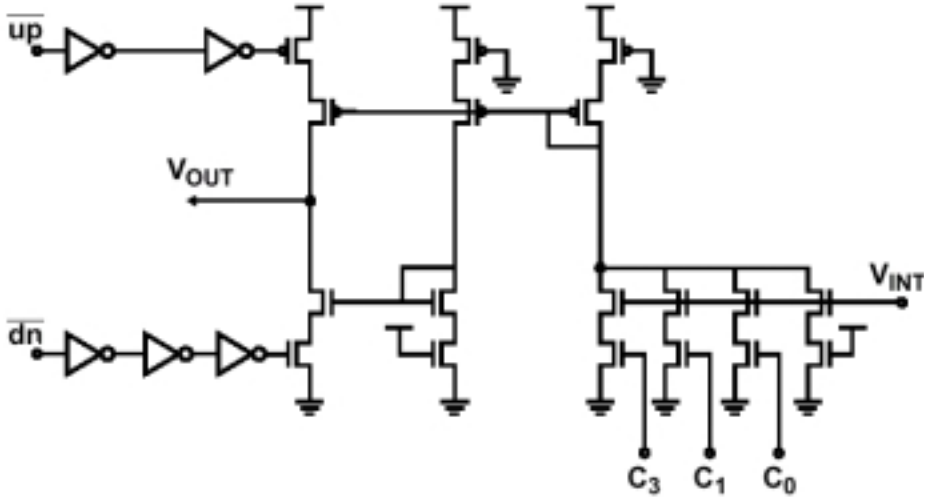


Figure 8: Charge pump schematic

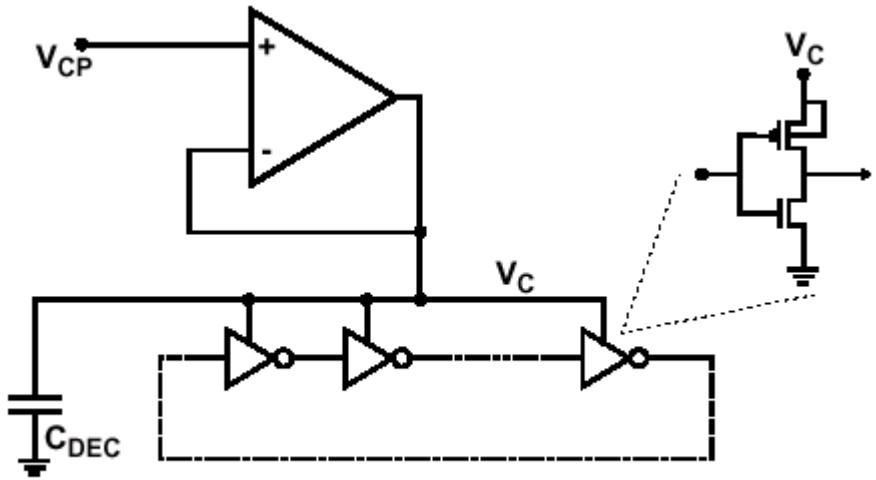


Figure 1: VCDL and VCO design

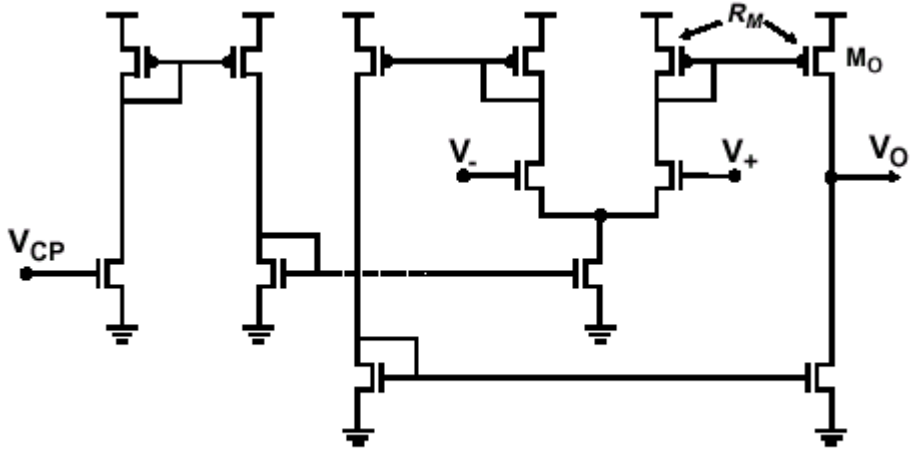


Figure 2: Regulating amplifier

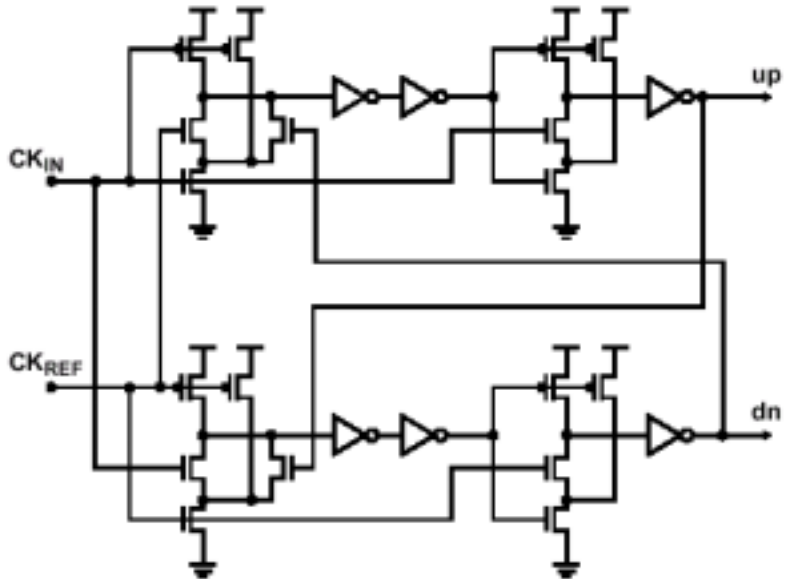


Figure 4: Core DLL phase detector

Fast-switching Frequency Synthesizer

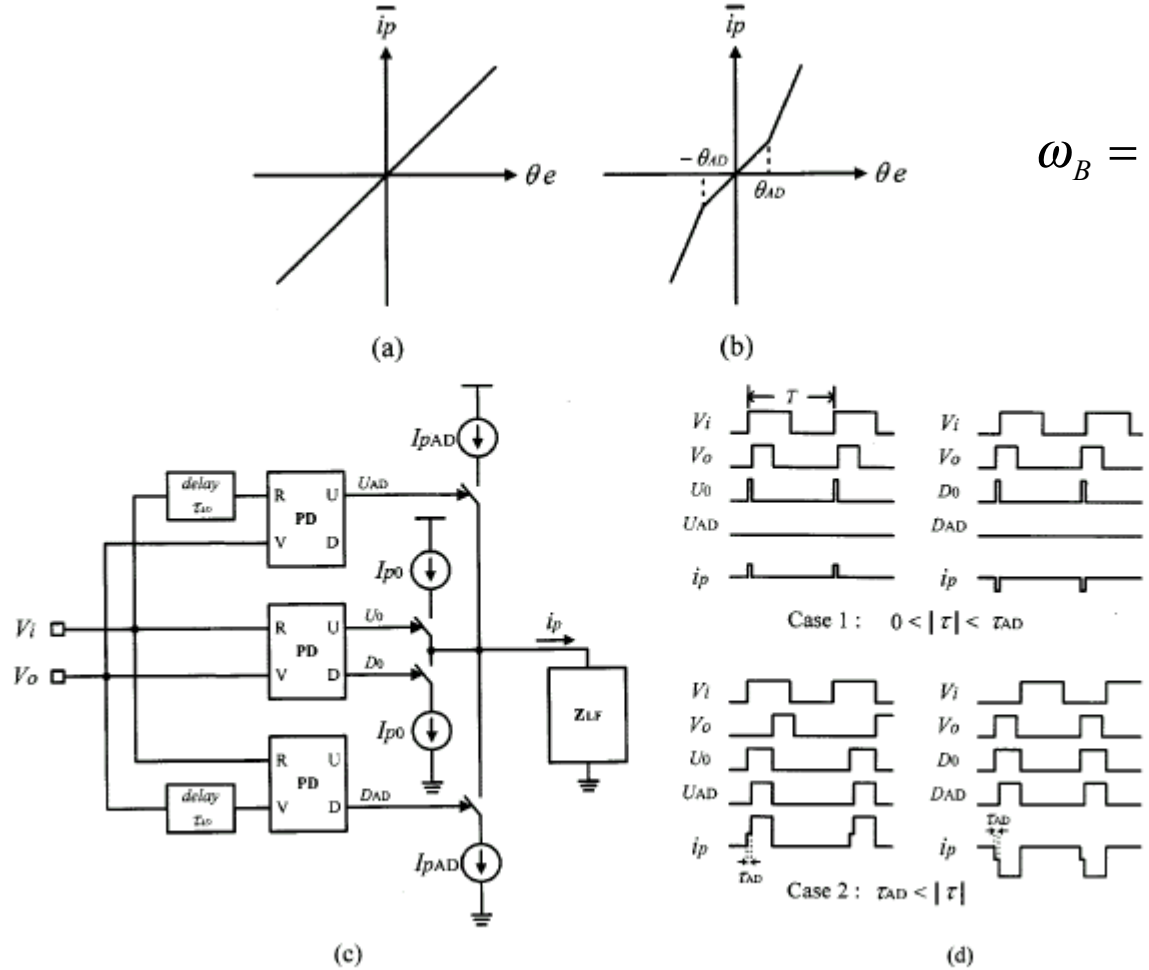


Fig. 4. (a) Characteristic of the conventional linear phase detector. (b) Characteristic of the nonlinear phase detector. (c) Block diagram of the nonlinear phase detector. (d) Operation of the nonlinear phase detector.

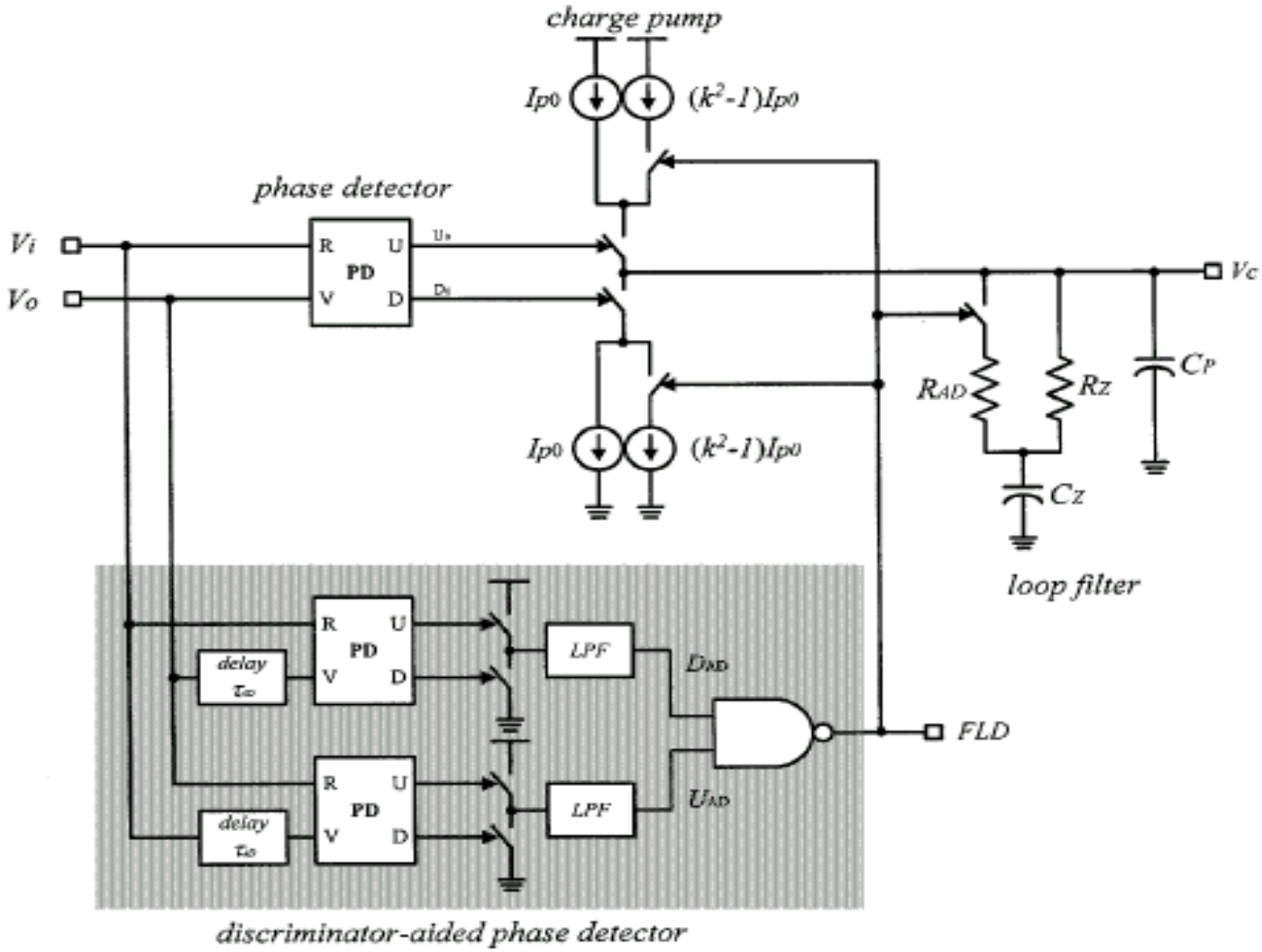
$$\omega_B = \sqrt{\frac{I_{CP} \cdot K_V}{C_{CP} \cdot N}} \quad and \quad \zeta = \frac{R}{2} \cdot \sqrt{\frac{I_{CP} \cdot K_V \cdot C_{CP}}{N}}$$

For constant phase margin,

$$\zeta \Rightarrow \text{constant}, \qquad \omega_B \Rightarrow k\omega_B$$

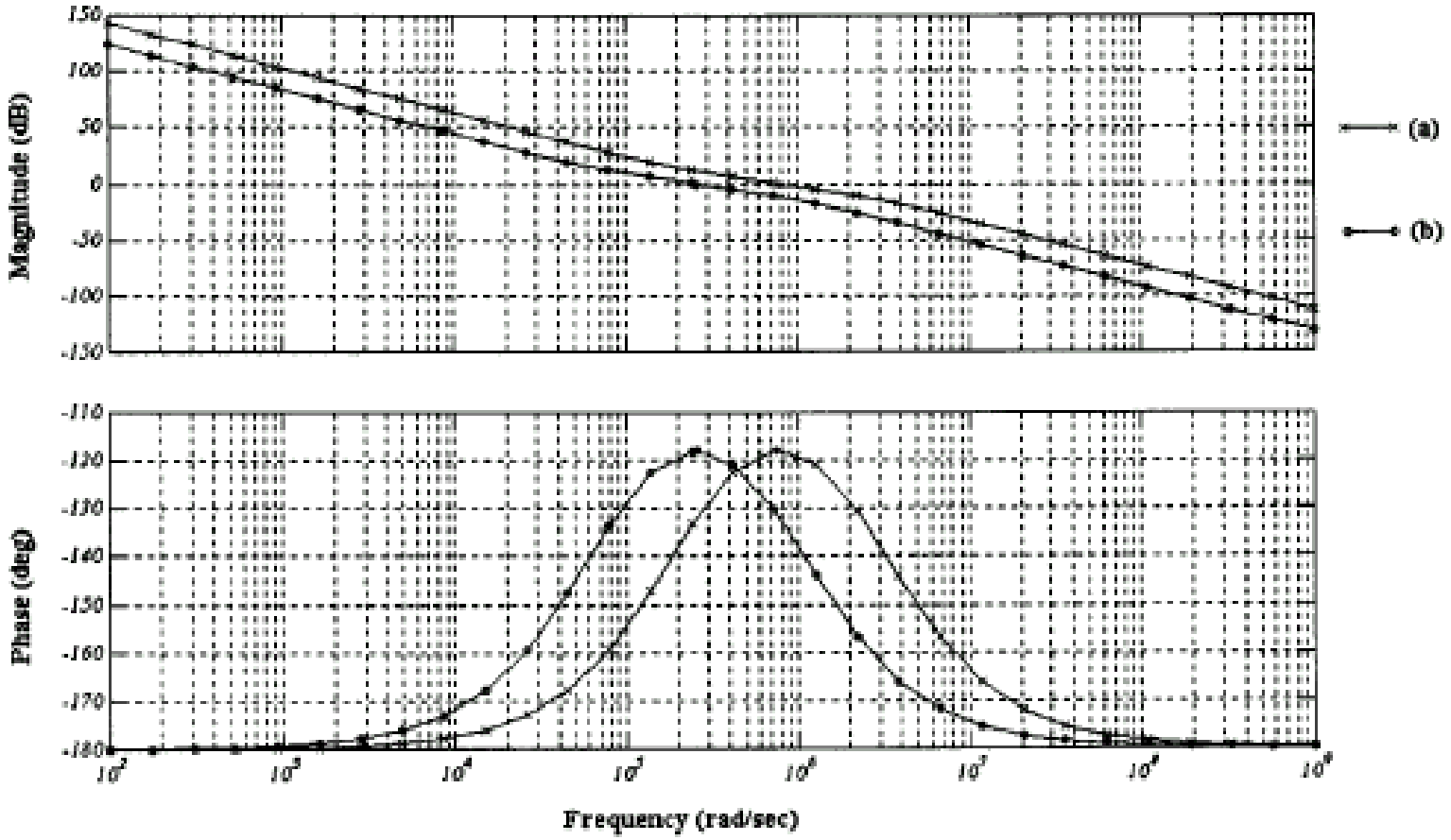
$$If \quad I_{CP} \Rightarrow k^2 \cdot I_{CP}$$

$$then \quad R \Rightarrow \frac{R}{k}$$



IEEE JSSC-35, pp. 1445-, Oct. 2000

Case, k=3 (from BW=120kHz to BW=40kHz)



Z-domain Digital Phase-Locked Loop

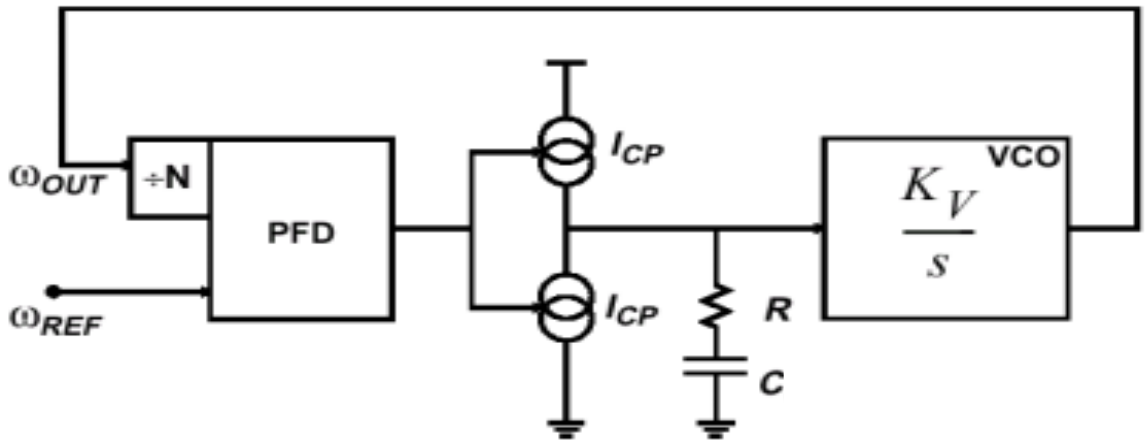


Figure 5: Conventional PLL block diagram

$$loop\ gain = K_p \cdot \frac{K_V}{s} \cdot F(s) \qquad if\ K_p = PFD's\ gain, N = 1$$

IEEE CAS-35, pp. 1391-, Nov. 1988

$$loop\ gain = \frac{K_p \cdot K_V}{C} \cdot (\frac{1}{s^2} + \frac{RC}{s})$$

By taking inverse Laplace transform

$$h_a(t) = \frac{K_p \cdot K_V}{C} \cdot [t + RC] \cdot u(t)$$

By impulse-invariant property

$$h[n] = h_a[nT] = \frac{K_p \cdot K_V}{C} \cdot [nT + RC] \cdot u[n]$$

By taking Z-transform

$$H(z) = \frac{K_p \cdot K_V}{C} \cdot [\frac{Tz^{-1}}{1 - z^{-1}} + \frac{RC}{1 - z^{-1}}]$$

where T is the sampling period
or input frequency

$$If\ \alpha = 1 - \frac{T}{RC}$$

$$H(z) = R \cdot K_p \cdot K_V \cdot \frac{z(z - \alpha)}{(z - 1)^2}$$

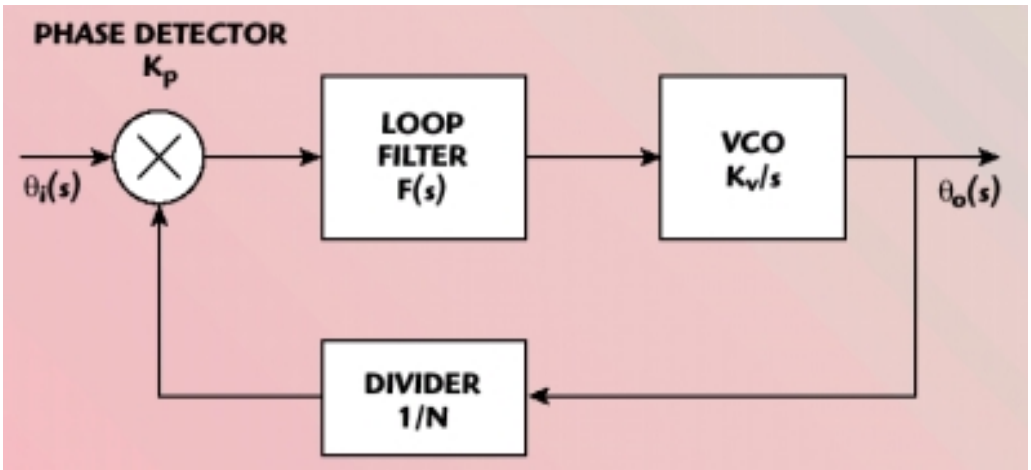
The closed loop transfer function

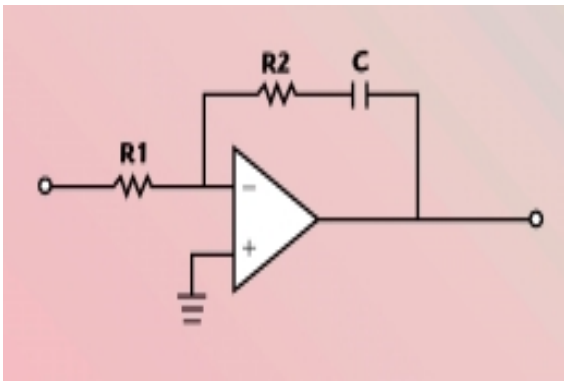
$$H_d(z) = \frac{H(z)}{1 + H(z)} = \frac{K}{1 + K} \cdot \frac{z(z - \alpha)}{z^2 - \frac{2 - \alpha K}{1 + K} z + \frac{1}{1 + K}}$$

$$K = R \cdot K_p \cdot K_V$$

$$K_p = \frac{\overline{I_{CP}}}{2\pi} = \frac{I_{CP}}{2\pi f_{VCO}}$$

Approximated Z-domain Digital Phase-Locked Loop





$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{K_p F(s)\frac{K_v}{s}}{1+\frac{1}{N}K_p F(s)\frac{K_v}{s}}$$

$$F(s) = \frac{-R2}{R1} - \frac{1}{sCR1}$$

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By applying $s \to \dfrac{z-1}{T_s}$

$$F(z) = -K_1 - K_2 \cdot \frac{z^{-1}}{1-z^{-1}}$$

$$K_1 = \frac{R_2}{R_1},\ K_2 = \frac{T_s}{CR_2}$$

$$H(z) = \frac{K_p F(z) K_v \left(\dfrac{T_s z^{-1}}{1-z^{-1}}\right)}{1 + \dfrac{K_p F(z) K_v}{N}\left(\dfrac{T_s z^{-1}}{1-z^{-1}}\right)}$$

$$H(z) = \frac{K_p K_v T_s (K1-K2) z^{-2} - (K_p K_v T_s K1) z^{-1}}{\left[1 + \dfrac{K_p K_v T_s (K1-K2)}{N}\right] z^{-2} + \left(-2 - \dfrac{K_p K_v T_s K1}{N}\right) z^{-1} + 1}$$

$$H(s) \to s = \frac{z-1}{T_S}$$

$$H(z) = \frac{\left(-2\omega_n \zeta T_s + \omega_n^2 T_s^2\right) z^{-2} + 2\omega_n \zeta T_s z^{-1}}{\left(1 - 2\omega_n \zeta T_s + \omega_n^2 T_s^2\right) z^{-2} + \left(-2 + 2\omega_n \zeta T_s\right) z^{-1} + 1}$$

Comparing with two equations,

$$K1 = \frac{-2N\omega_n \zeta}{K_p K_v} \qquad K2 = \frac{-NT_s \omega_n^2}{K_p K_v}$$

Clock/Data Recovery (CDR)

Type I

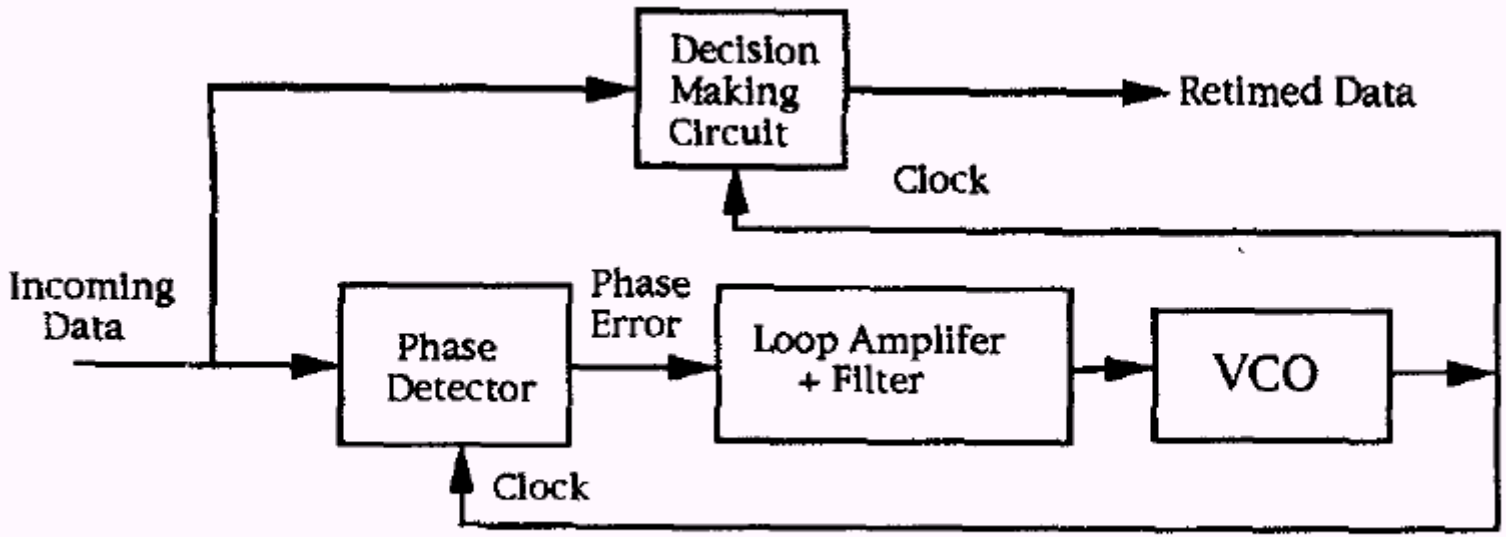


Fig. 2. PLL-based clock recovery system.

IEEE JSSC-27, pp. 1736, Dec. 1992

IEEE JSSC-34, pp. 1915-, Dec. 1999

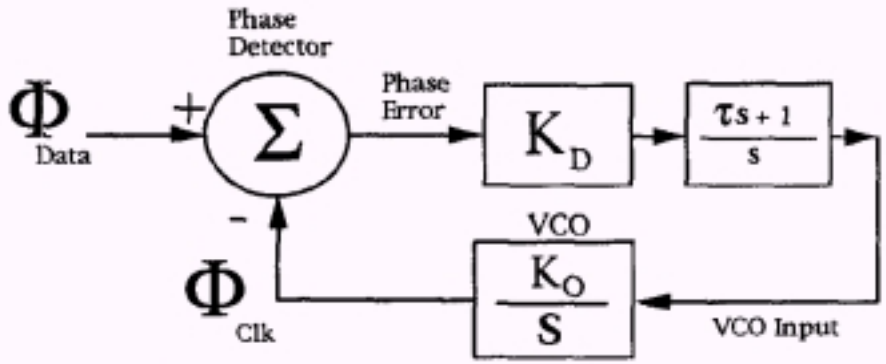


Fig. 3. Linearized block diagram of second-order PLL.

$$H(s) = \frac{\phi_{\text{clk}}(s)}{\phi_{\text{data}}(s)} = \frac{K(1 + \tau s)}{s^2 + K\tau s + K}$$

where $K = K_D K_O$.

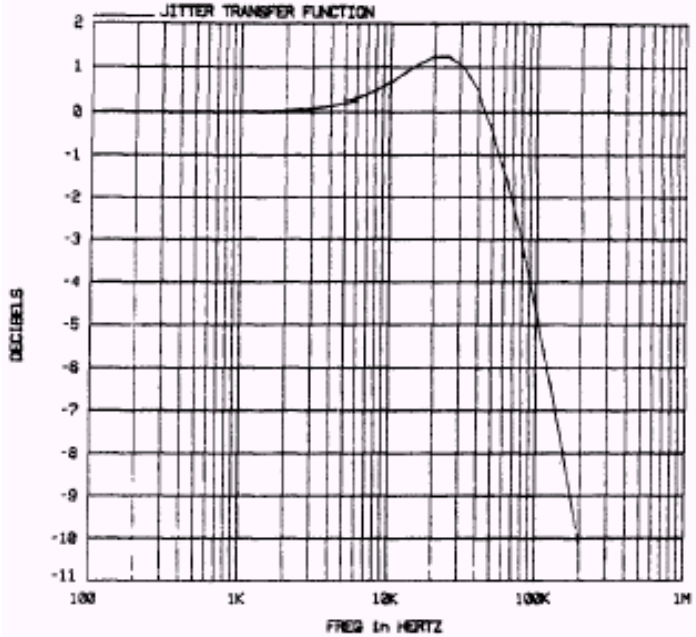


Fig. 5. Jitter transfer function of critically damped second-order PLL.

This gain in excess of unity is known as jitter peaking and is particularly objectionable in systems that employ many clock recovery units in cascade (such as in repeaters) because of the resulting exponential growth of jitter *A*.

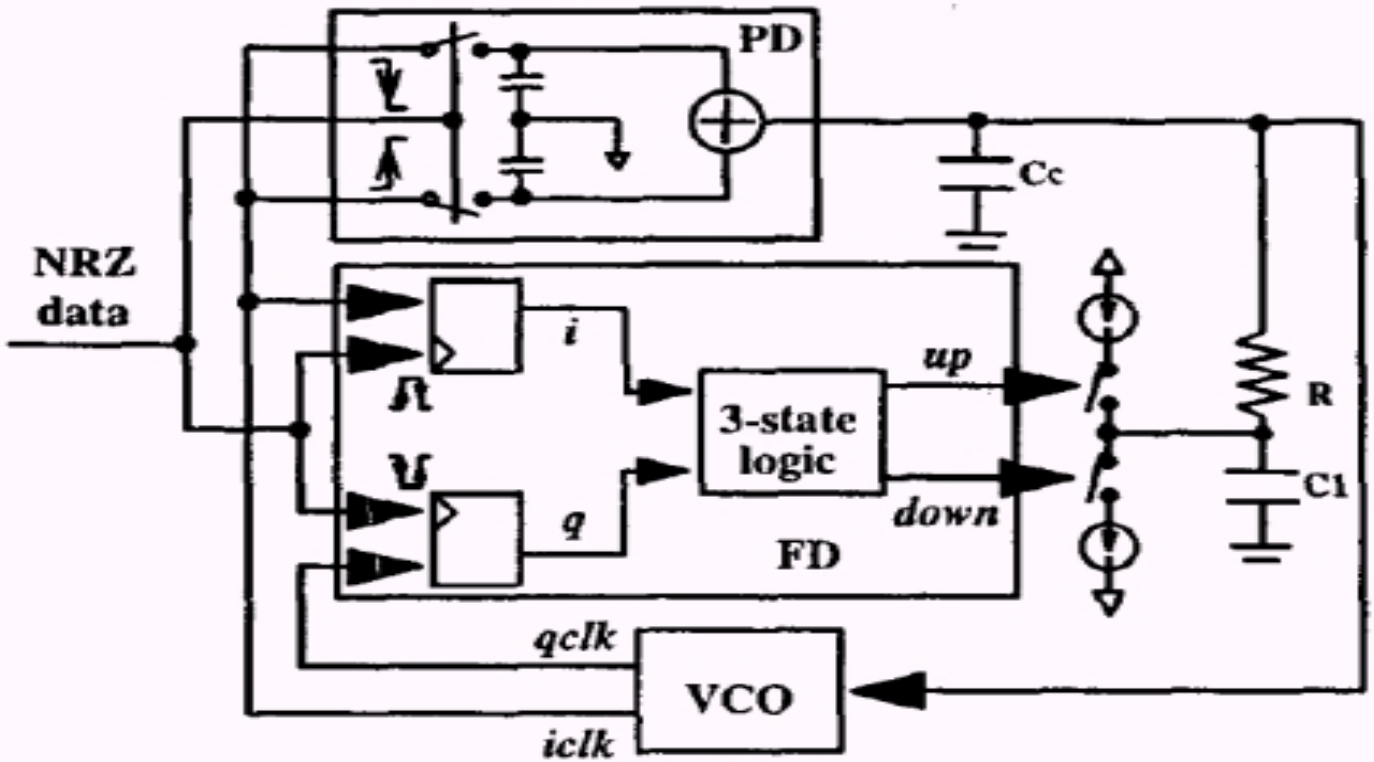


Fig. 1 Block diagram of the 0.7-1Gb/s clock recovery circuit

The First IEEE Asia Pacific Conference on , 1999 , pp. 291 –294

ISSCC, 1999 , pp. 354 -355

qclk

iclk

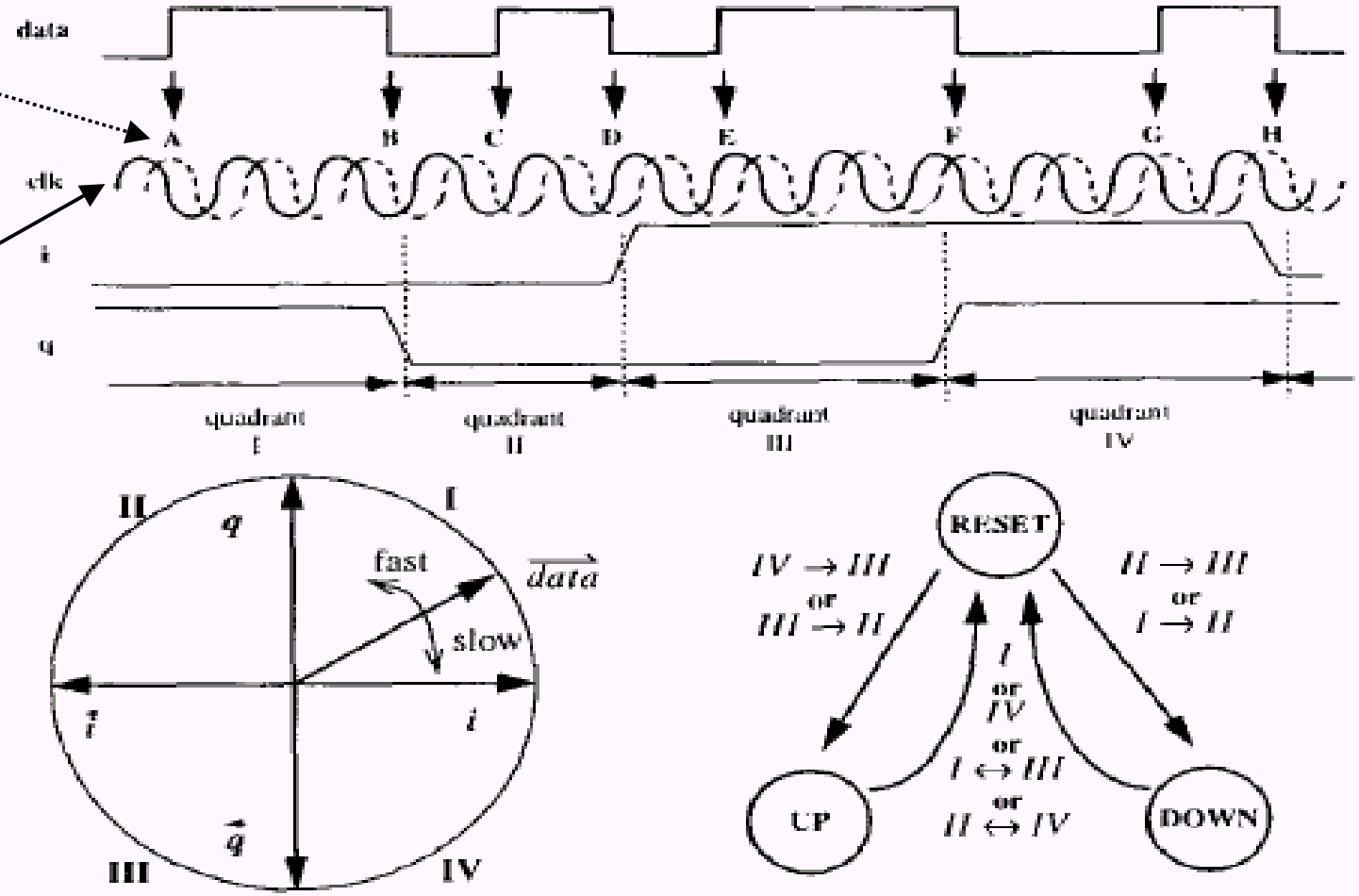


Figure 20.5.2: Three-state frequency detector.

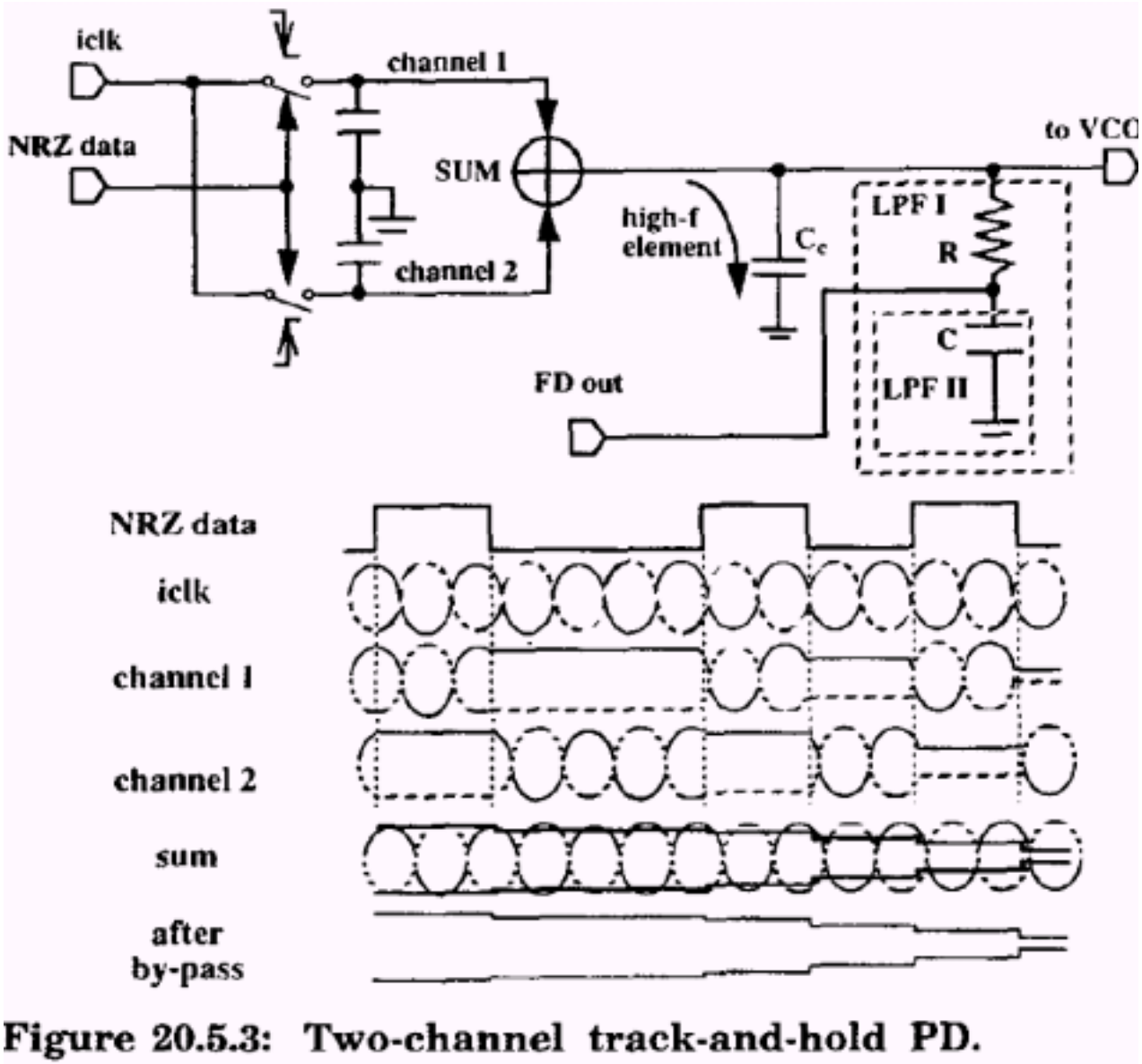


Figure 20.5.3: Two-channel track-and-hold PD.

The sampled areas in Ch2 toward negative

➔ Control voltage deceases

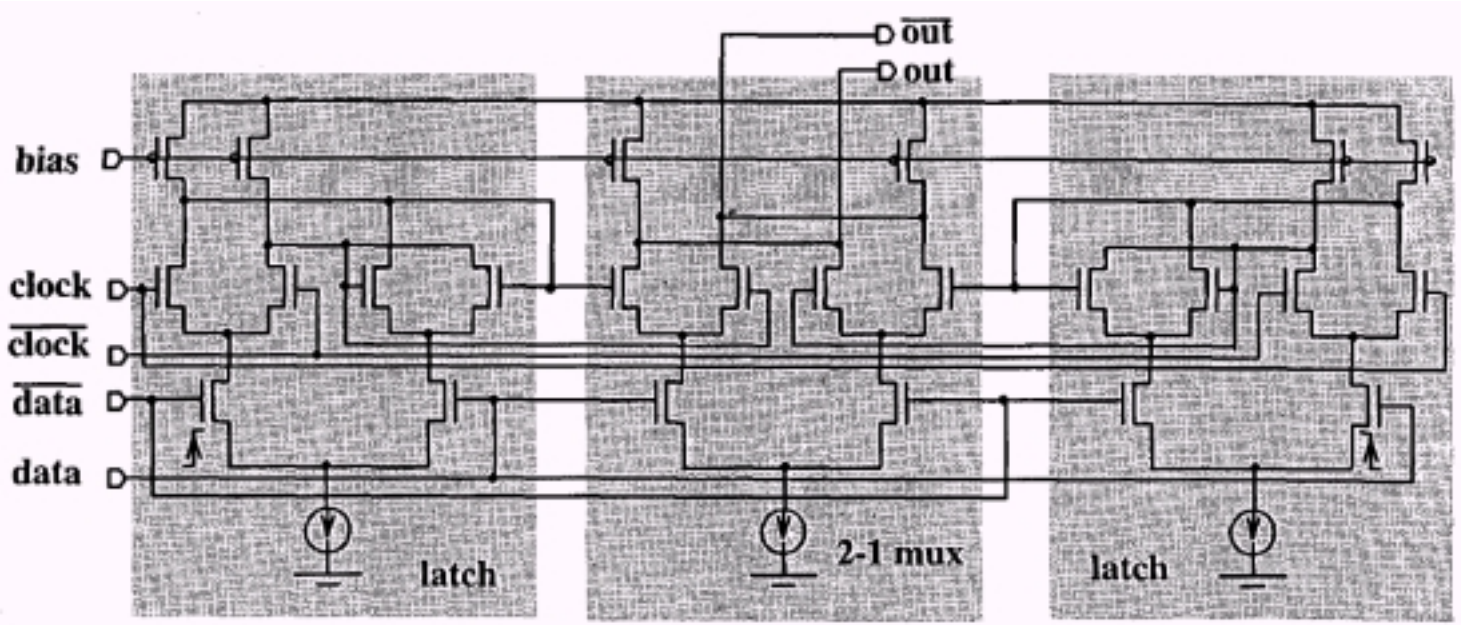
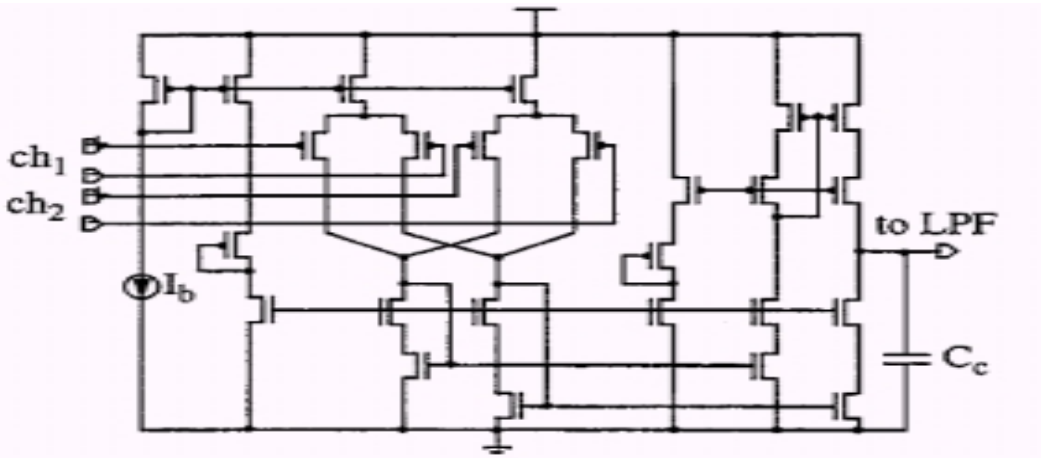
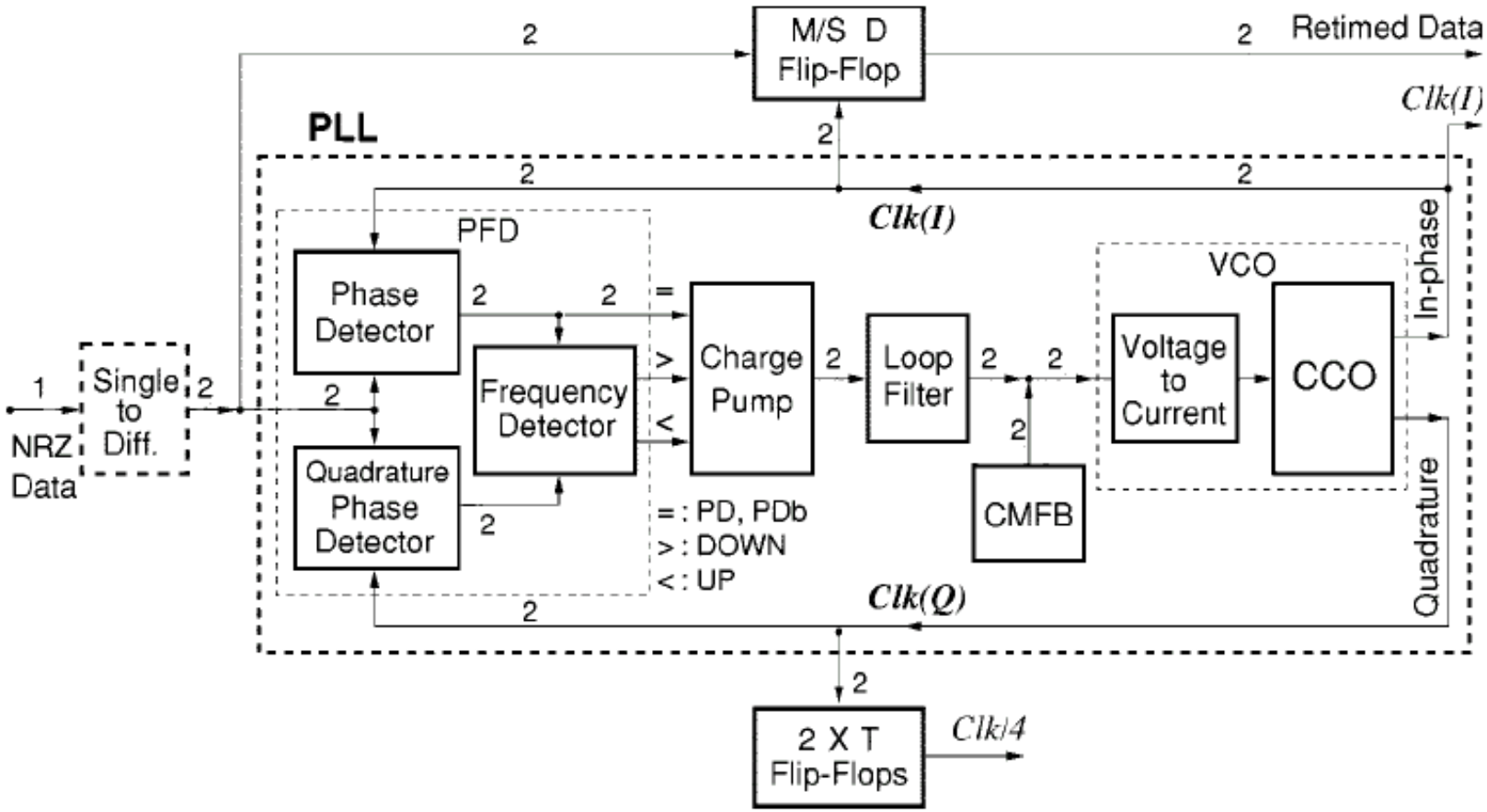


Fig. 4 Double-edge triggered D-flip flop

Summer





IEEE JSSC-27 , pp. 1747-, Dec. 1992

IEEE JSSC-35, pp. 847-, June 2000

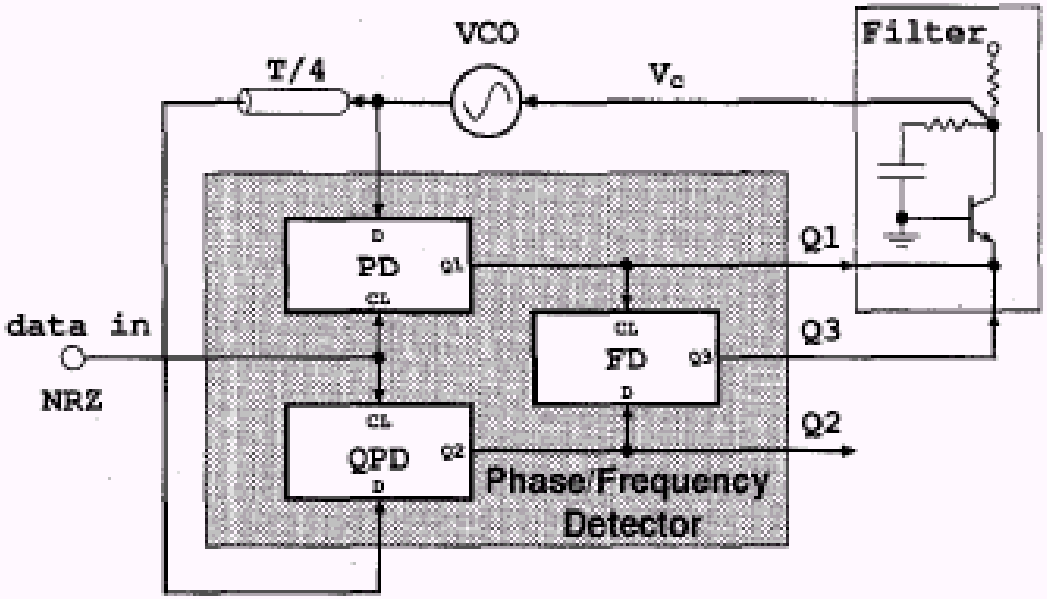


Fig. 1. Block diagram of the PFD IC.

TABLE I
LOGIC TABLE OF THE FREQUENCY DETECTOR

$Q1$	$Q2$	$Q3$
X	1	0
Rising	0	−1
Falling	0	+1

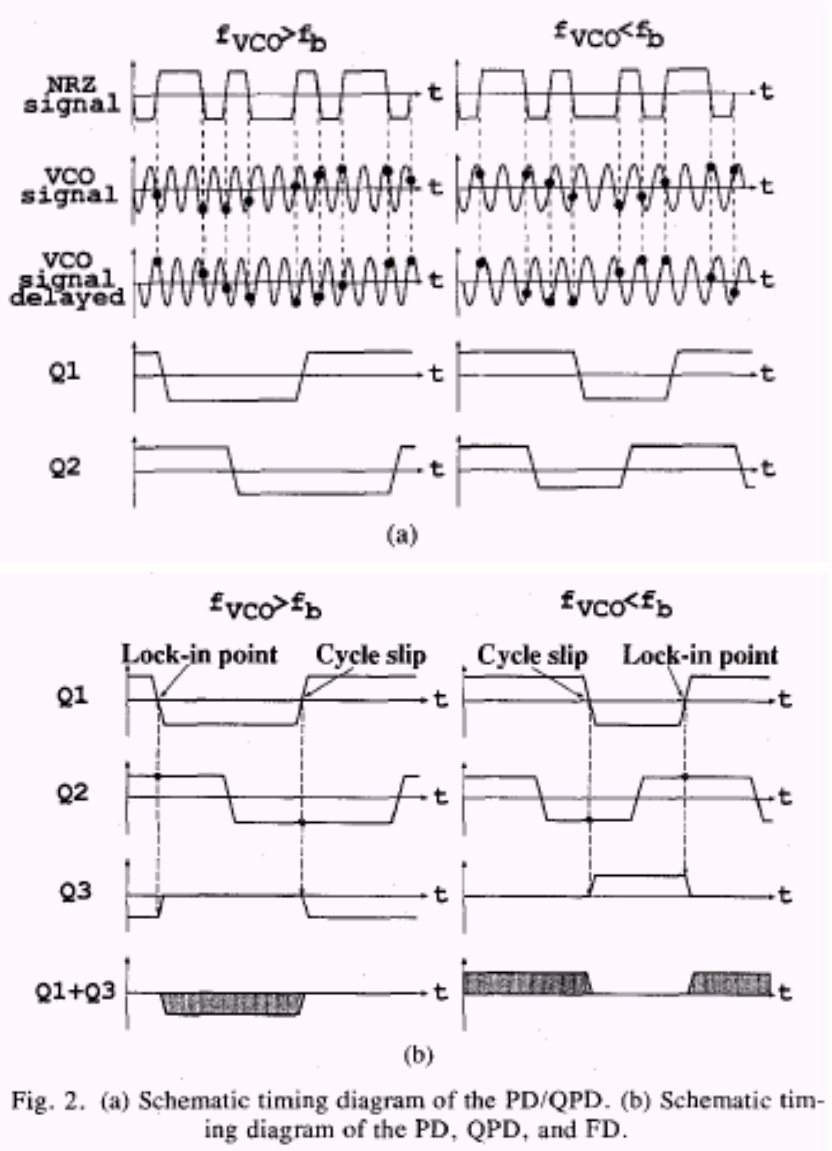


Fig. 2. (a) Schematic timing diagram of the PD/QPD. (b) Schematic timing diagram of the PD, QPD, and FD.

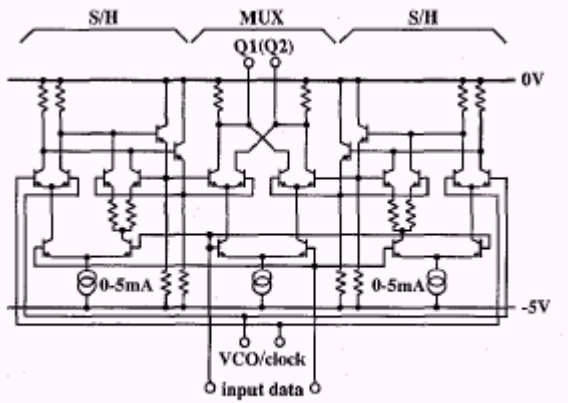


Fig. 3. Circuit diagram of the PD's.

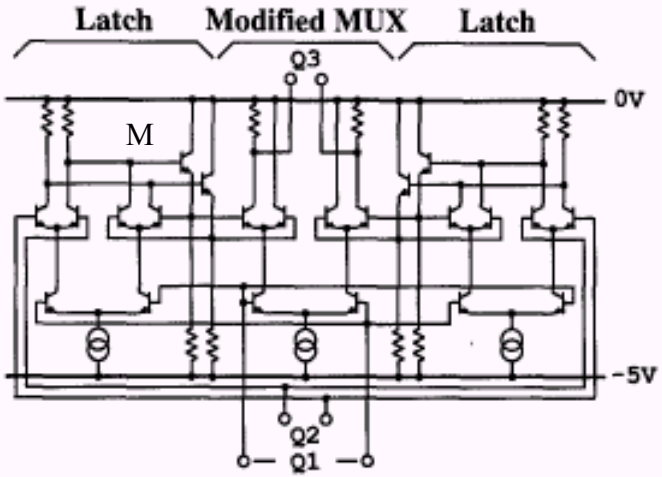
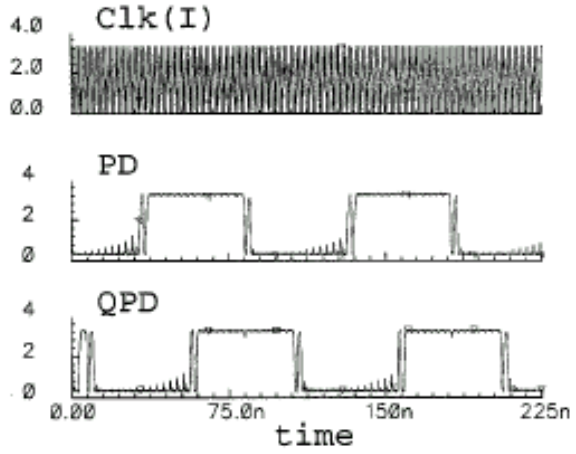


Fig. 4. Circuit diagram of the FD.

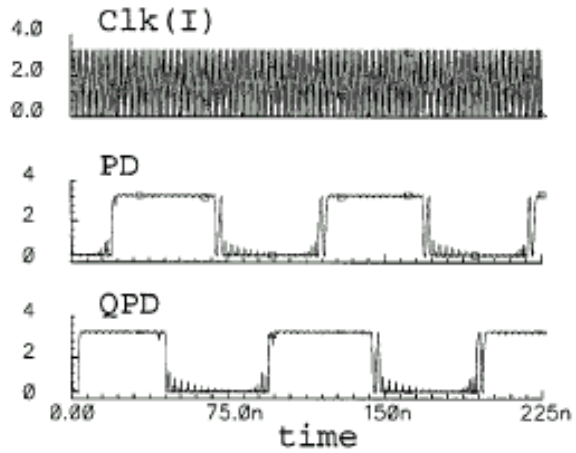
Q1	L	H	H	L
Q2	L	L	H	H
M	H	H	H	L
Q3	Vdd=0 High-X	-1 Low	-1 Low	Vdd=0 High-X

H: Vdd-IR+ΔV

L: Vdd-IR-ΔV

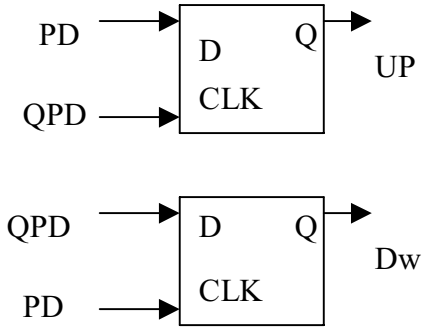


(a)



(b)

Fig. 8. PFD signals. (a) Oscillator frequency < data rate. (b) Oscillator frequency > data rate.



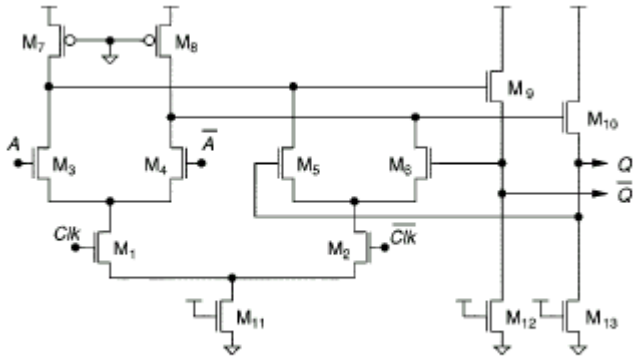
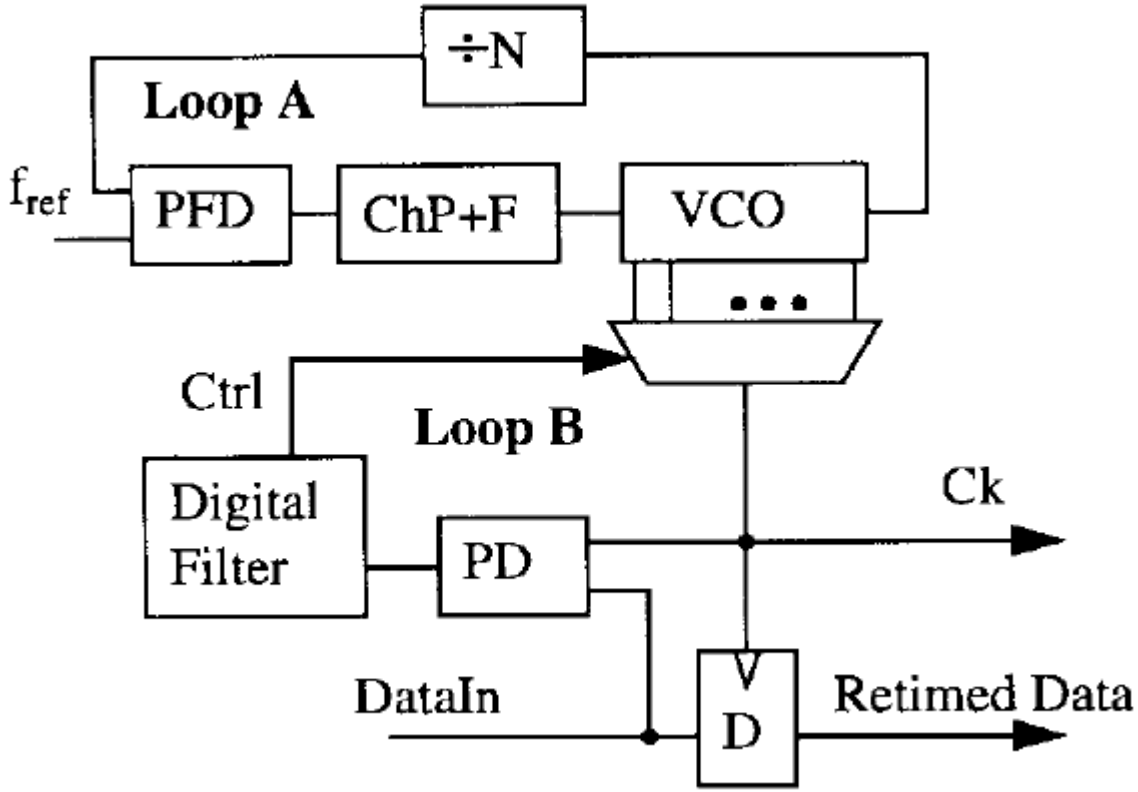
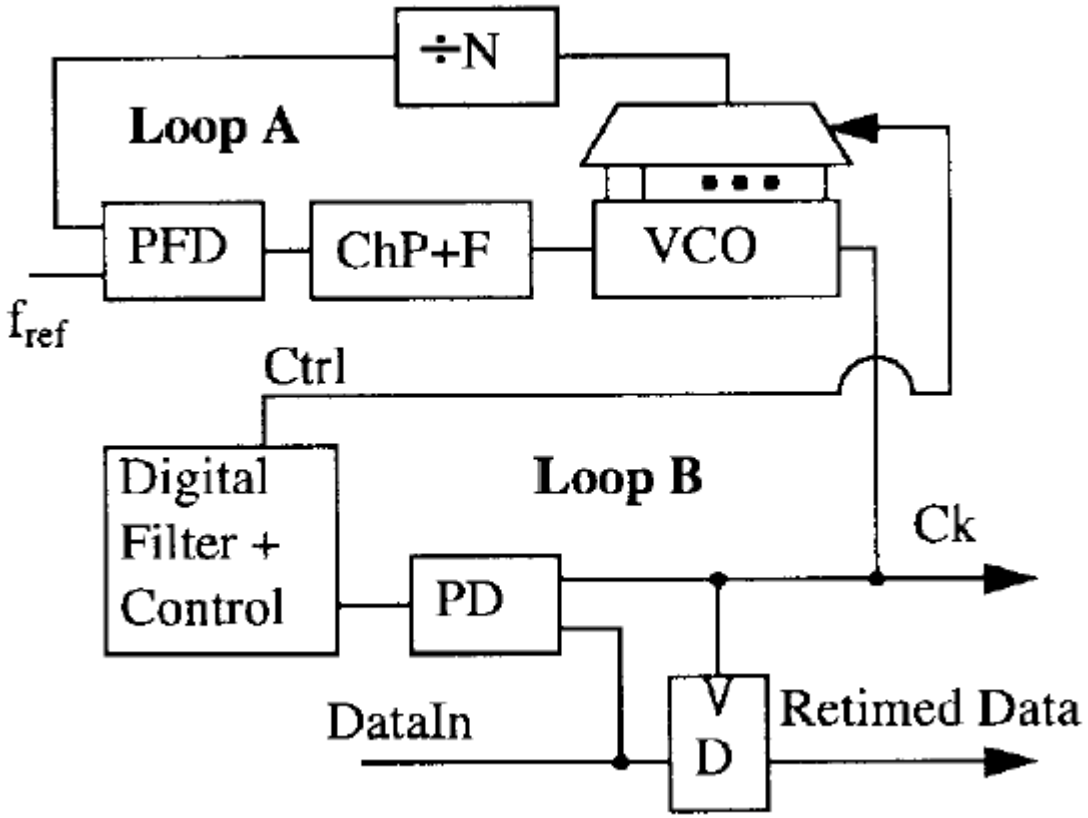


Fig. 11. Schematic of a differential latch (half of the MS flipflop).

Type II


÷N
Loop A
f_{ref}
PFD
ChP+F
VCO
Ctrl
Loop B
Digital Filter
PD
Ck
DataIn
D
Retimed Data

Type III



IEEE JSSC-34, pp. 1915-, Dec. 1999

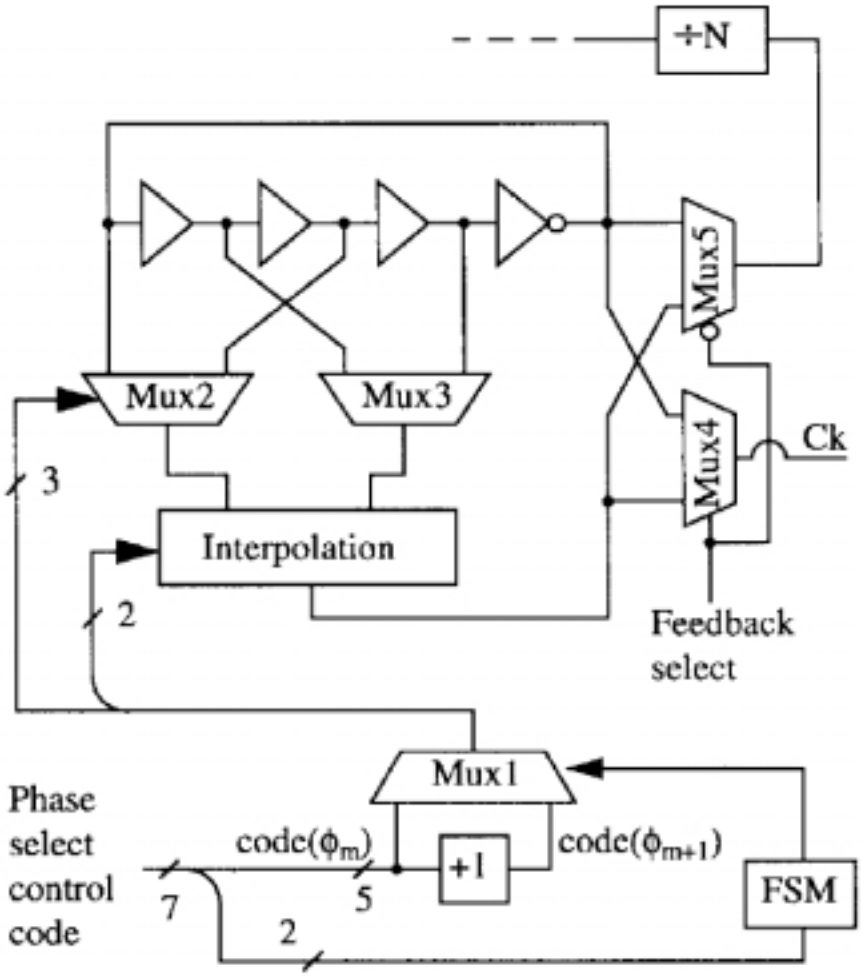


Fig. 2. VCO, phase selector, interpolator, and feedback multiplier.

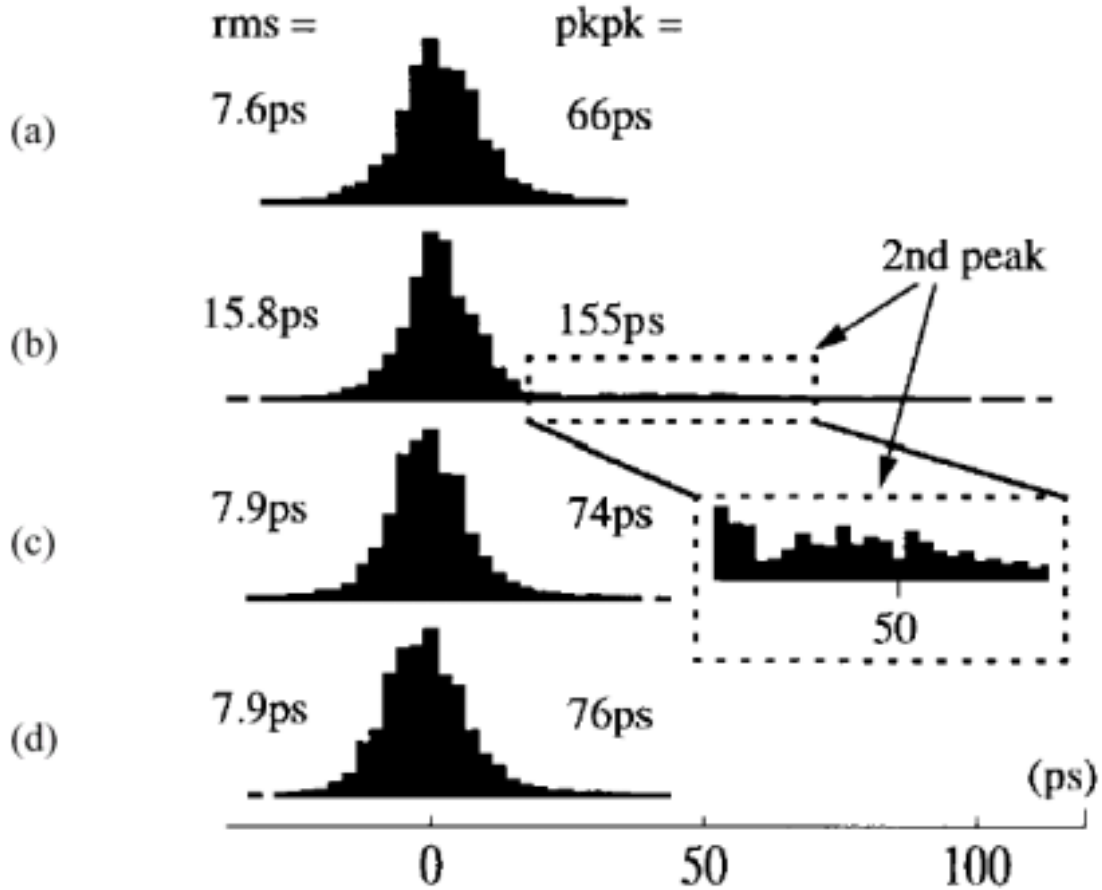
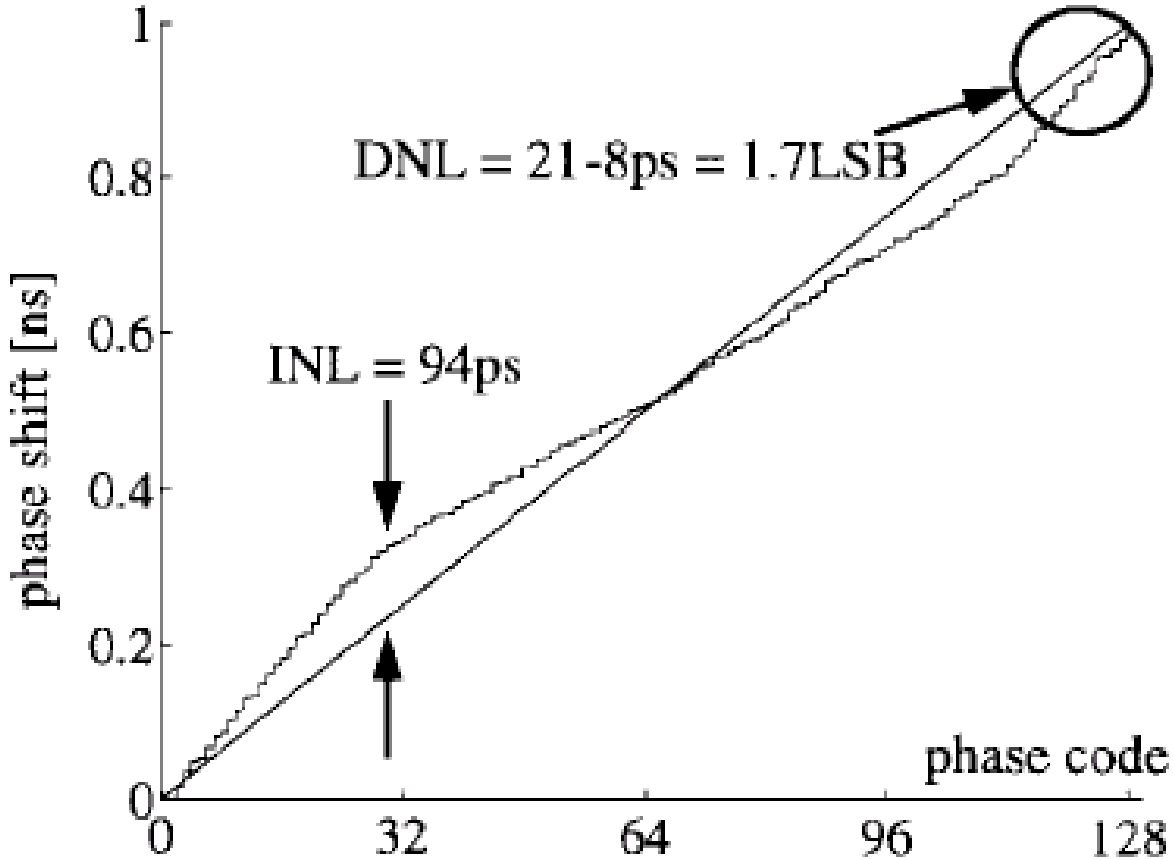


Fig. 3. 500-MHz period distribution histograms. (a) Clock recovery inactive, (b) standard phase selection, (c) feedback phase selection, and (d) averaging phase interpolation. Measurement conditions were $Vdd = 2.5$ V, $N = 25$, $f_{\mathrm{ref}} = 20$ MHz, and $f_{\mathrm{data}} = 499.4$ Mb/s.



Four-stage VCO

→8 phases

→4x interpolating

→4x averaging phase

→total 128 phases

Fig. 4. Phase shift versus phase code measured at 1 GHz.

Clock/Data Recovery D/PLL

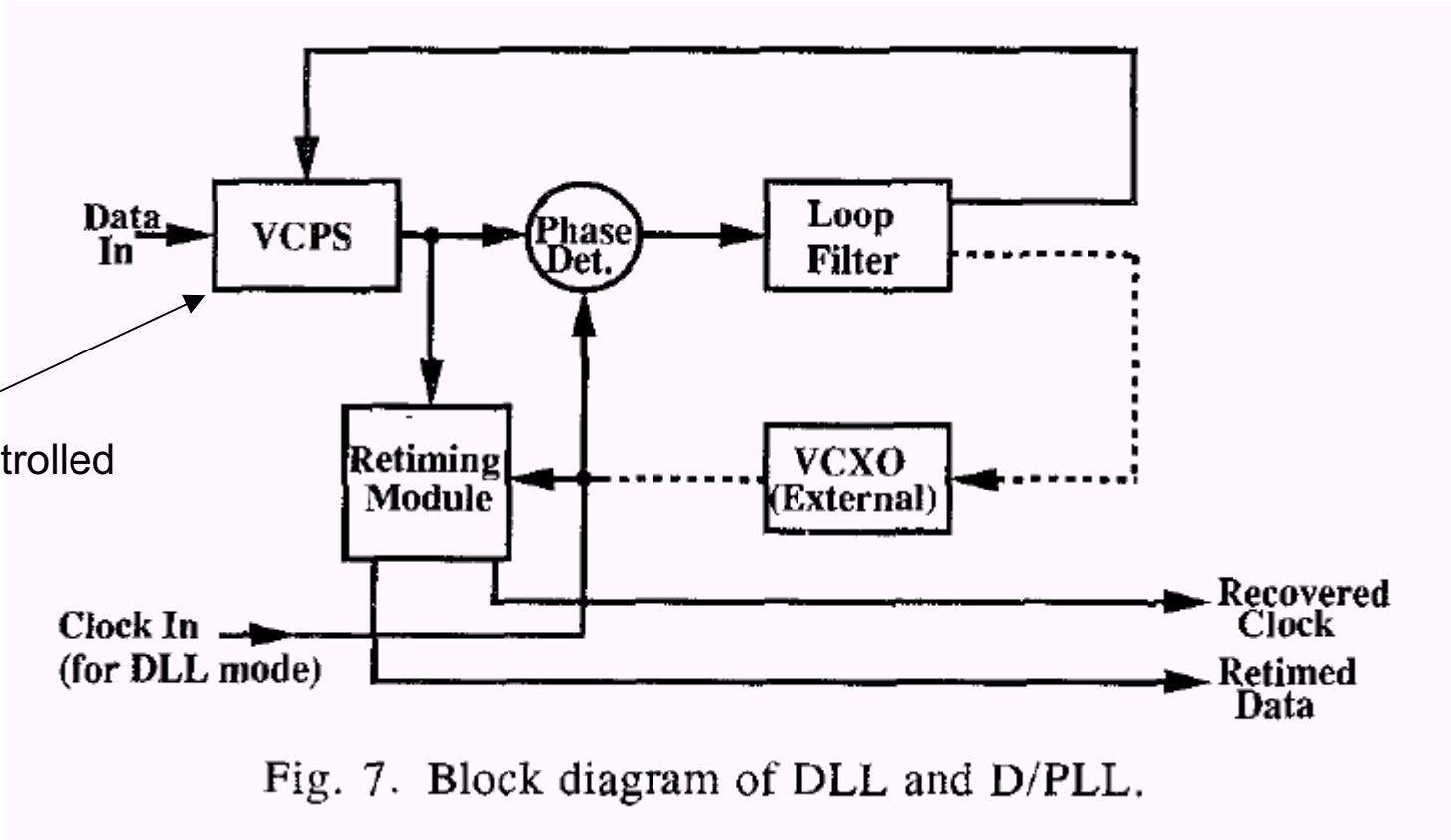


Fig. 7. Block diagram of DLL and D/PLL.

IEEE JSSC-27, pp. 1736, Dec. 1992

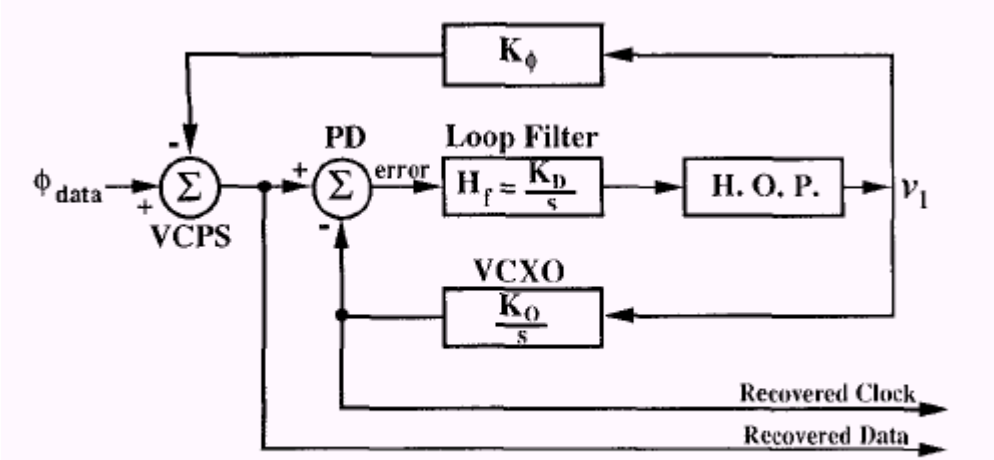


Fig. 9. D/PLL linearized block diagram.

$$v_1 = \frac{K_D}{s}(\phi_{\text{data}} - K_\phi v_1 - \phi_{\text{clk}})$$

$$\phi_{\text{clk}} = v_1 \frac{K_O}{s}$$

$$H(s) = \frac{\phi_{\text{clk}}(s)}{\phi_{\text{data}}(s)} \approx \frac{K}{s^2 + K\tau s + K}$$

Loop zero out of forward path

Hogge Phase Detector

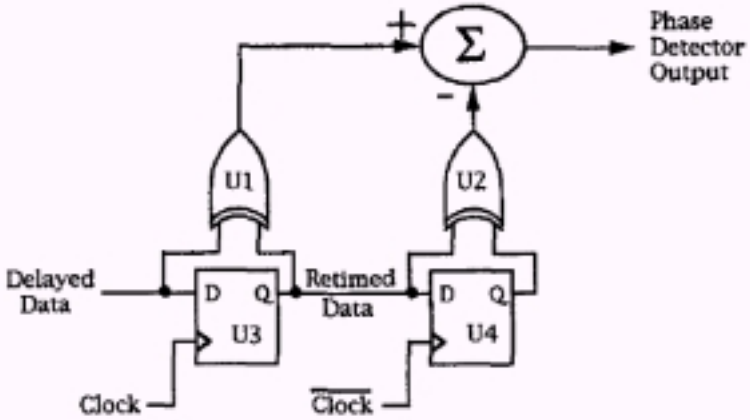


Fig. 11. Hogge phase detector.

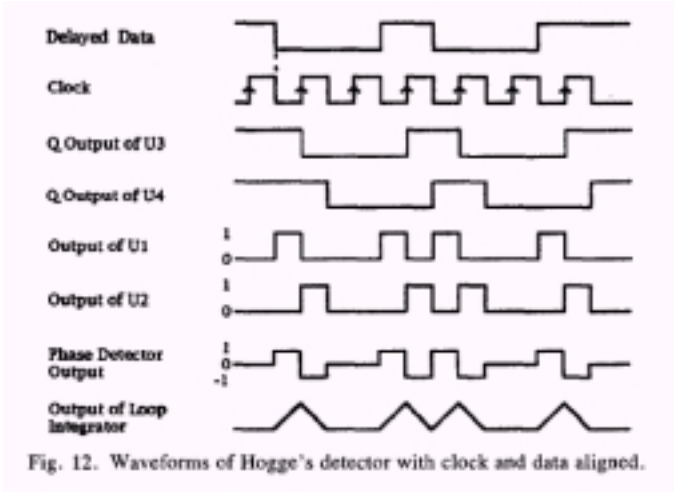


Fig. 12. Waveforms of Hogge's detector with clock and data aligned.

This detector does suffer from a sensitivity to the data transition density. Since each triangular pulse on the output of the loop integrator has positive net, the presence or absence of such a pulse affects the average output of the loop integrator. -->data-dependent jitter

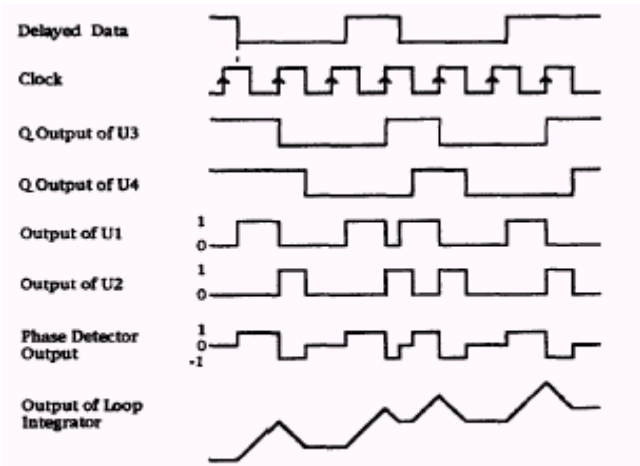


Fig. 13. Waveforms of Hogge's detector with data ahead of clock.

Triwave Phase Detector

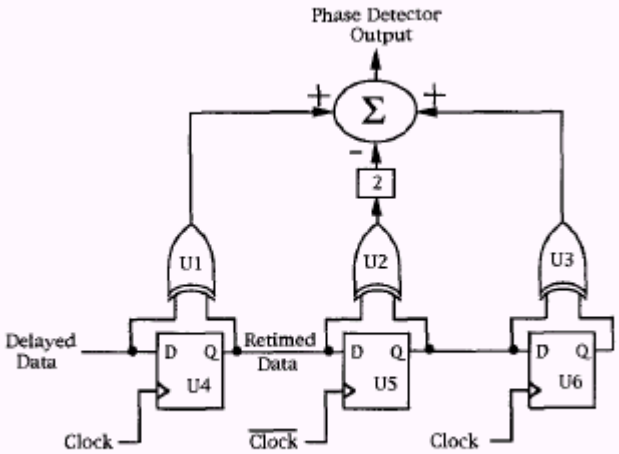


Fig. 15. Triwave phase detector.

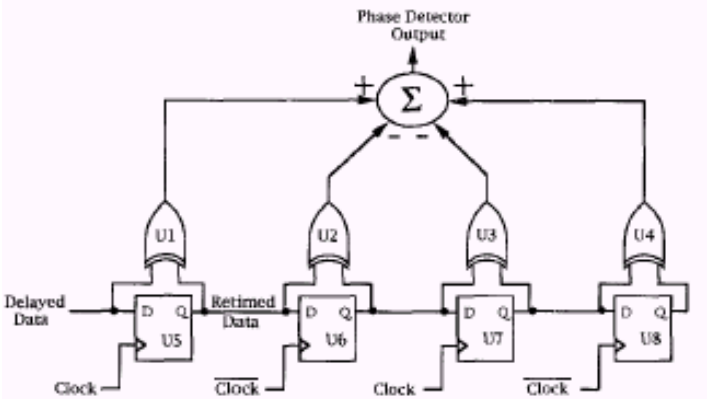


Fig. 17. Modified triwave phase detector.

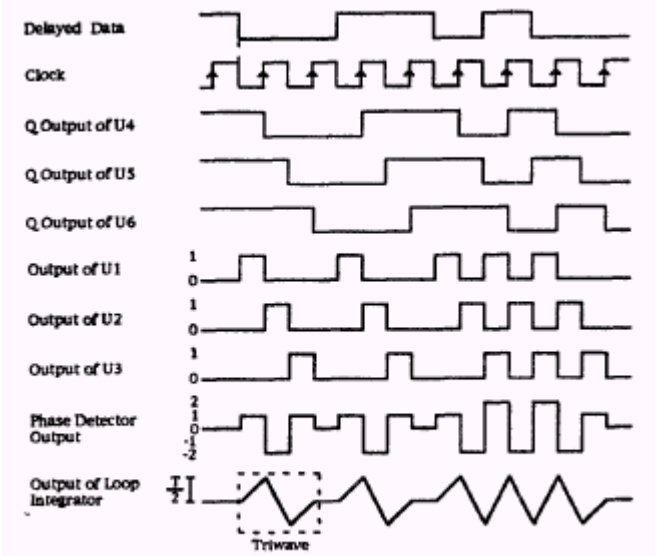
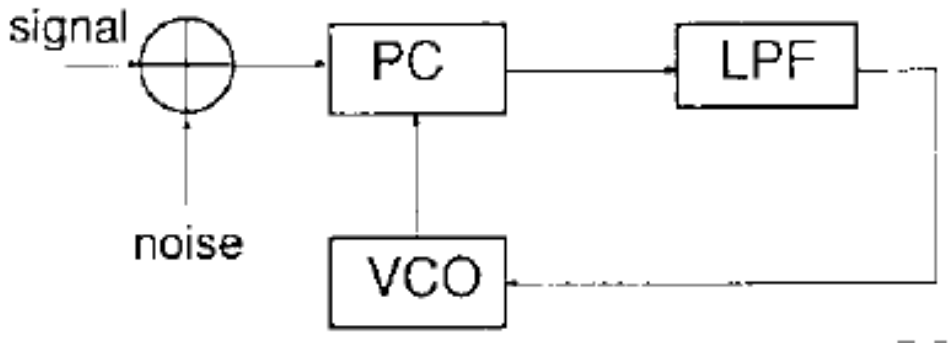


Fig. 16. Waveforms of triwave detector with clock and data aligned.

CDR with tunable jitter

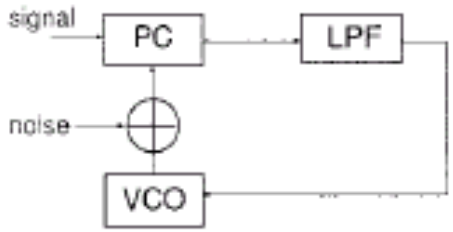
Additive noise



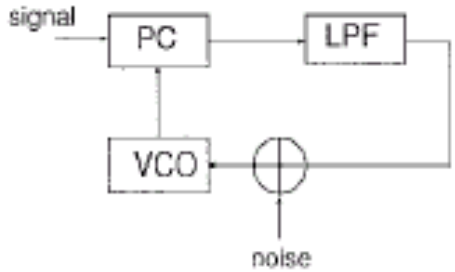
$$\sigma_1 = \sqrt{\frac{N_0}{A^2}\frac{\omega_n}{4\xi}\left[1+\left(2\xi-\frac{\omega_n}{K}\right)^2\right]}$$

where is No the power spectra density of noise, A is the input signal amplitude, ωn is the natural angular frequency, ξ is the damping factor, and K is the loop gain. When the loop gain becomes larger, the jitter becomes larger, This means that smaller loop gain causes narrow noise bandwidth, thereby suppressing jitter.

Jitter generation



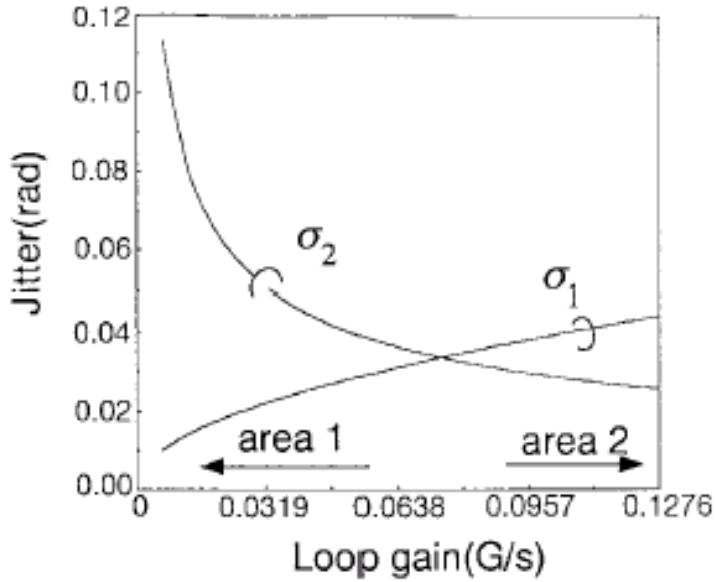
noise forward VCO



noise present for VCO

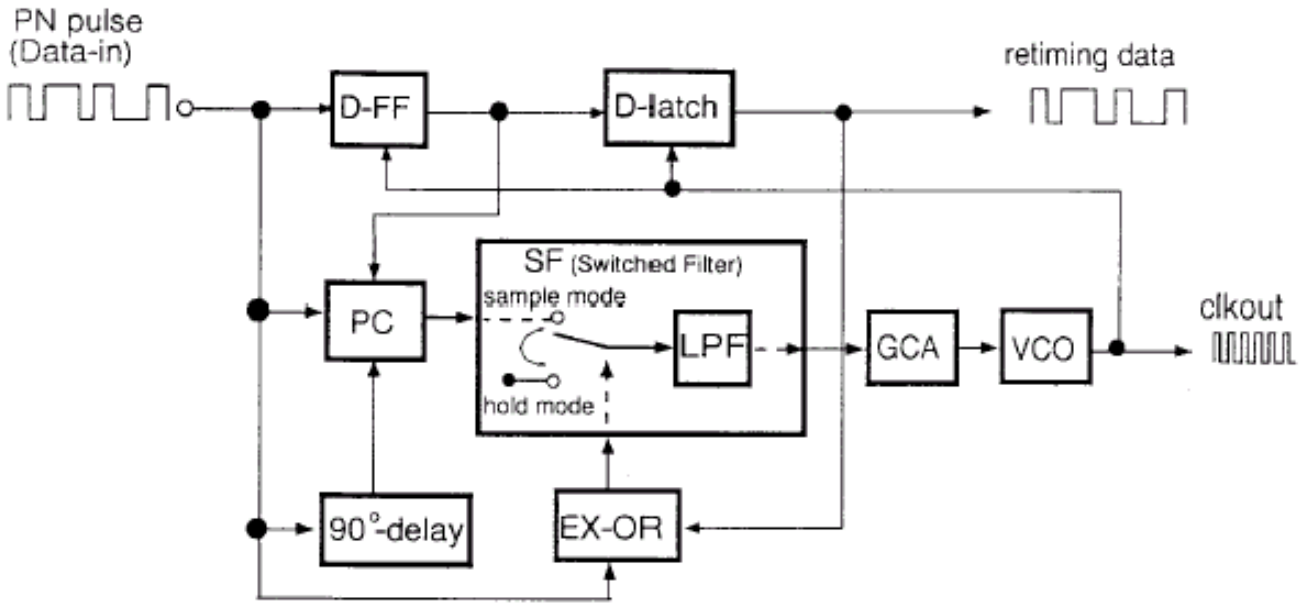
$$\sigma_2 = \sqrt{\frac{\eta}{2}\frac{\pi^2}{\xi\omega_n}\left(1+\frac{\omega_n^2}{K^2}\right)}$$

where σ2 is the power spectral density of noise. This equation is derived assuming that the instantaneous frequency deviation of the VCO output is caused by disturbance due to random phase noise. In this equation, when the loop gain becomes larger, the jitter becomes smaller.



Loop-gain dependence of jitter.

Switched-filter CDR with tunable jitter



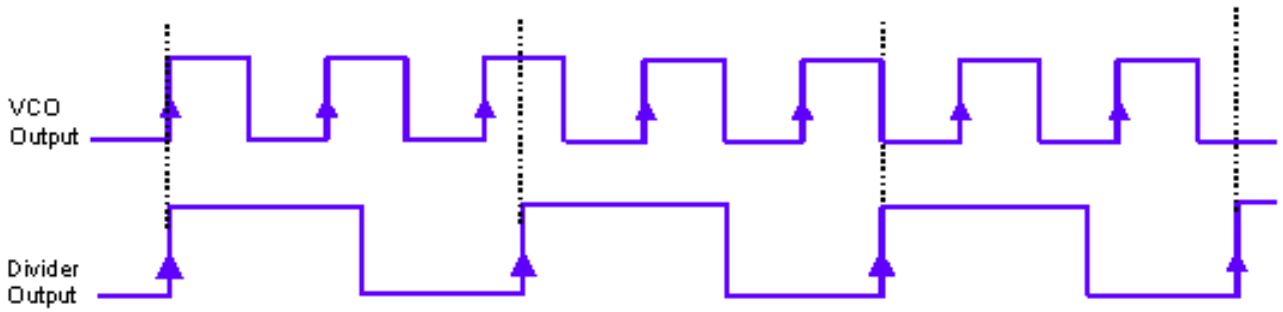
The main features of SF circuit operation are that the PC output can be transferred to the low-pass filter (LPF) only when data transitions occur (sample mode) and the LPF output can be constant during consecutive data inputs (hold mode).

Fractional-N Frequency Synthesizer

$$f_{VCO} = f_{ref} \cdot (N + \frac{k}{M}) = f_{ref} \cdot (N + 0.F)$$ where K and M are integer numbers, k<M

$$T_{ref} = T_{VCO} \cdot (N + 0.F)$$

Ex. N.F=2.25



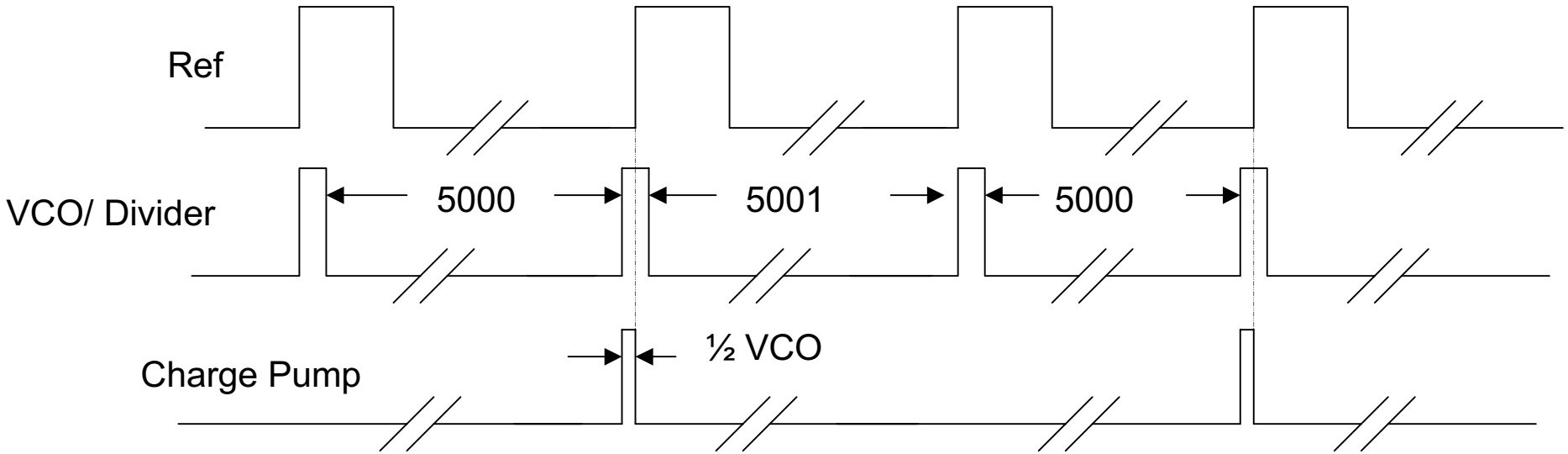
Electronic Design , Sept. 2000

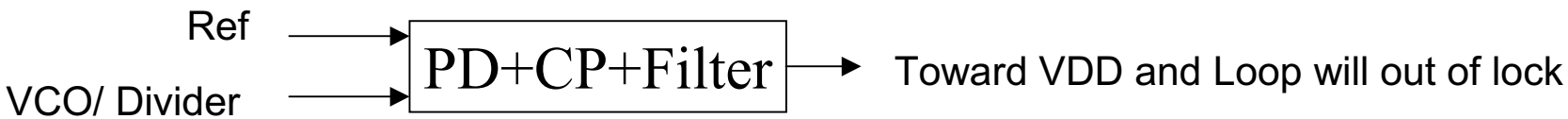
W. Rhee, Ph.D thesis and IEEE JSSC-35, pp. 1453-, Oct. 2000

Emerging technologies, Tutorial for 1996 ISCAS

Fractional divider

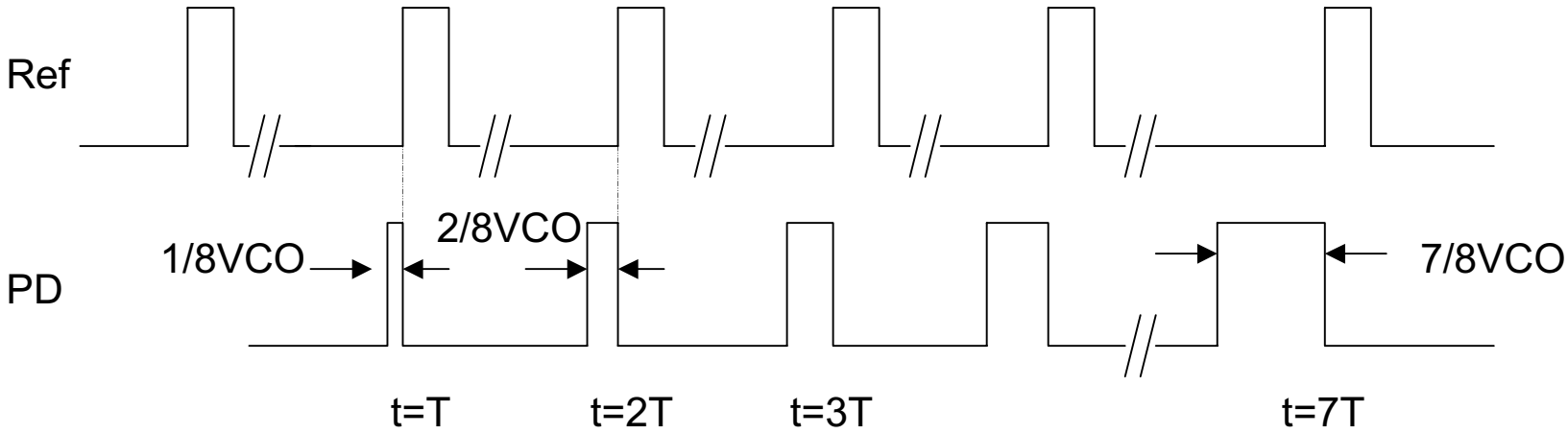
Suppose N.F=5000.5 and N=5000, N+1=5001





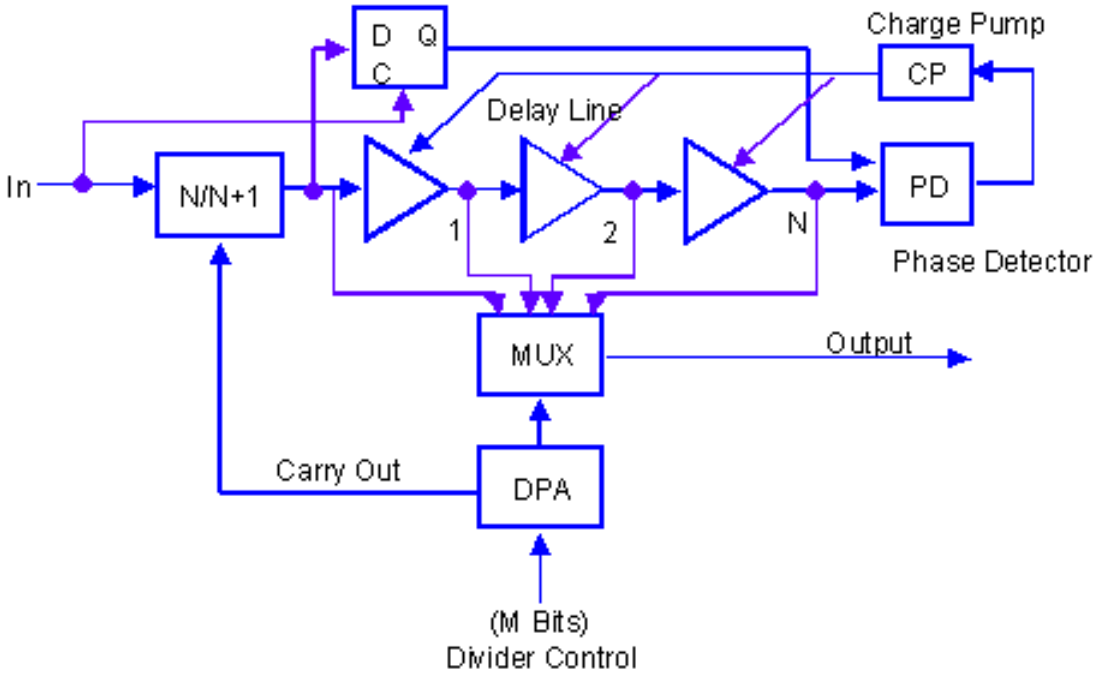
RF design , pp. 34-, Nov. 2000

Ex. N.F=N+1/8

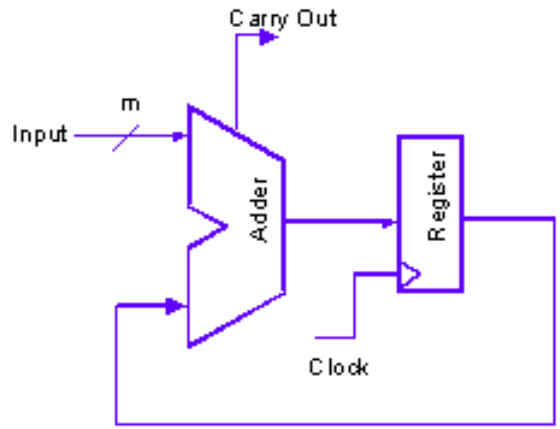


Intuitionally, one can increase the delay for every output of the VCO/divider to compensate the phase errors.

Fractional divider



An example of fractional N divider implementation



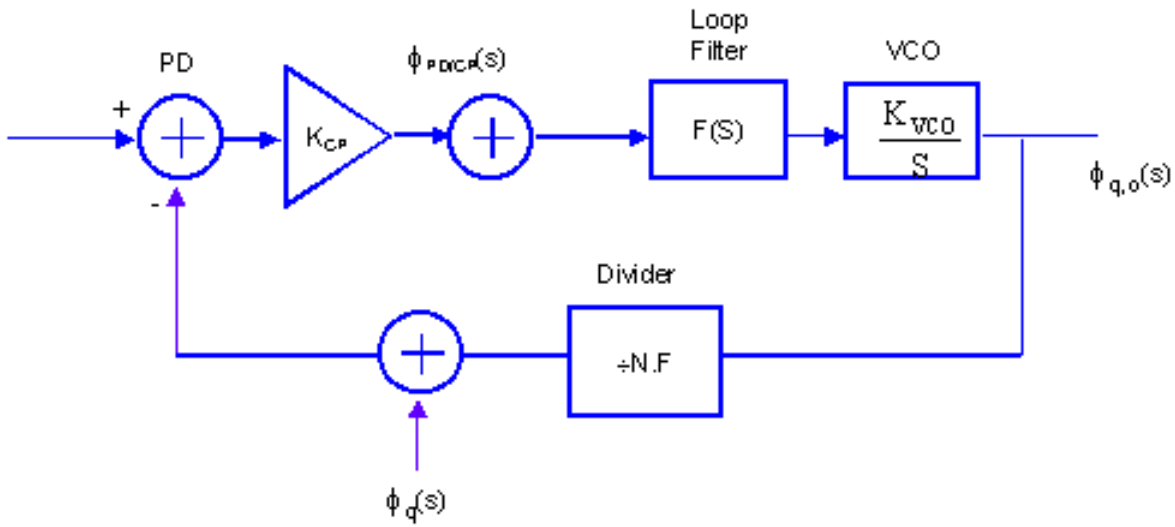
Design of a simple digital phase accumulator

Suppose Nd=8=2^m and m=3 $N.F = N + \frac{x}{2^m}\ and\ 0.F = \frac{x}{2^m} = \frac{2}{8}$

Suppose the DPA has 3 bits and, therefore, the delay line has 8 elements. Each phase packet corresponds to 1/8 of a VCO cycle. When no carry-out occurs, the DMD divides by N. DPA is incremented by 2 every reference cycle. This means that the output is phase shifted by a progressively increasing number of phase packets. i.e., 0, 2, 4, 6, 8, As a result, the period of the DMD output is increased by 2/8 of a VCO cycle. Therefore, the effective division ratio becomes N+0.25. When the DPA content reaches 8, the content of DPA will be reset. The carry-out forces the DMD to divide by N+1. This is equivalent to the DMD dividing by N and its output being delayed by 8 phase packets. i.e., one VCO cycle.

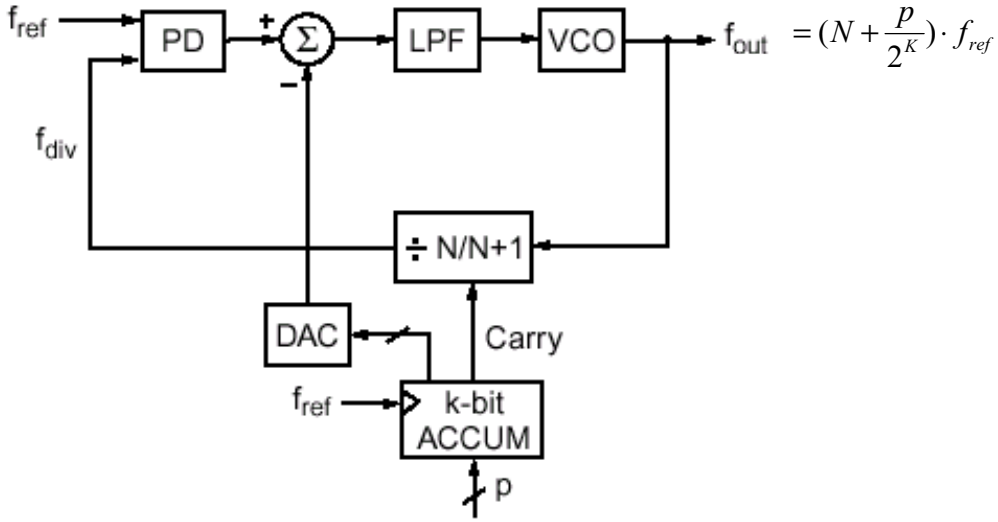
This method is subject to the jitter of the DLL and mismatch of the cells.

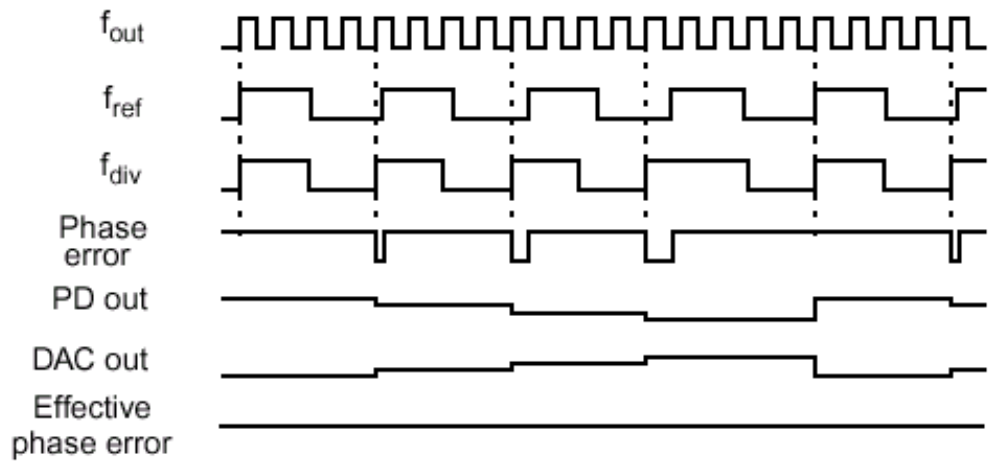
Current-injection-based synthesizer



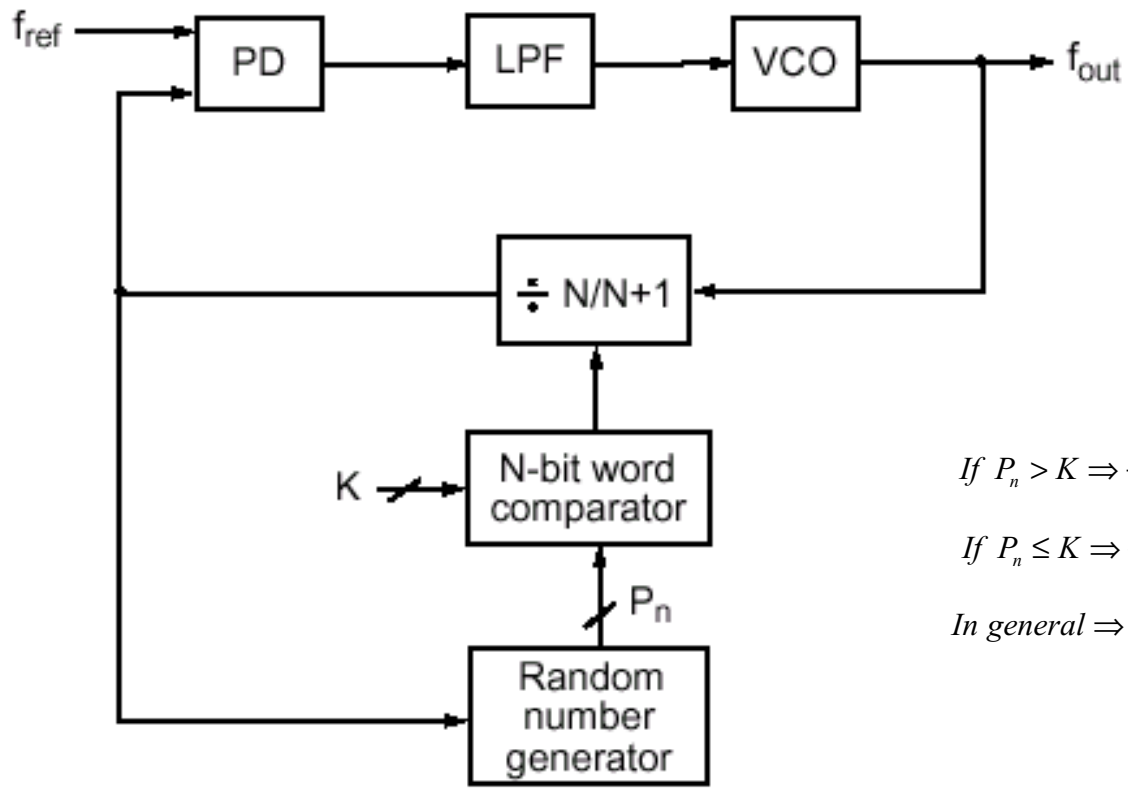
$$\Phi_{q,o}(s) = \frac{N.FK_{CP}K_{VCO}F(s)}{N.Fs + F(s)K_{VCO}K_{CP}}\Phi_q(s)$$

Current-injection-based synthesizer





Random Jittering synthesizer

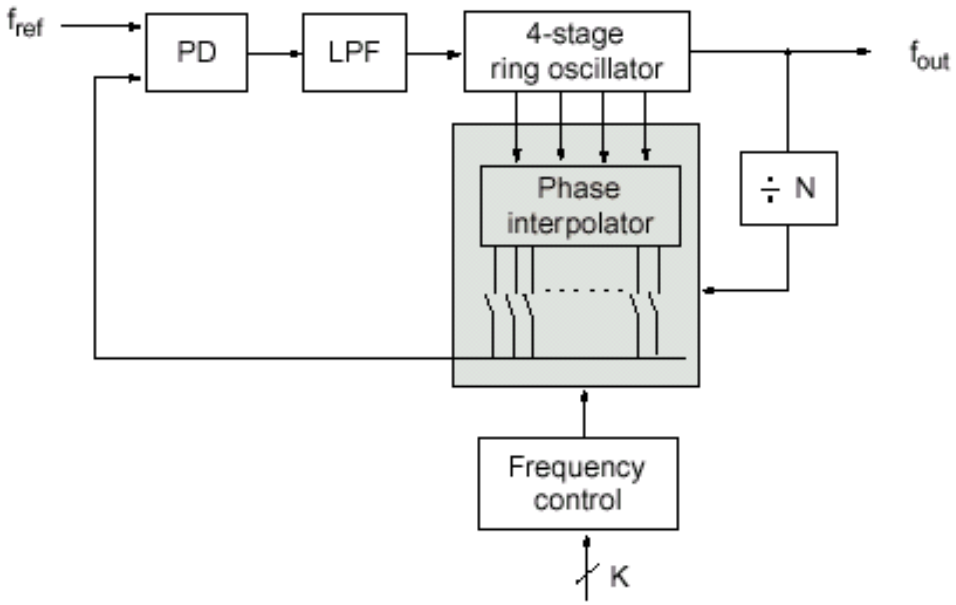


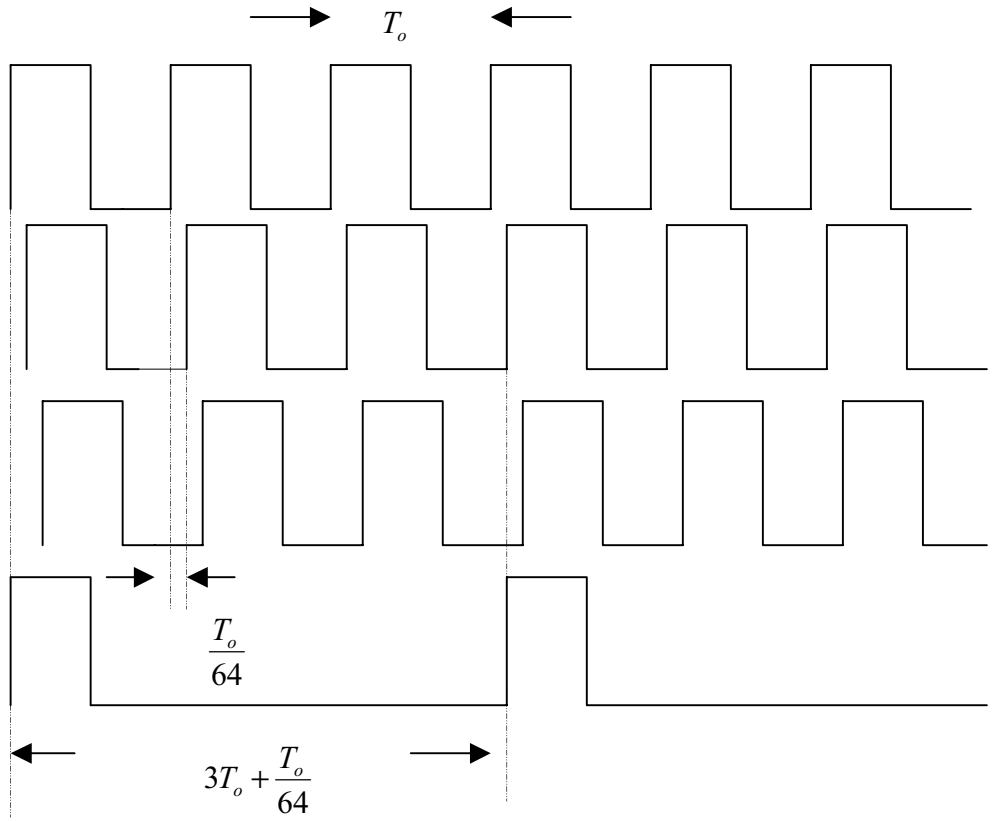
$If\ P_n > K \Rightarrow \div(N+1)$

$If\ P_n \le K \Rightarrow \div N$

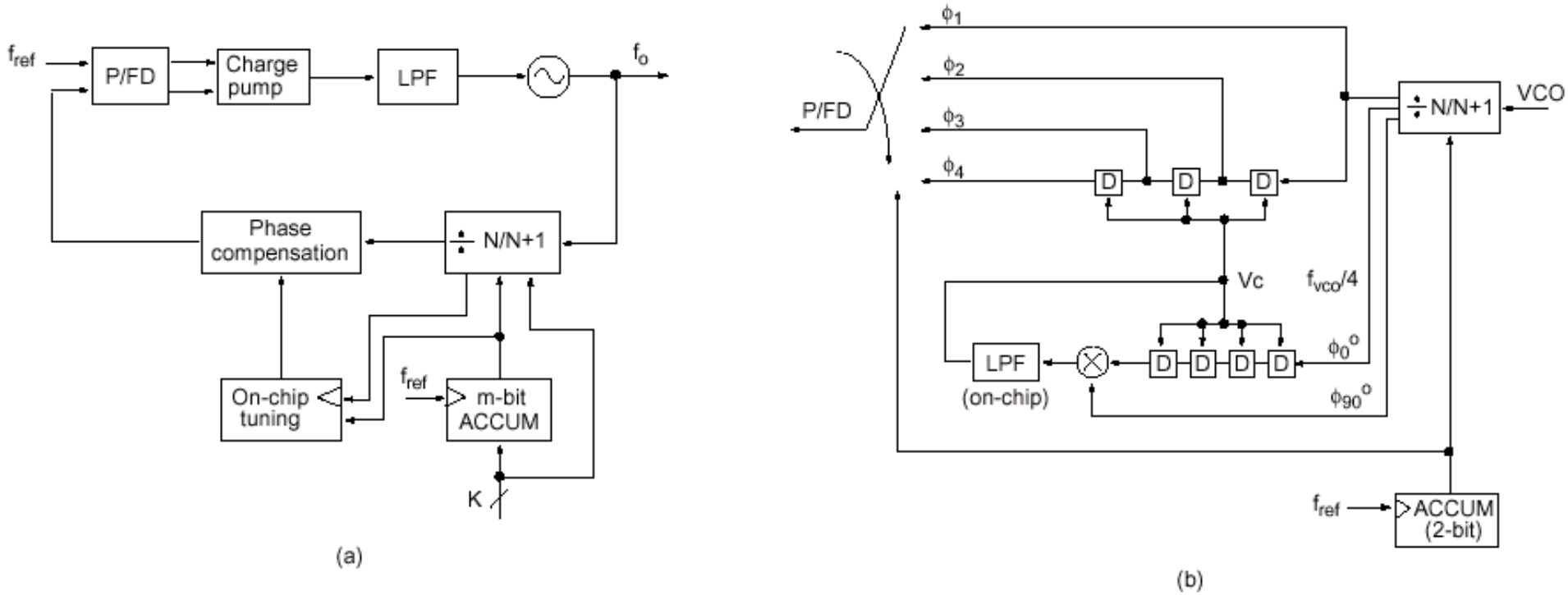
$In\ general \Rightarrow \div(N.K)$

Phase-interpolated synthesizer



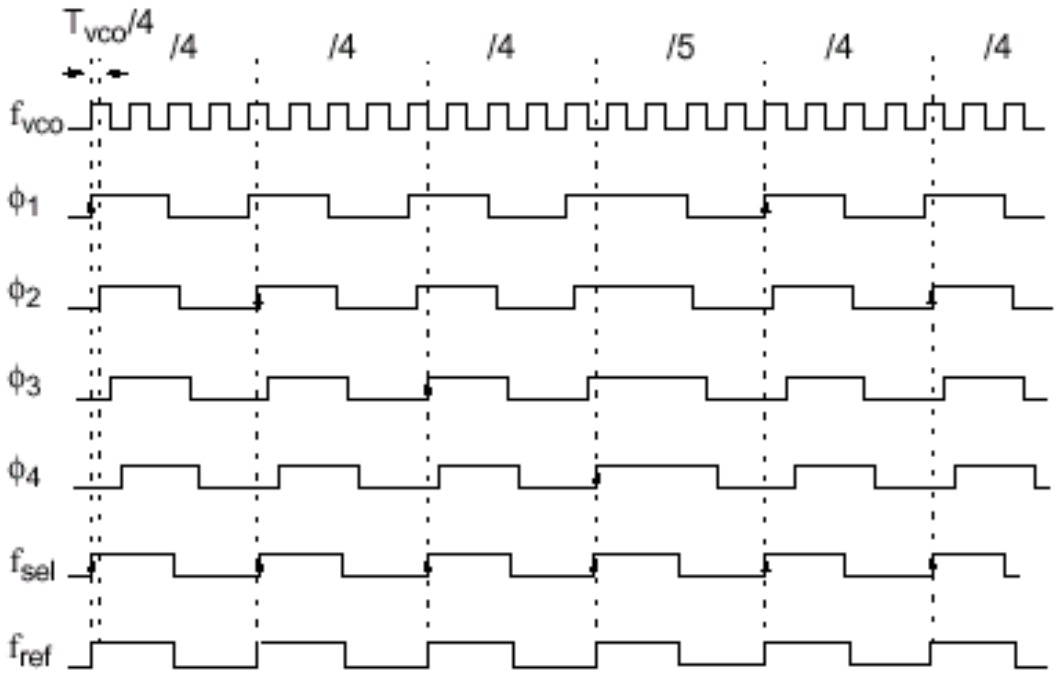


Phase-Compensation synthesizer

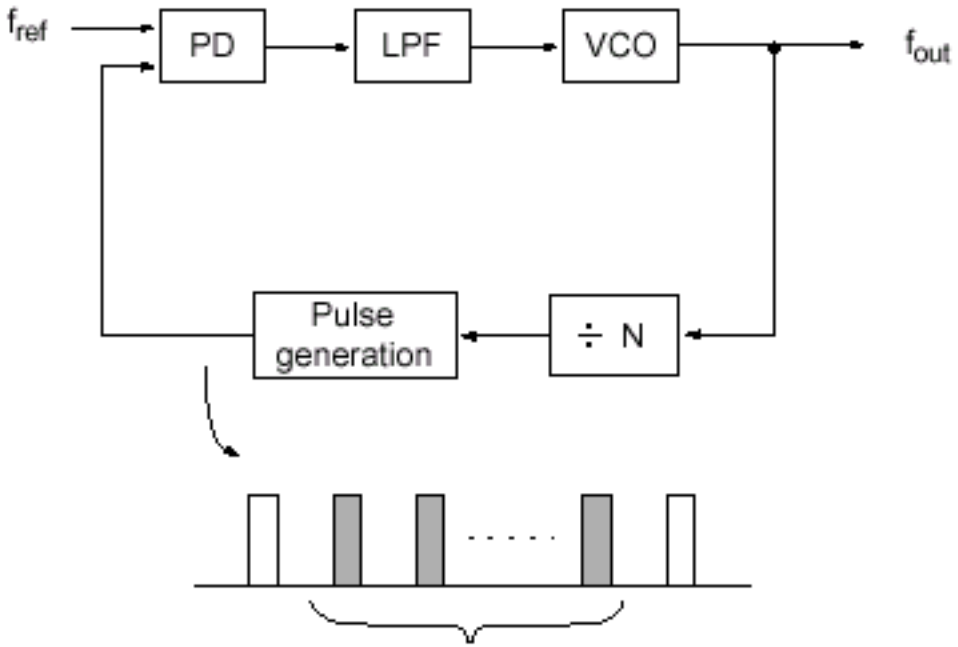


(a) Phase compensation method, and (b) on-chip tuning with DLL.

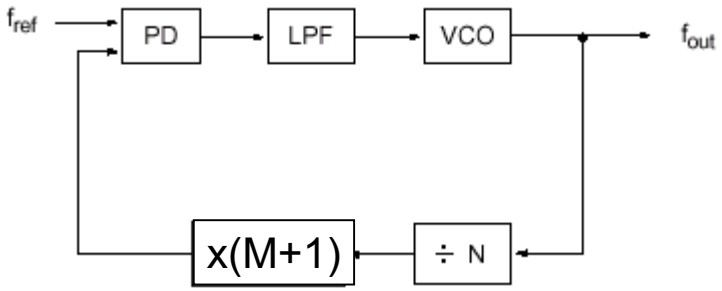
Timing diagram example for 4 + 1/4 division



Phase-generation synthesizer

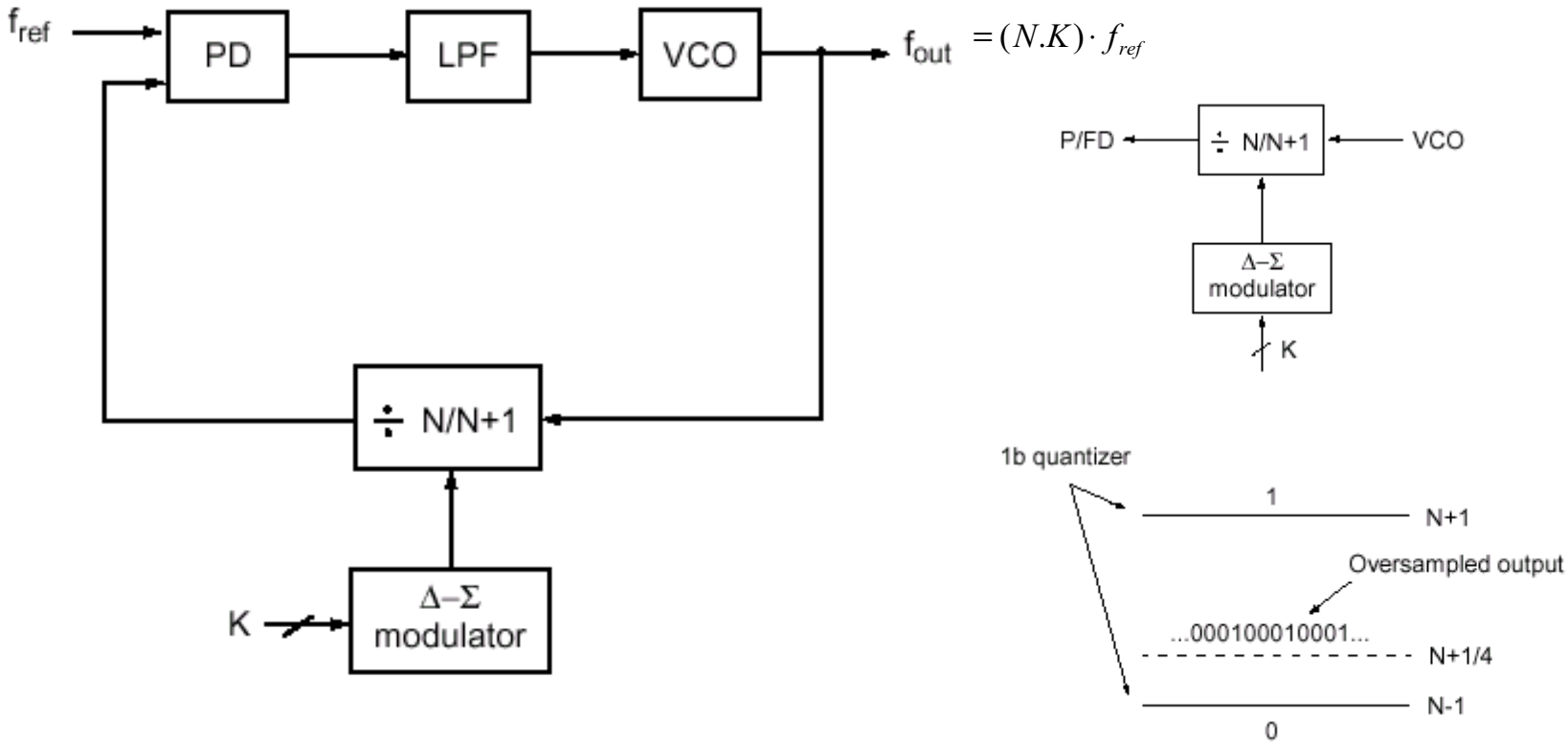


Equivalent Ckt

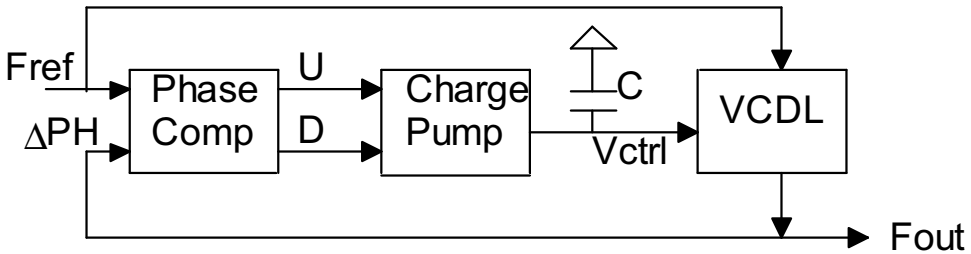


$$f_{out} = (\frac{N}{M+1}) \cdot f_{ref}$$

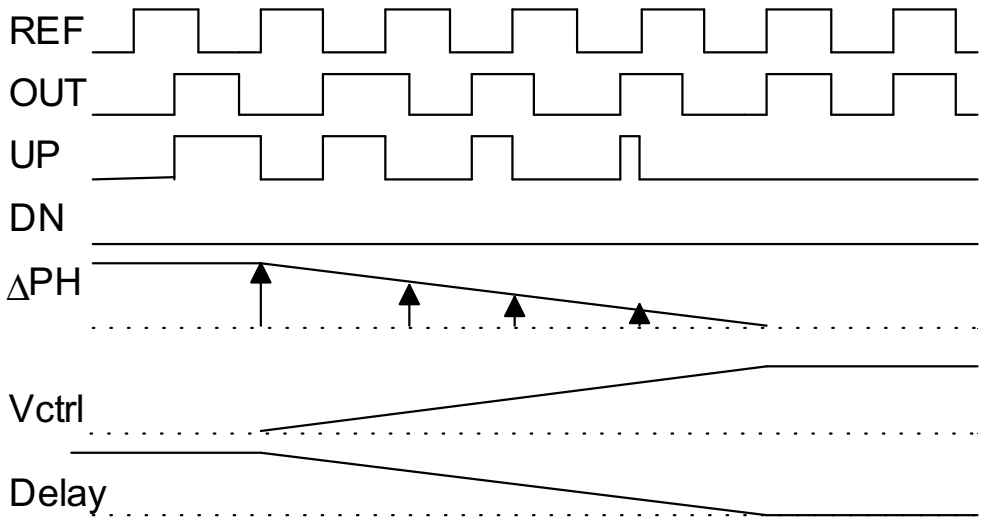
Delta-Sigma-modulator-based synthesizer



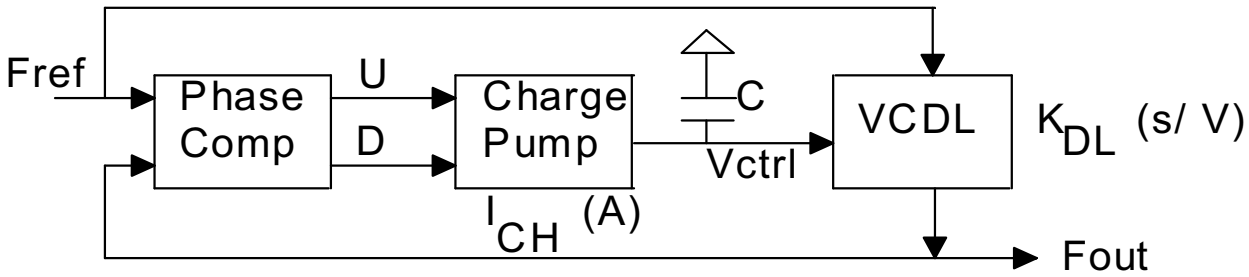
Analog Delay Locked Loop



VCDL: Voltage Controlled Delay Line



Analog Delay Locked Loop



Opened-Loop Response

$$D_O(s) = \left(\frac{D_I(s)}{T_{REF}} \cdot I_{CH} \right) \cdot \frac{K_{DL}}{s \cdot C}$$

$$\frac{D_O(s)}{D_I(s)} = \frac{K_{DL}}{s \cdot C} \cdot I_{CH} \cdot F_{REF} = H(s)$$

Analog Delay Locked Loop

Closed-Loop Response

$$D_O(s) = H(s) \cdot (D_I(s) - D_O(s))$$

$$\frac{D_O(s)}{D_I(s)} = \frac{H(s)}{1 + H(s)}$$

$$\frac{D_O(s)}{D_I(s)} = \frac{1}{1 + \frac{s \cdot C}{I_{CH} \cdot K_{DL} \cdot F_{REF}}}$$

$$\frac{D_O(s)}{D_I(s)} = \frac{1}{1 + s/\omega_N}$$ where ω_N (rad/s) is the loop bandwidth

$$\omega_N = I_{CH} \cdot K_{DL} \cdot F_{REF}/C$$

Design Strategy

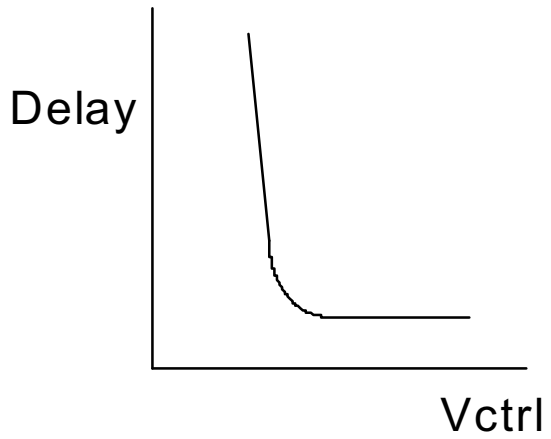
- ωn must be about a decade below Fref

$$\frac{\omega_N}{F_{REF}} = \frac{I_{CH} \cdot K_{DL}}{C} \leq \frac{\pi}{5}$$

- VCDL much have adequate delay range
- Locking Constraints
  - Reset phase comparator
  - Reset VCDL to minimum delay

Bandwidth Tracking

- Assume the symmetric load buffer is used to implement VCDL and the operating freq.,fclk, is smaller than its -3dB BW.



- fclk ↗ Delay time ↘
- fclk ↘ Delay time ↗ KDL ↗
- ω_n / Ref ↗
- Stability constraints will lead to a small operating range of the DLL

IEEE JSSC-31, pp. 1723-, Nov. 1996

Bandwidth Tracking

$$I_D = \frac{k}{2}(V_{Ctrl} - V_T)^2$$

$$g_m = k(V_{Ctrl} - V_T)$$

The delay for the n satge VCDL

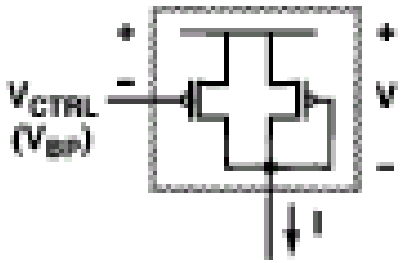
$$D = n \cdot t = \frac{n \cdot C_{EFF}}{k(V_{Ctrl} - V_T)} \text{ where } t \triangleq \frac{C_{EFF}}{g_m}$$

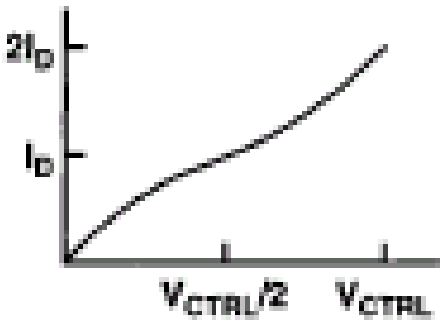
$$K_{DL} = \left|\frac{dD}{dV_{Ctrl}}\right| = \frac{C_B}{4 \cdot I_D} \text{ where } C_B \triangleq 2 \cdot n \cdot C_{EFF}$$

Let the charge pump current I_{CH} be

$$I_{CH} = x \cdot (2 \cdot I_D)$$

$$\frac{\omega_N}{\omega_{REF}} = \frac{x}{4\pi} \cdot \frac{C_B}{C}$$





Duty Cycle Correction

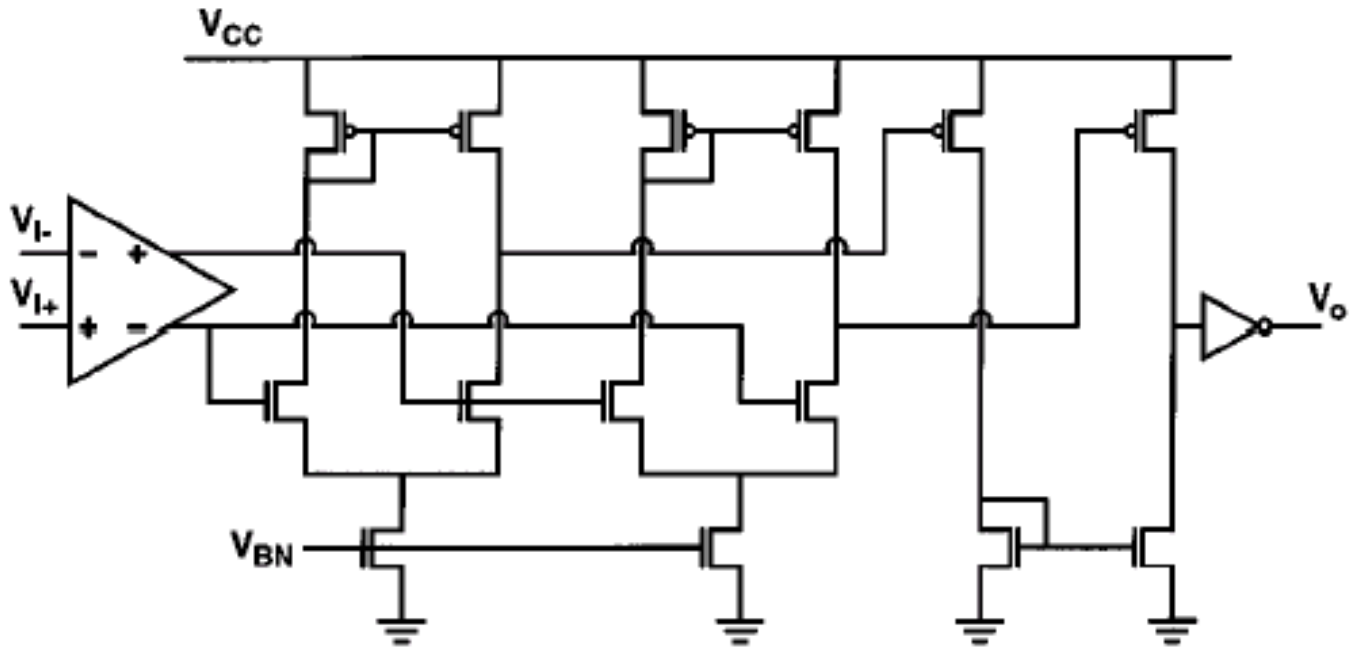
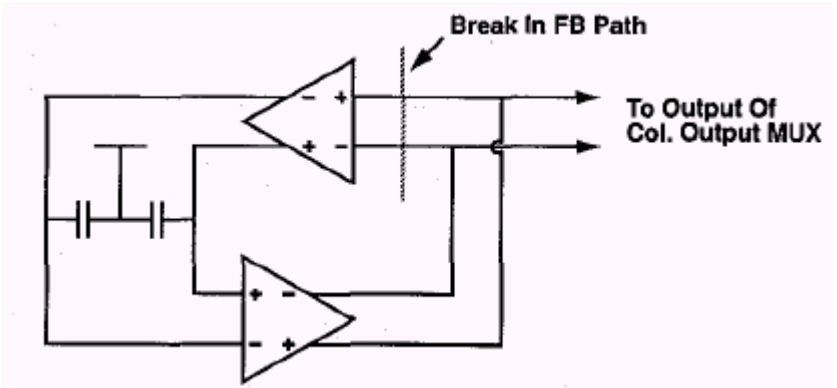
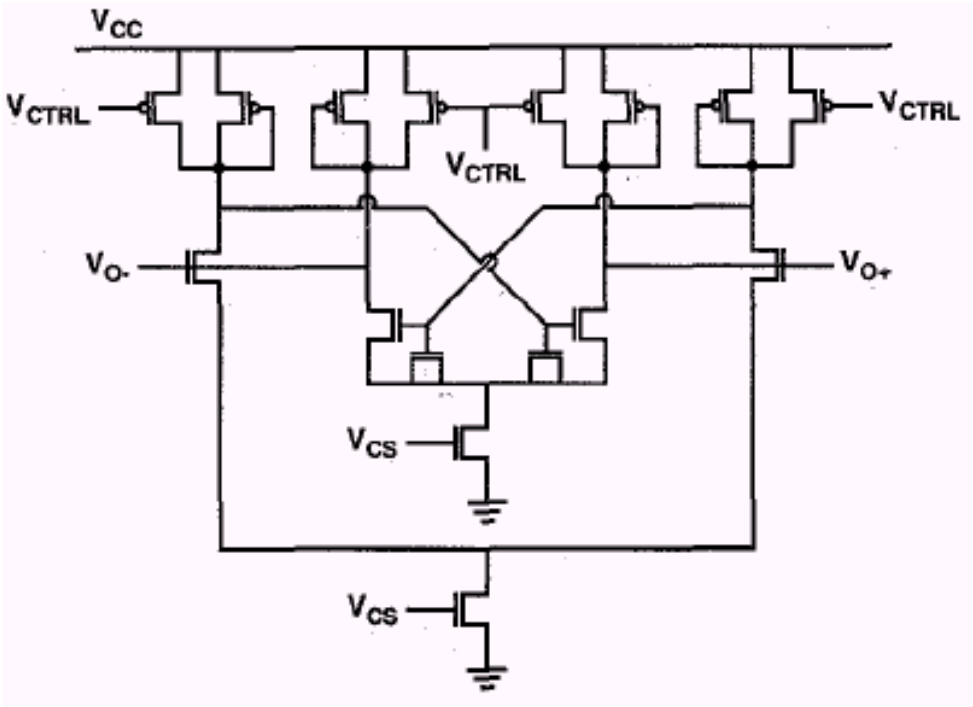


Fig. 15. Differential-to-single-ended converter with 50% duty cycle output.

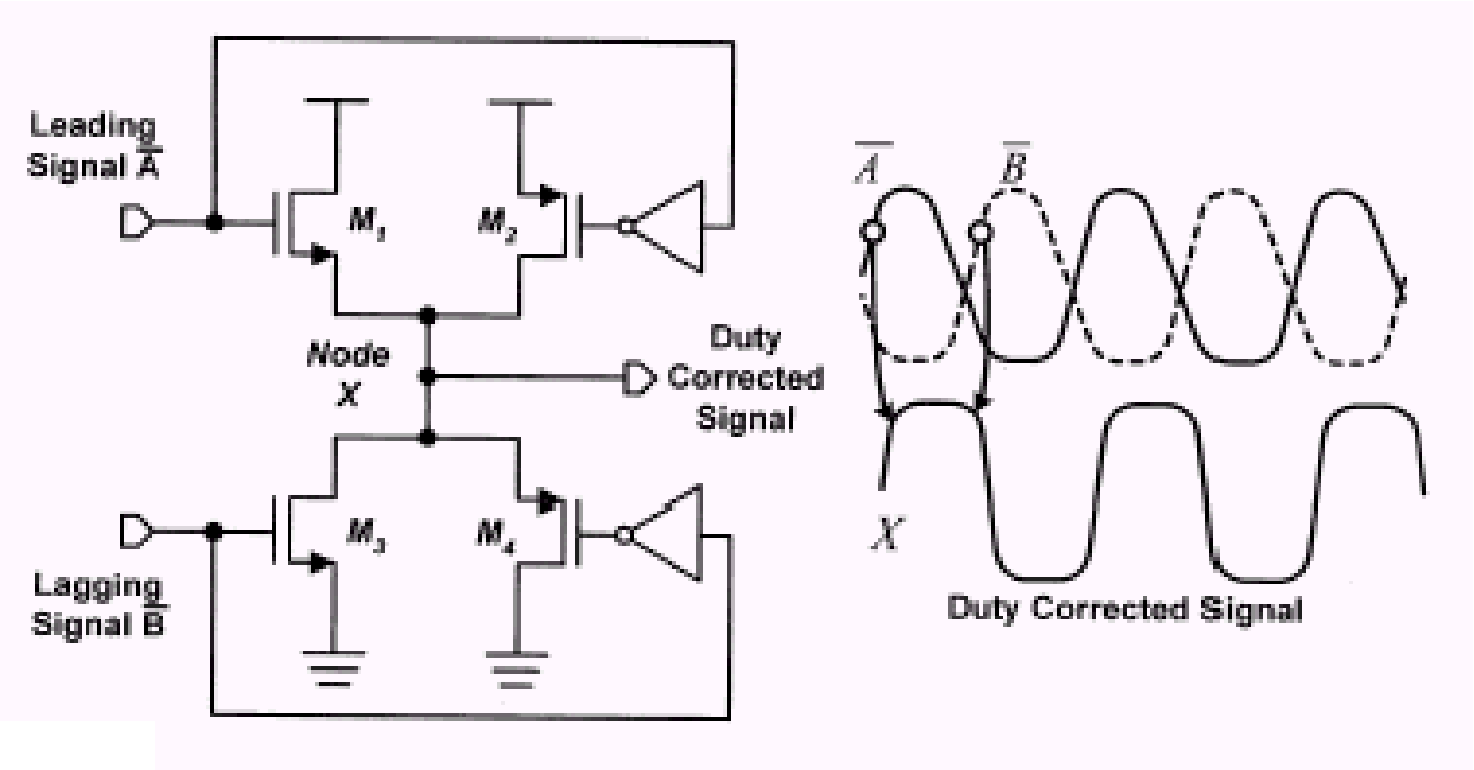
Duty Cycle Correction





IEEE JSSC-28, pp. 1273-, Dec. 1993

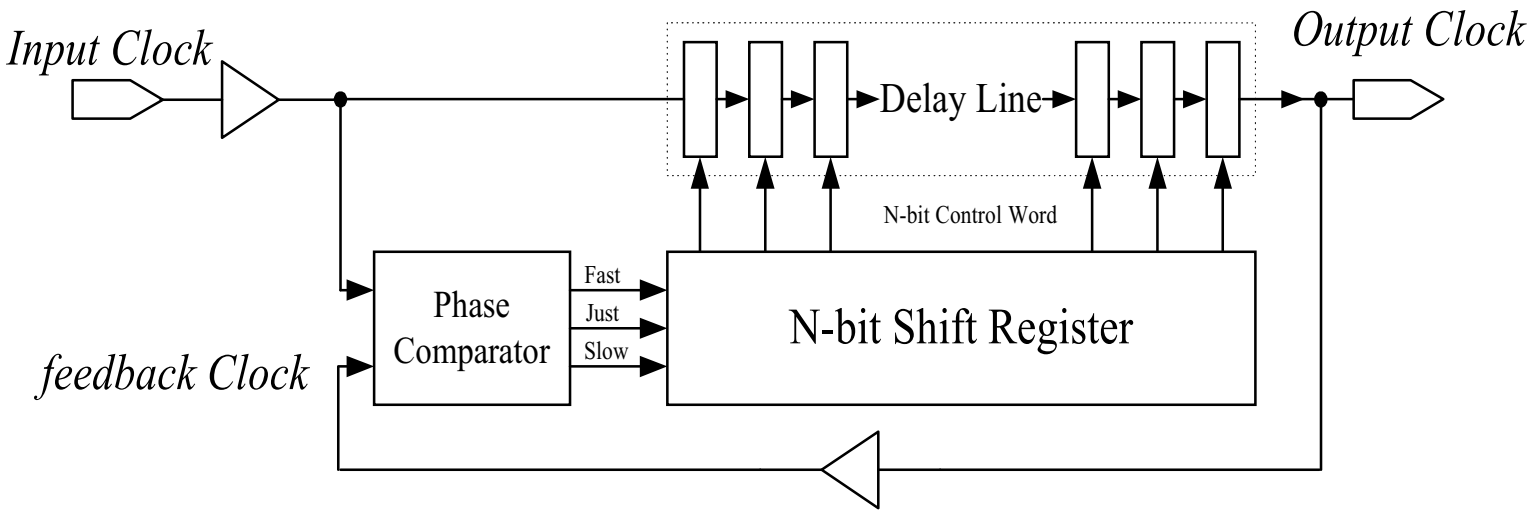
Duty Cycle Correction



ISSCC'99, pp. 346-, Feb. 1999

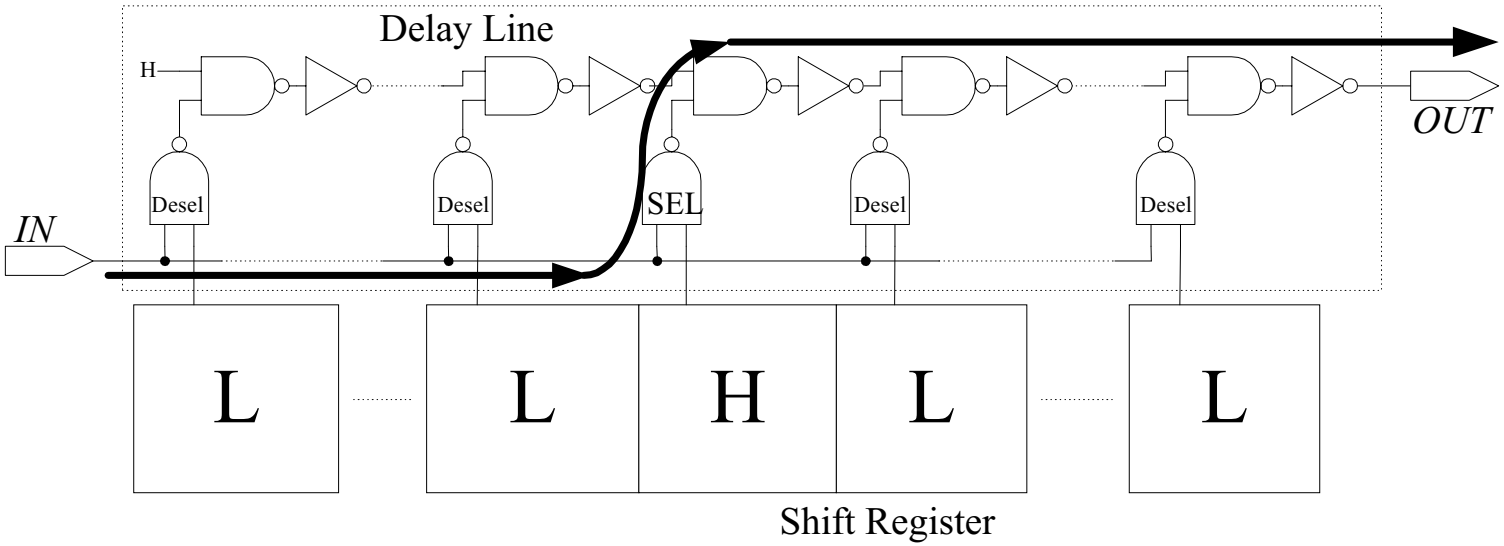
Digital Delay Locked Loop

- Register-controlled DLL

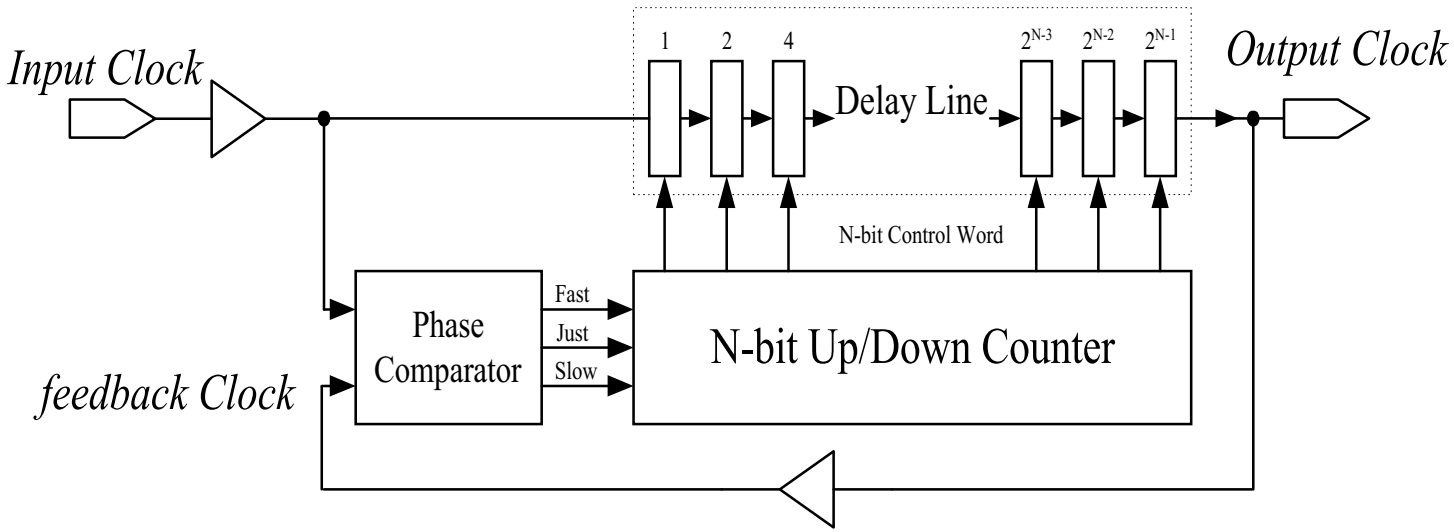


IEEE JSSC-32, pp. 1728-, Nov. 1997,

Register-controlled DLL

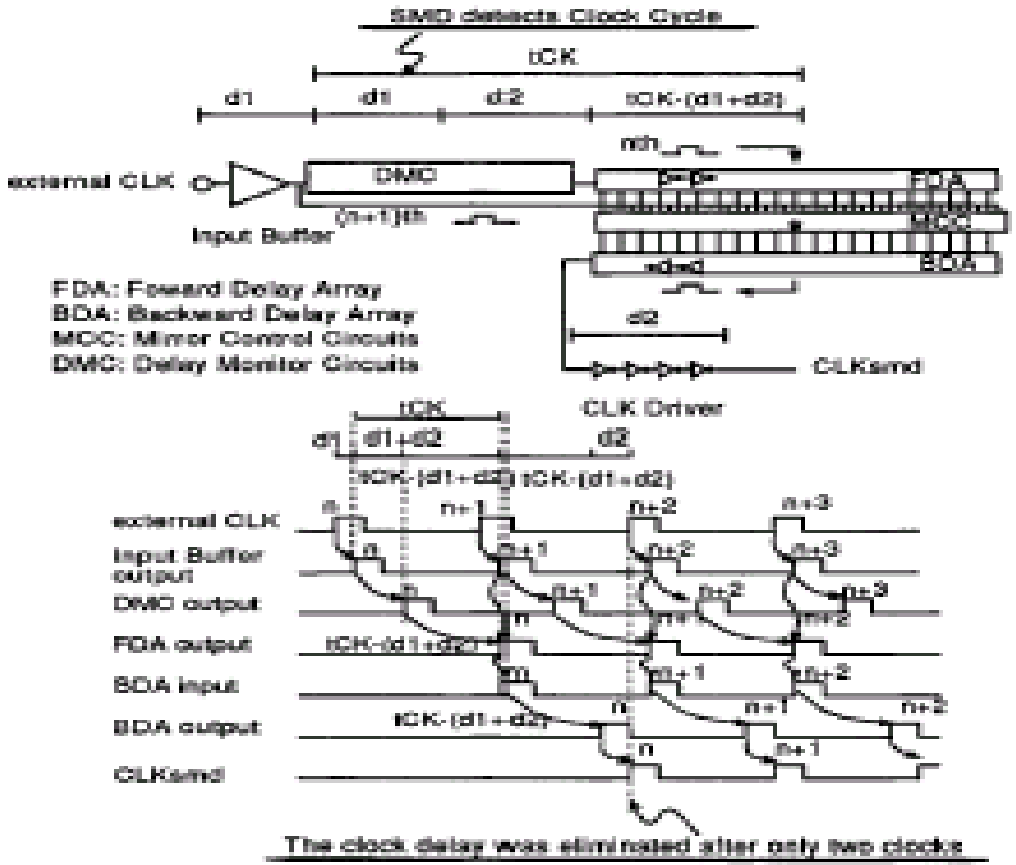


Counter-controlled DLL



IEEE CICC, pp. 163-, 1995, IEICE Trans. Electron., E79-C, pp.798-, June 1996.

Synchronous Mirror DLL



IEEE JSSC-31, pp. 1656-, Nov. 1996, IEEE JSSC-34, pp. 372, Marxh. 1999

Synchronous Mirror DLL

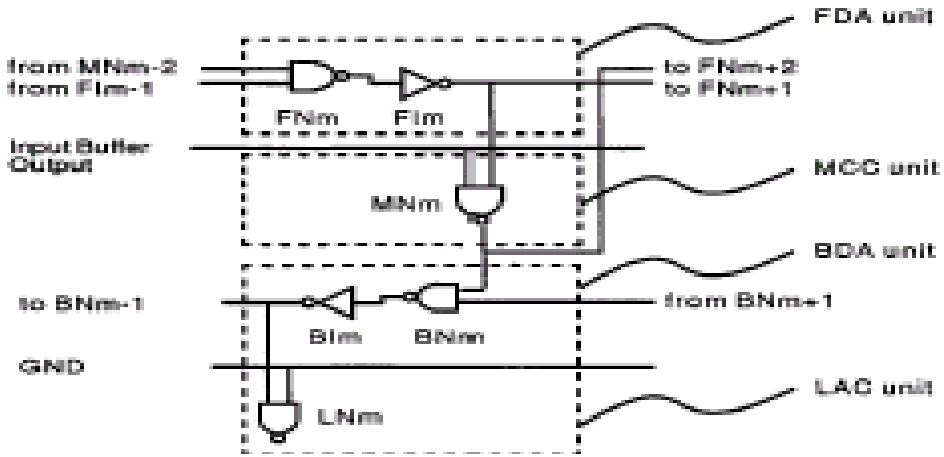
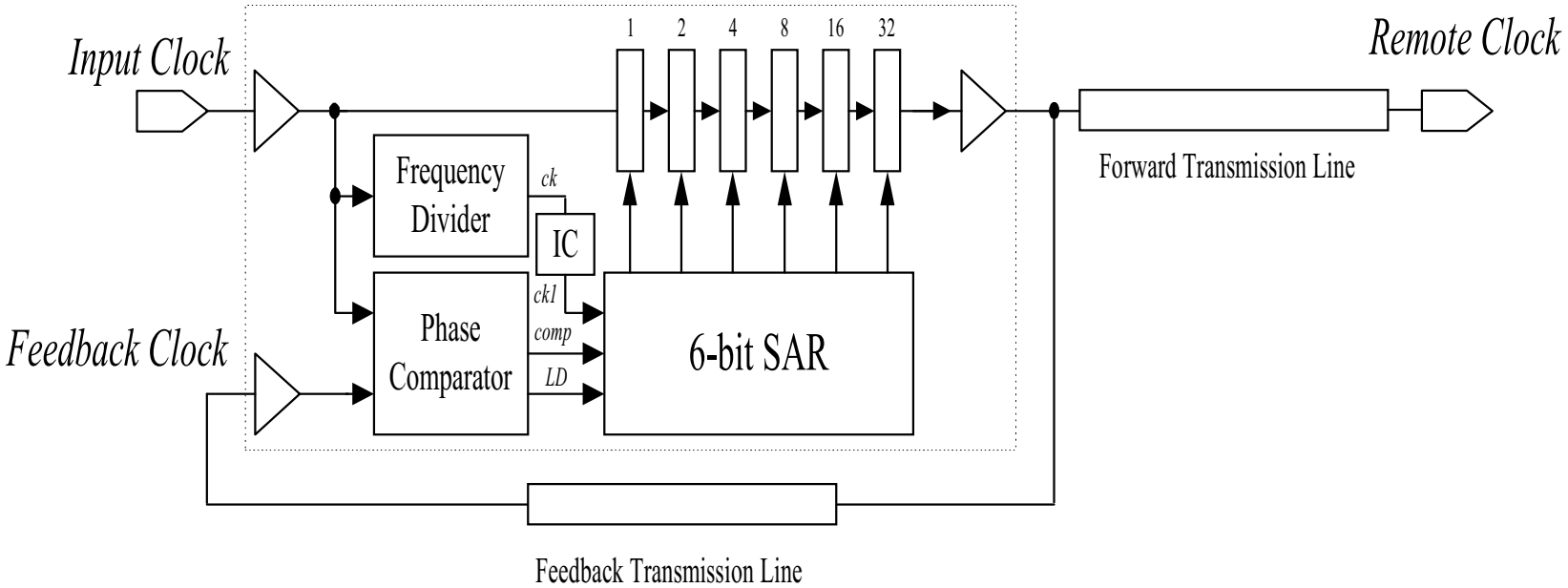
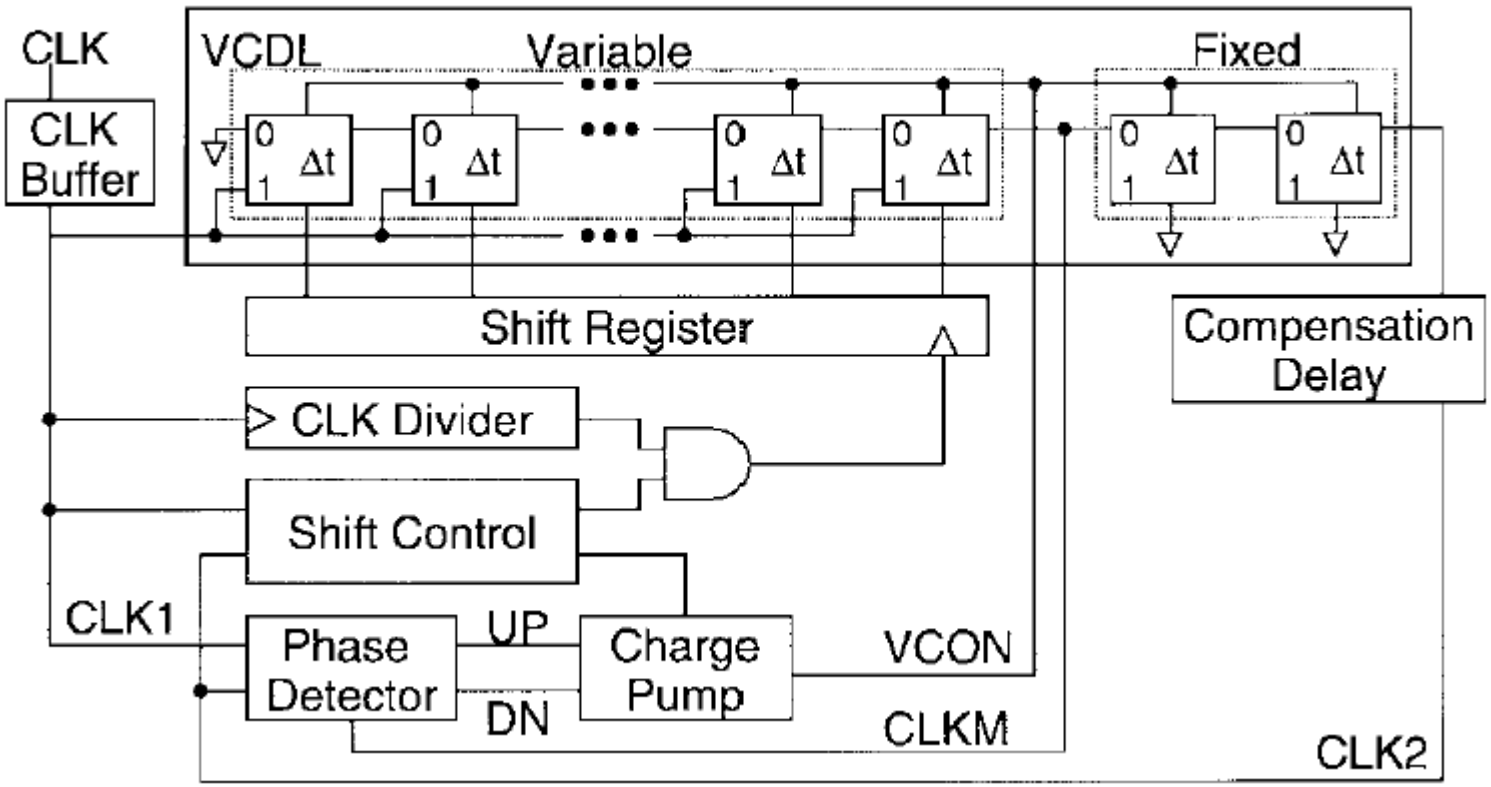


Fig. 10. SMD unit. The operation is explained using the ▬th clock pulse and (▬ ▬)th clock pulse. The ▬▬ output is ▬ (low) standby. The ▬▬ and ▬▬ output is ▬ (high) standby. When the ▬th clock ▬ pulse goes into the FDA unit from ▬▬ ▬▬ and the input buffer output clock of (▬ ▬)th goes into the MCC unit simultaneously, the ▬▬ output becomes ▬. Then both the ▬▬ and the ▬▬ ▬▬ output become ▬. The ▬ output of ▬▬ goes backward on the BDA as the ▬ pulse. The ▬ output of the ▬▬ ▬▬ eliminates the ▬ pulse on the FDA.

SAR-controlled DLL

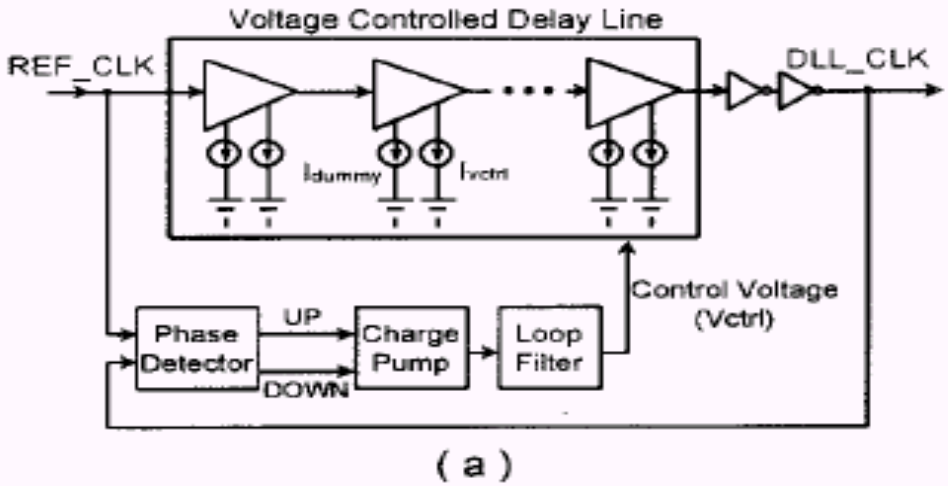


Mixed mode DLL



IEEE JSSC-34, pp. 1589-, Nov. 1999, IEE Electronics Letters, vol. 35, pp. 1700-, Sept. 1999

Range Problem



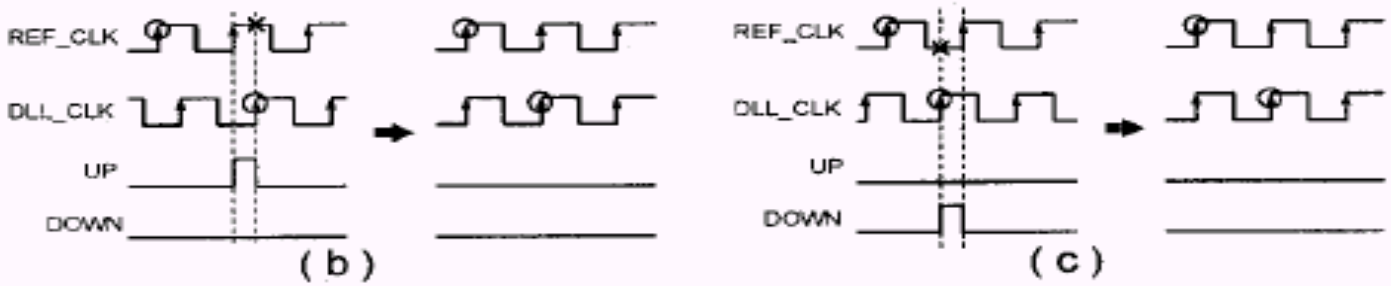


Fig. 1. (a) Block diagram of a conventional DLL, (b) Synchronization mechanism when DLL_CLK lags REF_CLK, and (c) Synchronization mechanism when DLL_CLK leads REF_CLK.

(b)PD charges

V_{ctrl} increases

T_D decreases

(c)PD discharges

V_{ctrl} decreases

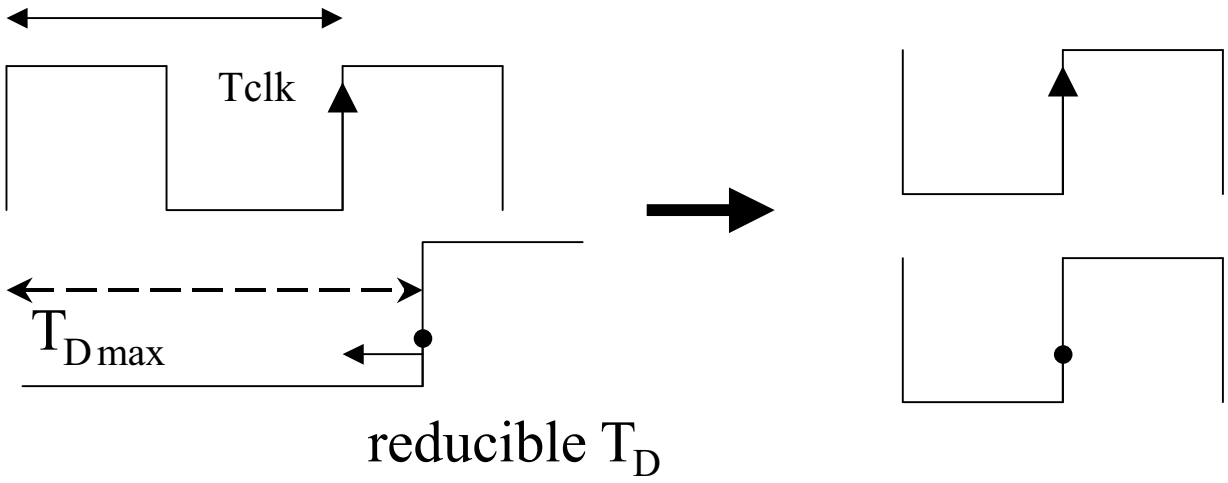
T_D increases

IEEE CICC, pp. 299-, May 1998

Range Problem

$T_{clk} < T_{D\,max} < \frac{3}{2} T_{clk}$

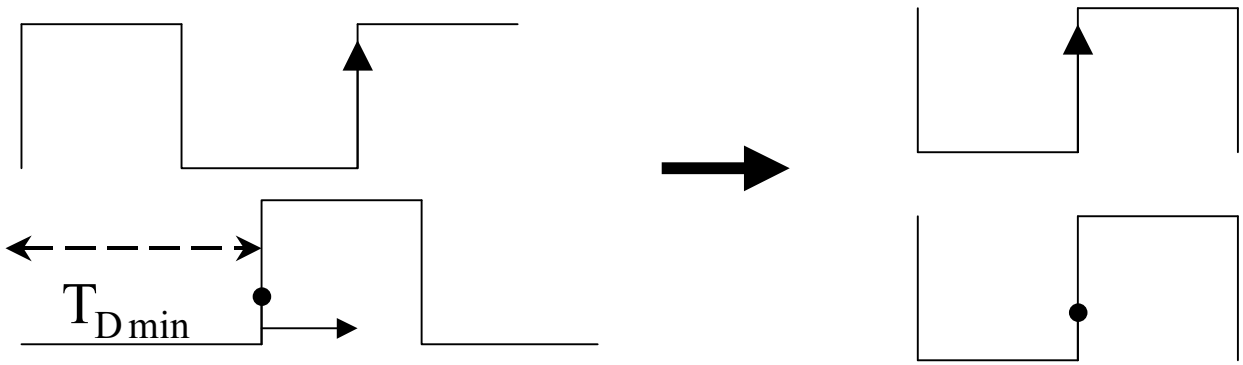
$T_{D\,max}$ the max dely when V_{ctrl} min



reducible T_D

$\frac{1}{2} T_{clk} < T_{D\,min} < T_{clk}$

$T_{D\,min}$ the min dely when V_{ctrl} max



added T_D

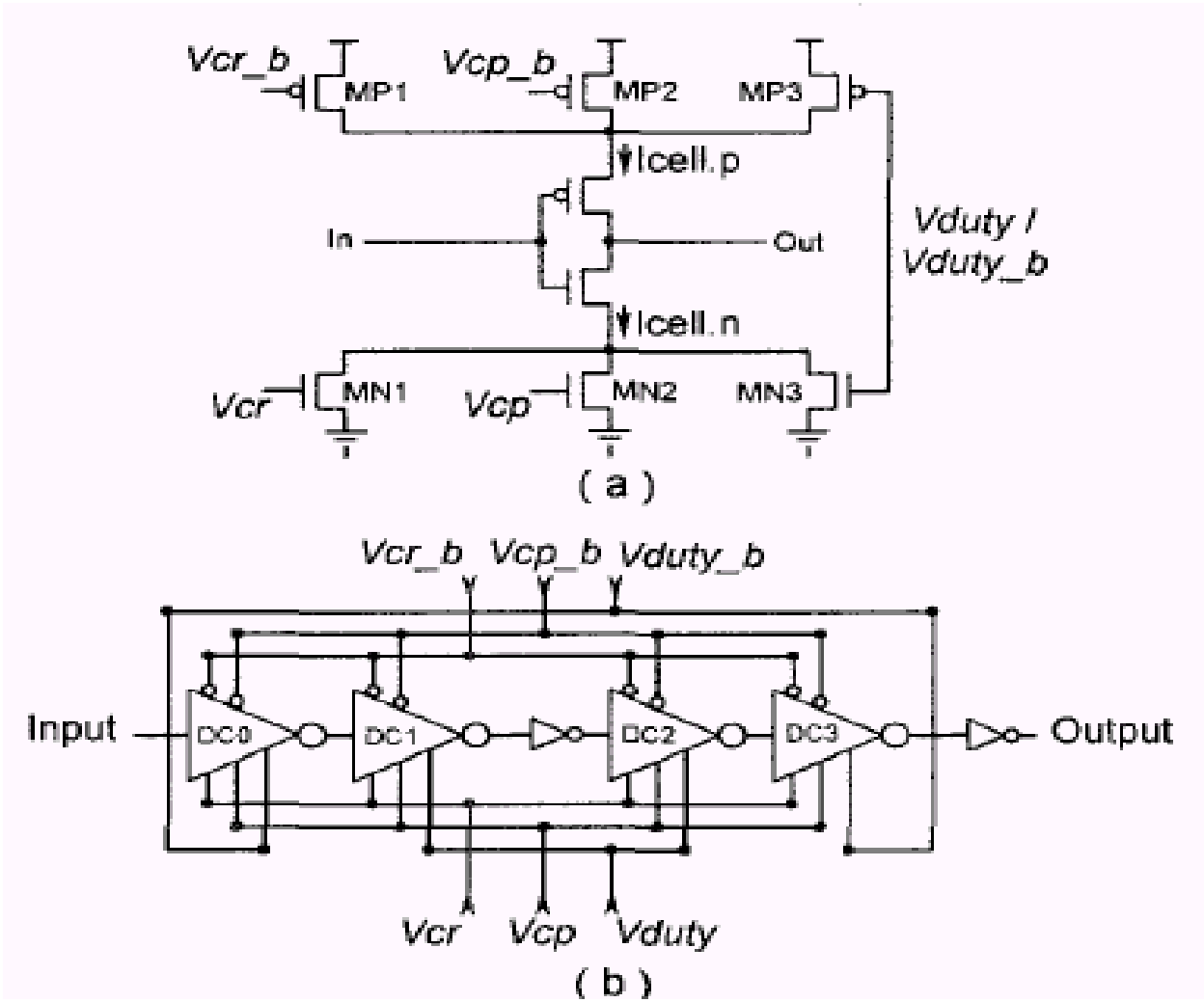
Range Problem

$$T_{clk} < T_{D\max} < \frac{3}{2}T_{clk} \qquad \frac{1}{2}T_{clk} < T_{D\min} < T_{clk}$$

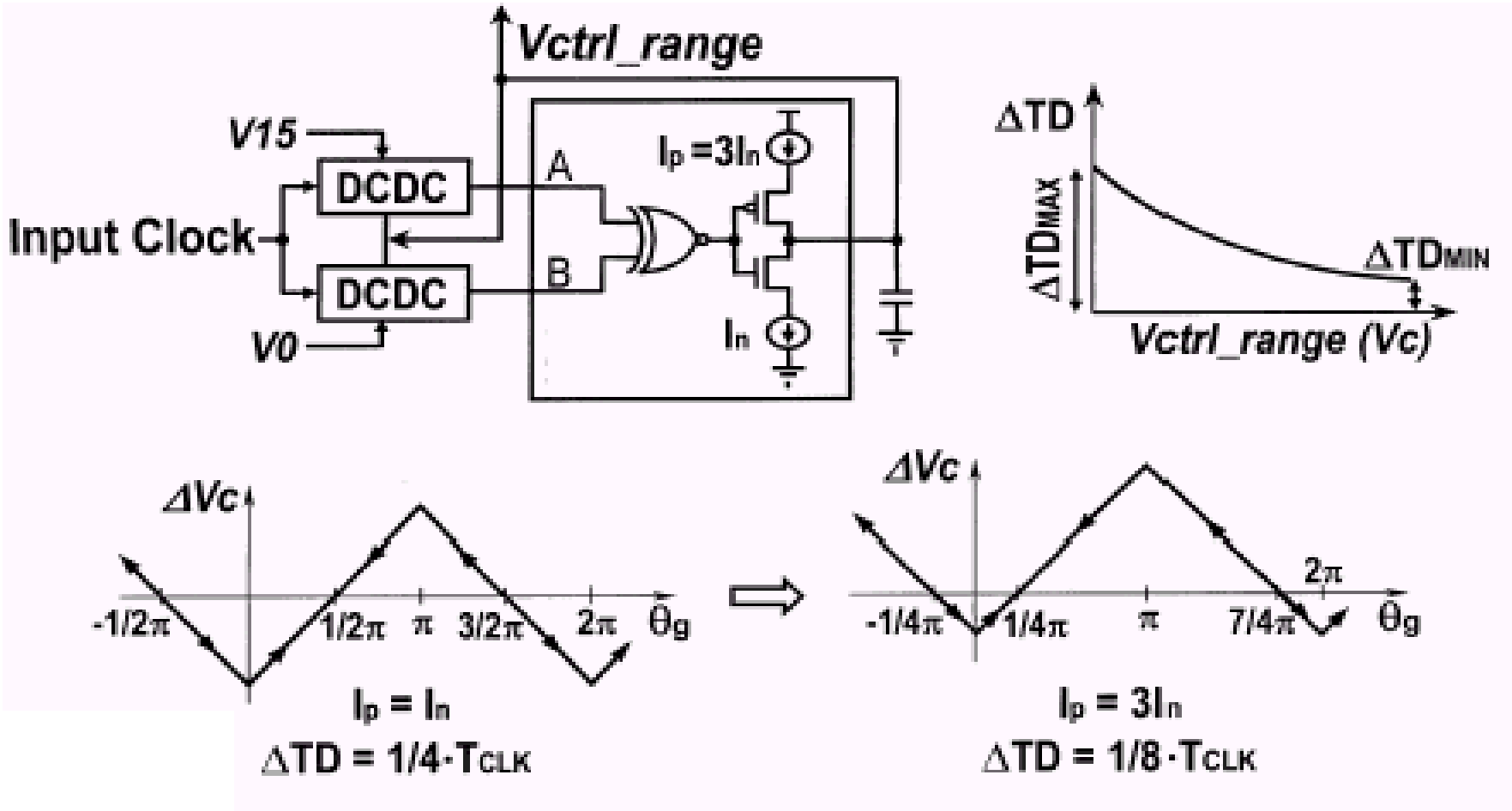
$$\max\left\{T_{D\min}, \frac{2}{3}T_{D\max}\right\} < T_{clk} < \min\left\{2T_{D\min}, T_{D\max}\right\}$$

If $T_{D\max} > 3T_{D\min} \Rightarrow$ no solution

Delay Cell Group



Range Problem



Range Problem

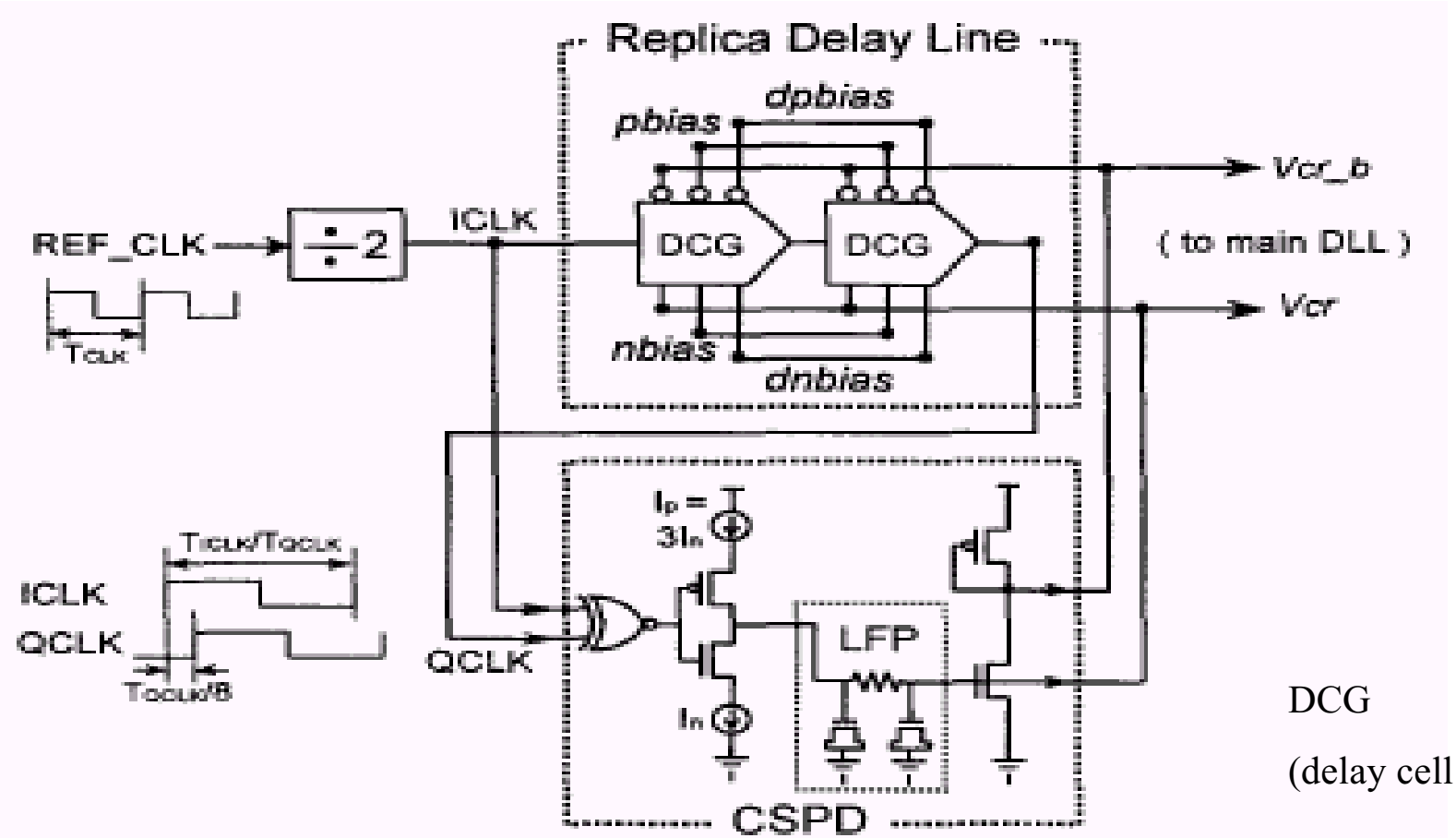
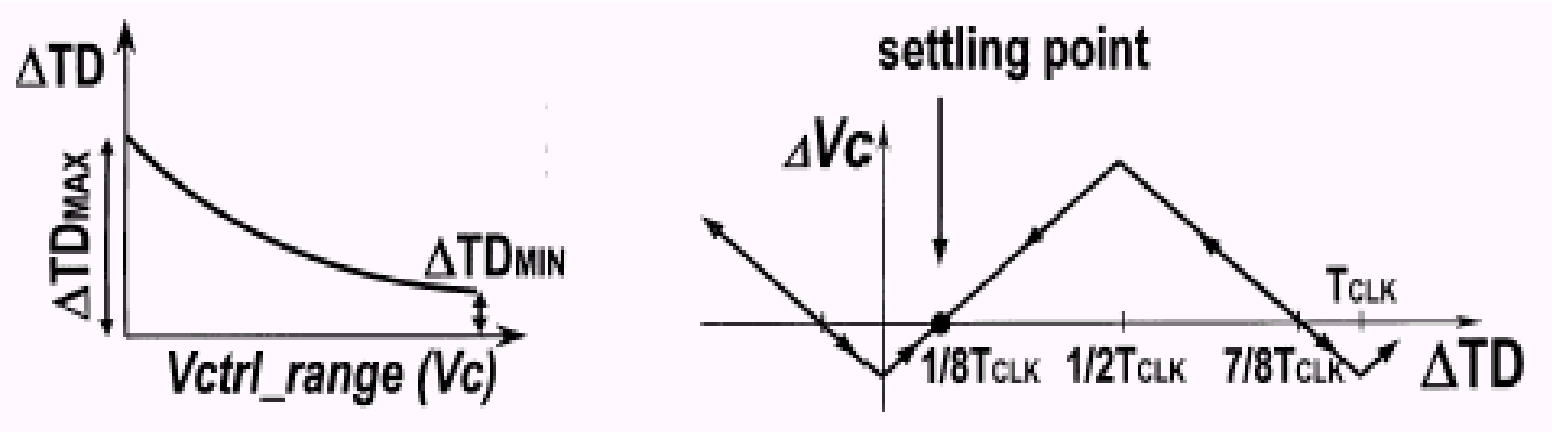


Fig. 2. Replica delay loop to generate control-signals for the core DLL.

DCG

(delay cell group)

Range Problem



$0 < TDR_{MIN} < 1/8\ T_{QCLK}$ and $1/8\ T_{QCLK} < TDR_{MAX} < 7/8\ T_{QCLK}$,

$\max\{8\ TDR_{MIN},\ 8/7\ TDR_{MAX}\} < T_{QCLK} < 8\ TDR_{MAX}$,

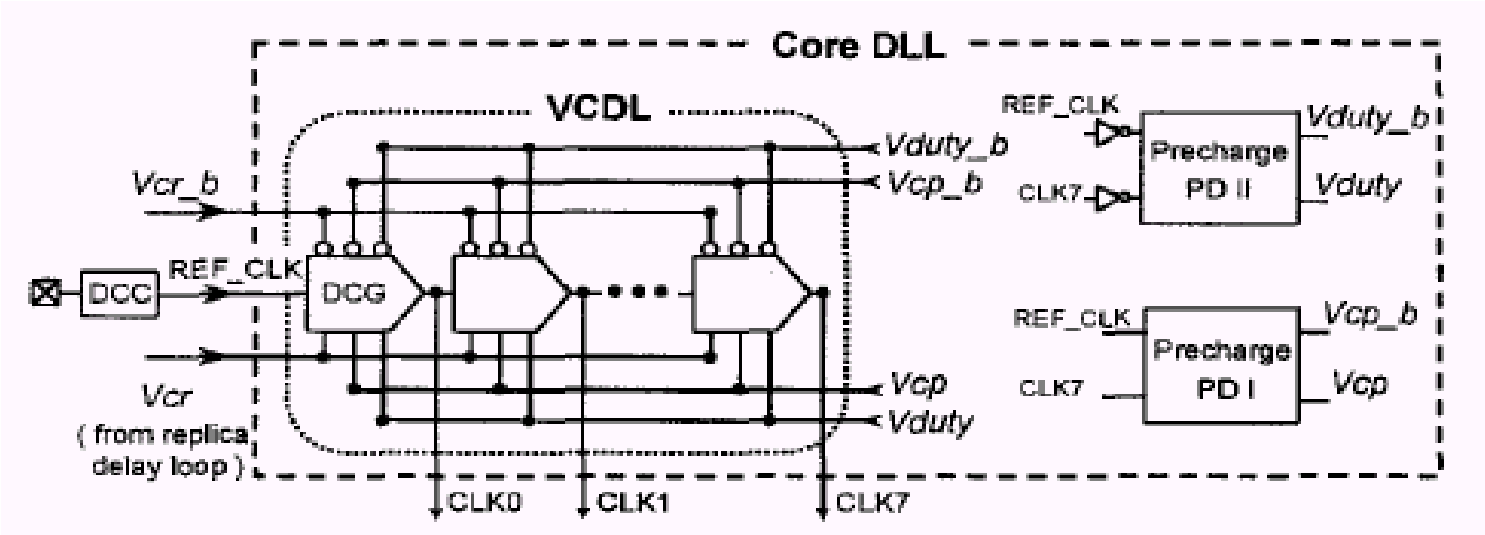
$8/7\ TDR_{MAX} < T_{QCLK} < 8\ TDR_{MAX}$, if $TDR_{MAX} > 7\ TDR_{MIN}$

$8\ TDR_{MIN} < T_{QCLK} < 8\ TDR_{MAX}$, if $TDR_{MAX} < 7\ TDR_{MIN}$

$\because 2T_{clk} = T_{Qclk}$ and $TDR = 2TDG$, TDG: the delay time of the DCG

$8\ TDG_{MIN} < T_{CLK} < 8\ TDG_{MAX}$, if $TDG_{MAX} < 7\ TDG_{MIN}$

Range Problem

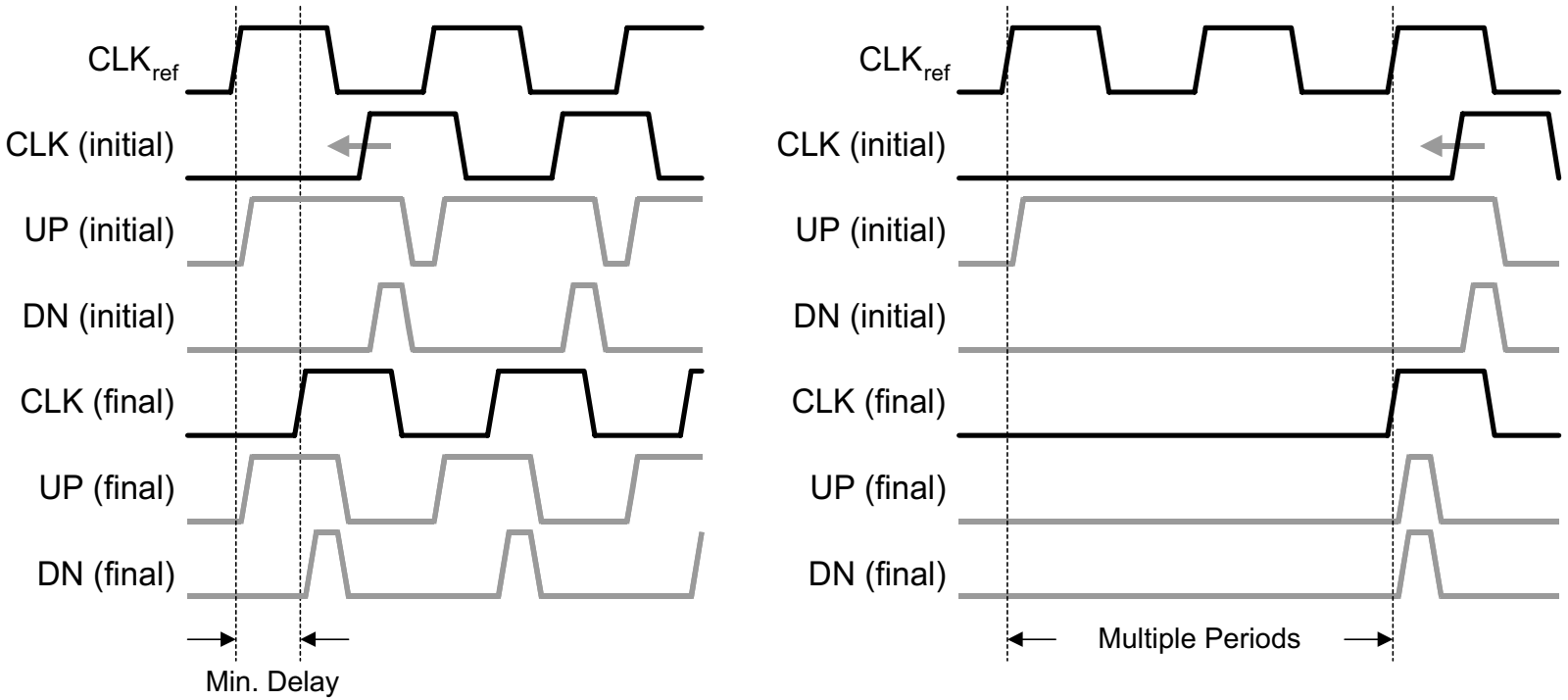


$\because TD = 8TDG$, TD: the delay time of the VCDL

$TD_{MIN} < T_{CLK} < TD_{MAX}$, if $TD_{MAX} < 7\ TD_{MIN}$,

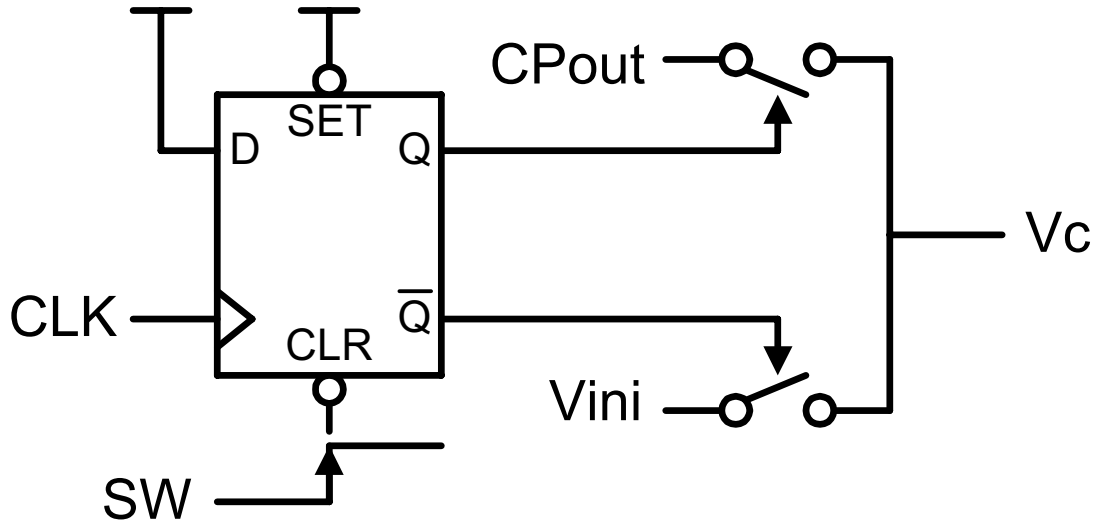
$1/TD_{Max} < f_{CLK} < 1/TD_{MIN}$, if $TD_{MAX} < 7\ TD_{MIN}$.

Harmonic Locking Problem



(a) Unable to Lock

(b) False Lock

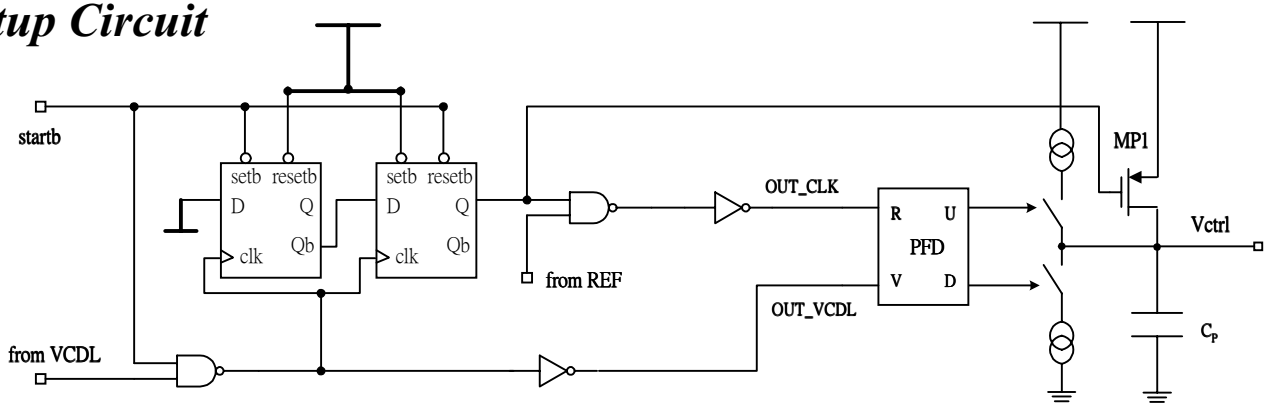


Initially, SW = Low and reset Q=Low, and Vc is connected to Vini.

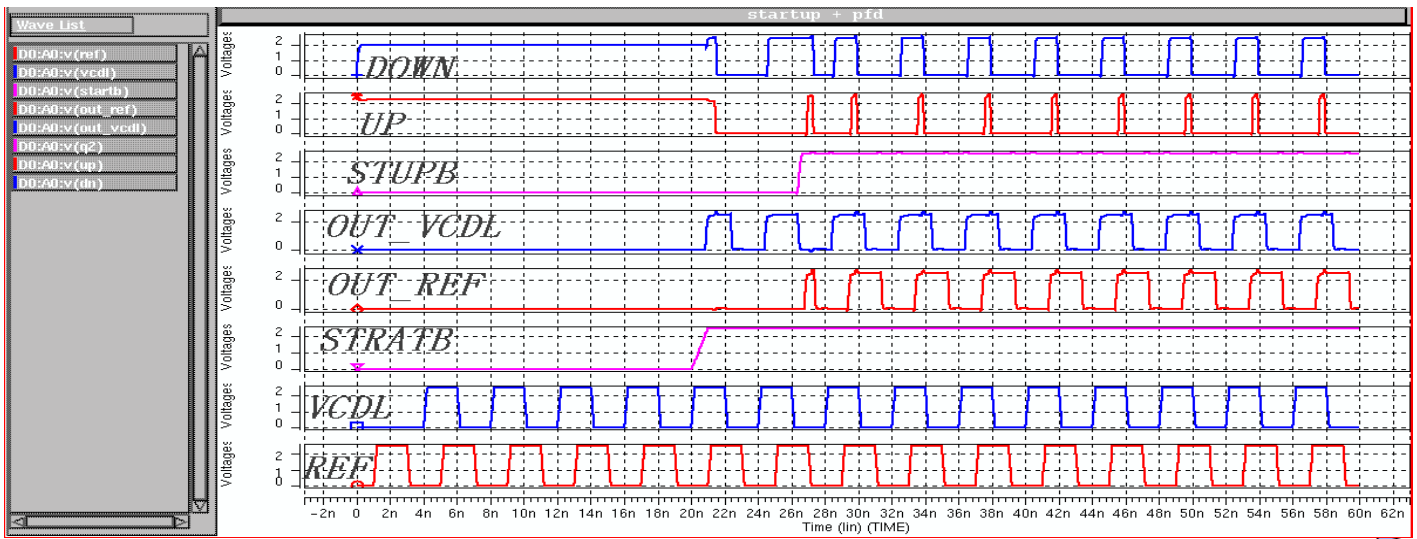
After SW =High, Q=High, connecting Vc to CPout, the capacitor would be charged to reduce the phase difference until DLL is in locked state.

Startup Circuit for Harmonic Locking Problem

- ***Startup Circuit***



- ***Simulation Diagram***



Z-domain Delay-Locked Loop

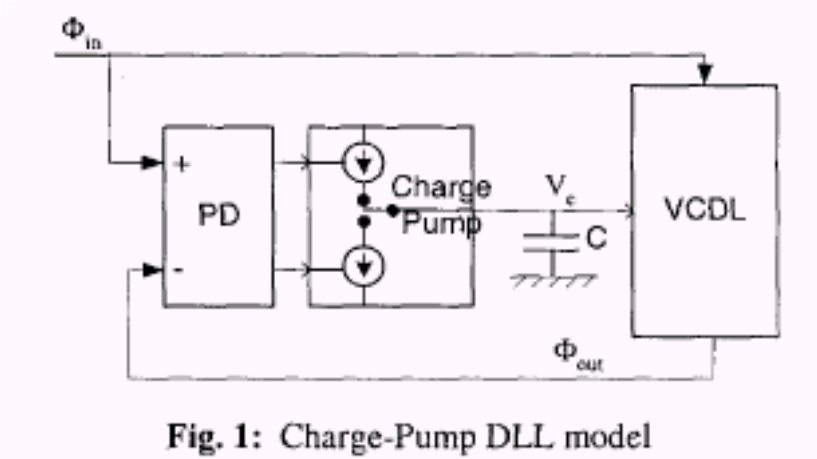


Fig. 1: Charge-Pump DLL model

$$\Phi_{out}(t) = \Phi_{in}(t - \alpha T) - K_{VCDL} \cdot V_C(t) \quad \text{and} \quad V_C(t) = \frac{\Phi_{in}(t) - \Phi_{out}(t)}{C} \int_{-\infty}^{t} I_C(t)dt$$

where aT (a>1) is the total delay of the VCDL

$$\Phi_{out}(n) = \Phi_{in}(n - \alpha) - K_{VCDL} \cdot V_C(n) \qquad V_C(n) = \frac{\Phi_{in}(n-1) - \Phi_{out}(n-1)}{C} I_P T$$

$$\Phi_{out}(n) = \Phi_{in}(n - \alpha) - K_T \cdot [\Phi_{in}(n-1) - \Phi_{out}(n-1)] \quad \textit{where} \quad K_T = \frac{K_{VCDL} I_P T}{C}$$

$$H(z) = \frac{\Phi_{out}(z)}{\Phi_{in}(z)} = \frac{1 - K_T z^{\alpha-1}}{z^{\alpha} - K_T z^{\alpha-1}}$$

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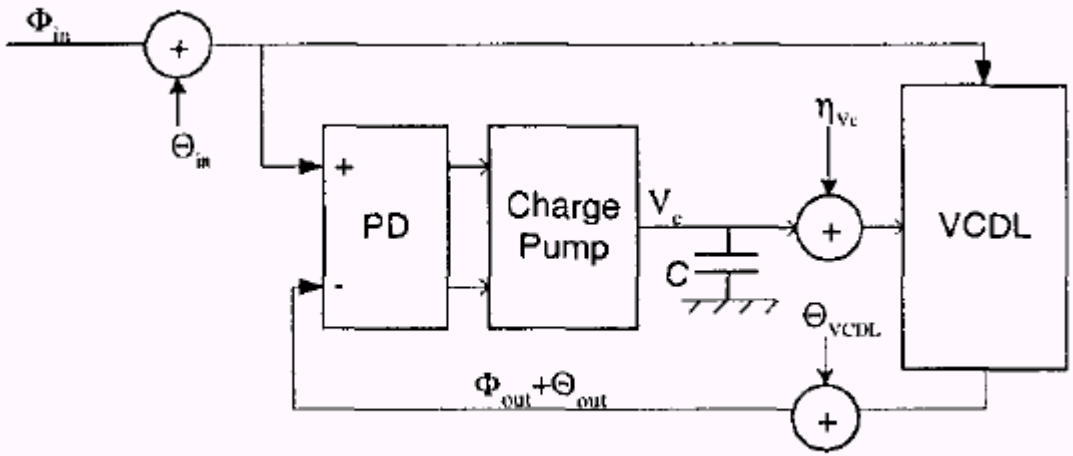


Fig. 2 - Charge-Pump DLL jitter model

VCDL jitter $$J_{VCDL}(z) = \frac{\theta_{out}(z)}{\theta_{VCDL}(z)} = \frac{K_T}{z - K_T}$$

Control voltage, Vc, jitter $$J_{V_C}(z) = \frac{\theta_{out}(z)}{\theta_{V_C}(z)} = K_{VCDL}$$

Input jitter $$J_{input}(z) = H(z)$$

1. *Assume* $\theta_{VCDL}(z) = \frac{2\pi}{T}\delta_n$: *an impulse with random amplitude*

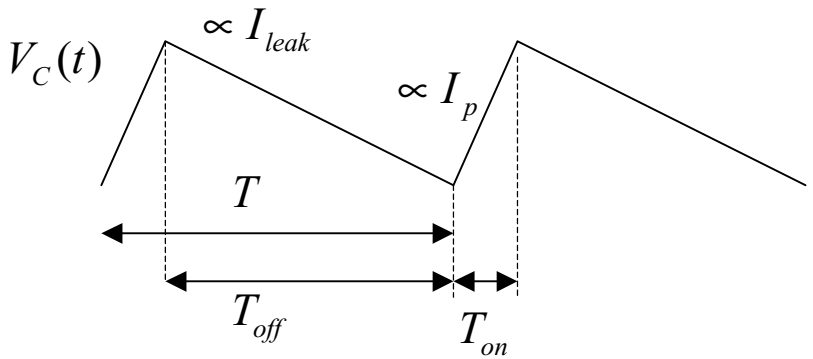
$$\theta_{out}(z) = J_{VCDL}(z)\cdot\theta_{VCDL}(z) = \frac{K_T}{z-K_T}\cdot\frac{2\pi}{T}\delta_n \quad inverse \quad z-Tx \Rightarrow \theta_{out}^{Total}(n) = \frac{2\pi}{T}\sum_{k=-\infty}^{n}\delta_k K_T^{n-k}$$

$$E[\theta_{out}^{Total}(n)\cdot\theta_{out}^{Total}(n)] = (\frac{2\pi}{T})^2\sum_{i=-\infty}^{n}E(\delta_i\delta_i)(K_T^{n-i})^2 = (\frac{2\pi}{T})^2\frac{\sigma_\varepsilon^2}{1-K_T^2} \Rightarrow \sigma_{VCDL} = \frac{2\pi}{T}\frac{\sigma_\varepsilon}{\sqrt{1-K_T^2}}$$

2. *Assume* $\theta_{in}(z) = \frac{2\pi}{T}\delta_n$: *an impulse with random amplitude*

$$\theta_{out}(z) = J_{in}(z)\cdot\theta_{in}(z) \qquad E[\theta_{out}^{Total}(n)\cdot\theta_{out}^{Total}(n)] = (\frac{2\pi}{T})^2\sigma_{in}^2[\frac{(K_T^\alpha-1)^2}{1-K_T^2} + \frac{K_T^2(1-K_T^{2(\alpha-1)})}{1-K_T^2}]$$

3. *Assume* $V_c(t)$ *is described as follows*



If $T_{off} >> T_{on}$

$$E[V_C^2(t)] = K_{VCDL}^2\frac{T^2 I_{leak}^2}{12\cdot C^2} \qquad \sigma_{VCDL} = K_{VCDL}\frac{T\cdot I_{leak}}{\sqrt{12}\cdot C}$$