LECTURE 090 –FILTERS AND CHARGE PUMPS

Objective

The objective of this presentation is to examine the circuits aspects of loop filters and charge pumps suitable for PLLs in more detail.

Outline

- Filters
- Charge Pumps
- Summary

FILTERS

Why Does the PLL Need a Filter?

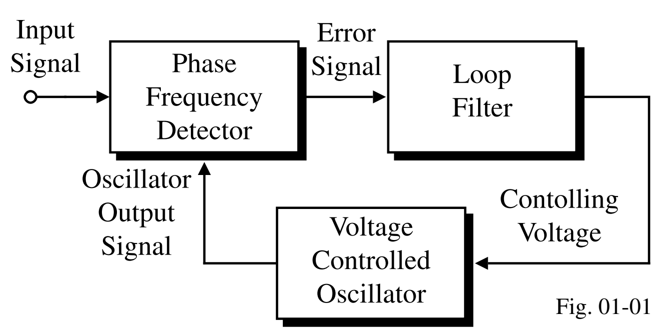


Fig. 01-01

The loop filter is important to the performance of the PLL.

1.) Removes high frequency noise of the detector
2.) Influences the hold and capture ranges
3.) Influences the switching speed of the loop in lock.
4.) Easy way to change the dynamics of the PLL

Passive Loop Filters

1.) $F(s) = \dfrac{R_1}{R_1 + \dfrac{1}{sC_1}} = \dfrac{1}{sR_1C_1 + 1} = \dfrac{1}{1 + s\tau_1}, \qquad \tau_1 = R_1C_1$

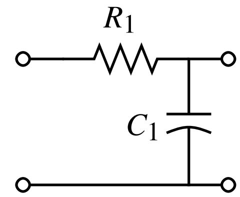


Fig. 3.1-26

2.) $F(s) = \dfrac{R_2 + \dfrac{1}{sC}}{R_1 + R_2 + \dfrac{1}{sC}} = \dfrac{sCR_2 + 1}{sC\,(R_1 + R_2) + 1} = \left(\dfrac{1 + s\tau_2}{1 + s\tau_1}\right)$

$\tau_1 = C(R_1 + R_2)$ and $\tau_2 = R_2C$

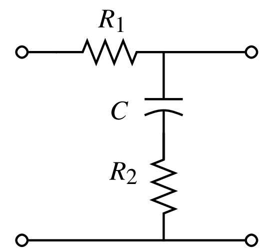


Fig. 3.1-27

Advantages:
- Linear
- Relatively low noise
- Unlimited frequency range

Disadvantages:
- Hard to integrate when the values are large (C>100pF and R > 100kΩ)
- Difficult to get a pole at the origin (increase the order of the type of PLL)

Active Filters

1.) Active lag filter-I

$$F(s) = -\frac{R_2 + \dfrac{1}{sC_2}}{R_1 + \dfrac{1}{sC_1}} = -\left(\frac{C_1}{C_2}\right)\left(\frac{sR_2C_2 + 1}{sR_1C_1 + 1}\right)$$

$$= -\left(\frac{C_1}{C_2}\right)\left(\frac{s\tau_2 + 1}{s\tau_1 + 1}\right), \quad \tau_1 = R_1C_1 \text{ and } \tau_2 = R_2C_2$$

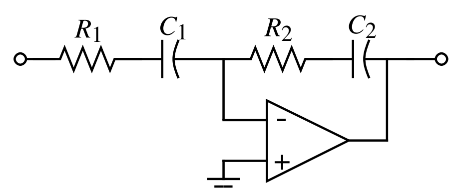


Fig. 3.1-28

2.) Active lag filter – II

$$F(s) = -\frac{\dfrac{R_2\dfrac{1}{sC_2}}{R_2 + \dfrac{1}{sC_2}}}{\dfrac{R_1\dfrac{1}{sC_1}}{R_1 + \dfrac{1}{sC_1}}} = -\left(\frac{R_2}{R_1}\right)\left(\frac{sR_1C_1+1}{sR_2C_2+1}\right) = -\left(\frac{R_2}{R_1}\right)\left(\frac{s\tau_1 + 1}{s\tau_2 + 1}\right)$$

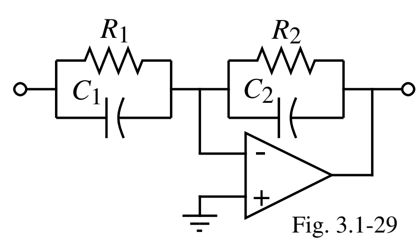


Fig. 3.1-29

Active Filters - Continued

3.) Active PI filter.

$$F(s) = -\frac{R_2 + \frac{1}{sC_2}}{R_1} = -\left(\frac{sR_2C_2 + 1}{sR_1C_2}\right) = -\left(\frac{s\tau_2 + 1}{s\tau_1}\right)$$

$\tau_1 = R_1C_2$ and $\tau_2 = R_2C_2$

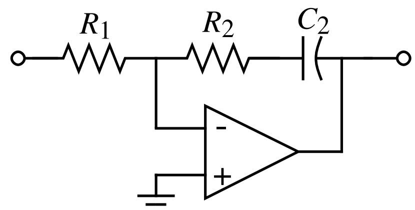


Fig. 3.1-30

Advantages:

- Can get poles at the origin
- Can reduce the passive element sizes using transresistance

We can show that $R_1(\text{eq.}) = 2R_1 + \frac{R_1{}^2}{R_x}$

Assume $R_1 = 10\text{k}\Omega$ and $R_x = 10\Omega$

gives $R_1(\text{eq.}) = 20\text{k}\Omega + \frac{100{,}000\text{k}\Omega}{10\Omega} \approx 10\text{M}\Omega$

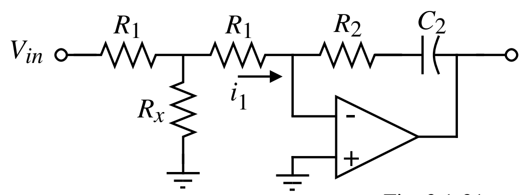


Fig. 3.1-31

Disadvantages:

- Noise
- Power
- Frequency limitation

Active Filters – Continued

Cancellation of the temperature/voltage dependence on the Tee transresistance:

Let $R_T = 2R_1 + \frac{R_1{}^2}{R_x}$

Differentiate R_T with respect to x where $x = T$ or V.

$$\frac{dR_T}{dx} = 2\frac{dR_1}{dx} + \frac{2R_1dR_1}{R_x\ dx} - \frac{R_1{}^2dR_x}{R_x{}^2\ dx} = \left(2 + \frac{2R_1}{R_x}\right)\frac{dR_1}{dx} - \left(\frac{R_1{}^2}{R_x{}^2}\right)\frac{dR_x}{dx}$$

Setting the above = 0 and assuming that $\frac{dR_1}{dx} = \frac{dR_x}{dx}$, gives

$$\left(\frac{R_1}{R_x}\right)^2 - 2\frac{R_1}{R_x} - 2 = 0 \quad \Rightarrow \quad R_1 = 2.732R_x \quad \Rightarrow \quad R_T = 12.9282R_x$$

Design:

1.) Choose R_T. 2.) Solve for R_x. 3.) Solve for R_1.

Example:

Let $R_T = 100\text{k}\Omega$.

$$R_x = \frac{100\text{k}\Omega}{12.9282\text{k}\Omega} = 7.735\text{k}\Omega \quad \rightarrow \quad R_1 = 12.9282R_x = 21.132\text{k}\Omega$$

Check-

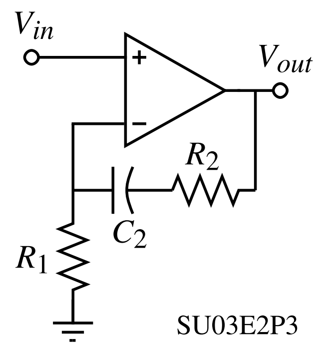
$$R_T = 2(21.132\text{k}\Omega) + \frac{21.132\text{k}\Omega^2}{7.735\text{k}\Omega} = 100\text{k}\Omega$$

Example 1 – Loop Filter

(a.) Find the transfer function of the filter shown assuming an ideal op amp.

(b.) Sketch a Bode plot for the magnitude of this filter if $R_1 = R_2 = 10\text{k}\Omega$ and $C_2 = 0.159\mu\text{F}$.

(c.) For the values in part (b.), find the single sideband spur at a reference frequency of 25 kHz if the op amp has an input offset current of I_{os} = 50nA and an input offset voltage of V_{io} = 100µV. Assume that the spurious deviation due to the offset voltage at 25 kHz can be expressed as $\theta_d = 100V_{pm}$, where V_{pm} is the phase modulation caused by the offset voltage of the filter.



SU03E2P3

Solution

(a.) The transfer function assuming an ideal op amp can be found as,

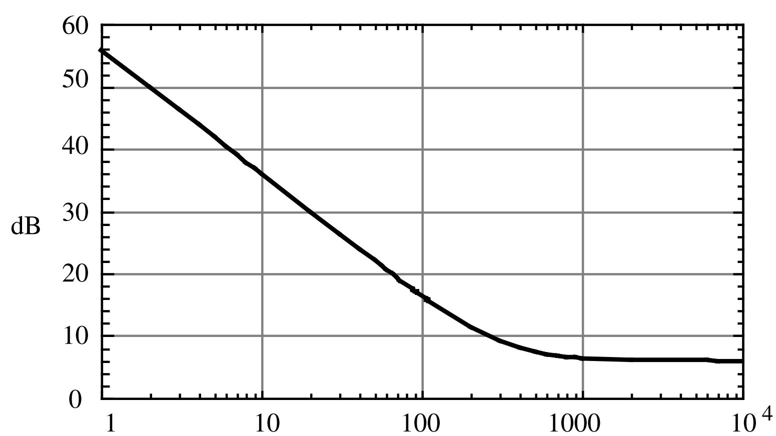
$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{Z_1+Z_2}{Z_1} = \frac{R_1 + R_2 + (1/sC_2)}{R_1} = \frac{s(R_1+R_2)C_2 + 1}{sC_2R_1}$$

(b.) If $R_1 = R_2 = 10\text{k}\Omega$ and $C_2 = 0.159\mu\text{F}$, then the filter transfer function becomes,

$$F(s) = \frac{s(R_1+R_2)C_2 + 1}{sC_2R_1} = \frac{s0.00318 + 1}{0.00159s} = \frac{\frac{s}{314.5} + 1}{\frac{s}{628.9}}$$

Example 1 - Continued

The sketch for the magnitude of this transfer function is below.



SU03E2S3

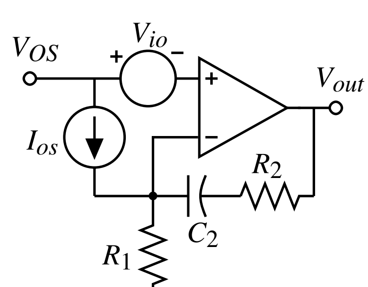
(c.) Find the offset voltage at the input of the filter, V_{OS}, from the figure shown.

$$V_{OS} = V_{io} + I_{os}R_1 = 100\mu\text{V} + 50\text{nA}\cdot 10\text{k}\Omega$$

$$V_{OS} = 0.1\text{mV} + 0.5\text{mV} = 0.6\text{mV} = 600\mu\text{V}$$

$$\therefore\ \theta_d = 100V_{pm} = 100(2\cdot V_{OS}) = 0.12$$

$$SSB = 20\log_{10}(\theta_d/2) = \underline{\underline{-24.44\ \text{dBc}}}$$



SU03E2S3B

Higher-Order Active Filters

1.) Cascading first-order filters (all poles are on the negative real axis)

Uses more op amps and dissipates more power.

2.) Extending the lag-lead filter.

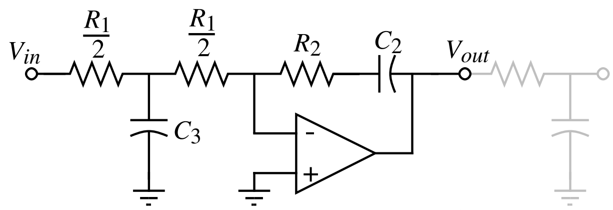


Fig. 120-02

From the previous slide we can write,

$$Z_1(s)(\text{eq.}) = R_1\left(\frac{sR_1C_3}{4}+1\right) \quad \text{and} \qquad Z_2(s) = \frac{sR_2C_2+1}{sC_2}$$

$$\therefore \quad \frac{V_{out}}{V_{in}} = -\frac{\dfrac{sR_2C_2+1}{sC_2}}{R_1\left(\dfrac{sR_1C_3}{4}+1\right)} = -\frac{sR_2C_2+1}{sC_2R_1\left(\dfrac{sR_1C_3}{4}+1\right)} = -\frac{s\tau_2+1}{s\tau_1(s\tau_3+1)}$$

where $\tau_1 = R_1C_2$, $\tau_2 = R_2C_2$, and $\tau_3 = 0.25R_1C_3$

The additional pole could also be implemented by a *RC* network at the output. However, now the output resistance is not small any more.

Non-Idealities of Active Filters

DC Offsets:

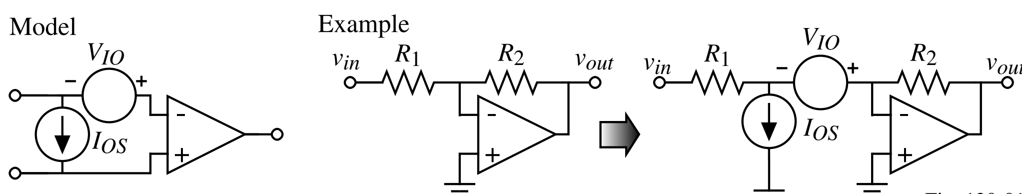


Fig. 120-01

What is the input and output offset voltages of this example?

Output offset voltage = $V_{OS}(\text{out}) = \left(\frac{R_2}{R_1}\right) V_{IO} + R_2I_{OS}$

Input offset voltage = $V_{OS}(\text{in}) = -V_{IO} + R_1I_{OS}$

Assume the op amp is a 741 with $V_{IO} = 3\text{mV}$, $I_{OS} = 100\text{nA}$, and $R_1 = R_2 = 10\text{k}\Omega$.

$\therefore \quad V_{OS}(\text{out}) = 3\text{mV} + 10\text{k}\Omega\cdot 100\text{nA} = 4\text{mV}$

$V_{OS}(\text{in}) = -3\text{mV} + 10\text{k}\Omega\cdot 100\text{nA} = -2\text{mV}$

We have seen previously that these input offset voltages can lead to large spurs in the PLL output.

Non-Idealities of Active Filters - Continued

Inverting and Noninverting Amplifiers:

Fig. 9.2-01

Gain and $GB = \infty$:

$$\frac{V_{out}}{V_{in}} = \frac{R_1+R_2}{R_1} \qquad\qquad \frac{V_{out}}{V_{in}} = -\frac{R_2}{R_1}$$

Gain $\neq \infty$, $GB = \infty$:

$$\frac{V_{out}(s)}{V_{in}(s)} = \left(\frac{R_1+R_2}{R_1}\right)\frac{\dfrac{A_{vd}(0)R_1}{R_1+R_2}}{1+\dfrac{A_{vd}(0)R_1}{R_1+R_2}} \qquad\qquad \frac{V_{out}(s)}{V_{in}(s)} = -\left(\frac{R_2}{R_1}\right)\frac{\dfrac{R_1A_{vd}(0)}{R_1+R_2}}{1+\dfrac{A_{vd}(0)R_1}{R_1+R_2}}$$

Gain $\neq \infty$, $GB \neq \infty$:

$$\frac{V_{out}(s)}{V_{in}(s)} = \left(\frac{R_1+R_2}{R_1}\right)\frac{\dfrac{GB\cdot R_1}{R_1+R_2}}{s+\dfrac{GB\cdot R_1}{R_1+R_2}} = \left(\frac{R_1+R_2}{R_1}\right)\frac{\omega_H}{s+\omega_H} \qquad \frac{V_{out}(s)}{V_{in}(s)} = \left(-\frac{R_2}{R_1}\right)\frac{\dfrac{GB\cdot R_1}{R_1+R_2}}{s+\dfrac{GB\cdot R_1}{R_1+R_2}} = \left(-\frac{R_2}{R_1}\right)\frac{\omega_H}{s+\omega_H}$$

Non-Idealities of Active Filters - Continued

Example:

Assume that the noninverting and inverting voltage amplifiers have been designed for a voltage gain of +10 and -10. If $A_{vd}(0)$ is 1000, find the actual voltage gains for each amplifier.

Solution

For the noninverting amplifier, the ratio of R_2/R_1 is 9.

$$A_{vd}(0)R_1/(R_1+R_2) = \frac{1000}{1+9} = 100.$$

$$\therefore \quad \frac{V_{out}}{V_{in}} = 10\left(\frac{100}{101}\right) = 9.901 \text{ rather than } 10.$$

For the inverting amplifier, the ratio of R_2/R_1 is 10.

$$\frac{A_{vd}(0)R_1}{R_1+R_2} = \frac{1000}{1+10} = 90.909$$

$$\therefore \quad \frac{V_{out}}{V_{in}} = -(10)\left(\frac{90.909}{1+90.909}\right) = -\,9.891 \text{ rather than } -10.$$

Non-Idealities of Active Filters - Continued

Finite Gainbandwidth:

Assume that the noninverting and inverting voltage amplifiers have been designed for a voltage gain of +1 and -1. If the unity-gainbandwidth, *GB*, of the op amps are 2πMrads/sec, find the upper -3*dB* frequency for each amplifier.

Solution

In both cases, the upper -3*dB* frequency is given by

$$\omega_H = \frac{GB \cdot R_1}{R_1 + R_2}$$

For the noninverting amplifier with an ideal gain of +1, the value of R_2/R_1 is zero.

$$\therefore \quad \omega_H = GB = 2\pi \text{ Mrads/sec (1MHz)}$$

For the inverting amplifier with an ideal gain of -1, the value of R_2/R_1 is one.

$$\therefore \quad \omega_H = \frac{GB \cdot 1}{1+1} = \frac{GB}{2} = \pi \text{ Mrads/sec (500kHz)}$$

Non-Idealities of Active Filters - Continued

Integrators – Finite Gain and Gainbandwidth:

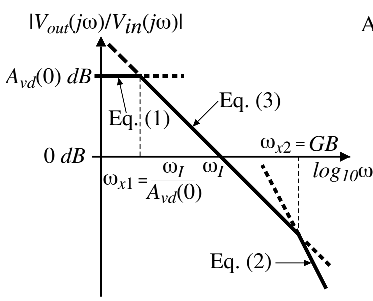
$$\frac{V_{out}}{V_{in}} = -\left(\frac{1}{sR_1C_2}\right) \frac{\dfrac{A_{vd}(s)\, sR_1C_2}{sR_1C_2 + 1}}{1 + \dfrac{A_{vd}(s)\, sR_1C_2}{sR_1C_2 + 1}} = \left(-\frac{\omega_I}{s}\right) \frac{\dfrac{A_{vd}(s)\,(s/\omega_I)}{(s/\omega_I) + 1}}{1 + \dfrac{A_{vd}(s)\,(s/\omega_I)}{(s/\omega_I) + 1}}$$

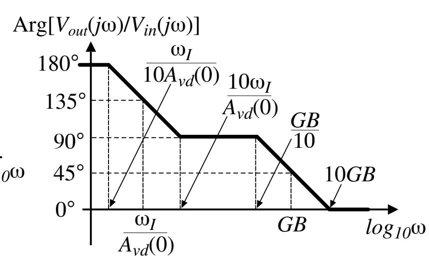
where $$A_{vd}(s) = \frac{A_{vd}(0)\omega_a}{s + \omega_a} = \frac{GB}{s + \omega_a} \approx \frac{GB}{s}$$

Case 1: $s \to 0 \;\Rightarrow\; A_{vd}(s) = A_{vd}(0) \;\Rightarrow\; \dfrac{V_{out}}{V_{in}} \approx -A_{vd}(0)$

Case 2: $s \to \infty \;\Rightarrow\; A_{vd}(s) = \dfrac{GB}{s} \;\Rightarrow\; \dfrac{V_{out}}{V_{in}} \approx -\left(\dfrac{GB}{s}\right)\left(\dfrac{\omega_I}{s}\right)$

Case 3: $0 < s < \infty \;\Rightarrow\; A_{vd}(s) = \infty \;\Rightarrow\; \dfrac{V_{out}}{V_{in}} \approx -\dfrac{\omega_I}{s}$





CHARGE PUMPS

The use of the PFD permits the use of a charge pump in place of the conventional PD and low pass filter. The advantages of the PFD and charge pump include:

- The capture range is only limited by the VCO output frequency range
- The static phase error is zero if the mismatches and offsets are negligible.

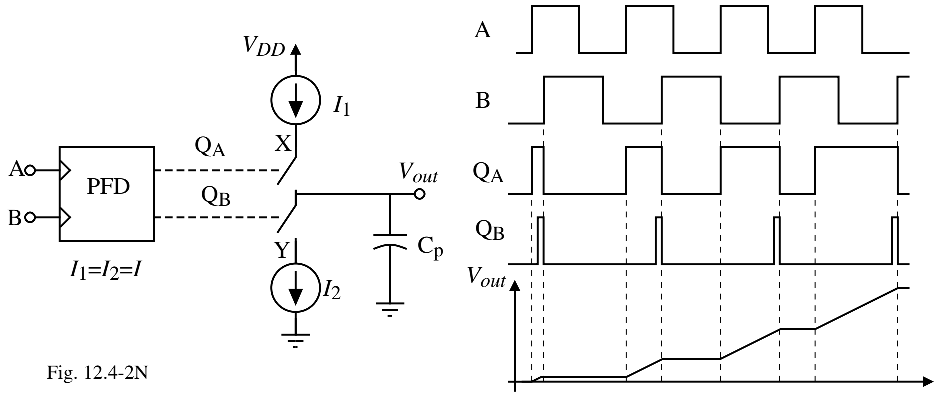


Fig. 12.4-2N

Q_A high deposits charge on C_p (A leads B).
Q_B high removes charge from C_p (B leads A).
Q_A and Q_B low V_{out} remains constant.
We have seen that a resistor in series with C_p is necessary for stability.

(QB is high for a short time due to reset delay but the difference between average values between QA and QB still accurately represents the input phase or frequency difference.)

Types of Charge Pumps

- Conventional Tri-Stage
  - Low power consumption, moderate speed, moderate clock skew
  - Low power frequency synthesizers, digital clock generators
- Current Steering
  - Static current consumption, high speed, moderate clock skew
  - High speed PLL (>100MHz), translation loop, digital clock generators
- Differential input with Single-Ended output
  - Medium power, moderate speed, low clock skew
  - Low-skew digital clock generators, frequency synthesizers
- Fully Differential
  - Static current consumption, high speed (>100MHz)
  - Digital clock generators, translation loop, frequency synthesizer (with on-chip filter)
- Advantages of charge pumps
  - Consume less power than active filters
  - Have less noise than active filters
  - Do not have the offset voltage of op amps
  - Provide a pole at the origin
  - More compatible with the objective of putting the filter on chip

Nonidealities in Charge Pumps[†]

Leakage current:

Small currents that flow when the switch is off.

Mismatches in the Charge Pump:

The up and down (charge and discharge) currents are unequal.

Timing Mismatch in PFD:

Any mismatch in the time at which the PFD provides the up and down outputs.

Charge Sharing:

The presence of parasitic capacitors will cause the charge on the desired capacitor to be shared with the parasitic capacitors.

† Woogeun Rhee, "Design of High-Performance CMOS Charge Pumps in Phase-Locked Loops," *Proc. of 1999 ISCAS*, Page II-545-II548, May 1999.

Charge Pumps

The low pass filter in the PLL can be implemented by:

1.) Active filters which require an op amp

2.) Passive filters and a charge pump.

The advantages of a charge pump are:

- Reduced noise
- Reduced power consumption
- No offset voltage

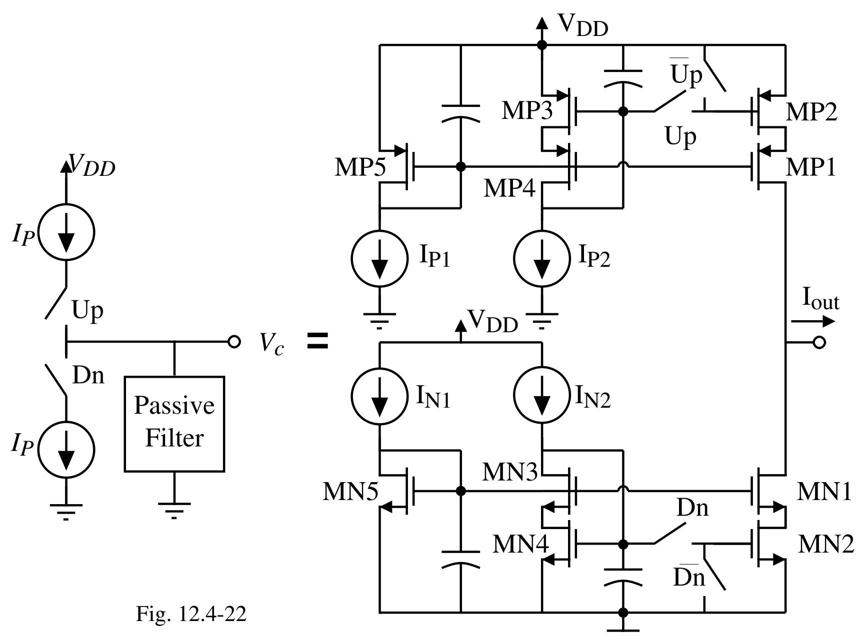


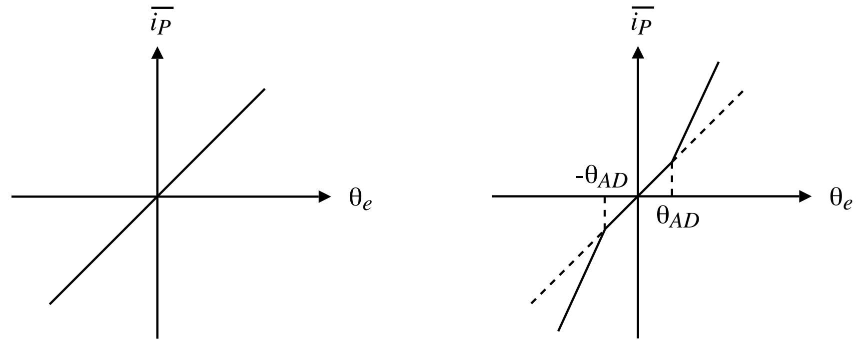
Fig. 12.4-22

Discriminator-Aided PFD/Charge Pump†

This circuit reduces the pull-in time, T_P, and enhances the switching speed of the PLL while maintaining the same noise bandwidth and avoiding modulation damping.

Technique:

Increase the gain of the phase detector for increasing values of phase error.



Characteristic of a Conventional PD   Characteristic of a Nonlinear PD

Fig. 3.1-32

The gain of the phase detector is increased when θ_e becomes larger than θ_{AD} or smaller than $-\theta_{AD}$. During the time the phase detector gain has increased by k, the loop filter bandwidth is also increased by k.

† C-Y Yang and S-I Liu, "Fast-Switching Frequency Synthesizer with a Discriminator-Aided Phase Detector," *IEEE J. of Solid-State Circuits*, Vol. 35, No. 10, Oct. 2000, pp. 1445-1452.

Discriminator-Aided Phase Detector (DAPD) – Continued

Schematic of a phase detector with DAPD and charge-pump filter:

If the absolute value of the delay between V_i and V_{osc} is greater than τ_{AD}, the output signal of the DAPD is high and increases the charge pump current by k^2 and adjusts the loop filter bandwidth.

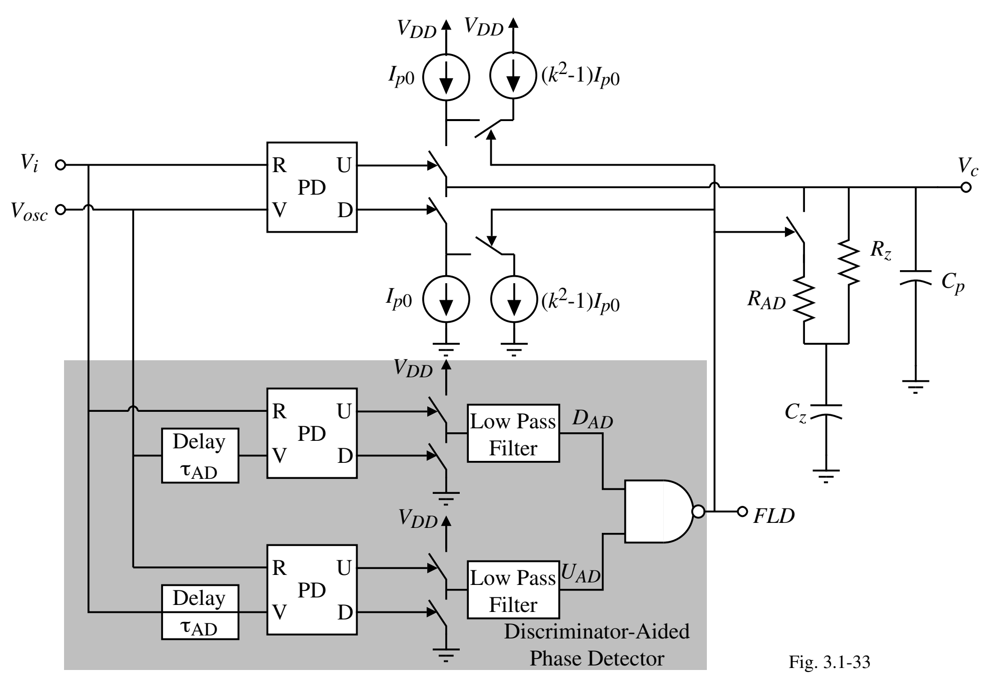


Fig. 3.1-33

0.35µm CMOS: Switching time for a 448 MHz to 462 MHz step is reduced from 90µs to 15µs ($k = 3$).

A Type-I Charge Pump†

This PLL uses an on-chip, passive discrete-time loop filter with a single state, charge-pump to implement the loop filter. The stabilization zero is created in the discrete-time domain rather than using RC time constants.

Block diagram of the Type-I, charge pump PLL frequency synthesizer:

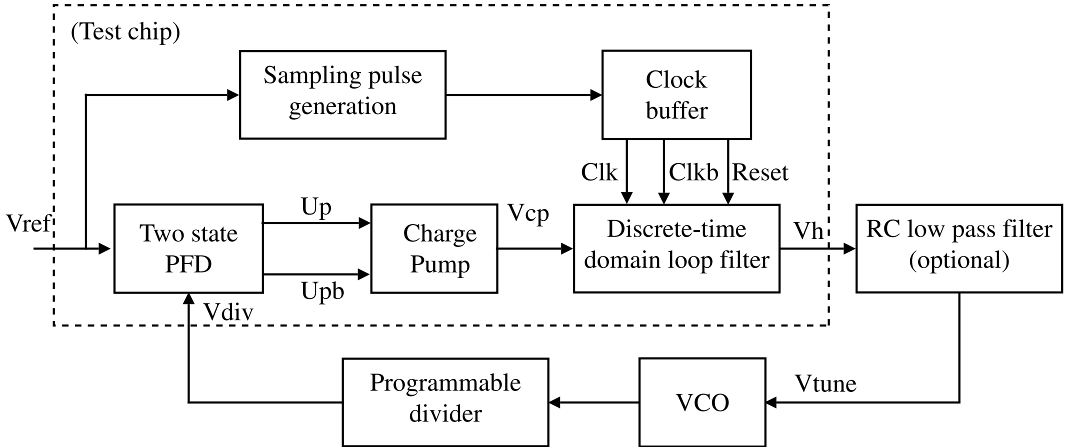


Fig. 120-03

† B. Zhang, P.E. Allen and J.M. Huard, "A Fast Switching PLL Frequency Synthesizer With an On-Chip Passive Discrete-Time Loop Filter in 0.25μm CMOS," *IEEE J. of Solid-State Circuits*, vol. 38, no. 6, June 2003, pp. 855-865.

Type-I Charge Pump – Continued

Comparison of a conventional 3-state PFD and a 2-state PFD:

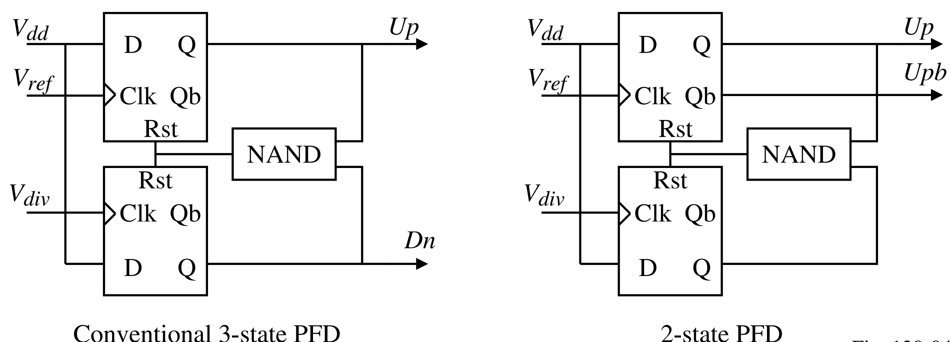


Fig. 120-04

Dual polarity and single polarity charge pumps:

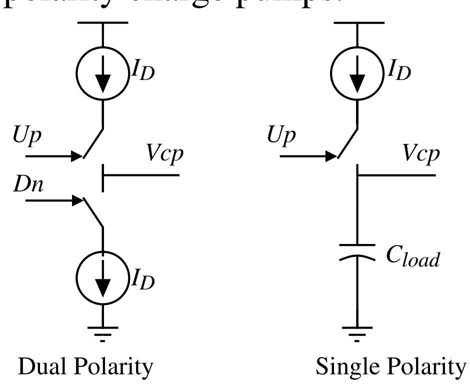


Fig. 120-05

Single Polarity Charge Pump

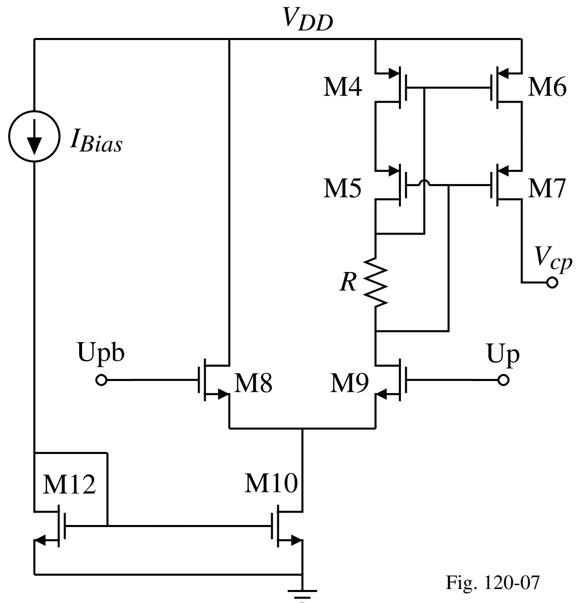


Fig. 120-07

No matching problems.

Type-I Charge Pump – Continued

The discrete-time loop filter:

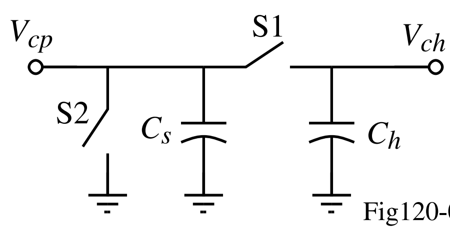


Fig120-06

$$F_1(s) \approx (1\text{-}z^{-1})\frac{k_{lf}f_1(s)}{s}$$

where $z = e^{sT_s}$, T_s is the sampling period ($S1$), k_{lf} is a gain constant, and $f_1(s)$ accounts for the loading effect of the low pass filter.

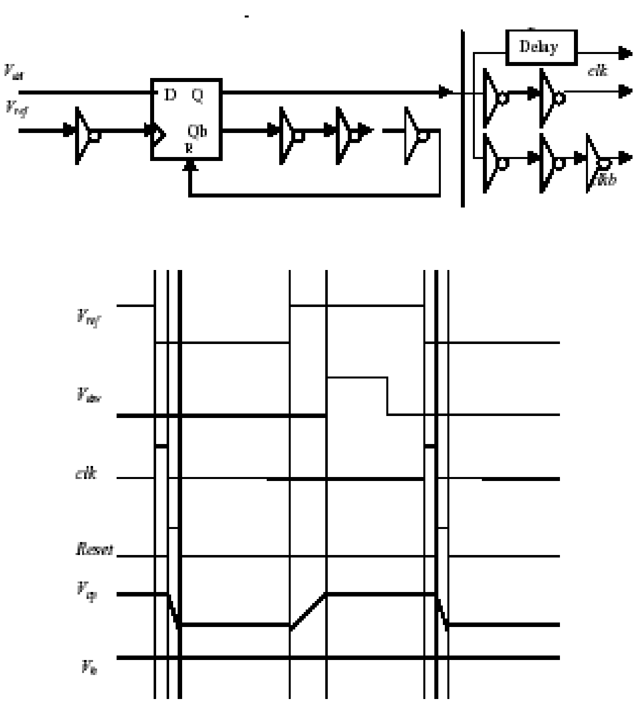
The open-loop transfer function of this system is given as,

$$T(s) = (1\text{-}z^{-1})\frac{K_dK_ok_{lf}f_1(s)}{s^2N} \quad\rightarrow\quad T(s) = (sT_s)\frac{K_dK_ok_{lf}f_1(s)}{s^2N} = \frac{T_sK_dK_ok_{lf}f_1(s)}{sN}$$

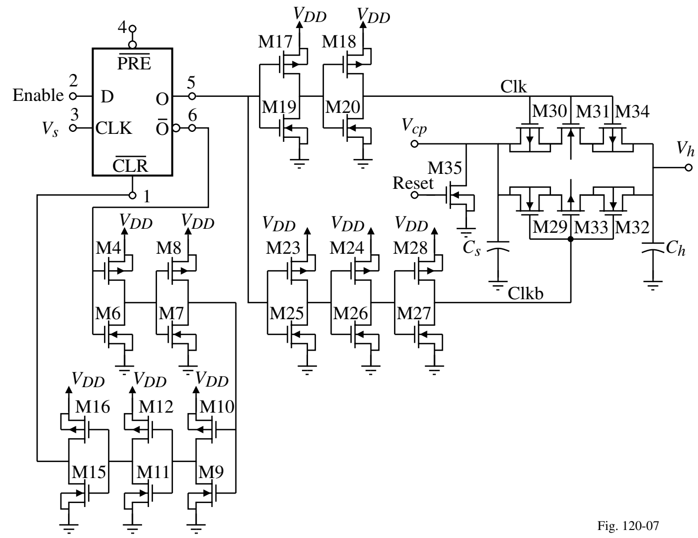
which is a Type I system if $\omega << 2\pi/T_s$.

Type-I Charge Pump – Continued

Clock generator and clock waveforms:

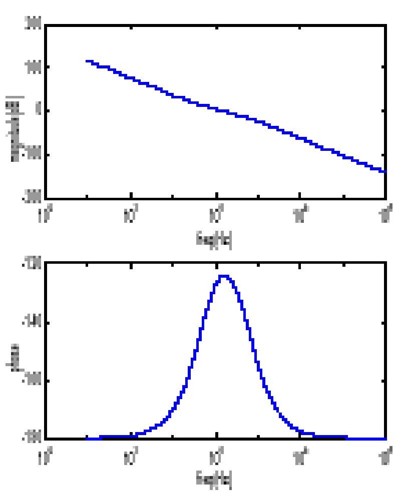


Discrete-time loop filter:

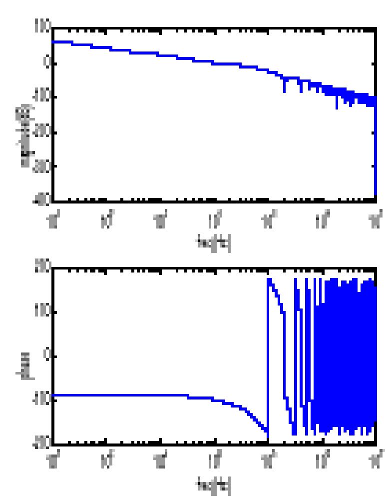


Type-I Charge Pump – Continued

Comparison of the frequency response of the conventional and single state architectures:



Conventional architecture



Single-state architecture

Results:

	Conventional Architecture	Type-I Architecture
Reference spur	-53dBc	-62dBc
Switching time	140µs	30µs
Loop filter size	Off-chip filter	Integrated (70pF)

Use of Active Filters with Charge Pumps

Second-Order PLL:

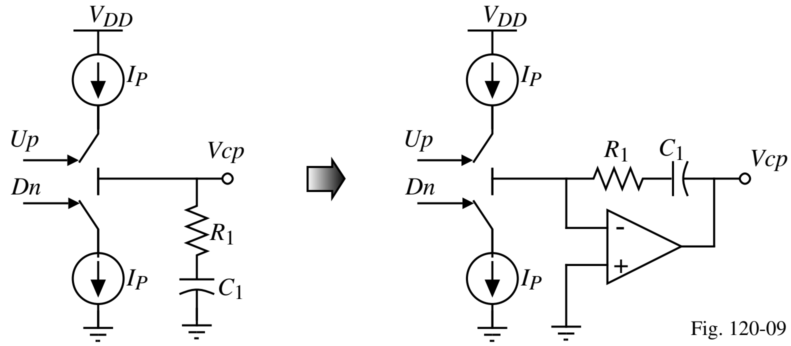


Fig. 120-09

PLL Crossover Frequency:

$$\omega_{c2} = \sqrt{\frac{K^2\tau^2 + \sqrt{K^4\tau^4 + 4\,K^4}}{2}} \qquad \text{where } K = \frac{K_v}{NC_1}$$

PLL Settling Time for a Frequency step of $\Delta\omega$:

$$t_{s2} \approx \frac{2}{\omega_{c2}} \sqrt{\frac{1+\sqrt{1+\frac{4}{K^4\tau^4}}}{2}}\; ln\left(\frac{\Delta\omega}{\alpha N\sqrt{1-\left(\frac{\tau\sqrt{K}}{2}\right)^2}}\right) \qquad \text{where } \alpha = \frac{\theta(t_{s2})}{\theta(\infty)}$$

Charge Pump with a Third-Order Filter

The additional pole of a third-order PLL provides more spurious suppression. However, the phase lag associated with the pole introduces a stability issue.

Circuit:

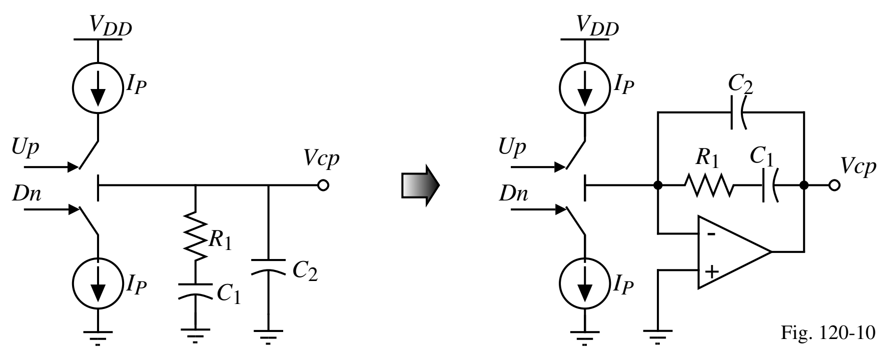


Fig. 120-10

The impedance of the loop filter is,

$$Z(s) = \left(\frac{b}{b+1}\right)\frac{s\tau+1}{s^2C_1\left(\frac{s\tau}{b+1}+1\right)} \text{ where } \tau = R_1C_1 \quad \text{and} \quad b = \frac{C_1}{C_2}$$

The loop gain for this PLL is

$$LG(s) = -\frac{K_oI_P}{2\pi N}\left(\frac{b}{b+1}\right)\frac{s\tau+1}{s^2C_1\left(\frac{s\tau}{b+1}+1\right)}$$

The phase margin of the loop is,

$$\text{PM} = tan^{-1}(\tau\omega_{c3}) - tan^{-1}\left(\frac{\tau\omega_{c3}}{b+1}\right) \qquad \text{where } \omega_{c3} \text{ is the crossover frequency}$$

Charge Pump with a Third-Order Filter – Continued

Differentiating with respect to ω_{c3}, shows that max. phase margin occurs when

$$\omega_{c3} = \sqrt{b+1}\,/\tau$$

$$\therefore\ \text{PM(max)} = \tan^{-1}(\sqrt{b+1}\,) - \tan^{-1}\left(\frac{1}{\sqrt{b+1}}\right)$$

Maximum phase margin as a function of $b = C_1/C_2$.

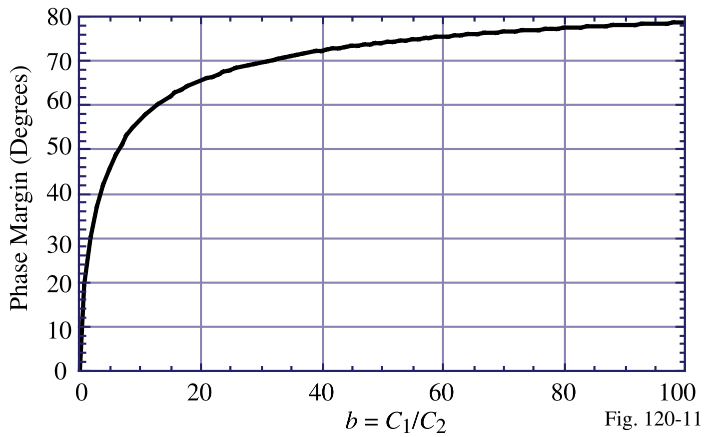


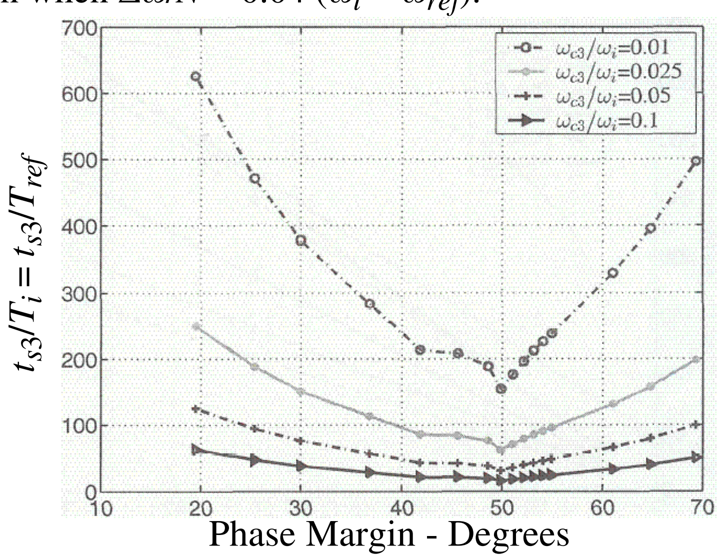
Fig. 120-11

Note that for $b \leq 1$, the phase margin is less than 20°.

Charge Pump with a Third-Order Filter – Continued

An analytical expression for settling time is difficult to calculate for the third-order filter.

The following figure shows the simulated settling time to 10ppm accuracy as a function of phase margin when $\Delta\omega/N = 0.04$ ($\omega_i = \omega_{ref}$).



For $\Delta\omega/N < 0.04$ and 20°<PM<79°, we may estimate the settling time to 10ppm accuracy as

$$t_{s3} \approx \frac{2\pi}{\omega_{c3}}\,[0.0067\cdot\text{PM}^2 - 0.6303\cdot\text{PM} + 16.78]$$

Charge Pump with a Third-Order Filter – Continued

A loop filter design recipe:

1.) Find K_v for the VCO.

2.) Choose a desired PM and find b from the max. PM equation.

3.) Choose the crossover frequency, ω_{c3}, and find τ from $\omega_{c3} = \sqrt{b+1}\,/\tau$.

4.) Select C_1 and I_P such that they satisfy

$$\frac{I_P K_v}{2\pi N}\left(\frac{b}{b+1}\right) = \frac{C_1}{\tau^2}\sqrt{b+1}$$

5.) Calculate the noise contribution of $R_1{}^2$. If the calculated noise is negligible the design is complete. If not, then go back to step 4.) and increase C_1.

Example: Let $K_v = 10^7$ rads/sec., $N = 1000$, PM = 50° and f_{c3} = 10kHz.

Now, $$50° = tan^{-1}(\sqrt{b+1}\,) - tan^{-1}\left(\frac{1}{\sqrt{b+1}}\right) \quad \rightarrow \quad b \approx 6.65 \text{ (by iteration)}$$

$$\tau = \frac{\sqrt{b+1}}{2\pi\cdot f_{c3}} = \frac{\sqrt{6.65+1}}{2\pi\cdot 1000} = 0.44 \text{ msec}$$

If I_P = 200µA, then $$C_1 = \frac{I_P K_v}{2\pi N}\left(\frac{b}{b+1}\right)\frac{\tau^2}{\sqrt{b+1}} = 19.34 \text{ nF} \rightarrow \quad R_1 = \frac{\tau}{C_1} = 22.72\text{k}\Omega$$

$$\text{Noise} = 4kTR = 4(1.38\text{x}10^{-23})(300)(22.72\text{k}\Omega) = 3.76\text{x}10^{-16}\ \text{V}^2/\text{Hz}$$

Charge Pump with a Fourth-Order Filter

To further reduce the spurs with out decreasing the crossover frequency and thereby increasing the settling time, an additional pole needs to be added to the loop.

Circuit:

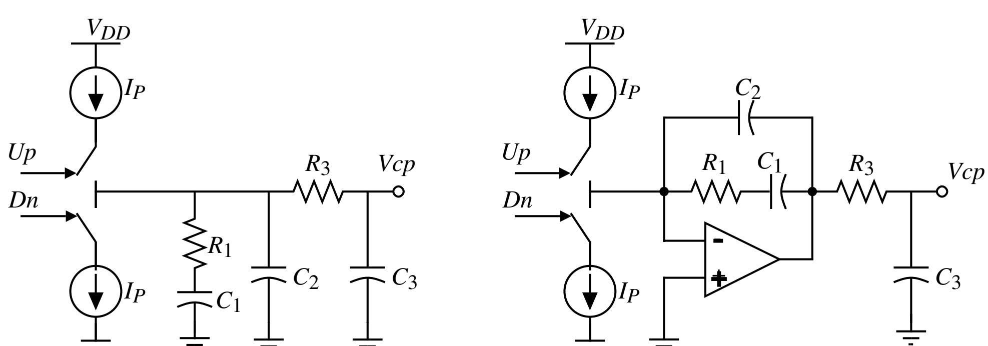


Fig. 120-12

The impedance of the passive filter is given as,

$$Z(s) = \frac{s\tau + 1}{sC_1\left(1+\frac{C_2}{C_1}+\frac{C_3}{C_1}\right)[B(s\tau)^2 + As\tau + 1]}$$

where

$$A = \frac{1+b\frac{\tau_2}{\tau}\left(1+\frac{C_2}{C_1}\right)}{1+b}, \quad B = \frac{b}{1+b}\frac{\tau_2 C_2}{\tau C_1}, \quad \tau = R_1C_1, \quad \tau_3 = R_3C_3 \quad \text{and} \quad b = \frac{C_1}{C_2+C_3}$$

Charge Pump with a Fourth-Order Filter – Continued

Phase margin:

$$PM = tan^{-1}(\tau\omega_{c4}) - tan^{-1}\left(\frac{A(\tau\omega_{c4})}{1-B(\tau\omega_{c4})^2}\right) \quad \text{where } \omega_{c4} = \text{crossover frequency}$$

The maximum phase margin is obtained when the derivative of the above equation with respect to ω_{c4} is set to zero. The results are:

$$\omega_{c4} = \frac{1}{\tau}\sqrt{\frac{1}{2}\left(\frac{2B+AB+A-A^2}{B(B-A)}\right) + \sqrt{\left(\frac{2B+AB+A-A^2}{B(B-A)}\right)^2 - \frac{4(1-A)}{B(B-A)}}}$$

For ω_{c4} to be the crossover frequency, it must satisfy the following equation,

$$\frac{I_P K_v}{2\pi N}\sqrt{\frac{1+(\tau\omega_{c4})^2}{(A\tau\omega_{c4})^2+[1-B(\tau\omega_{c4})^2]^2}} = C_1\left(\frac{1+b}{b}\right)\omega_{c4}^2$$

Practical simplifications:

A positive phase margin ⇒ Zero lower than the two high frequency poles ⇒ $\frac{C_2}{C_1} < 1$

For the fourth pole not to decrease the phase margin it has to be more than a decade away from the zero, therefore, $b\frac{\tau_2}{\tau} << 1$.

With these conditions we find that $B << A$.

Charge Pump with a Fourth-Order Filter – Continued

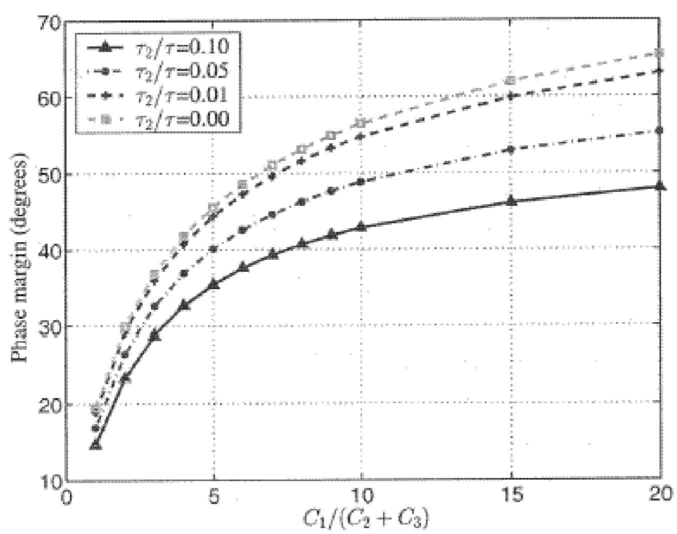
If $B << A$, then the previous relationships become,

$$A \approx \frac{1}{1+b}, \quad \omega_{c4} \approx \frac{1}{\tau\sqrt{A}} \approx \frac{\sqrt{1+b}}{\tau} \quad \text{and} \quad \frac{I_P K_v}{2\pi N}\left(\frac{b}{1+b}\right) \approx \frac{C_1}{\tau^2}\sqrt{1+b}$$

The maximum phase margin also simplifies to,

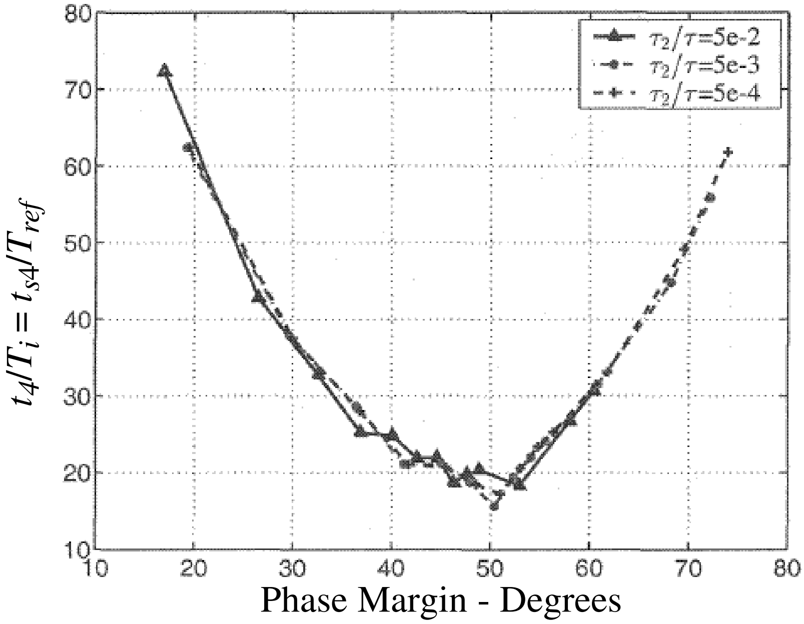
$$\text{PM(max)} \approx tan^{-1}(\sqrt{1+b}) - tan^{-1}\left(\frac{1}{\sqrt{1+b}}\right)$$

Exact phase margin:



Charge Pump with a Fourth-Order Filter – Continued

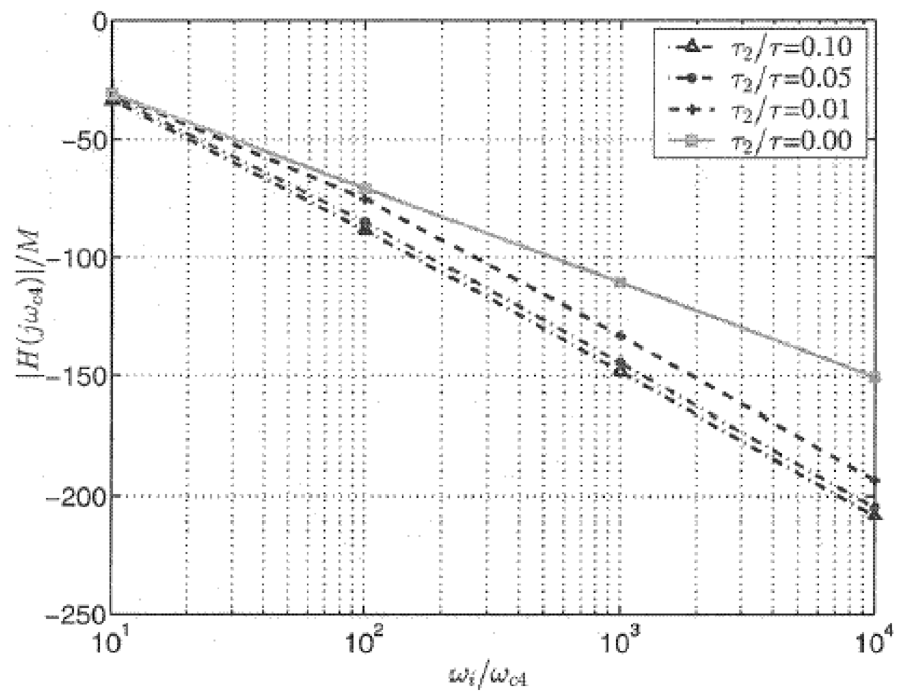
Simulation is used to estimate the settling time of the fourth-order loop to 10 ppm accuracy when $\Delta\omega/N < 0.04$:



Note that the settling time at a given phase margin is independent of τ_2/τ and is the same as that of a third-order loop.

Charge Pump with a Fourth-Order Filter – Continued

Spur suppression of the fourth-order filter.



Charge Pump with a Fourth-Order Filter – Continued

Loop filter design procedure:

1.) Find K_v for the VCO.

2.) Choose a desired phase margin and find b. (If PM = 50°, then b = 6.5)

3.) Choose the crossover frequency ω_{c4} and find τ. ($\tau \approx 2.7/\omega_{c4}$ if b = 6.5)

4.) Choose the desired spur attenuation and find τ_2/τ from the previous page.

5.) Select C_1 and I_P such that they satisfy $\frac{I_P K_v}{2\pi N}\left(\frac{b}{1+b}\right) \approx \frac{C_1}{\tau^2}\sqrt{1+b}$.

6.) Calculate the noise contribution of R_1 and R_3.

Example: Let $K_v = 10^7$ rads/sec., N = 1000, PM = 50°, f_{c4} = 1kHz and f_{ref} = 100kHz.

Since PM = 50°, b = 6.5

$\tau \approx 2.7/\omega_{c4} = 2.7/(2\pi\cdot 1000) = 430\mu\text{sec}$.

Let us choose τ_2/τ as 0.1 which corresponds to about –90dB of suppression.

If $I_P = 200\mu\text{A}$, then $C_1 = \frac{I_P K_v}{2\pi N}\left(\frac{b}{b+1}\right)\frac{\tau^2}{\sqrt{b+1}} = 18.63\text{ nF} \rightarrow \quad R_1 = \frac{\tau}{C_1} = 23.09\text{k}\Omega$

$\tau_2 = 0.1\tau = 43\mu\text{sec}$

If C_3 = 1nF, then $R_3 = \tau_2/C_3 = 43\mu\text{sec}/1\text{nF} = 43\text{k}\Omega$

Noise: $v_{R1}^2 = 4kTR_1 = 3.823 \times 10^{-16}\ \text{V}^2/\text{Hz}$ and $v_{R3}^2 = 4kTR_3 = 7.12 \times 10^{-16}\ \text{V}^2/\text{Hz}$

Charge Pump with a Fourth-Order Filter – Continued

Open loop transfer function for a typical fourth-order PLL:

PSPICE File:

```
Fourth-order, charge-pump PLL loop gain
.PARAM N=1000, KVCO=1E7, T=0.43E-3, T2=43E-6, KD=1, E=10
.PARAM A=0.2287 B=0.00868
*VCO Noise Transfer Function
VIN 1 0 AC 1.0
RIN 1 0 10K
EDPLL1 2 0 LAPLACE {V(1)}=
+{-KD*KVCO*46.52E6*(S*T+1)/(S+E)/(S+E)/(B*T*T*S*S+A*T*S+1)}
RDPLL1 2 0 10K
*Steady state AC analysis
.AC DEC 20 10 100MEG
.PRINT AC VDB(2) VP(2)
.PROBE
.END
```

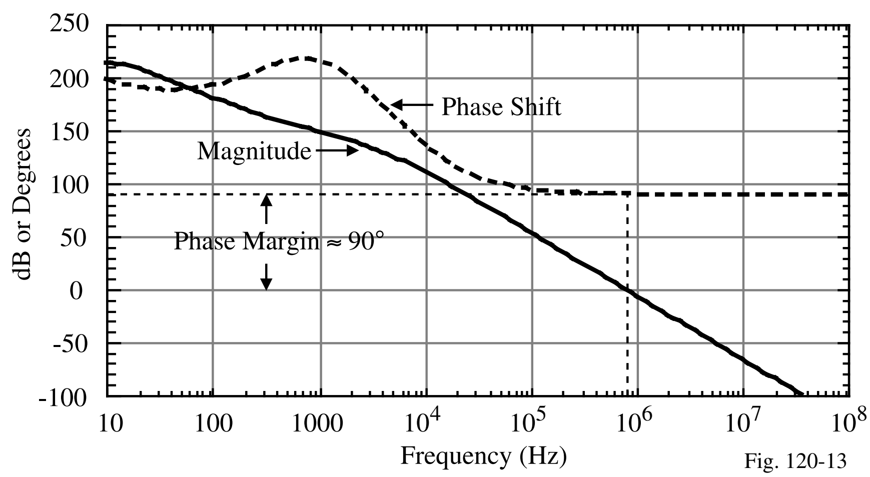


Fig. 120-13

SUMMARY

Filters

• Determines the dynamic performance of the PLL
• Active and passive filters
• Order of the filter – higher the order, the more noise and spur suppression
• Nonidealities of active filters
    - DC offsets
    - Finite op amp gain
    - Finite gain-bandwidth
    - Noise

Charge Pumps

• Avoid the use of the op amp to achieve a pole at the origin (Type-II systems)
• Nonidealities in charge pumps
    - Leakage current
    - Mismatches in the up and down currents
    - Timing mismatches
  - Charge sharing

