LECTURE 010 –CMOS PHASE LOCKED LOOPS
INTRODUCTION

Course Objective

Understand the principles and applications of phase locked loops using integrated circuit technology with emphasis on CMOS technology.

Organization:

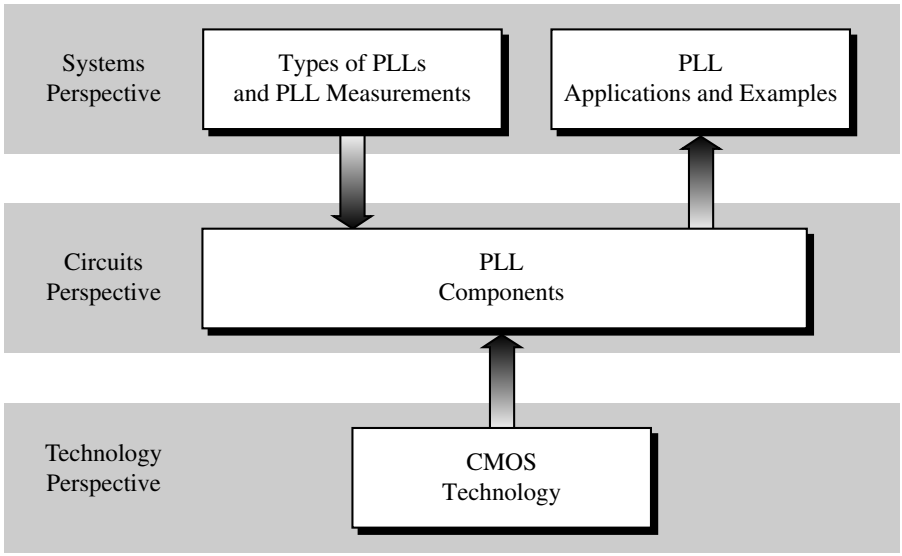

Fig.030901-03

Pertinent References

Phase Locked Loops:

1. F.M Gardner, *Phaselock Techniques*, 2nd ed., John-Wiley & Sons, Inc., NY, 1979.
2. B. Razavi (ed.), *Monolithic Phase-Locked Loops and Clock Recovery Circuits*, IEEE Press, 1997.
3. R.E. Best, *Phase-Locked Loops: Design, Simulation, and Applications*, 4th edition, McGraw-Hill, 1999 (4th edition?)
4. A. Hajimiri and T.H. Lee, *The Design of Low Noise Oscillators*, Kluwer Academic Publishers, 1999.
5. B. Razavi, *Design of Integrated Circuits for Optical Communications*, McGraw-Hill, 2003.
6. T.H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press, NY, 1998.
7. Recent publications of the *IEEE Journal of Solid-State Circuits*.

CMOS Analog Design:

1. Paul Gray, Paul Hurst, Steve Lewis and Robert Meyer, *Analysis and Design of Analog Integrated Circuits – Fourth Edition*, John Wiley and Sons, Inc., 2001
2. P.E. Allen and D.R. Holberg, *CMOS Analog Circuit Design – Second Edition*, Oxford University Press, 2002.
3. B. Razavi, *Design of Integrated Circuits for Optical Communications*, McGraw-Hill, 2003.

OPERATING PRINCIPLES OF PLLs

What is a PLL?

A PLL contains three basic components as shown below:

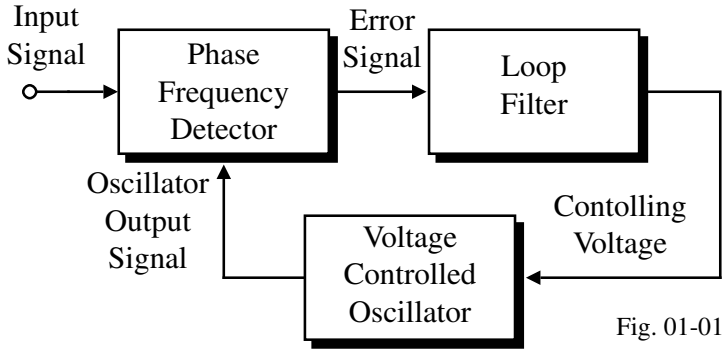

Fig. 01-01

- Phase/frequency detector determines the difference between the phase or frequency of two signals
- The loop filter removes the high-frequencies from the voltage-controlled oscillator (VCO) controlling voltage
- The VCO produces and output frequency controlled by a voltage

More Detailed PLL Block Diagram

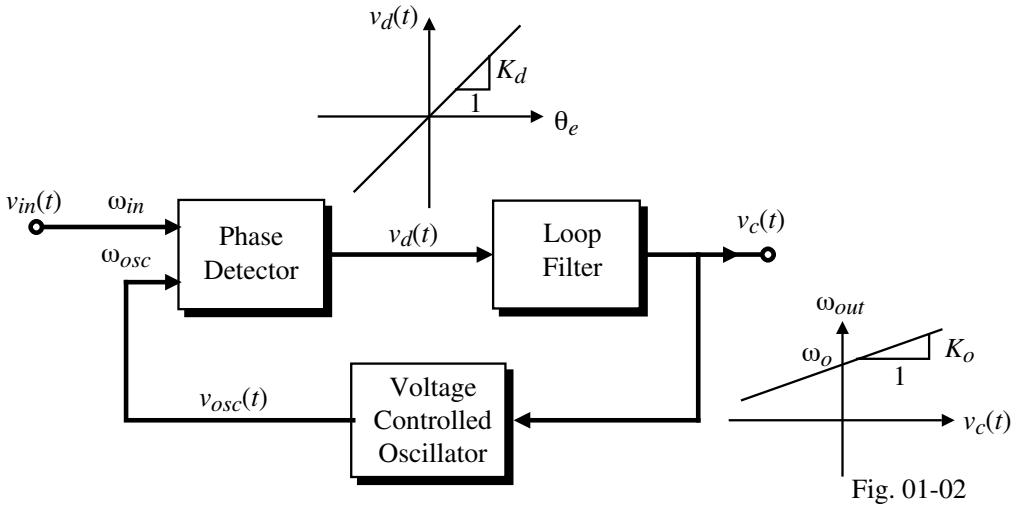

Fig. 01-02

$v_{in}(t)$ – The input or reference signal
ω_{in} – The radian frequency of the input signal
$v_{osc}(t)$ – The output of the VCO
ω_{osc} – The radian frequency of the VCO
$v_d(t)$ – The detector output voltage = $K_d\theta_e$
θ_e – Phase error between $v_{in}(t)$ and $v_{out}(t)$ = θ_{in} - θ_{osc}
$v_c(t)$ – The output voltage of the loop filter and the control voltage for the VCO

The Phase Detector and VCO in more Detail

Phase Detector:

$$v_d(t) = K_d\theta_e = K_d(\theta_{in} - \theta_{osc})$$

where K_d is the gain of the phase detector.

The units of K_d are volts/radians or simply volts assuming all phase shifts are in radians and not degrees.

Voltage Controlled Oscillator:

$$\omega_{osc} = \omega_o + K_o\, v_c(t)$$

where K_o is the VCO gain and ω_o is the free-running radian frequency.

The units of K_o are rads/sec·V or simply $(\text{sec}\cdot\text{V})^{-1}$ assuming all phase shifts are in radians and not degrees.

PLL Operation

Locked Operation:

- The loop is *locked* when the frequency of the VCO is exactly equal to the average frequency of the input signal.
- If the input signal has noise, the phase locked loop will remove much of the noise on the input signal.
- To maintain the control voltage needed for locked conditions, it is generally necessary for the output of the phase/frequency detector to be nonzero.

Unlocked Operation:

- The VCO runs at a frequency called the *free running frequency*, ω_o, which corresponds to no control voltage.
- The capture process is the means by which the loop goes from unlocked, free-running state to that of the locked state.

Transient Response of the PLL

Assume the input frequency is increased by an amount $\Delta\omega$.

1.) ω_{in} increases by $\Delta\omega$ at t_o.

2.) The input signal leads the VCO and v_d begins to increase.

3.) After a delay due to the loop filter, the VCO increases ω_{osc}.

4.) As ω_{osc} increases, the phase error reduces.

5.) Depending on the loop filter, the final phase error will be reduced to zero or to a finite value.

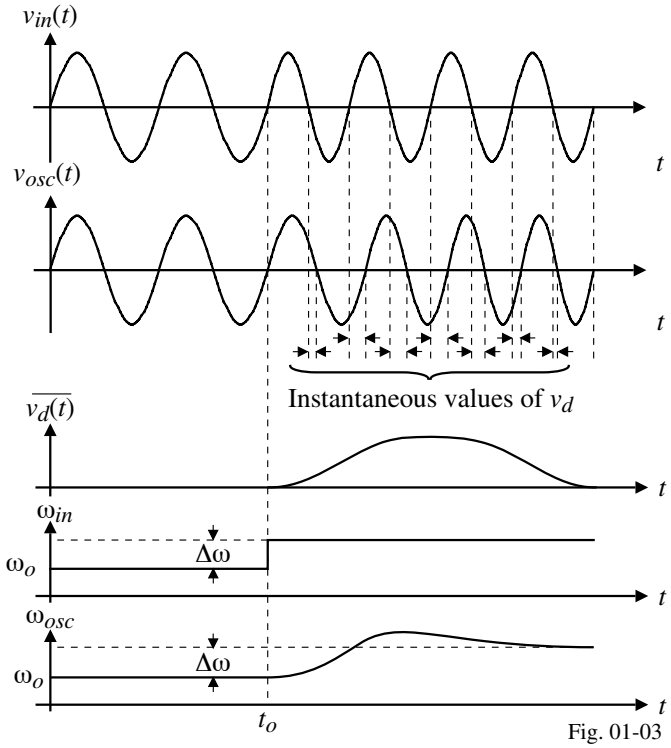

Fig. 01-03

CLASSIFICATION OF PLL TYPES

Types of PLLs

PLL Type	Phase Detector	Loop Filter	Controlled Oscillator
Linear PLL (LPLL)	Analog multiplier	RC passive or active	Voltage
Digital PLL (DPLL)	Digital detector	RC passive or active	Voltage
All digital PLL (ADPLL)	Digital detector	Digital filter	Digitally controlled
Software PLL (SPLL)	Software multiplier	Software filter	Software oscillator

The digital PLL (DPLL) has been the mainstay of most PLLs and is called the “classical” digital PLL.

The Linear PLL (LPLL)

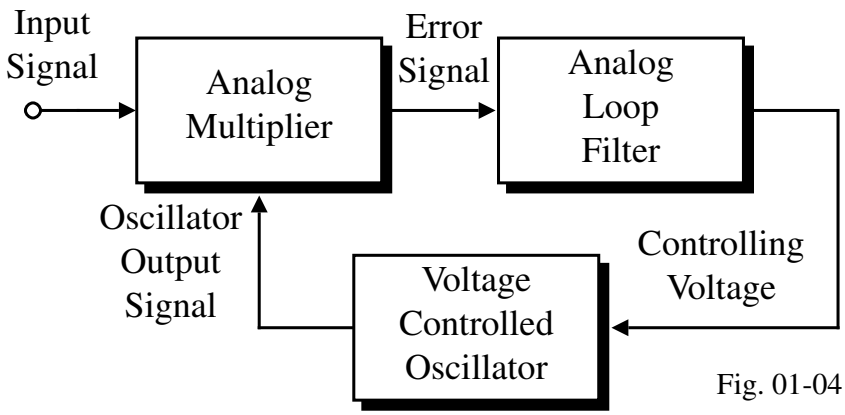

Fig. 01-04

The Digital PLL (DPLL)

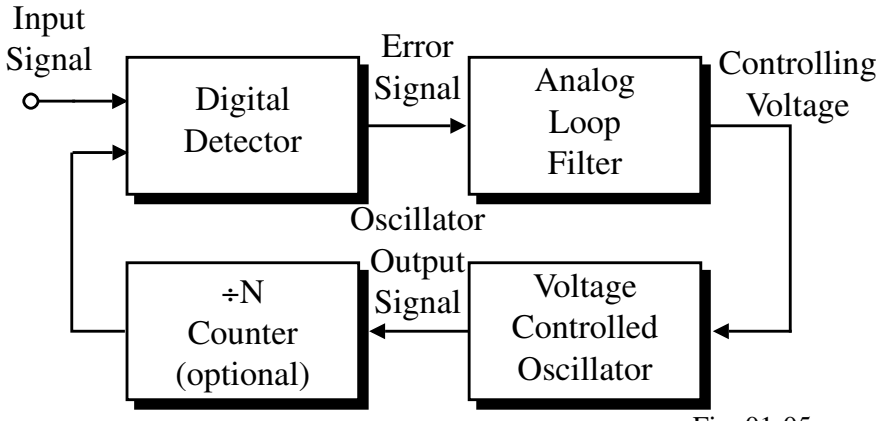

Fig. 01-05

The All-Digital PLL (ADPLL)

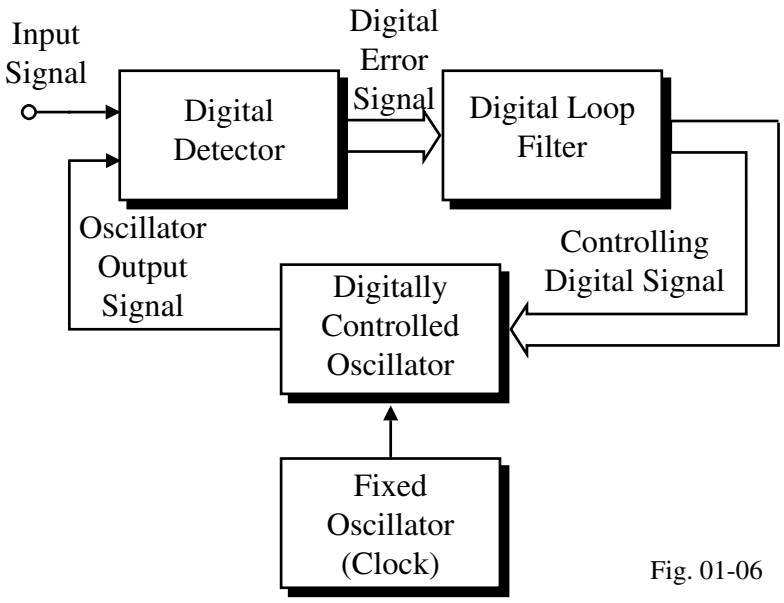

Fig. 01-06

The Software PLL (SPLL)

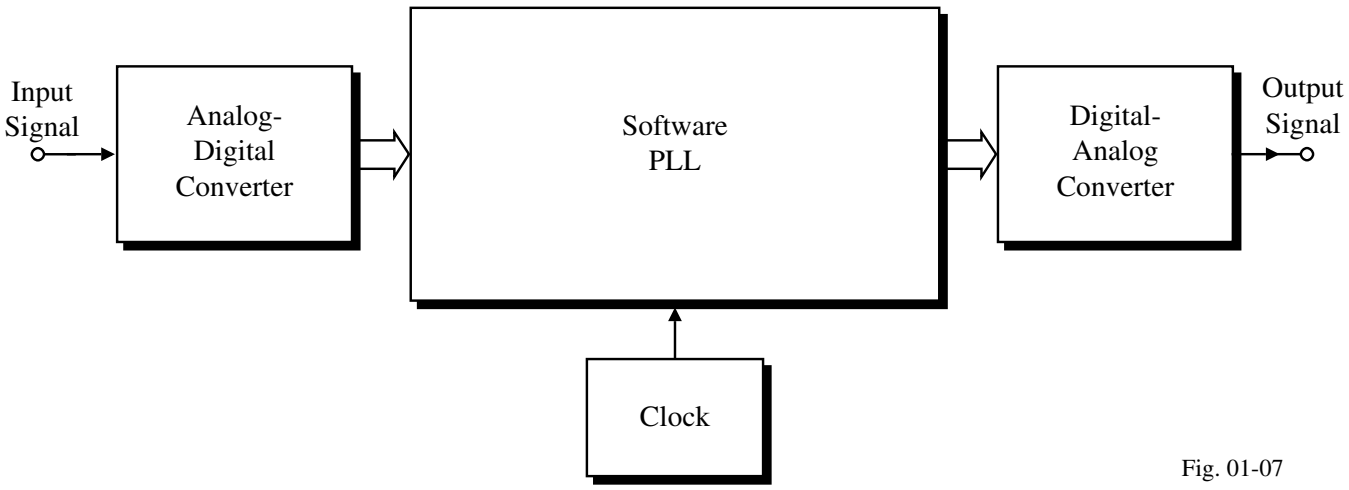

Fig. 01-07

Course Outline

1.) Review of technology
2.) Systems perspective of the various PLLs
3.) Circuits perspective of the PLL blocks
4.) Applications of PLLs

