LECTURE 160 –CDR EXAMPLES

INTRODUCTION

Objective

The objective of this presentation is:

1.) Show two examples of clock and data recovery circuits in CMOS technology

Outline

- A 2.5-GB/s CDR in 0.25μm CMOS
- A 10-GB/s CDR in 0.18μm CMOS
- Course Summary

A 2.5-GB/s CLOCK AND DATA RECOVERY CIRCUIT†

Introduction

Important considerations in this design are:

- Jitter
- VCO tuning range
- 2.5 GHz speed in 0.25μm CMOS technology
- Skew in phase detector and decision circuit

General block diagram of the architecture:

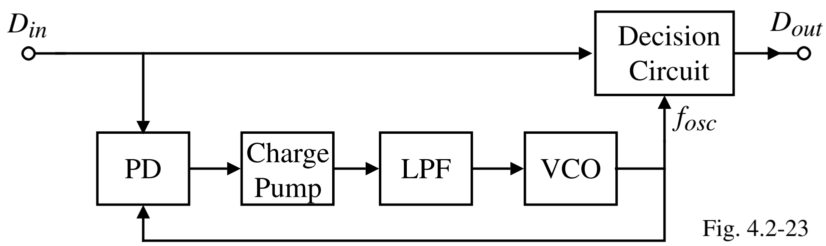


Fig. 4.2-23

† B. Razavi, "A 2.5-Gb/s 15-mW clock recovery circuit," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 472 - 480, April 1996.

Jitter Issues

Source of jitter:

- Input jitter, VCO device noise, VCO jitter due to ripple on control, supply and substrate noise.

Trade-offs in the choice of VCO gain, K_{VCO}:

- Low supply voltage necessitates high K_{VCO} for a given tuning range.
- For a given ripple on the control line, higher K_{VCO} results in higher jitter.

Solution:

Decompose the control line into fine and coarse control lines. The coarse control will be driven by the frequency detector and will remain quiet.

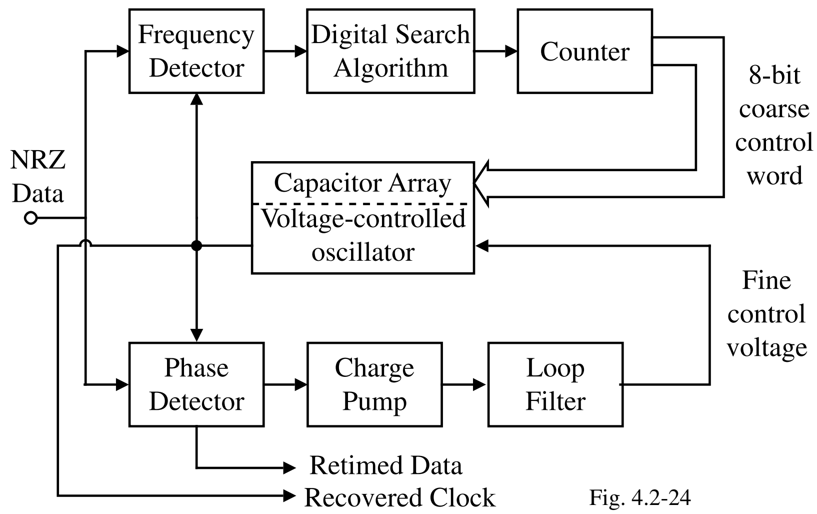


Fig. 4.2-24

Frequency Detector

Uses the Pottbacker quadrature frequency detector:

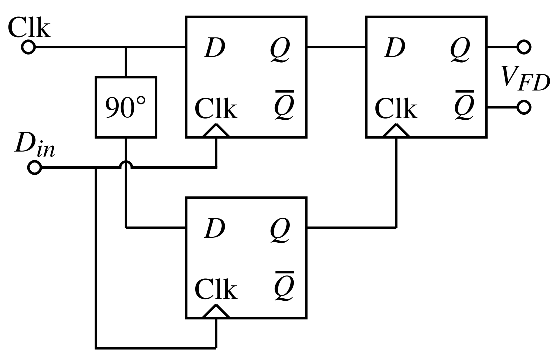
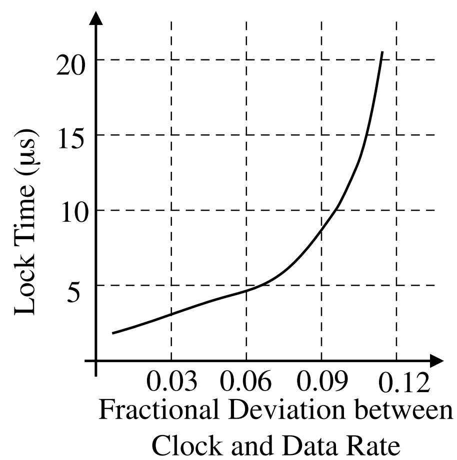


Fig. 4.2-25



Frequency Detector – Continued

Add a charge pump to the previous circuit to get:

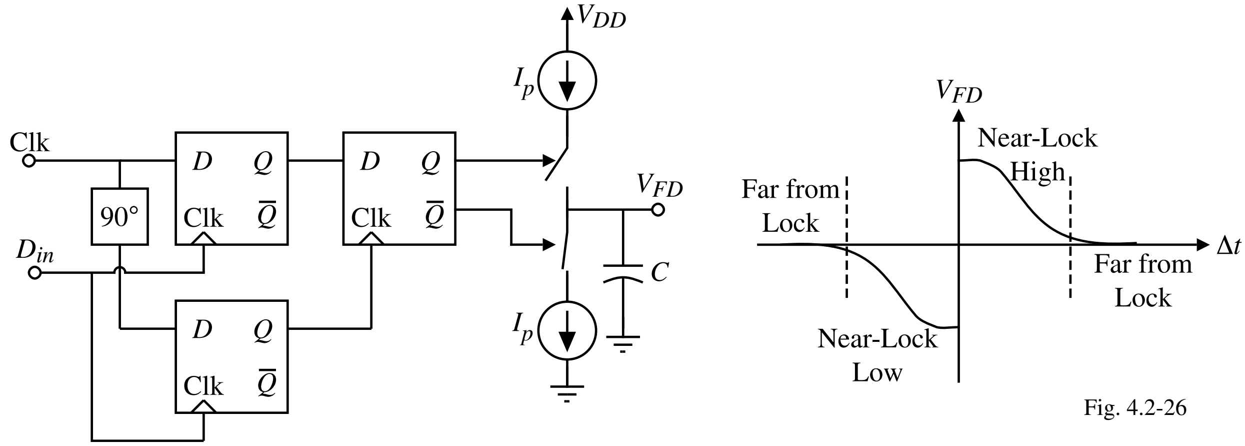


Fig. 4.2-26

Comments:

- In the near-lock regions, the output carries enough DC content to signify the polarity of the frequency difference.
- In the far-from-lock regions, the output carries little information.

Digital Search Algorithm with a Broad Range

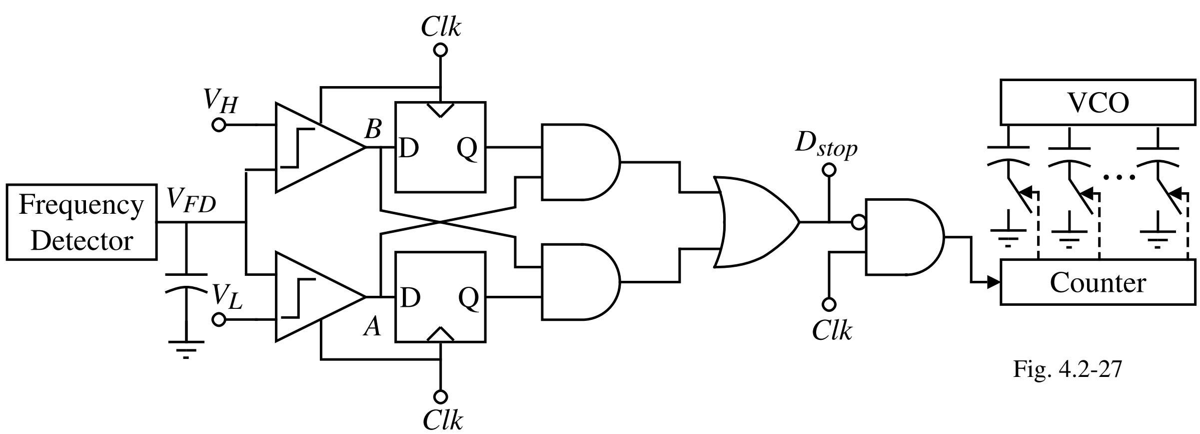


Fig. 4.2-27

Comments:

- 8 bits of resolution in the capacitor array allows a frequency step of 2.1 MHz.
- The fine VCO control can have a gain of only 50MHz/V.

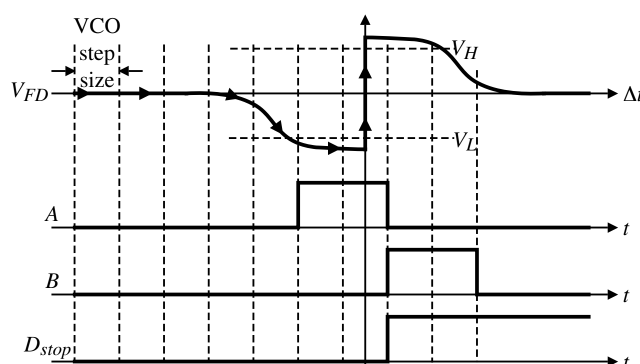


Fig. 4.2-28

VCO Circuit Implementation

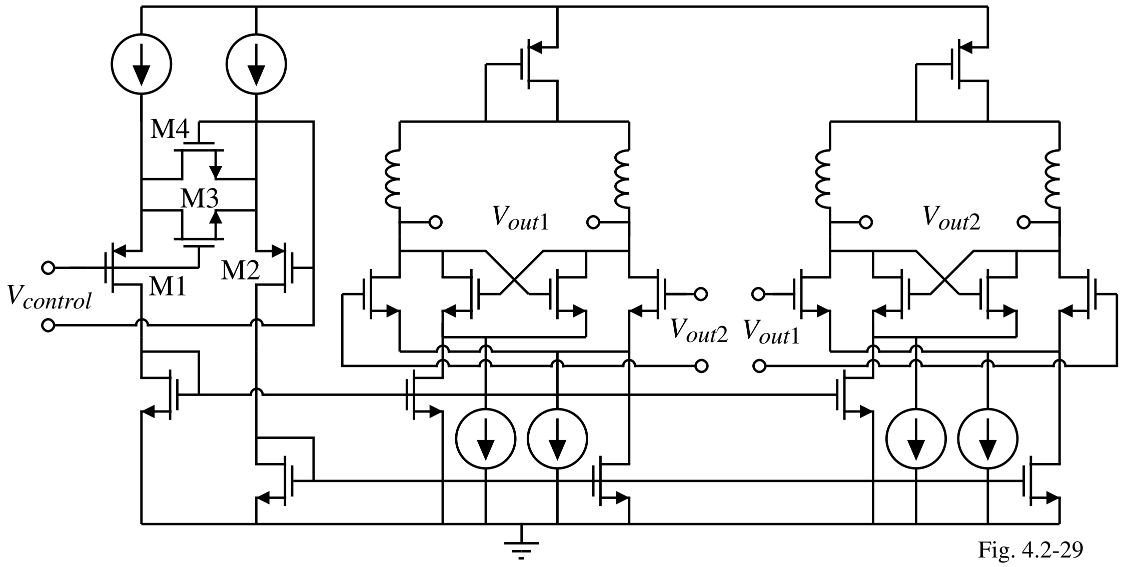


Fig. 4.2-29

Comments:

- Continuous frequency tuning is obtained by varying the coupling between oscillators.
- The VCO has a fully differential control.
- The input V/I converter, M1-M2, linearizes the input transconductance with M3-M4.

Capacitor Array

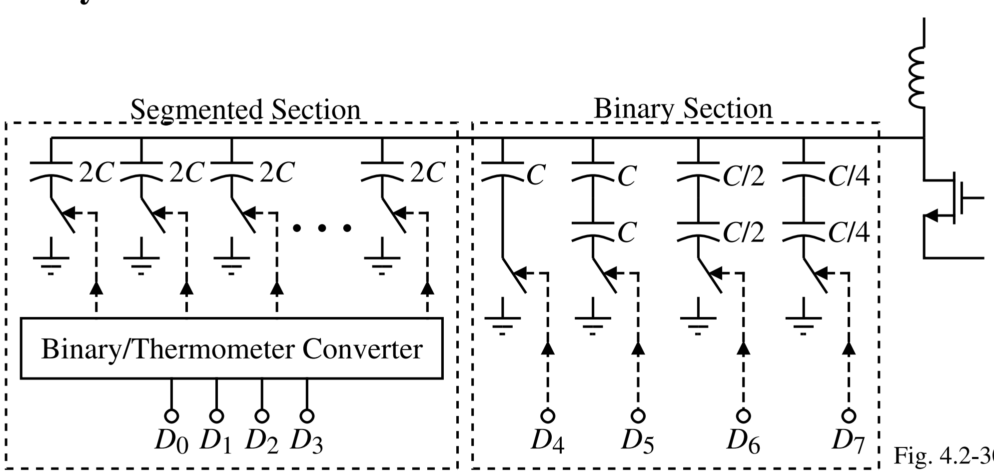


Fig. 4.2-30

Comments:

- The capacitors are divided into a 4-bit (MSB) segmented section and a 4-bit (LSB) binary-weighted section.
- Monotonicity guaranteed with up to 12.5% capacitor mismatch.
- Requires only 20 switched elements and has a worst case Q of 10.

Quadrature Frequency Detector Implementation

Use dummy loading to balance out delays.

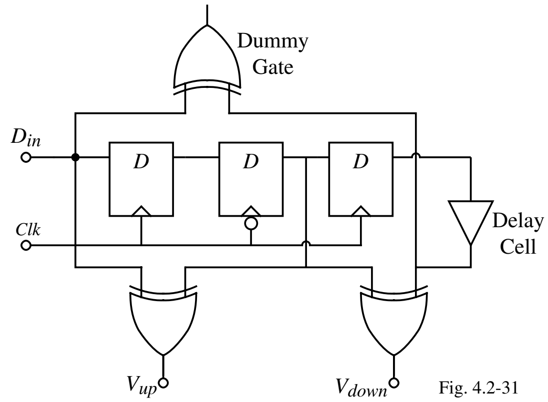
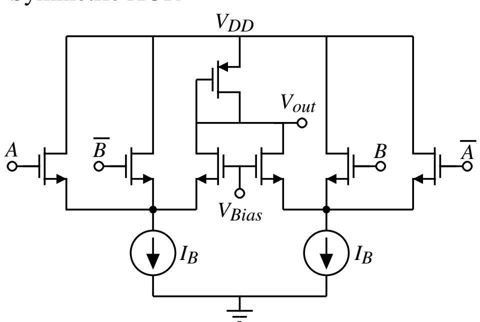


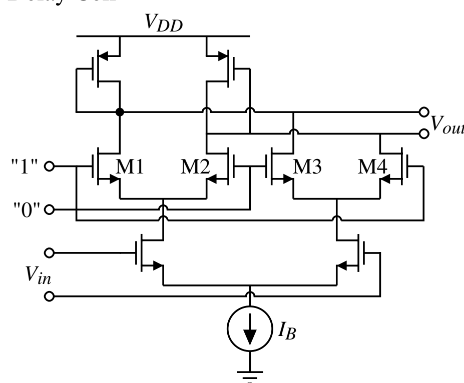
Fig. 4.2-31

Circuit Implementation:

Symmetric XOR

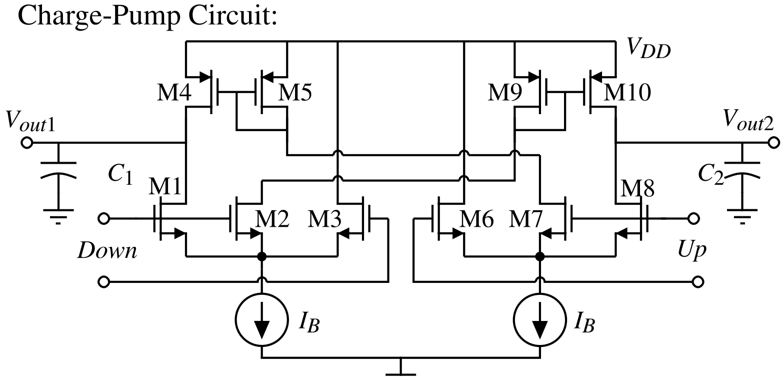


Delay Cell

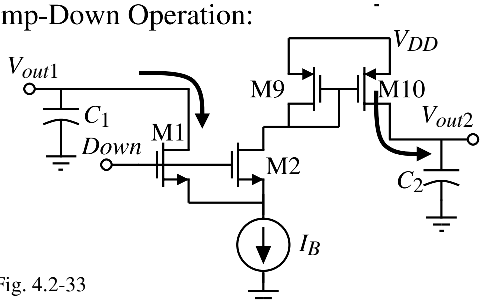


Charge Pump Implementation

Charge-Pump Circuit:



Pump-Down Operation:



No Up or Down Pulses:

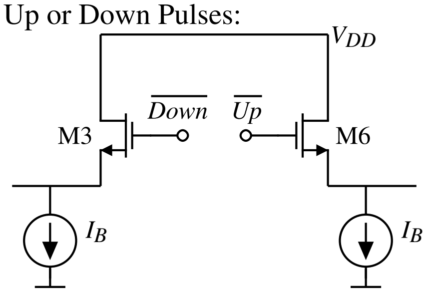


Fig. 4.2-33

This charge-pump has no current mismatch or charge mismatch.

Implementation of the Charge Pump – Continued

Conventional Implementation: This implementation:

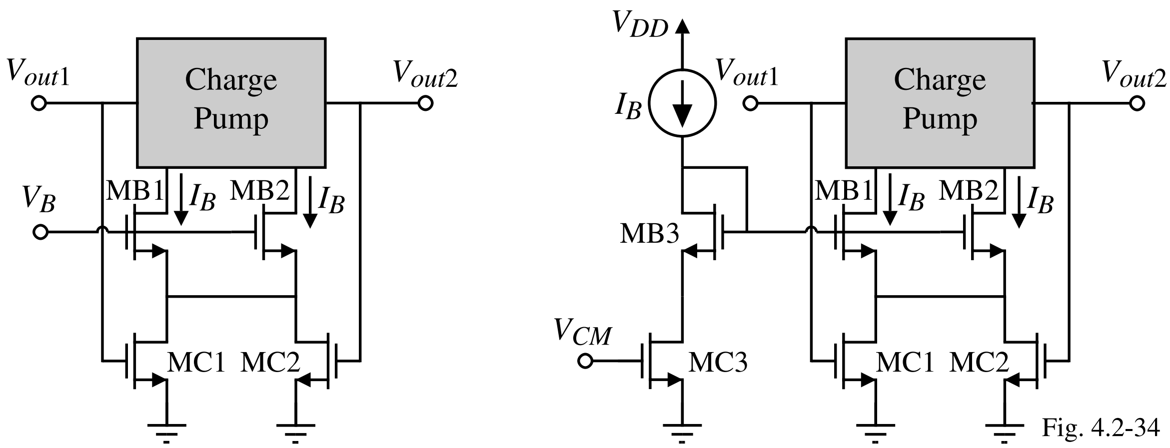
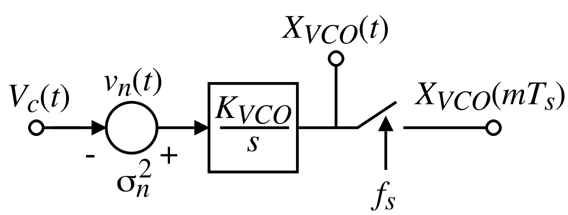


Fig. 4.2-34

The modified implemention stabilizes the common-mode output of the charge pump to a specific value, V_{CM}.

Theoretical Jitter Analysis (Open Loop)

Block diagram of the jitter model:



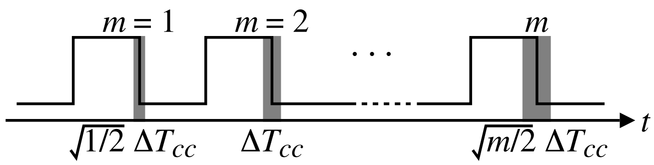


Fig. 4.2-35

The variation of the jitter as a function of mT_s can be written as,

$$\Delta T(mT_s) \approx K_{VCO}\sqrt{\frac{mT_s}{2}}\,\sigma_n\,\frac{T_s}{2\pi}$$

Therefore,

$$\Delta T(t) \approx \sqrt{\frac{f_o t}{2}}\;\Delta T_{cc}$$

Jitter Analysis – Continued

Recall that timing jitter creates phase noise, i.e.,

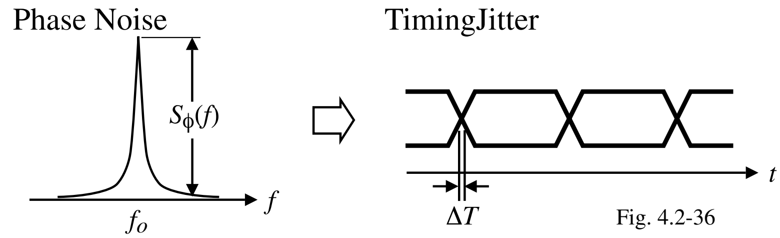


Fig. 4.2-36

$$S_\phi(f) \approx \frac{K_{VCO}^2\,\sigma_n^2}{2(2\pi)^2(f-f_o)^2}$$

$$\sigma_T{}^2 = \Delta T_{cc}^2 \approx \frac{2}{f_o^3} S_\phi(f)\,(f-f_o)^2$$

Illustration:

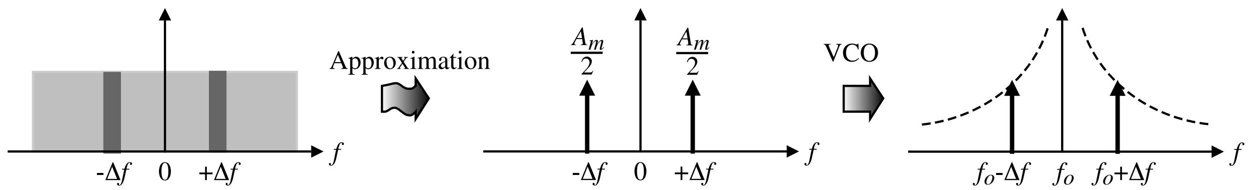


Fig. 4.2-37

Simulated Open- and Closed-Loop Jitter

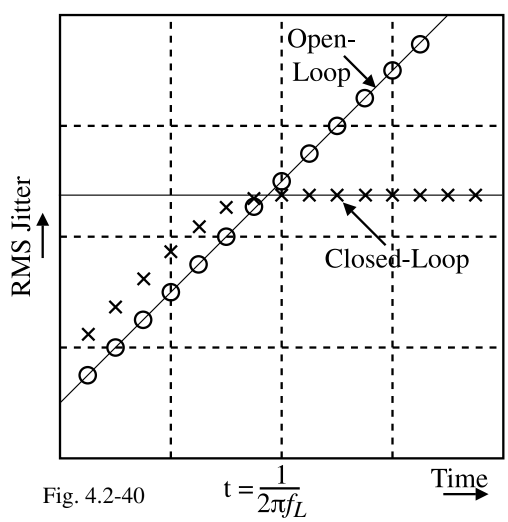
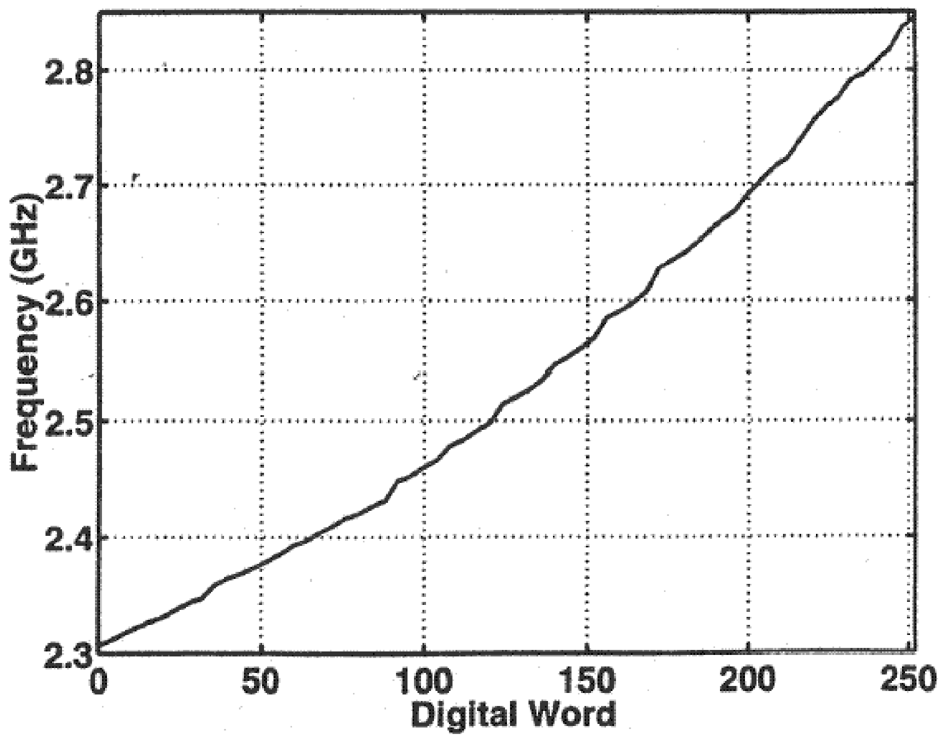


Fig. 4.2-40

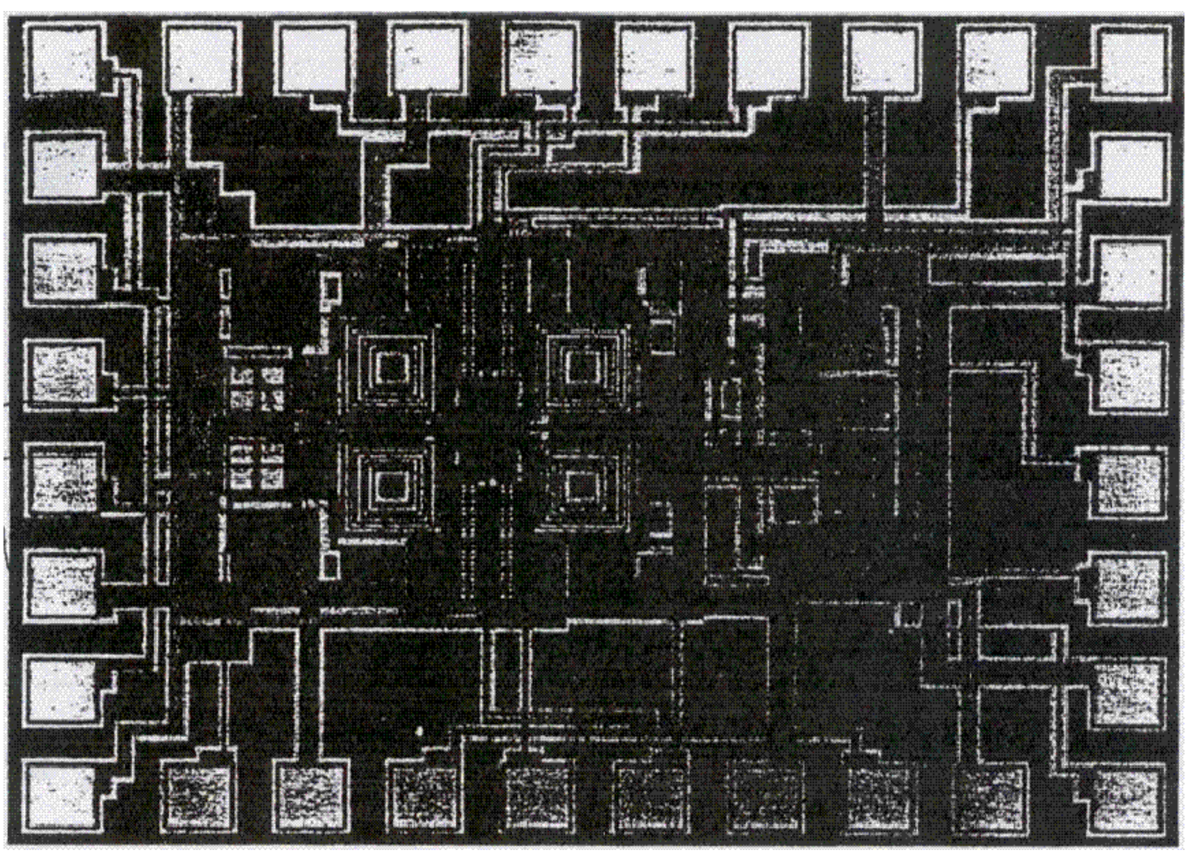
Maximum closed-loop jitter = $\sqrt{\frac{f_o}{2}}\;\Delta T_{cc}\sqrt{\frac{1}{2\pi f_L}}$

(J. McNeill, *JSSCC*, June 1997)

Measured VCO Characteristics

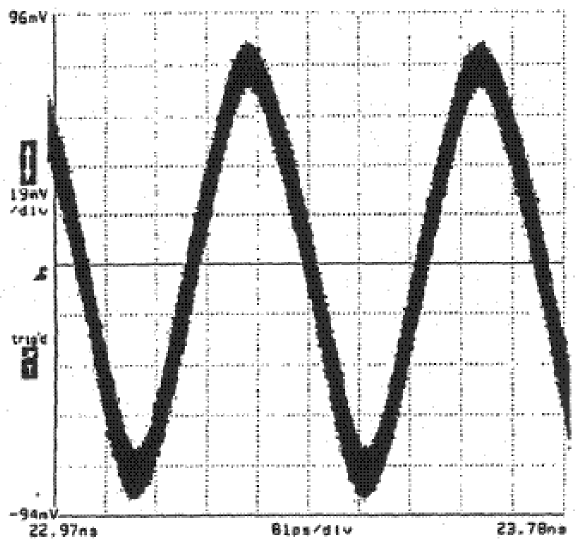


Chip Microphotograph

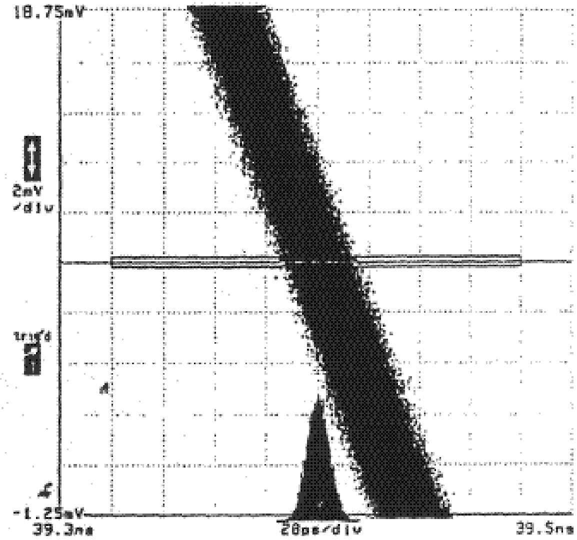


Jitter Measurements

PRBS of length 2^{23}-1:

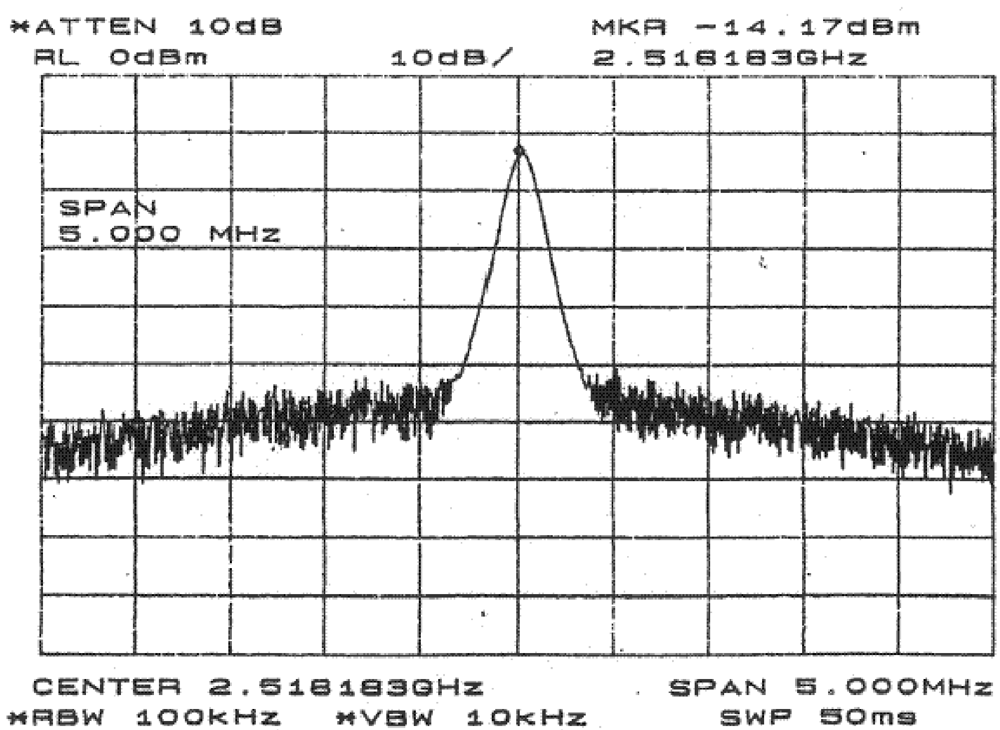


81 ps/div



20 ps/div

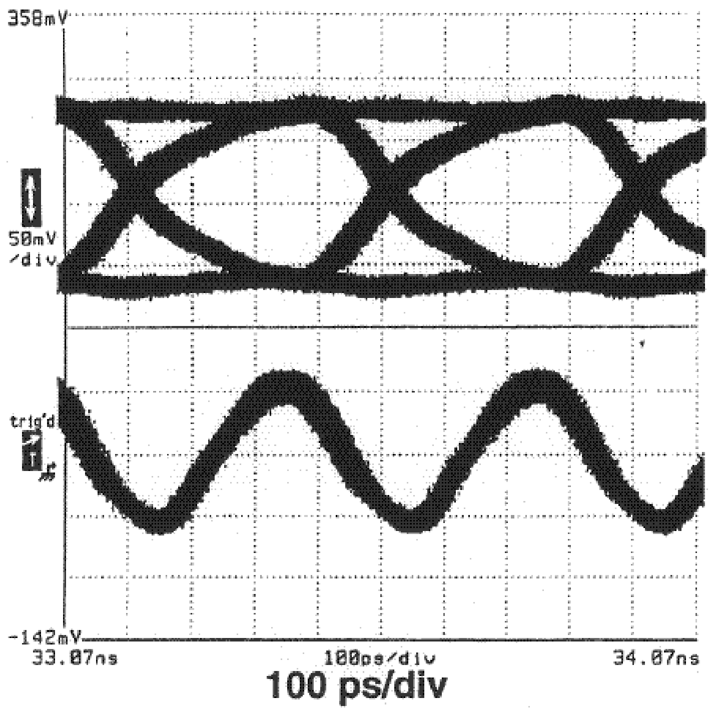
Recovered Clock Spectrum



10 dB/div

500 kHz/div

Eye Diagram



Theoretical Jitter versus Measured Jitter

Phase Noise

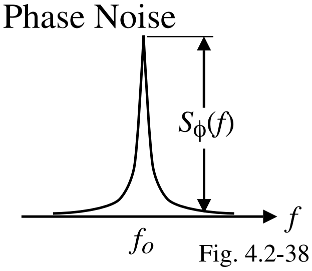


Fig. 4.2-38

- Measured free-running VCO phase noise = -85 dBc/Hz
- Closed-loop bandwidth = 3.1 MHz
- Theoretical closed-loop jitter = 5.08 ps

TimingJitter

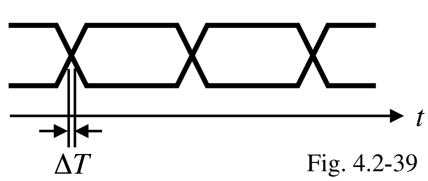


Fig. 4.2-39

Experimental closed-loop jitter = 5.1 ps

Summary of Experimental Results

Specification	Value
Bit Rate	2.5 Gb/s
Capture Range	540 MHz
Phase Noise at 1-MHz Offset	-92 dBc/Hz
Jitter for PRBS 2^{23}-1	5.1 ps
Power Dissipation:	
VCO	11mW
VCO Buffer	8mW
Phase detector and charge pump	28.5mW
Frequency detector and comparator	7.5mW
Total	55mW
Supply Voltage	2.5V
Die Area	0.9 mm x 0.6 mm
Technology	0.25 μm CMOS

Summary of 2.5 Gb/s Example

- A method to resolve the conflict between a wide tuning range and low VCO sensitivity is described utilizing a dual-loop topology.
- An LC-based VCO with a segmented capacitor array is used to discretely tune the oscillation frequency.
- A charge pump that reduces drift in the event of no UP or DOWN pump signal is introduced.
- A method is proposed to estimate the closed-loop jitter based on the phase noise of the free-running VCO.

A 10-Gb/s CMOS CLOCK AND DATA RECOVERY CIRCUIT WITH FREQUENCY DETECTION

Specification and Technology

Generic Clock and Data Recovery Block Diagram:

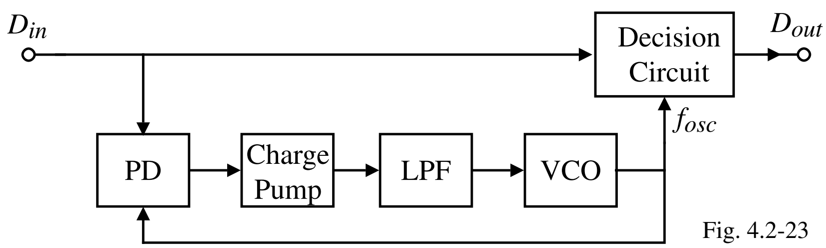


Fig. 4.2-23

Issues are:

- Jitter
- Skew between D_{in} and *Clk*
- Suitability for implementation in VLSI technology
- Power dissipation

Choice of Technology

Technology will be 0.18μm CMOS

Consequences:

- Limited speed:
  - Digital latches < 10 GHz
  - Phase detector < 10 GHz
- Low supply voltage (1.8V):
  - Limits the choice of circuit topologies
  - Leads to a large VCO gain and potentially high jitter

Choice of VCO

- LC
  - Small jitter
  - High center frequency
  - Narrow tuning range
  - Single-ended control
- Ring Oscillator
  - Large jitter
  - Low center frequency
  - Wide tuning range
  - Differential control

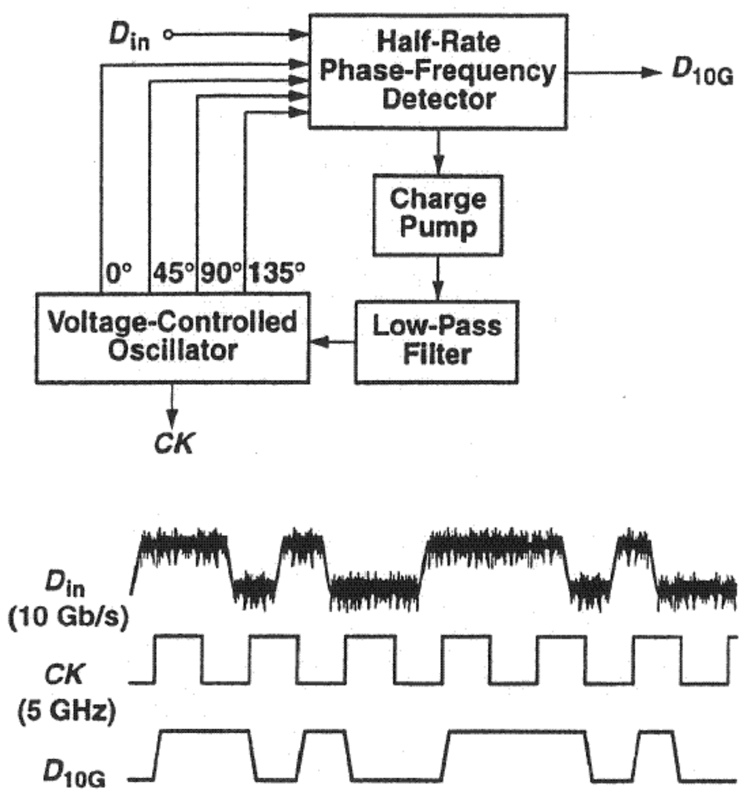
Phase Detector Design Issues

1.) System level
    Linear PD versus a bang-bang (Alexander)
2.) Technology limitations
    Full rate PD versus a half rate PD
3.) Skew problems
    No regeneration versus inherent regeneration

Frequency Detector Design Issues

1.) Capture range
    Analog versus digital
2.) System complexity
    Additional frequency detector versus phase detector compatibility
3.) Technology limitations
    Full rate FD versus a half rate FD

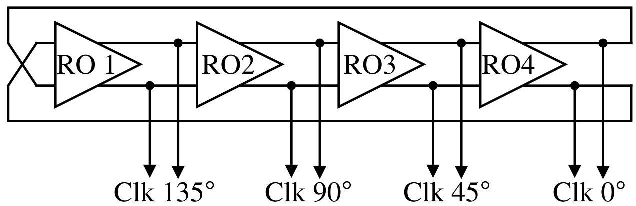
Clock Data Recovery Architecture for this Example



030904-05

Multiphase VCO

Use a 4-stage ring oscillator with spiral inductors and MOS varactors.



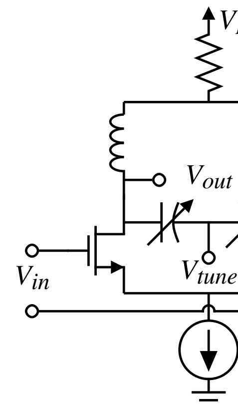


Fig. 4.2-47

Comments:

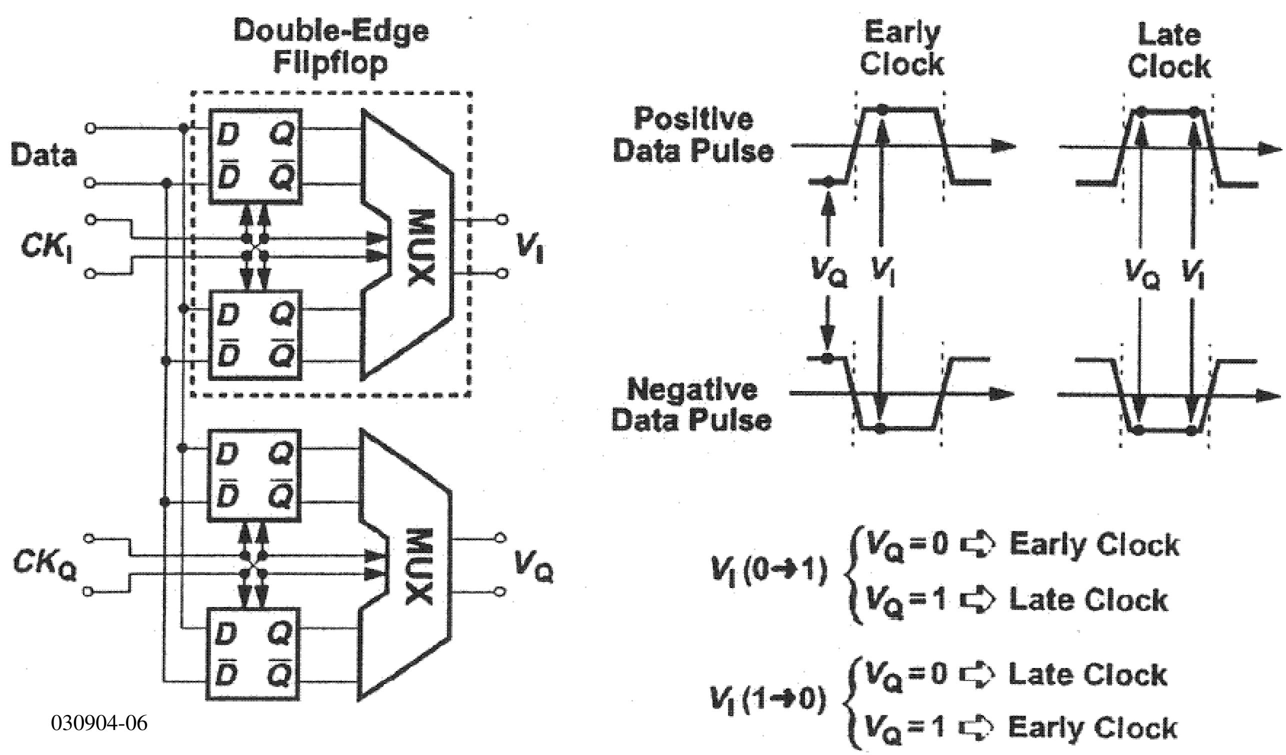
- The LC tank improves the phase noise of the oscillator
- The oscillation frequency is only a weak function of the number of stages

  If we model each stage by a parallel RLC circuit, the phase shift of each stage should be 45°. Therefore,

$$\text{Arg}[Z(j\omega)] = 45° \quad \Rightarrow \quad \tan^{-1}\left(\frac{L\omega}{R_p(1\text{-}LCQ\omega^2)}\right) = 45° \quad \Rightarrow \quad \omega_{osc} = \frac{1}{\sqrt{LC}}\sqrt{1 - \frac{1}{Q}}$$

- The oscillator’s common mode level is shifter to provide a large tuning range.

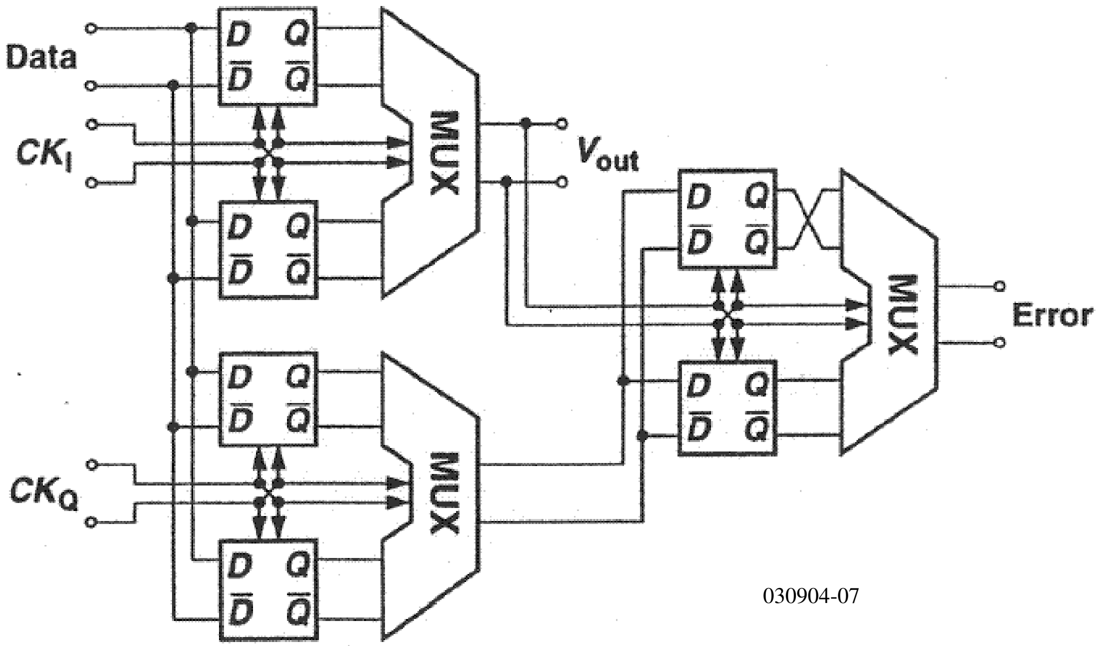
Half-Rate Phase Detection



030904-06

If V_1 makes a high-to-low transition, V_Q must be inverted to provide consistent phase error information.

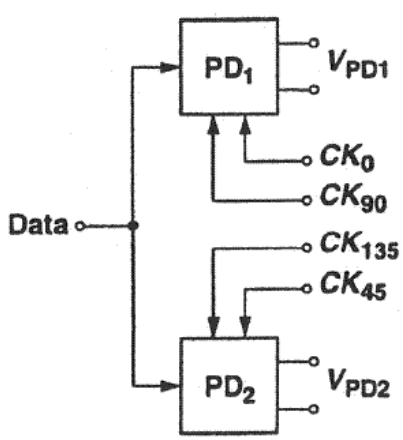
Overall Phase Detector (Anderson – U.S. Patent #3,626,298, 1971)

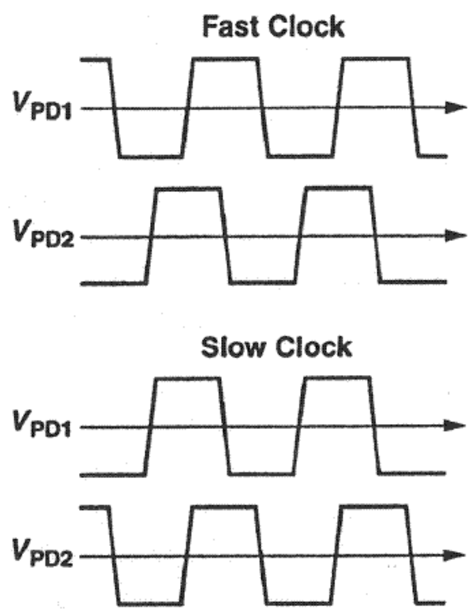


Comments:

- CK_I and CK_Q are 5GHz quadrature clock phases
- Data is a 10 Gb/s input data signal
- V_{out} is a 10 Gb/s output data signal

Half-Rate Frequency Detection

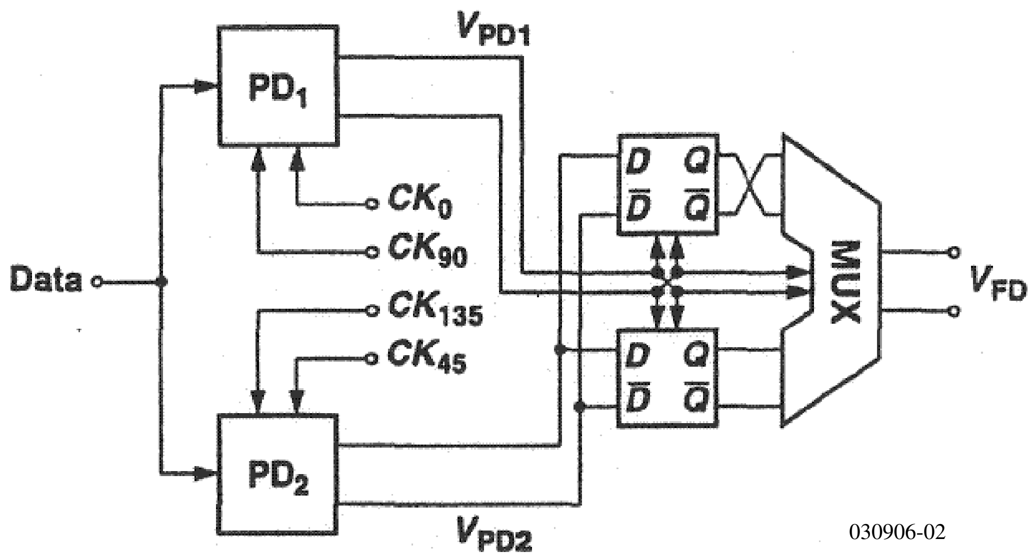




$$V_{PD1}(0\rightarrow 1)\begin{cases} V_{PD2}=0 & \Rightarrow \text{Slow Clock} \\ V_{PD2}=1 & \Rightarrow \text{Fast Clock} \end{cases}$$

$$V_{PD1}(1\rightarrow 0)\begin{cases} V_{PD2}=0 & \Rightarrow \text{Fast Clock} \\ V_{PD2}=1 & \Rightarrow \text{Slow Clock} \end{cases}$$

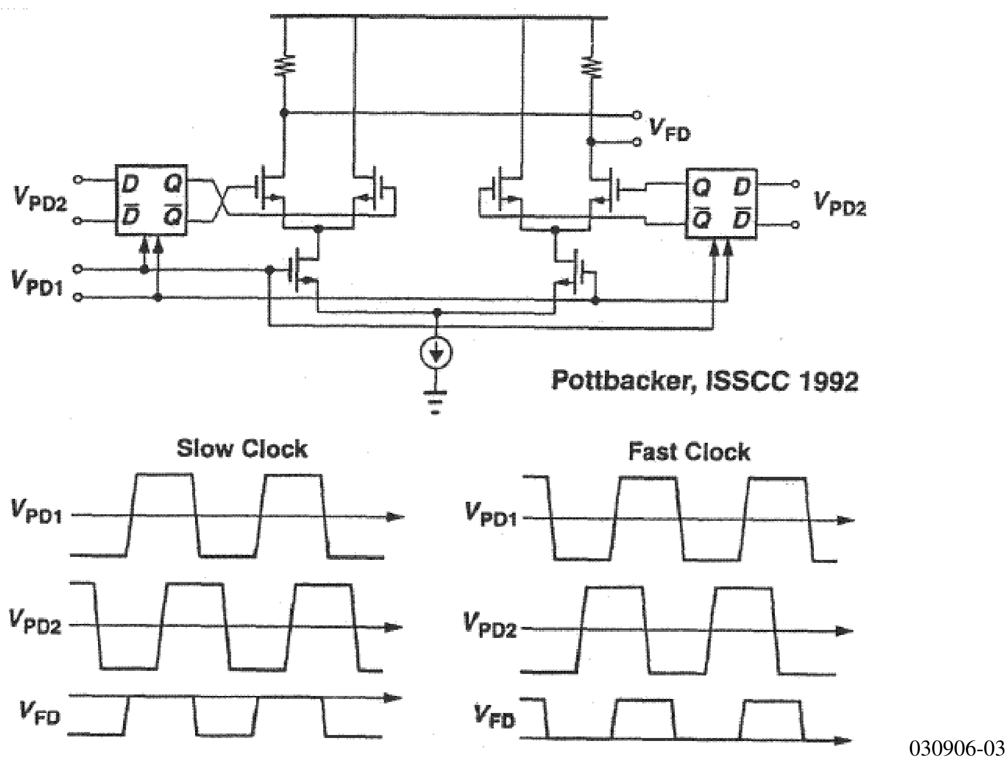
Half-Rate Frequency Detector



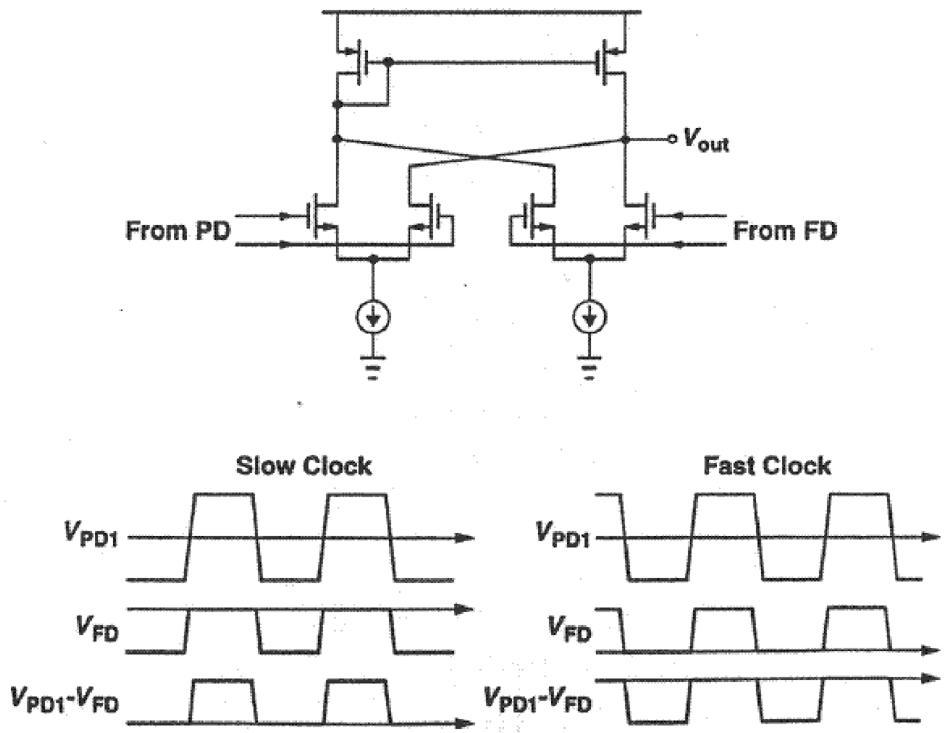
Comments:

- V_{FD} must carry unipolar pulses for fast and slow clock signals.
- V_{FD} must be a tri-state signal in the locked condition.

Modified Multiplexer



Charge Pump



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Output Buffer

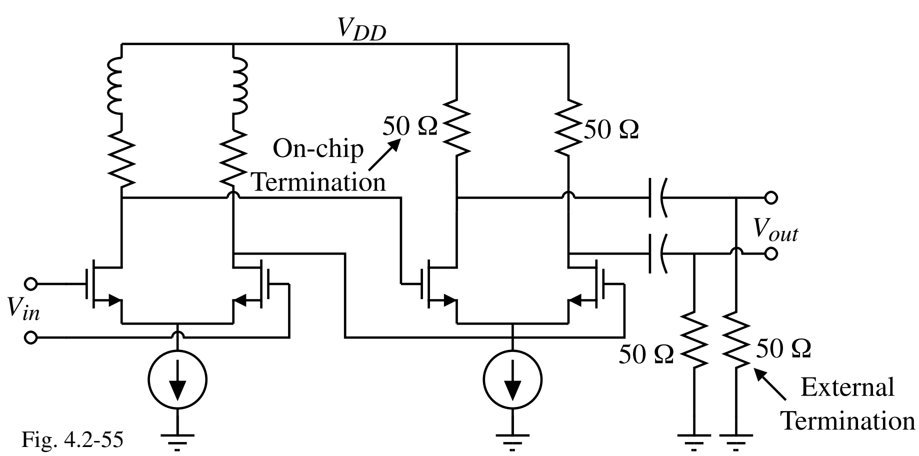
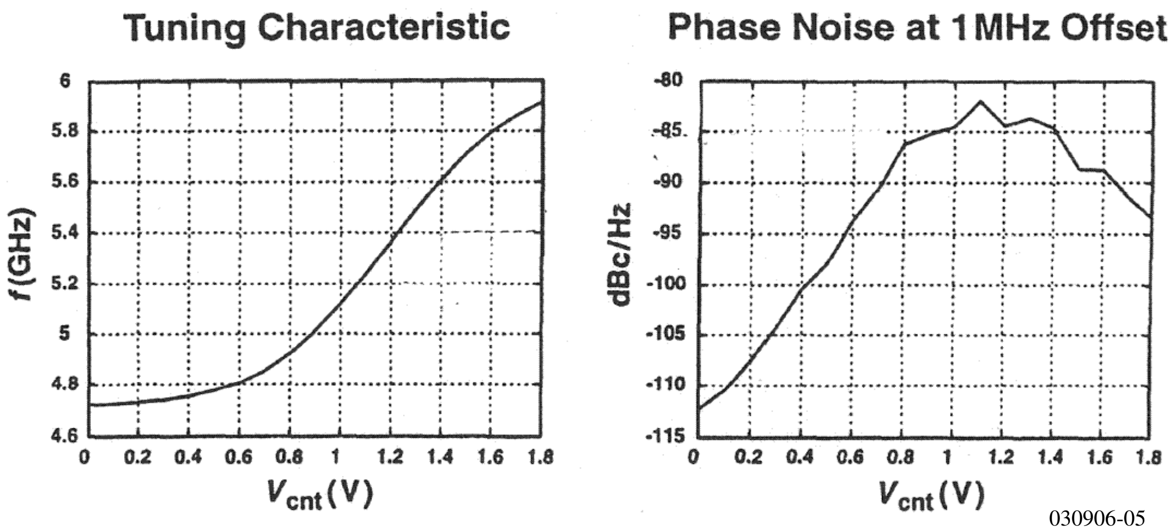


Fig. 4.2-55

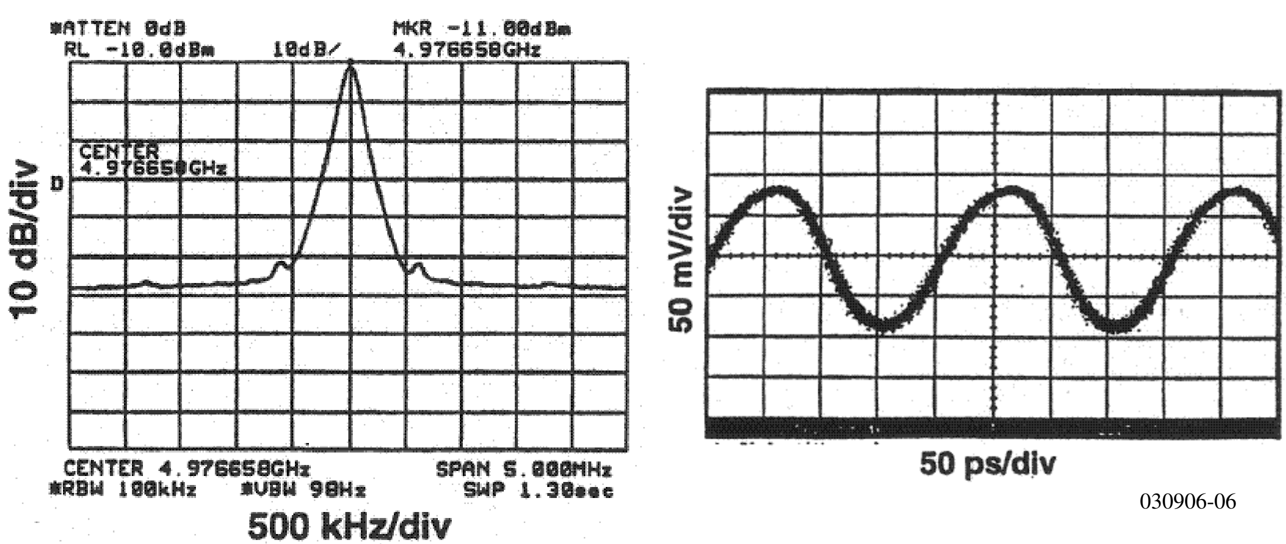
The inductors have a line width of 4µm to achieve a high self-resonance frequency.

Measured Open-Loop VCO Characteristics



030906-05

Measured Recovered Clock

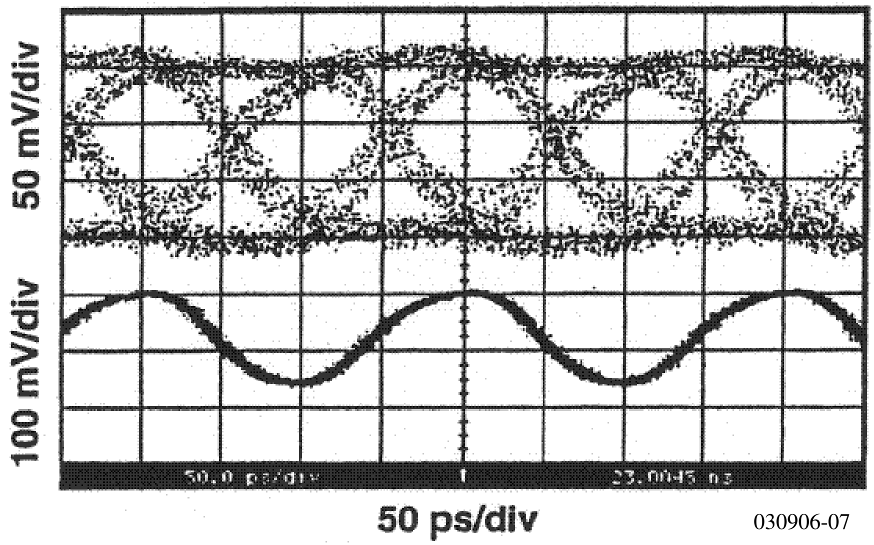


030906-06

Phase noise: -107 dBc/Hz at 1MHz offset.

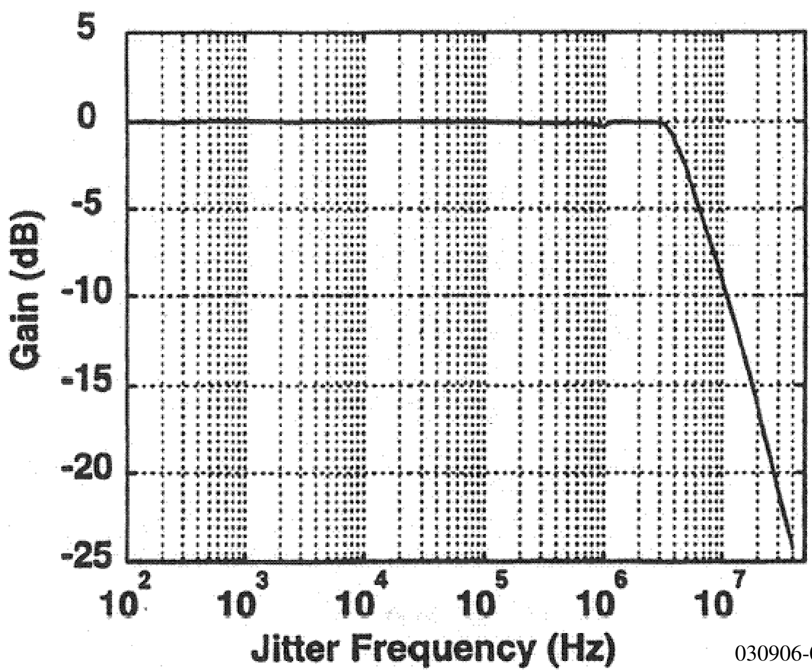
Input Sequence (PRBS)	Jitter (pp) (ps)	Jitter (rms) (ps)
2^{23}-1	9.9	0.8
2^{7}-1	2.4	0.4

Measured Data



030906-07

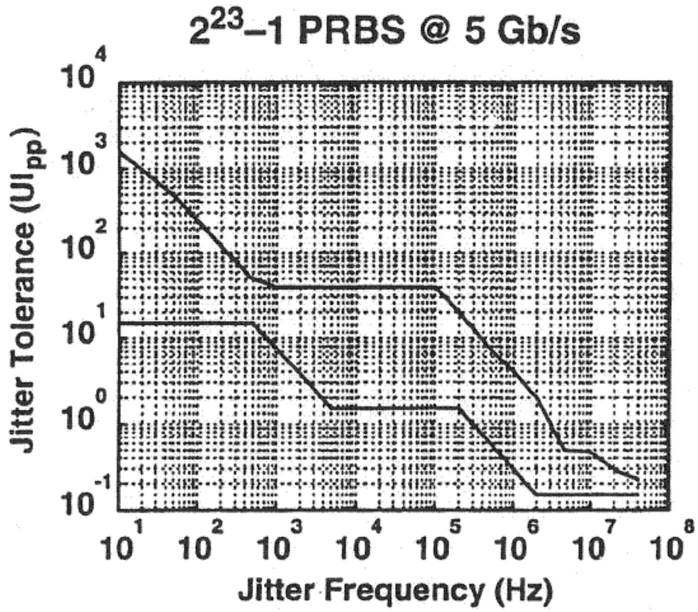
Measured Jitter Transfer Characteristic



030906-08

Loop Bandwidth = 5.2 MHz
Jitter Peaking = 0.04 dB

Measured Jitter Tolerance Characteristic



BER@10Gb/s = 10^{-9}

BER@5Gb/s = 10^{-12}

Output buffer probably increases the BER at lower bit rates.

Performance Summary

Characteristic	Performance
Input Bit Rate	10 Gb/s
Output Bit Rate	10 Gb/s
Output Clock	5 GHz
Capture Range	1.43 GHz
RMS Jitter	0.8 ps
Loop Bandwidth	5.2 MHz
Power Dissipation Oscillator: PFD: Buffers and Bias Circuits Total	 30.6 mW 42.2 mW 18.2 mW 91 mW
Area	1.75 mm x 1.55 mm
Supply Voltage	1.8V
Technology	0.18 µm CMOS

Summary of 10Gb/s Example

- A half-rate architecture relaxes the speed constraints of the system.
- A four-stage LC oscillator provide multiple phases with low jitter.
- A half-rate phase and frequency detector with inherent retiming is introduced.
- Inductive peaking enhances speed of the output buffers.

COURSE SUMMARY

Outline of Material Covered

Introduction to Phase Locked Loops (PLLs)

Systems Perspective of PLLs

- Linear PLLs
- Digital PLLs (DPLLs)
- All-Digital PLL (ADPLLs)
- PLL Measurements

Circuits Perspective of PLLs

- Phase/Frequency Detectors
- Filters and Charge Pumps
- Voltage Controlled Oscillators (VCOs)
- Phase Noise in VCOs

PLL Applications and Examples

- Applications of PLLs
- Frequency Synthesizers for Wireless Applications
- Clock and Data Recovery Circuits

Objective

Understand and demonstrate the principles and applications of phase locked loops using integrated circuit technology with emphasis on CMOS technology.

CMOS Technology

How well does CMOS implement the PLL?

- Very good for digital circuits and lower speed analog circuits
- Practical speed limits are found around 5-10 GHz. The primary challenge here is the VCO.
- At this point, circuit cleverness should allow most PLL applications to be possible and practical. With time, CMOS technology should allow the speed barrier to be pushed out.

Some Key Points

- CMOS is capable of implementing all types of PLLs – LPLL, DPLL, and ADPLL
- Noise in the PLL consists of component noise and timing jitter, both resulting in phase noise.
- Blocks of the PLL include the PFD/PD, filter, and VCO.
- To reduce phase noise in PLLs due to the VCO:
  - Make the tank Q or resonator Q large
  - Maximize the signal power
  - Minimize the impulse sensitivity function (ISF)
  - Force the energy restoring circuit to function when the ISF is at a minimum and to deliver its energy in the shorted possible time.
  - The best oscillators will possess symmetry which leads to minimum upconversion of 1/f noise.

Applications of PLLs

1.) Frequency synthesizer

GSM
Bluetooth

2.) Clock and data recovery

2.5 Gb/s
10 Gb/s

Pertinent References

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