LECTURE 080 –PHASE FREQUENCY DETECTORS

INTRODUCTION

Introduction

The objective of this presentation is examine and characterize phase/frequency detectors at the circuits level. Most of the circuits presented will be compatible with CMOS technology.

Organization:

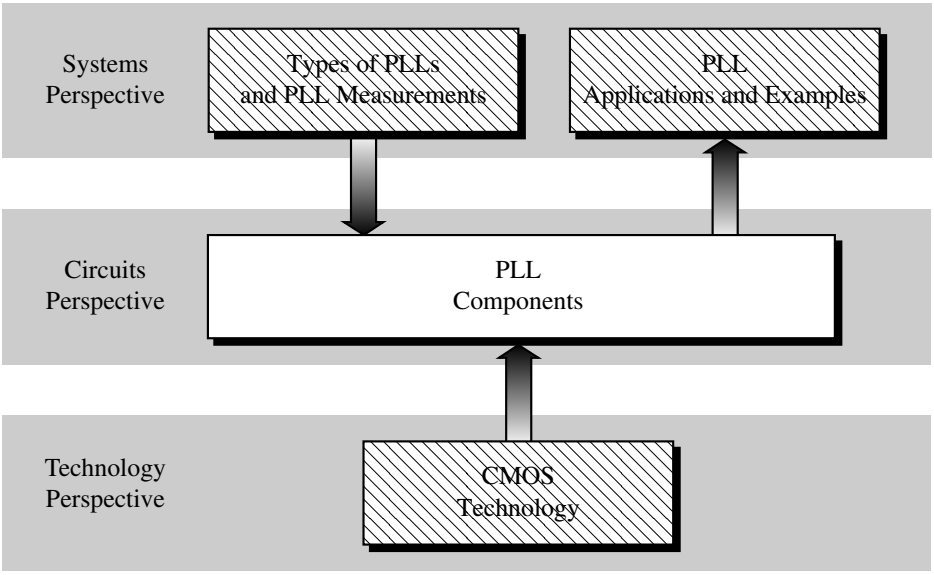


Fig. 030901-09

Outline

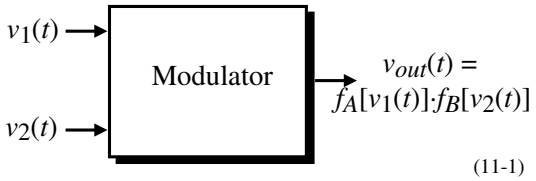
- Analog Multipliers
- Digital Detectors
- Summary

ANALOG MULTIPLIERS

Linear Multipliers

Modulators vs. Multipliers

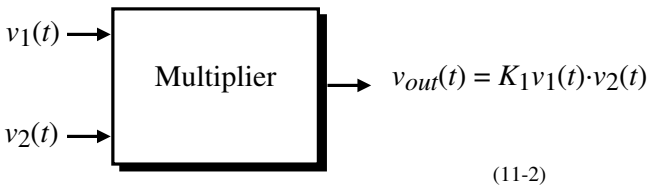
A *modulator* is a circuit with multiple inputs where one input can modify or control the signal flow from another input to the output.



(11-1)

where f_A and f_B are two arbitrary functions of $v_1(t)$ and $v_2(t)$, respectively.

A *multiplier* is a modulator where f_A and f_B are linear functions of $v_1(t)$ and $v_2(t)$.



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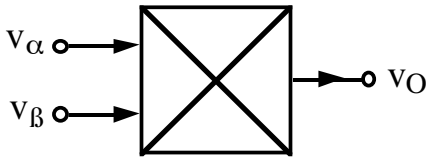
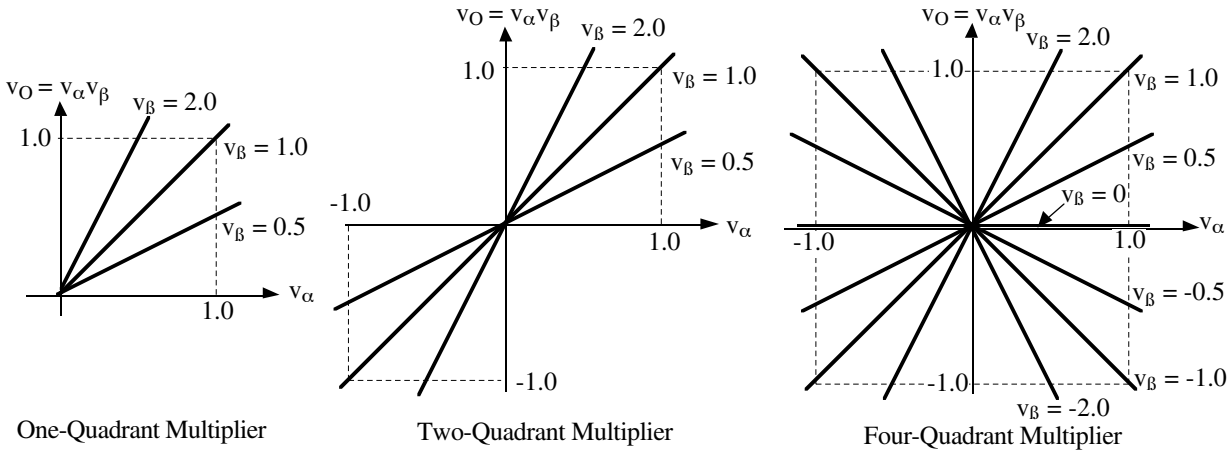
Applications of Multipliers

- Nonlinear analog signal processing
- Mixing
- Phase difference detection
- Modulation and demodulation
- Frequency translation

Symbol



Types of Multiplication



One-Quadrant Multiplier | Two-Quadrant Multiplier | Four-Quadrant Multiplier

Scaling:

Let K_m be a scaling constant such that

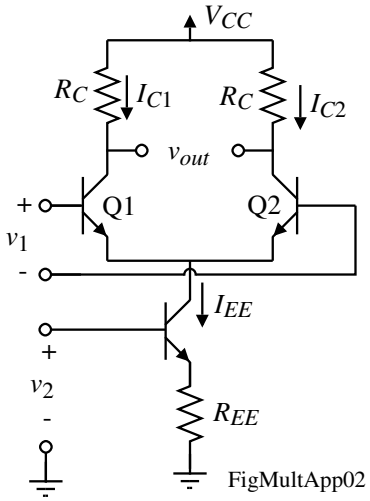
$$v_O = K_m v_\alpha v_\beta.$$

If V_{max} = max $|v_\alpha|$ or max $|v_\beta|$, then $K_m = \frac{1}{V_{max}}$ so that max $|v_O| = V_{max}$

Simple BJT 2-Quadrant Multiplier

The differential amplifier makes a simple multiplier/modulator.

Circuit:



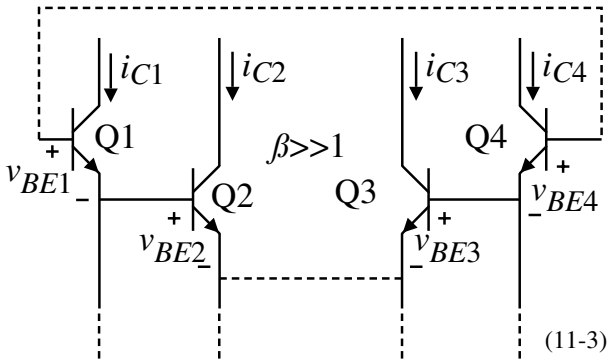
$$\Delta I_C = I_{C1}\text{-}I_{C2} = \alpha_F I_{EE}\ tanh\left(\frac{v_1}{2V_t}\right) \quad \text{and} \quad I_{EE} = I_s \exp\left(\frac{v_2}{V_t}\right) \approx \frac{v_2 - V_{BE}(\text{on})}{R_{EE}}$$

If $v_1 << 2V_t$ and $v_2 < V_t$, then

$$\Delta I_C \approx \frac{\alpha_F I_s}{R_{EE}}\left(\frac{v_1}{2V_t}\right)[v_2 - V_{BE}(\text{on})]$$

Basic Principle of Analog Bipolar Multiplier - Gilbert Cell

Circuit:



Note that

$$v_{BE1} + v_{BE2} = v_{BE3} + v_{BE4} \qquad (11\text{-}3)$$

Substituting for v_{BE} by,

$$v_{BE} = V_t\ ln\left(\frac{i_C}{I_s}\right)$$

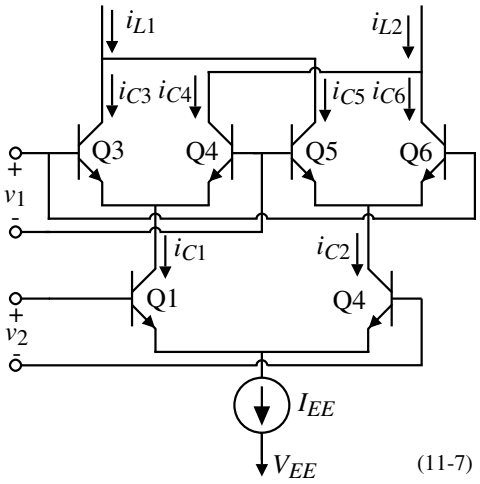
Gives,

$$ln\left(\frac{i_{C1}}{I_{s1}}\right) + ln\left(\frac{i_{C2}}{I_{s2}}\right) = ln\left(\frac{i_{C3}}{I_{s3}}\right) + ln\left(\frac{i_{C4}}{I_{s4}}\right) \quad \Rightarrow \quad ln\left(\frac{i_{C1}i_{C2}}{I_{s1}I_{s2}}\right) = ln\left(\frac{i_{C3}i_{C4}}{I_{s3}I_{s4}}\right) \Rightarrow \frac{i_{C1}i_{C2}}{I_{s1}I_{s2}} = \frac{i_{C3}i_{C4}}{I_{s3}I_{s4}}$$

If Q1 through Q4 are matched, then $I_{s1} = I_{s2} = I_{s3} = I_{s4}$, and

$$\boxed{i_{C1}i_{C2} = i_{C3}i_{C4}}$$

Gilbert Multiplier Cell



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Problems with a simple modulator are:

- 2-quadrant, $v_2 > 0$
- Small signal, $v_1 < 2V_t \approx 50\text{mV}$

Solution - Gilbert Cell:

$$i_{C3} = \frac{i_{C1}}{1 + \exp(-v_1/V_t)}, \quad i_{C4} = \frac{i_{C1}}{1 + \exp(v_1/V_t)}$$

$$i_{C5} = \frac{i_{C2}}{1 + \exp(v_1/V_t)}, \quad i_{C6} = \frac{i_{C2}}{1 + \exp(-v_1/V_t)},$$

$$i_{C1} = \frac{I_{EE}}{1 + \exp(-v_2/V_t)} \quad \text{and} \quad i_{C2} = \frac{I_{EE}}{1 + \exp(v_2/V_t)}$$

Let $\Delta i_C = i_{L1} - i_{L2} = (i_{C3} + i_{C5}) - (i_{C4} + i_{C6})$, therefore

$$i_{C3} = \frac{I_{EE}}{[1+\exp(-v_1/V_t)][1+\exp(-v_2/V_t)]}, \qquad i_{C4} = \frac{I_{EE}}{[1+\exp(v_1/V_t)][1+\exp(-v_2/V_t)]}$$

$$i_{C5} = \frac{I_{EE}}{[1+\exp(v_1/V_t)][1+\exp(v_2/V_t)]}, \qquad i_{C6} = \frac{I_{EE}}{[1+\exp(-v_1/V_t)][1+\exp(v_2/V_t)]}$$

Writing Δi_C as $\Delta i_C = (i_{C3} - i_{C6}) + (i_{C5} - i_{C4})$ gives

$$\Delta i_C = I_{EE}\left[\frac{1}{1+\exp(-v_1/V_t)} - \frac{1}{1+\exp(v_1/V_t)}\right]\left[\frac{1}{1+\exp(-v_2/V_t)} - \frac{1}{1+\exp(v_2/V_t)}\right]$$

Note that: $\dfrac{1}{1+e^{-x}} - \dfrac{1}{1+e^{x}} = \dfrac{e^{x/2}}{e^{x/2}+e^{-x/2}} - \dfrac{e^{-x/2}}{e^{x/2}+e^{-x/2}} = \dfrac{e^{x/2}-e^{-x/2}}{e^{x/2}+e^{-x/2}} = \tanh(x/2)$

Gilbert Multiplier Cell - Continued

$\therefore\ \Delta i_C = I_{EE} \tanh(v_1/2V_t) \tanh(v_2/2V_t)$ which solves the two-quadrant problem.

Assume that, $v_{OUT} = R(i_{L1} - i_{L2}) = R\Delta i_C = RI_{EE}\tanh(v_1/2V_t)\tanh(v_2/2V_t)$

Synchronous Modulator:

$v_1 << 2V_t$ and $v_2 >> 2V_t \Rightarrow v_{OUT} \approx RI_{EE}\, sgn[v_2(t)]\tanh(v_1/2V_t)$

Waveforms:

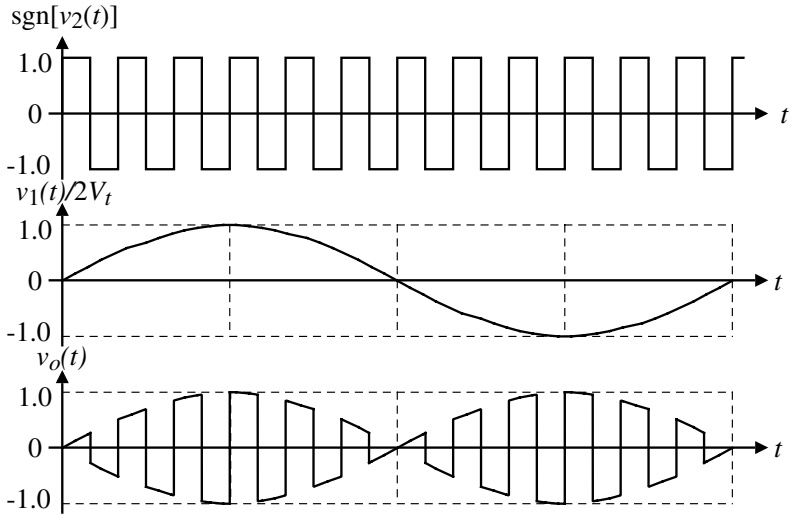
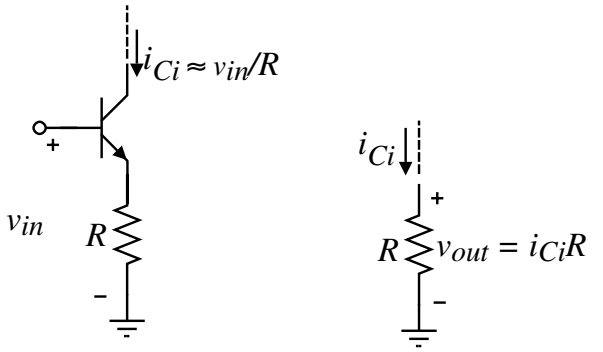


Fig. 11-8

Problem: $v_1 < 2V_t$ and $v_2 < 2V_t$

Using Voltages for the Gilbert Cell

Voltage Equivalent:



Input Circuit Output Circuit (11-4)

Therefore the previous results can be converted to,

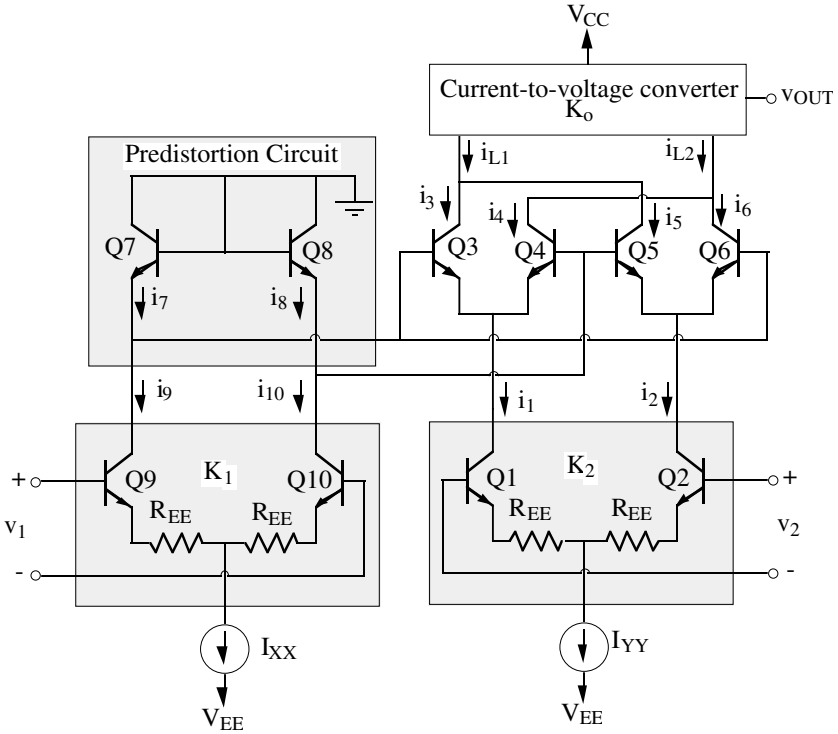
$$v_{in}v_2 = v_3v_4$$

Let v_4 be an output, then

$$v_4 = v_{out} = \frac{v_{in}v_2}{v_3}$$

Four Quadrant Linear Multiplier

Circuit:



The predistortion circuit forms tanh^{-1}x type shaping prior to the tanh x shaping of the following stage.

Four Quadrant Linear Multiplier - Continued

Analysis

Note that, $v_{BE3} - v_{BE4} + v_{BE5} - v_{BE6} = 0 \rightarrow V_T\ln\left(\frac{i_3}{I_{s3}}\right) - V_T\ln\left(\frac{i_4}{I_{s4}}\right) + V_T\ln\left(\frac{i_5}{I_{s5}}\right) - V_T\ln\left(\frac{i_6}{I_{s6}}\right) = 0$

Assuming matched transistors gives $i_3 i_5 = i_4 i_6$, $i_9 i_3 = i_4 i_{10}$ and $i_9 i_6 = i_5 i_{10}$

Also note that, $i_1 = i_3 + i_4$, $i_2 = i_5 + i_6$, $i_{L1} = i_3 + i_5$, $i_{L2} = i_4 + i_6$, and $I_{XX} = i_9 + i_{10}$

Assume that $i_9 - i_{10} = \frac{v_1}{K_1}$, $i_1 - i_2 = \frac{V_2}{K_2}$, and $v_{OUT} = K_o(i_{L1} - i_{L2})$ where $K_1 = K_2 \approx 2R_{EE}$

Now,

$$v_{OUT}=K_o[(i_4+i_6)-(i_3+i_5)]=K_o\left[\left(i_4+i_5\frac{i_{10}}{i_9}\right)-\left((i_4\frac{i_{10}}{i_9}+i_5)\right)\right]=K_o\left[i_4-i_4\frac{i_{10}}{i_9}-i_5+i_5\frac{i_{10}}{i_9}\right]=K_o(i_4-i_5)\left(1-\frac{i_{10}}{i_9}\right)=K_o\left(\frac{i_9-i_{10}}{i_9}\right)(i_4-i_5)$$

Next, find $i_4 - i_5$ in terms of $i_1 - i_2$ as follows.

$$i_1 - i_2 = (i_3 + i_4) - (i_5 + i_6) = \left(i_4\frac{i_{10}}{i_9} + i_4\right) - \left(i_5 + i_5\frac{i_{10}}{i_9}\right) = \left(\frac{i_9 + i_{10}}{i_9}\right)(i_4 - i_5)$$

Therefore, $i_4 - i_5 = \left(\frac{i_9}{i_9 + i_{10}}\right)(i_1 - i_2)$ which is the desired result.

Substituting gives

$$v_{OUT} = K_o\left(\frac{i_9 - i_{10}}{i_9}\right)\left(\frac{i_9}{i_9 + i_{10}}\right)(i_1 - i_2) = K_o\frac{(i_9 - i_{10})(i_1 - i_2)}{i_9 + i_{10}} = \frac{K_o}{I_x}(i_9 - i_{10})(i_1 - i_2)$$

$$\therefore \quad \boxed{v_{OUT} = \frac{K_o}{I_{XX}K_1K_2}v_1 v_2 = K_m v_1 v_2}$$

Gilbert Cell CMOS Multiplier

As we have seen, the classical Gilbert Cell mixer may be implemented in a single-balanced or doubly-balanced configuration.

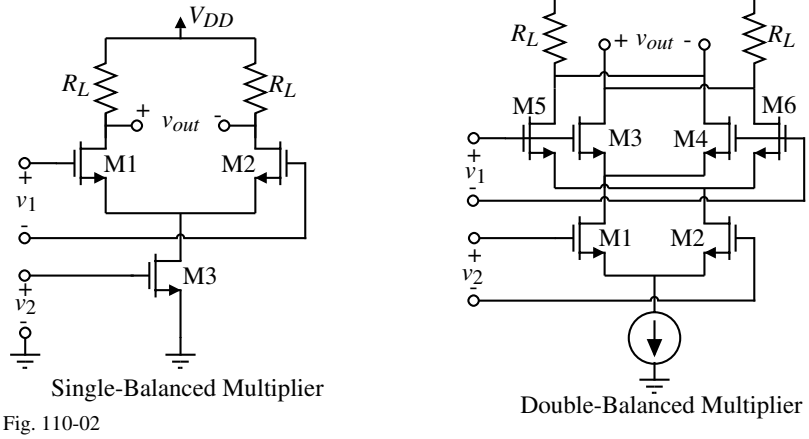


Fig. 110-02

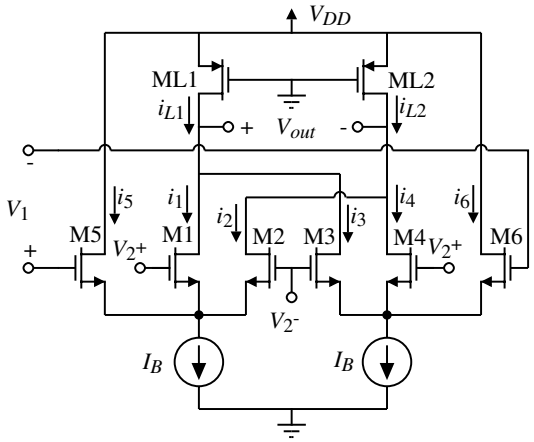
As with the BJT multipliers, one input, v_1, is large enough that it cause the differential input transistor to act as a current steering switch. As a consequence, these mixers are really modulators.

The gain of the multipliers is $g_m R_L$.

A problem with the double-balanced multiplier is that it uses three stacked transistors.

2V, High-Frequency CMOS Multiplier†

Based on the Gilbert cell with two source-followers as current modulators.



Comparison with the Gilbert cell:

- Can operate at a lower supply voltage because the mixer does not use stacking
- Source followers give better linearity
- Has a smaller mixer gain because sharing the bias currents with the followers reduces g_m

† K-K Kan, D. Ma, K-C Mak and H.C. Luong, "Design Theory and Performance of a 1-GHz CMOS Downconversion and Upconversion Mixers," *Analog Integrated Circuit and Signal Processing*, Vol. 24, No. 2, pp. 101-111, July 2000.

How Does the Previous Multiplier Work?

The oscillator input is sufficiently large that M1-M4 are fully switched on or off. Therefore, the multiplier is redrawn as shown and consists of two pairs of unbalanced source coupled MOSFETs.

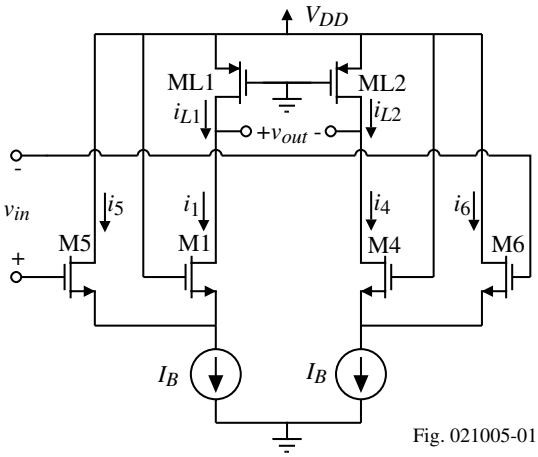


Fig. 021005-01

The differential drain current of an unbalanced source-coupled pair is

$$\Delta i_D = i_{L1} - i_{L2} = I_{DC} + i_{SQ} + i_{non}$$

where $$I_{DC} = \frac{(W_1/L_1)-(W_5/L_5)}{(W_1/L_1)+(W_5/L_5)} I_B$$

which is the current due to the asymmetry of the unbalanced source-coupled pair.

$$i_{SQ} = \frac{(W_1/L_1)(W_5/L_5)[(W_5/L_5)-(W_1/L_1)]K_n'}{[(W_1/L_1)+(W_5/L_5)]^2} V_i^{\,2}$$

which is a current proportional to the square of the differential input voltage, $V_i = V_{G1} - V_{G5}$ and where V_G is the gate voltage from the inherent square law model

$$i_{non} = \frac{2(W_1/L_1)(W_5/L_5)K_n'V_i}{[(W_1/L_1)+(W_5/L_5)]^2} \sqrt{[(W_1/L_1)+(W_5/L_5)]\frac{2I_B}{K_n'} - (W_1/L_1)(W_5/L_5)V_i^2}$$

which is the portion of current that causes harmonic distortion.

Frequency Response of the Previous Multiplier

There are four poles and one zero.

Dominant pole:

$$p_1 = \frac{1}{R_O C_O}$$

where R_O is the output resistance at V_{IF} (v_{out}).

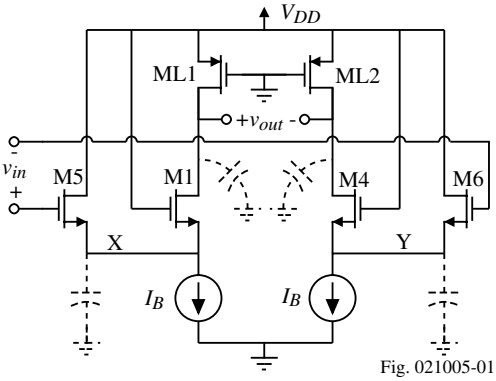


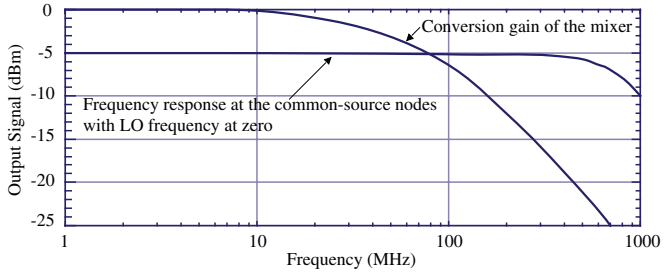
Fig. 021005-01

Second pole:

$$p_2 = \frac{g_{m1}+g_{mbs1}+g_{m5}+g_{mbs5}+g_{o5}+g_{o7}}{C_x+C_{gs1}+C_{gs5}}$$

where g_{o7} is the output conductance of I_B and C_x is the capacitance contributed by the biasing transistor as well as the cutoff transistor. The other two poles and zero are higher in magnitude and can be neglected.

Frequency response:

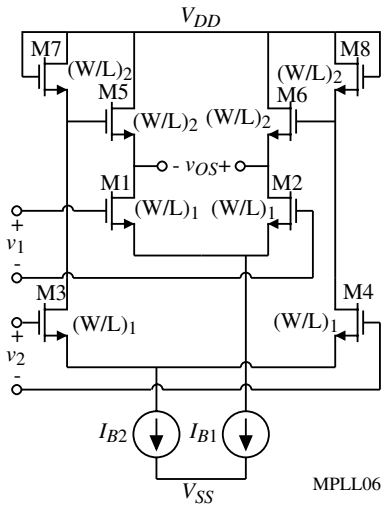


A Quarter-Square CMOS Multiplier†

Quarter-Square Principle:

$$v_O = \frac{k}{4}[(v_1+v_2)^2 - (v_1-v_2)^2] = \frac{k}{4}[v_1^2 + 2v_1v_2 + v_2^2 - v_1^2 + 2v_1v_2 - v_2^2] = kv_1v_2$$

Differential Summer Circuit:



$$v_{OS} = V_{DD}-v_{GS8}-v_{GS6}-V_{DD}+v_{GS5}+v_{GS7}$$

$$v_{OS} = v_{GS5}+v_{GS7}-v_{GS6}-v_{GS8}$$

But, $v_{ON5} = \sqrt{\frac{(W/L)_1}{(W/L)_2}}\, v_{ON1}$, $v_{ON7} = \sqrt{\frac{(W/L)_1}{(W/L)_2}}\, v_{ON3}$,

$v_{ON6} = \sqrt{\frac{(W/L)_1}{(W/L)_2}}\, v_{ON2}$ and $v_{ON8} = \sqrt{\frac{(W/L)_1}{(W/L)_2}}\, v_{ON4}$

$$v_{OS} = \sqrt{\frac{(W/L)_1}{(W/L)_2}}[(v_{GS1}-v_{GS2}) + (v_{GS3}-v_{GS4})]$$

$$\therefore \quad v_{OS} = \sqrt{\frac{(W/L)_1}{(W/L)_2}}(v_1 + v_2)$$

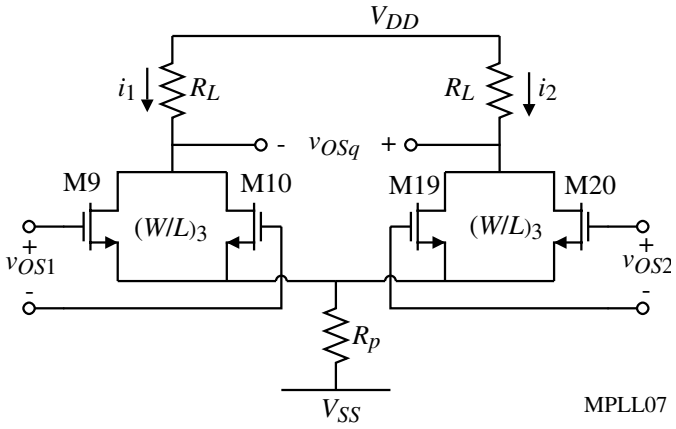
† J.S. Peña-Finol and J.A. Connelly, "A MOS Four-Quadrant Analog Multiplier Using the Quarter-Square Technique," *J. of Solid-State Circuits*, vol. SC-22, No. 6, pp. 1064-1073, Dec. 1987.

Quarter-Square Multiplier - Continued

Dual Differential Squaring Circuit:

$$v_{OSq} = V_{DD} - R_L i_2 - V_{DD} + R_L i_1$$
$$= -R_L[(i_{19}+i_{20}) - (i_9+i_{10})]$$

$$i_9+i_{10} = \left(\frac{K_p'}{2}\right)\left(\frac{W}{L}\right)_3[(V_{GS}+0.5v_{OS1}-V_T)^2]$$
$$+\left(\frac{K_p'}{2}\right)\left(\frac{W}{L}\right)_3(V_{GS}-0.5v_{OS1}-V_T)^2]$$
$$= K_p'\left(\frac{W}{L}\right)_3[(V_{GS}-V_T)^2+0.25v_{OS1}^2]$$



MPLL07

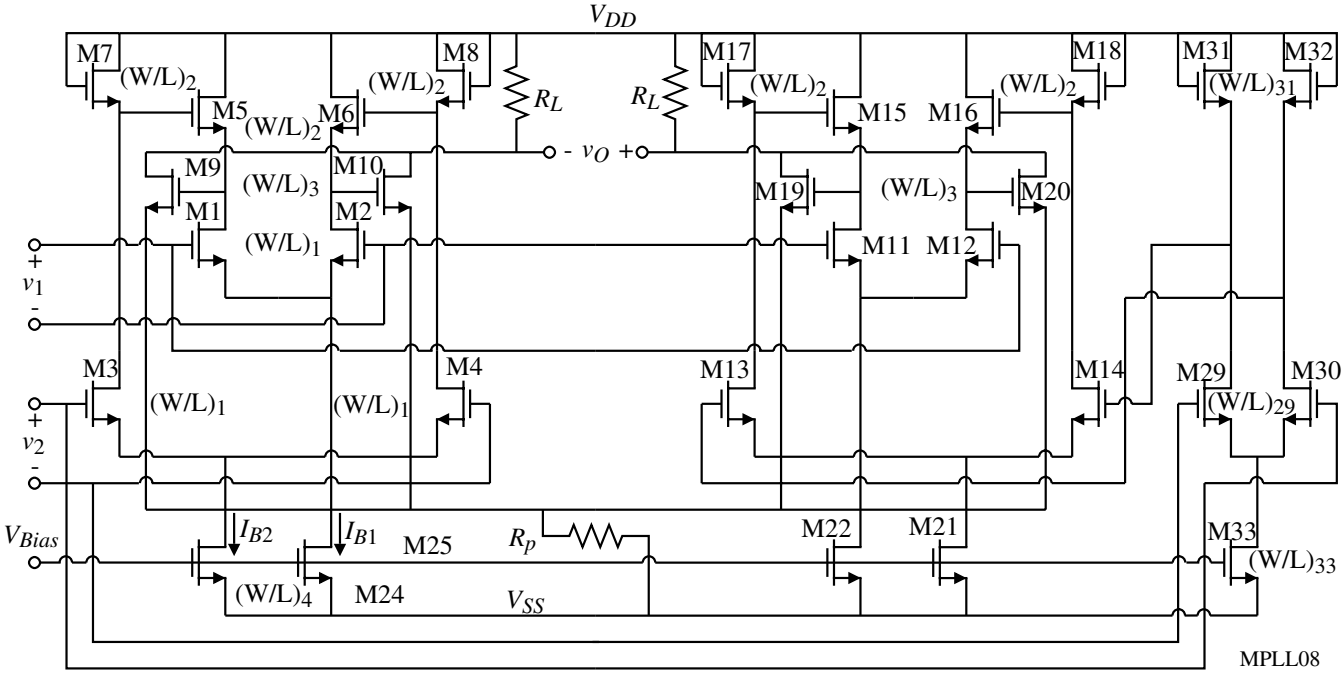
Similarly, $i_{19}+i_{20} = K_p'\left(\frac{W}{L}\right)_3 [(V_{GS}-V_T)^2+0.25v_{OS2}^2]$

$$\therefore\ v_{OSq} = R_L K_p'\left(\frac{W}{L}\right)_3[(V_{GS}-V_T)^2+0.25v_{OS1}^2 - (V_{GS}-V_T)^2-0.25v_{OS2}^2]$$
$$= R_L K_p'\left(\frac{W}{L}\right)_3[0.25(v_{OS1}^2 - v_{OS2}^2)$$

which is valid as long as $v_i << V_{ic}$ where V_{ic} is associated with the value of $\pm v_i$ when one of the transistors leaves the saturation region.

Quarter-Square Multiplier - Continued

Complete Circuit:



MPLL08

$$v_O = + K'R_L(W/L)_3 \frac{(W/L)_1}{(W/L)_2} v_1 v_2 = K'R_L S_3 \frac{S_1}{S_2} v_1 v_2 \quad \text{where } S_i = \frac{W_i}{L_i}$$

Four-Quadrant CMOS Multiplier[†]

Small Signal Analysis:

$i_{out} = i_7 - i_8 = (i_3+i_5)-(i_4+i_6) = (i_3-i_4)-(i_6-i_5)$

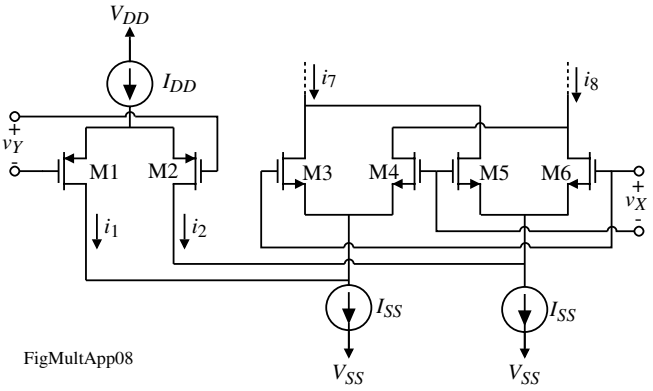
where

$$i_3 = \frac{g_{m34}v_x}{2}, \; i_4 = \frac{-g_{m34}v_x}{2},$$

$$i_6 = \frac{g_{m56}v_x}{2}, \text{ and } i_5 = \frac{-g_{m56}v_x}{2}$$

$$\therefore \; i_{out} = g_{m34}v_x - g_{m56}v_x$$

$$= \left(\sqrt{2K_NS_NI_{34}} - \sqrt{2K_NS_NI_{56}}\right) v_x$$



FigMultApp08

However, $I_{34} = I_{SS} - (0.5I_{DD}+i_1)$ and $I_{56} = I_{SS} - (0.5I_{DD}+i_2)$

If $I_{DD} = I_{SS}$ and $i_1 < I_{SS}$ and $i_2 < I_{SS}$, then $I_{34} = 0.5I_{SS}-i_1$ and $I_{56} = 0.5I_{SS} - i_2$

$$\therefore \; i_{out} = \sqrt{2K_NS_N}\left(\sqrt{I_{34}} - \sqrt{I_{56}}\right)v_x = \sqrt{2K_NS_N}\left(\sqrt{0.5I_{SS}-i_1} - \sqrt{0.5I_{SS} - i_2}\right)v_x$$

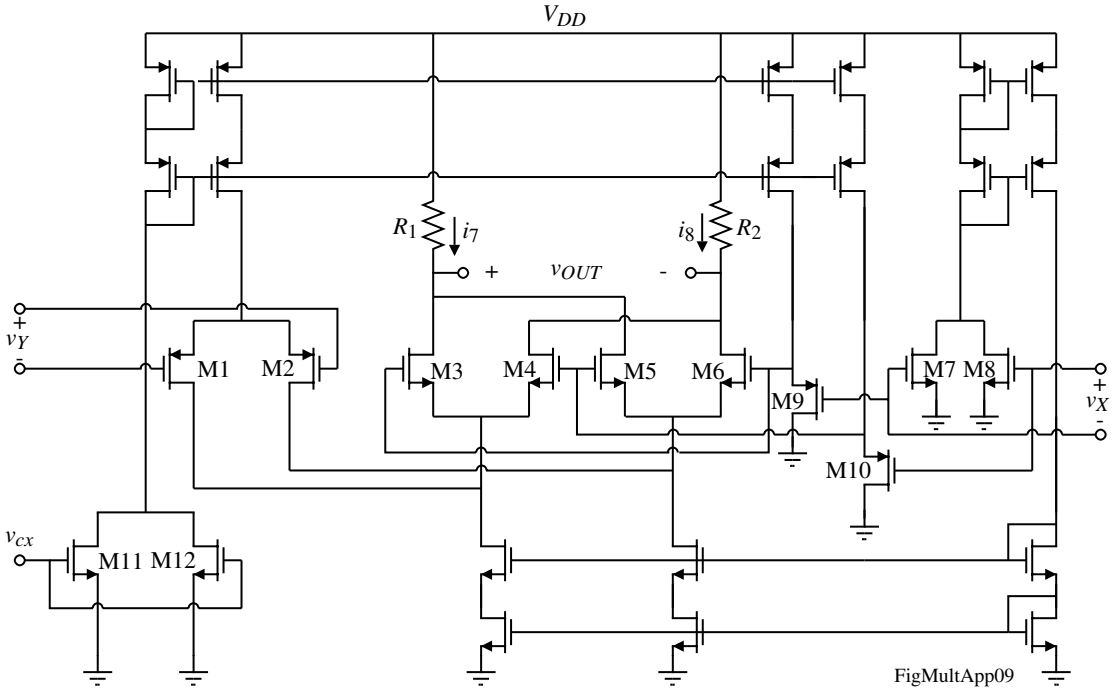
$$= \sqrt{K_NS_NI_{SS}}\left(\sqrt{1 -(2i_1/I_{SS})} - \sqrt{1 -(2i_2/I_{SS})}\right)v_x \approx \sqrt{K_NS_NI_{SS}}\,[(-i_1/I_{SS}) + (i_2/I_{SS})]v_x$$

$$i_{out} = \sqrt{\frac{K_NS_N}{I_{SS}}}(-i_1+i_2)v_x = \sqrt{\frac{K_NS_N}{I_{SS}}}\left(\frac{g_{m12}v_y}{2}+\frac{g_{m12}v_y}{2}\right)v_x = \sqrt{\frac{K_NS_N}{I_{SS}}}\,g_{m12}v_yv_x = \sqrt{2K_NS_NK_PS_P}v_xv_y$$

[†] Babanezhad and Temes - *JSSC*, Dec. 1985.

CMOS Four-Quadrant Multiplier

Complete circuit:



FigMultApp09

v_{CX} is a voltage used to establish the common mode in the multiplier.

CMOS Four Quadrant Multiplier

Uses FETs in the triode region to achieve a linear four-quadrant multiplier.

Ideal Operation (Op Amp Gain = ∞ and $v_i = 0$):

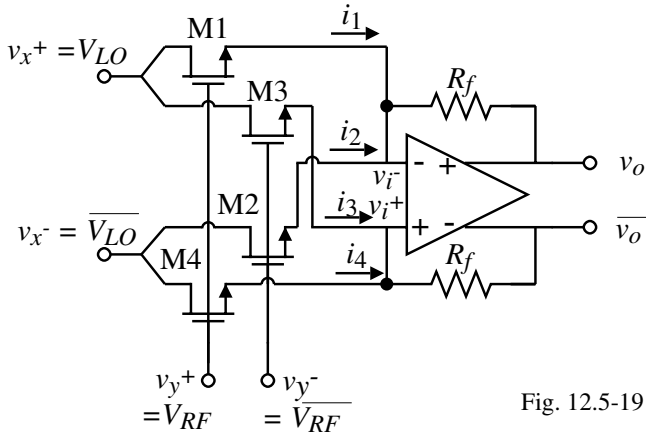


Fig. 12.5-19

$$i_1 = K'\left[\left(V_{GS} + \frac{v_y}{2} - V_T\right)\frac{v_x}{2} - \frac{1}{2}\left(\frac{v_x}{2}\right)^2\right]$$

$$i_2 = K'\left[\left(V_{GS} - \frac{v_y}{2} - V_T\right)\left(\frac{-v_x}{2}\right) - \frac{1}{2}\left(\frac{-v_x}{2}\right)^2\right]$$

$$i_3 = K'\left[\left(V_{GS} - \frac{v_y}{2} - V_T\right)\frac{v_x}{2} - \frac{1}{2}\left(\frac{v_x}{2}\right)^2\right]$$

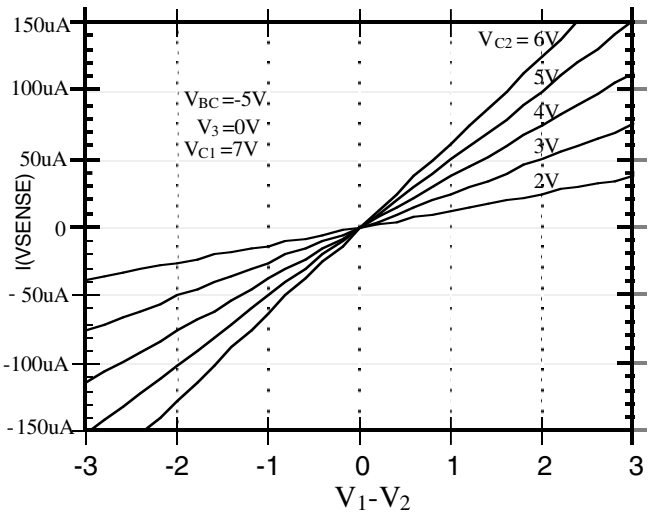
$$i_4 = K'\left[\left(V_{GS} + \frac{v_y}{2} - V_T\right)\left(\frac{-v_x}{2}\right) - \frac{1}{2}\left(\frac{-v_x}{2}\right)^2\right]$$

$$v_o = R(v_o^+ - v_o^-) = RK'(-i_4 - i_3 + i_1 + i_2) = RK'\left(\frac{v_x v_y}{2} + \frac{v_x v_y}{2}\right) = RK' v_x v_y$$

$$\therefore \quad \boxed{v_o = RK' v_{LO} v_{RF} = G_T v_{LO} v_{RF}}$$

where the gain, $G_T = RK'$

CMOS Four-Quadrant Multiplier - Performance



SPICE Input File:

```
Double MOSFET Differential Resistor Realization
M1 1 2 3 4 MNMOS1 W=3U L=3U
M2 1 5 8 4 MNMOS1 W=3U L=3U
M3 6 5 3 4 MNMOS1 W=3U L=3U
M4 6 2 8 4 MNMOS1 W=3U L=3U
VSENSE 3 8 DC 0
VC1 2 0 DC 7V
VC2 5 0
VSS 4 0 DC -5V
V12 1 6
.MODEL MNMOS1 NMOS VTO=0.75 KP=25U
+LAMBDA=0.01 GAMMA=0.8 PHI=0.6
.DC V12 -3 3 0.2 VC2 2 6 1
.PRINT DC I(VSENSE))
.PROBE
.END
```

Comments:

- Good linearity and tunability.
- Frequency range limited by the op amp

CMOS Four Quadrant Multiplier - Continued

Previous circuit with a finite op amp gain (A):

$$v_o = v_o^+ - v_o^- = A\,(v_i^+ - v_i^-) \quad \Rightarrow \quad v_i^+ = \frac{v_o}{2A} \text{ and } v_i^- = \frac{-v_o}{2A}$$

$$i_1 = K'\left[\left(V_{GS} + \frac{v_y}{2} - \frac{v_o}{2A} - V_T\right)\left(\frac{v_x}{2} - \frac{v_o}{2A}\right) - \frac{1}{2}\left(\frac{v_x}{2} - \frac{v_o}{2A}\right)^2\right]$$

$$i_2 = K'\left[\left(V_{GS} - \frac{v_y}{2} - \frac{v_o}{2A} - V_T\right)\left(-\frac{v_x}{2} - \frac{v_o}{2A}\right) - \frac{1}{2}\left(\frac{v_x}{2} + \frac{v_o}{2A}\right)^2\right]$$

$$i_3 = K'\left[\left(V_{GS} - \frac{v_y}{2} + \frac{v_o}{2A} - V_T\right)\left(\frac{v_x}{2} + \frac{v_o}{2A}\right) - \frac{1}{2}\left(\frac{v_x}{2} + \frac{v_o}{2A}\right)^2\right]$$

$$i_4 = K'\left[\left(V_{GS} + \frac{v_y}{2} + \frac{v_o}{2A} - V_T\right)\left(-\frac{v_x}{2} + \frac{v_o}{2A}\right) - \frac{1}{2}\left(-\frac{v_x}{2} + \frac{v_o}{2A}\right)^2\right]$$

$$v_o = \frac{R}{1 + \frac{1}{A}}(-i_4 - i_3 + i_1 + i_2) = \frac{RK'}{1 + \frac{1}{A}}\left[\frac{v_x v_y}{2} + \frac{V_T v_o}{A} - \frac{V_{GS} v_o}{A} + \frac{v_x v_y}{2} - \frac{V_{GS} v_o}{A} + \frac{V_T v_o}{A}\right]$$

$$v_o\left[\left(1 + \frac{1}{A}\right)\frac{2RK'}{A}(V_{GS} - V_T)\right] = RK' v_x v_y \qquad \therefore \qquad \boxed{v_o = \frac{G_T}{1 + \frac{1}{A} + \frac{2G_T}{A}(V_{GS} - V_T)} v_x v_y}$$

CMOS Four Quadrant Multiplier - Continued

Previous circuit with a finite op amp gain (A) and a threshold variation (ΔV_T^+ and ΔV_T^-):

$$i_1 = K'\left[\left(V_{GS} + \frac{v_y}{2} - \frac{v_o}{2A} - V_T - \Delta V_T^+\right)\left(\frac{v_x}{2} - \frac{v_o}{2A}\right) - \frac{1}{2}\left(\frac{v_x}{2} - \frac{v_o}{2A}\right)^2\right]$$

$$i_2 = K'\left[\left(V_{GS} - \frac{v_y}{2} - \frac{v_o}{2A} - V_T - \Delta V_T^+\right)\left(-\frac{v_x}{2} - \frac{v_o}{2A}\right) - \frac{1}{2}\left(\frac{v_x}{2} + \frac{v_o}{2A}\right)^2\right]$$

$$i_3 = K'\left[\left(V_{GS} - \frac{v_y}{2} + \frac{v_o}{2A} - V_T - \Delta V_T^-\right)\left(\frac{v_x}{2} + \frac{v_o}{2A}\right) - \frac{1}{2}\left(\frac{v_x}{2} + \frac{v_o}{2A}\right)^2\right]$$

$$i_4 = K'\left[\left(V_{GS} + \frac{v_y}{2} + \frac{v_o}{2A} - V_T - \Delta V_T^-\right)\left(-\frac{v_x}{2} + \frac{v_o}{2A}\right) - \frac{1}{2}\left(-\frac{v_x}{2} + \frac{v_o}{2A}\right)^2\right]$$

$$v_o = \frac{R}{1 + (1/A)}(-i_4 - i_3 + i_1 + i_2)$$

$$= \frac{RK'}{1 + (1/A)}\left[\frac{v_x v_y}{2} + \frac{\Delta V_T^+ v_o^\circ}{A} + \frac{V_T v_o}{A} + \frac{v_o^2}{2A^2} - \frac{V_{GS} v_o}{A} + \frac{v_x v_y}{2} + \frac{\Delta V_T^- v_o}{A} + \frac{V_T v_o}{A} - \frac{v_o^2}{2A^2} - \frac{V_{GS} v_o}{A}\right]$$

$$v_o = \frac{G_T}{1 + (1/A)}\left[v_x v_y - \frac{2v_o}{A}(V_{GS} - V_T) + \frac{v_o}{A}(\Delta V_T^+ + \Delta V_T^-)\right]$$

$$\therefore \qquad \boxed{v_o = \frac{G_T}{\left(1 + \frac{1}{A}\right)\left[1 + \frac{2G_T}{1 + A}(V_{GS} - V_T) - \frac{G_T}{1 + A}(\Delta V_T^+ + \Delta V_T^-)\right]} v_x v_y}$$

CMOS Multiplier - 4 FET Switch Plus Inverter

Circuit:

- V-I converter based on CMOS inverter
- LO commutates four-FET switch to mix with the RF current
- Linearity limited by V-I converter
- Noise set by V-I converter

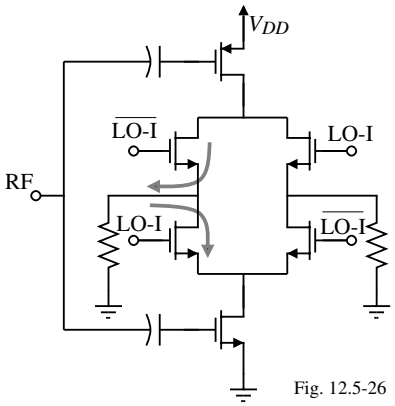


Fig. 12.5-26

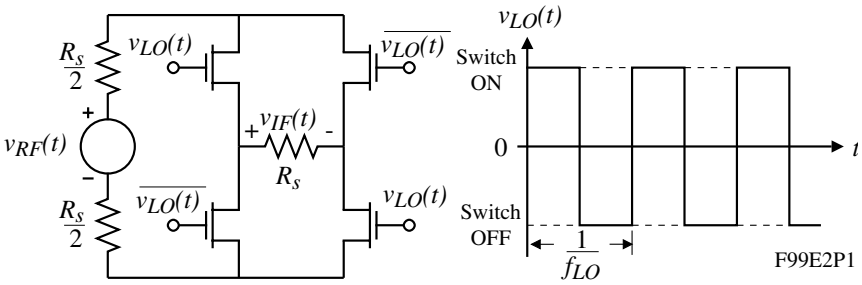
Performance:

- Implemented for a 900 MHz RF, 100 MHz IF superheterodyne receiver
- Image noise suppression filter is required between the LNA and mixer to satisfy the matched input impedance requirement at the mixer.

Specification	Value
Conversion Gain	9 dB
DSB Noise Figure	6.7 dB
IIP3	-4 dBm
LO level	0 dBm
Current Drain	2.6 mA at 2.7V
Technology	0.5 μm CMOS

Passive Mixer Example

A simple, doubly balanced passive CMOS down-conversion mixer is shown along with the local oscillator waveform, $v_{OL}(t)$. Assume that $v_{RF}(t) = A_{RF}cos(\omega_{RF}t)$ and $v_{LO}(t)$ is shown below. (a.) Find the conversion gain, G_c, in dB if the switches are ideal. (b.) Find the conversion gain in dB if the switches have an ON resistance of $R_s/2$.



Solution

Assume the switches have an ON resistance of R_{ON} and work both parts (a) and (b) simultaneously. Also, The equation for $v_{IF}(t)$ can be written as,

$$v_{IF}(t) = \left(\frac{R_s}{2R_s+2R_{ON}}\right)v_{RF}(t) \cdot \text{sgn}[v_{LO}(t)]$$

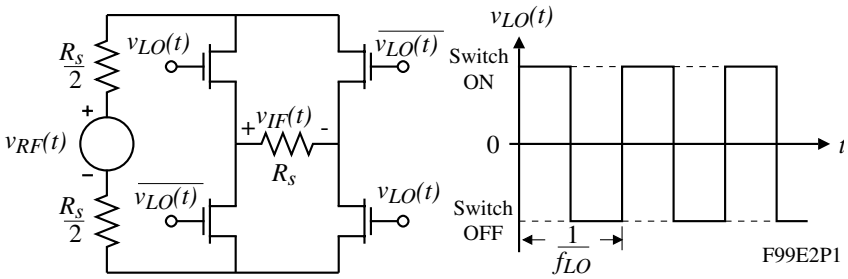
$$V_{IF}(j\omega) = \left(\frac{R_s}{2R_s+2R_{ON}}\right)A_{RF}cos(\omega_{RF}t) \cdot \left[\frac{4}{\pi}cos(\omega_{LO}t) + \frac{4}{3\pi}cos\,(3\omega_{LO}t) + \cdots\right]$$

$$\therefore \quad V_{IF}(j\omega) \approx \left(\frac{R_s}{2R_s+2R_{ON}}\right)\frac{4A_{RF}}{\pi}\,cos(\omega_{RF}t) \cdot cos(\omega_{LO}t) = \left(\frac{R_s}{2R_s+2R_{ON}}\right)\frac{2A_{RF}}{\pi}\,cos[\omega_{RF}-\omega_{LO})t]$$

Passive Mixer Example - Continued

The conversion gain in general is written as

$$G_c = \frac{|V_{IF}|}{|V_{RF}|} = \left(\frac{R_s}{2R_s+2R_{ON}}\right)\frac{2}{\pi}$$

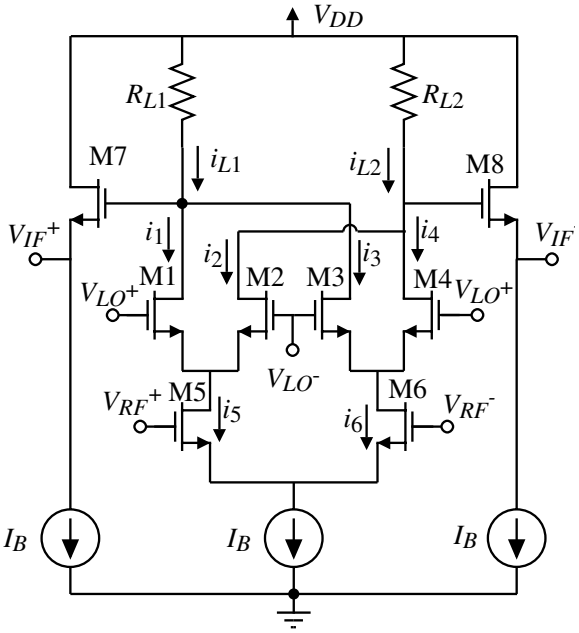


(a.) For $R_{ON} = 0$, $G_c = \frac{1}{\pi}$ → $\boxed{G_c = \frac{1}{\pi} = -9.943\text{dB}}$

(b.) For $R_{ON} = 0.5R_s$, $G_c = \frac{2}{3\pi}$ → $\boxed{G_c = \frac{2}{3\pi} = -13.465\text{dB}}$

A 1.8V, 1.9GHz CMOS Multiplier†

This mixer uses a stacked Gilbert cell as shown.



Performance for RF = 1.9GHz and IF = 250MHz:

Supply Voltage	1.8V	2.1	3.0
LO Power (1.65GHz)	-8dBm	-8dBm	-8dBm
SSB NF (50Ω)	10.2dB	9.4dB	8.2dB
Conversion Gain	0.5dB	2.4dB	6.5dB
IIP3	-6dBm	-5.5dBm	-3dBm
Input -1dB Compression	-15dBm	-14.5dBm	-12dBm
Total Current	4.8mA	5.8mA	13.1mA

† P.J. Sullivan, B.A. Xavier and W.H. Ku, "Low Voltage Performance of a Microwave CMOS Gilbert Cell Mixer," *IEEE J. of Solid-State Circuits*, Vol. 32, No. 7, July 1997, pp. 1151-1155.

DIGITAL DETECTORS

Conventional Phase Frequency Detector[†]

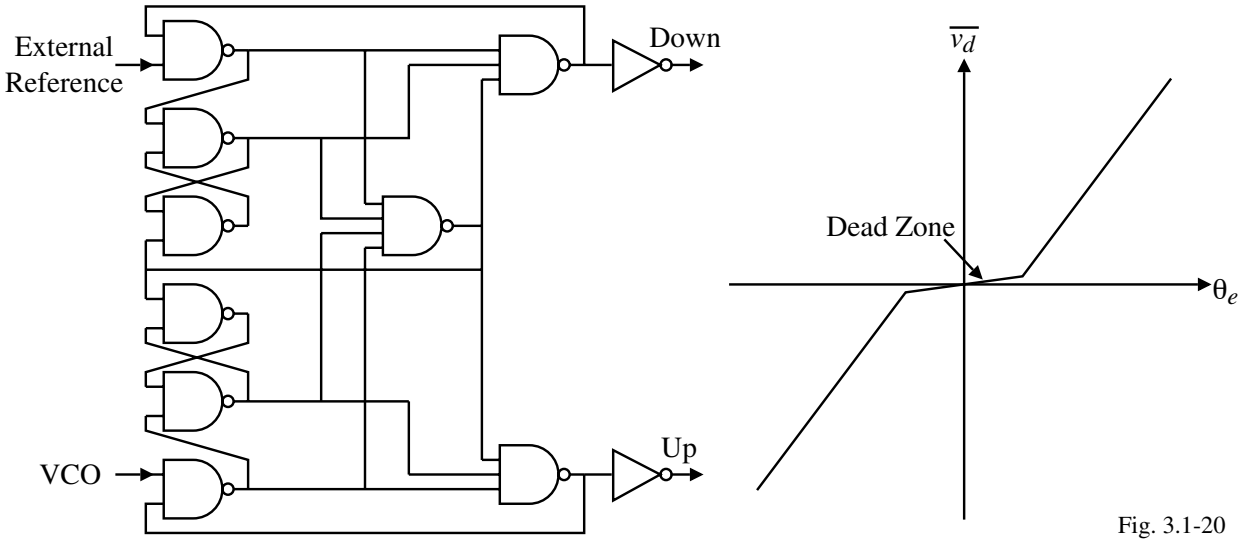


Fig. 3.1-20

The primary problem with the conventional PFD is the dead zone which causes phase jitter.

[†] N. H. E. Weste and K. Eshragrian, *Principles of CMOS VLSI Design*, 2nd. ed., Reading, MA, Addison Wesley, 1993 also see B.D Muer and M. Steyaert, *CMOS Fractional-N Synthesizers-Design for High Spectral Purity and Monolithic Integration*, Kluwer Academic Publishers, Norwell, MA, 2003.

Delay in the Conventional PFD

The PFD is an asynchronous state machine. The circuit speed depends on the delay time necessary to reset all internal nodes. The critical path is shown below in bold and consists of 6 gate delays.

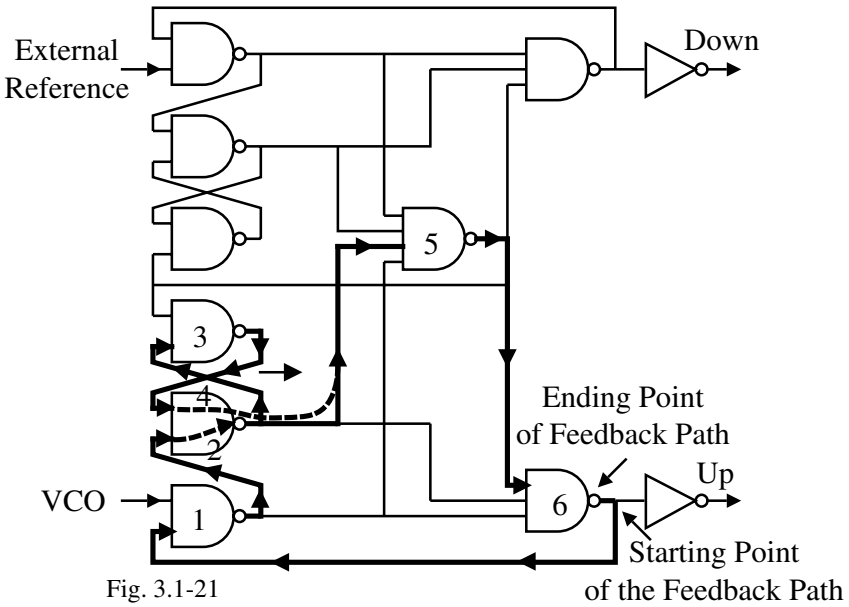


Fig. 3.1-21

Precharge PFD†

The critical path has a delay of only three gates reducing the dead zone and resulting phase jitter.

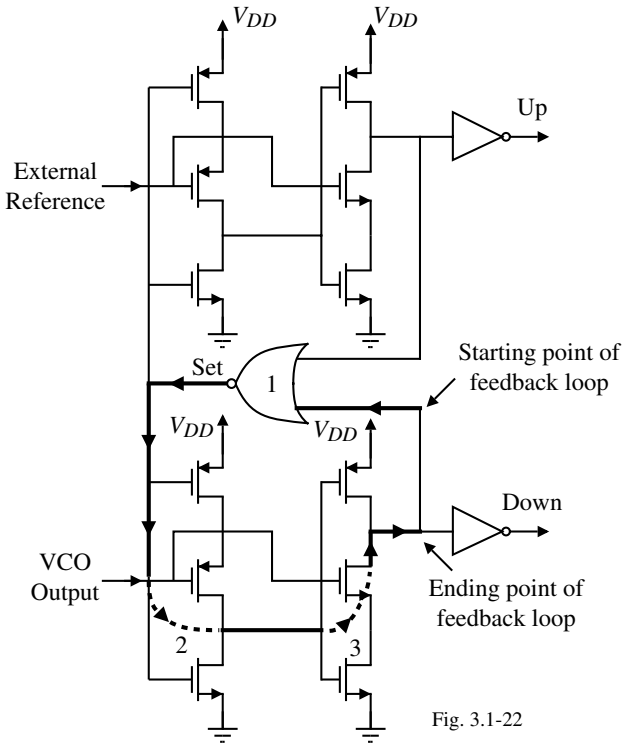


Fig. 3.1-22

† S. Kim, et. al., "A 960-Mb/s/pin Interface for Skew-Tolerant Bus Using Low Jitter PLL, *IEEE J. of Solid-State Circuits*, Vol. 32, No. 5, may 1997, pp. 691-700.

Modified Precharge PFD†

Circuit:

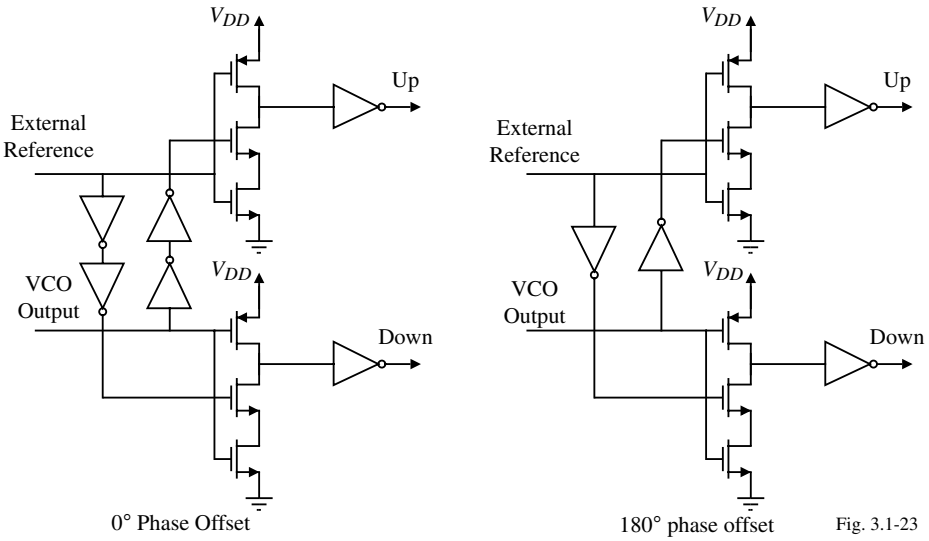


Fig. 3.1-23

The two delays inserted at the external reference and the VCO output remove the dead zone in the phase characteristic around the equilibrium point of the phase detector.

† H. O. Johansson, "A Simple Precharged CMOS Phase Fequency Detector," *IEEE J. of Solid-State Circuits*, Vol. 33, No. 2, Feb. 1998, pp. 295-299.

Comparison of Various PFD's

V_{DD} = 3V and f_o = 50MHz

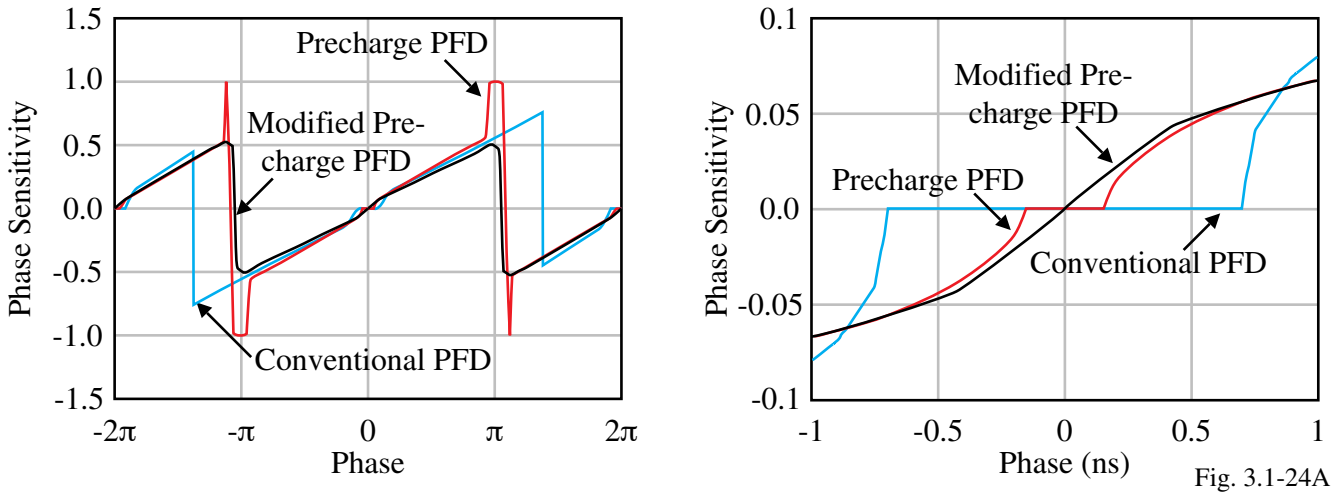


Fig. 3.1-24A

The duty cycle of the input will influence the dead-zone of the PFD including the modified PFD. For example, a duty cycle of 5% at 50 MHz gives a phase offset of 0.063π or 630ps.

Frequency Response of Various PFDs

The maximum operation frequency is defined as the frequency where the size of the dead zone starts to deviate significantly from the low-frequency value.

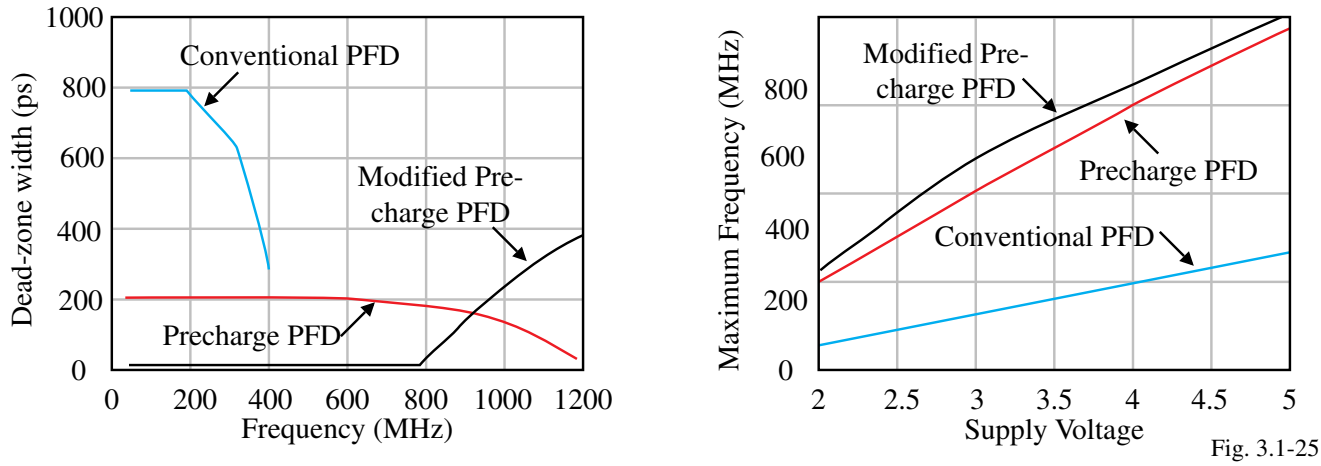


Fig. 3.1-25

SUMMARY

Analog Multipliers:

- 1-, 2-, and 4-quadrant
- Modulator - output voltage is the product of arbitrary functions of the inputs
- Multiplier - output voltage is a linear product of the inputs
- BJT multipliers - Gilbert Cell
- MOS multipliers - quarter-square principle, translinear principle
- The linearity of the multipliers can be increased by various methods.

Digital Detectors:

- The EXOR and JK phase detectors are reasonably simple and straightforward
- The primary objective of the phase frequency detector is to eliminate the dead zone
- Techniques for reducing the dead zone
  - Precharge PFD
  - Modified Precharge PFD