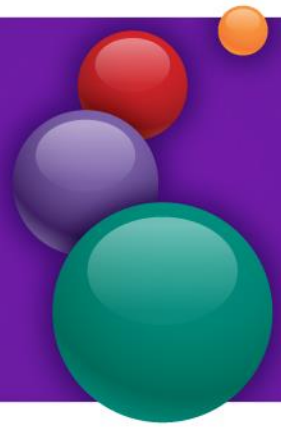
MIPI Alliance Introduction
&
MIPI Camera Serial Interface Overview

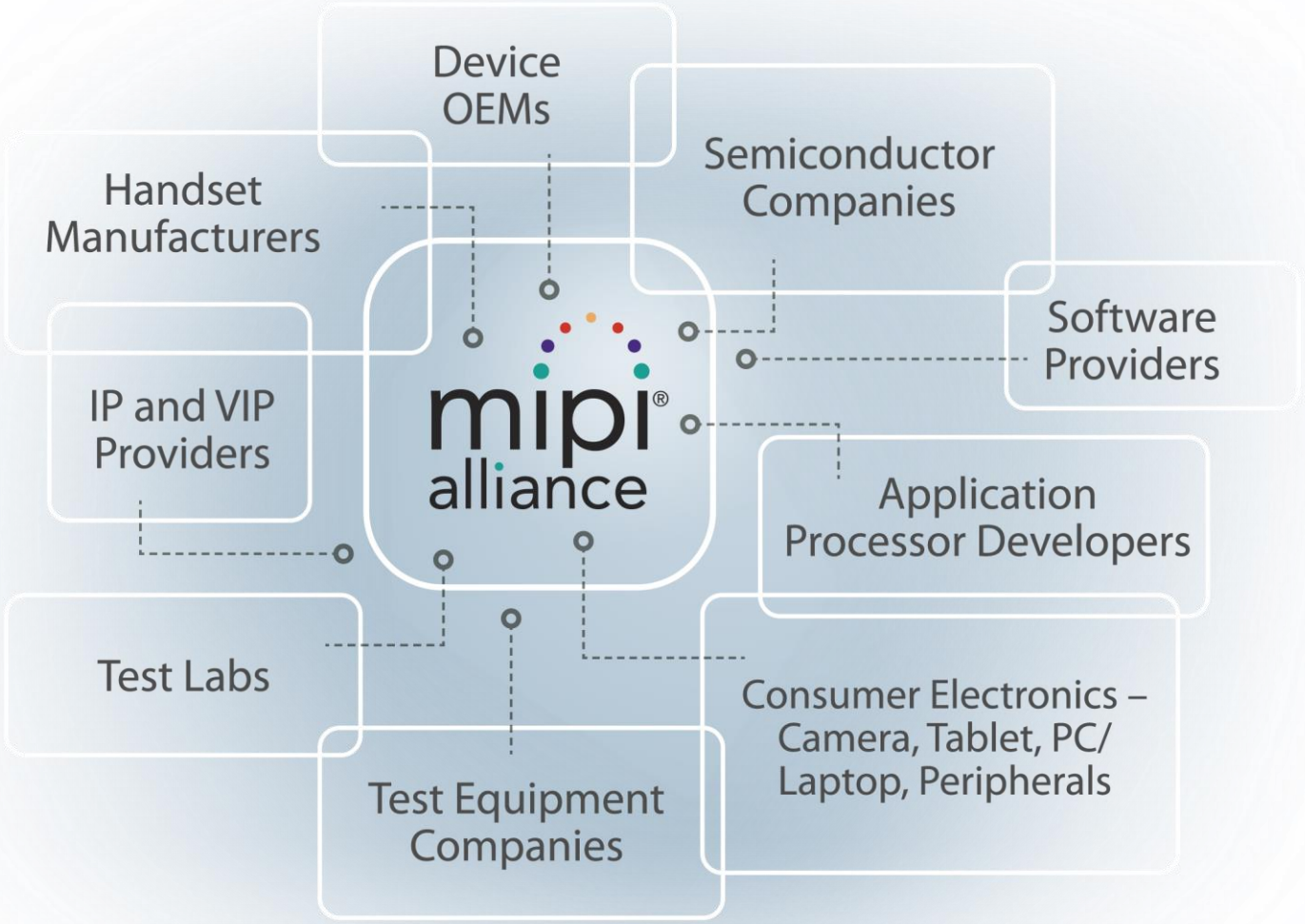


Haran Thanigasalam
Vice Chair, MIPI Camera Working Group

About MIPI Alliance

- 260 Members (as of 4 May 2015)
- 45+ specifications and supporting docs
- We drive **mobile** and **mobile-influenced interface** technology through the development of hardware and software **specifications**
- We work **globally** and **collaboratively** with other standards bodies to **benefit the mobile ecosystem**

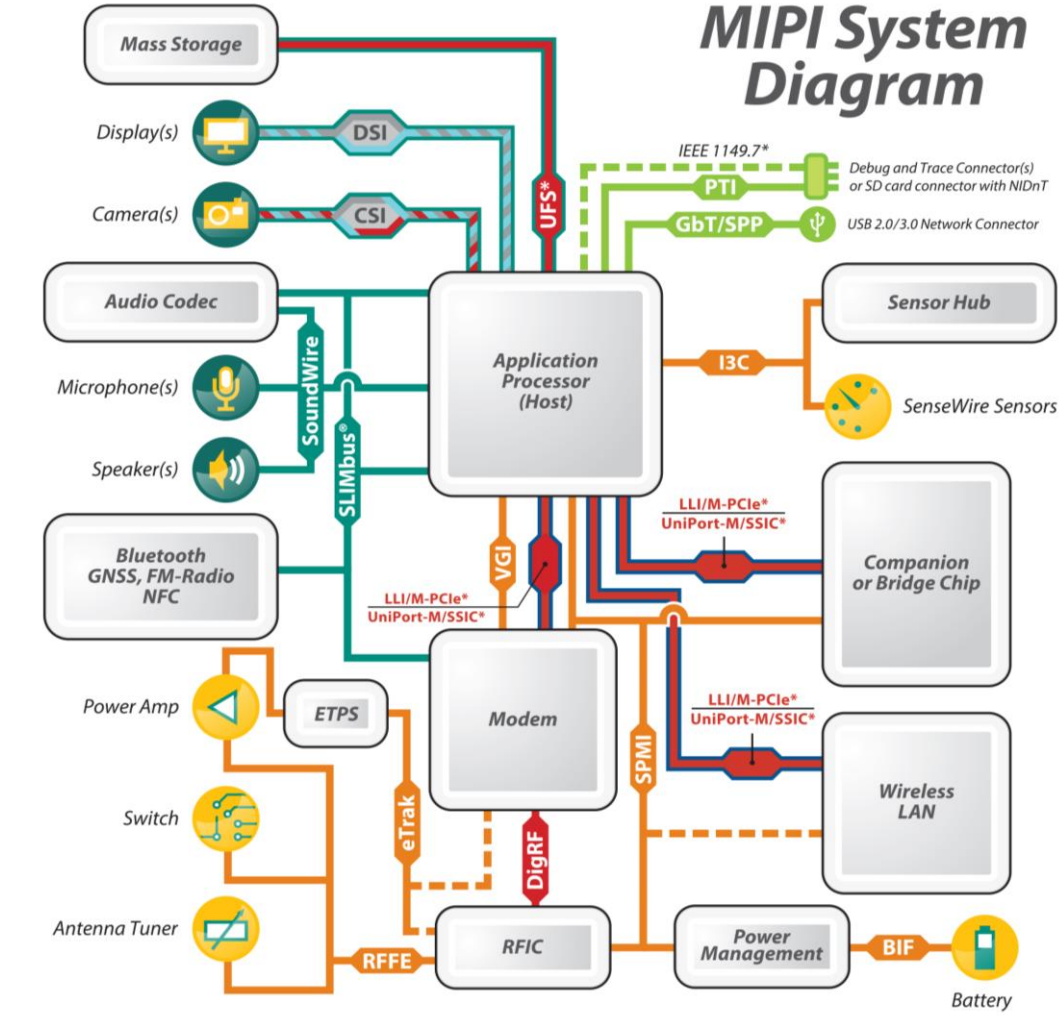
MIPI Alliance Member Ecosystem

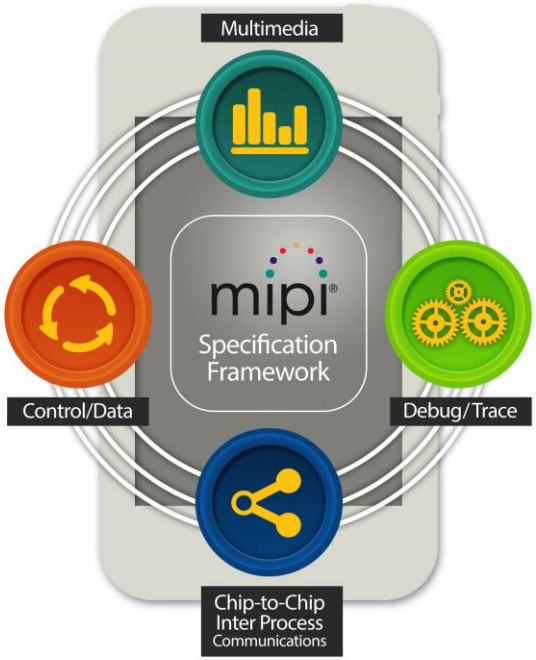


Active MIPI Alliance Working Groups

- Analog Control Interface
- Battery Interface
- Camera
- Debug
- Display
- Low Latency Interface
- Low Speed Multipoint Link (New - SoundWire℠)
- Marketing
- PHY (C / D / M)
- Reduced Input Output (RIO) (New)
- RF Front-End (RFFE℠)
- Sensor / I3C℠ (New)
- Software (New)
- Technical Steering Group
- Test
- UniPro℠

MIPI System Diagram





mipi alliance

* The UFS (Universal Flash Storage) specification from JEDEC, the SSIC (SuperSpeed Inter Chip) specification from USB-IF, and the M-PCIe (Mobile PCI Express®) specification from PCI-SIG® all use the MIPI M-PHY® physical layer.

* UFS (Universal Flash Storage) specification is available from JEDEC and uses the MIPI UniPort-M.

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Recent Announcements

- 18 February 2015 - MIPI Alliance Updates its Widely Adopted CSI Specification to Bring High-Resolution Imaging, Richer Color and Video to Mobile and Mobile-Influenced Applications

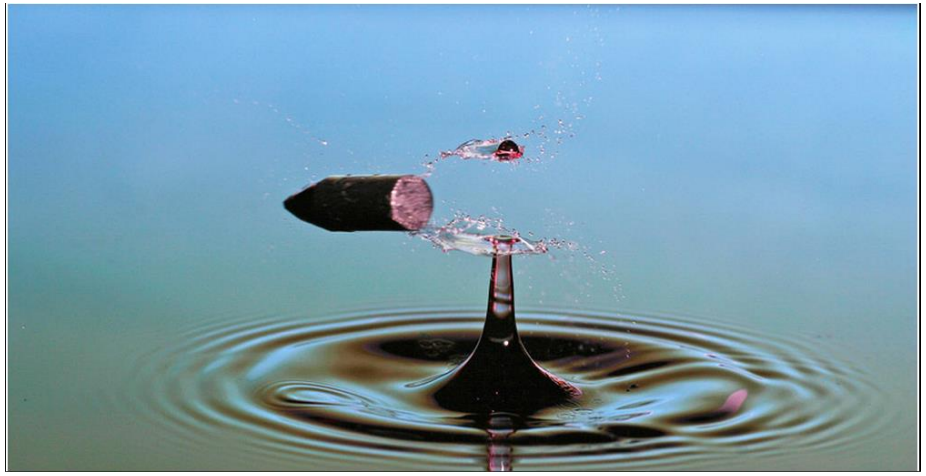
- 12 March 2015 - MIPI Alliance Updates its MIPI RFFE Interface for Mobile Device RF Front-End Architectures

The Future of MIPI – Beyond Mobile

- Mobile influences **everything**
  - Automotive
  - IoT
  - Wearables
- Everything gets faster, smaller and lower power
  - MIPI will continue to evolve specs to take advantage of the evolution of technology in mobile devices

Evolution of imaging on mobile products

- Trend 1 - Performance imaging to match compact camera / SLR capabilities:
  - MP
  - FPS
  - BPP
- Trend 2 – Capturing beyond visible spectrum (400nm – 700 nm)
- Forward-looking imaging use cases:
  - Always On Imaging
  - Always Aware
  - Thermal / IR
  - Low-light / Night Capture
  - Medical
  - Security
- Form Factors:
  - Monolithic, Wearable, Tablets, Automotive



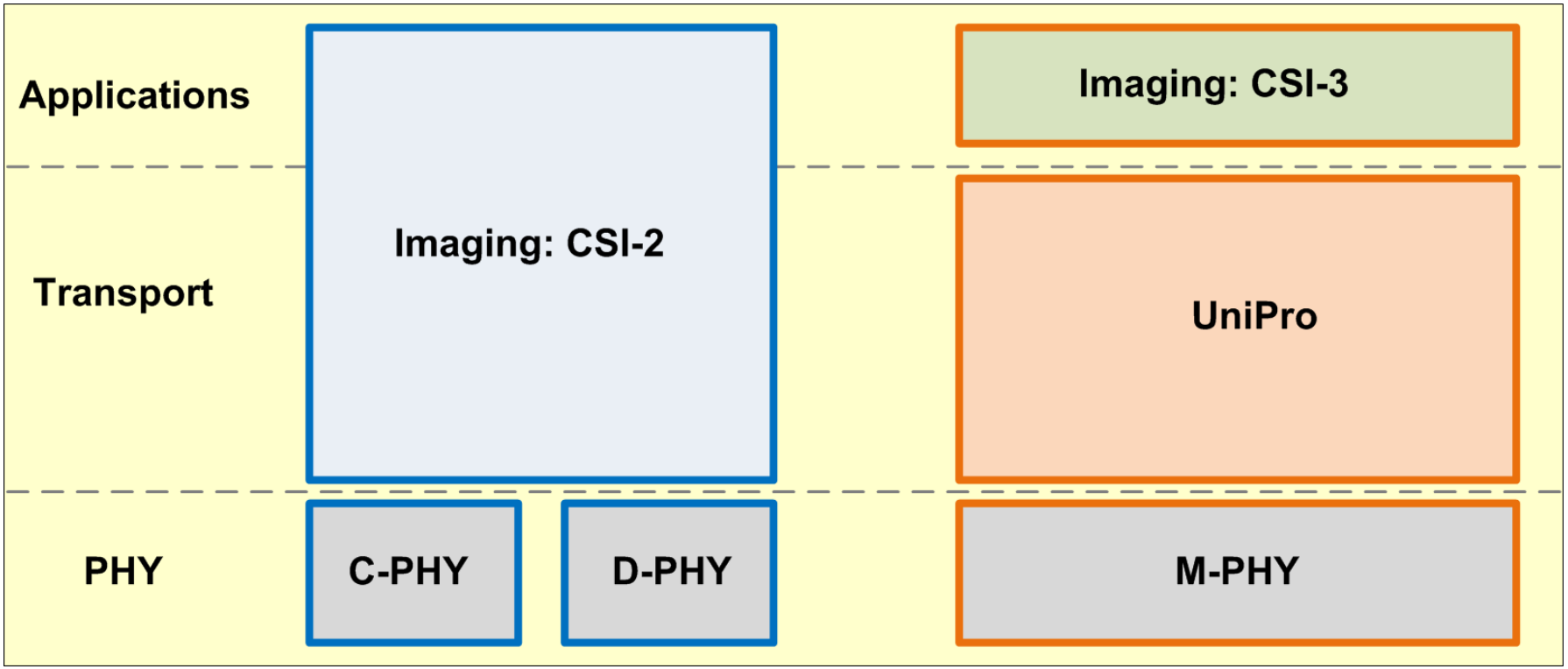
SLR Example

Credit: Lex Augusteijn

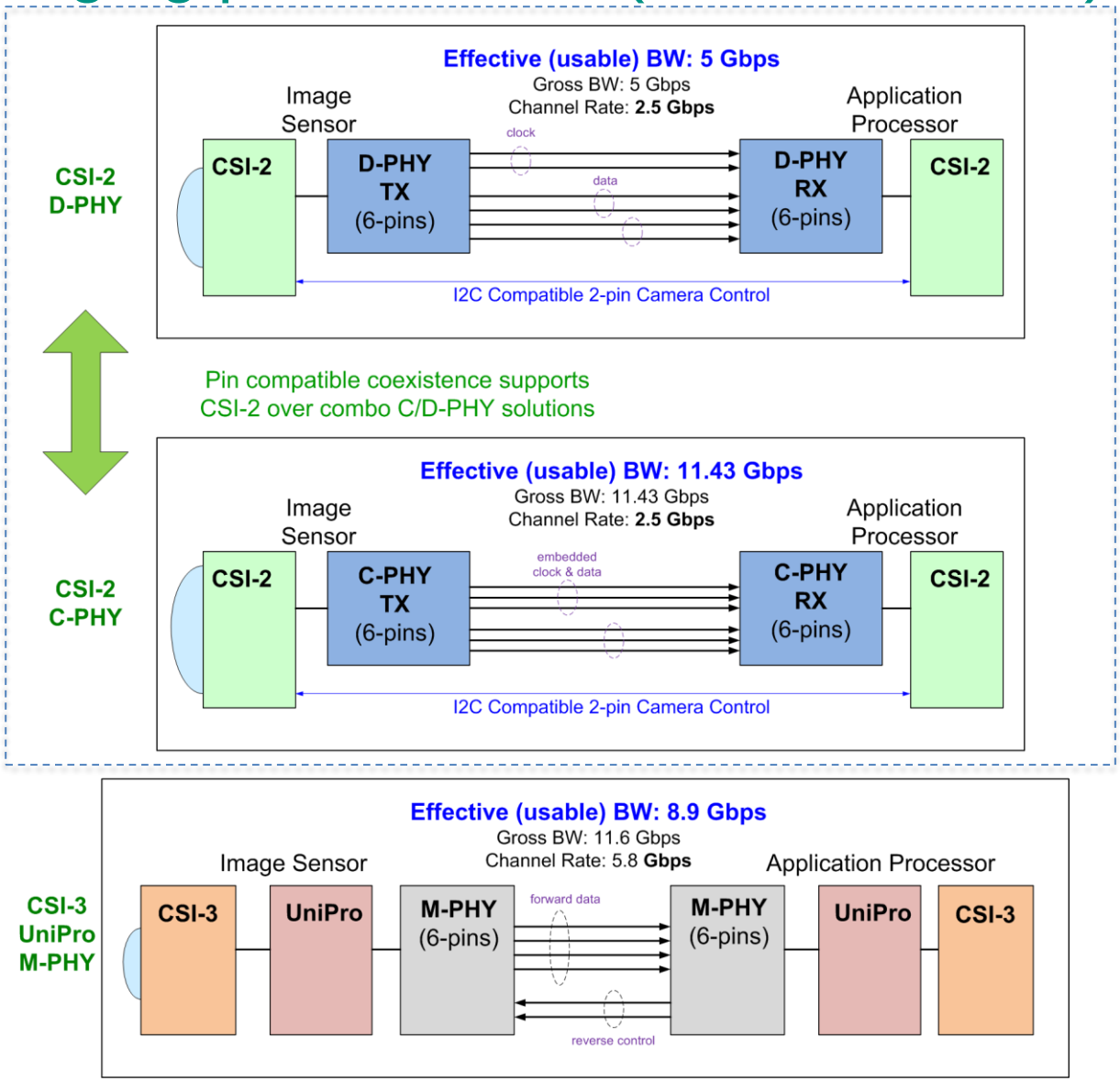
Two Highly Capable Imaging Architectures

CSI-2 protocol contains transport and application layers, and natively supports **D-PHY & C-PHY**

CSI-3 application stack connects to **UniPro** transport layer, which in turns bolts onto **M-PHY**



Imaging performance (MP, FPS, BPP)

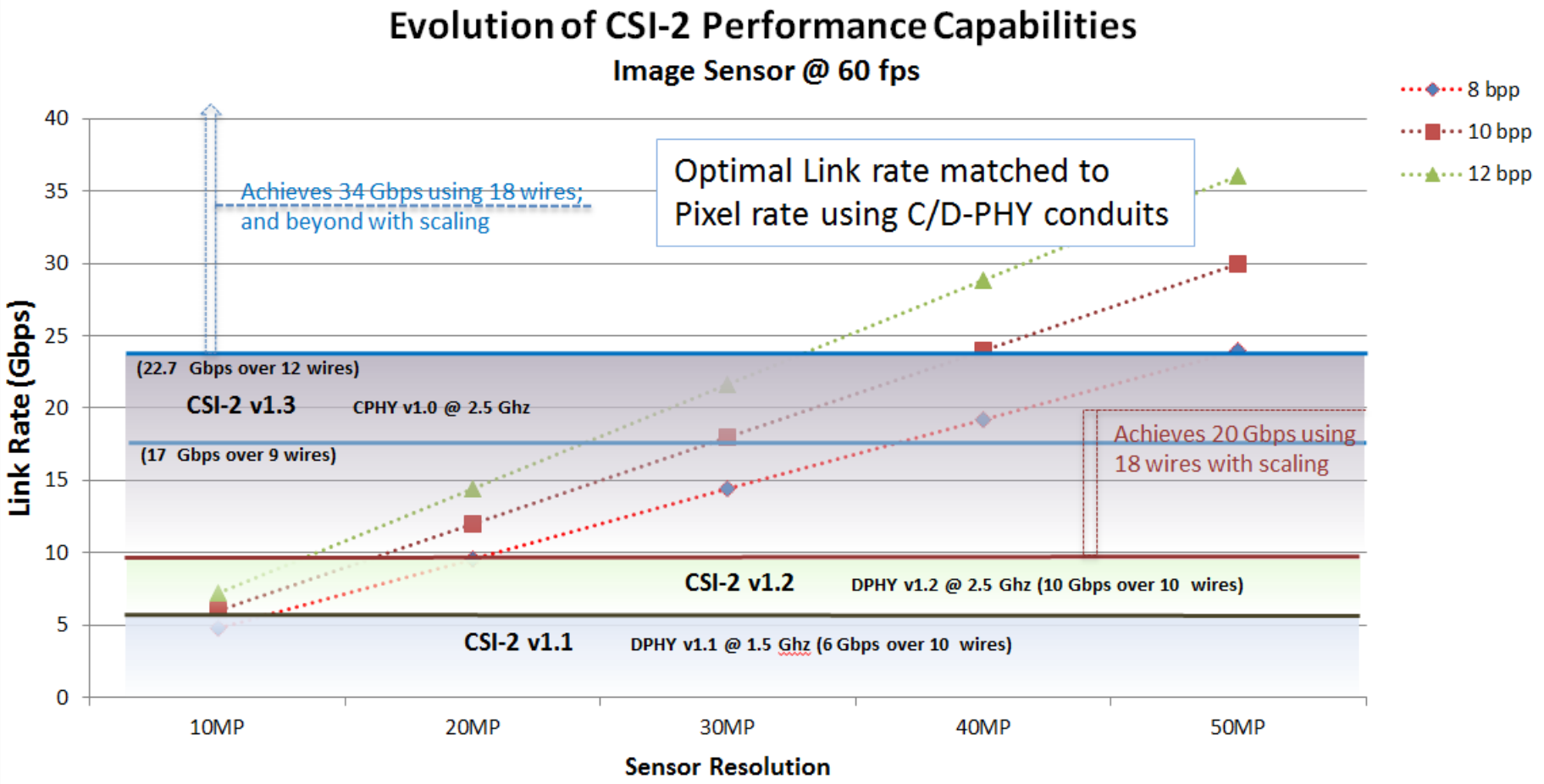


Popular Imaging Format

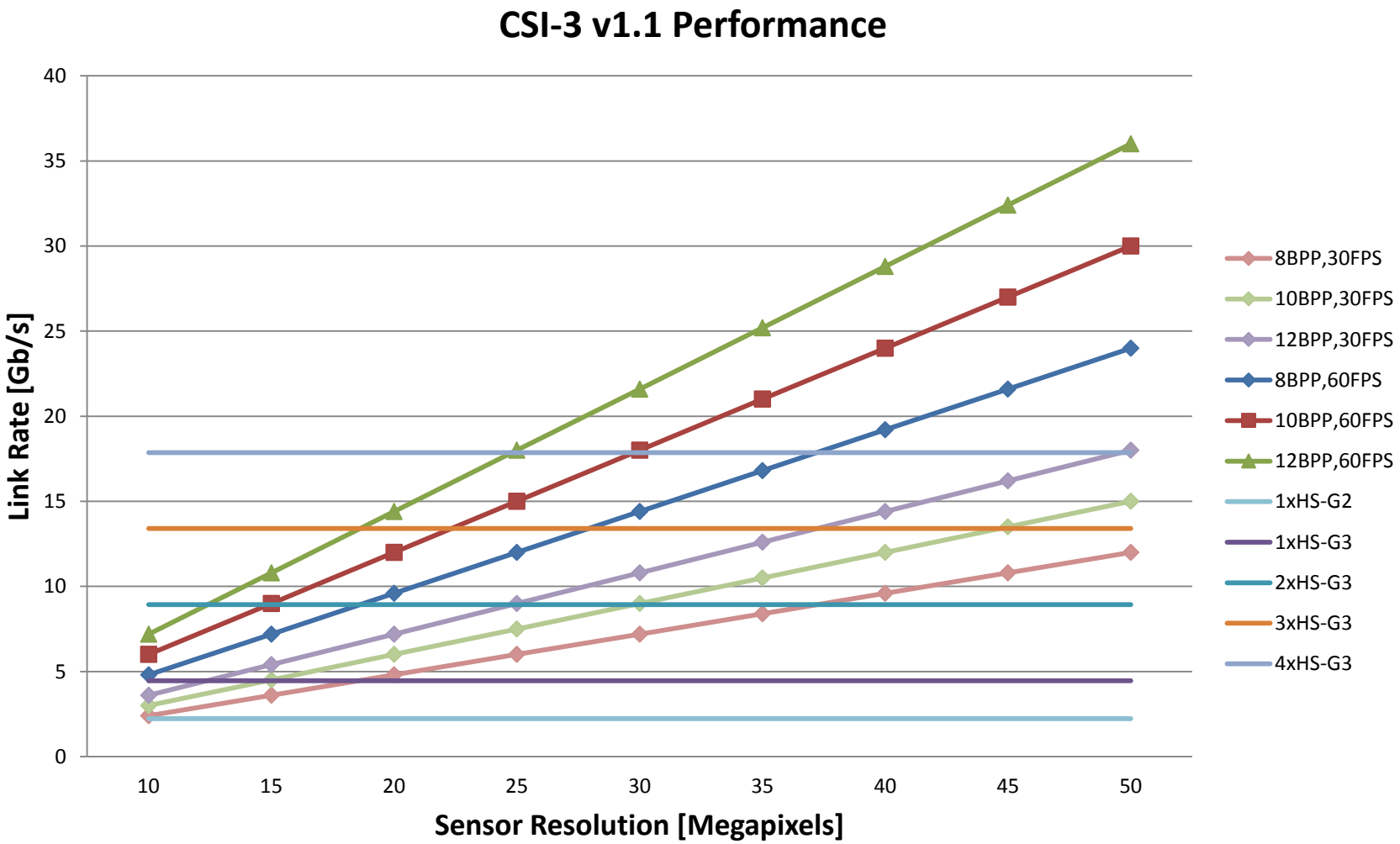
4K @ 30 fps and 12 BPP					
Required MIPI Specs (IPs)	**PHY pins**	**Channel rate**	**Required BW**	**Variable link rate**	**Control Interface**
[CSI-2] [D-PHY]	**6**	**1.78 Gbps**	3.56 Gbps	Yes	I2C
[CSI-2] [C-PHY]	**3**	**1.55 Gsps**	3.56 Gbps	Yes	I2C
[CSI-3] [UniPro] [M-PHY]	**4**	**5.0 Gbps**	3.56 Gbps	No	In-band

- I2C control interface requires 2 GPIO pins and widely used in camera subsystems (VCM), and used to integrate imaging solutions with a wide array of (MEMS, ALS, IR, Gyro, Presence, Accelerometer) sensors on mobile platforms (p8)

CSI-2 v1.3 over C/D-PHY (Adopted Specs)



CSI-3 over UniPro & M-PHY (Adopted Specs)



Adopted CSI Specs

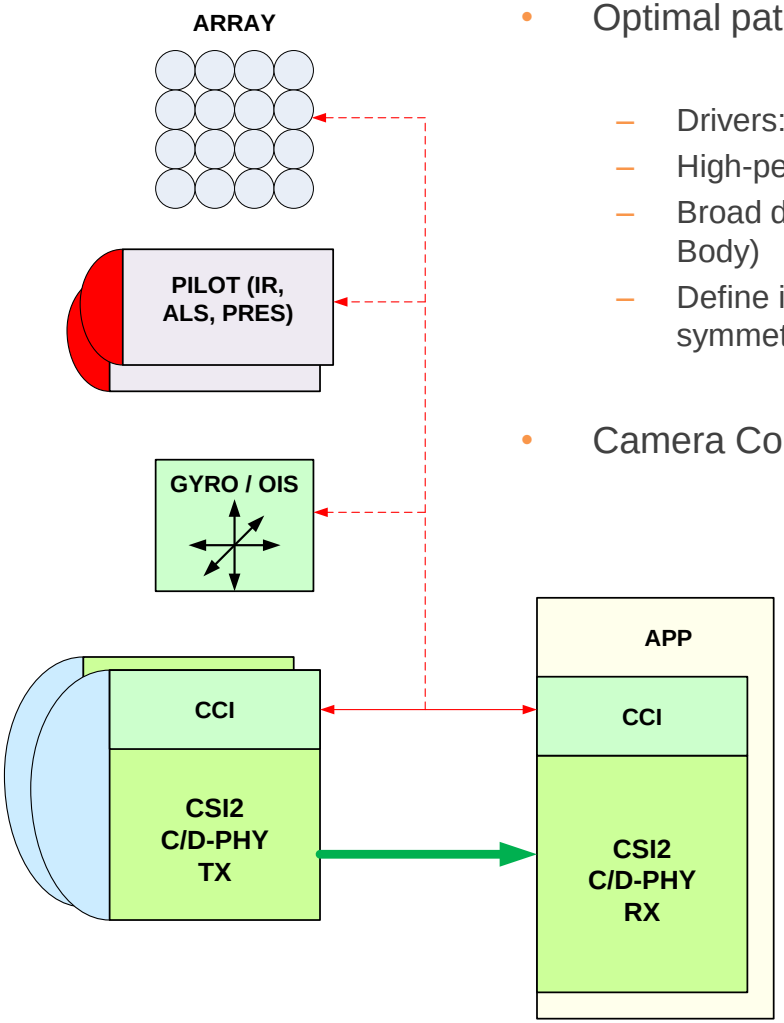
CSI-2 1.3

- D-PHY 1.2, C-PHY 1.0 or "combo PHY" is possible
- 4 Virtual Channels
- I2C based control interface
- Line based transmission
  - Easy implementation
  - Low gate count
  - Matched data rates for sensor and link
- In-band interrupts
- RGB, YUV, RAW, JPEG
- Embedded Data
- CRC/ECC for payload and header protection

CSI-3 1.1

- M-PHY 3.0
- 32 Virtual Channels
- In-band control
- Packet based transmission
  - Line-buffer-less architectures
  - Interleaving on message basis
  - Integration in network architectures
- In-band interrupts
- RGB, YUV, RAW, JPEG
- Embedded Data
- Notification channels for metadata, audio, etc.
- CCI bridging
- Guaranteed delivery of data

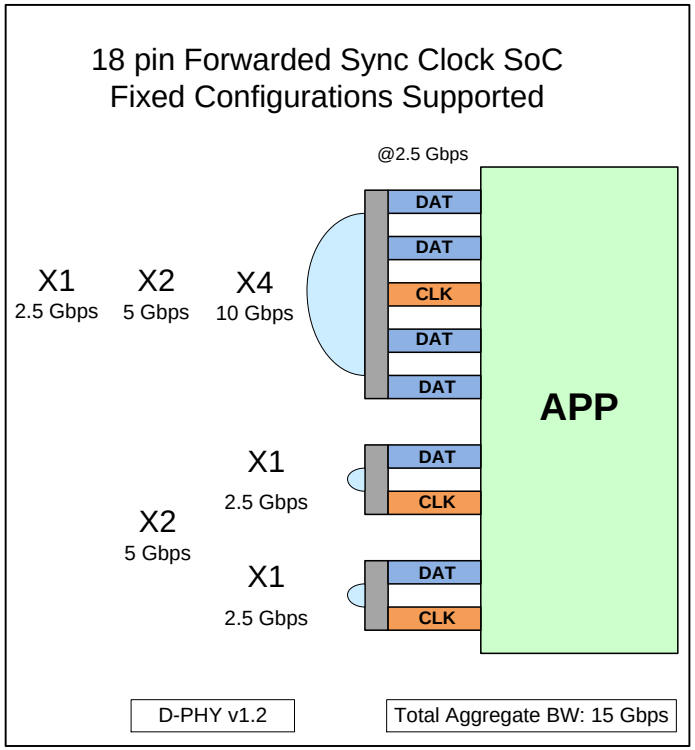
Sensor integration beyond traditional camera sensors (CSI-2)

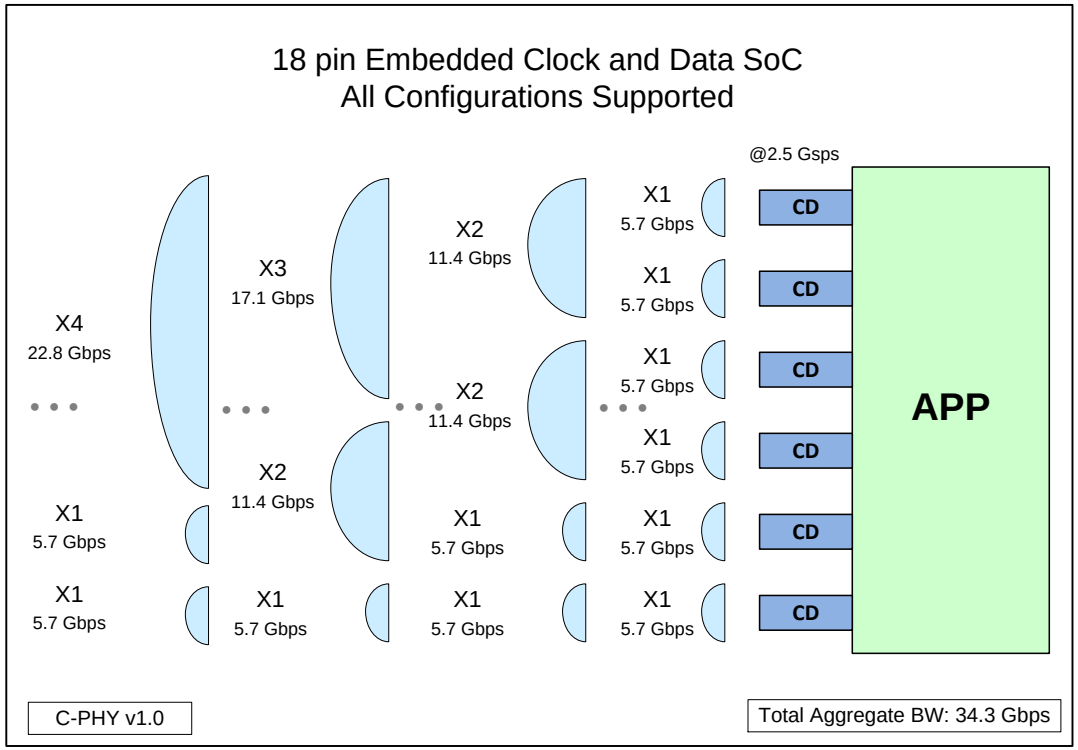


- Optimal pathway for multiple forward-looking advancements in imaging
  - Drivers: Health, Convenience, Security, Lifestyle, Efficiency
  - High-perf pixel conduit needs met with C/D-PHY advancements
  - Broad definitions and fuzzy range: (i.e. Wearable: Near Body, On Body, In Body)
  - Define imaging requirements for CCI, emerging AOI, array, and non-symmetrical applications
- Camera Controller Interface (CCI) advancement considerations:
  - Point-to-Point and Multi-Drop configurations
  - Energy consumed / Gb transfer
  - Limit latency for VB & HB
  - Precision Timing & Sync
  - Independent Transport: Pixel Data & Control
  - Channel Integrity (Error Detection)
  - FW Upload (ISP, Neural)
  - AOI Image Sensors

Benefits of Embedded Clock & Data (CSI-2)

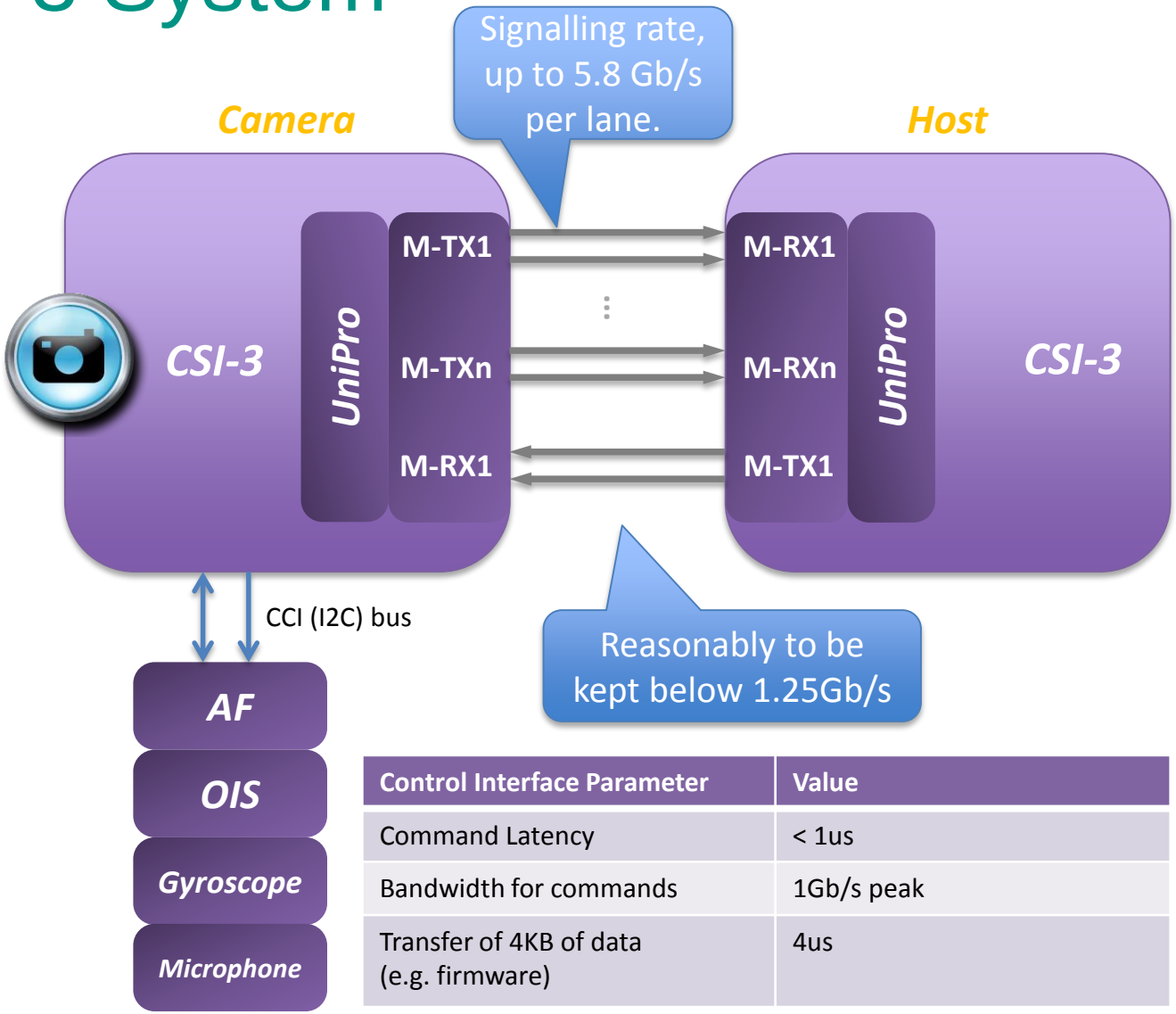
- Multiple port configurations are required to map Imaging Use Cases
- Embedded clock and data provides logical port realizations





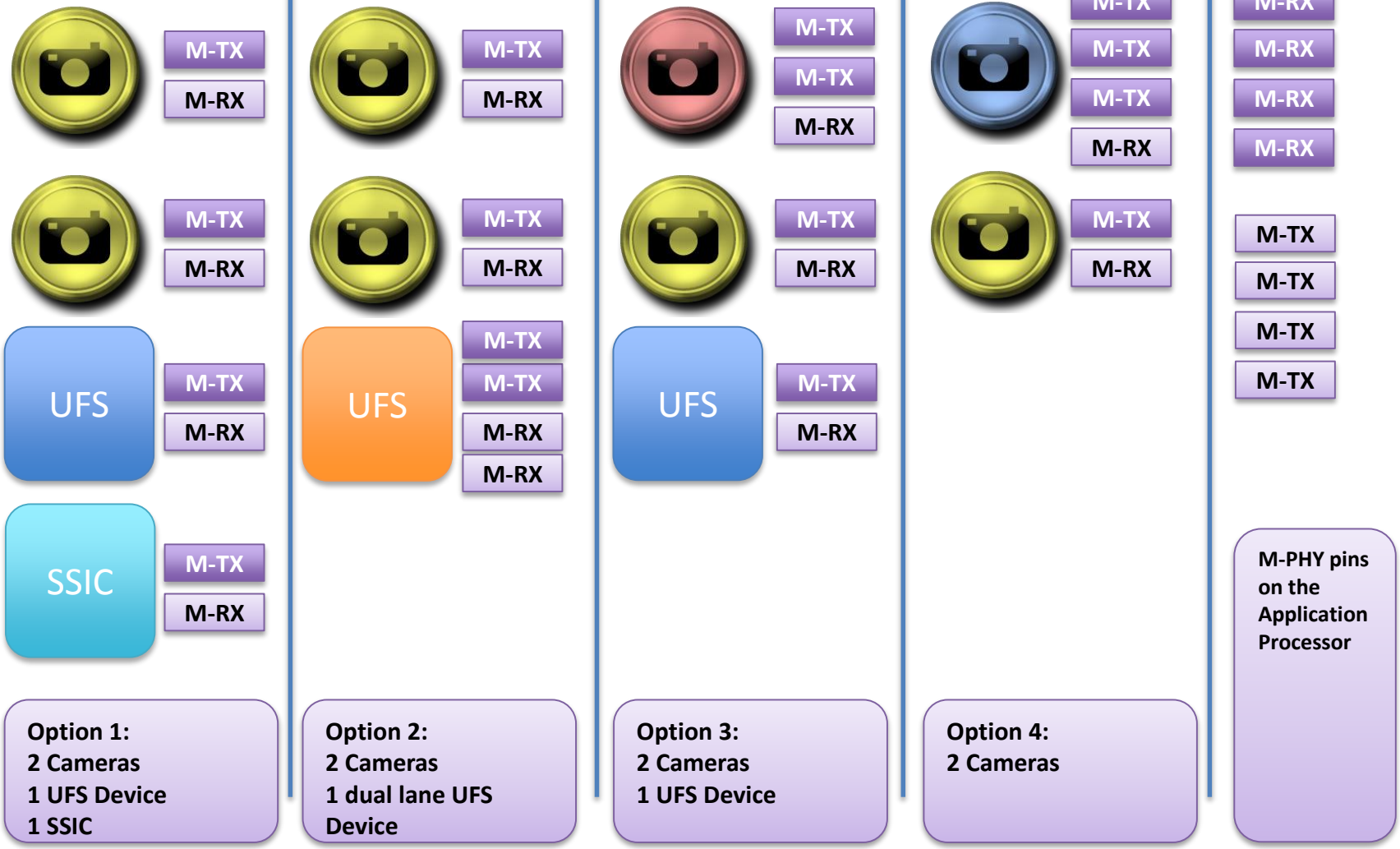
A x8 port maybe supported by allotting 16 pins for data and 2 pins for clock

CSI-3 System

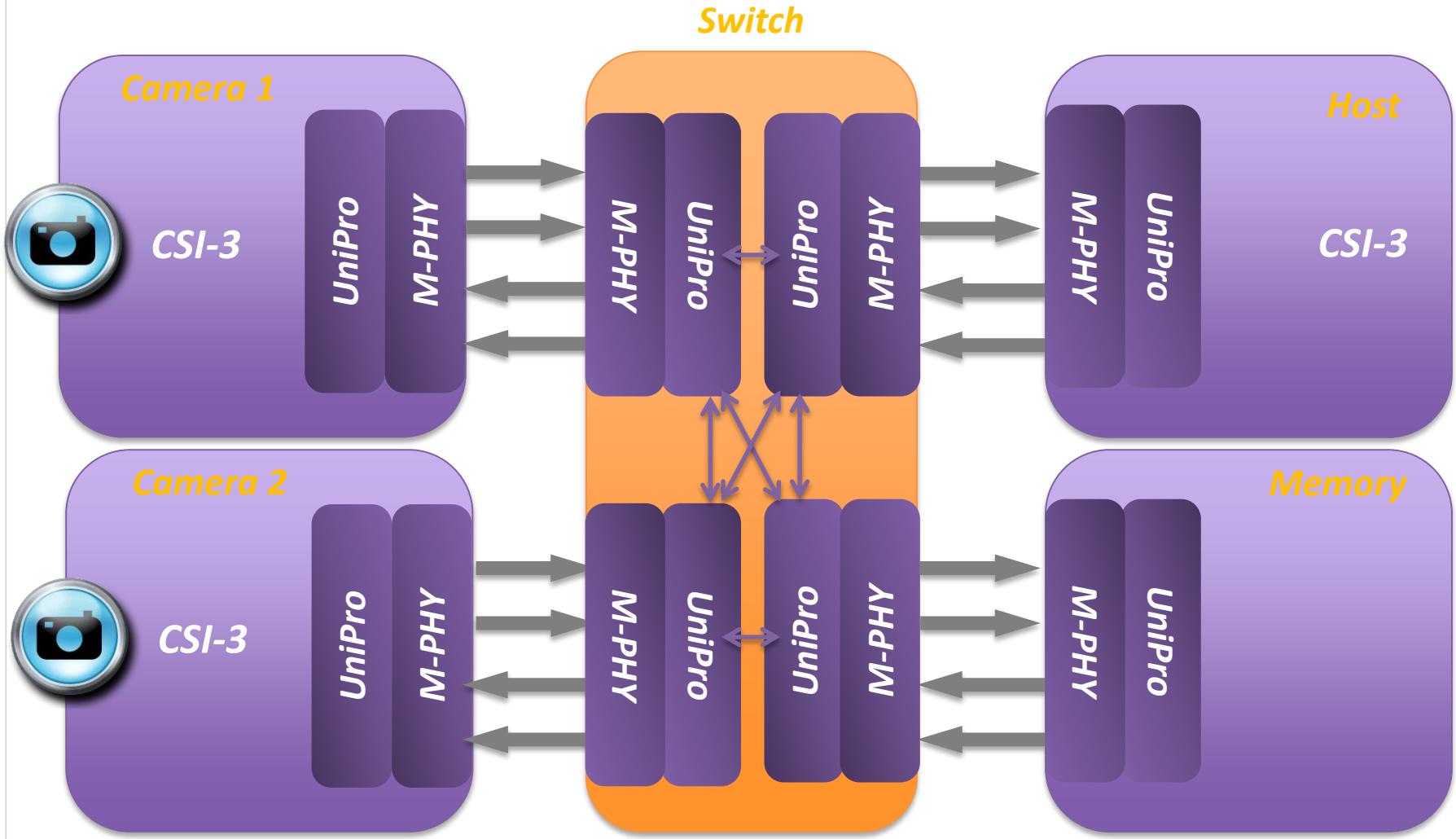


Control Interface Parameter	Value
Command Latency	< 1us
Bandwidth for commands	1Gb/s peak
Transfer of 4KB of data (e.g. firmware)	4us

Some of many options of multiplexing of M-PHY pins



CSI-3 over UniPro Switch Network



Questions?