Module 1
8086 Microprocessor

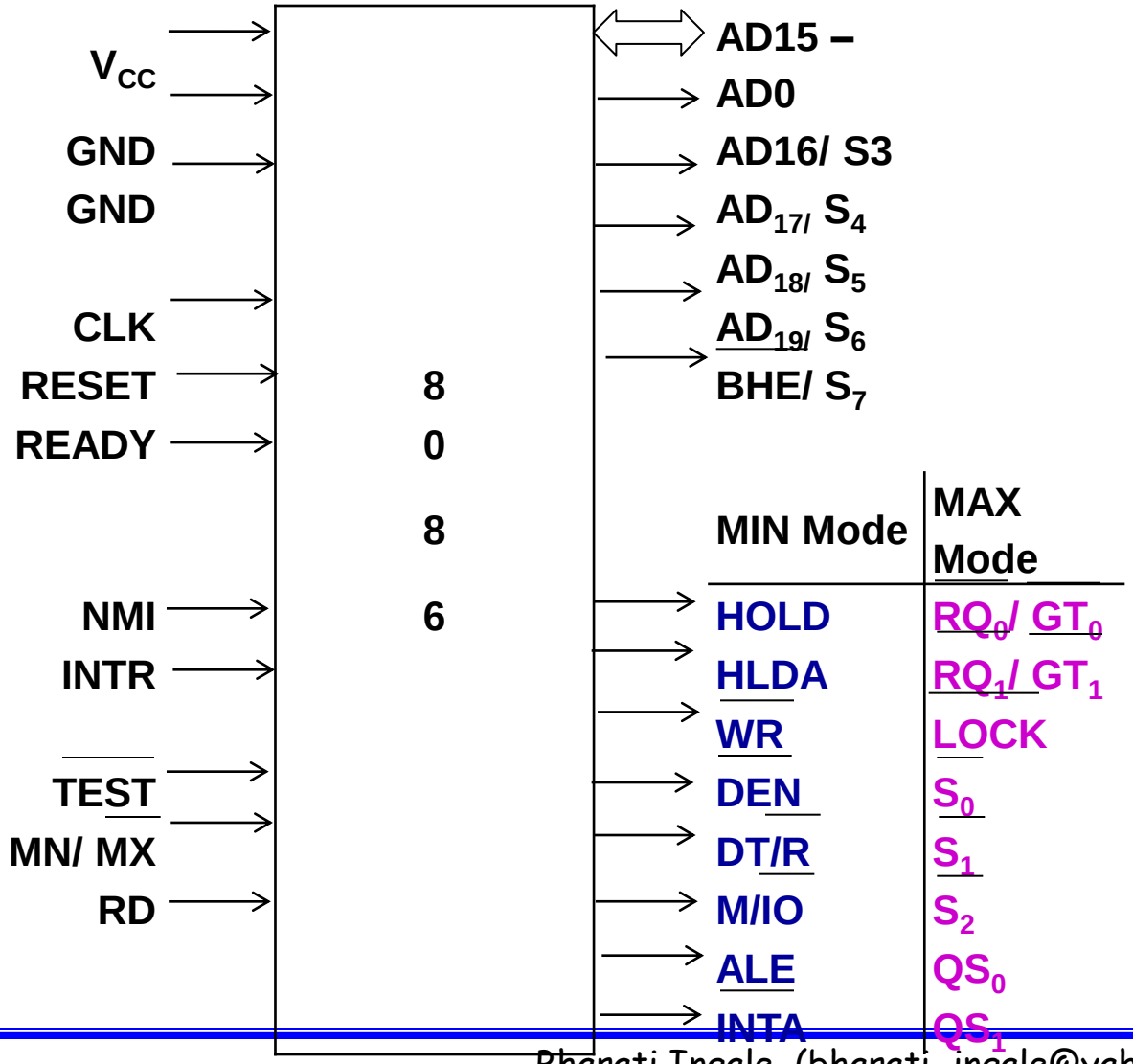
Modes of Operation

Bharati Ingale (bharati_ingale@yahoo.com)

8086 – Pin Diagram

- 8086 operates in 2 modes:
  i. Minimum Mode
  ii. Maximum Mode
- The minimum mode is used for a small system with a single processor
- The maximum mode is for medium size to large systems with 2 or more processors.

8086 – Functional Pin Diagram

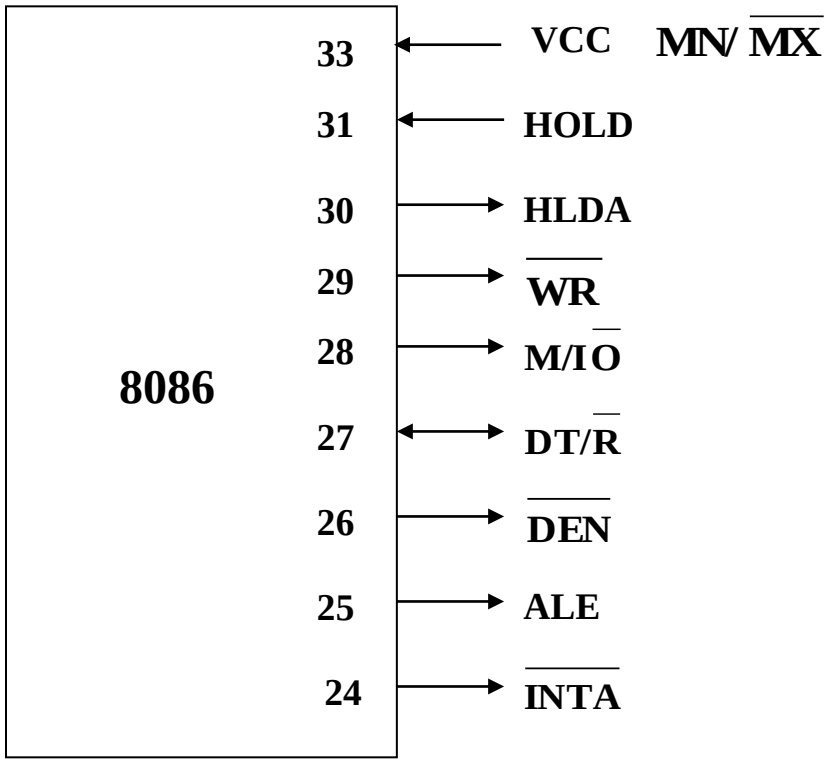


8086 – Pin Configuration

Pin Definitions:

6) Mode Multiplexed signals (8 pins)

MIN Mode	MIN Mode
HOLD	DT/$\overline{R}$
HLDA	M/$\overline{IO}$
$\overline{WR}$	ALE
$\overline{DEN}$	INTA

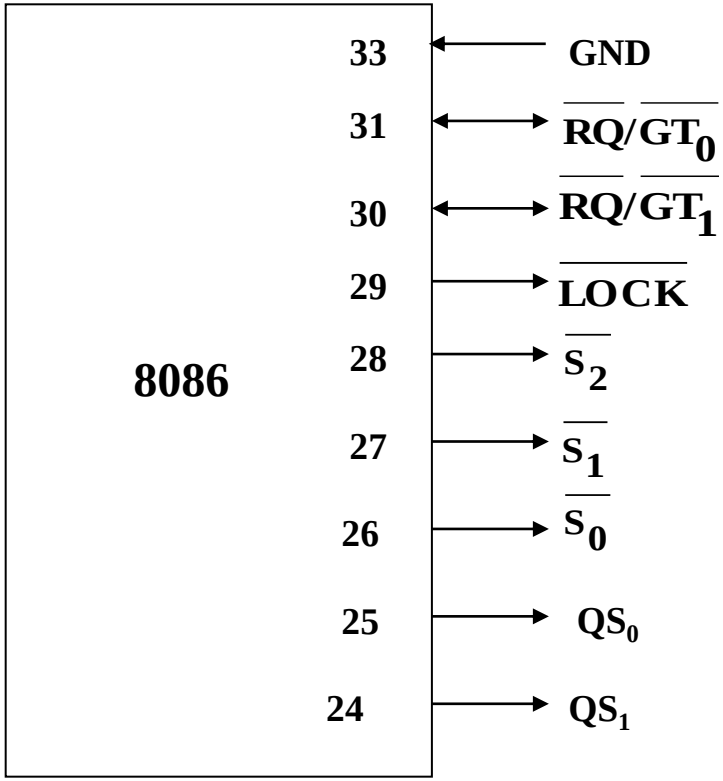


8086 – Pin Configuration

Pin Definitions:

6) Mode Multiplexed signals (8 pins)

MAX Mode	MAX Mode
$\overline{RQ_0}$/ $\overline{GT_0}$	$\overline{S_1}$
$\overline{RQ_1}$/ $\overline{GT_1}$	$\overline{S_2}$
$\overline{LOCK}$	QS_0
$\overline{S_0}$	QS_1



8086

Some common components of 8086 circuit in MIN or MAX mode are:

1. 8282: (8 – bit) Octal Latch
2. 8286: (8 – bit) Octal bus Transreceiver
3. 8284: Clock Generator.
4. 8288: Bus Controller

8284: Clock Generator

8284: Clock Generator & Driver

i. Provides CLOCK (C LK) signal, a train of pulses at a constant frequency

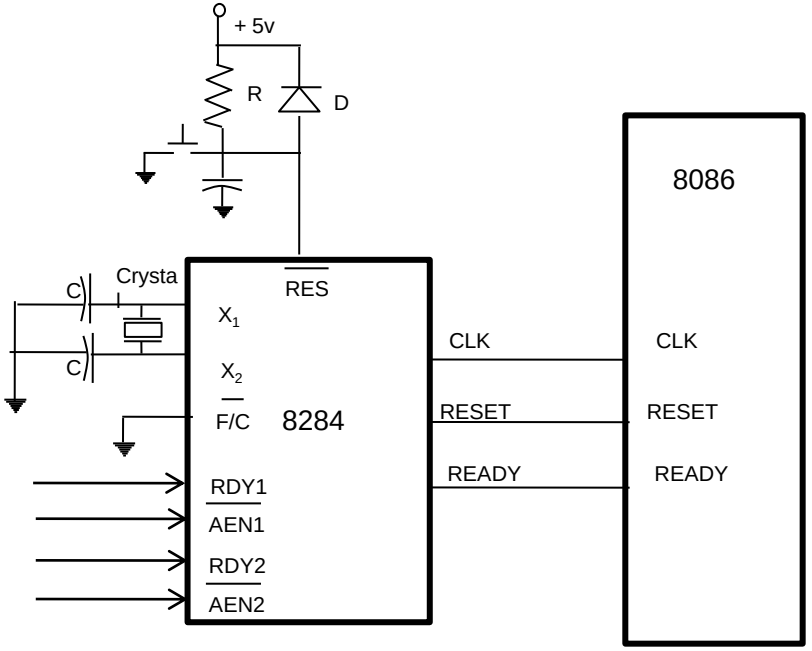
ii. It synchronizes the READY (RDY) signal which indicates that an interface is ready for data.

iii. Also synchronizes the RESET (RST) signal which is used to initialize the system

iv. 2 ways :

EFI - (External Frequency Input)

X1,X2 –Oscillator Clock Input)



Clock Input selection

F/C = 0 ⟶ Input clock given through EFI

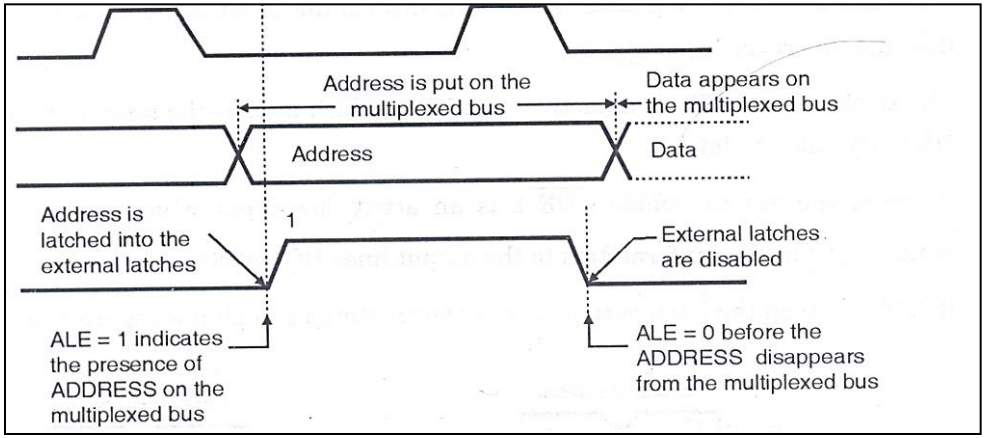
F/C = 1 ⟶ Input clock given through Crystal

(Oscillator inputs X1,X2 pins)

8282: (8 – bit) Octal Latch

8282: 8 bit latch

- The address data bus AD15-AD0 is time multiplexed: Time Sharing Basis
- The address lines A16 – A19 are multiplexed with S_3 -S_6
- Also $\overline{BHE}$ & S7 is multiplexed.



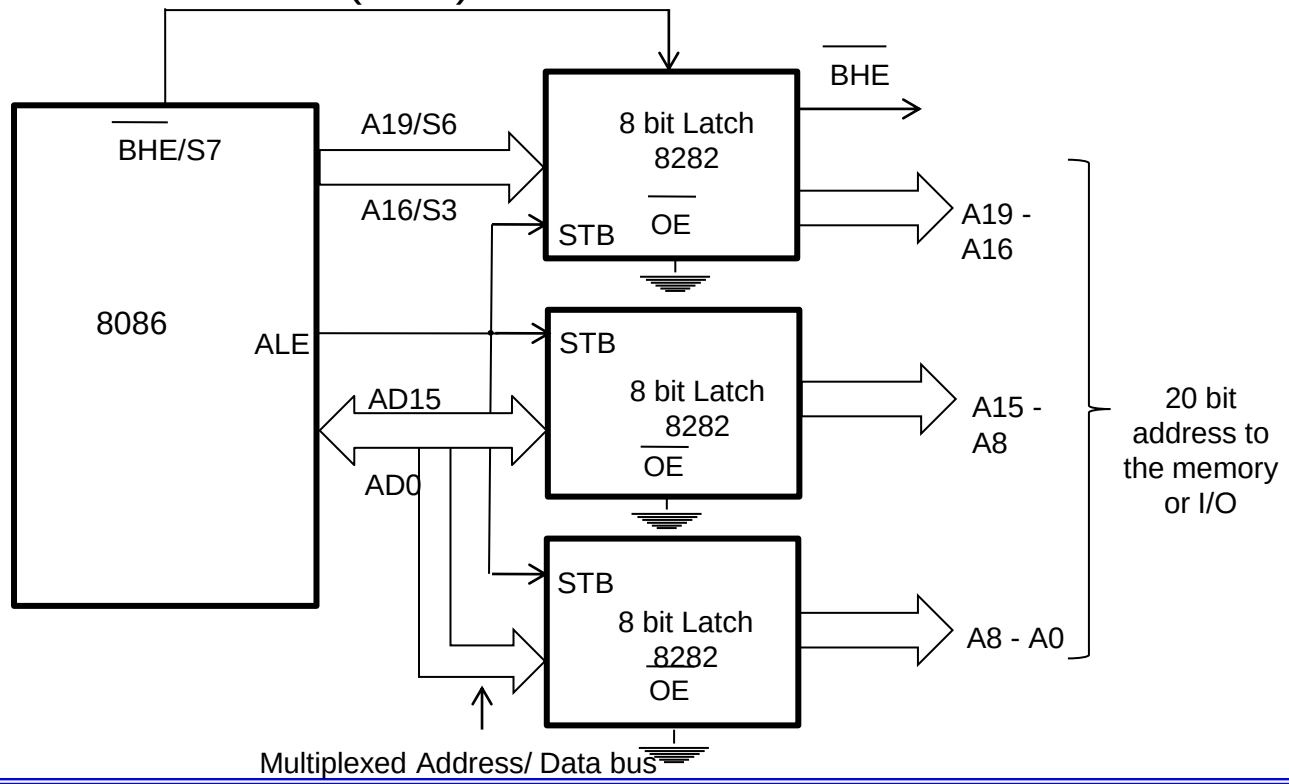
Timing diagram showing the role of ALE in Multiplexed Address Data Bus

- The address bus and the $\overline{BHE}$ signal are demultiplexed using the ALE signal and then latched into 8282

8282: 8 bit latch

- The latches are buffered D FF.
- Used to separate the valid address from the multiplexed Address/data bus by using the control signal ALE,
- ALE is connected to strobe($\overline{STB}$) of 8282

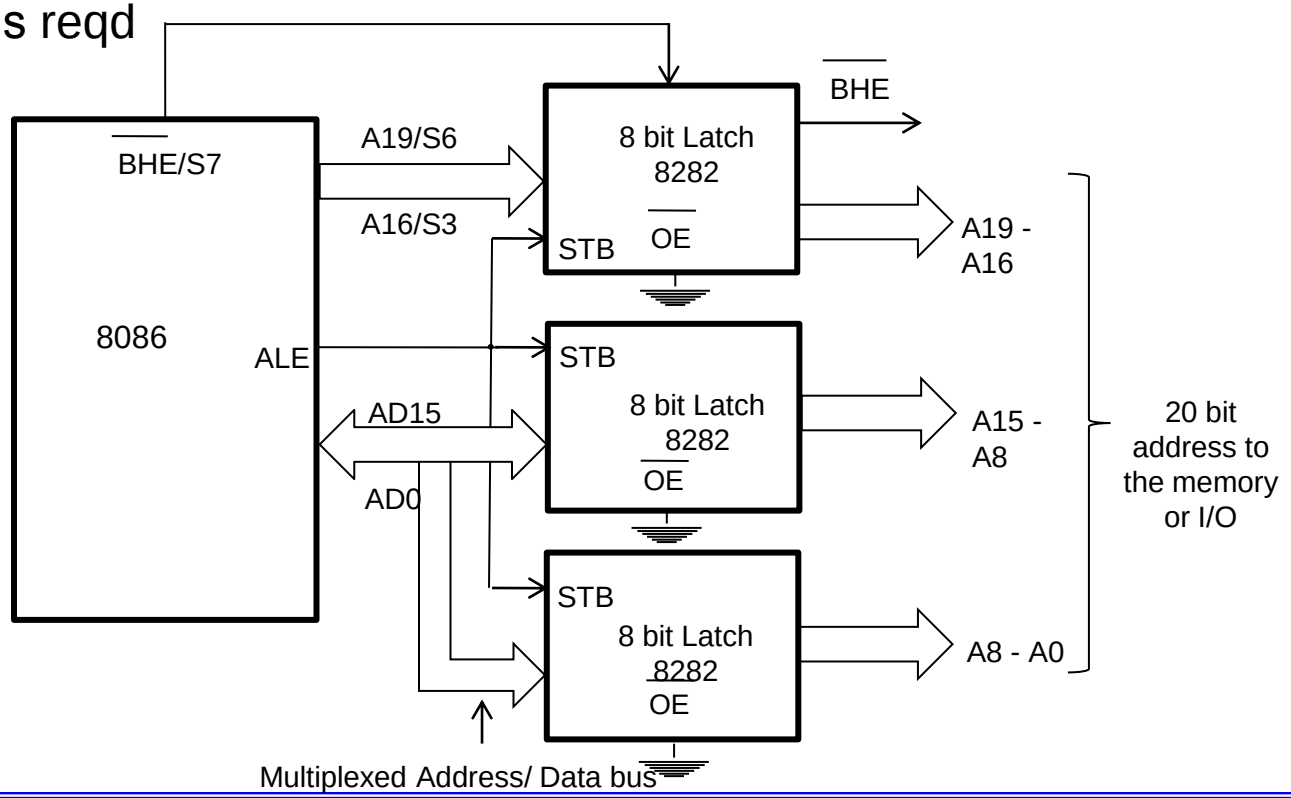
(8 bit latch & 21 lines, so 3 latches reqd).



8282: 8 bit latch

- The high ALE asserts the STB of 8282, It enables the external latches to store the address.
- Thus to get the 20 bit address (A0-A7, A8-A15,A16-A19) and the $\overline{BHE}$ signal, 3 - 8282's is reqd

(8 bit latch & 21 lines, so 3 latches reqd).



8286: (8 – bit) Octal bus Transreceiver

8286: Octal trans-receiver (Transmitters & Receivers)

i. Contains fully parallel 8 bit bus trans- receiver. ∴ 2 transceivers are required as data bus is 16 – bits.

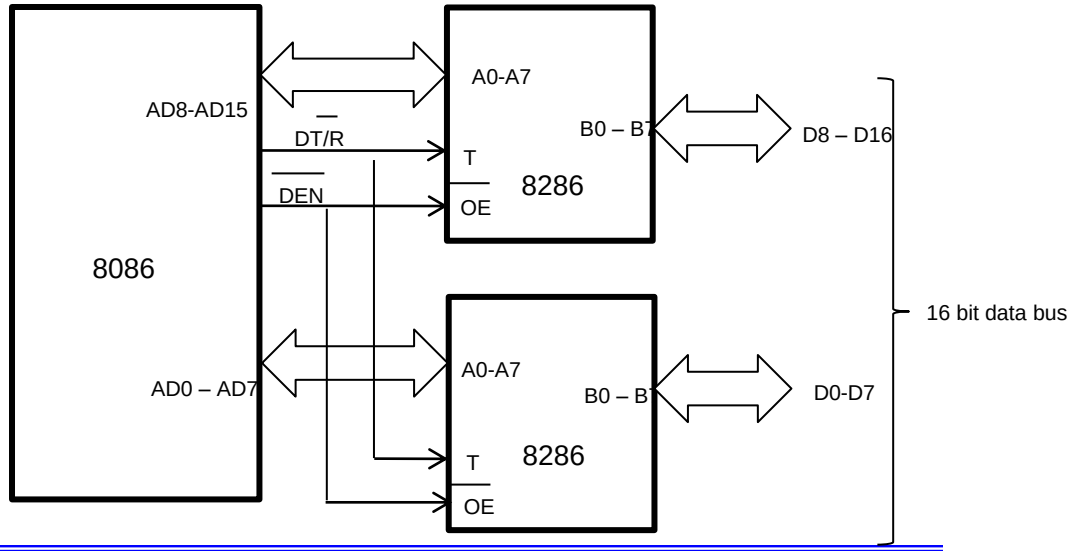
ii. Tri-state (high impedance outputs)

iii. Acts as bidirectional buffer and increases the driving capacity of the data bus.

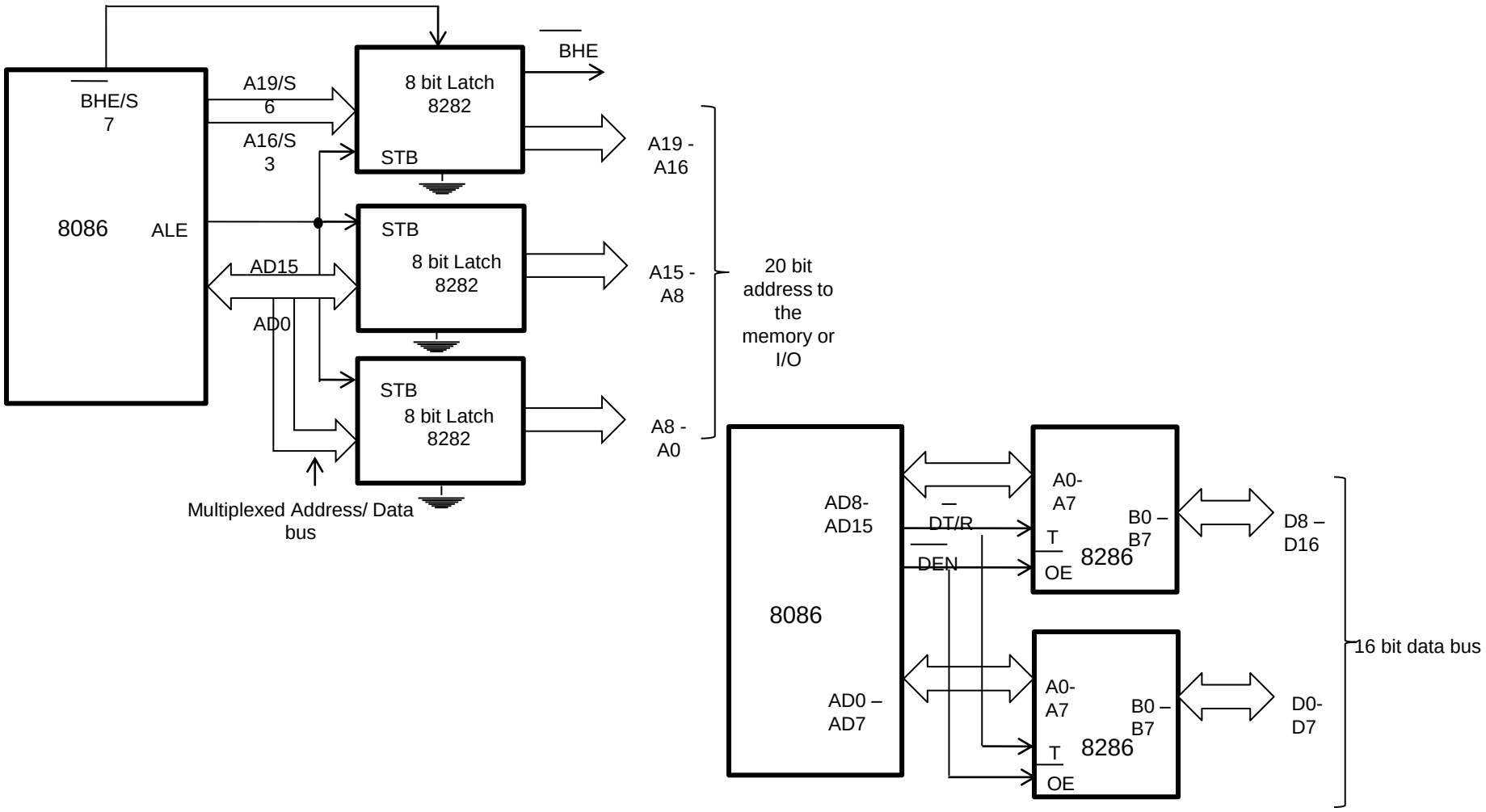
iv. It is enabled when $\overline{OE}$ is low

v. T controls the direction of flow of data

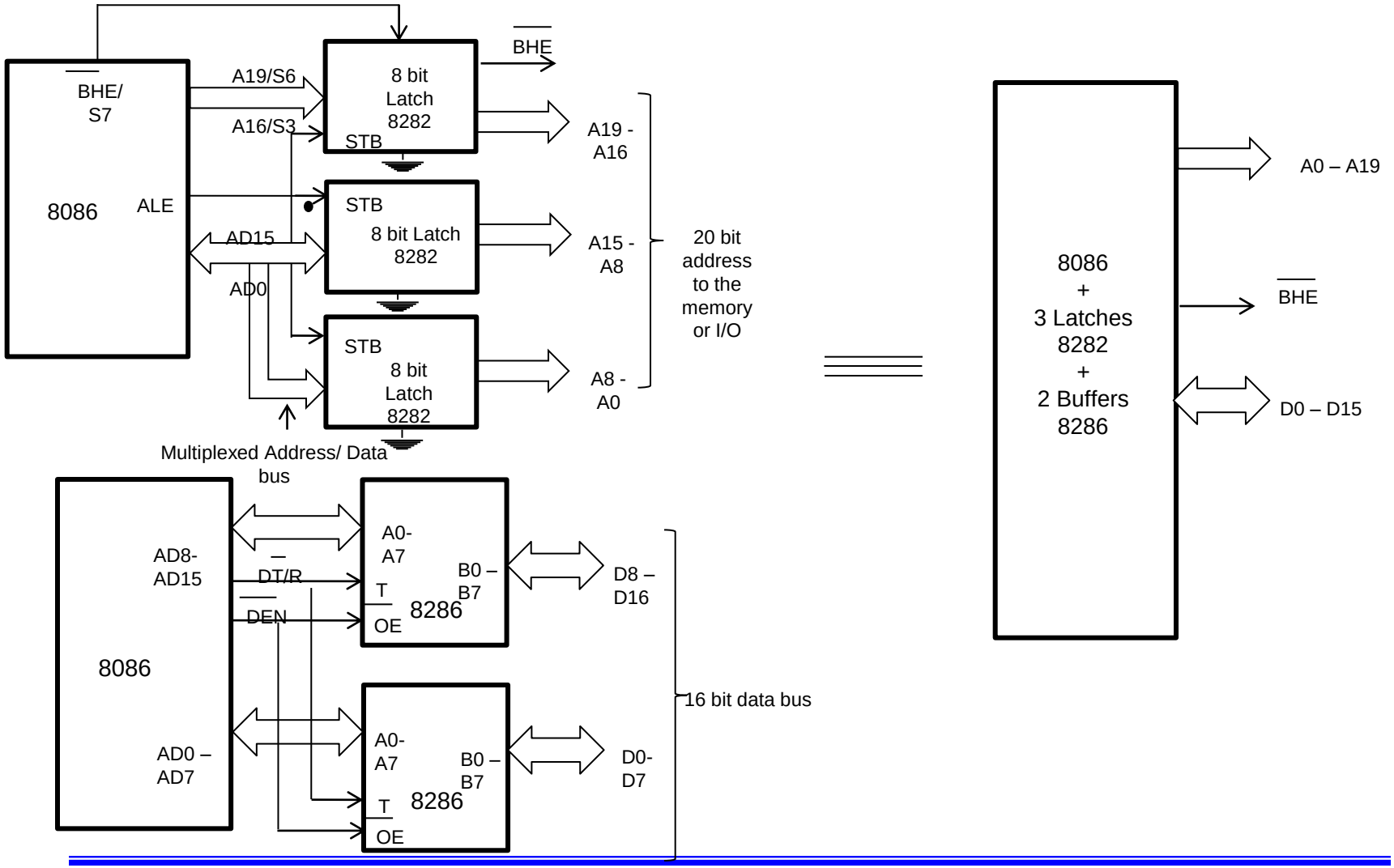
- T =1 ⟶ data is transmitted
- T = 0⟶ data is received



8086 – Demultiplexing Address and Data Bus



8086 – Demultiplexing Address and Data Bus



8288: Bus Controller

8086 : Operating Modes

- When the Minimum mode operation is selected, the **8086 provides all control signals** needed to implement the memory and I/O interface.

- While in Maximum mode operation, the **8288 provides all control signals** needed to implement the memory and I/O interface.

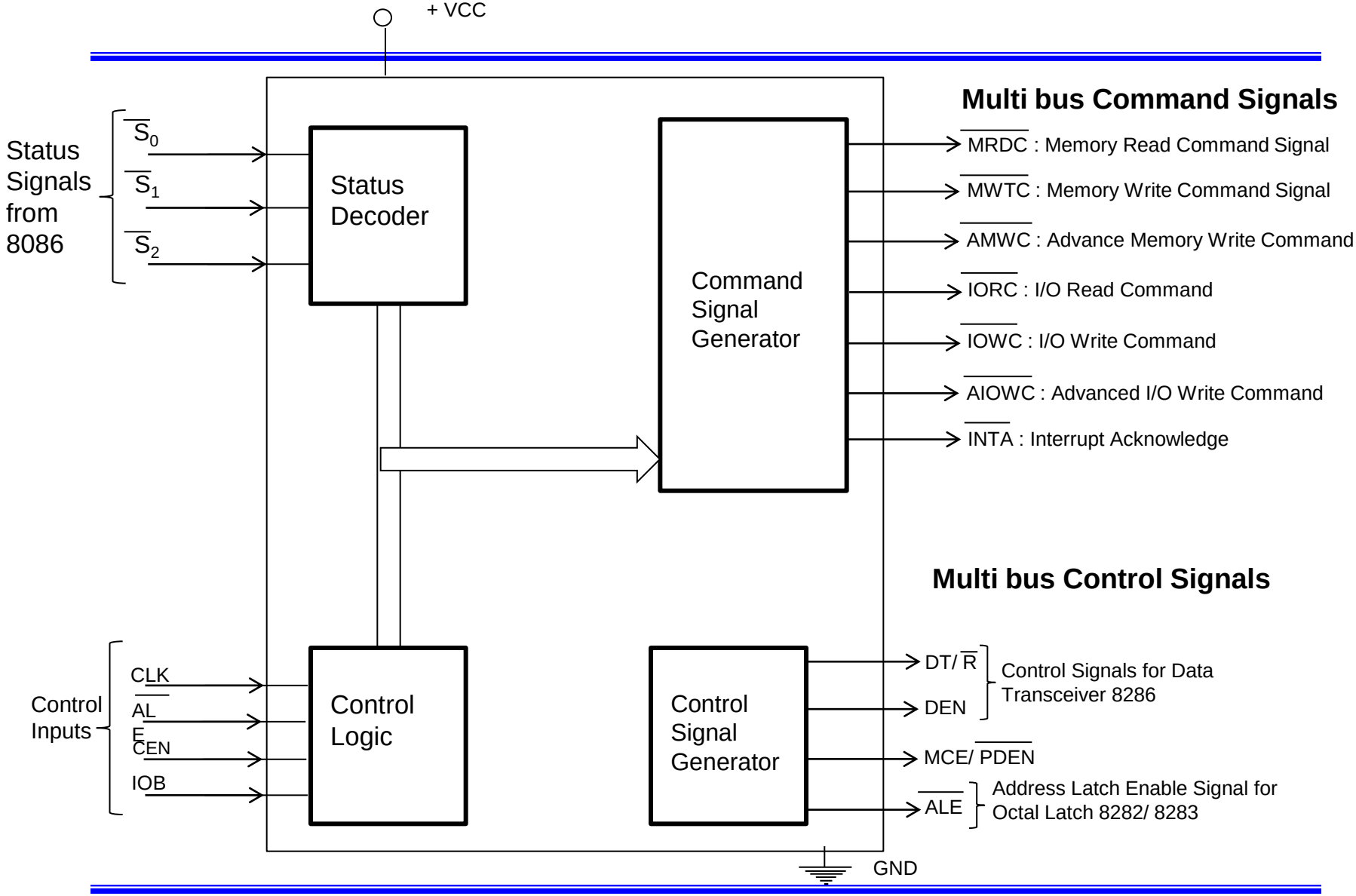
.

8288: Bus Controller

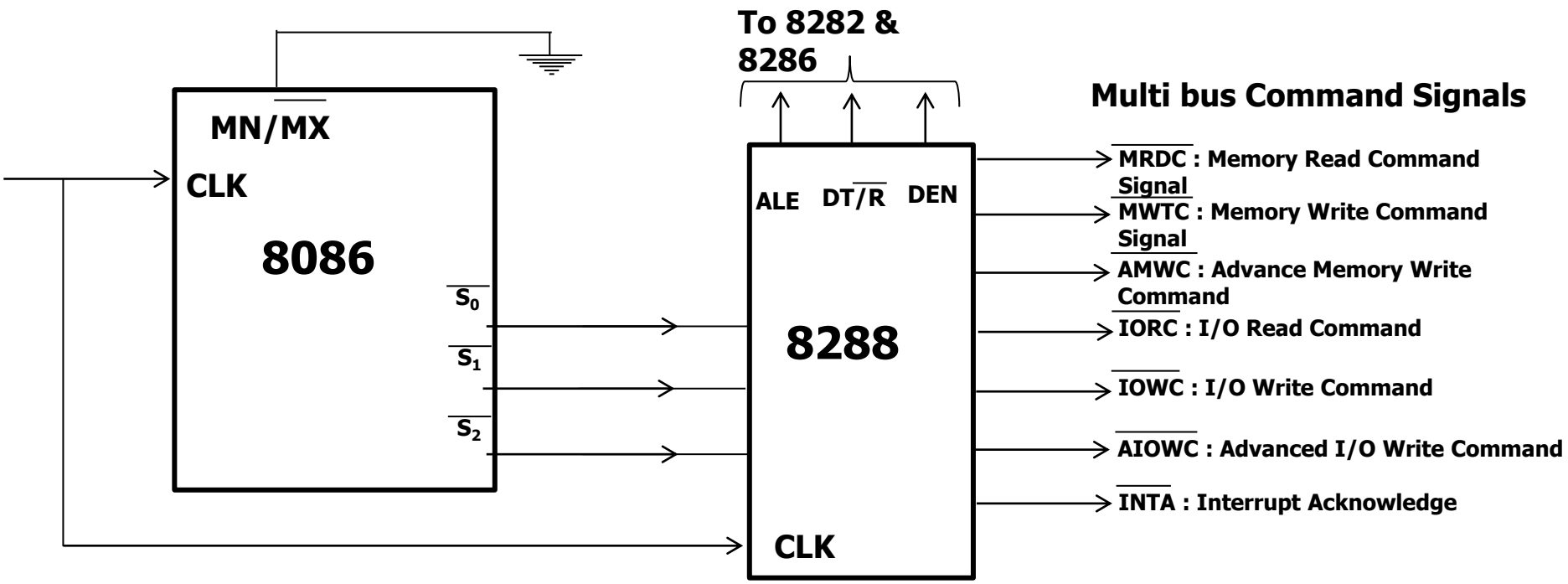
- It is used in maximum mode configuration
- It accepts the CLK signal along with S_0, S_1, S_2
- It generates the
  i. command,
  ii. control &
  iii. timing signals at its output

Bharati Ingale (bharati_ingale@yahoo.com)

8288: Bus Controller



8288: Bus Controller

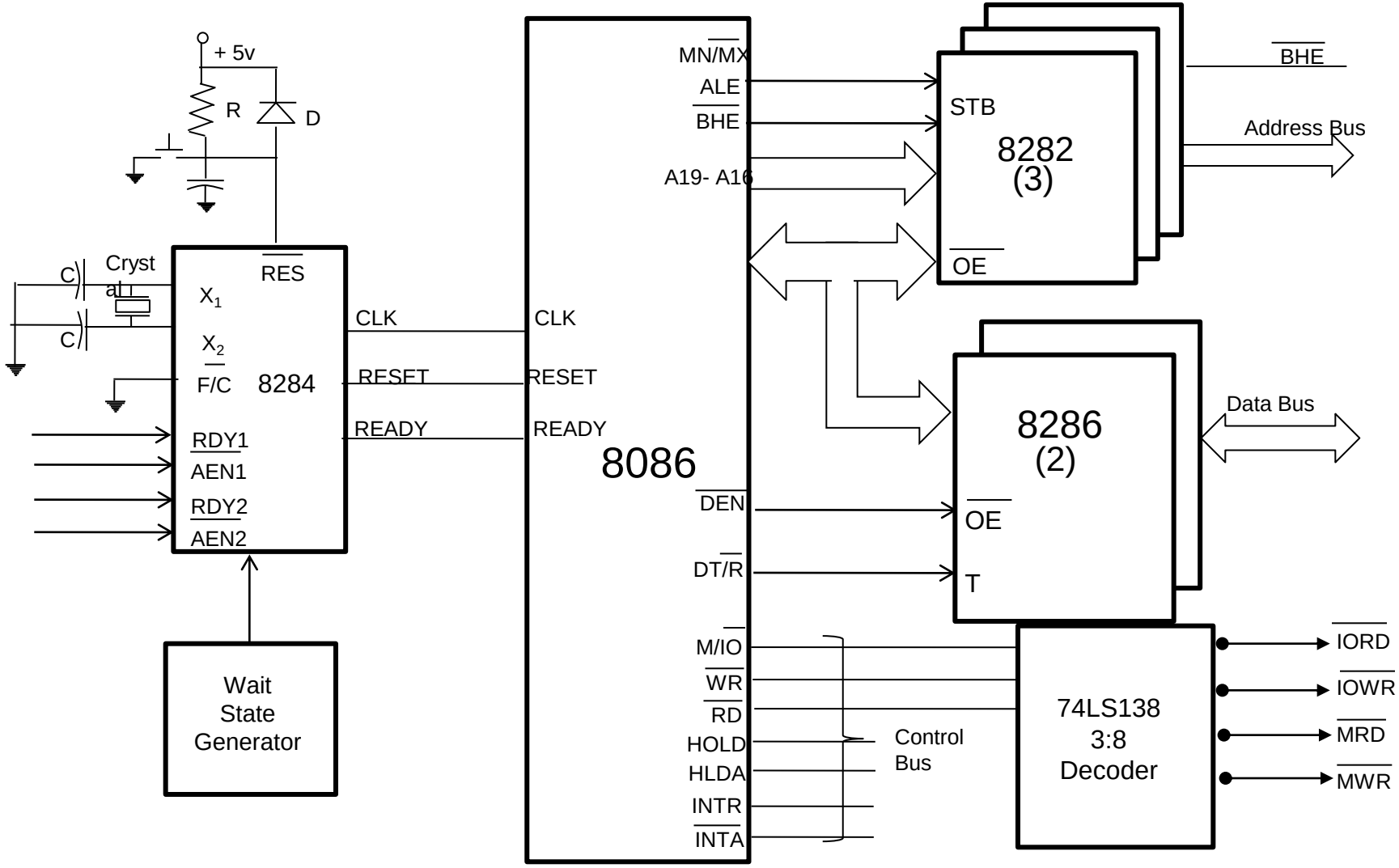


8086 – Machine Cycle

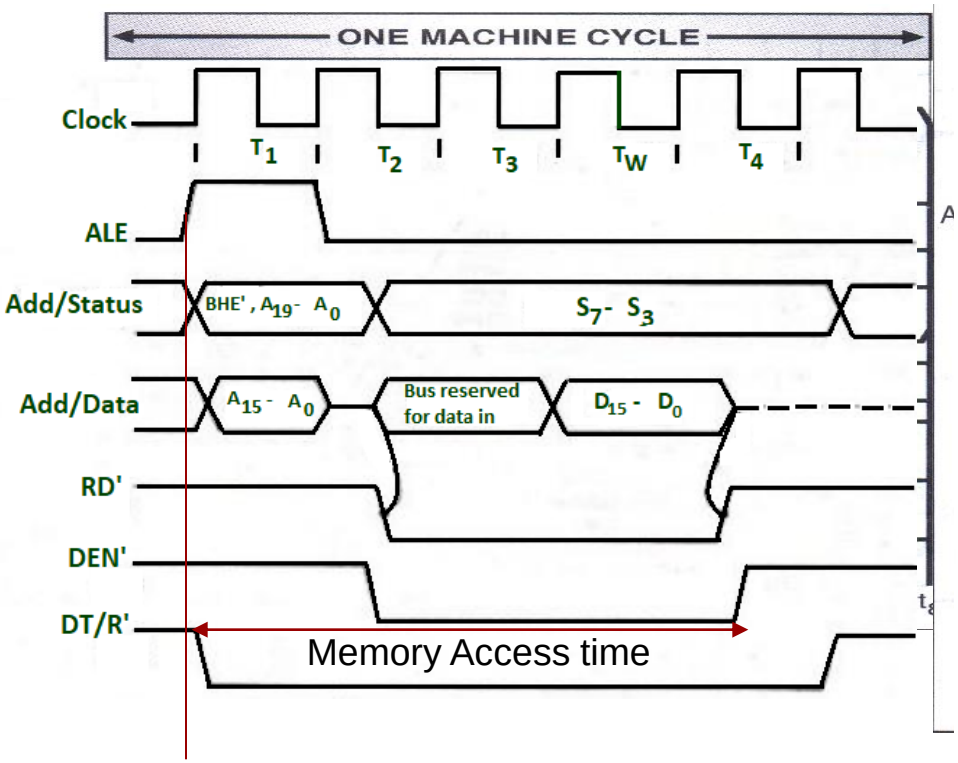
In Maximum Mode S_0,S_1, S_2 lines are connected to 8288

S_2	S_1	S_0	**Bus Cycle/ Machine Cycle**
0	0	0	INTA Cycle
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt
1	0	0	Opcode Fetch
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	Inactive

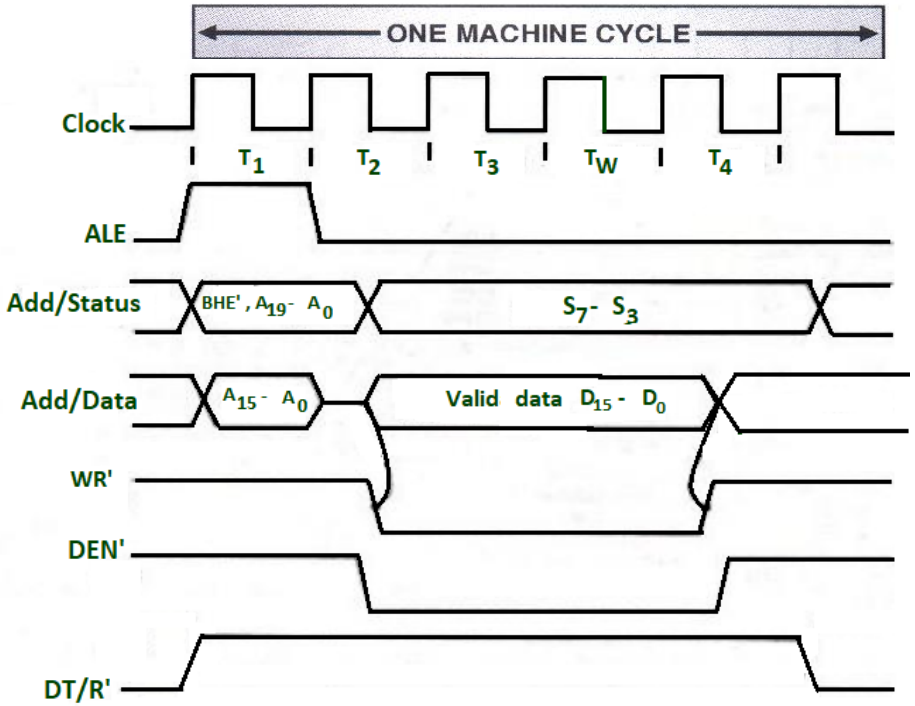
8086 - Minimum Mode Minimum System Block Diagram



Read M/Cycle in Min Mode

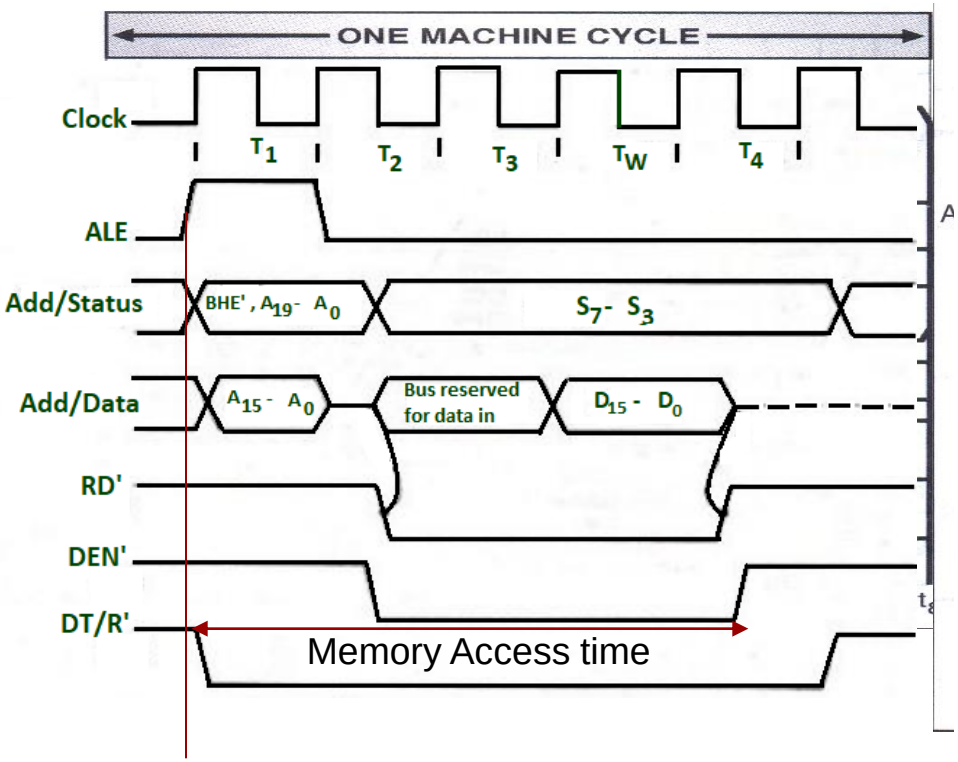


Write M/Cycle in Min Mode

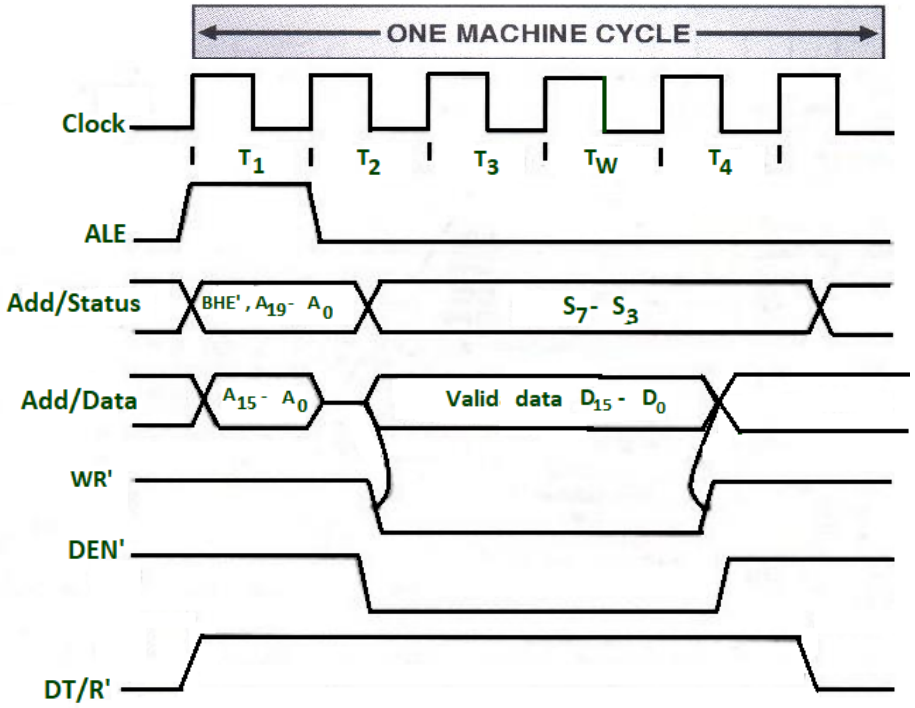


- All processors bus cycle is of at least 4 T-states(T_1,T_2,T_3,T_4) .

Read M/Cycle in Min Mode

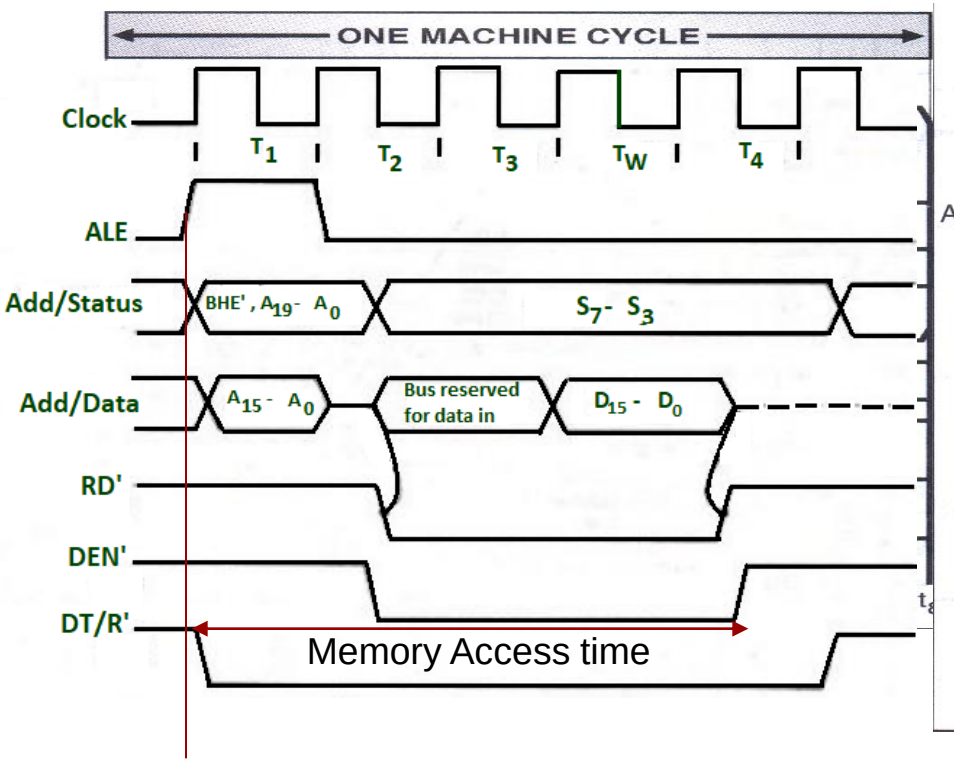


Write M/Cycle in Min Mode

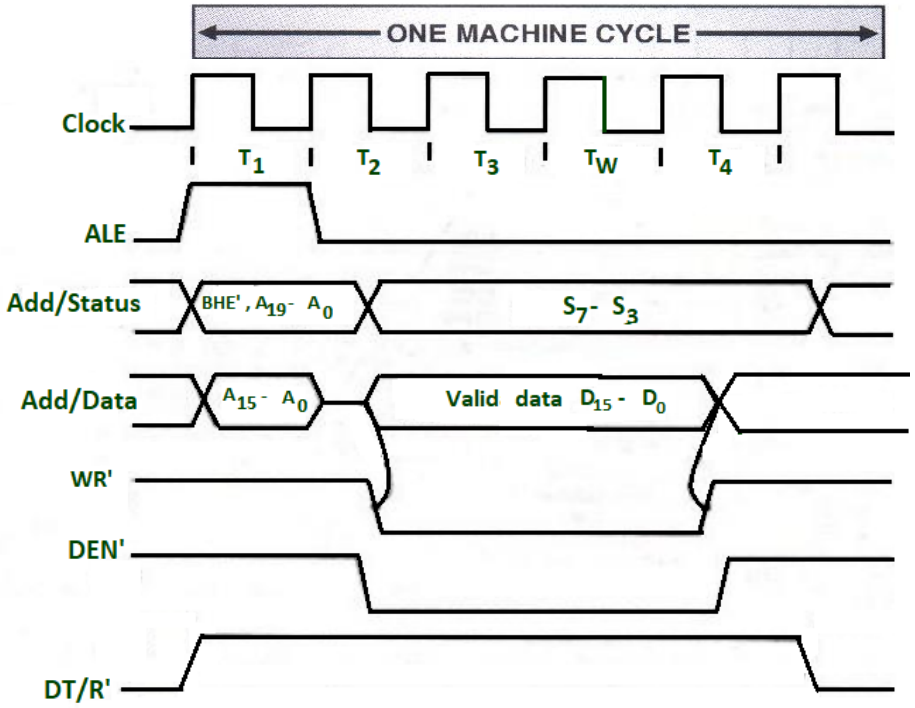


- The address is given by processor in the T1 state. It is available on the bus for **one T-state.**

Read M/Cycle in Min Mode

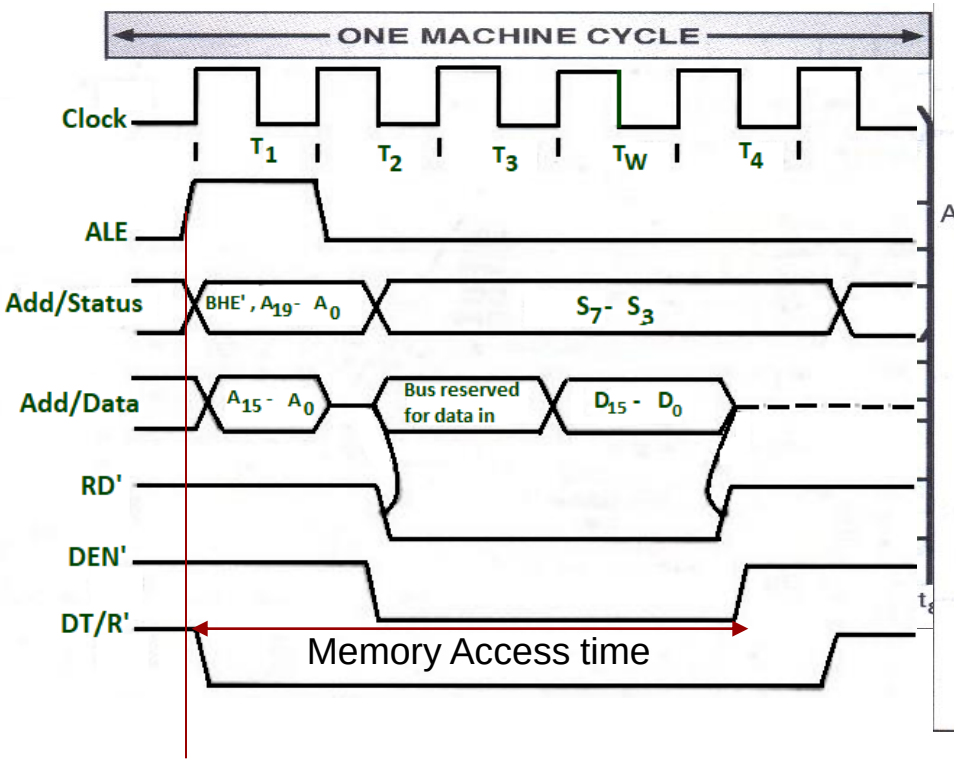


Write M/Cycle in Min Mode

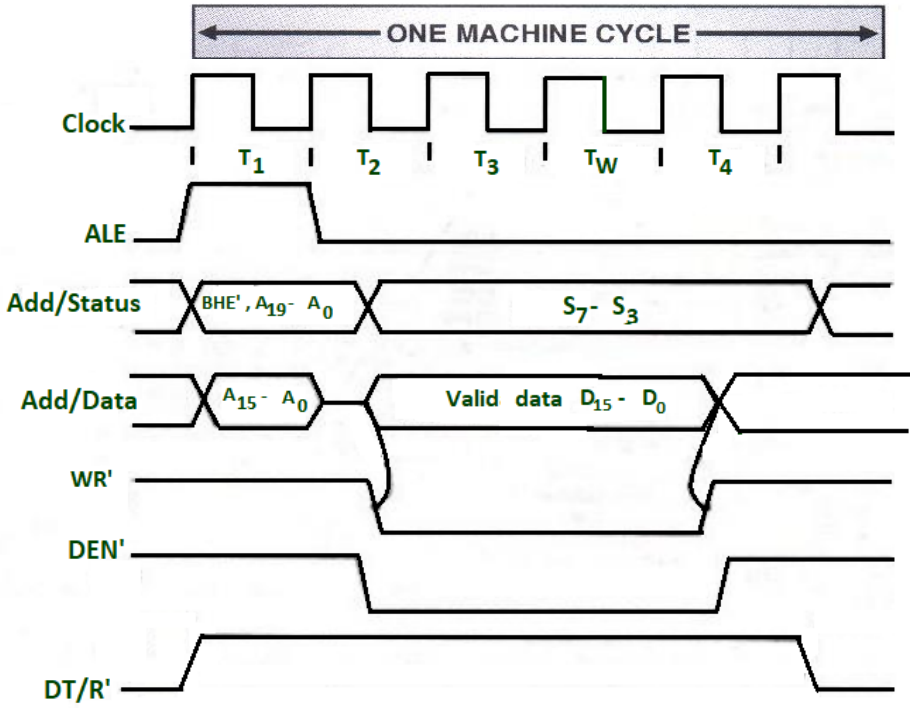


- In T2, the bus is tristated for changing the direction of the bus(in the case of a data read cycle.)

Read M/Cycle in Min Mode

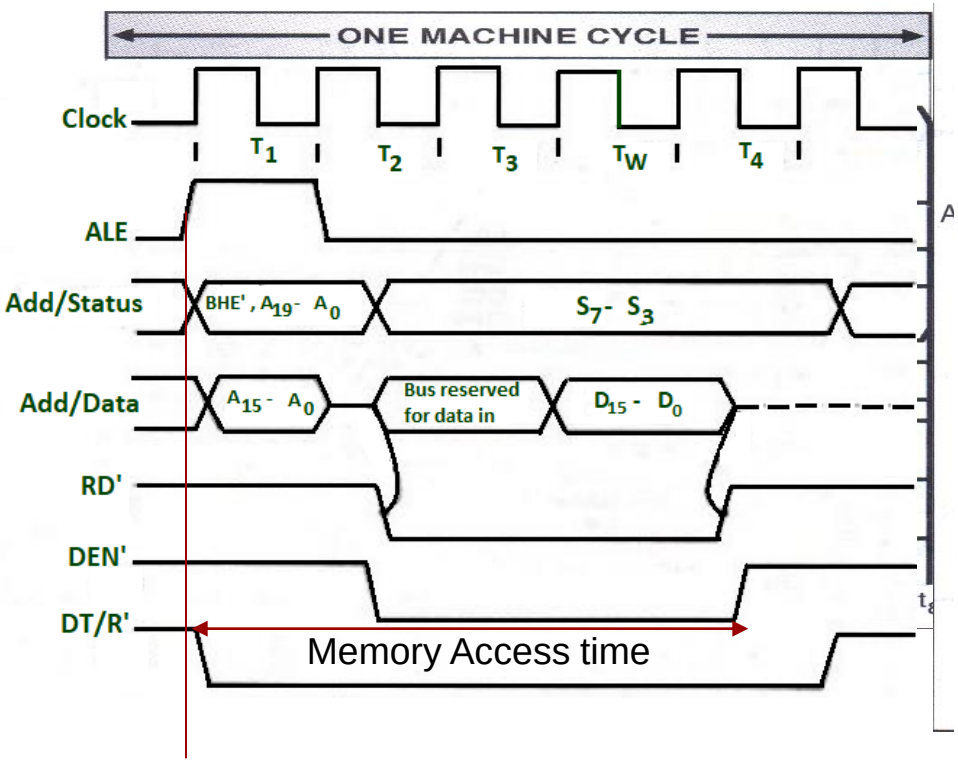


Write M/Cycle in Min Mode

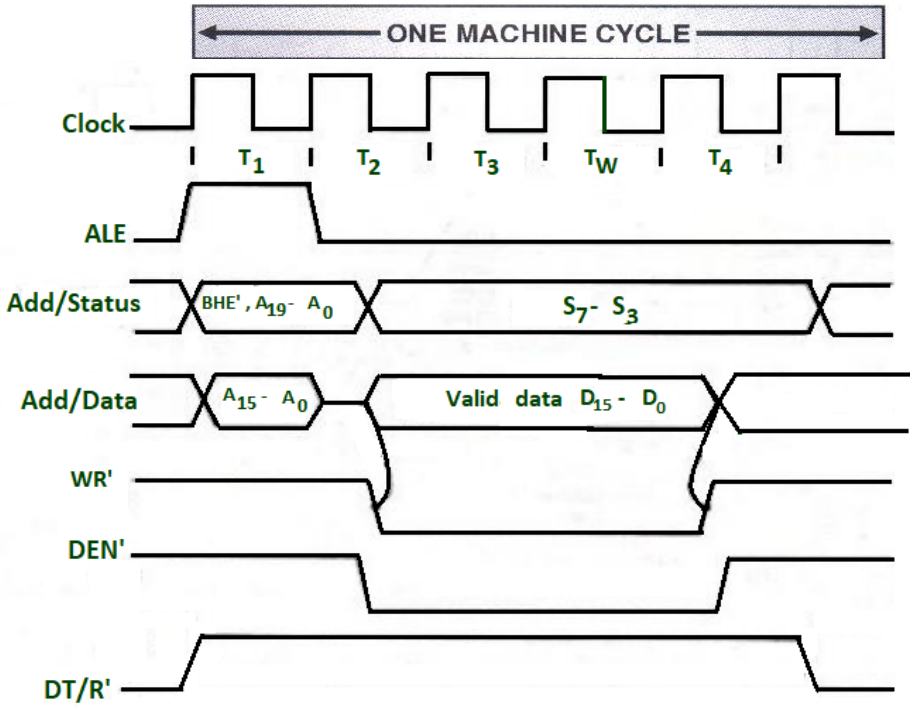


- The data transfer takes place between T3 and T4.

Read M/Cycle in Min Mode

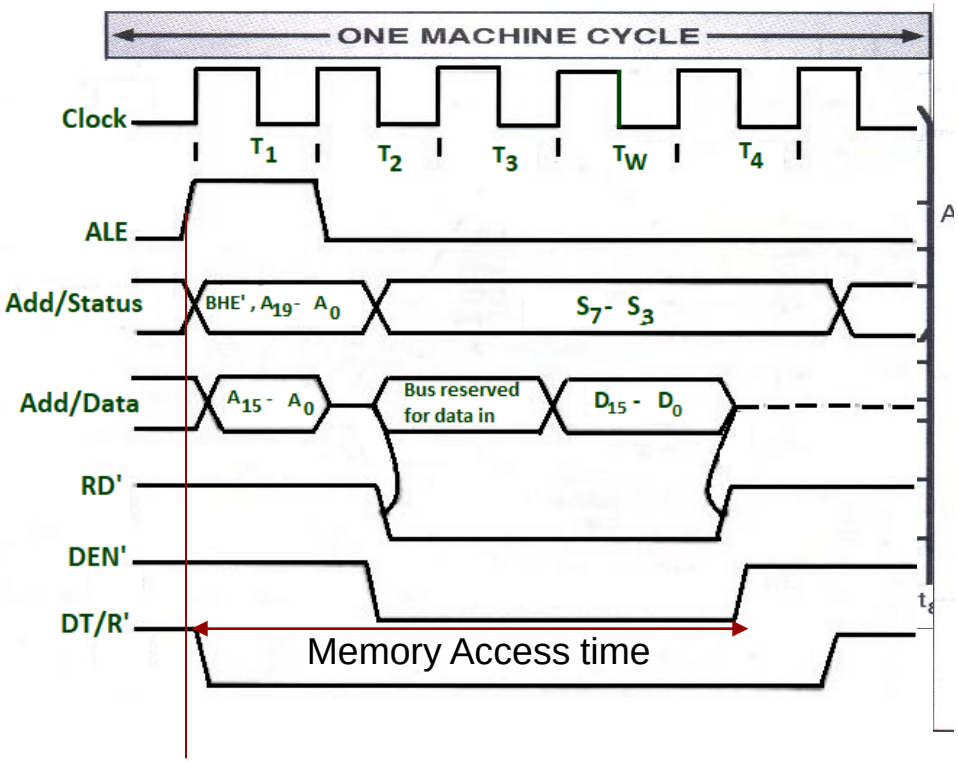


Write M/Cycle in Min Mode

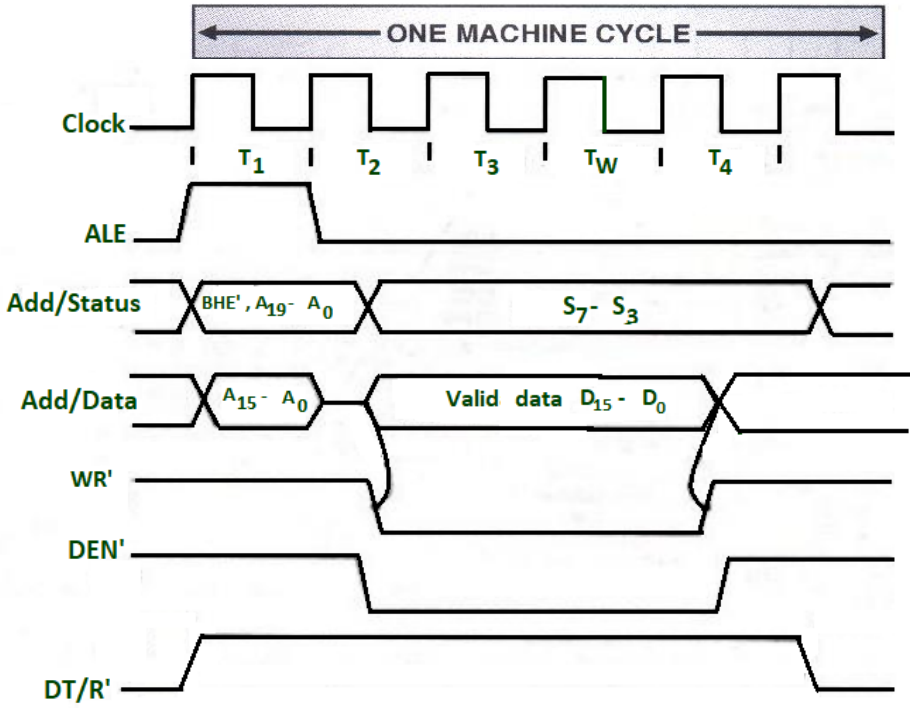


- If the addressed device is slower, then the wait state is inserted between T3 and T4.

Read M/Cycle in Min Mode

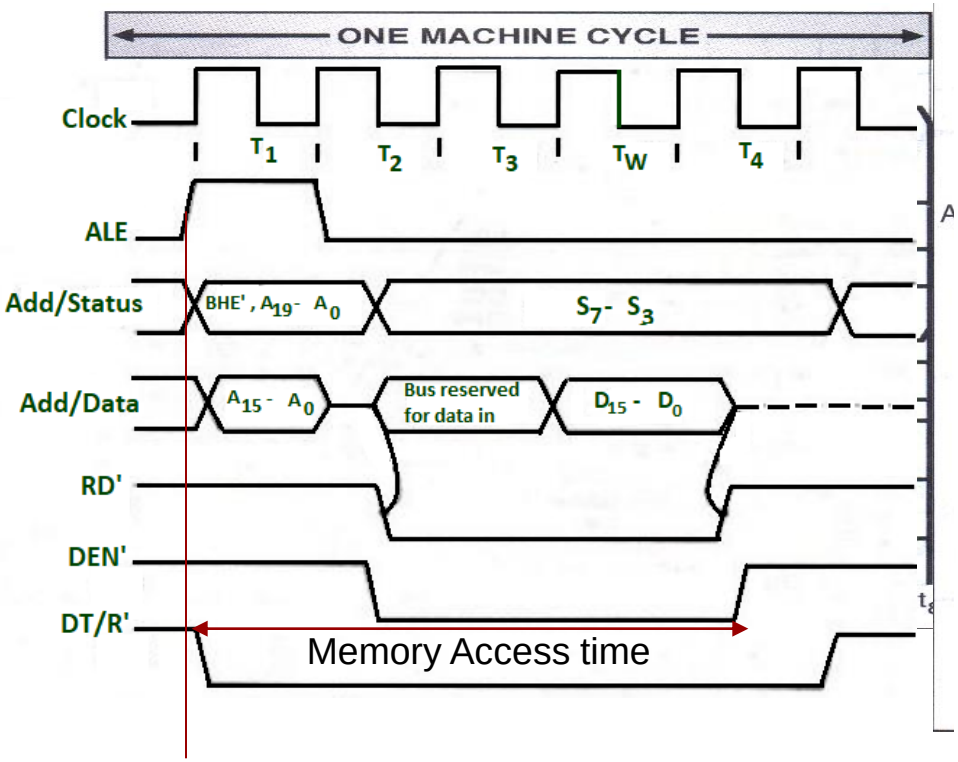


Write M/Cycle in Min Mode

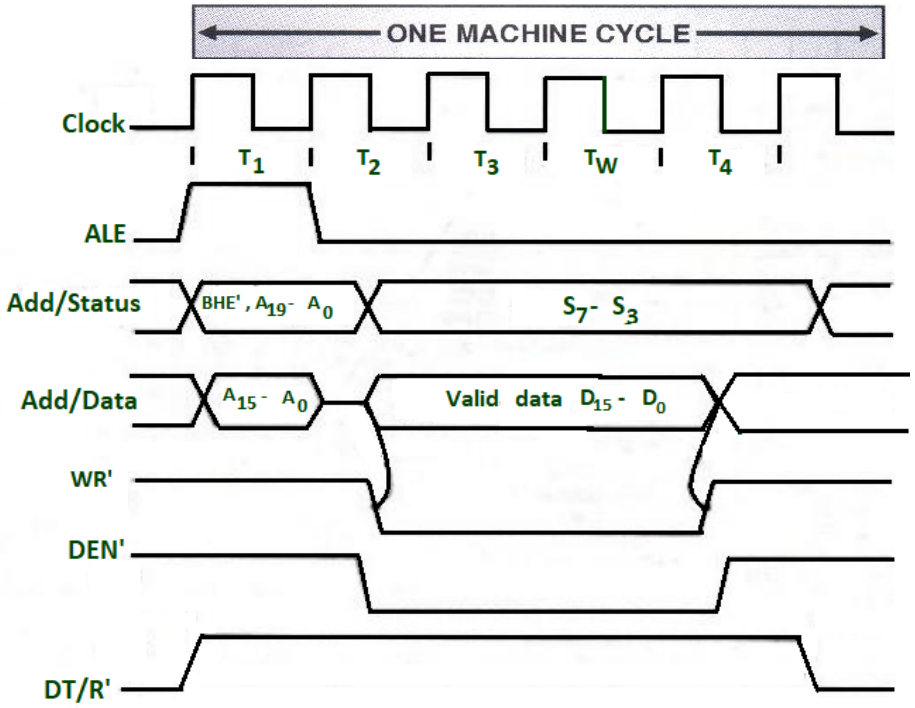


- At T1 state ALE =1 ,this indicates that a valid address is latched on the address bus and also M / IO'= 1, which indicates the memory operation is in progress.

Read M/Cycle in Min Mode

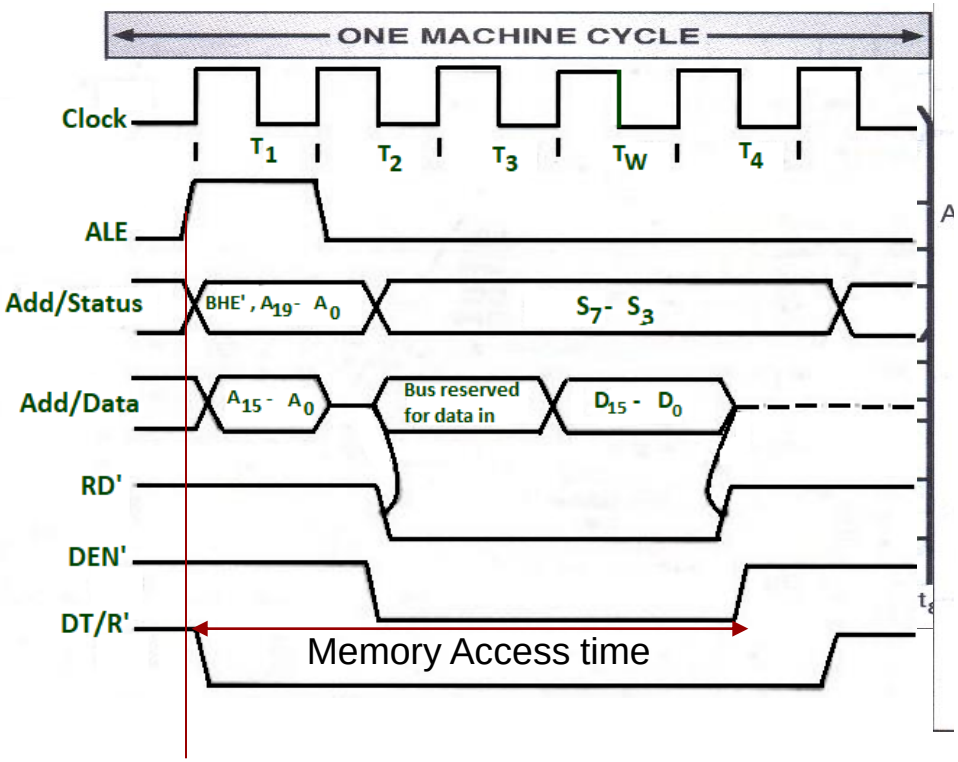


Write M/Cycle in Min Mode

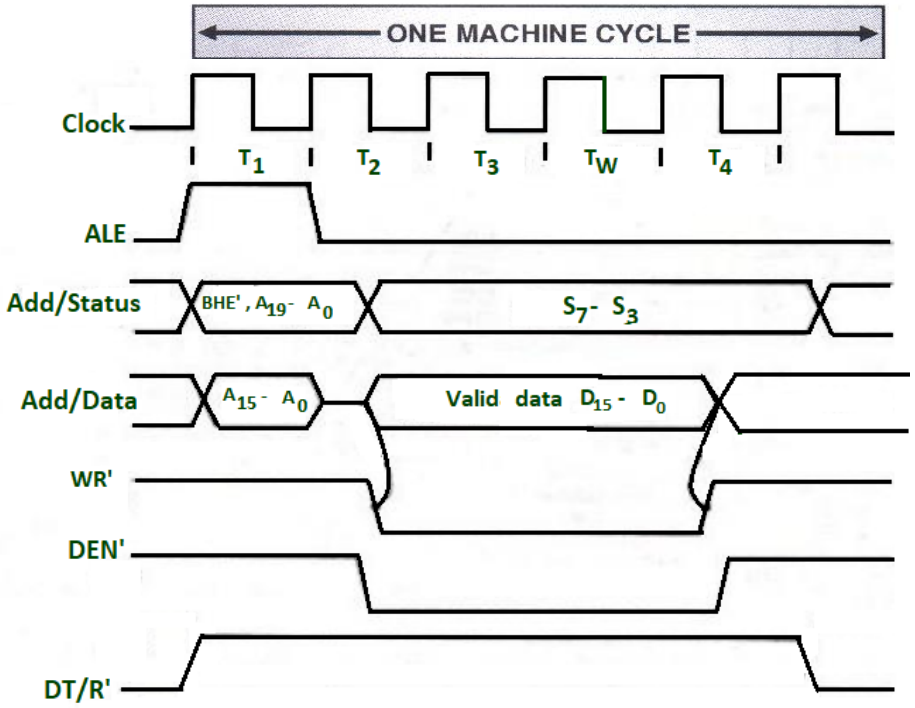


- In T2, the address is removed from the local bus and is sent to the addressed device. Then the bus is tristated.

Read M/Cycle in Min Mode

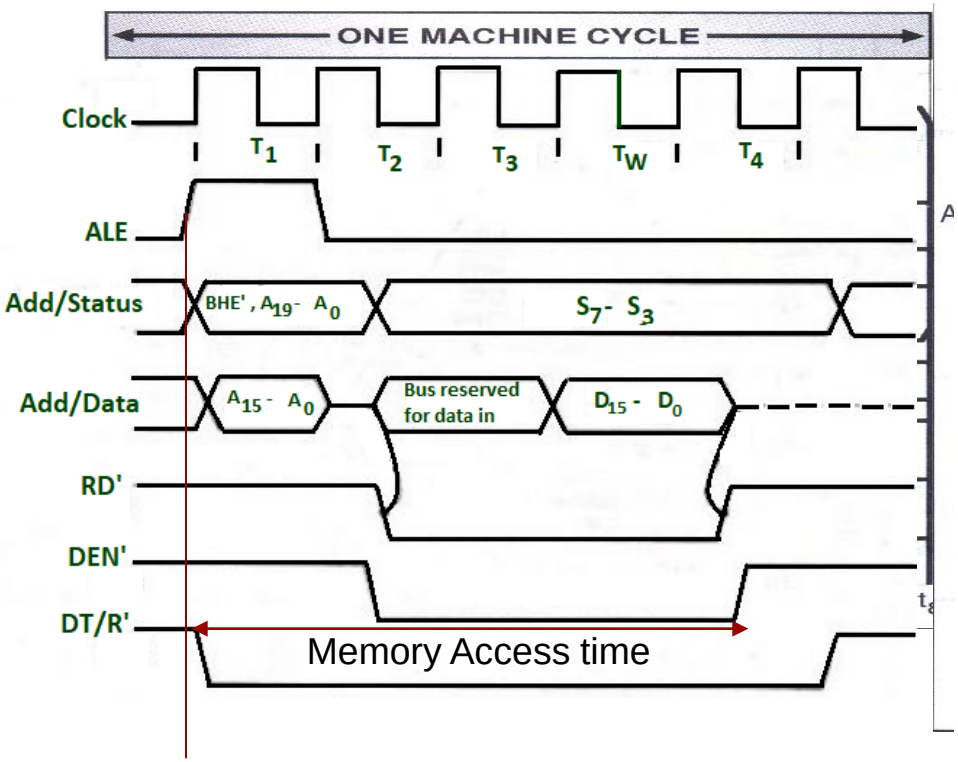


Write M/Cycle in Min Mode

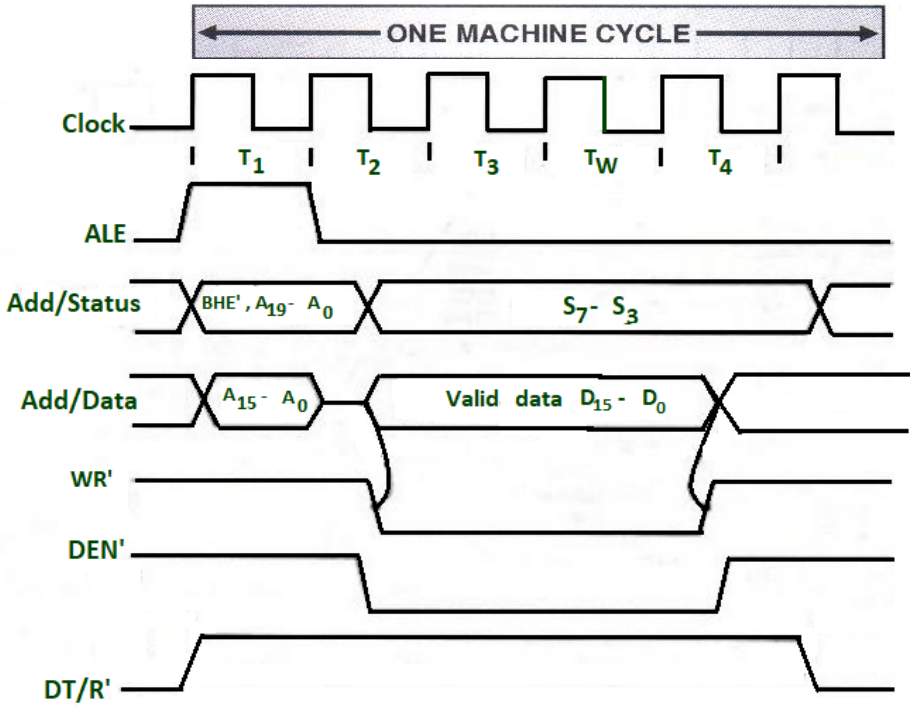


- When RD' = 0 , the valid data is present on the data bus.
- During T2 DEN' =0, which enables transceivers and DT/R' = 0 ,which indicates that the data is received.

Read M/Cycle in Min Mode

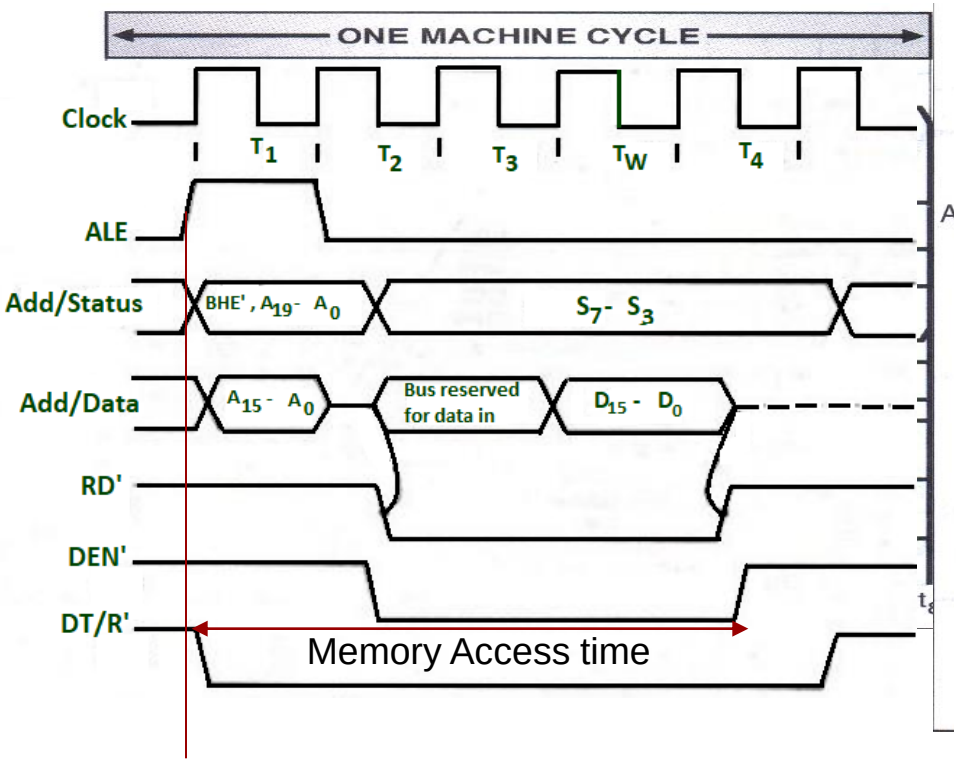


Write M/Cycle in Min Mode

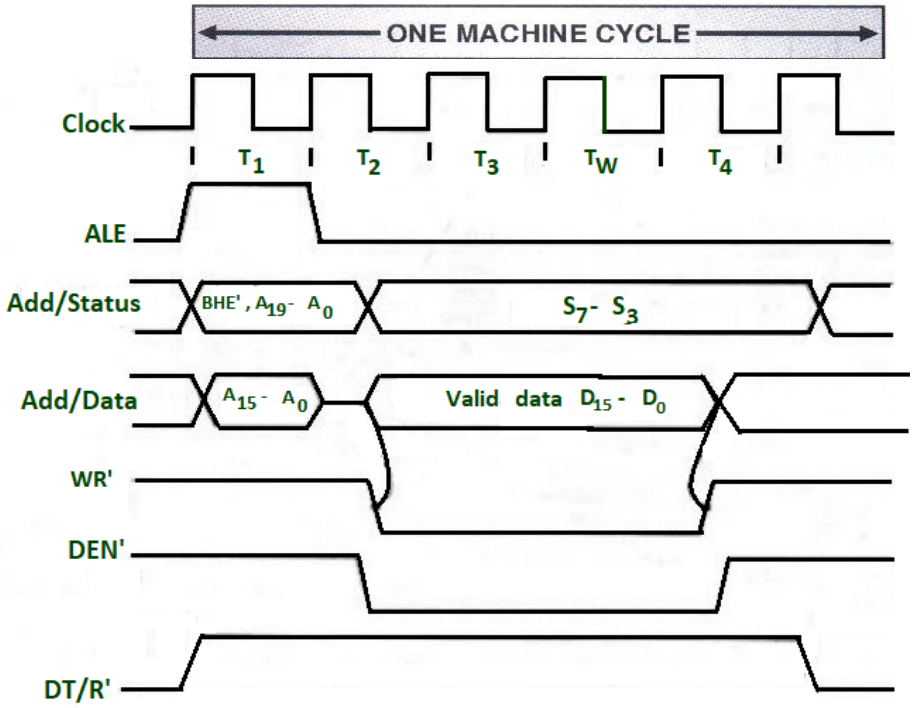


- During T3, data is put on the data bus and the processor reads it.

Read M/Cycle in Min Mode

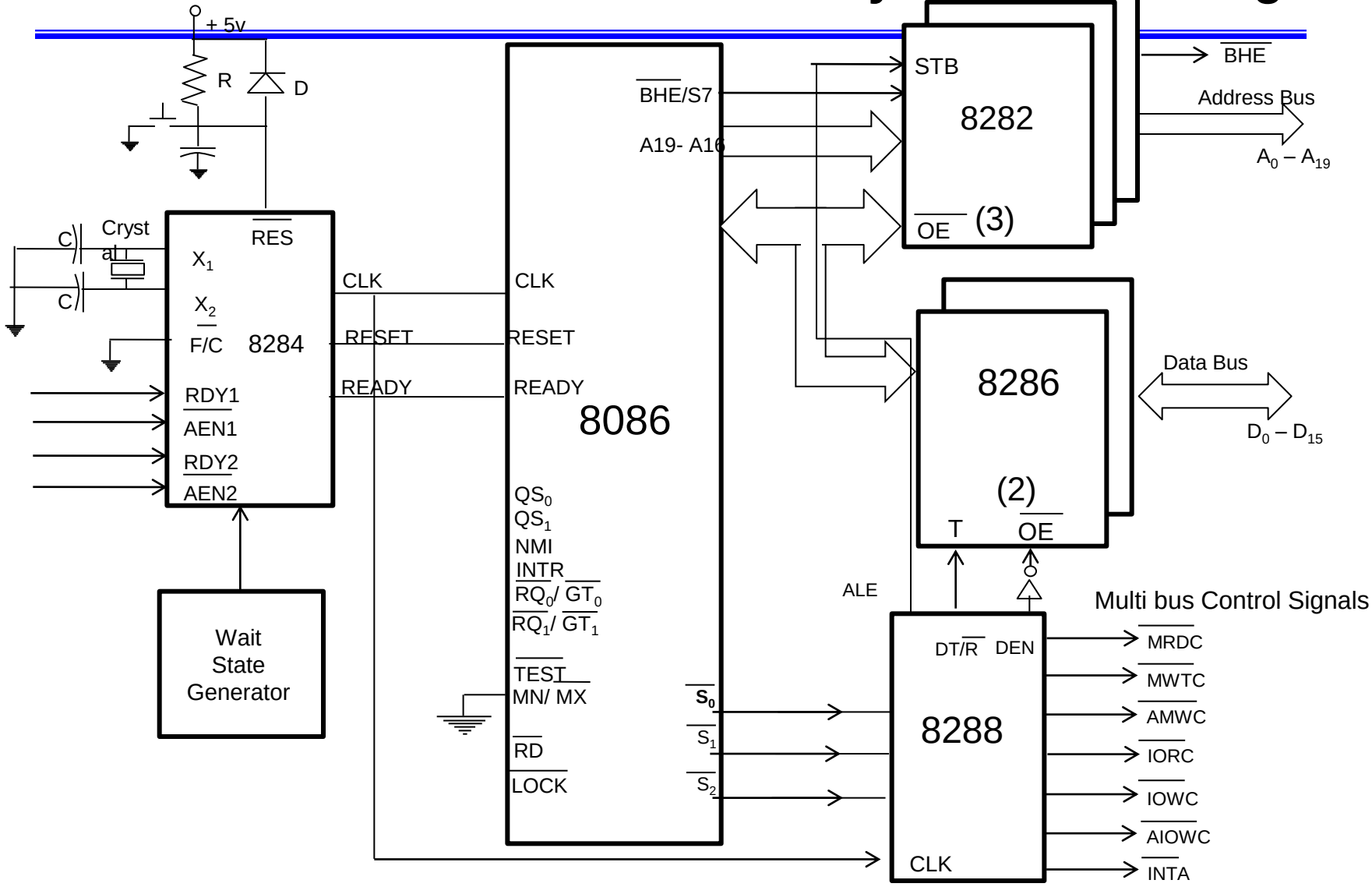


Write M/Cycle in Min Mode



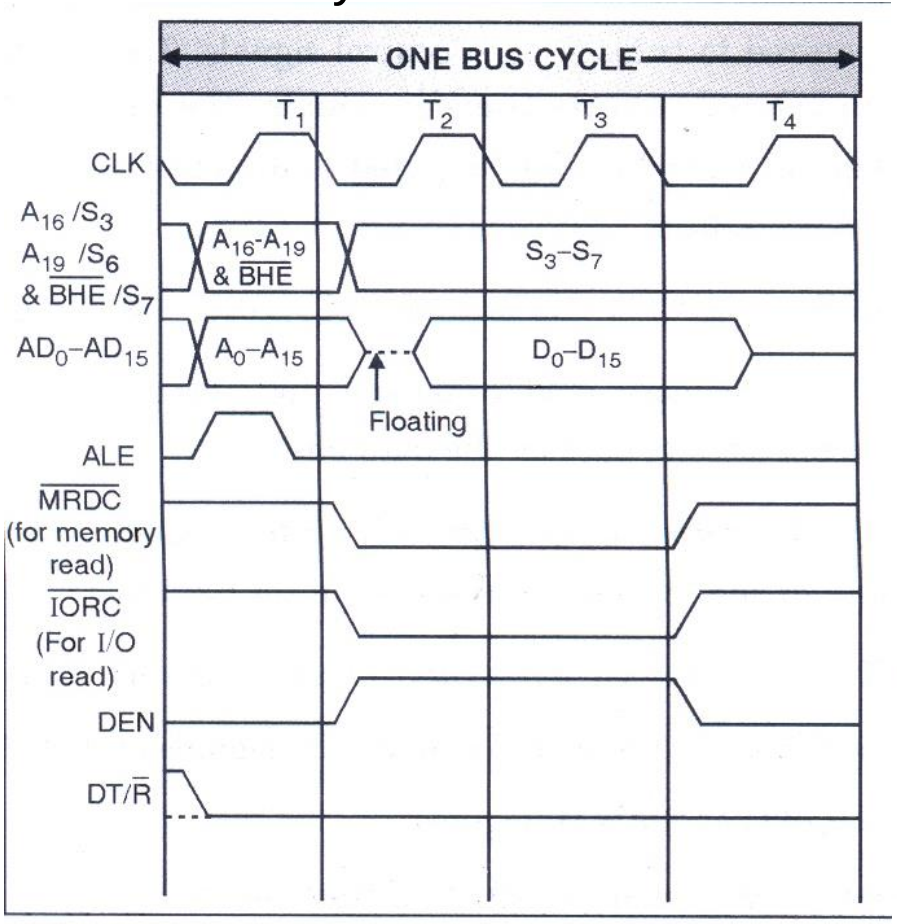
- The output device makes the READY line high.
- This means the output device has performed the data transfer process.
- When the processor makes the read signal to 1, then the output device will again tristate its bus drivers.

8086 – Maximum Mode Maximum System Block Diagram

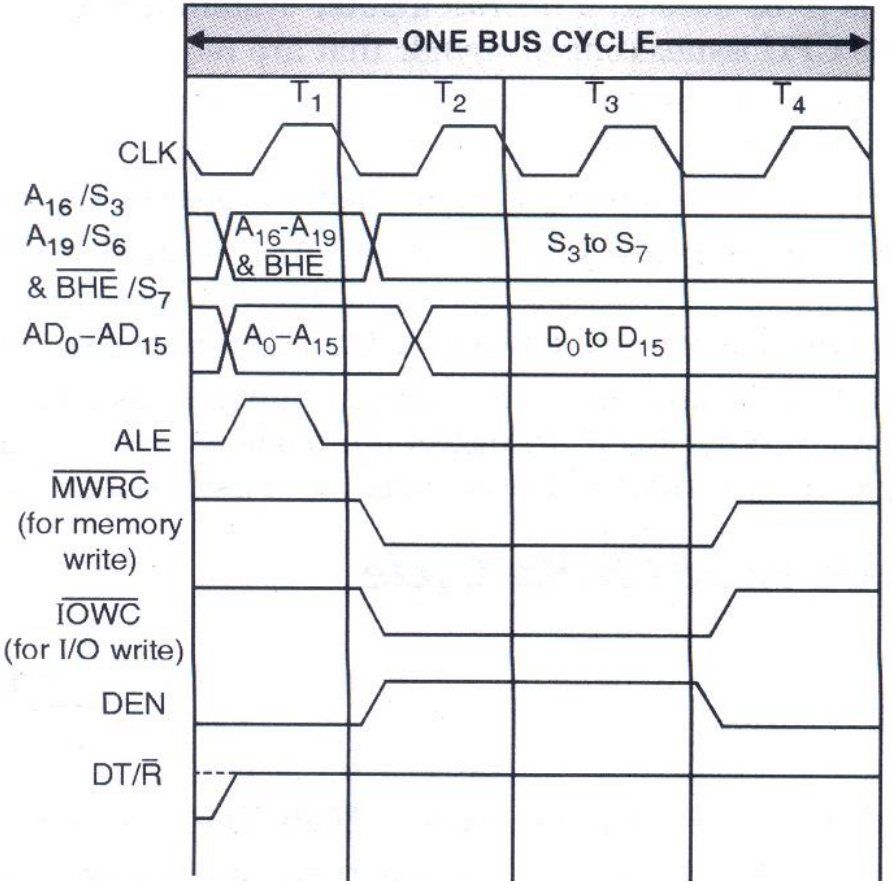


8086

Read M/Cycle in Max Mode



Write M/Cycle in Max Mode



Comparison between Min and Max mode

Minimum Mode 8086	Maximum Mode 8086
There can be only one processor	There can be multiple processor
ALE – Address Latch Enable for the latch is given by 8086	ALE for the latch is given by 8288 bus controller
HOLD and HLDA signals are used for bus request	RQ, GT, RQ^{-}, GT^{-} etc signals are used for bus request
The circuit is simpler	The circuit is more complex
Multiprocessing cannot be performed	Multiprocessing can be performed
Performance is slower.	High performance.

Thank you