Chapter 3

8086 Microprocessor

Pin Configuration & Functions

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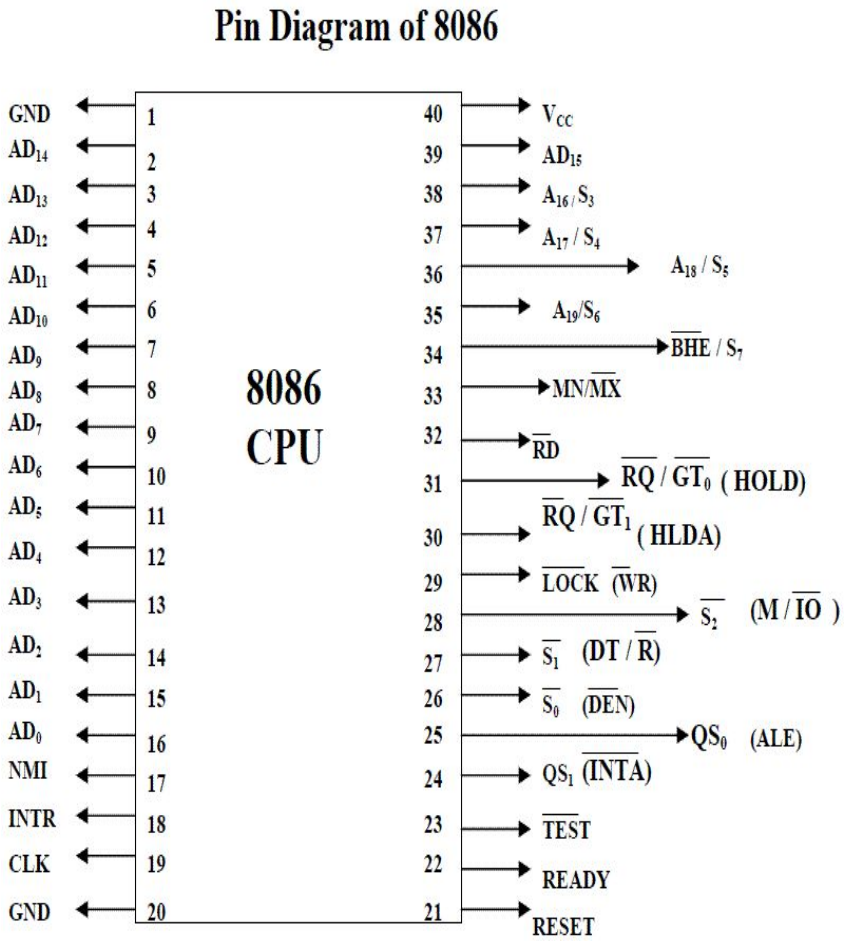
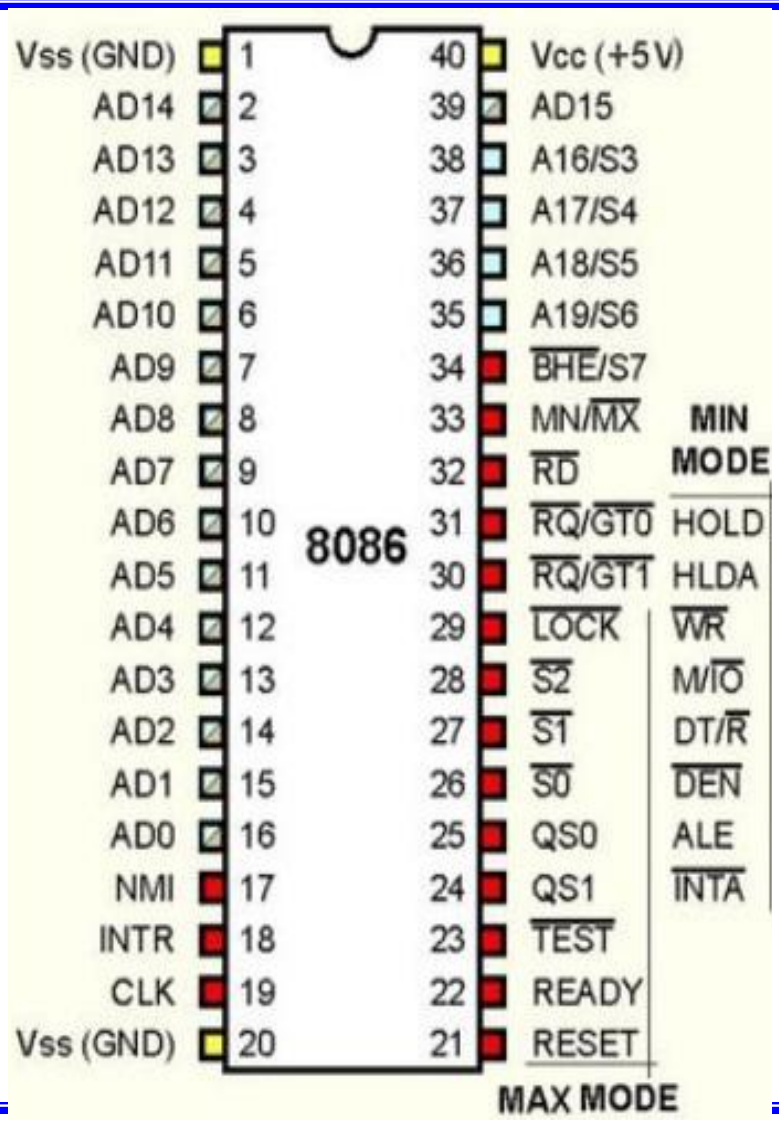
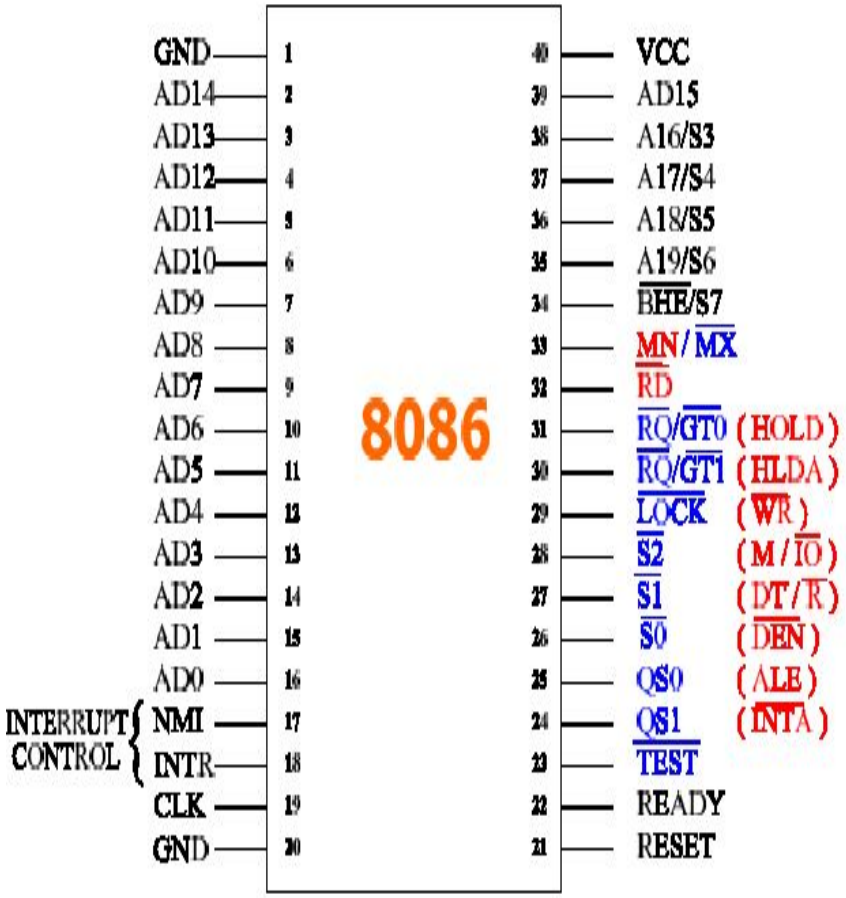
8086 – Pin Configuration



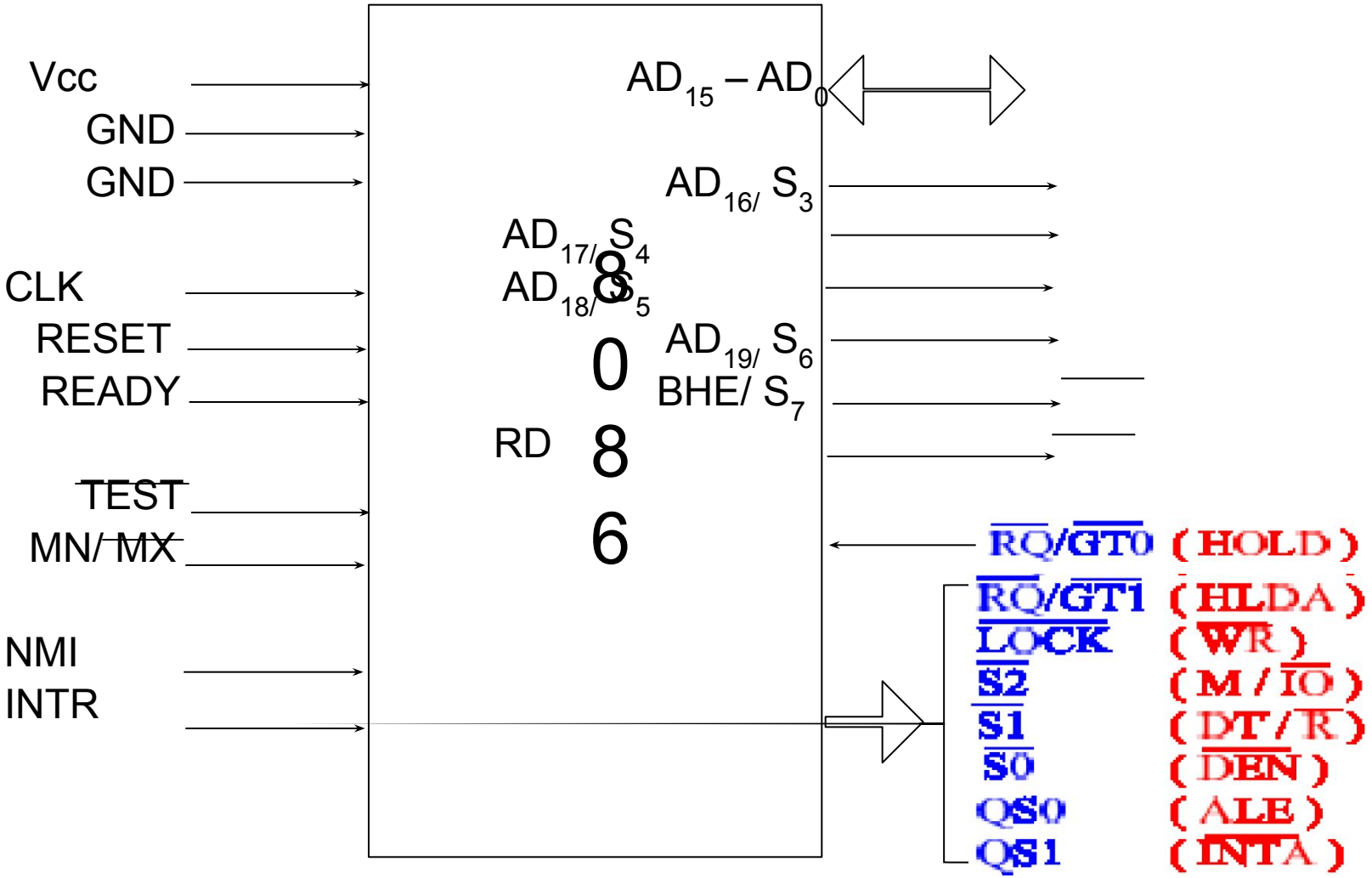


8086 – Pin Configuration

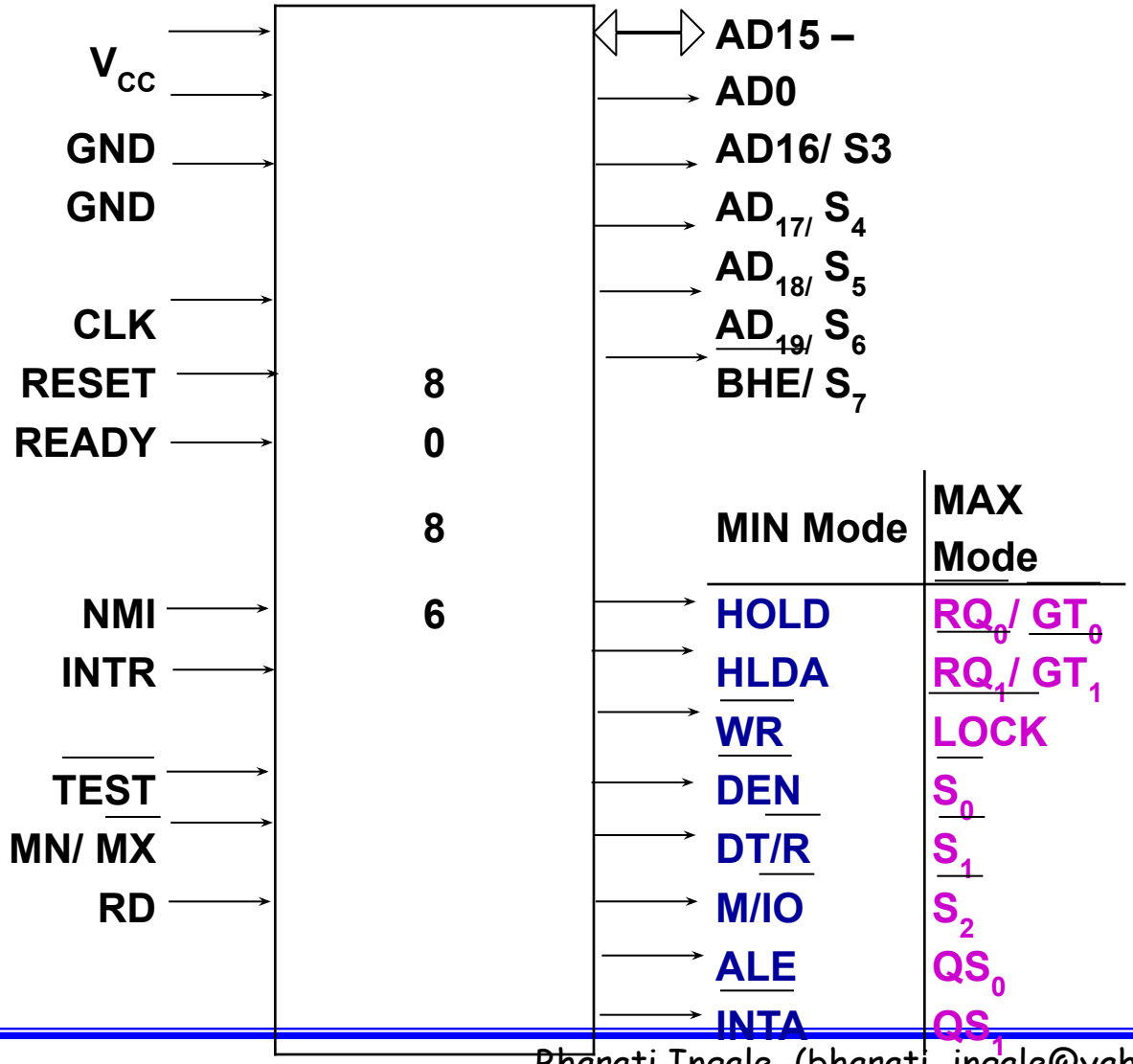
8086 is a 40 pin DIP using MOS technology.



8086 – Functional Pin Diagram



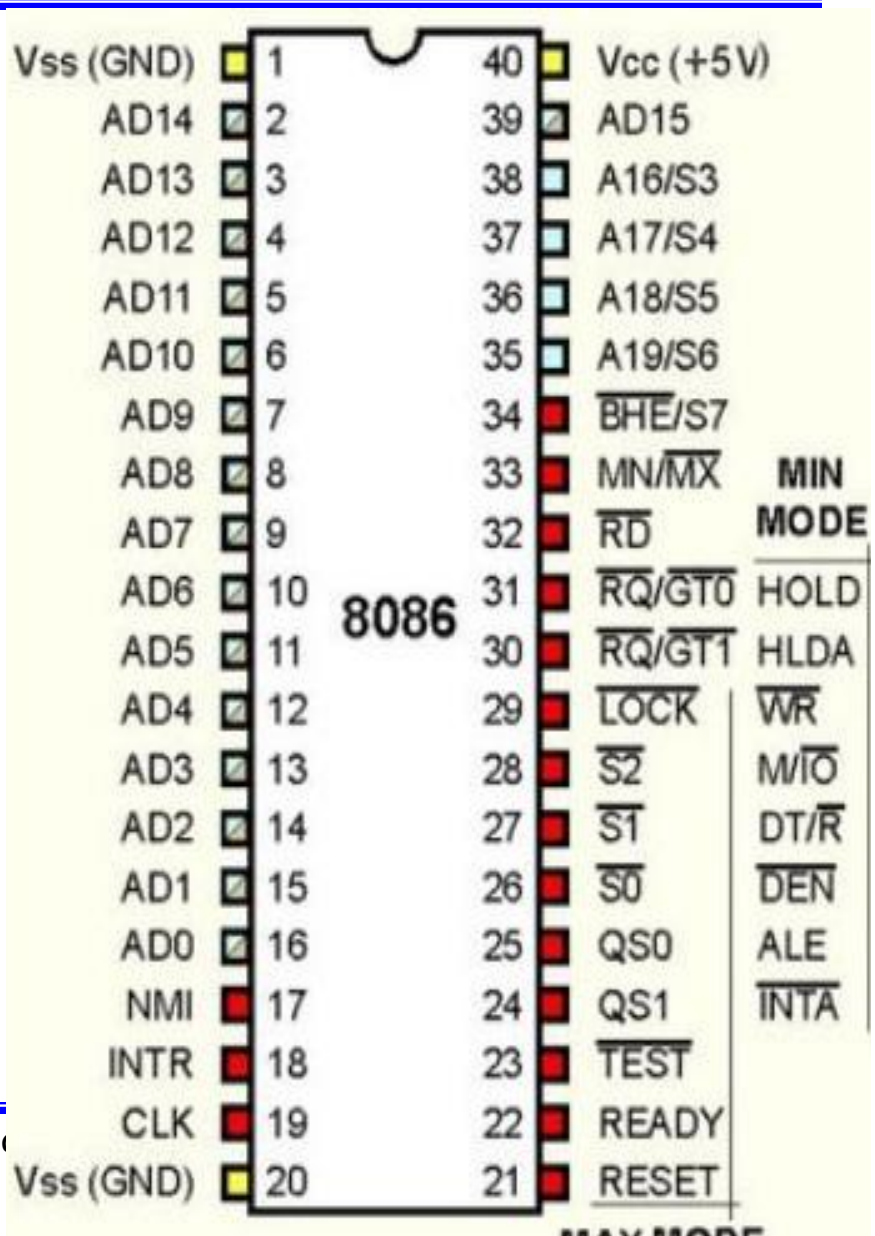
8086 – Functional Pin Diagram



8086 – Pin Configuration

Pin Definitions:

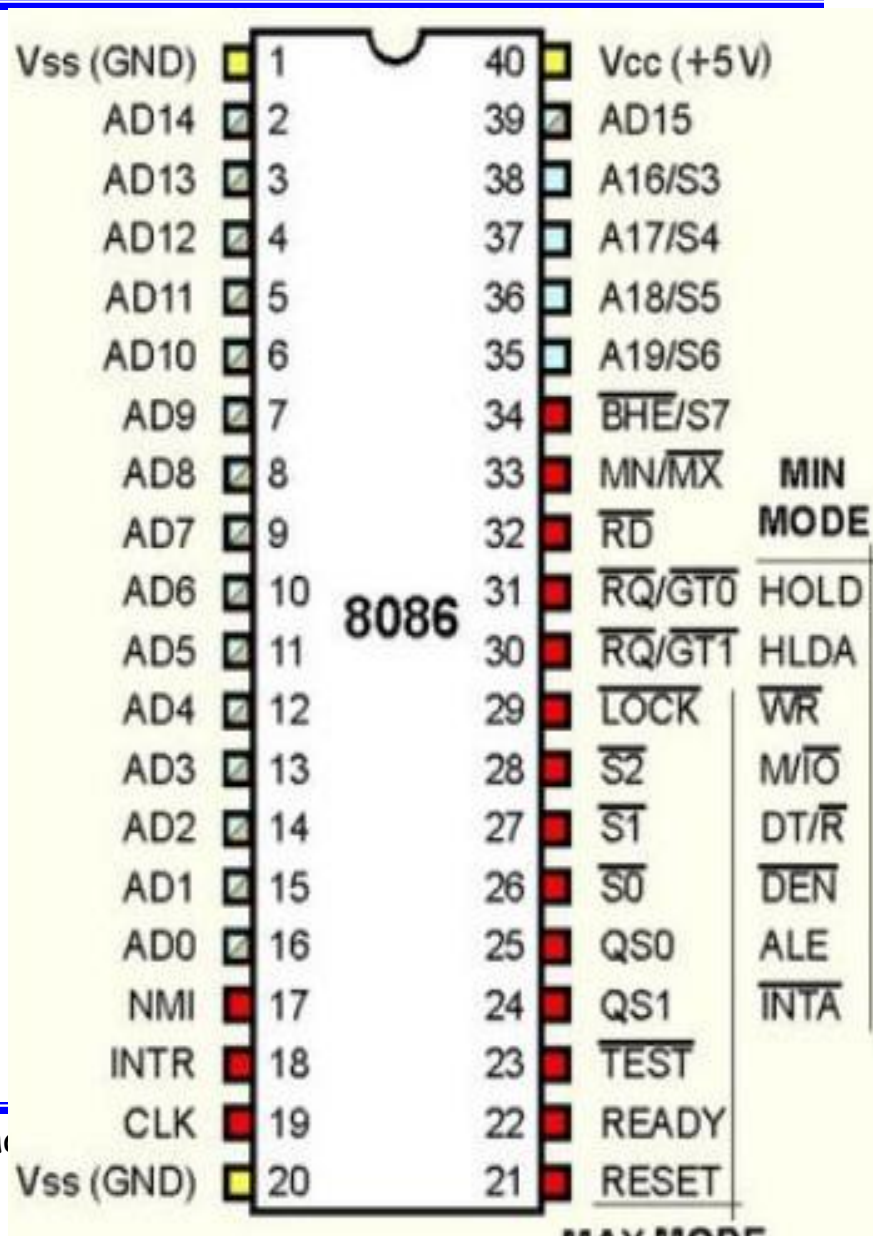
1) Supply pins (3 pins)
2) Clock related pins (3 pins)
3) Address & Data pins (21 pins)
4) Interrupt pins (2 pins)
5) Other Control pins (3 pins)
6) Mode Multiplexed signals (8 pins)



8086 – Pin Configuration

Pin Definitions:

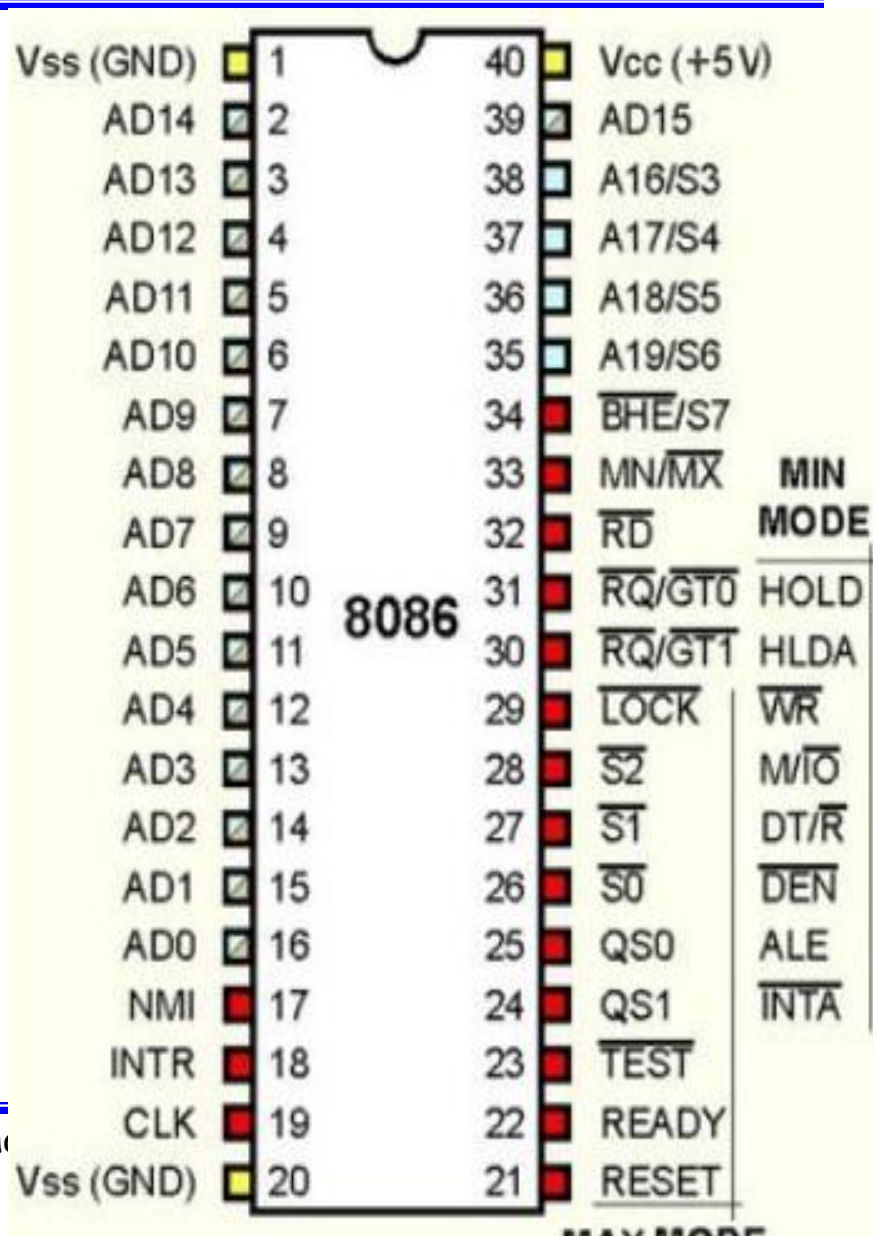
1) Supply pins (3 pins)
   - V_{CC}
   - GND – 2 pins



8086 – Pin Configuration

Pin Definitions:

2) Clock related pins
   (3 pins)
   - CLK
   - RESET
   - READY

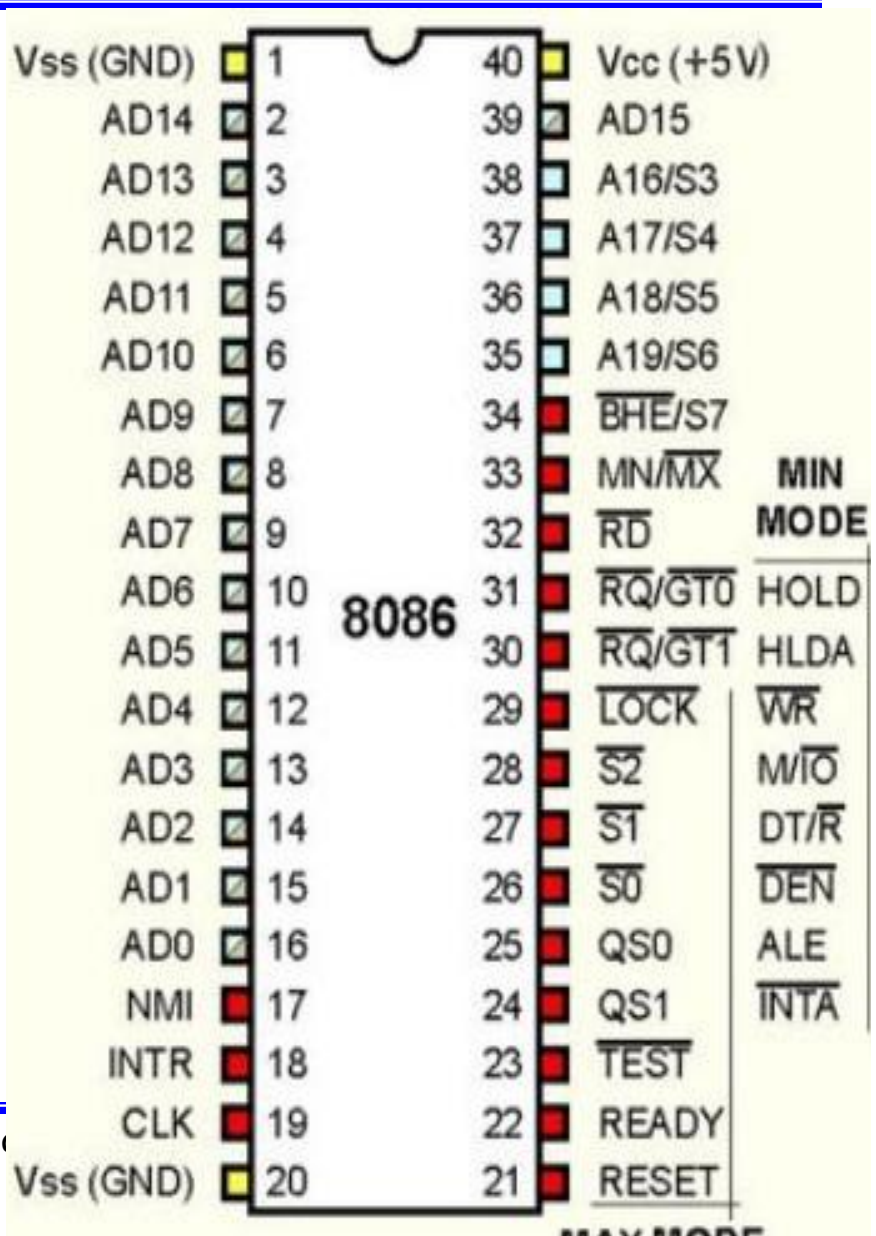


8086 – Pin Configuration

Pin Definitions:

3) Address & Data pins (21 pins)

- $AD_{15} – AD_0$
- AD_{16} /S_3
- AD_{17} /S_4
- AD_{18} /S_5
- AD_{19} /S_6
- ~~BHE~~ $/S_7$



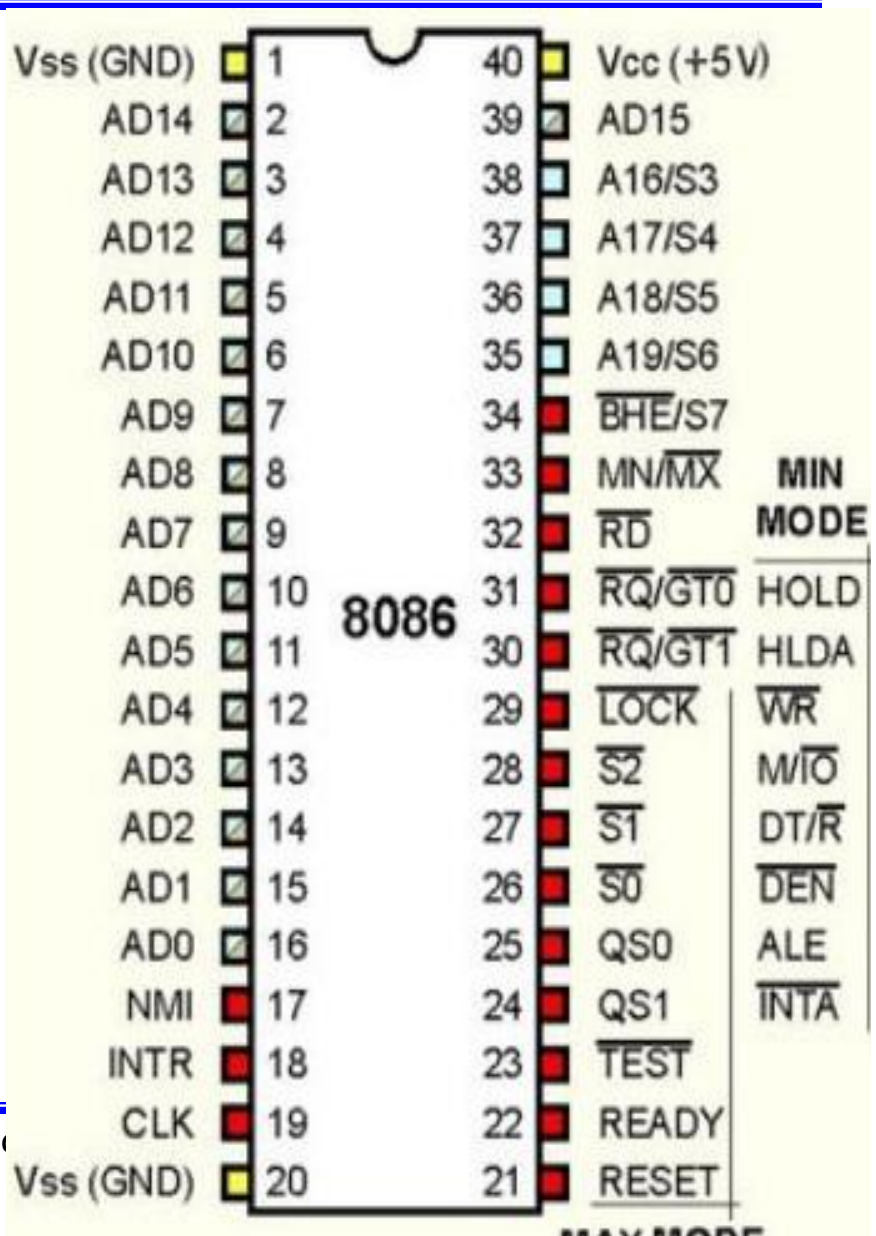
8086 – Segment Selection

S_4	S_3	**Segment Selected**
0	0	Extra Segment
0	1	Stack Segment
1	0	CS/ No Segment Selected
1	1	Data Segment

8086 – Pin Configuration

Pin Definitions:

4) Interrupt pins (2 pins)
   - NMI
   - INTR



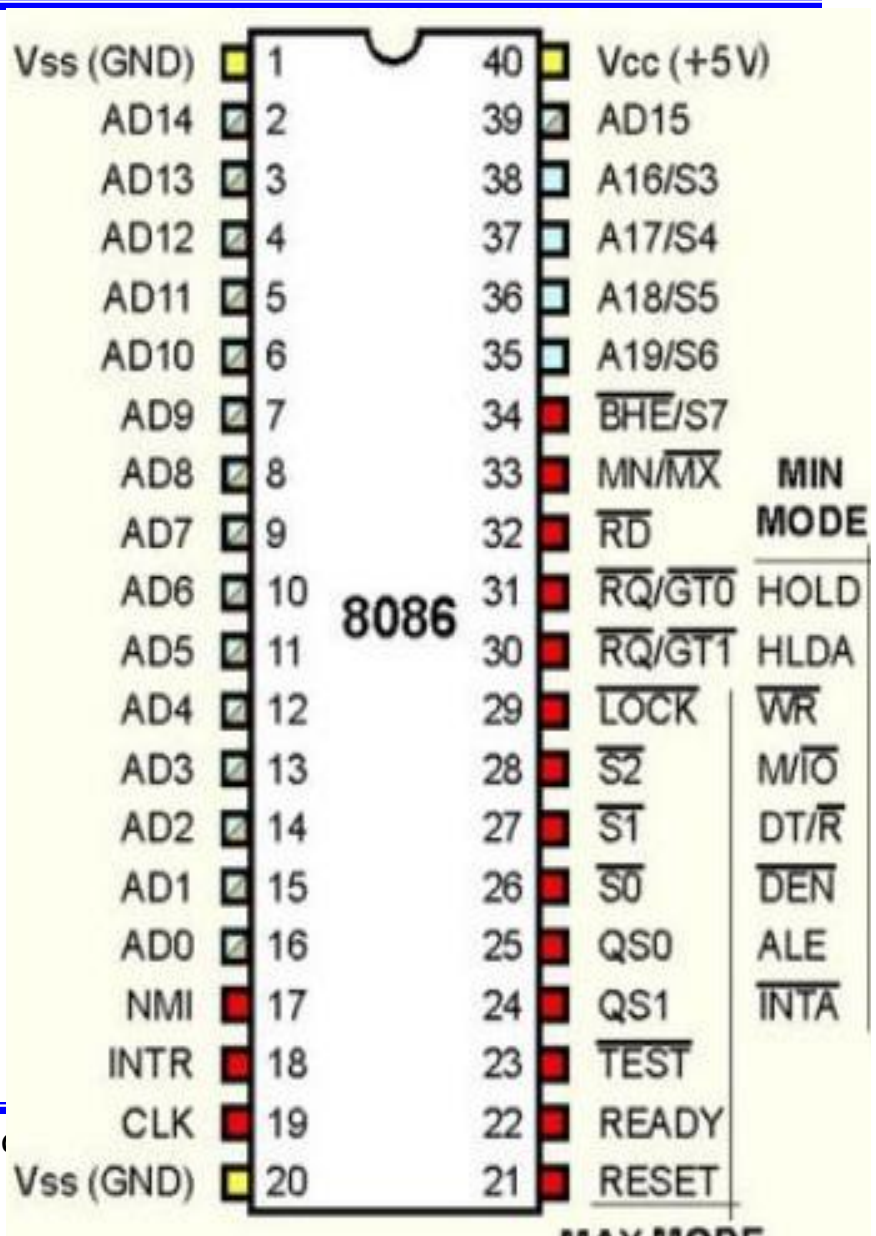
8086 – Pin Configuration

Pin Definitions:

5) Other Control pins

(3 pins)

- ~~TEST~~
- MN/~~MX~~
- ~~RD~~

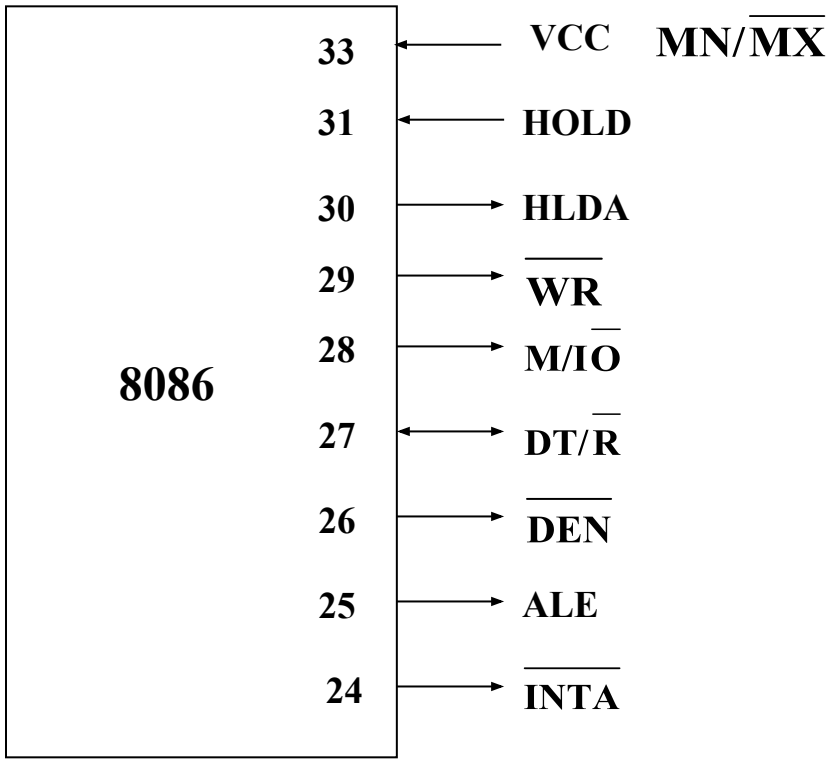


8086 – Pin Configuration

Pin Definitions:

6) Mode Multiplexed signals (8 pins)

MIN Mode	MIN Mode
HOLD	$\overline{DT/R}$
HLDA	M/IO
$\overline{WR}$	ALE
DEN	$\overline{INTA}$

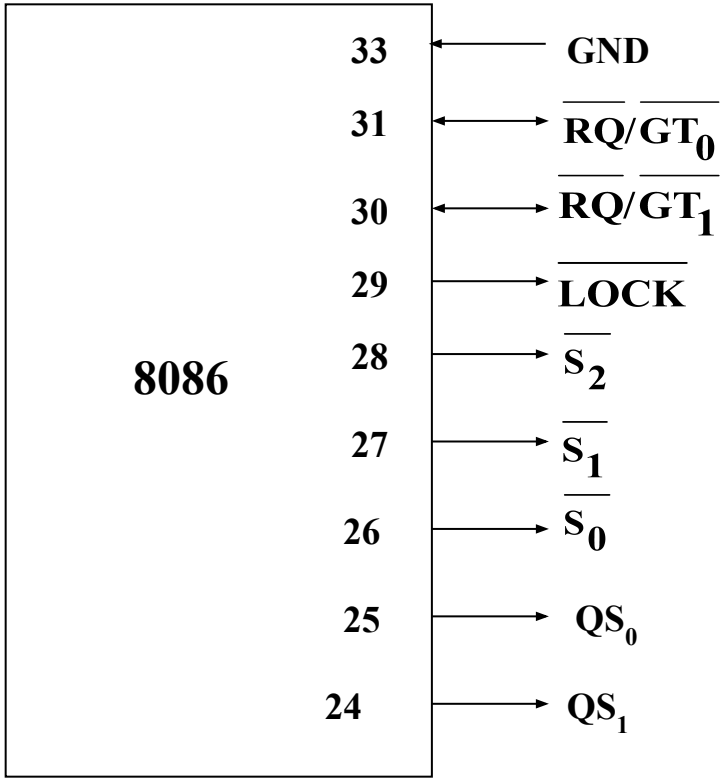


8086 – Pin Configuration

Pin Definitions:

6) Mode Multiplexed signals (8 pins)

MAX Mode	MAX Mode
$\overline{RQ_0}$/ $\overline{GT_0}$	$\overline{S_1}$
$\overline{RQ_1}$/ $\overline{GT_1}$	S_2
$\overline{LOCK}$	QS_0
S_0	QS_1



8086 – Machine Cycle

S_2	S_1	S_0	**Bus Cycle/ Machine Cycle**
0	0	0	$\overline{\text{INTA}}$ Cycle
0	0	1	I/O Read
0	1	0	I/O Write
0	1	1	Halt
1	0	0	Opcode Fetch
1	0	1	Memory Read
1	1	0	Memory Write
1	1	1	Inactive

8086 – Queue Operation

QS_1	QS_0	**Segment Selected**
0	0	NOP
0	1	Opcode Fetch from Queue
1	0	Queue is cleared
1	1	Fetch remaining instruction bytes from Queue.

Thank You