

注意

1. 一律將此檔轉成 PDF 檔繳交
2. 繳交期限為
3. 隔週三上午九點
4. 一人繳交一份
5. 檔名：學號_HW?.pdf
6. 檔名請按照作業檔名格式進行填寫
7. 未依照格式不予批改

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實驗五

姓名：黃文祺 學號：01057013

班級：資工 3A

E-mail：OOOOOOOOO


```

36     .HEX0(),
37     .HEX1(),
38     .HEX2(),
39     .HEX3(),
40     .HEX4(),
41     .HEX5(),
42
43     //////////// KEY ////////////
44     .KEY      (KEY),
45     .RESET_N  (rst_n),
46
47     //////////// LED ////////////
48     .LEDR     (LEDR),
49
50
51     //////////// SW ////////////
52     .SW       (SW)
53 );
54
55 //assign KEY[0] = rst_n;
56
57
58 task noise_gen; begin
59     for (i=0; i<25; i=i+1) begin
60         #100     enc = 0;    //noise
61         #100     enc = 1;
62     end
63 end
64 endtask
65
66
67
68 always #10 CLOCK_50 = ~CLOCK_50;
69
70 always begin
71
72     noise_gen;
73
74
75     #10000 enc = 0;    // signal
76
77     noise_gen;
78
79     #10000 enc = 1;    // signal
80
81     noise_gen;
82
83     #20000 enc = 0;    // signal
84     #20000 enc = 1;
85     //
86     noise_gen;
87
88     #10000 enc = 0;    // signal
89
90     noise_gen;
91
92     #15000 enc = 1;    // signal
93
94     noise_gen;
95
96     #25000 enc = 0;    // signal
97     #27000 enc = 1;
98
99
100
101 end
102
103 assign SW[0] = enc;
104
105
106 initial begin
107     CLOCK_50 = 0;
108     rst_n = 0;
109     enc = 0;
110
111     #20 rst_n = 1;;
112
113     #500000 $stop;
114 end
115
116
117 endmodule

```

SignalPeriodCnt.sv (延續之前作業名稱複製的，沒改名稱@@)

```
C:\Users\user\Desktop\HW5\signal\design\SignalPeriodCnt.sv - Notepad++
檔案(F) 編輯(E) 搜尋(S) 檢視(V) 編碼(N) 語言(L) 設定(T) 工具(O) 巨集(M) 執行(R) 外掛(P) 視窗(W) ?
雙色點陣2種顏色測試.c 雙色點陣雙色交替動態顯示.c testbench_DEMO.sv SignalPeriodCnt.sv seven_segment.sv Low_Pass_Filter_4ENC.sv frequency_divider.sv Posedge[< >]
1 module SignalPeriodCnt(
2     input clk_50M,
3     input rst,
4     input enc,
5     output logic [31:0] cnt_meas
6 );
7
8     logic enc_filter;
9     logic enc_pos;
10    logic [31:0] cnt; //proj 的 cnt
11    logic rst_cnt, enable_cnt;
12    logic load_cnt;
13    logic step_col;
14    logic [31:0] mul_result;
15    logic [31:0] mul_cnt; //proj2 的 cnt
16    logic rst_mul_cnt, enable_mul_cnt;
17    logic load_mul_result;
18    logic [10:0] r_distance;
19    logic [2:0] enc_pos_test; //讓 mul_cnt到第二個enc_pos再計數
20
21    typedef enum logic[2:0] {
22        START,
23        POSEDGE,
24        MUL_RESULT,
25        CNT
26    } state_t;
27
28    state_t ps, ns;
29
30
31    // Low pass filter
32    Low_Pass_Filter_4ENC Lpf1(
33        .clk(clk_50M),
34        .reset(rst),
35        .signal(enc),
36        .r_LPF_threshold_enc(20),
37        .sig_filter(enc_filter)
38    );
39
40    // positive edge detector
41    PosedgeDetector Pd1(
42        .clk_50M(clk_50M),
43        .rst(rst),
44        .enc_filter(enc_filter),
45        .enc_pos(enc_pos)
46    );
47
48
49
50
51    // mul_cnt
52    always_ff @(posedge clk_50M) begin
53        if(rst_mul_cnt)
54            mul_cnt <= 0;
55        else if(enable_mul_cnt)
56            mul_cnt <= mul_cnt + 1;
57    end
58    // r_distance
59    assign r_distance = 173;
60
61    //mul_cnt_dff
62    always_ff @(posedge clk_50M) begin
63        if(rst)
64            mul_result <= 0;
65        if(load_mul_result)
66            mul_result <= cnt_meas * r_distance / 4233;
67    end
68
69
70    // cnt
71    always_ff @(posedge clk_50M) begin
72        if(rst_cnt)
73            cnt <= 0;
74        else if(enable_cnt)
75            cnt <= cnt + 1;
76    end
77
78    // cnt_dff
79    always_ff @(posedge clk_50M) begin
80        if(!rst)
81            cnt_meas <= 0;
82        else if(load_cnt)
83            cnt_meas <= cnt;
84    end
85
86    // fsm
87    always_ff @(posedge clk_50M) begin
88        if(!rst)
89            ps <= START;
90        else
91            ps <= ns;
92    end
93 end
```

```

93
94 always_comb begin
95     rst_cnt      = 0;
96     load_cnt     = 0;
97     enable_cnt   = 0;
98     step_col     = 0;
99     rst_mul_cnt  = 0;
100    load_mul_result = 1;
101    enable_mul_cnt = 0;
102
103    if(!rst)
104        enc_pos_test<=0;    // 讓 mul_cnt到第二個enc_pos再計數
105
106    ns      = ps;
107
108    case(ps)
109    START: begin
110        rst_cnt      = 1;
111        rst_mul_cnt  = 1;
112        ns      = CNT;
113    end
114
115    CNT: begin
116        if(enc_pos)
117            ns      = POSEDGE;
118
119        if (enc_pos_test!=2)    // 讓 mul_cnt到第二個enc_pos再計數
120            rst_mul_cnt=1;
121
122        if(mul_cnt>=mul_result & mul_cnt > 0 ) begin
123            step_col      =1;
124            rst_mul_cnt =1;
125        end
126
127        enable_cnt      =1;
128        enable_mul_cnt  =1;
129    end
130
131    POSEDGE: begin
132        load_cnt = 1;
133        rst_cnt  = 1;
134
135        enc_pos_test=enc_pos_test+1;    //----- //
136        if(enc_pos_test>1)              // 讓 mul_cnt到第二個enc_pos再計數 //
137            enc_pos_test=2;              //----- //
138
139        ns      = CNT;
140    end
141
142    endcase
143 end
144 endmodule
145

```

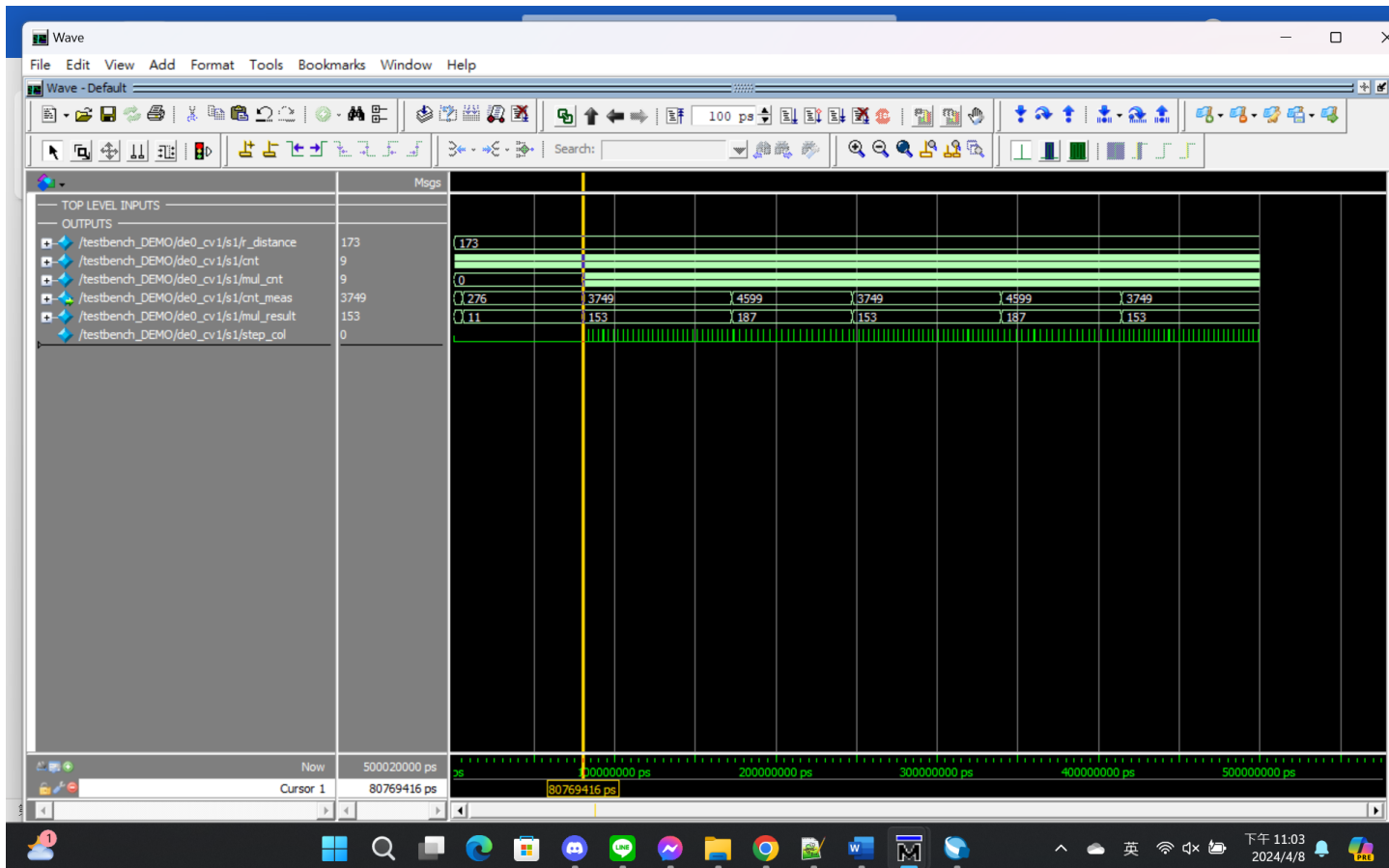
PosedgeDetector.sv

```

C:\Users\user\Desktop\HW5\signal\design\PosedgeDetector.sv - Notepad++
檔案(F) 編輯(E) 搜尋(S) 檢視(V) 編碼(N) 語言(L) 設定(T) 工具(O) 巨集(M) 執行(R) 外掛(P) 視窗(W) ?
雙色點陣雙色交替動態顯示.c testbench_DEMO.sv SignalPeriodCntsv seven_segment.sv Low_Pass_Filter_4ENC.sv frequency_divider.sv PosedgeDetector.sv DE0_CV.sv
1 module PosedgeDetector(
2     input clk_50M,
3     input rst,
4     input enc_filter,
5     output reg enc_pos
6 );
7
8     logic s_signal;
9     logic d_signal;
10
11    // posedge of encoder
12    always_ff @(posedge clk_50M) begin
13        if (!rst) begin
14            s_signal <= 1;
15            d_signal <= 1;
16            enc_pos <= 0;
17        end else begin
18            {d_signal, s_signal} <= {s_signal, enc_filter};
19            enc_pos <= s_signal & ~d_signal;
20        end
21    end
22 endmodule

```

■ 模擬結果與結果說明：



1. 這次作業的 cnt 是 mul_cnt，第一個 cnt 是 proj1 的 cnt
 2. 黃線以前處理乾淨了(cnt 和 mul_cnt 比較)
- SignalPeriodCnt 註解 //讓 mul_cnt 到第二個 enc_pos 再計數

■ 結論與心得：

Demo3 結束後其實數據就差不多了，但要注意的就是 cnt 不是作業 4 的 cnt 然後就是 mul_cnt 要稍微做一點改變，才能和作業 5 的模擬範例一樣。owob