

注意

1. 繳交時一律轉 PDF 檔
2. 繳交期限為
下周上課前
3. 一人繳交一份
4. 檔名請按照作業檔名格式進行填寫
未依照格式不予批改

2024/02/21

實驗一 軟體截圖

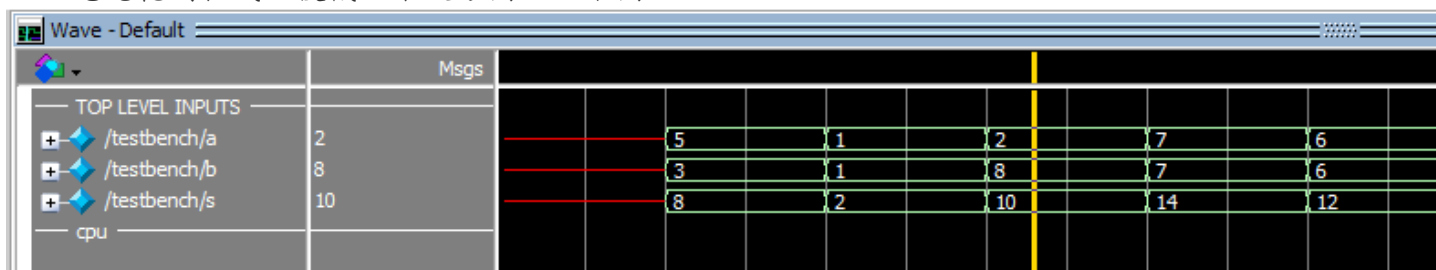
姓名：黃文祺 學號：01057013

班級：資工 3A

E-mail：OOOOOOOOO

實驗說明：

- 請按照教材中的說明下載並安裝 Quartus19.1 與 modelsim。
- 完成後截圖軟體 icon 及啟動畫面。
- 下載助教給的範例程式，跟著教學影片中的 modelsim 使用教學跑一遍程式。
- 跑完範例程式之後截結果波形圖，如下圖。



軟體 icon 及啟動畫面截圖：



Quartus Prime Lite Edition

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Hierarchy

Compilation Hierarchy

Home

Recent Projects

DE0_CV.qpf (C:/Users/user/Desktop/DE0_CV/DE0_CV.qpf)

New Project Wizard

Open Project

Compare Editions

Buy Software

Documentation

Training

Support

What's New

Notifications

Close page after project load

Don't show this screen again

IP Catalog

Device Family Cyclone V (E/GX/GT/SX/SE/ST)

Installed IP

Project Directory

No Selection Available

Library

Basic Functions

DSP

Interface Protocols

Memory Interfaces and Controllers

Processors and Peripherals

University Program

Search for Partner IP

Tasks

RTL Simulation

Task

Time

Analysis & Elaboration

RTL Simulation

Find...

Find Next

Messages

System

Processing

Connecting to Intel FPGA web site...

Quartus Prime Lite Edition - C:/Users/user/Desktop/DE0_CV/DE0_CV - DE0_CV

File Edit View Project Assignments Processing Tools Window Help

DE0_CV

Project Navigator

Files

design/adder_4bit.v

design/DE0_CV.v

DE0_CV.SDC

Table of Contents

Flow Summary

Flow Status

Successful - Wed Feb 21 14:59:04 2024

Quartus Prime Version

19.1.0 Build 670 09/22/2019 SJ Lite Edition

Revision Name

DE0_CV

Top-level Entity Name

DE0_CV

Family

Cyclone V

Device

5CEBA4F23C7

Timing Models

Final

Logic utilization (in ALMs)

N/A until Partition Merge

Total registers

N/A until Partition Merge

Total pins

N/A until Partition Merge

Total virtual pins

N/A until Partition Merge

Total block memory bits

N/A until Partition Merge

Total PLLs

N/A until Partition Merge

Total DLLs

N/A until Partition Merge

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Installed IP

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RTL Simulation

Task

Time

Analysis & Elaboration 00:00:07

RTL Simulation 00:00:07

Find...

Find Next

Messages

System

Processing (13)

Info: Generated ModelSim-Altera script file C:/Users/user/Desktop/DE0_CV/simulation/modelsim/DE0_CV_run_msim_rtl_verilog.do

Info: Spawning ModelSim-Altera Simulation software

Info: Successfully spawned ModelSim-Altera Simulation software

Info: NativeLink simulation flow was successful

Info: For messages from NativeLink scripts, check the file C:/Users/user/Desktop/DE0_CV/DE0_CV_nativeLink_simulation.rpt

23030 Evaluation of Tcl script c:/intelfpga_lite/19.1/quartus/common/tcl/internal/nativeLink/qnativesim.tcl was successful

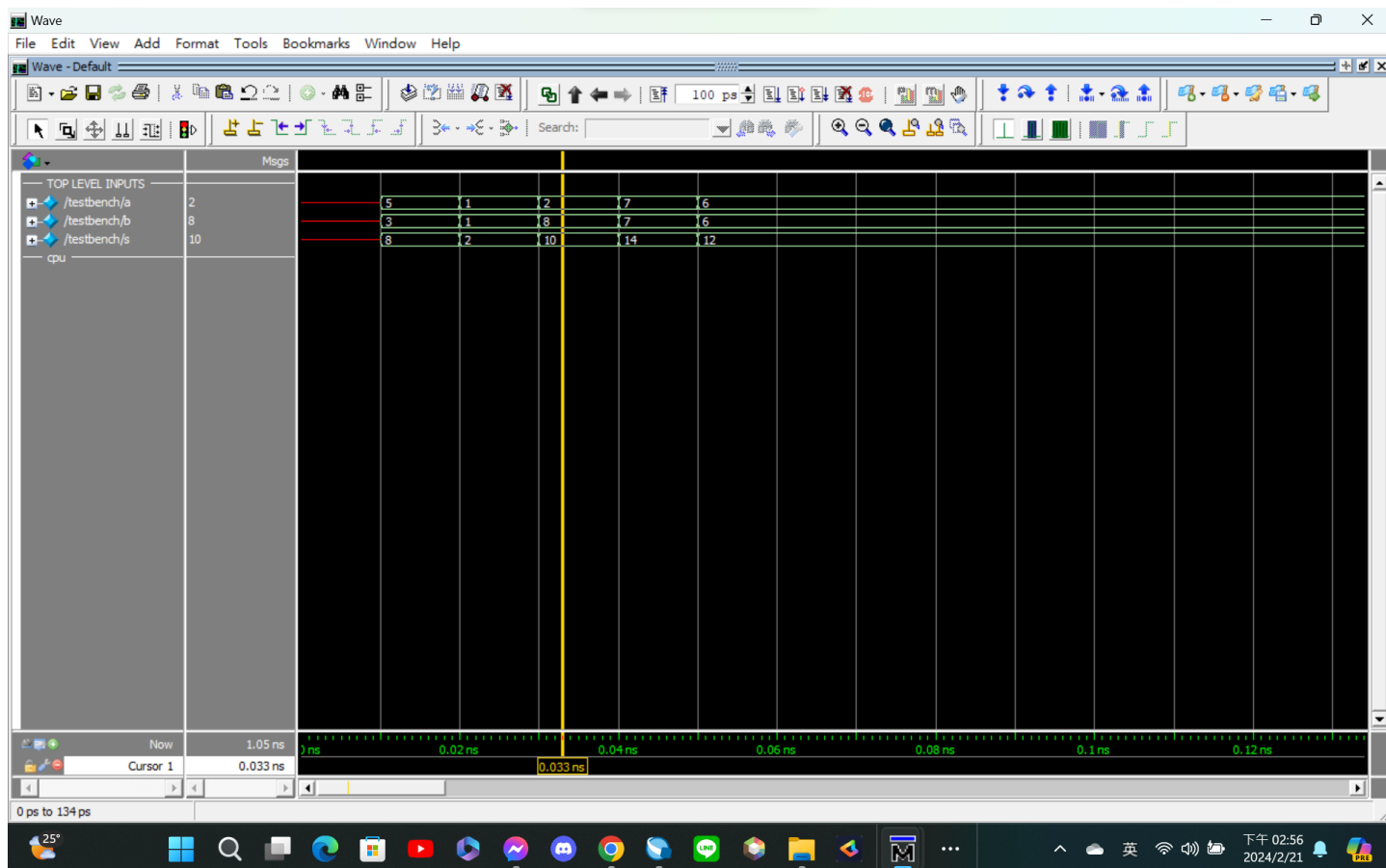
Quartus Prime Shell was successful. 0 errors, 1 warning

25°

下午 02:59

2024/2/21

🧑 模擬結果截圖：



🧑 結論與心得：

雖然之前計算機系統設計做下載過了，但這學期有換電腦，所以還是重新下載了一次，基本設定跟使用都沒問題，上學期的還沒忘記，這學期也麻煩助教了！