CPS2390 Midterm Exam
WKU Fall 2015

Name： StudentID： Score：

一 True/False questions (1 point each, 20 points)

1. (F)If numbers are to be represented with 10 bits, we can represent more unique numbers if we use an unsigned integer representation than if we use signed integer representations.

2. (T) If we add the 2's complement representation of a number to itself, and if the sign bit does not change, the result will simply be the same as if we had shifted the original number one bit to the left, and inserted a 0 at the right end.

3. (F) The exponent of an IEEE Floating point number is encoded in 2's complement representation

4. (F)The ASCII code for semicolon is formed by adding the ASCII codes for period and comma.

5. (T)The floating point data type allows us to represent both much larger and much smaller numbers than is possible with 2's complement integers.

6. (F)All 8-bit address spaces are byte addressable

7. (F) An 8-bit register contains a value, the value 1 is written into it, the original value can still be recovered

8. (F) If a memory has addressability of 4 bits then we need 2 bits to specify the address space

9. (F)It is not possible to have a 1 bit register

10. (T)The two outputs of a latch are always the complement of each other

11. (T)Most ISA's provides some small temporary storage very close to the ALU to allow the results to be temporarily stored if they will be needed to produce results in the near future.

12. (F)All instructions require all six phases of the instruction cycle to be carried out. That is, at least one clock cycle must be devoted to carrying out the work of each phase of each instruction.

13. (F)Some instructions do not require the FETCH phase

14. (F)The Processing unit interacts with memory using the Memory Status Register and the Memory data register.

15. (F)The function of the Instruction Register is to point to next instruction to be processed.

16. (F)The data type supported by the LC-3 ISA is 1's complement integers.

17. (F)All LC-3 instructions modify the condition codes.

18. (F)There exists a sequence of LC-3 instructions such that after they are all executed, the condition codes will be set to N = 0, Z = 0, and P = 0.

19. (T)Using a sentinel to control the number of executions of a loop is very effective if the programmer does not know ahead of time how many iterations will be performed.

20. (F)Some LC-3 data movement instructions move data from one memory location to another.

二 Multiple Choice (2 point each, 40 points)

1. Two values A = 11111111111111111111111010101 and B = 1111010101are representations of 2's complement integers.

a. A is larger
b. B is larger
c. A and B are equal
d. You can not tell from the information provided.

Answer: c

2. Using 8 bits, the unsigned integer representation of -13 is:

a. 10001101
b. 11110101
c. not possible to represent.

Answer: c

3. To divide a 2's complement integer by 4,

a. it is first necessary to convert the bit string to its decimal value.
b. shift right the bit string two places, and insert 0 in the two left-most bit positions.
c. shift right the bit string two places, and insert the sign bit in the two left-most bit positions.
d. shift left the bit string two places, and insert 0 in the two right-most bit positions.

Answer: c

4. With 12 bits, we can represent uniquely:

a. exactly 12 distinct items
b. exactly 2 times 12, or 24 distinct items
c. exactly 4096 distinct items.
d. as many distinct items as we wish to.

Answer: c

5. The operation ADD is

a. a unary operator because it performs ONE function, ADD.
b. a binary operator because it requires TWO operands.
c. a ternary operator because it requires TWO values to add and produces in addition, ONE result.

Answer: b

6. For a memory with a 16-bit address space, the addressability is
a. 16 bits
b. 8 bits
c. 2^16 bits
d. Cannot be determined
Answer: d

7. When the write enable input is not asserted, the gated D latch _____ its output.
a. can not change
b. clears
c. sets
d. complements
Answer: a

8. We say that a set of gates is logically complete if we can build any circuit without using any other kind of gates. Which of the following sets are logically complete
a. set of {AND,OR}

b. set of {EXOR, NOT}
c. set of {AND,OR,NOT}
d. None of the above
Answer: c

9. If the number of address bits in a memory is reduced by 2 and the addressability is doubled, the size of the memory (i.e., the number of bits stored in the memory)
a. doubles
b. remains unchanged
c. halves
d. increases by 2^(address bits)/addressability

Answer : c

10. If m is a power of 2, the number of select lines required for an m-input mux is:

a. m
b. 2^m
c. log2 (m)
d. 2*m

Answer: c

11. The Decode phase of the Instruction Cycle examines the _____ part of the instruction.

a. Immediate (literal) value
b. Opcode
c. Offset
d. Register

Answer: b

12. Each phase of an instruction cycle requires
a. exactly one clock cycle to do its job.
b. at least one clock cycle to do its job.
c. no more than one clock cycle to do its job.
d. between 0 and some finite value n cycles to do its job.
Answer: d

13. In the FETCH phase, an instruction is transferred from _____ to the Instruction Register.
a. Memory.
b. Processing Unit
c. Input device
d. Output device
Answer: a

14. If memory accesses take 100 times more than register accesses, then a LDR instruction will take ___ machine cycles than an JMP R3 instruction .
a. fewer
b. more
c. same number of
Answer: b

15. The PC is incremented so that during the next instruction cycle, the next instruction will be processed. This happens during the
a. FETCH phase
b. DECODE phase
c. EVAL ADDRESS phase

d. EXEC phase
Answer: a

16. Which of the following instructions can reference a memory location that is #1000 locations from the instruction?

a. ADD
b. LD
c. STR
d. LEA
e. All of the above
f. None of the above

Answer: c

17. After the execution of which of the following instructions will the value in the Program Counter (PC) be 0x306e?

```
i.   0000111001011100 at location 0x3011
ii.  0000000001101110 at location 0x306d
iii. 1010011001101110 at location 0x306d
```

a. i and ii
b. i and iii
c. ii and iii
d. i, ii, and iii

Answer: d

18. If the LC-3 ISA was modified to specify 32 general purpose registers and every other specification remained unchanged, how many bits would be required to encode an LC-3 ADD instruction?

a. 16
b. 20
c. 24
d. 31
e. 32

Answer: b

19. If the condition codes have values N = 0, Z = 0, P = 1 at the beginning of the execution of the following sequence of instructions, what will their value be at the end of the execution of the following sequence?

```
Address             Instruction
-------             ------------------------
0x3050              0000001000000001
0x3051              0101000000100000
0x3052              0001000000100001
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```
a. N = 0, Z = 0, P = 1
b. N = 0, Z = 1, P = 0
c. N = 1, Z = 0, P = 0
d. Cannot be determined with the information given in the question.
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Answer: d
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20. If the control is redirected to location 0x4444 after the execution of the following instructions, what should have been the relationship between R1 and R2 before these instructions were executed?

Address	Instruction
0x4400	1001100010111111
0x4401	0001100100100001
0x4402	0001100001000100
0x4403	0000100001000000

a. R1 > R2 (R1 was greater than R2)
b. R1 < R2 (R2 was greater than R1)
c. R1 = R2 (R1 and R2 were equal)
d. Cannot be determined with the given information.

Answer: b

三 Fill in Blanks (2 points each, total 40 points)

(Note: Blank is indicated by parentheses, which contains the answer)

1. If we add the 2's complement representation of k to the 2's complement representation of -k, the result will be (all 0's, plus a carry).

2. 110001 is the 6-bit 2's complement representation for (-15).

3. ADD, SUB are examples of (arithmetic) operators; AND, NOT are examples of (logical) operators.

4. The (ALU) is the mechanism inside a computer that actually does the arithmetic and logical operations.

5. Every key on the keyboard has at least two corresponding (ASCII) codes, depending on whether or not the SHIFT key is also simultaneously depressed.

6. If A[15:0] = 1000110001110001, A[12:9] = (0110).

7.If 16 bits are used to specify the address space of a memory, the memory has (65536) uniquely identifiable locations.

8. A decoder with n inputs can have no more than (2^n) outputs.

9. One can write into a gated D latch only while the (WE) signal is asserted.

10. We clear an R-S latch by momentarily setting the (R) signal to (0).

11. Memory supplies data and accepts data to/from other devices through the (MEMORY DATA REGISTER -MDR).

12. The size of the quantities normally processed by the ALU is often referred to as the (WORD LENGTH) of the computer.

13. The Program counter contains the (address of the next instruction to be processed).

14. A 16-bit instruction takes the following format <OPCODE><DR><SR><IMM> where DR specifies the destination register, SR specifies the source register, and IMM is a 2's complement immediate value. If there are 27 opcodes and 16 registers, the number of bits left to specify the immediate value is (3).

15. For a particular 16-bit ISA, the LDR instruction has the following format <Opcode = 0110> <DR><BaseR><OFFSET>. If there are 4 registers, the number of bits available to specify the offset is (8).

16. LD, LDR, LDI, LEA, ST, STR, and STI are (data movement) instructions of the LC-3 ISA.

17. If an ISA has 256 opcodes, the number of bits in the instruction encoding used to specify the opcode should be at least (8).

18. (Control instructions) change the sequence of the instructions that are executed.

19. The number of system calls that could be uniquely identified using a trapvector of 12 bits would be (4096).

20. The instruction 0011000100101111 at memory location 0x5611 store the value of register R0 into memory location 0x(5541) when executed.