Digital System Design Lab Report, Lab3

Author: Ying Yiwen
Number: 12210159

Contents

1 Assignment2

1.1 Introduction

1.2 VHDL Code

```
-- import library
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

-- entity declaration
entity sig_var is
Port ( x : in STD_LOGIC;
       y : in STD_LOGIC;
       z : in STD_LOGIC;
       res1 : out STD_LOGIC;
       res2 : out STD_LOGIC);
end sig_var;

-- architecture declaration
architecture Behavioral of sig_var is

-- signal declaration
signal sig_s1, sig_s2 : std_logic;

-- logic function
begin

-- process declaration, variable type
proc1: process (x, y, z) is
variable var_s1, var_s2 : std_logic;
begin
    var_s1 := x and y;
    var_s2 := var_s1 xor z;
    res1 <= var_s1 nand var_s2;
end process proc1;

-- process declaration, signal type
proc2: process (x, y, z) is
begin
    sig_s1 <= x and y;
    sig_s2 <= sig_s1 xor z;
    res2 <= sig_s1 nand sig_s2;
end process proc2;

end Behavioral;
```

1.3 Testbench Code

```
-- import library
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
```

```
-- entity declaration
entity testbench is
--  Port ( );
end testbench;

-- architecture declaration
architecture tb of testbench is
-- component declaration
component sig_var is
Port ( x : in STD_LOGIC;
        y : in STD_LOGIC;
        z : in STD_LOGIC;
        res1 : out STD_LOGIC;
        res2 : out STD_LOGIC);
end component;

-- signal and constant declaration
signal x, y, z, r1, r2 : std_logic ;
constant period: time := 10ns;

-- logic function
begin
-- instantiation
uut: sig_var port
    map( x => x,
            y => y,
            z => z,
            res1 => r1,
            res2 => r2);

-- test case
x <= '0' after period * 0, '1' after period * 4;
y <= '0' after period * 0, '1' after period * 2, '0' after period * 4, '1' after
    period * 6;
z <= '0' after period * 0, '1' after period * 1, '0' after period * 2, '1' after
    period * 3,
        '0' after period * 4, '1' after period * 5, '0' after period * 6, '1'
           after period * 7;

end tb;
```

1.4 Simulation Result

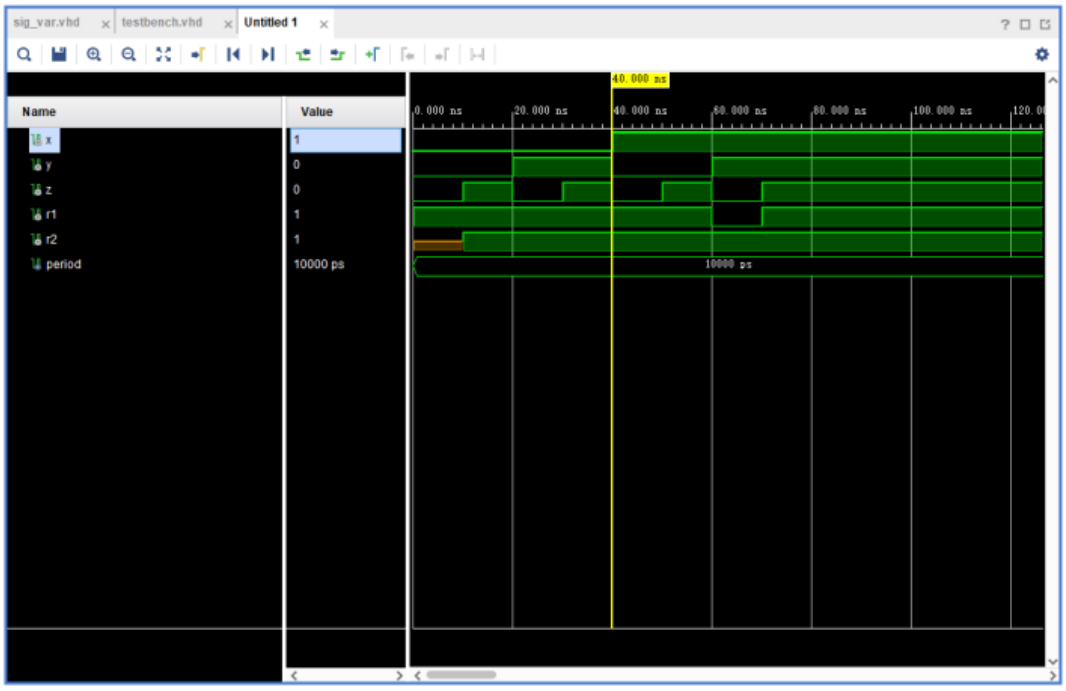

Figure 1: Behavior Simulation Result

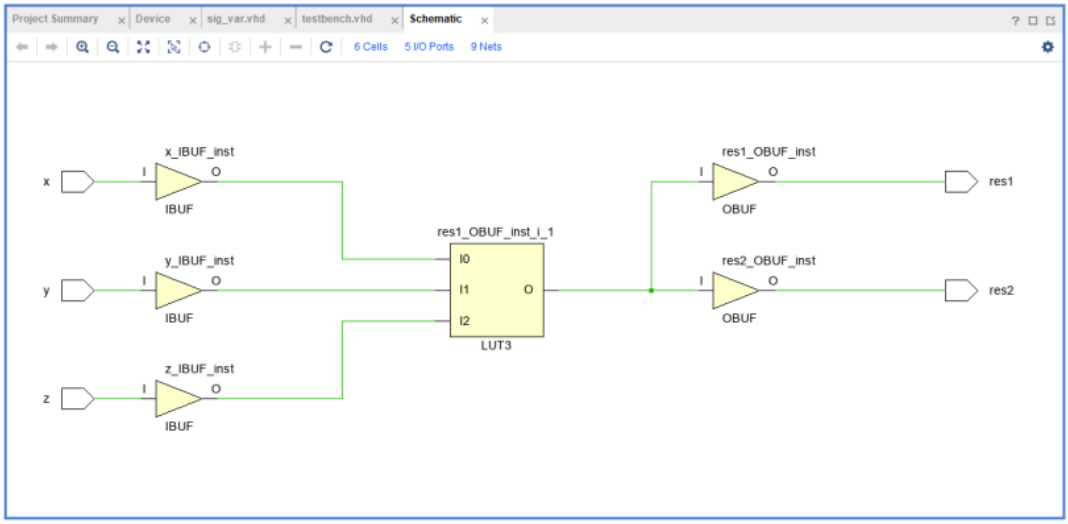

Figure 2: Schematic Simulation Result

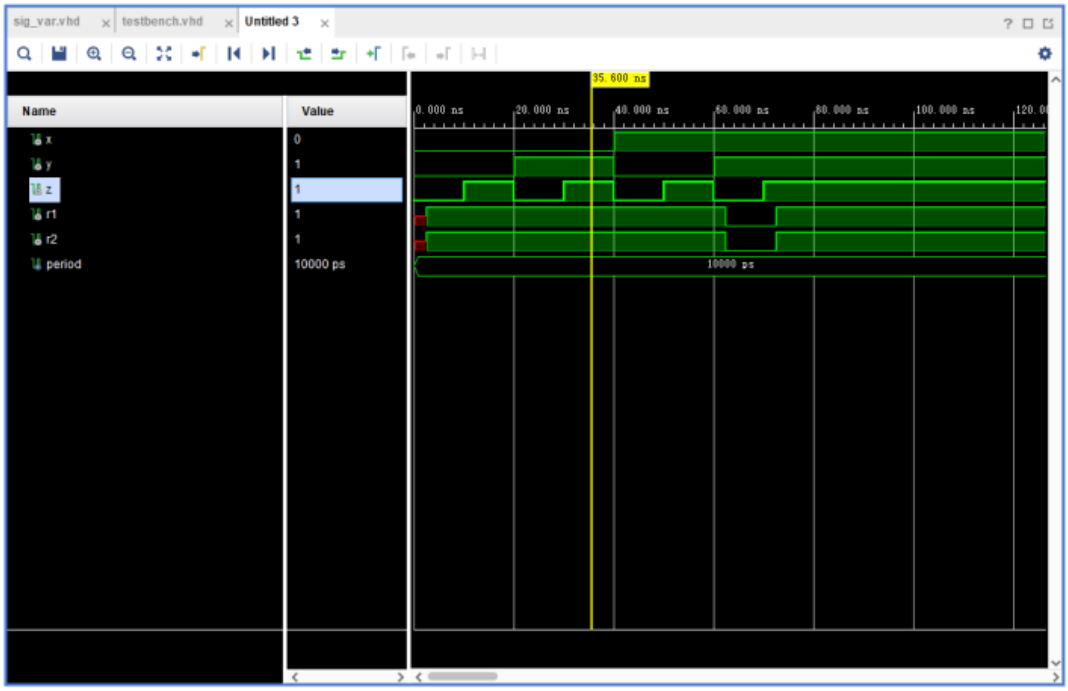

Figure 3: Post Synthesis Timing Simulation Result

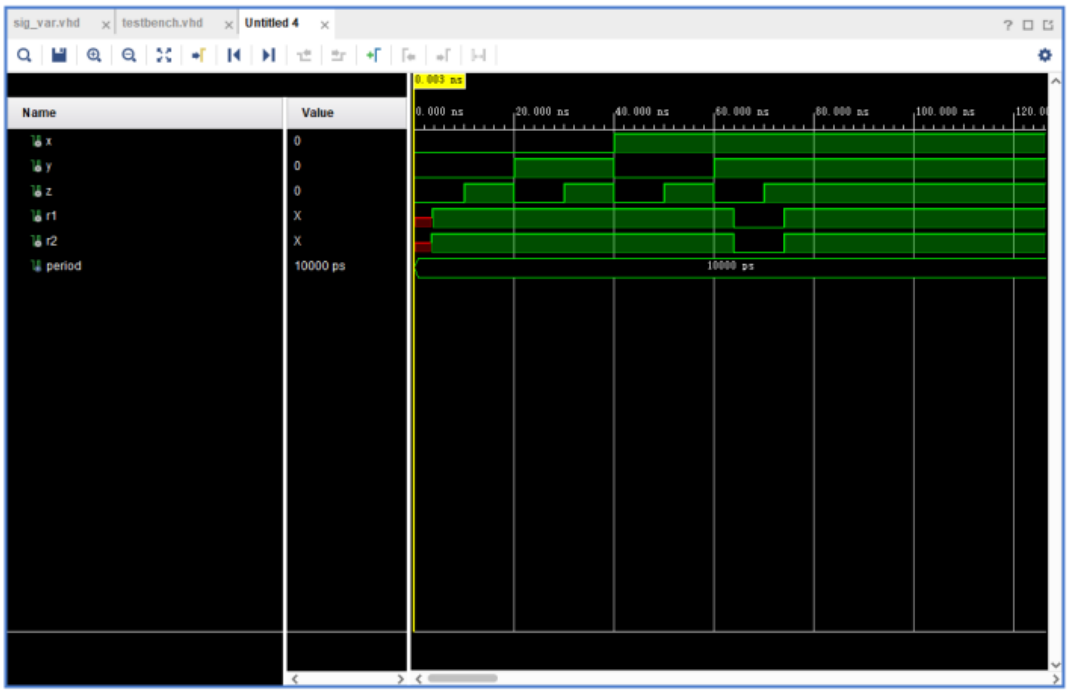

Figure 4: Post Implementation Timing Simulation Result