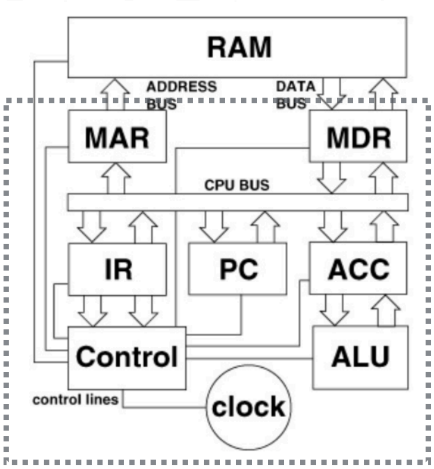
Week 5 Processors and Pipelining

Question 1

The Central Processing Unit (CPU) is made up by the control unit, the arithmetic logic unit(ALU) and several registers.

1. Explain the functions of each basic CPU configuration — ALU, MDR, CU, IR, MAR, Accumulator, and Program Counter.
2. The main job of the CPU is to execute programs using the fetch-decode-execute cycle (also known as the instruction cycle). Describe how the fetch-decode-execute cycle works and show how addresses and data (instructions and operands) are transferred between memory and CPU.



Question 2

Think of a real-world (non computing) activity that is analogous to instruction level parallelism; for example, a manufacturing assembly line, or a chain of events such as a supply-chain.

1. In this activity, what are the pipeline stages?
2. How long (comparatively speaking) does each stage take?
3. Are there any situations where a stage could"stall"?

Question 3

Assume a CPU has a 4-stage pipeline (i.e. stages for Fetch, Decode, Execute, Store) and each stage takes 1 clock cycle. Assume a stream of instructions A, B, C, etc...

Instruction No.	Pipeline Stage						
A	F_A	D_A	E_A	S_A			
B		F_B	D_B	E_B	S_B		
C			F_C	D_C	E_C	S_C	
D				F_D	D_D	E_D	S_D
E					F_E	D_E	E_E
F						F_F	D_F
Clock Cycle	1	2	3	4	5	6	7

1. How many instructions have been executed at the end of the 3rd clock cycle?
2. What is the state of the pipeline?
3. How many instructions have been executed at the end of the 5th clock cycle?
4. How many instructions have been executed at the end of the 7th clock cycle?
5. How many clock cycles does it take to fill an N-stage pipeline?

6. Assume instruction A is a WHILE LOOP test, and instructions B & C are inside the loop and have been speculatively loaded into the pipeline. But on executing A, the processor discovers the loop will terminate so B & C should not be performed. Draw the pipeline for the next 4 clock cycles.

Question 4

Compare the relative benefits and drawbacks of:

1. A deeply pipelined processor
2. A multi-core processor
3. A processor core that supports simultaneous multithreading

Question 5

Central Processing Unit Architecture operates the capacity to work from "Instruction Set Architecture" to where it was designed. The architectural designs of CPU are RISC (Reduced instruction set computing) and CISC (Complex instruction set computing).
There was a time when RISC architecture threatened to overtake the more traditional CISC architecture. Investigate the properties of RISC and CISC and why this did not happen in the end.

Question 6

What's the difference between a CPU and a GPU?
What are the differences between GPUs and graphics cards?