Week 3 Digital Logic & Boolean Algebra

Question 1 — Binary Negative Numbers

1. To get the two's complement negative notation of an integer, you write out the number in binary. You then invert the digits, and add one to the result.
   Show how -27_{10} would be expressed in two's complement notation.
2. Our numbers are 8-bits long, suppose we want to subtract 27_{10} from 115_{10}, show how to perform binary subtraction using the two's complement method.
3. Our numbers are 8-bits long, suppose we want to subtract 115_{10} from 27_{10}, show how to perform binary subtraction using the two's complement method. Show how to convert the result to decimal using the two's complement method.

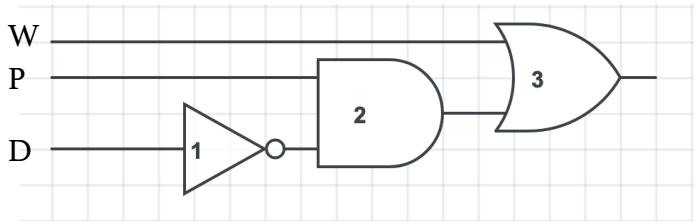
Question 2

Using Truth Tables prove whether the following Boolean equalities are true:

1. /(A + B) = /A . /B
2. /(A.B) = /A . /B

Question 3

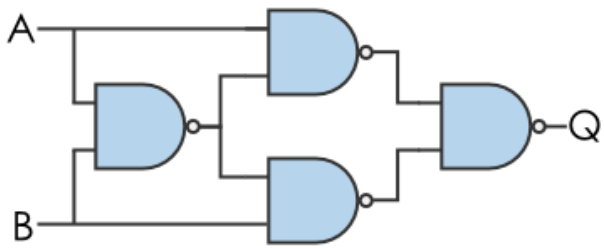
Consider the following logic diagram with switches W, P and D:



1. Identify the three gates being used in the diagram.
2. Write the logic expression that is equivalent to the diagram. (It need not be simplified.)
3. Complete a truth table that shows the output (X) for inputs (W, P and D).
4. Using LogiSim (or DigitalWorks or alternative software) draw the logic diagram and verify the truth table in 3 by placing a lamp at the final output.

Question 4

Consider the following logic diagram composed of NAND gates.



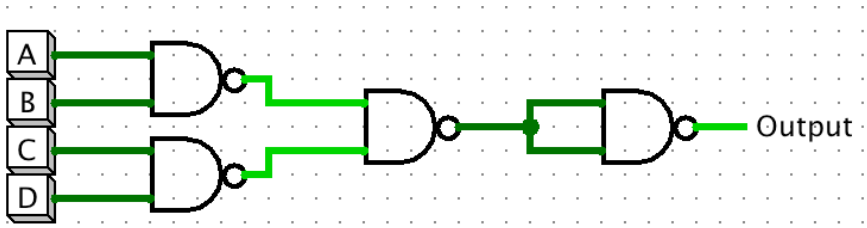
1. Write a truth table that shows the output (Q) for inputs (A and B).
2. Which logic gate is this equivalent to?

Question 5

Draw the logic diagrams for each of the following Boolean expressions.
(You can draw these by hand or using LogiSim, Digitalworks or other software)

1. (A+B).(A+C)
2. /A.B +A.B.C + /A./B./C./D

Question 6



By hand write down

1. the output of each gate, and
2. the final output for the given digital logic diagram.

Question 7 (Optional)

Build and test a half-adder out of discrete logic gates using Logisim (or alternative software)

1. Extend your half-adder into a full-adder.
2. Connect multiple full-adders into a parallel adder.

The relevant logic diagrams, and blueprint for extending the adders' functionality, are available in the online and lecture notes.