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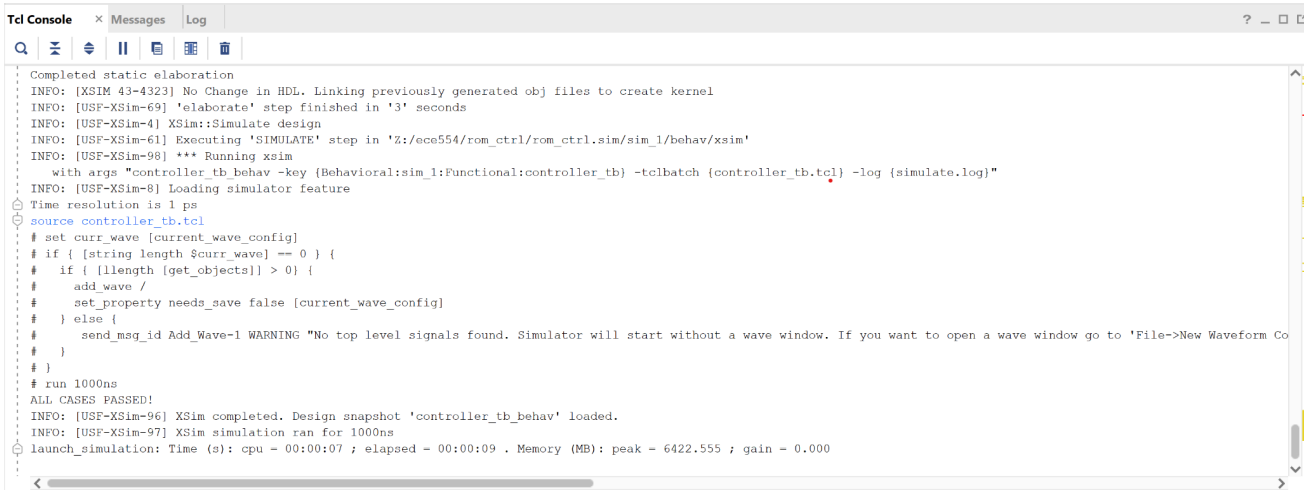
# Mini Lab 0 Report

## 1) GitHub Repository Info

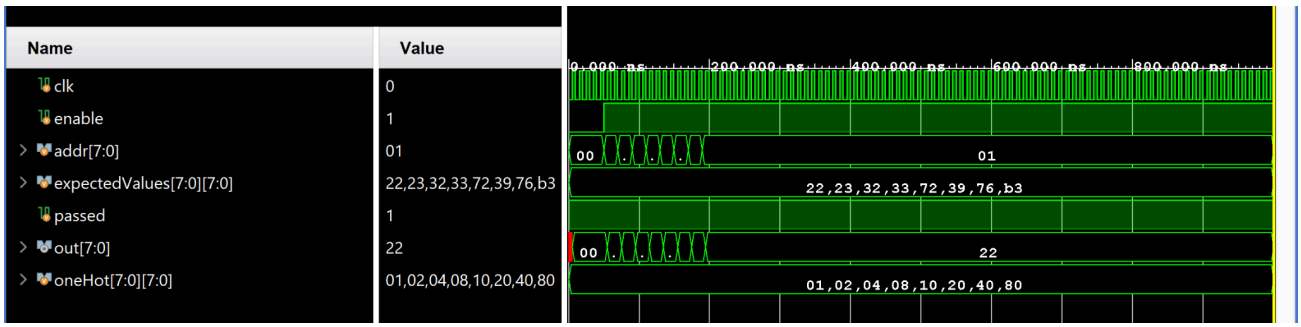
Link: https://github.com/WerynWolf/ECE554SP26/tree/main/ECE554SP26_Minilab0

This repository was created through the GitHub website. The files were cloned from Madi's repository, as her Vivado instance was used while working through the Lab.

## 2) Simulation Log




## 3) Simulation Waveform Snapshot



4) Differences in Resource Utilization reports

Synthesis converts the HDL code into digital logic (LUTs, Flops, etc.) but does not map it onto the physical hardware (the Synthesis report lists the board layout as a Blackbox, while the Implementation report lists it as an Instantiated Netlist).

This means that the Synthesis report cannot yet see what hardware resources will utilized – the breakdown of CLBs by type is visible only in the Implementation report. Additionally, this means that while Synthesis sees I/O *signals*, only the Implementation report can provide a breakdown of I/O *devices* utilized.

5) Large Memory Design

The available registers are insufficient to hold any memory system of significant size. When designing such a memory system, the on-PL memory resources would be used to instantiate a Cache, with the main memory being kept either on a peripheral device (interfacing through either the Pmod+ or the Grove interconnect) or in the 8GB DDR memory on the PS (interfacing through AXI).