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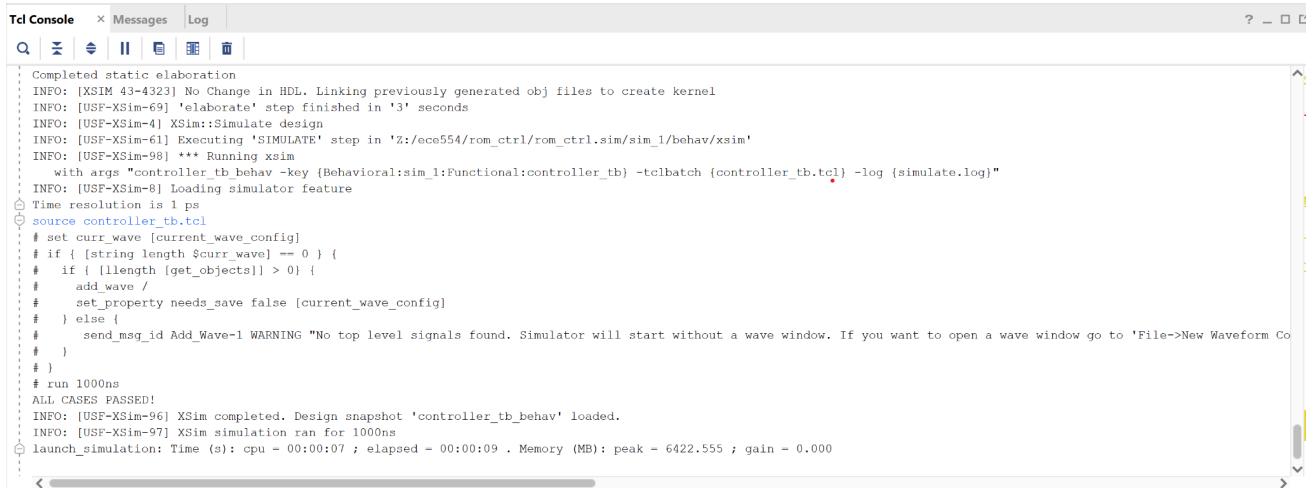
## Mini Lab 0 Report

### 1) GitHub Repository Info

Link: [https://github.com/WerynWolf/ECE554SP26/tree/main/ECE554SP26\\_Minilab0](https://github.com/WerynWolf/ECE554SP26/tree/main/ECE554SP26_Minilab0)

This repository was created through the GitHub website. The files were cloned from Madi's repository, as her Vivado instance was used while working through the Lab.

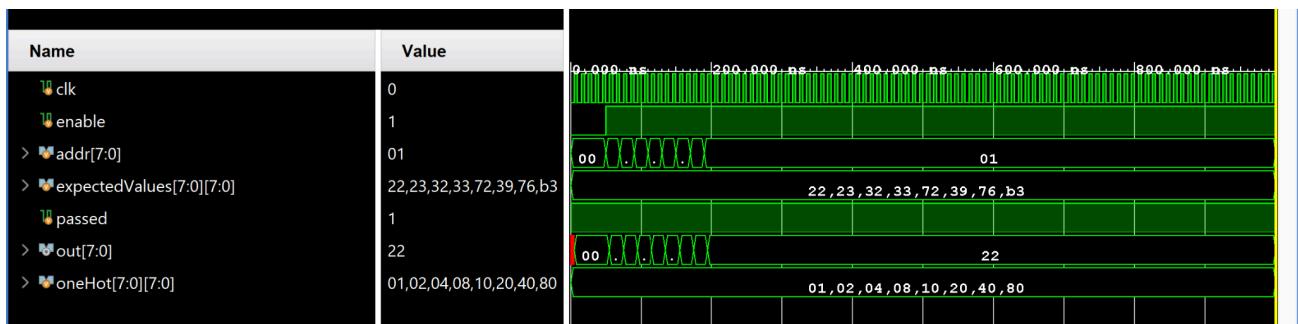
### 2) Simulation Log



The screenshot shows the Vivado Tcl Console window. The log output is as follows:

```
Completed static elaboration
INFO: [XSIM 43-4323] No Change in HDL. Linking previously generated obj files to create kernel
INFO: [USF-XSim-69] 'elaborate' step finished in '3' seconds
INFO: [USF-XSim-4] XSim::simulate design
INFO: [USF-XSim-61] Executing 'SIMULATE' step in 'z:/ece554/rom_ctrl/rom_ctrl.sim/sim_1/behav/xsim'
INFO: [USF-XSim-98] *** Running xsim
    with args "controller_tb_behav -key {Behavioral:sim_1:Functional:controller_tb} -tclbatch (controller_tb.tcl) -log {simulate.log}"
INFO: [USF-XSim-8] Loading simulator feature
Time resolution is 1 ps
source controller_tb.tcl
# set curr_wave [current_wave_config]
# if { [string length $curr_wave] == 0 } {
#   if { [llength [get_objects]] > 0} {
#     add_wave /
#     set_property needs_save false [current_wave_config]
#   } else {
#     send_msg_id Add_Wave-1 WARNING "No top level signals found. Simulator will start without a wave window. If you want to open a wave window go to 'File->New Waveform Co
#   }
# }
# run 1000ns
ALL CASES PASSED
INFO: [USF-XSim-96] XSim completed. Design snapshot 'controller_tb_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:07 ; elapsed = 00:00:09 . Memory (MB): peak = 6422.555 ; gain = 0.000
```

### 3) Simulation Waveform Snapshot



#### 4) Differences in Resource Utilization reports

Synthesis converts the HDL code into digital logic (LUTs, Flops, etc.) but does not map it onto the physical hardware (the Synthesis report lists the board layout as a Blackbox, while the Implementation report lists it as an Instantiated Netlist).

This means that the Synthesis report cannot yet see what hardware resources will be utilized – the breakdown of CLBs by type is visible only in the Implementation report. Additionally, this means that while Synthesis sees I/O *signals*, only the Implementation report can provide a breakdown of I/O *devices* utilized.

#### 5) Large Memory Design

The available registers are insufficient to hold any memory system of significant size. When designing such a memory system, the on-PL memory resources would be used to instantiate a Cache, with the main memory being kept either on a peripheral device (interfacing through either the Pmod+ or the Grove interconnect) or in the 8GB DDR memory on the PS (interfacing through AXI).