**信息科学与工程学院**

**2019－2020学年第二学期**

实 验 报 告

课程名称： 电子设计自动化

实验名称： 实验二 编码器和译码器设计

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实 验 时 间 2020年4月

实验报告

【实验目的】

1.掌握使用VHDL语言进行硬件设计的基本方法

2.掌握基本的Quartus Ⅱ使用方法

3.学会testbench的编写，掌握波形仿真的基本方法

【实验要求】

1.设计一个8-3线优先编码器（74LS148）

2.设计一个3-8线译码器（74LS138）

【实验具体内容】

### 【第一个实验】

1.实验原理

（1）真值表

|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 端口名 | DIN() | | | | | | | | OP() | | |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 2 | 1 | 0 |
| 真值表 | X | X | X | X | X | X | X | X | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| X | X | X | X | X | X | X | 0 | 0 | 0 | 0 |
| X | X | X | X | X | X | 0 | 1 | 0 | 0 | 1 |
| X | X | X | X | X | 0 | 1 | 1 | 0 | 1 | 0 |
| X | X | X | X | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| X | X | X | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| X | X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| X | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

其中，1－高电平 ，0－低电平 ，X－任意

（2）逻辑函数

OP(2) = DIN(4)+DIN(5)+DIN(6)+DIN(7)

OP(1) = DIN(2)DIN(4)DIN(5)+DIN(3)DIN(4)DIN(5)+DIN(6)+DIN(7)

OP(0) = DIN(1)DIN(2)DIN(4)DIN(6)+DIN(3)DIN(4)DIN(6)+DIN(5)DIN(6)+DIN(7)

2.设计模块代码（Design Block）

LIBRARY IEEE;

USE IEEE.STD\_LOGIC\_1164.ALL;

ENTITY CODER\_74LS148 IS

PORT (

din : IN STD\_LOGIC\_VECTOR(0 TO 7);

op : OUT STD\_LOGIC\_VECTOR(2 DOWNTO 0)

);

END ENTITY CODER\_74LS148;

ARCHITECTURE behav OF CODER\_74LS148 IS

BEGIN

PROCESS (din)

BEGIN

IF (din(7)='0') THEN op <= "000" ;

ELSIF (din(6)='0') THEN op <= "001" ;

ELSIF (din(5)='0') THEN op <= "010" ;

ELSIF (din(4)='0') THEN op <= "011" ;

ELSIF (din(3)='0') THEN op <= "100" ;

ELSIF (din(2)='0') THEN op <= "101" ;

ELSIF (din(1)='0') THEN op <= "110" ;

ELSE op <= "111" ;

END IF ;

END PROCESS ;

END ARCHITECTURE behav;

3.激励模块代码（Test Bench）

LIBRARY ieee;

USE ieee.std\_logic\_1164.all;

ENTITY CODER\_74LS148\_vhd\_tst IS

END CODER\_74LS148\_vhd\_tst;

ARCHITECTURE CODER\_74LS148\_arch OF CODER\_74LS148\_vhd\_tst IS

SIGNAL din1 : STD\_LOGIC\_VECTOR(0 TO 7);

SIGNAL op1 : STD\_LOGIC\_VECTOR(2 DOWNTO 0);

COMPONENT CODER\_74LS148

PORT (

din : IN STD\_LOGIC\_VECTOR(0 TO 7);

op : OUT STD\_LOGIC\_VECTOR(2 DOWNTO 0)

);

END COMPONENT;

BEGIN

i1 : CODER\_74LS148

PORT MAP (

din => din1,

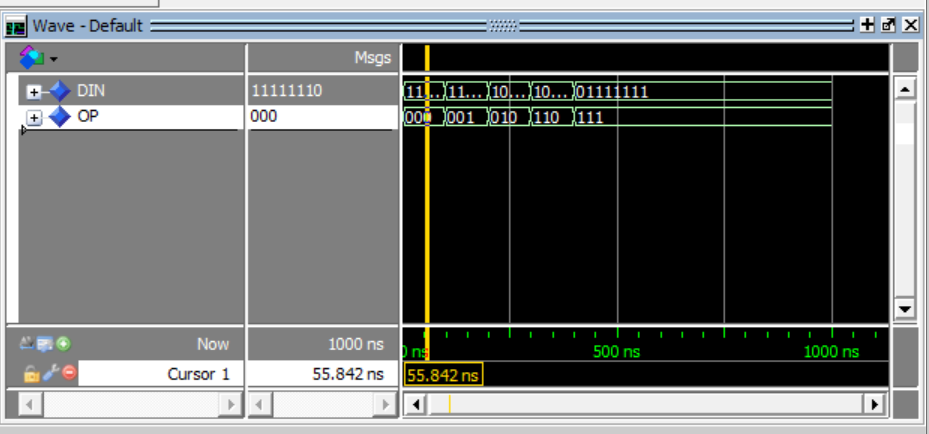
op => op1

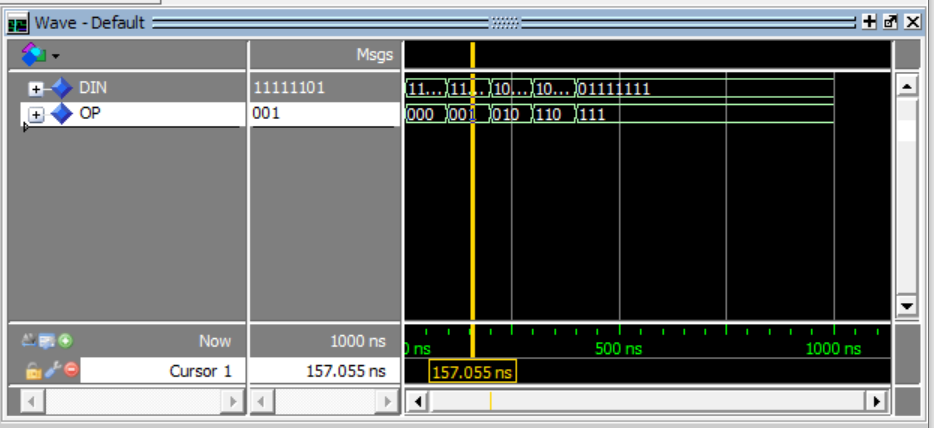
);

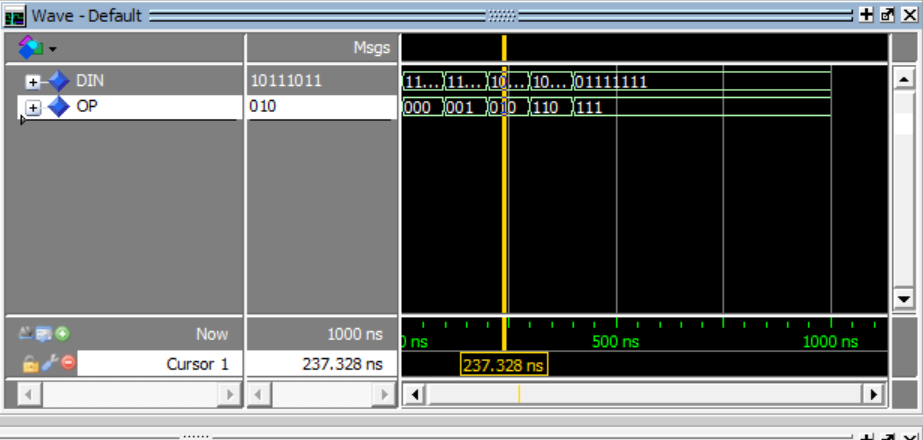
din1 <= "11111110", "11111101" AFTER 100 NS, "10111011" AFTER 200 NS, "10111111" AFTER 300 NS, "01111111" AFTER 400 NS;

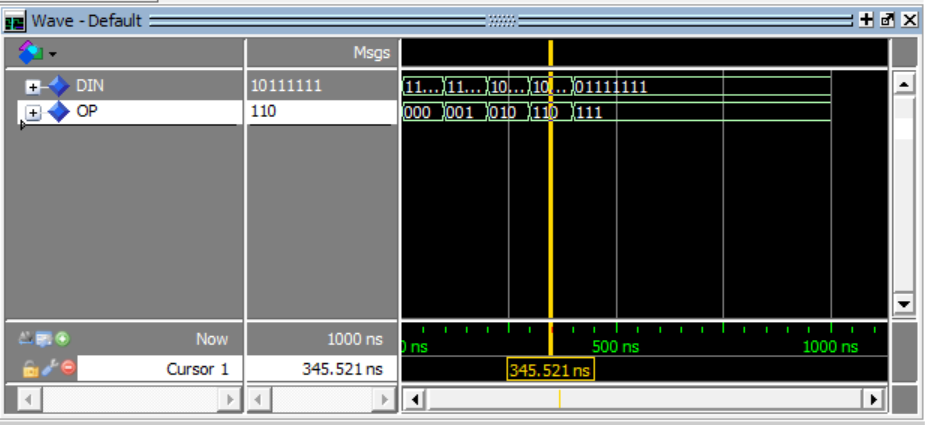
END CODER\_74LS148\_arch;

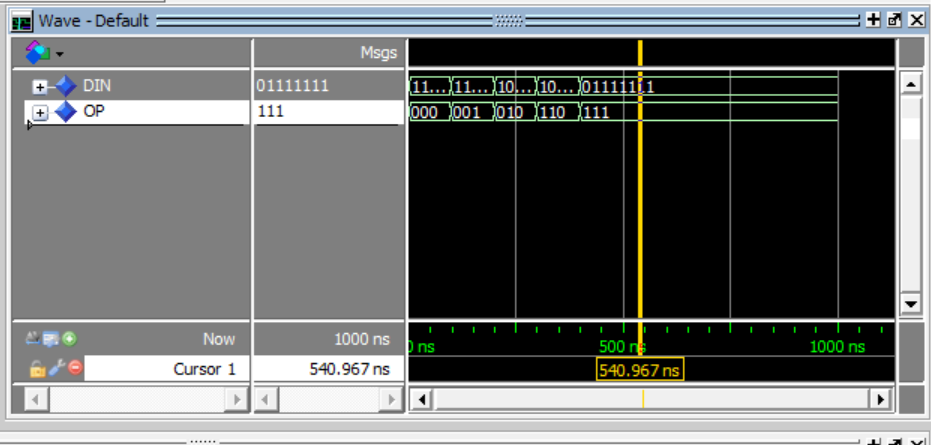
4.仿真波形图



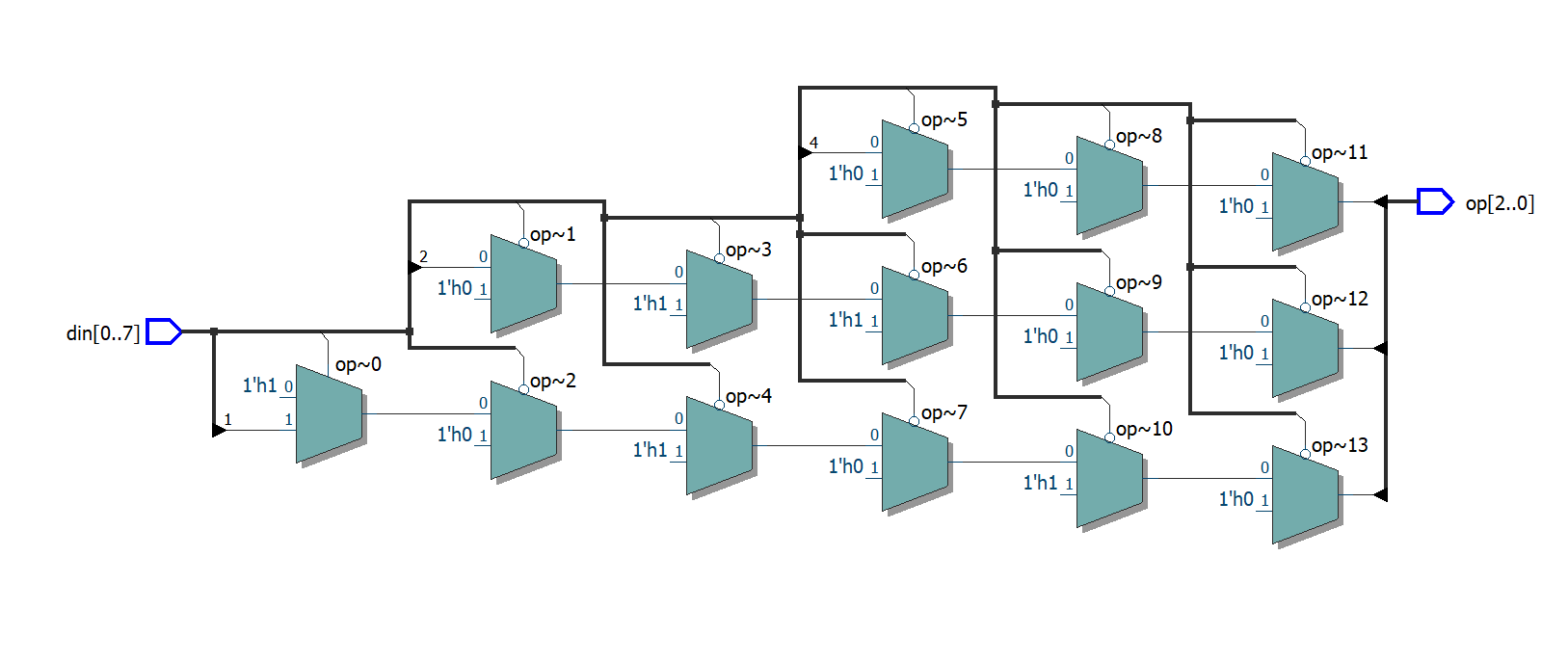








5.门级电路图



6.结果分析与思考

1. 注意输出口不要用output，输入口不要用in作标识符，不然仿真可能报错
2. 如仿真图所示，设计的电路能实现相应功能，对高位进行优先编码，输出的OP向量各位取反得到的二进制数即为0的输入端的号码

### 【第二个实验】

1.实验原理

（1）真值表

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 输入 | | | | | | 输出 | | | | | | | |
| G1 | G2A | G2B | A2 | A1 | A0 | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| × | 1 | × | × | × | × | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| × | × | 1 | × | × | × | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | × | × | × | × | × | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

其中，1－高电平 ，0－低电平 ，X－任意

（2）逻辑函数

当G1&G2A&G2B为”100”

Y0=A2’A1’A0’

Y1=A2’A1’A0

Y2=A2’A1A0’

Y3=A2’A1A0

Y4=A2A1’A0’

Y5=A2A1’A0

Y6=A2A1A0’

Y7=A2A1A0

当G1&G2A&G2B不为”100”

无论Ai输入多少Y0~Y7均输出”11111111”

2.设计模块代码（Design Block）

LIBRARY IEEE;

USE IEEE.STD\_LOGIC\_1164.ALL;

ENTITY ENCODER\_74LS138 IS

PORT(A,B,C,G1,G2A,G2B : IN STD\_LOGIC;

Y : OUT STD\_LOGIC\_VECTOR (7 DOWNTO 0));

END ENTITY ENCODER\_74LS138;

ARCHITECTURE RTL OF ENCODER\_74LS138 IS

SIGNAL INDATA : STD\_LOGIC\_VECTOR(2 DOWNTO 0);

BEGIN

INDATA <= C & B & A;

PROCESS(INDATA,G1,G2A,G2B)

BEGIN

IF (G1 = '1' AND G2A = '0' AND G2B = '0') THEN

CASE INDATA IS

WHEN "000" => Y<="11111110";

WHEN "001" => Y<="11111101";

WHEN "010" => Y<="11111011";

WHEN "011" => Y<="11110111";

WHEN "100" => Y<="11101111";

WHEN "101" => Y<="11011111";

WHEN "110" => Y<="10111111";

WHEN "111" => Y<="01111111";

WHEN OTHERS => Y<="XXXXXXXX";

END CASE;

ELSE

Y<="11111111";

END IF;

END PROCESS;

END ARCHITECTURE RTL;

3.激励模块代码（Test Bench）

LIBRARY ieee;

USE ieee.std\_logic\_1164.all;

ENTITY ENCODER\_74LS138\_vhd\_tst IS

END ENCODER\_74LS138\_vhd\_tst;

ARCHITECTURE ENCODER\_74LS138\_arch OF ENCODER\_74LS138\_vhd\_tst IS

SIGNAL A1 : STD\_LOGIC;

SIGNAL B1 : STD\_LOGIC;

SIGNAL C1 : STD\_LOGIC;

SIGNAL G11 : STD\_LOGIC;

SIGNAL G2A1 : STD\_LOGIC;

SIGNAL G2B1 : STD\_LOGIC;

SIGNAL Y1 : STD\_LOGIC\_VECTOR(7 DOWNTO 0);

COMPONENT ENCODER\_74LS138

PORT (

A : IN STD\_LOGIC;

B : IN STD\_LOGIC;

C : IN STD\_LOGIC;

G1 : IN STD\_LOGIC;

G2A : IN STD\_LOGIC;

G2B : IN STD\_LOGIC;

Y : OUT STD\_LOGIC\_VECTOR(7 DOWNTO 0)

);

END COMPONENT;

BEGIN

i1 : ENCODER\_74LS138

PORT MAP (

A => A1,

B => B1,

C => C1,

G1 => G11,

G2A => G2A1,

G2B => G2B1,

Y => Y1

);

G11 <= '1', '0' AFTER 700 NS;

G2A1 <= '0', '1' AFTER 500 NS, '0' AFTER 600 NS;

G2B1 <= '0', '1' AFTER 400 NS, '0' AFTER 500 NS;

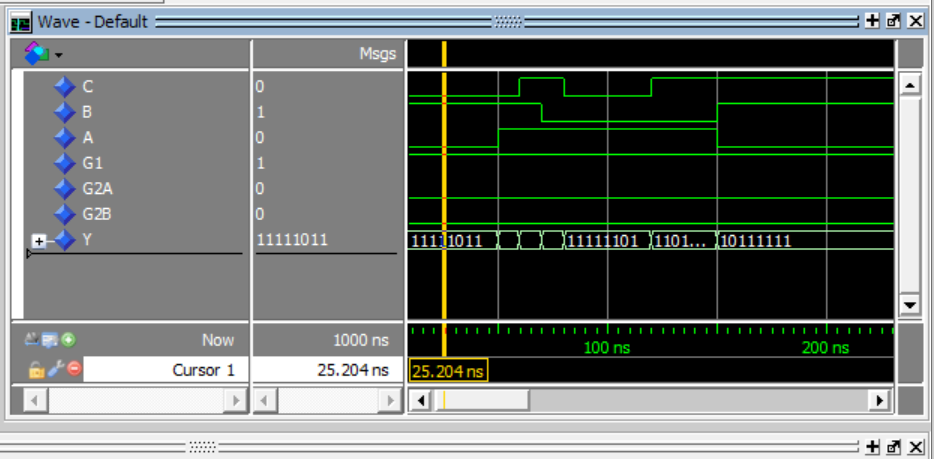
A1 <= '0', '1' AFTER 50 NS, '0' AFTER 150 NS;

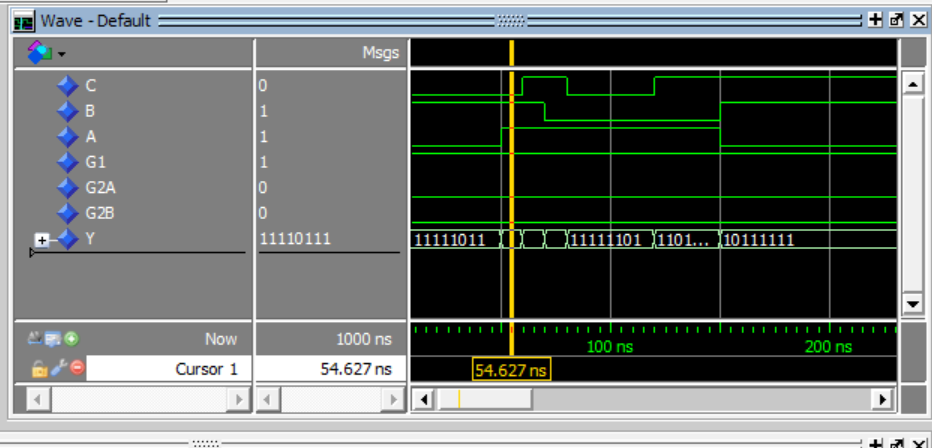
B1 <= '1', '0' AFTER 70 NS, '1' AFTER 150 NS;

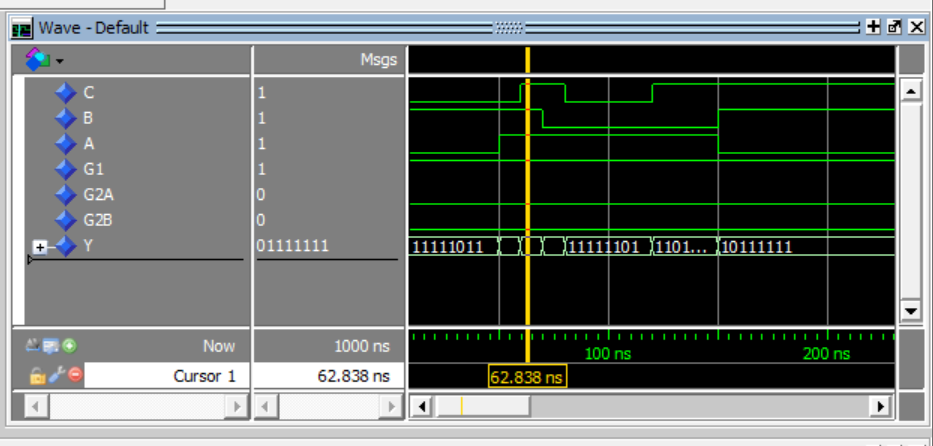
C1 <= '0', '1' AFTER 60 NS, '0' AFTER 80 NS, '1' AFTER 120 NS;

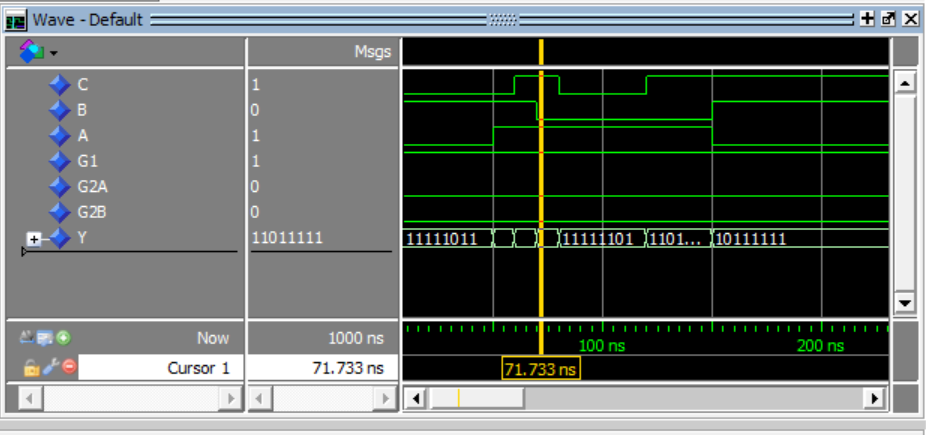
END ENCODER\_74LS138\_arch;

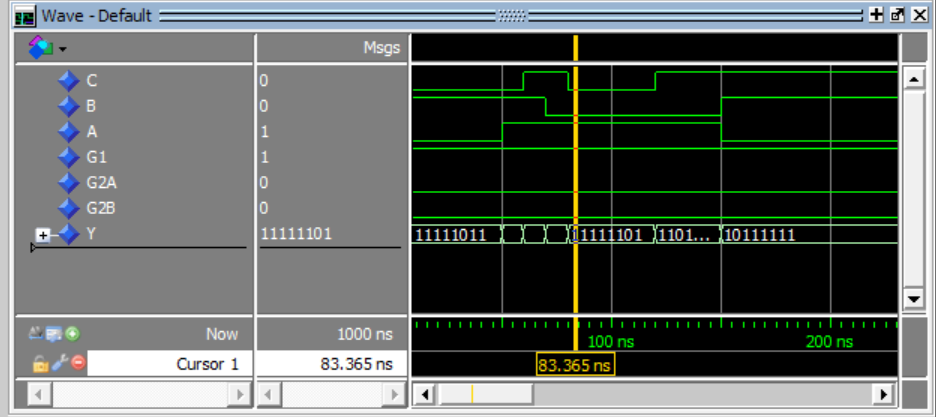
4.仿真波形图

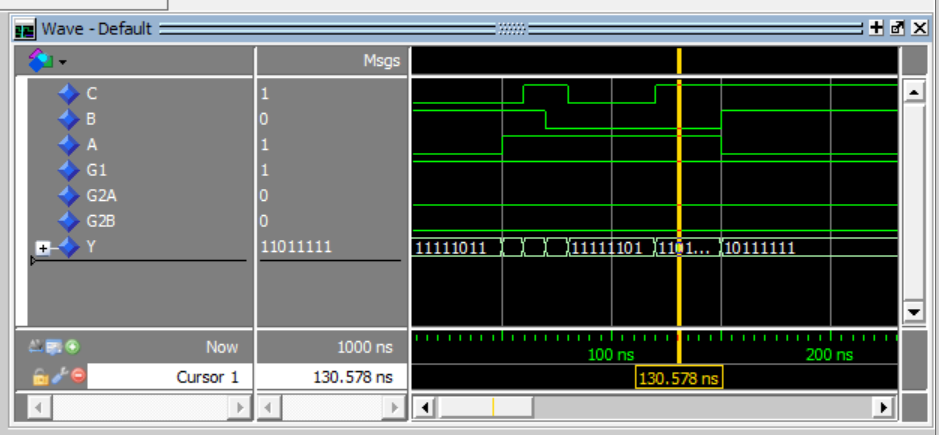


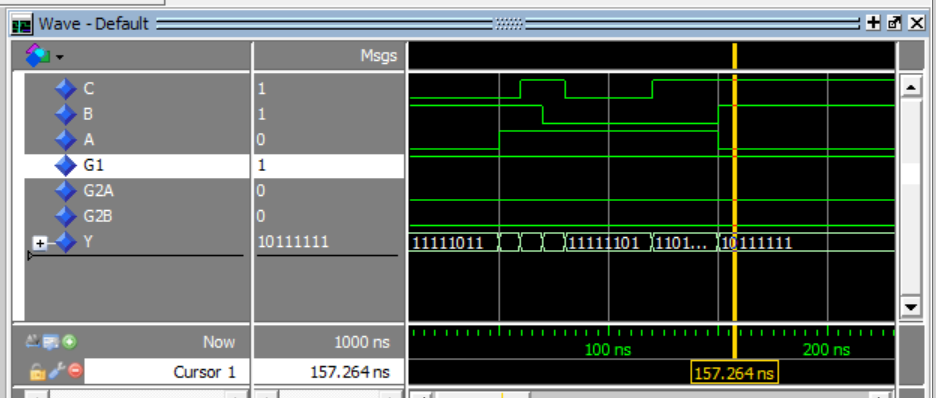




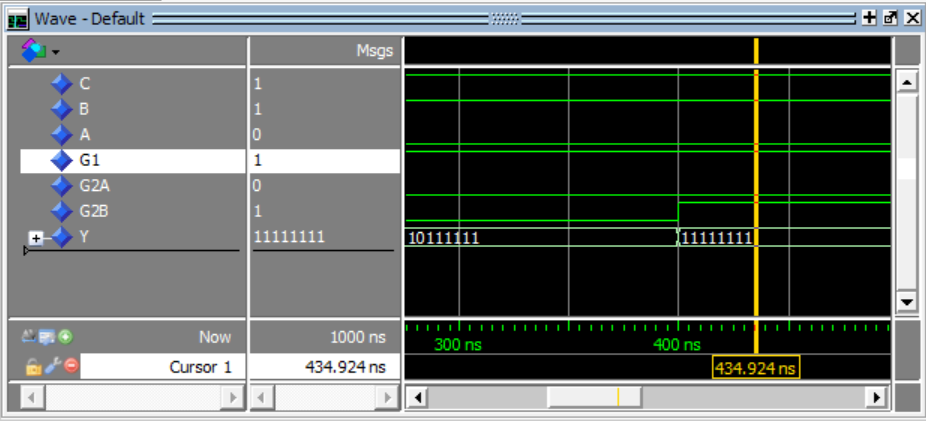


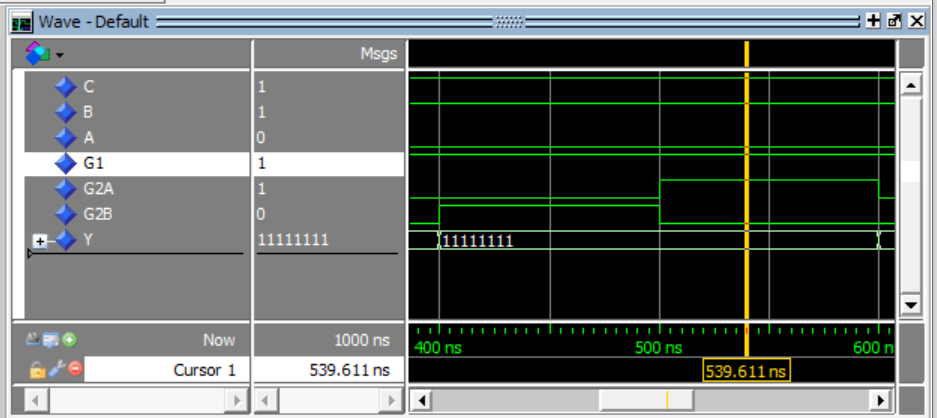


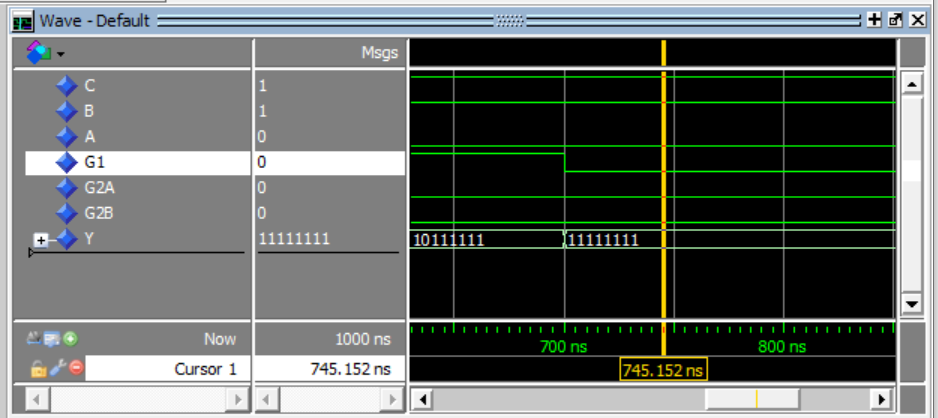




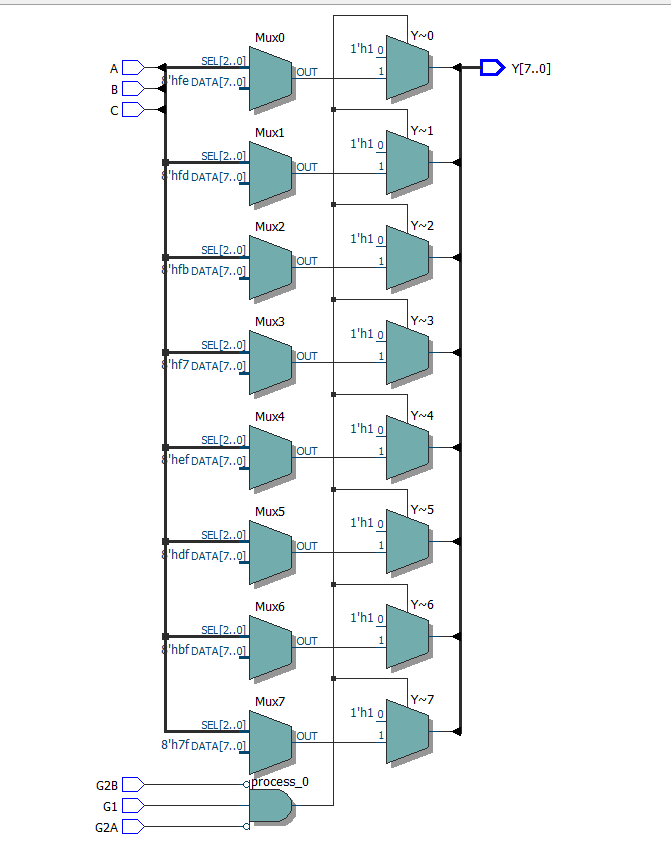
下面实现对三个使能端G1&G2A&G2B不为“100”的情况的测试，可见输出均为“11111111”







5.门级电路图



6.结果分析与思考

（1）如波形图所示，电路实现了所需功能，对输入信号A&B&C进行译码，输出结果为输入信号三位取反后的二进制数代表的那一位为0，其余7位均为1，而使能端必须为”100”，不然输出全为1

（2）真正的74LS138中各个端口应带一个取反号，不过限于EDA软件的命名规则，此处用未取反的端口名代替了