The pipelining was implemented using the given functions. Completed all the pipeline functions that depended on instructions from the given input. Each function was filled in with it's corresponding required values from the struct. Then proceeded to the push_pipeline_stage function.
Focused on the second block of code for the branch for a while. I was confused as to how the branch prediction worked at first. I first altered the given branch_taken variable given in the code using the hint in the pdf file. The value of the variable would be 1(true) if the branch was taken. I then figured out that the initial value in the beginning of the program that asked for branch prediction indicated that it would assume that all branches would either be taken or not taken depending on the user input. So I thought that to check if the branch taken was correct by comparing it to whether it was actually taken. Then if the prediction was incorrect, I incremented the cycles and pushed the instructions to the right while inserting a nop in the DECODE stage. If the prediction was correct then it simply incremented the correct number of branch predictions variable. I wasn't sure how to account for forwarding. I considered comparing des_reg of ALU and MEM stages if ALU was rtype or MEM was sw or lw. I wasn't sure how the regs would be forwarded from those regs to the current regs so I left it blank.
In 3 I had to check if there were delays in the ALU stage and the only way there would need delays was if the value was being altered which meant it had to be an rtype function altering the value. If there was a conflict, I incremented the nop value and pipeline cycles as a form of stalling. I also pushed the instruction forward and NOP-ed the current stage. If there was a miss in the cache, which was found using the trap_address function then the pipeline cycles would be stalled by the number of inserted nops and the CYCLE_MISS_DELAY -1 because the instructions were being pushed forward anyways.
The fourth stage was only affected by a miss so that only incremented the pipeline cycles if it missed. Then the pipeline_cycles was incremented as a whole because it meant that a cycle has finished so it was really for pushing. Then the stages were pushed right and FETCH was nulled to accept a new instruction.