CSCI-2500 Computer Organization
Carry-Lookahead (CLA) Adder

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1 Equation Dependencies for 64 Bit CLA

Recall that we can express the sum of two numbers as:

$$\text{sum}_i = a_i \bigoplus b_i \bigoplus c_{i-1} \tag{1}$$

Also, we know that:

$$c_i = g_i + p_i c_{i-1} \tag{2}$$

where g_i is the *generate function* which says did we generate a carry in the i^{th} stage and the p_i is the *propagate function* which says did we propagate a carry in the i^{th} stage assuming the carry-in, c_{i-1}, was positive. This yields the following:

$$g_i = a_i \times b_i \tag{3}$$

$$p_i = a_i + b_i \tag{4}$$

$$c_i = g_i + p_i c_{i-1} \tag{5}$$

Now, using the above recurrence we can find what c_i is for any 4 bit block or *group*.

$$\begin{aligned} c_i &= g_i + p_i c_{i-1} && (6) \\ c_{i+1} &= g_{i+1} + p_{i+1} c_i && (7) \\ c_{i+2} &= g_{i+2} + p_{i+2} c_{i+1} && (8) \\ c_{i+3} &= g_{i+3} + p_{i+3} c_{i+2} && (9) \end{aligned}$$

Notice how each of the c_i equations can all be written in terms of the the g, p and c_{i-1}. But, c_{i-1} is really the carry-in for this *group* of 4 bits. So, this means that the carry-in to those groups depends on the gc equations, which are:

$$\begin{aligned} gc_j &= gg_j + gp_j gc_{j-1} && (10) \\ gc_{j+1} &= gg_{j+1} + gp_{j+1} gc_j && (11) \\ gc_{j+2} &= gg_{j+2} + gp_{j+2} gc_{j+1} && (12) \\ gc_{j+3} &= gg_{j+3} + gp_{j+3} gc_{j+2} && (13) \\ & && (14) \end{aligned}$$

where...

$$\begin{aligned} gg_j &= g_{i+3} + p_{i+3} g_{i+2} + p_{i+3} p_{i+2} g_{i+1} + p_{i+3} p_{i+2} p_{i+1} g_i && (15) \\ gp_j &= p_{i+3} p_{i+2} p_{i+1} p_i && (16) \end{aligned}$$

Again, notice how each of the gc_j equations can all be written in terms of the the gg, gp and gc_{j-1}. But, gc_{j-1} is really the carry-in for this *section* of 4 groups. So, this means that the carry-in to those sections depends on the sc equations, which are:

$$\begin{aligned} sc_k &= sg_k + sp_k sc_{k-1} && (17) \\ sc_{k+1} &= sg_{k+1} + sp_{k+1} sc_k && (18) \\ sc_{k+2} &= sg_{k+2} + sp_{k+2} sc_{k+1} && (19) \\ sc_{k+3} &= sg_{k+3} + sp_{k+3} sc_{k+2} && (20) \\ & && (21) \end{aligned}$$

where...

$$\begin{aligned} sg_k &= gg_{j+3} + gp_{j+3} gg_{j+2} + gp_{j+3} gp_{j+2} gg_{j+1} + gp_{j+3} gp_{j+2} gp_{j+1} gg_j && (22) \\ sp_k &= gp_{j+3} gp_{j+2} gp_{j+1} gp_j && (23) \end{aligned}$$

2 Steps for Calculation for 64 Bit CLA

1. Calculate g_i and p_i for all i. (1 gate delay)

2. Calculate gg_j and gp_j for all j using g_i and p_i. (2 gate delays)

3. Calculate sg_k and sp_k for all k using gg_j and gp_j. (2 gate delays) *Note, it is at this point, we can shift to computing the top-level sectional carries. This is because the number of sections is less than or equal the block size which is 4 bits.*

4. Calculate sc_k using sg_k and sp_k for all k and 0 for sc_{i-1}. (2 gate delays)

5. Calculate gc_j using gg_j, gp_j and correct $sc_k, k = (j \text{ div } 4)$ as sectional carry-in for all j. (2 gate delays)

6. Calculate c_i using g_i, p_i and correct $gc_j, j = (i \text{ div } 4)$ as group carry-in for all i. (2 gate delays)

7. Calculate sum$_i$ using $a_i \bigoplus b_i \bigoplus c_{i-1}$ for all i. (2 gate delays)

8. **Total gate delays for 64 bit CLA is 13.**