**MCU Bus Interface**

* ARM CM4 Processor has 3 busses :
  + I- Bus : used to fetch instructions from flash
  + D-Bus : used to fetch const data from flash
  + S-Bus
* If the instructions are present in between the memory locations 0x0000 0000 to 0x1FFF FFFC then the Cortex Processor will fetch the instructions using I-CODE interface
* If the instructions are present outside of 0x0000 0000 to 0x0x1FFF FFFC then processor fetches the instructions over the system bus.
* If the data is present in between the memory locations 0x0000 0000 to 0x0x1FFF FFFC, then processor fetches the data over D-CODE bis interface.
* If the data is present outside 0x0000 0000 to 0x0x1FFF FFFF memory locations then, the data will be fetched over the system bus.

**Questions**

1. Is it true that System Bus is not connected to FLASH memory?
   1. True
2. The processor can fetch instructions form SRAM over I-CODE bus T/F?
   1. False
3. System Bus can operate at the speed up to 180MHz?
   1. True
4. SRAMs are connected to System Bus T/F?
   1. True
5. Can APB1 bus operate at a speed up to 180Mhz?
   1. False
6. Let’s say I have a peripheral whose datasheet says that its operating frequency or speed must be above 95Mhz, can I connect that peripheral via APB2 bus?
   1. No
7. Processor can fetch instructions as well as data simultaneously from SRAM T/F?
   1. False
8. Processor can fetch instructions as well as data simultaneously from FLASH T/F?
   1. True
9. What is Max. HCLK value of MCU?
   1. 180Mhz
10. What is Max. P1CLK value of MCU?
    1. 15Mhz
11. What is Max. P2CLK value of MCU?
    1. 90Mhz
12. GPIOs and processor communicate over AHB1 bus T/F?
    1. True
13. USB OTG and processor communicate over AHB2 bus T/F?
    1. True
14. USB OTG and GPIOs can communicate to processor concurrently or simultaneously T/F?
    1. False
15. Processor can talk to flash memory and SRAM simultaneously T/F?
    1. True (dedicated buses)