Karnaugh maps

- PRO's of smaller number of gates:
 - · minimize use of different type of gates
 - · lower cost of product

 4 simpler gates is easier to produce = less mistakes made
- Logic gates are quick yet use low energy

4 don't get overworked

Listen prescribed number of 1/0 ports needed by microcontroller by straightforward data encryption & decryption

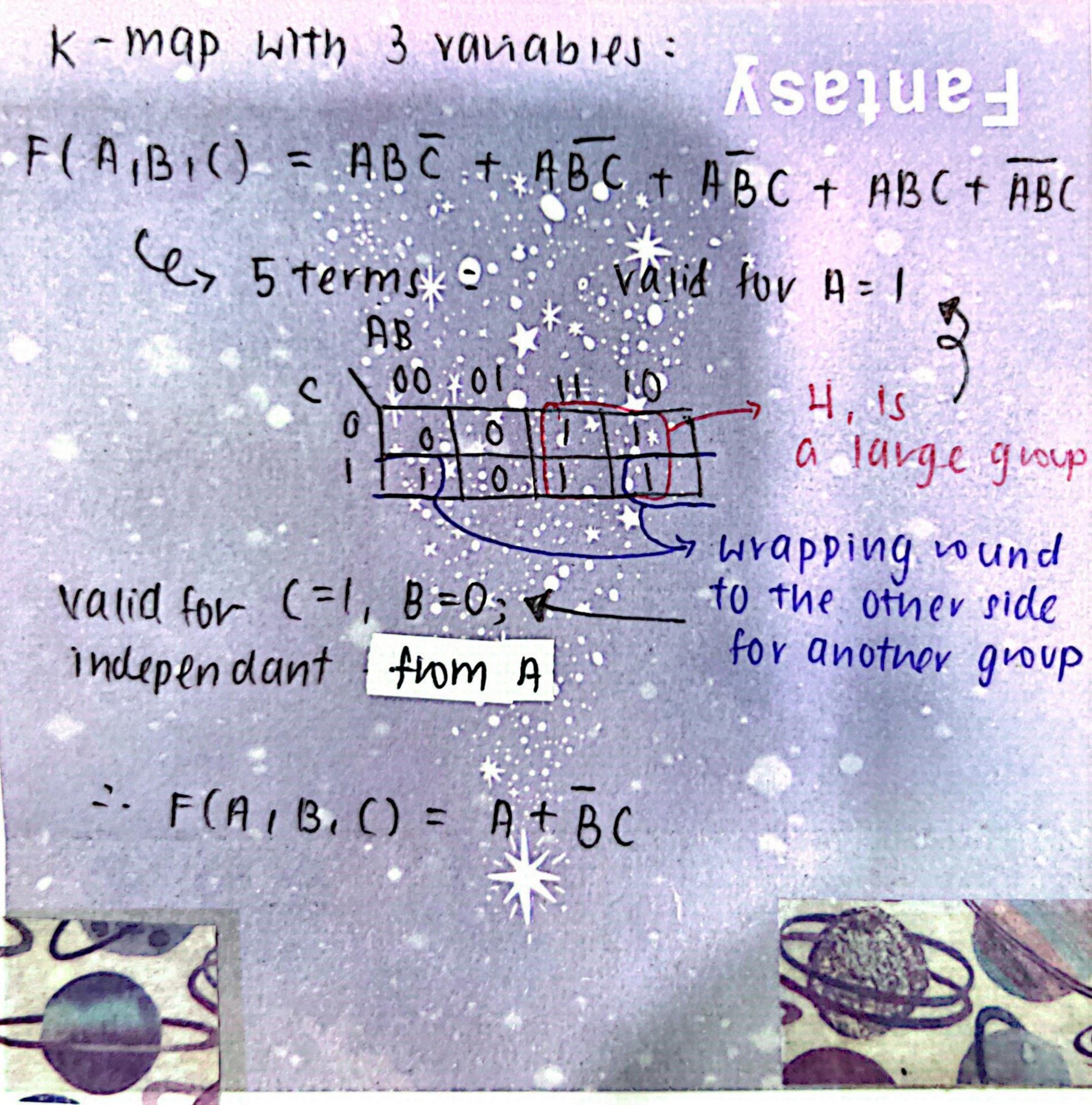
- General approach for minimising Boolean tunctions
 - = Karnaugh maps (k-maps)

Ly use graphical representation to find cases

Ly where different terms in Boowan formula

Ly can be combined to one simpler term

Lag. FROM: $(A \wedge B) \vee (A \wedge \overline{B}) = A \wedge (B \vee \overline{B}) = A \wedge 1 = A$ To: $(A \wedge B \wedge C) \vee (A \wedge \overline{B} \wedge C) = A \wedge C$



Scanned with CamScanner

