Crystal Growth

The two most important semiconductors for discrete devices and integrated circuits are silicon and gallium arsenide.
The starting material are chemically processed to form a high-purity polycrystalline semiconductor from which single crystals are grown. The single-crystal ingots are shaped to define the diameter of the material and are sawed (锯开) into wafers. These wafers are etched and polished to provide smooth, specular surfaces from which devices will be made.

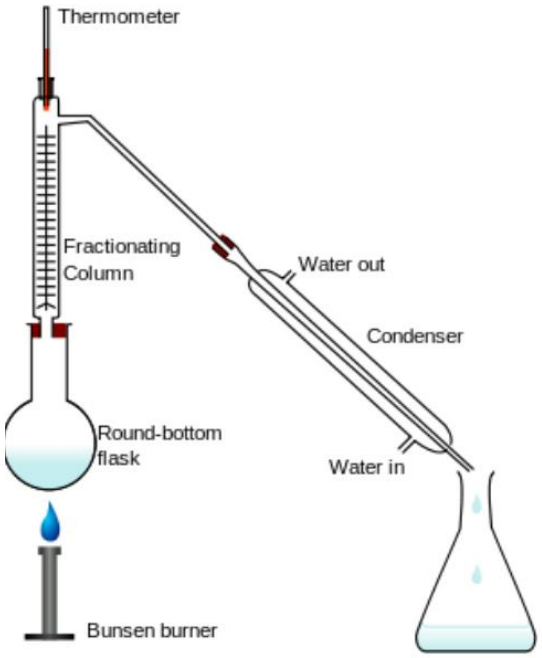
0. Outline

basic techniques to grow silicon and GaAs single-crystal ingots (锭).
Wafer-shaping steps from ingots to polished wafers.
Wafer characterisation in terms of its electrical and mechanical properties.

1. Silicon crystal growth from the melt

1.1 Starting material – ECS

- The starting material for silicon is a relatively pure form of sand (SiO2) called quartzite (石英岩).
- Is put in a furnace (窑炉) with various kinds of carbon to produce solid Si, gas SiO (Silicon monoxide) and CO (Carbon monoxide). The process produces metallurgical-grade silicon (冶金级硅，通常是通过热碳还原法从石英中提取的) with a purity of ~98%.
- The next step is producing ''trichloro'silane (三氯硅烷) with solid silicon and hydrogen chloride.
- Use the distillation method (e.g. fractional distillation, 分馏) to remove the impurities.

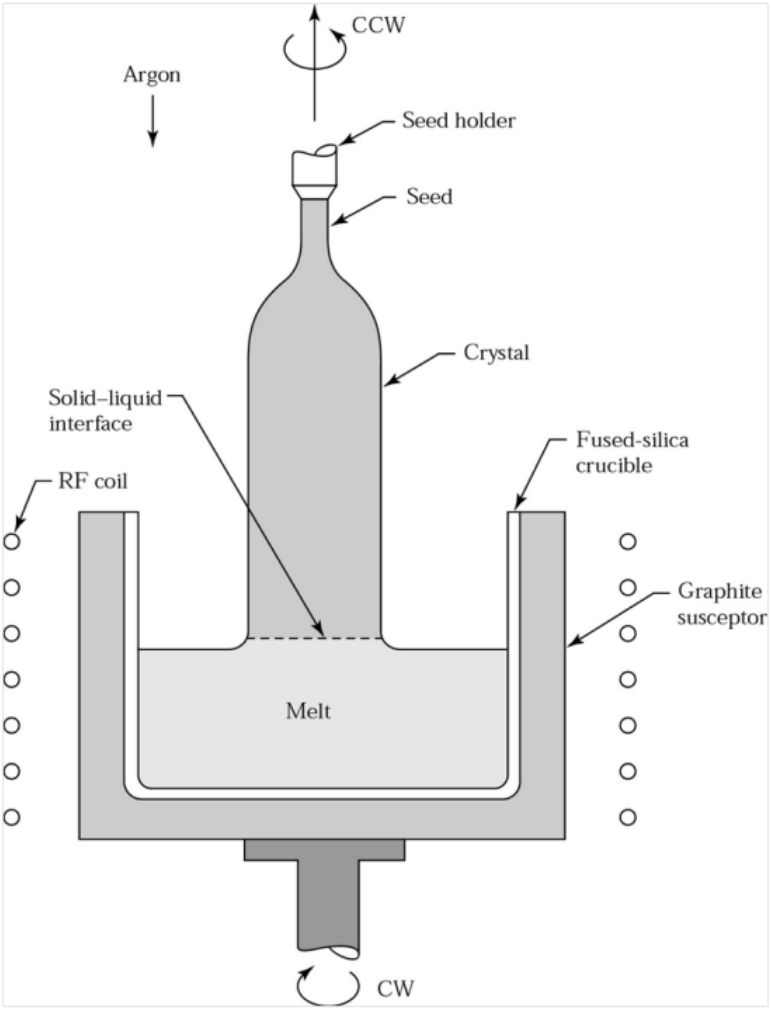


- The purified trichlorosilane is then used in a hydrogen reduction reaction (氢还原反应) to prepare the electronic-grade silicon. (ECS) → a high-purity polycrystalline material. (杂质浓度

一般在十亿分之一范围内)

1.2 The Czochralski technique

- Uses a device called a crystal puller.
- 3 main components:
  a) A furnace (熔炉) → a fused-silica crucible (坩埚), a graphite susceptor (石墨承烧体), a rotation mechanism (CW), a heating element + a power supply. → 图中底部的那一部分
  b) A crystal-pulling mechanism → a seed holder + a rotation mechanism (CCW)
  c) An ambient control (环境控制) → a gas source, a flow control + an exhaust system (排气系统)



- The process of the Czochralski technique
  a) Polycrystalline silicon (ECS) is placed in the crucible. The furnace is heated above the melting temperature of silicon/
  b) A suitably oriented crystal seed is suspended (悬挂) over the crucible in a seed holder. The seed is inserted into the melt. The tip of the remaining seed crystal still touches the liquid surface.
  c) Then the seed crystal is slowly withdrawn. (典型拉晶速度是每分钟几毫米)

1.3 Distribution of dopant

- A known amount of dopant is added to the melt to obtain a certain doping concentration. For silicon, boron (硼, B) and phosphorus (磷, P) are the most common dopants for p- and n-type

materials.

- During the crystal-pulling process, the doping concentration in the crystal/solid may differ from that in the melt/liquid.
- Define the equilibrium segregation coefficient (平衡分凝系数) $k_0 \equiv \frac{C_s}{C_l} < 1$ (typically)
- The doping distribution in the crystal is given by

$$C_s = k_0 C_0 \left(1 - \frac{M}{M_0}\right)^{k_0 - 1}$$

- 计算的时候可以假设 melt 的质量 M0 足够大，省略后面的指数项；有时需要假定 pull 出来的晶体质量和初始 melt 质量相同；

1.4 Effective segregation coefficient

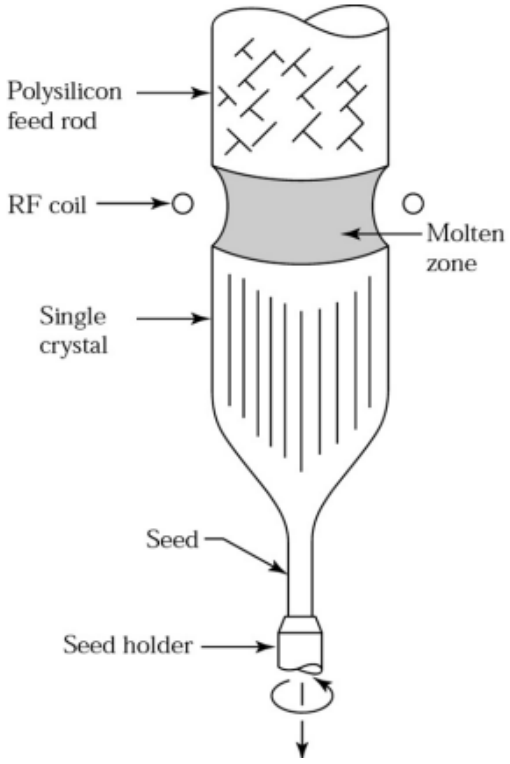
- If the rejection rate is higher than the rate at which the dopant can be transported away by diffusion, then a concentration gradient will develop at the interface.
- We can define an effective segregation coeff. which illustrates the impurity concentration far away from the interface. (always larger than k0, because the doping concentration far away form the interface is always lower than that of the liquid-solid interface)

$$k_e \equiv \frac{C_s}{C_l} = \frac{k_0}{k_0 + (1 - k_0)e^{-v\delta/D}}$$

- In order to obtain uniform doing distribution (ke=1), these approaches can be implemented
  a) a high pull rate v
  b) slow rotation, since sigma is inversely proportional to the rotation speed.
  c) Add ultrapure polycrystalline silicon continuously to the melt.

  总之实现均匀掺杂的目的就是为了减小指数项，例如增大提拉速度可以增加对流 (convection), 捕捉更多杂质进入固相等；

2. Silicon float-zone process



- The float-zone method can be used to grow silicon that has lower contamination (污染) than the Czochralski technique.
- A high-purity polycrystalline rod with a seed crystal at the bottom is held in a vertical direction and rotated. The rod is enclosed in a quartz envelope within which an inert (惰性的) atmosphere (argon, 氩气) is maintained.
- During the operation, a small zone (几厘米) of the crystal rod is kept molten by a radio-frequency (RF) heater, which is moved from the seed upward so that this floating zone traverses (穿过) the length of the rod.
- As the floating zone moves upward, single-crystal silicon freezes at the zone's retreating (后退) end and grows as an extension of the seed crystal (作为种子晶体的外延生长).
- Since no crucible is used, there is no contamination from the crucible.
- Are used mainly for high-power, high-voltage devices where high resistivity is required.
- 类似的描述掺杂浓度的公式：

$$C_s = C_0\left[1 - 1(1 - k_e)e^{-k_e x/L}\right]$$

L the length of the molten zone at a distance x along the rod.

- Both methods can be used to remove the impurities, however,
  a) A single path in the float-zone method behaves worse than a single Czochralski growth.
  b) However, it is much easier to perform the float-zone passes on a rod.
  c) Thus, multiple float-zone process (zone-refining technique) is used to provide a very high purity level of the raw material.

3. GaAs crystal growth techniques

3.1 Starting material

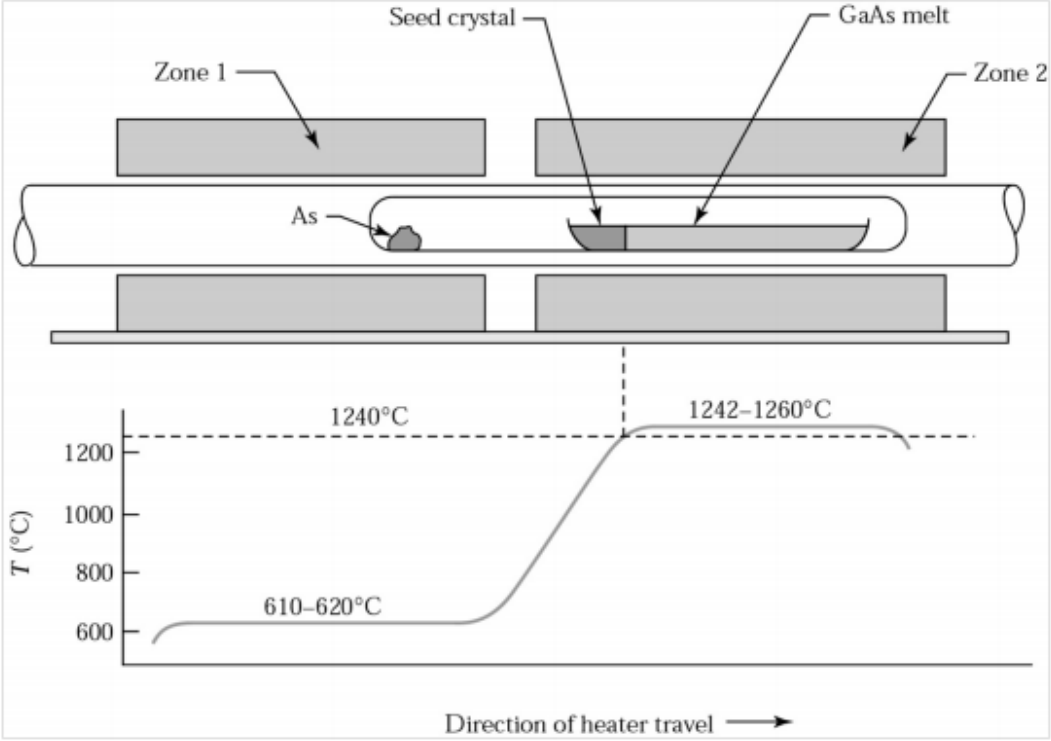
- The starting materials for the 'synthesis of polycrystalline gallium arsenide are the elemental (基本的), chemically pure gallium and arsenic.
- Phase diagram: shows the relationship between the two components as a function of temperature. A phase is a state in which a material may exist. 相图分析 Slide P38
- To synthesise GaAs, an evacuated (真空的), sealed (密封的) quartz tube system with a 2-temperature furnace is commonly used. The high-purity arsenic/gallium is placed in the 2 graphite boat and heated. Under certain conditions, an overpressure of arsenic is established to cause the transport of arsenic vapor to the gallium melt, converting it into GaAs, and preventing the decomposition of the GaAs while it is being formed in the furnace. (防止产物被分解). The produced high-purity polycrystalline GaAs serves as a raw material to grow single-crystal GaAs.
- GaAs 的掺杂：Slide P48 e.g. Zinc for p-type, Silicon for n-type.

3.2 Crystal growth techniques

- The Czochralski technique
  a) More popular for the growth of larger-diameter GaAs
  b) To prevent the decomposition of the melt, a liquid encapsulation (封装) method is employed.
  c) The liquid is melton boron trioxide (B2O3) layer as a cap about 1cm thick. Molten B2O3 is

inert to the GaAs, preventing the decomposition of the melt as long as the pressure on ites surface is higher than 1 atm. B2O3 can dissolve (溶解) SiO2, so the graphite crucible is used

- The Bridgman technique



a) A 2-zone furnace is used. The left-hand zone is held at a tempature to maintain the the required overpressure of As, whereas the right-hand zone is held just above the melting point if GaAs.
b) The boat is loaded with a charge of polycrystalline GaAs with the As kept at the other end of the tube.
c) As the furnace is moved toward the right, the melt cools at one end. The gradual freezing (solidification) of the melt allows a single crystal to propagate at the liquid-crystal surface. (from a seed crystal with a certain orientation of course.)

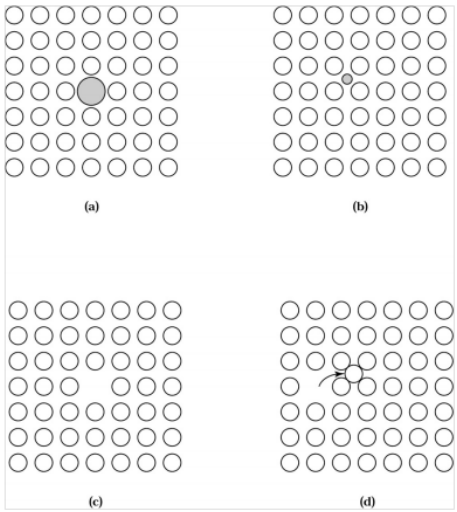
4. Material characterization

4.1 Wafer shaping

- 1st step: remove the seed crystal & the other end of the ingot, which is last to solidify.
- 2nd step: grind the surface so that the diameter of the material is defined.
- 3rd step: one or more flat regions are ground along the length of the ingot (不是很懂 Slide P52)
- 4th step: be sliced by diamond saw into wafers.
  Thickness, taper (which is the wafer thickness variations from one end to another), bow (which is the surface curvature of the wafer), surface orientation.
- 5th step: using a mixture of Al2O3 and glycerine (甘油) to lap (研磨), producing a typical flatness uniformity within 2 um. The lapping damage/contamination can be removed by etching.
- Final step: polishing → to provide a smooth, specular (镜子一样的) surface
- Notice: GaAs is more fragile than silicon.

4.2 Crystal defects

- Point defects
  a) Any foreign atom incorporated into the lattice at a substitutional site. 置换杂质
  b) Any foreign atom incorporated into the lattice at an interstitial (间隙的) site. 间隔杂质
  c) A missing atom in the lattice that creates a vacancy.空位缺陷
  d) Frenkel defect: a host atom that is situated (坐落于) between regular lattice sites (规则晶格的位置) and adjacent to a vacancy (且在一个空缺边上)
  e) Important in the kinetics (动力学) of oxidation and diffusion.



- Line defects
  a) Edge dislocation 刃型位错: An extra plane of atom AB is inserted.
  b) Screw dislocation 螺型位错: cutting the crystal partway (部分地) through and pushing the upper part one lattice spacing over. 切一半，把上面一半平推一个晶格长度
  c) Act as precipitation sites (沉积位置) for metallic impurities, degrading device performance.

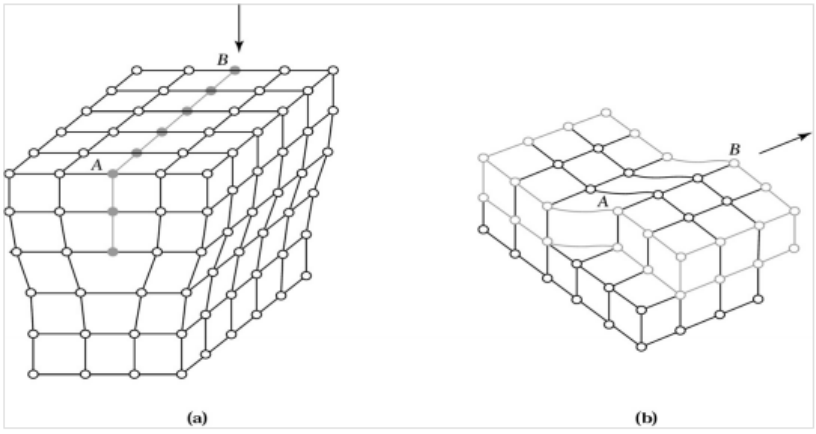


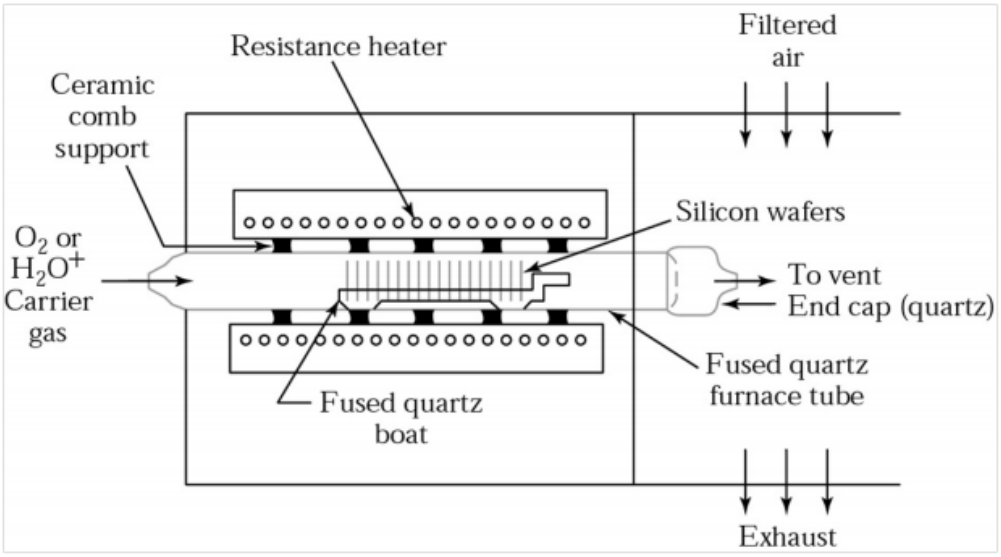
Figure 1.15: (a) Edge and (b) screw dislocation formation in cubic crystals.

- Area defects
  a) Stacking fault: ABC ABC ABC → ABC C ABC / ABC AB ABC ...
  b) Twins (孪生, 面内晶向改变) and grain boundaries (晶界, 两个取向之间的过渡状态)
- Volume defects
  Caused by dopants.

Silicon Oxidation

- Oxidation typically means the growing process of a silica layer on top of the silicon surface.
- GaAs have no native and stable oxides. → Si has a very stable oxide → popular.
- 2 groups of oxides:
  a) Grown directly on silicon ('thermal' oxides) → 'oxidation'
  b) Deposited from gas phase without silicon surface presenting. → 'deposition'

1. Basic thermal oxidation apparatus



- Consists of a resistance-heated furnace, a cylindrical fused-quartz tube containing the silicon wafers + a source of pure dry oxygen/ pure water vapor
- The loading end of the furnace tube protrudes (突出) into a vertical flow hood (流罩) where a filtered flow of air is maintained (被保持的). → to reduce the contamination and reduce dust and particulate matter.
- Typical temperature: 900-1200℃; gas flow: 1L/min.
- Microprocesses are implemented to
  a) Control the automatic insertion and removal of silicon wafers.
  b) Regulate the gas flow sequence 调节气体流动顺序
  c) Ramp (斜坡) the temperature up/down so that the wafers will not warp (弯曲) due to sudden temperature change.
  d) Matain the oxidation temperature to within +-1℃

2. Chemical reaction

– in oxygen (dry oxidation):

$$Si(solid) + O_2(gas) \rightarrow SiO_2(solid)$$

– or water vapor (wet oxidation):

$$Si(solid) + 2H_2O(gas) \rightarrow SiO_2(solid) + 2H_2(gas)$$

-

- The SiO2 interface moves into the silicon during the oxidation process.
- The basic structural unit of thermally grown SiO2: a silicon atom surrounded tetrahedrally (四面体地) by four oxygen atoms.
- Silica has several crystalline structures (e.g. quartz). When silicon is thermally oxidized, the SiO2 structure is amorphous. (无定形的) → no periodic structure at all. → relatively open structure accounts for the lower density and allows a variety of impurities to enter and diffuse readily (容易地) through the SiO2 layer.

3. Kinetics of growth

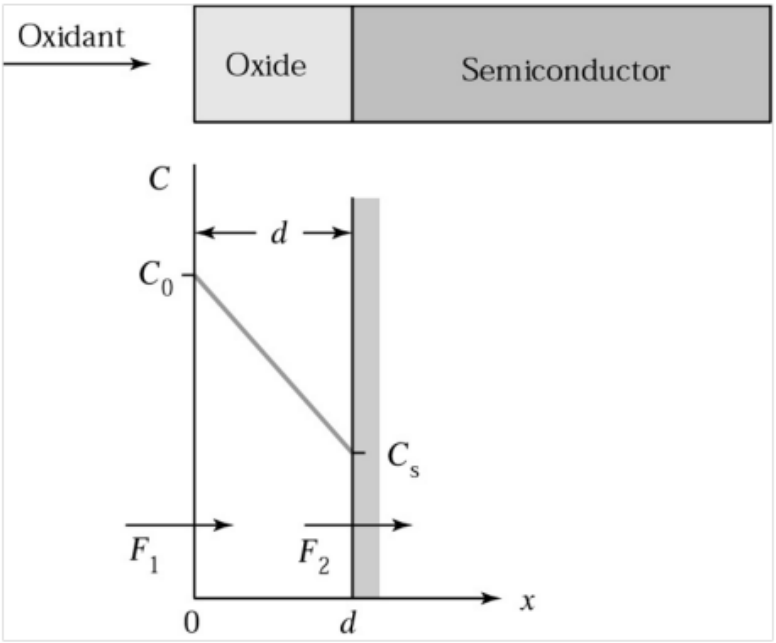


Figure 2.3: Basic model for the thermal oxidation of silicon

- During the early stages of oxide growth, when surface reaction is the rate-limiting factor, the oxide thickness varies linearly with time. As the oxide layer becomes thicker, the oxidant must diffuse through the oxide layer to react at the silicon-silicon dioxide interface, and the reaction become diffusion-limited → parabolic growth rate

$$x = \frac{D}{\kappa}\left[\sqrt{1 + \frac{2C_0\kappa^2(t+\tau)}{DC_1}} - 1\right]$$

For samall t → linear growth rate; lager t → parabolic growth rate
或者写成另一种更紧凑的形式

$$\text{Linear range: } x = \frac{B}{A}(t+\tau)$$

$$\text{Parabolic range: } x^2 = B(t+\tau)$$

两个系数分别称为 linear rate constant 和 parabolic rate constant (注意这里可能有计算 Slide P21)

- Under a given oxidation condition, the linear rate constant depends on crystal orientation. This is because the rate constant is related to the rate of incorporation of oxygen atoms into the silicon. → surface bond structure dependent → e.g. the density od available bonds on <111> is higher than that on the <100> plabe,

- The parabolic rate constant is independent of crystal orientation. → it is a measure of the diffusion process of the oxidising species through a random network layer of amorphous silica.
- Dry oxidation 质量好，但是时间更长 (chemical equilibrium constant?)
- Relatively slow growth rate must be used to reproducibly (可再生产地) grow thin oxide films of precise thickness.
  a) 纯氧+低温 → mainstream approach
  b) 低压
  c) 加惰性气体 inert gas with reduced partial pressures of O2 (都可以从化学平衡常数角度理解)
  d) 使用 modern vertical oxidation furnaces → 现代垂直氧化炉

4. Impurity redistribution during oxidation

- Dopant impurities near the silicon surface will be redistributed during the thermal oxidation. Due to several factors.
  a) Impurity redistribution when 2 solid phases are brought together untill equilibrium → define the segregation coefficient. (和之前拉晶时定义的差不多一样)

$$k = \frac{\text{Equilibrium concentration of impurity in silicon}}{\text{Equilibrium concentration of impurity in } SiO_2}$$

  b) Impurity may diffuse rapidly through the SiO2 into the gaseous ambient. (气体环境)
  c) The oxide is growing, and thus the boundary between the silicon and the oxide is advancing into the silicon as a function of time. → depends on how rapidly the impurity can diffuse through the oxide.
  d) 具体描述，阅读教材 P32；总地分成两大类，分别是 k>1 ：氧化物倾向于拒绝杂质离子/k<1：氧化物倾向于吸收杂质离子 两种情况；还与扩散速度有关。
  e) 即使 k=1，由于生长的二氧化硅层相同摩尔数体积较大，杂志例子依然会重新分布导致耗尽。

5. Masking properties of silicon dioxide

- A silicon dioxide layer can provide a selective mask against the diffusion of dopants at elevated temperatures.
- The diffusivities of P, Sb (锑, antimony), As and B are all orders of magnitude less than their corresponding values in silicon, while for Ga and Al is not the case. (SiN is used instead)

6. Oxide thickness characterization

- The simplest method for determining the thickness of an oxide: compare the color with a reference. → interference
- Profilometry: a mechanical method. A step feature in the film is created by etching / masking during deposition; then the profilometer drags a fine stylus (细针) across the film surface and a signal variation indicates the step height. → 100nm~>5um
- Ellipsometry: changes in polarization are a function of the optical properties including complex refractive index, thickness, operating wavelength & angle of incidence.

Photolithography

- Photolithography is the process of transferring patterns of geometric shapes on a mask to a thin layer of photosensitive material (photoresist) covering the surface of a semiconductor wafer.
- The resist patterns defined by the lithographic process are not permanent (永久的) elements of the final device, but only replicas (复制品) of circuit features. To produce circuit features, these resist patterns must be transferred once more into the underlying layers comprising (由...构成) the device (etching).

1. Cleanroom

- A cleanroom has a controlled level of contamination. Two systems are used to define the classes of a clean room.
  a) English system: the maximum allowable number of particles that are 0.5um and larger per cubic foot.
  b) Logarithm of the maximum allowable number of particles that are 0.5um and larger per cubic meter.
- Controlling the air plays a significant role when designing a cleanroom. 2 kinds of controlling methods;
  a) Turbulent cleanroom (湍流超净间)
     Turbulent airflow uses both laminar air flow hoods and nonspecific velocity filters to keep air in a cleanroom in constant motion, although not all in the same direction.
  b) Laminar cleanroom (层流超净间)
     laminar air flow systems direct filtered air downward in a constant stream towards filters located on walls near the cleanroom floor or through raised perforated floor panels.

2. Exposure tools

- The performance of an exposure tool is determined by three parameters: resolution, registration and throughput (一小时的产量).

  - Resolution
    - minimum feature dimension that can be transferred with high fidelity
  - Registration
    - how accurately patterns on successive masks can be aligned with respect to previously defined patterns on the wafer
  - Throughput
    - the number of wafers that can be exposed per hour for a given mask level

- There are basically 2 optical exposure methods
  a) Shadow printing
     Has the mask and wafer in direct contact with one another (contact printing) or in close proximity (邻近的, proximity printing)
     其中, contact printing suffers a major drawback caused by dust particles which may cause permanent damage to the mask and results defects in the wafer with each eucceeding exposure.
     为了避免模具损坏，采用了 proximity printing. There is a small gap (10-50um) between the wafer and the mask during exposure. → diffraction at feature edges on the photomask → some light penetrates (穿透) into the shadow region → resolution degraded to 2-5 um range, 公式给出，波长越短、间距（包括 photoresist 的厚度）越小，分辨率就越高。但是间距变小就可能导致 dust 对模具的损坏。所以使用接下来的这种方法。
  b) Projection printing
     To increase the resolution, only a small portion of the mask is exposed at a time. The small image area is scanned or stepped over the wafer to cover the entire wafer surface.
     有以下几种：Annual-field wafer scan; 1:1 step-and-repeat; M:1 reduction step-and-repeat; M:1 reduction step-and-scan 注意 1：1 的光学系统设计比较简单，但是没有缺陷的 mask 制作比较复杂，反之亦然。且在进行 reduction step-and-scan 的时候，mask 的移动速度要比 photoresist 的移动速度快 M 倍。
     注意，减小波长和增大数值孔径都可以增加分辨率，但是增大 NA 的同时 DOF（景深）会呈二次方减小， which means the tolerance of im-flatness of the wafer decreases. 所以主流的提高分辨率的办法都是减小波长。

$$l_m = k_1 \frac{\lambda}{NA}$$

$$DOF = \frac{\pm l_m/2}{\tan\theta} \approx \frac{\pm l_m/2}{\sin\theta} = k_2 \frac{\lambda}{(NA)^2}$$

$$with\ k\ the\ process - dependent\ factor$$

- 浸没光刻（Immersion Lithography）是一种先进的光刻技术，用于制造半导体芯片和其他微电子器件。它是在传统干式光刻（Dry Lithography）基础上发展起来的，通过在光刻系统的透镜和晶圆之间引入液体介质来提高分辨率和景深。

3. Masks

- The mask consists of a fused-silica substrate covered with a chromium (铬) layer. 掩膜是熔融石英基板镀了一层铬；
- The digital data produced by the CAD system then drives a pattern generator, which is an e-beam lithographic system.
- The thickness is required to minimize pattern placement errors due to substrate distortion. The fused-silica plate is needed for its low coefficient of thermal expansion, high transmission at shorter wavelengths and mechanical strength.
- We can define 'yield', which is the ratio of good chips per wafer to the total number of chips per wafer, which is exponentially inversely proportional to the defect density & the defect-sensitive area.

4. Photoresist

- Photoresist is a radiation-sensitive compound that can be classified as positive or negative,
  a) Positive photoresist
     The exposed regions become more soluble → The patterns formed in the positive resist are the same as those on the mask.
  b) Negative photoresist
     The exposed regions become less soluble → The patterns formed in the negative resist are the reverse of the mask patterns. → make use of the polymer cross-linking reaction (聚合物交联反应) → the whole resist mass swells (膨胀) by absorbing developer solvent (显影剂) → degraded solution
- Spin coating photoresist is a commonly used technique for uniformly applying photoresist onto the surface of a wafer or other substrates.
- 显影过程：photoresist development – 湿显影/wet development
  a) Immersion development (浸入显影): wafer dipping + slow movement
     Easy, but changing concentration of developer due to addition of dissolved resist in the developer. 显影液浓度会变
  b) Puddle development: Add developer to the surface of the wafer and spin it to remove excess (多余的) developer. → expensive.
- The response curve describes the percentage of resist remaining after exposure and development versus the exposure energy.
  a) Threshold energy: as the exposure energy increases, the solubility gradually increases until at a threshold energy E_T, the resist becomes completely soluble.
- 正阻片的灵敏度定义中的 E1 指在 E_T 处画切线，达到 100%不溶时得到的能量。→ larger sensitivity, sharper the patterns.
- The edge of the resist image is generally not at the vertically projected positions of the mask edges because of the diffraction. The edge of the resist image corresponds to the position where the total absorbed optical energy = E_T (curved edge because the solubility gradually increases)
- 负阻片的灵敏度定义为 the energy required to retain (保留) 50% of the original resist film thickness in the exposed region.

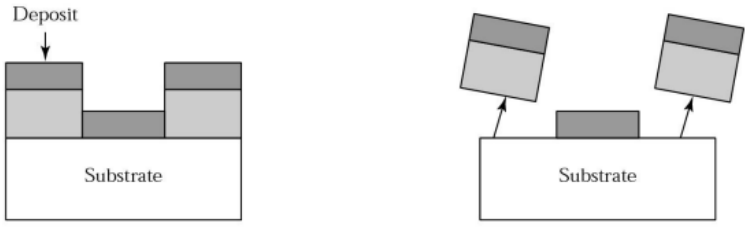
5. Pattern transfer

- Now let us describe the whole process of transferring IC patterns from mask to silicon wafer with SiO2 layer.
  a) 黄光超净间(光刻胶不敏感) + adhesion promoter (promoting a chemically compatible surface for the resist)
  b) Spin coating 涂上光刻胶
  c) Soft bake (pre-baking): 90-120 deg for 60-120s to remove the solvent from the photoresist film and to increase resist adhesion to the wafer.
  d) UV exposure 光刻，把 mask 上 pattern 转移到光刻胶上，可正可负
  e) Flooding the wafer with the developer solution 显影液冲洗
  f) Wafer rinsing (漂洗) and drying

g) Post bake (hard bake) at 100-180 deg to increase the adhesion of the resist.

h) Etching of the (un)exposed insulation layer 蚀刻暴露的绝缘层，得到正片 or 负片

- Liftoff technique: use a positive resist → 高分辨率 Slide P63 是什么？

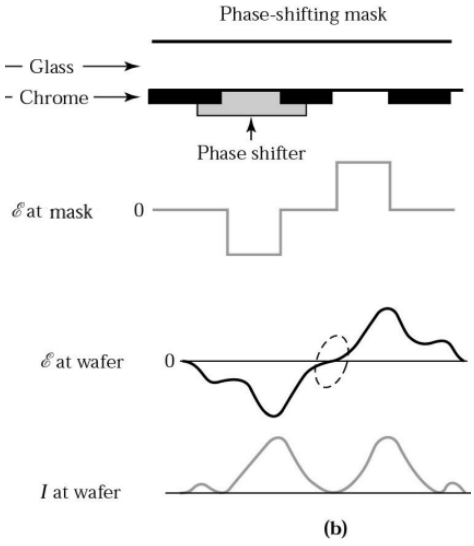


- The film (e.g., aluminum) is deposited
- The film thickness must be smaller than that of the resist
- Those portions of the film on the resist are removed by selectively dissolving the resist layer in an appropriate liquid etchant so that the overlying film is lifted off and removed

6. Resolution enhancement technique

- Phase-shifting mask (PSM)

- The phase-shift layer that covers adjacent apertures reverses the sign of the electric field
- Because the intensity at the mask is unchanged, the electric field of the images at the wafer can be cancelled
- Images that are projected close to one another can be separated
- A 180 ° phase change is obtained by using a transparent layer of thickness d = λ/2 (n-1)



- Optical proximity correction (OPM)
  Use modified shapes of adjacent sub-resolution geometry to improve imaging capability. 使用相邻亚分辨率几何形状。

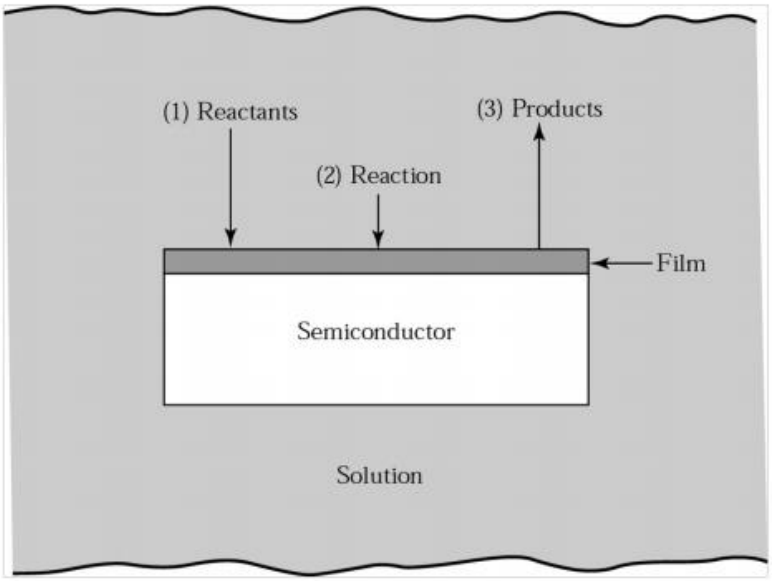
7. Next-generation lithographic methods Slide P77 必须看，有相关题目

- E-beam lithography: DOF 比较大，不需要 mask，可以生成 submicron 图案；但是慢
- Extreme UV lithography
- X-ray lithography
- Ion beam lithography: 分辨率最高；

Etching

1. Wet chemical etching

- The mechanisms for wet chemical etching involve 3 essential steps



  a) The reactants (反应物) are transported by diffusion to the reacting surface
  b) Chemical reactions occur at the surface
  c) The products from the surface are removed by diffusion
- For immersion etching (浸泡蚀刻), the wafer is immersed in the etch solution, and mechanical agitation is usually required to ensure etch uniformity and a consistent (一致的) etch rate.
- Spray etching has gradually replaced immersion etching because it greatly increases the etch rate and uniformity by constantly supplying fresh etchant to the wafer surface.
- Etching uniformity must be required under any variations.

$$\text{Etch rate uniformity (\%)} = \frac{\text{Maximum etch rate} - \text{Minimum etch rate}}{\text{Maximum etch rate} + \text{Minimum etch rate}} \times 100\%$$

- Etching process can also be used to lapping & polishing to gice an optically flat, damage-free surface (Ch1), to remove contamination

2. Silicon etching

- For semiconductor materials, wet chemical etching usually proceeds by oxidation, followed by the dissolution of the oxide by a chemical reaction (先氧化，再除氧化物).
- For silicon, the most commonly used etchants: HNO3 (nitride acid) +HF (hydrofluoric acid) in water (as diluent 缓冲剂)/CH3COOH (acetic acid) → 硝酸作为强氧化剂 (Strong oxidants) 先氧化 Si，氧化物再有氢氟酸除去。
- Some etchants dissolve a given crystal plane of single-crystal silicon much faster than another plane. 例如硅的<111>面化学键更多，理论上蚀刻速率应该更慢。
- We can use the large orientation dependence in the etch rates to fabricate device structures with submicron feature lengths. E.g. silicon V-grooves to align and fix the fiber.
- For example, <100> silicon's etching creates V(or U)-shaped grooves, and the width of the

bottom surface is given by

$$W_b = W_0 - 2l\cot\ 54.7°$$

3. SiO2 etching

- Notice that a loosely structured oxide formed by chemical vapor deposition or sputtering (溅射) exhibits a faster etch rate than thermally grown oxide.

4. SiN, Al, GaAs etching: 略

5. Wet v.s. Dry etching

- Most of the layer materials are amorphous or polycrystalline thin films, resulting in isotropic etching rate for wet etching → undercut (根切) of the layer underneath the mask → a loss of resolution
- Define the degree of anistropy

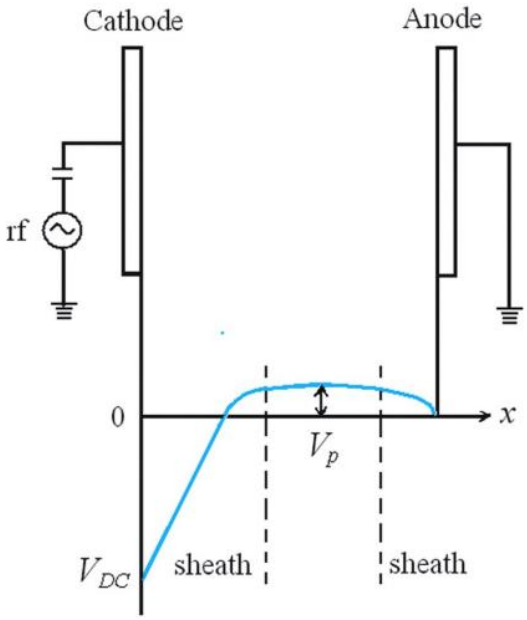
$$A_f \equiv 1 - \frac{l}{h_f} = 1 - \frac{R_l t}{R_v t} = 1 - \frac{R_l}{R_v}$$

In practive, the value of Af is chosen to be close to unity → anisotropic etching must be used. →dry etching→also plasma-assisted etching.

6. Plasma fundamentals

- A plasma is a fully or partially ionized gas composed of (由...组成) equal numbers of positive and negative charges and a different number of unionized molecules.
- A plasma is produced when an electric field of sufficient magnitude is applied to a gas, causing the gas to break down and become ionized.
- The plasma is initiated (发起) by free electrons that are released by e.g. field emission from a negatively biased electrode
- The free electrons gain kinetic energy from the electric field. When they travel through the gas, the collision causes energy transversion.
- Therefore, when the applied voltage is larger than the breakdown potential, a sustained plasma is formed throughout the reaction chamber.
- Capacitively coupled (rf) plasma etcher 电容耦合等离子蚀刻机
  a) The cathode (阴极) is capacitively (电容式的) coupled to an rf generator, anode is grounded. 阴极串一个电容+射频发生器，阳极接地
  b) Since electrons are more mobile than positive ions, more electrons are attracted to the front surface of the electrodes during the positive half cycle. 加电压后电极之间的气体被电离成电子和正离子，由于电子移动性更强，所以前半段电极上的电子更多 → current is larger in the positive half cycle
  c) Resultant electron current charges up the capacitively coupled electrode 电流给电容充电。（假设击穿电压无限大）
  d) Cathode acquires an increasing negative bias voltage (self-bias) during successive cycles. 随着电子在阴极累计，阴极表面的负偏压电压逐渐增加。自偏压的形成是因为阴极通过电容耦合方式连接到射频电源，因此没有直接的电流流动来中和这些电荷。

e) Then the plasma forms a compensating positive potential Vp relative to the grounded anode. E.g. sheath 鞘层，在阴极和等离子体之间形成，这个鞘层中电位迅速变化，从阴极的负电位到等离子体的正电位；鞘层内的电场阻止电子进入鞘层，同时推动正离子进入阴极，从而维持电中性。典型的在 10um-1mm, conformal (共形) with the electrode surface.



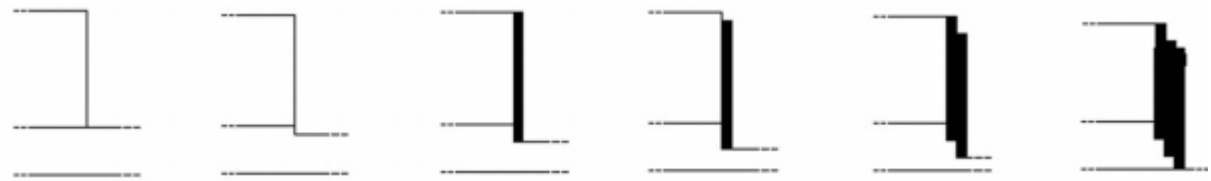
f) Thus, positive ion energy gain is primarily (主要地) in the direction normal to the surface and the ion beam is essentially (本质上) unidirectional → anisotropic etching

g) Anisotropic relies on the bombardment (冲击) of unidirectional energetic ions at the substrate surface, which can be placed on the cathode or anode.

h) 阴极上的电压大很多→ anisotropic etching is very strong on the cathode surface due to the strong field, and is weaker on the anode.

7. Surface chemistry

- Requirement: 侧壁和底部的几何结构，selectivity 选择性、均匀蚀刻、与其他工艺的兼容
- Physical sputtering 物理溅射
  One of the simplest material removal processes. → bonbardment of target material by energic ions or neutrals. →non-selective
- Reactive ion etching (RIE, 反应离子蚀刻)
  大部分用这个办法 → relatively more selective → simultaneous bombardment of energetic ions and reactive neutral radicals onto the material surface. 高能离子和活性中性自由基同时轰击材料表面，自由基腐蚀是各向异性的；
- Chemical etching
  例如用氟 (fluorine) 蚀刻硅；基本上是各向同性的，除了一些和晶体取向有关的各向异性。
- Polymer deposition
  a) One surface mechanism is polymer deposition. The presence of films on vertical surfaces limits contact of the material surface with the etchant species to inhibit (抑制) horizontal etching.
  b) Mechanisms of the sidewall passivation (侧壁钝化):
  • plasma discharges with carbon-containing source gases. → 含碳气体的分解产物沉积
  • The etch product species generated at horizontal surface exposed to ion bombaedment. →nonvolatile (不挥发性的) → stick to and react with vertical surfaces not exposed to ion bonbardment. → ‘redeposition’



- Substrate temperature
  One can vary the degree of anisotropic etching by varying the substrate temperature to control the feature profile.

8. Capacitively coupled plasma etchers

- 和之前的图一样，
- 放在 anode: plasma etching mode with energetic ion bombardment→the plasma potential is always above the grounded potential.
- 放在 cathode: reactive ion etch mode with higher energetic ion bombardment due to higher self-bias.

9. Plasma diagnostics (诊断) and end-point control

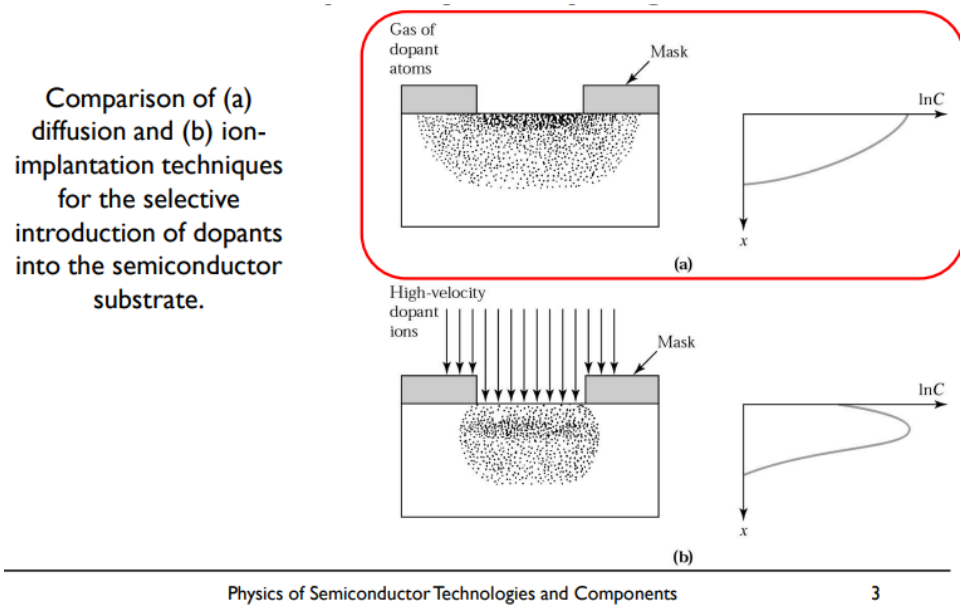
- Most processing plasmas emit radiation in the range from infrared to ultraviolet. 用 optical emission spectroscopy 判断发射强度与波长的关系，确定 neutral and ionic species.
- Dry etching has less selectivity to the underlying layer → end-point detection is needed. → laser interferometry→通过反射光之间的相互干涉 → 蚀刻层要是透明/半透明的

10. Etching chemistries and applications

- Silicon etching 硅蚀刻： Chlorine-based (Cl-) and bromine-based (Br-) chemistries
- Dielectric etching 电介质蚀刻
- Interconnect metal etching 互联金属蚀刻

Diffusion

- Impurity doping is the introduction of controlled amounts of impurity dopants into semiconductors. Diffusion and ion implantation are the two key methods of impurity doping. For example, diffusion is used to form a deep junction, whereas ion implantation is used to form a shallow junction. 扩散形成深结，离子扩散形成浅结



Comparison of (a) diffusion and (b) ion-implantation techniques for the selective introduction of dopants into the semiconductor substrate.

1. Basic diffusion process

- Diffusion of impurities is typically done by placing semiconductor wafers in a carefully controlled, high-temperature (800-1200 deg for Si, 600-1000 deg for GaAs) quartz-tube furnace and passing a gas mixture that contains the desired dopant through it. The number of dopant atoms that diffuse into the semiconductor is related to the partial pressure of the dopant impurity in the gas mixture.
- Dopants can be introduced in several ways including solid/liquid/gaseous sources.
  - An example of the chemical reaction for phosphorus diffusion using a liquid source is

$$4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2 \uparrow$$

  - Phosphorus pentoxide P_2O_5 forms a glass-on-silicon wafer and is then reduced to phosphorus by silicon

$$2P_2O_5 + 5Si \rightarrow 4P + 5SiO_2$$

  - The phosphorus is released and diffuses into the silicon, and Cl_2 is vented

  Cl2: Chlorine;
- For diffusion in GaAs, the high vapor pressure of arsenic requires special methods to prevent the loss of arsenic by decomposition (分解) or evaporation (蒸发). → diffusion in sealed ampules (安瓿瓶) with an overpressure of arsenic / diffusion in an open-tube furnace with a doped oxide capping (覆盖) layer.
-

2. Diffusion equation

- Diffusion in a semiconductor can be visualized as the atomic movement of the diffusant (dopant atoms) in the crystal lattice by vacancies or interstitials (间质的). An atom smaller than the host atom often moves interstitially.
- Define flux, which is proportional to the concentration gradient → dopant atoms will diffuse away from a high-concentration region to a lower-concentration region
- Ficks diffusion equation:

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2}$$

Where C is the dopant concentration, D is the diffusion coefficient independent to C for a lower concentration. 我们结合实验结果把 D 唯象的写成， Ea is the activation energy.

$$D = D_0 \exp\left(\frac{-E_a}{kT}\right)$$

- For the interstitial diffusion model, Ea is related to the energies required to move dopant atoms from one interstitial site to another → fast diffusants
- For vacancy diffusion, Ea is related to both the energies of motion and the energies of formation of vacancies → slow diffsants

3. Diffusion profiles

- Diffusion profile of the dopant atoms is dependent on the initial and boundary conditions.
- Constant surface concentration
  Impurity atoms are transported from a vapour source that maintains a constant level of surface concentration during the entire diffusion period.
- Constant total dopant diffusion
  It is the gaussian distribution. Since the dopant will move into the semiconductor as time increases, in order to keep the total dopant S constant, the surface concentration must decrease.

4. Extrinsic diffusion

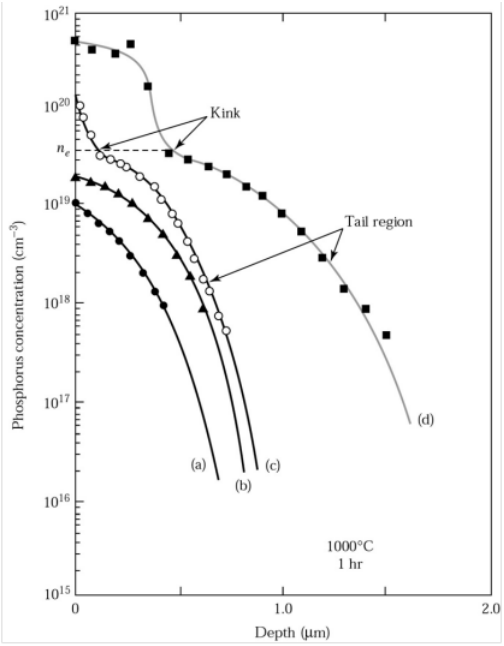
- The diffusion profiles described above are for constant diffusivities (D) → the doping concentration is lower than the intrinsic carrier concentration. 即掺杂浓度小于本征半导体载流子浓度的时候； → intrinsic diffusivity, intrinsic diffusion region
- However, when the impurity concentration increases, the semiconductor becomes extrinsic → in the extrinsic diffusion region, the diffusivity (D) becomes concentration-dependent.
- 可以考虑对扩散系数进行修正，并数值求解

$$D = D_s\left(\frac{C}{C_s}\right)^{\gamma}$$

- 可以发现修正系数大于 1 时，it results in an increasingly steep and boxlike concentration profile. → abrupt concentration profiles
- 特别地，修正系数为-2 时, leads to a concave profile, 末尾上升，和其他情况不一样

5. Different diffusion profiles 不用学！

- In silicon
  a) For boron & arsenic, correction factor=1 → abrupt concentration profiles
  b) For gold & platinum, correction factor=-2 → concave shaped
  c) For phosphorus, correction factor=2, however, because of a dissociation effect, the diffusion profile exhibits anomalous behaviour. 反常行为→ as the concentration increases, the profile begins to deviate from the simple expression.
  → at very high concentration, the profile near the surface is indeed similar to that $\gamma = 2$, however, at a certain concentration, a kink occurs and is followed by a rapid diffusion in the tail region.
  ➔ This concentration corresponds to an energy level, at which the coupled impurity-vacancy pair dissociates to P+, V- and an electron.
  ➔ Thus, the dissosiation generates a large number od singly charged acceptor vacancies V-, which in turn enhances the diffusion in the tail region of the profile.
  ➔ <u>Commonly used to form deep junctions. 和开头对应上了</u>



- In GaAs: Zinc is the most extensively studied diffusant, $\gamma = 2$, always extrinsic.

6. Lateral diffusion

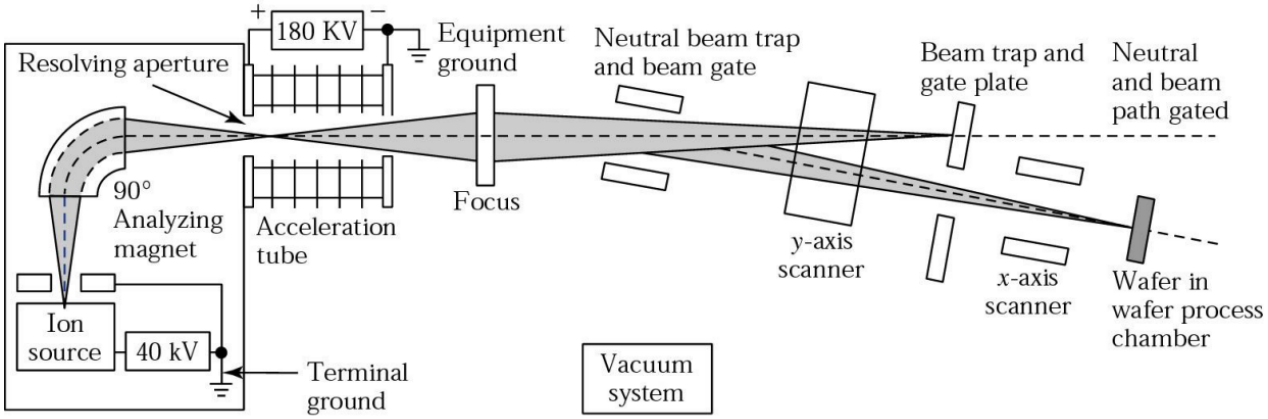
- Because of the lateral diffusion effect, the junction consists of a central plane region with approximately cylindrical edges with a radius of curvature. In addition, if the diffusion mask contains sharp corners, the shape of the junction near the corner will be roughly spherical because of lateral diffusion. → lower avalanche breakdown voltages→曲率半径小，电场大

Ion implantation

In this process the dopant ions are implanted into the semiconductor by means of an ion beam. The doping concentration has a peak distribution inside the semiconductor, and the profile of the dopant distribution is determined mainly by the ion mass and the implanted-ion energy,.

1. Medium-current ion implantor 中电流离子注入机

- Ion implantation is the introduction of energetic, charged particles into a substrate such as silicon.
- Implantation energies are between 1keV – 1MeV, resulting in ion distributions with average depths ranging from 10nm to 20um. → more precise control and reproducibility (可重复性) of impurity dopings + lower processing temperature



- Medium-current ion implantor
  a) The ion source has a heated filament (细线) to break up source gases into charged ions.
  b) An extraction voltage (40kV) causes the charged ions to move out of the ion-source chamber (腔体) into a mass analyser the magnetic field of the analyzer is chosen such that only ions with the desired mass-to-charge ratio can travel through it without being filtered.
  c) The selected ions then enter the acceleration tube, where they are accelerated to the implantation energy as they move from high voltage to ground.
  d) Apertures ensure that the ion beam is well collimated.
  e) The pressure in the implant is kept below 10-4 Pa to minimize ion scattering by gas molecules.
  f) The ion beam is scanned over the wafer surface using electro-static deflection plates 静电偏转板 and is implanted into the semiconductor.
  g) The energetic ions lose energy through collisions with electrons and nuclei (核) in the substrate
  h) The dopant dose can be controlled by monitoring the ion current during the implantation
  i) Side effects is disruption (击穿) or damage of the semiconductor lattice due to ion collision → annealing (退火) needed

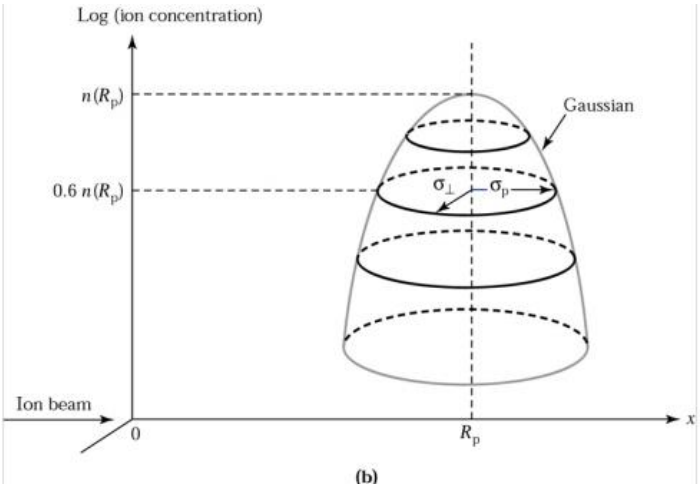
2. Ion distribution

- The total distance that an ion travels in （介词表达某个动作的状态或过程中）coming to rest

（动名词做补语，表示达到静止的过程） is called its range (R).

*e.g. She was injured in playing soccer.

- Because the number of collisions per unit distance and the energy lost per collision are random variables, there will be a spatial distribution of ions having the same mass and the same initial energy. → gaussian distribution



$$n(x) = \frac{S}{\sqrt{2\pi}\sigma_p} \exp\left[-\frac{(x-R_p)^2}{2\sigma_p^2}\right]$$

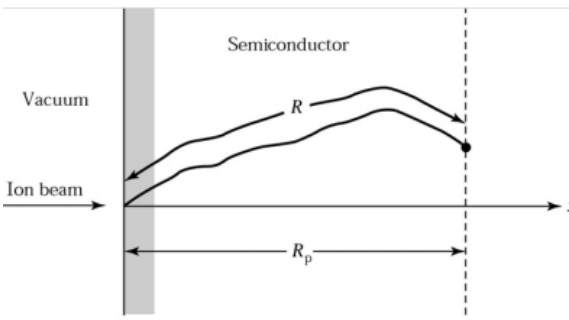
- Along the axis perpendicular to the implantation, the distribution is also Gaussian function. Because of this distribution, there will be some lateral implantation. → <u>but smaller than that from the thermal diffusion process.</u>
- Thus, for diffusion the maximum concentration is at x=0, whereas for ion implantation the maximum concentration is the projected range.

3. Ion stopping

- 2 mechanisms
  a) Tranfering its energy to the target nuclei → causes deflection (偏转) of the incident ion and dislodges (驱逐) many target nuclei from their original lattice sites.
  b) The interaction of the incident ion with the cloud of electrons surrounding the target's atom. → loss energy through Coulombic interaction → may cause excitation & ionization
  c) 可以定义能流表征能量损失速率

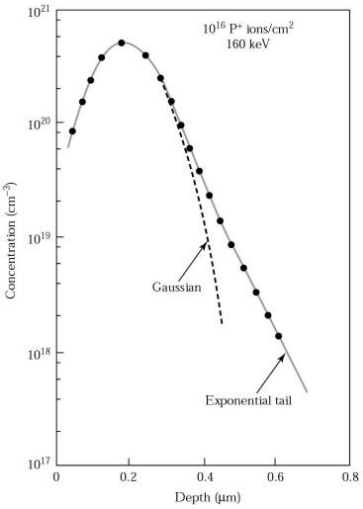
$$\frac{dE}{dx} = S_n(E) + S_e(E)$$

- Visualization: by elastic collision 弹性碰撞→maximum energy loss is a head-on collision 对心碰撞; → 碰撞过程能量是守恒的，但是碰撞过后能量散失了
- Calculations show that the nuclear stopping power increases linearly with energy at low energies. At high energies, Sn(E) (derivative with x-axis) becomes smaller because fast particles may not have sufficient interaction time with the target atoms to achieve effective energy transfer. 注意，这里讨论的是能量损失的速率与入射能量之间的函数;
- Heavier the atoms, larger the nuclear stopping power, larger the energy loss per unit distance.
- Once the S(E) is known, one can calculate the range R and the projected range Rp.
- The larger the energy loss, the smaller the range; also, the projected range and straggles increase with ion energy.
- Most popular dopants have larger Rp in Si than GaAs.



4. Ion channeling

- Silicon and GaAs behave as if they were amorphous when misoriented form the crystallographic direction.
- Ion channelling effect: channelling occurs when incident ions align with a major crystallographic direction and are guided between rows of atoms in a crystal, which forms the exponential tail.
- Ions implanted in the <110> direction will follow trajectories (轨迹) that will not bring them close enough to a target atom to lose energy in nuclear collisions → only electronic cloud stopping
- Can be minimized:
  a) Blocking amorphous layer (e.g. SiO2)
  b) Misorientation of the wafer
  c) Pre-damaging the wafer surface



5. Inplant damage

- Electronic collisions do not displace semiconductor atoms from their lattice positions. Only nuclear collisions can transfer sufficient energy to the lattice so that host atoms are displaced, resulting in implant damage (lattice disorder). → may cause the material become amorphous.
- Book P99