

| | Original | | Unrolled | |
|--|--------------------|---|--------------------|---|
| sim_seconds | 40.49874 | > | 39.35633 | # Number of seconds simulated |
| sim_ticks | 40,498,700,000,000 | > | 39,356,330,693,500 | # Number of ticks simulated |
| system.mem_ctrls.bw_read::cpu0.inst | 1,381 | < | 1,431 | # Total read bandwidth from this memory (bytes/s) |
| system.mem_ctrls.bw_read::cpu0.data | 1,542,780 | < | 1,587,772 | # Total read bandwidth from this memory (bytes/s) |
| system.mem_ctrls.bw_read::total | 1,544,161 | < | 1,589,203 | # Total read bandwidth from this memory (bytes/s) |
| system.mem_ctrls.bw_inst_read::cpu0.inst | 1,381 | < | 1,431 | # Instruction read bandwidth from this memory (bytes/s) |
| system.mem_ctrls.bw_inst_read::total | 1,381 | < | 1,431 | # Instruction read bandwidth from this memory (bytes/s) |
| system.mem_ctrls.bw_write::writebacks | 76,387 | < | 78,604 | # Write bandwidth from this memory (bytes/s) |
| system.mem_ctrls.bw_write::total | 76,387 | < | 78,604 | # Write bandwidth from this memory (bytes/s) |
| system.mem_ctrls.bw_total::writebacks | 76,387 | < | 78,604 | # Total bandwidth to/from this memory (bytes/s) |
| system.mem_ctrls.bw_total::cpu0.inst | 1,381 | < | 1,431 | # Total bandwidth to/from this memory (bytes/s) |
| system.mem_ctrls.bw_total::cpu0.data | 1,542,780 | < | 1,587,772 | # Total bandwidth to/from this memory (bytes/s) |
| system.mem_ctrls.bw_total::total | 1,620,548 | < | 1,667,808 | # Total bandwidth to/from this memory (bytes/s) |
| system.cpu0.dtb.rdAccesses | 11,461,623,462 | > | 11,337,041,862 | # TLB accesses on read requests |
| system.cpu0.dtb.wrAccesses | 2,973,804,875 | < | 2,983,388,075 | # TLB accesses on write requests |
| system.cpu0.dtb.rdMisses | 14,866 | = | 14,867 | # TLB misses on read requests |
| system.cpu0.dtb.wrMisses | 486 | = | 486 | # TLB misses on write requests |