Assignment No : 8

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Batch: A4

***P*roblem Statement :** Design Program using Control Transfer instruction using CPU simulator.

Code:

```
1,14,#FALSE#,#FALSE#,"abc_2",0,700,0,71,1,6,1767010425
0,0,0,0,0,0
0
0
0
0,4,"IN 0, R00",0,0,0,0,#FALSE#
6,4,"IN 0, R01",0,0,0,0,#FALSE#
12,1,"SUB #48, R00",0,0,0,0,#FALSE#
18,1,"SUB #48, R01",0,0,0,0,#FALSE#
24,0,"MOV #0, R02",0,0,0,0,#FALSE#
30,1,"ADD R00, R02",0,0,0,0,#FALSE#
```

35,1,"DEC R01",0,0,0,0,#FALSE#

38,2,"JNZ 30",0,0,0,0,#FALSE#

42,3,"CMP #9, R02",0,0,0,0,#FALSE#

48,2,"JLE 58",0,0,0,0,#FALSE#

52,1,"ADD #7, R02",0,0,0,0,#FALSE#

58,1,"ADD #48, R02",0,0,0,0,#FALSE#

64,4,"OUT R02, 1",0,0,0,0,#FALSE#

70,2,"HLT",0,0,0,0,#FALSE#

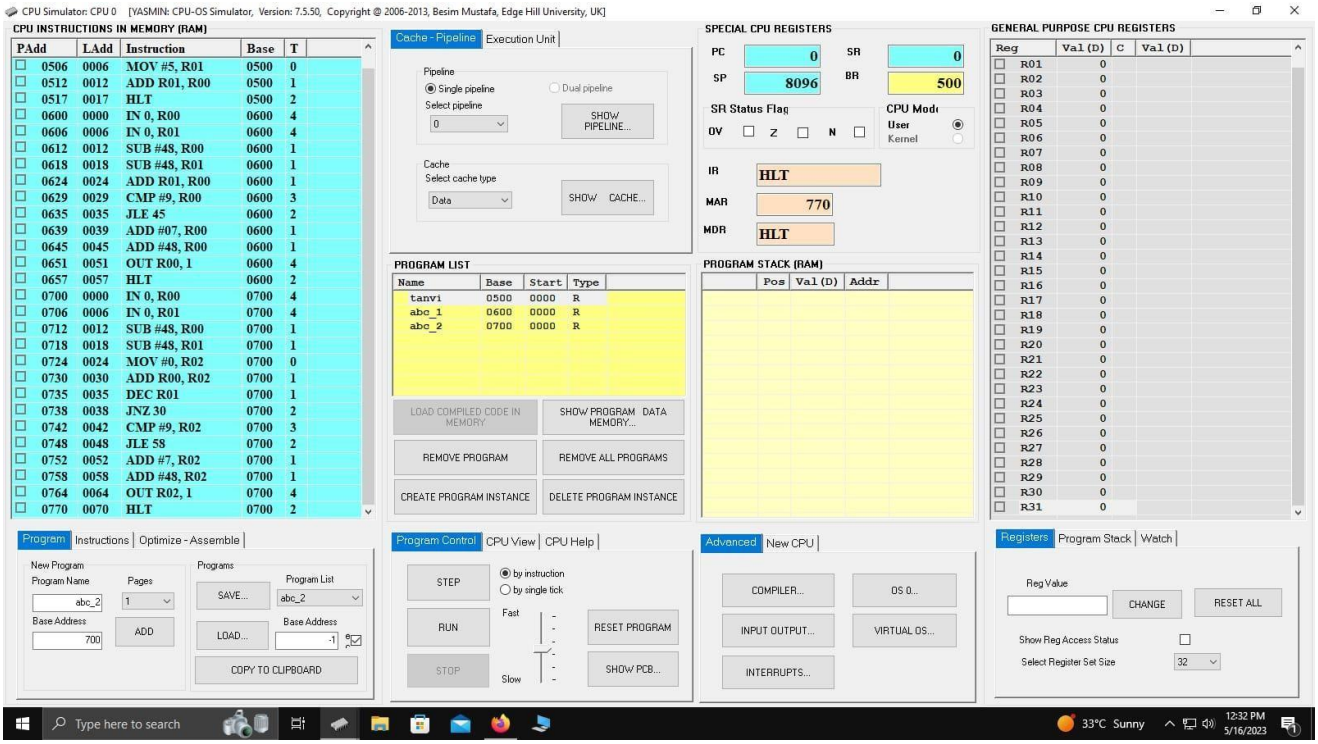
0

0

0

-1

Output:


CPU Simulator: CPU 0 [YASMIN: CPU-OS Simulator, Version: 7.5.50, Copyright @ 2006-2013, Besim Mustafa, Edge Hill University, UK]
CPU INSTRUCTIONS IN MEMORY (RAM)
PAdd LAdd Instruction Base T
0506 0006 MOV #5, R01 0500 0
0512 0012 ADD R01, R00 0500 1
0517 0017 HLT 0500 2
0600 0000 IN 0, R00 0600 4
0606 0006 IN 0, R01 0600 4
0612 0012 SUB #48, R00 0600 1
0618 0018 SUB #48, R01 0600 1
0624 0024 ADD R01, R00 0600 1
0629 0029 CMP #9, R00 0600 3
0635 0035 JLE 45 0600 2
0639 0039 ADD #07, R00 0600 1
0645 0045 ADD #48, R00 0600 1
0651 0051 OUT R00, 1 0600 4
0657 0057 HLT 0600 2
0700 0000 IN 0, R00 0700 4
0706 0006 IN 0, R01 0700 4
0712 0012 SUB #48, R00 0700 1
0718 0018 SUB #48, R01 0700 1
0724 0024 MOV #0, R02 0700 0
0730 0030 ADD R00, R02 0700 1
0735 0035 DEC R01 0700 1
0738 0038 JNZ 30 0700 2
0742 0042 CMP #9, R02 0700 3
0748 0048 JLE 58 0700 2
0752 0052 ADD #7, R02 0700 1
0758 0058 ADD #48, R02 0700 1
0764 0064 OUT R02, 1 0700 4
0770 0070 HLT 0700 2
Program Instructions Optimize - Assemble
New Program
Program Name
abc_2
Pages
1
Base Address
700
ADD
Programs
SAVE...
Program List
abc_2
LOAD...
Base Address
-1
COPY TO CLIPBOARD
Cache - Pipeline Execution Unit
Pipeline
Single pipeline
Dual pipeline
Select pipeline
0
SHOW PIPELINE...
Cache
Select cache type
Data
SHOW CACHE...
PROGRAM LIST
Name Base Start Type
tanvi 0500 0000 R
abc_1 0600 0000 R
abc_2 0700 0000 R
LOAD COMPILED CODE IN MEMORY
SHOW PROGRAM DATA MEMORY...
REMOVE PROGRAM
REMOVE ALL PROGRAMS
CREATE PROGRAM INSTANCE
DELETE PROGRAM INSTANCE
Program Control CPU View CPU Help
STEP
by instruction
by single tick
RUN
Fast
Slow
RESET PROGRAM
STOP
SHOW PCB...
SPECIAL CPU REGISTERS
PC 0
SR 0
SP 8096
BR 500
SR Status Flag
OV Z N
CPU Mode
User
Kernel
IR HLT
MAR 770
MDR HLT
PROGRAM STACK (RAM)
Pos Val(D) Addr
Advanced New CPU
COMPILER...
OS 0...
INPUT OUTPUT...
VIRTUAL OS...
INTERRUPTS...
GENERAL PURPOSE CPU REGISTERS
Reg Val(D) C Val(D)
R01 0
R02 0
R03 0
R04 0
R05 0
R06 0
R07 0
R08 0
R09 0
R10 0
R11 0
R12 0
R13 0
R14 0
R15 0
R16 0
R17 0
R18 0
R19 0
R20 0
R21 0
R22 0
R23 0
R24 0
R25 0
R26 0
R27 0
R28 0
R29 0
R30 0
R31 0
Registers Program Stack Watch
Reg Value
CHANGE
RESET ALL
Show Reg Access Status
Select Register Set Size
32
Type here to search
33°C Sunny
12:32 PM
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