# Assignment No : 7

**Name: Pankaj Suresh Harer**

**Roll No. :76**

**PRN No. : 202202040002**

**Batch: A4**

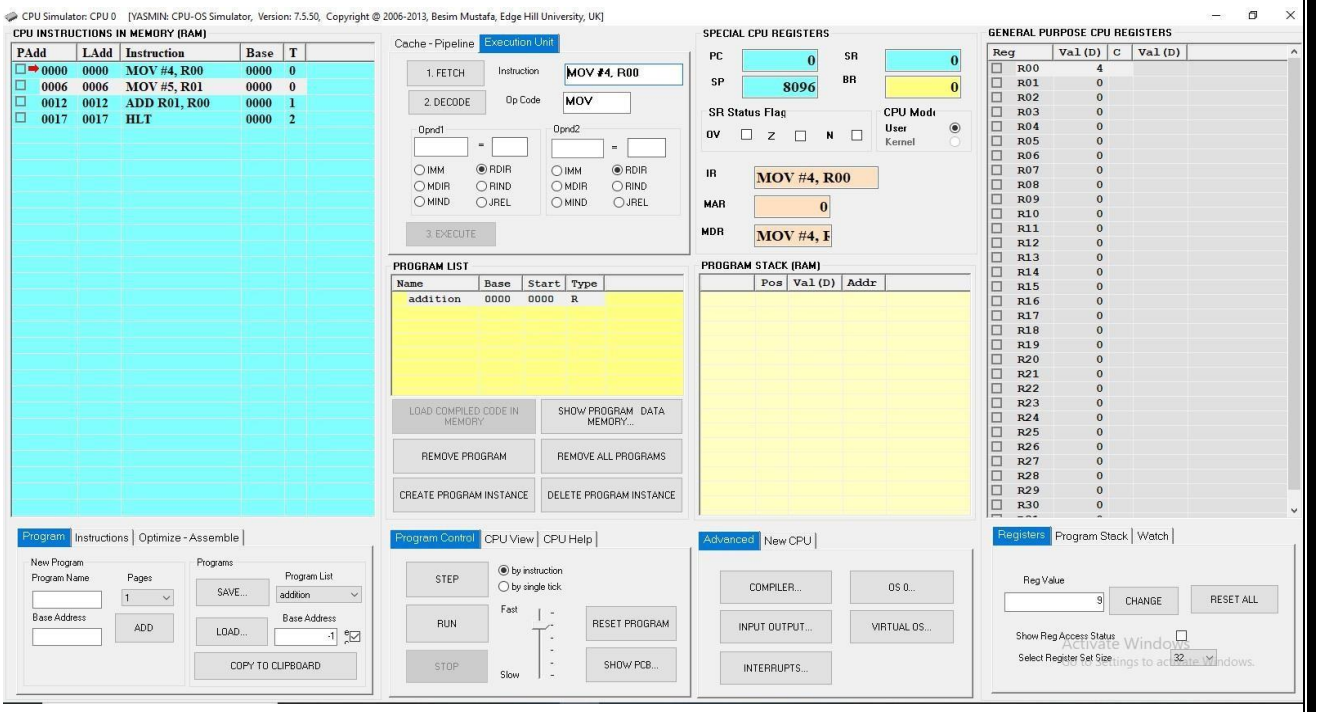
**Problem Statement : Design your ALU using CPU simulator for arithmetic operations.**

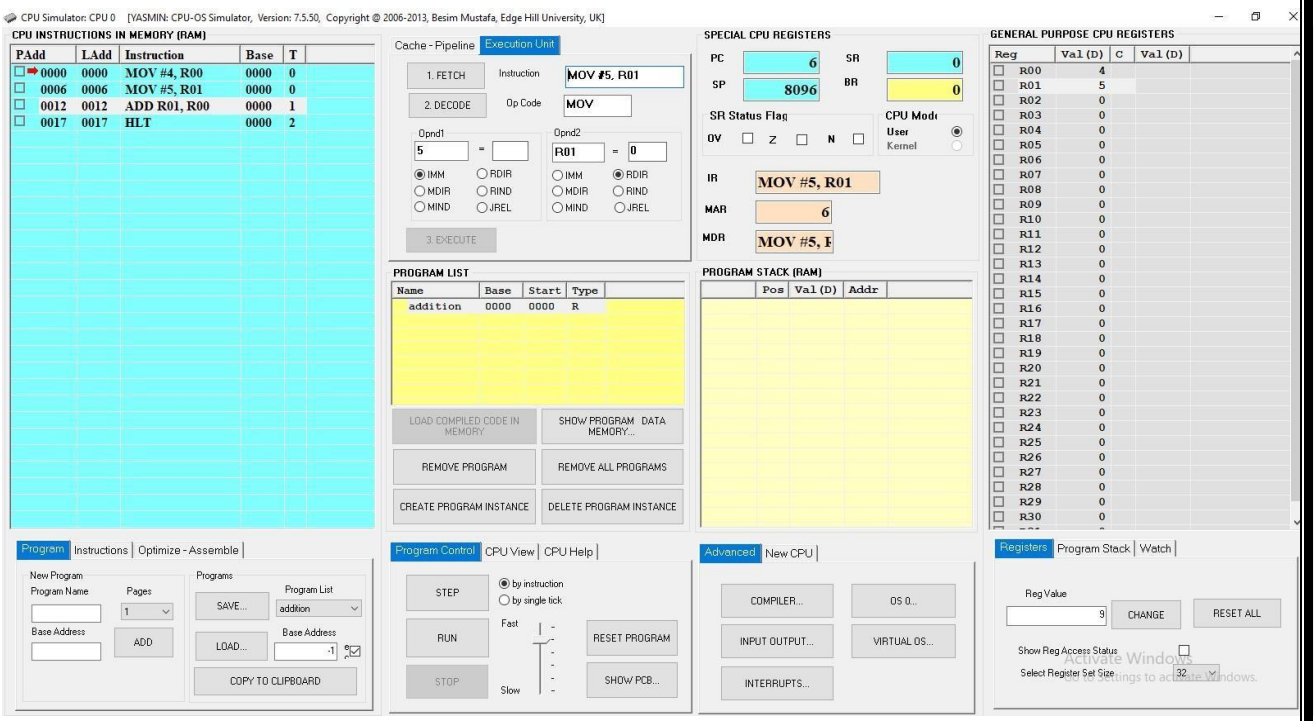
addition.sas_4e570e05be64f02f93

File Edit View

```
1,4,#FALSE#,#FALSE#,"addition",0,500,0,18,1,6,-1217933896
0,0,0,0,0,0
0
0
0
0,0,"MOV #4, R00",0,0,0,0,#FALSE#
6,0,"MOV #5, R01",0,0,0,0,#FALSE#
12,1,"ADD R01, R00",0,0,0,0,#FALSE#
17,2,"HLT",0,0,0,0,#FALSE#
0
0
0
-1
```

## OUTPUT :


CPU Simulator: CPU 0 [YASMIN: CPU-OS Simulator, Version: 7.5.50, Copyright @ 2006-2013, Besim Mustafa, Edge Hill University, UK]
CPU INSTRUCTIONS IN MEMORY (RAM)
PAdd LAdd Instruction Base T
0000 0000 MOV #4, R00 0000 0
0006 0006 MOV #5, R01 0000 0
0012 0012 ADD R01, R00 0000 1
0017 0017 HLT 0000 2
Cache - Pipeline
Execution Unit
1. FETCH
Instruction
MOV #4, R00
2. DECODE
Op Code
MOV
Opnd1
Opnd2
IMM RDIR MDIR RIND MIND JREL
3. EXECUTE
SPECIAL CPU REGISTERS
PC 0
SR 0
SP 8096
BR 0
SR Status Flag
OV Z N
CPU Mode
User
Kernel
IR MOV #4, R00
MAR 0
MDR MOV #4, R
GENERAL PURPOSE CPU REGISTERS
Reg Val (D) C Val (D)
R00 4
R01 0
R02 0
R03 0
R04 0
R05 0
R06 0
R07 0
R08 0
R09 0
R10 0
R11 0
R12 0
R13 0
R14 0
R15 0
R16 0
R17 0
R18 0
R19 0
R20 0
R21 0
R22 0
R23 0
R24 0
R25 0
R26 0
R27 0
R28 0
R29 0
R30 0
PROGRAM LIST
Name Base Start Type
addition 0000 0000 R
LOAD COMPILED CODE IN MEMORY
SHOW PROGRAM DATA MEMORY...
REMOVE PROGRAM
REMOVE ALL PROGRAMS
CREATE PROGRAM INSTANCE
DELETE PROGRAM INSTANCE
PROGRAM STACK (RAM)
Pos Val (D) Addr
Program
Instructions
Optimize - Assemble
New Program
Program Name
Pages
Base Address
ADD
Programs
SAVE...
Program List
addition
LOAD...
Base Address
-1
COPY TO CLIPBOARD
Program Control
CPU View
CPU Help
STEP
by instruction
by single tick
RUN
Fast
Slow
STOP
RESET PROGRAM
SHOW PCB...
Advanced
New CPU
COMPILER...
OS 0...
INPUT OUTPUT...
VIRTUAL OS...
INTERRUPTS...
Registers
Program Stack
Watch
Reg Value
9
CHANGE
RESET ALL
Show Reg Access Status
Select Register Set Size
32
Activate Windows
Go to Settings to activate Windows.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PAdd LAdd Instruction Base T
0000 0000 MOV #4, R00 0000 0
0006 0006 MOV #5, R01 0000 0
0012 0012 ADD R01, R00 0000 1
0017 0017 HLT 0000 2
Cache - Pipeline
Execution Unit
1. FETCH
2. DECODE
3. EXECUTE
Instruction
MOV #5, R01
Op Code
MOV
Opnd1
5
Opnd2
R01
0
IMM RDIR MDIR RIND MIND JREL
SPECIAL CPU REGISTERS
PC 6
SR 0
SP 8096
BR 0
SR Status Flag
OV Z N
CPU Mode
User
Kernel
IR MOV #5, R01
MAR 6
MDR MOV #5, R
GENERAL PURPOSE CPU REGISTERS
Reg Val (D) C Val (D)
R00 4
R01 5
R02 0
R03 0
R04 0
R05 0
R06 0
R07 0
R08 0
R09 0
R10 0
R11 0
R12 0
R13 0
R14 0
R15 0
R16 0
R17 0
R18 0
R19 0
R20 0
R21 0
R22 0
R23 0
R24 0
R25 0
R26 0
R27 0
R28 0
R29 0
R30 0
PROGRAM LIST
Name Base Start Type
addition 0000 0000 R
PROGRAM STACK (RAM)
Pos Val (D) Addr
LOAD COMPILED CODE IN MEMORY
SHOW PROGRAM DATA MEMORY...
REMOVE PROGRAM
REMOVE ALL PROGRAMS
CREATE PROGRAM INSTANCE
DELETE PROGRAM INSTANCE
Program
Instructions
Optimize - Assemble
New Program
Program Name
Pages
Base Address
ADD
Programs
Program List
addition
SAVE...
LOAD...
Base Address
COPY TO CLIPBOARD
Program Control
CPU View
CPU Help
STEP
by instruction
by single tick
RUN
STOP
Fast
Slow
RESET PROGRAM
SHOW PCB...
Advanced
New CPU
COMPILER...
OS 0...
INPUT OUTPUT...
VIRTUAL OS...
INTERRUPTS...
Registers
Program Stack
Watch
Reg Value
CHANGE
RESET ALL
Show Reg Access Status
Select Register Set Size
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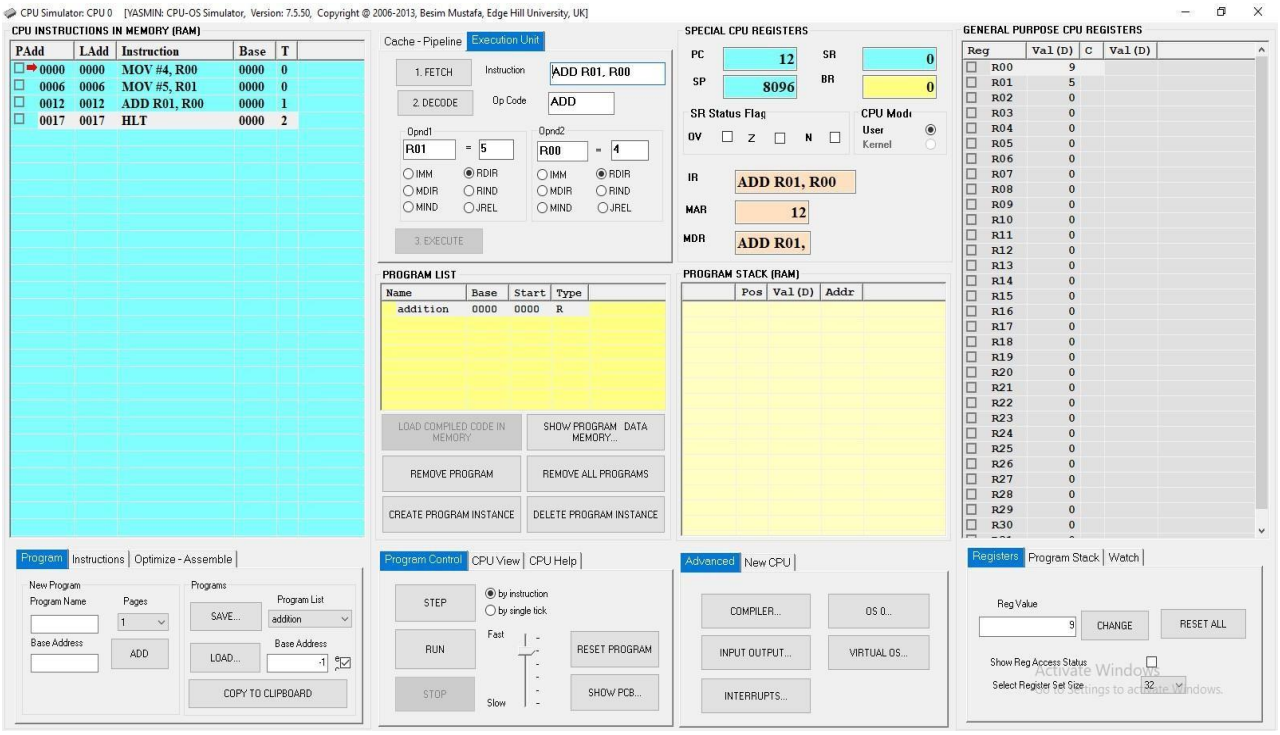
Activate Windows
Go to Settings to activate Windows.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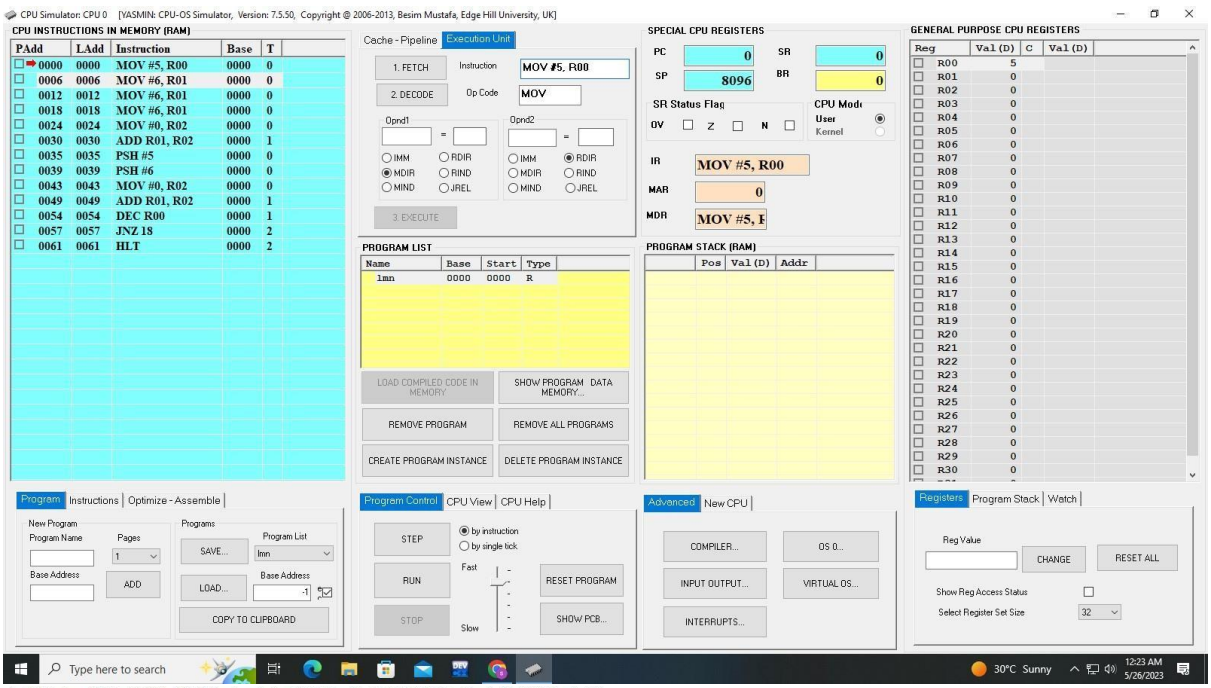
CPU INSTRUCTIONS IN MEMORY (RAM)
PAdd LAdd Instruction Base T
0000 0000 MOV #4, R00 0000 0
0006 0006 MOV #5, R01 0000 0
0012 0012 ADD R01, R00 0000 1
0017 0017 HLT 0000 2
Cache - Pipeline
Execution Unit
1. FETCH
2. DECODE
3. EXECUTE
Instruction
ADD R01, R00
Op Code
ADD
Opnd1
R01
5
Opnd2
R00
4
IMM RDIR MDIR RIND MIND JREL
SPECIAL CPU REGISTERS
PC 12
SR 0
SP 8096
BR 0
SR Status Flag
OV Z N
CPU Mode
User
Kernel
IR ADD R01, R00
MAR 12
MDR ADD R01,
GENERAL PURPOSE CPU REGISTERS
Reg Val (D) C Val (D)
R00 9
R01 5
R02 0
R03 0
R04 0
R05 0
R06 0
R07 0
R08 0
R09 0
R10 0
R11 0
R12 0
R13 0
R14 0
R15 0
R16 0
R17 0
R18 0
R19 0
R20 0
R21 0
R22 0
R23 0
R24 0
R25 0
R26 0
R27 0
R28 0
R29 0
R30 0
PROGRAM LIST
Name Base Start Type
addition 0000 0000 R
PROGRAM STACK (RAM)
Pos Val (D) Addr
LOAD COMPILED CODE IN MEMORY
SHOW PROGRAM DATA MEMORY...
REMOVE PROGRAM
REMOVE ALL PROGRAMS
CREATE PROGRAM INSTANCE
DELETE PROGRAM INSTANCE
Program
Instructions
Optimize - Assemble
New Program
Program Name
Pages
Base Address
ADD
Programs
Program List
addition
SAVE...
LOAD...
Base Address
COPY TO CLIPBOARD
Program Control
CPU View
CPU Help
STEP
by instruction
by single tick
RUN
STOP
Fast
Slow
RESET PROGRAM
SHOW PCB...
Advanced
New CPU
COMPILER...
OS 0...
INPUT OUTPUT...
VIRTUAL OS...
INTERRUPTS...
Registers
Program Stack
Watch
Reg Value
CHANGE
RESET ALL
Show Reg Access Status
Select Register Set Size
32
Activate Windows
Go to Settings to activate Windows.

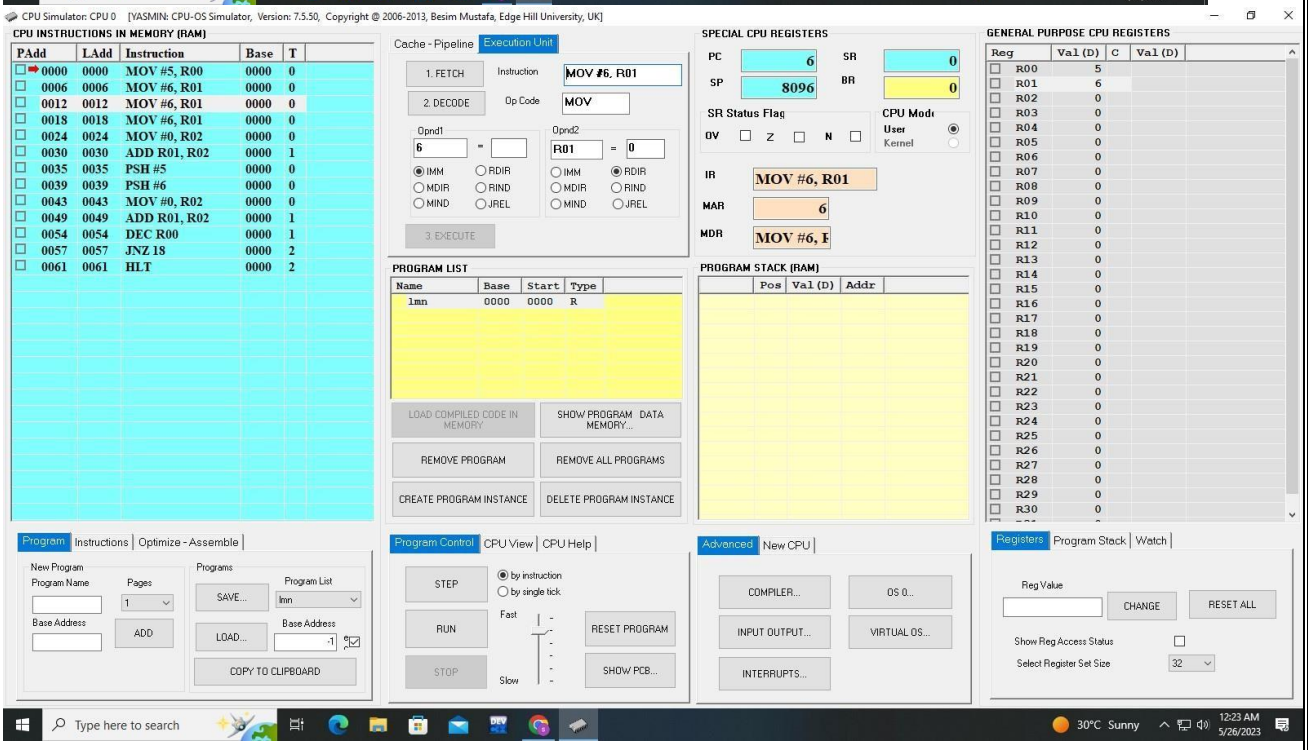
addn.sas_b485586c6ca03d2fc1e16f

File Edit View

```
1,13,#FALSE#,#FALSE#,"lmn",0,700,0,66,1,6,-1959775606
0,0,0,0,0,0
0
0
0
0,0,"MOV #5, R00",0,0,0,0,#FALSE#
6,0,"MOV #6, R01",0,0,0,0,#FALSE#
12,0,"MOV #6, R01",0,0,0,0,#FALSE#
18,0,"MOV #6, R01",0,0,0,0,#FALSE#
24,0,"MOV #0, R02",0,0,0,0,#FALSE#
30,1,"ADD R01, R02",0,0,0,0,#FALSE#
35,0,"MOV #5, SP",0,0,0,0,#FALSE#
41,0,"MOV #6, SP",0,0,0,0,#FALSE#
47,0,"MOV #0, R02",0,0,0,0,#FALSE#
53,1,"ADD R01, R02",0,0,0,0,#FALSE#
58,1,"DEC R00",0,0,0,0,#FALSE#
61,2,"JNZ 18",0,0,0,0,#FALSE#
65,2,"HLT",0,0,0,0,#FALSE#
0
0
0
-1
```

Ln 22, Col 3 100%


CPU Simulator: CPU 0 [YASMIN: CPU-OS Simulator, Version: 7.5.50, Copyright @ 2006-2013, Besim Mustafa, Edge Hill University, UK]
CPU INSTRUCTIONS IN MEMORY (RAM)
PAdd LAdd Instruction Base T
0000 0000 MOV #5, R00 0000 0
0006 0006 MOV #6, R01 0000 0
0012 0012 MOV #6, R01 0000 0
0018 0018 MOV #6, R01 0000 0
0024 0024 MOV #0, R02 0000 0
0030 0030 ADD R01, R02 0000 1
0035 0035 PSH #5 0000 0
0039 0039 PSH #6 0000 0
0043 0043 MOV #0, R02 0000 0
0049 0049 ADD R01, R02 0000 1
0054 0054 DEC R00 0000 1
0057 0057 JNZ 18 0000 2
0061 0061 HLT 0000 2
Cache - Pipeline
Execution Unit
1. FETCH
2. DECODE
3. EXECUTE
Instruction
MOV #5, R00
Op Code
MOV
Opnd1
Opnd2
IMM RDIR MDIR RIND MIND JREL
SPECIAL CPU REGISTERS
PC 0
SP 8096
SR 0
BR 0
SR Status Flag
OV Z N
CPU Mode
User
Kernel
IR MOV #5, R00
MAR 0
MDR MOV #5, R
GENERAL PURPOSE CPU REGISTERS
Reg Val (D) C Val (D)
R00 5
R01 0
R02 0
R03 0
R04 0
R05 0
R06 0
R07 0
R08 0
R09 0
R10 0
R11 0
R12 0
R13 0
R14 0
R15 0
R16 0
R17 0
R18 0
R19 0
R20 0
R21 0
R22 0
R23 0
R24 0
R25 0
R26 0
R27 0
R28 0
R29 0
R30 0
PROGRAM LIST
Name Base Start Type
lmn 0000 0000 R
PROGRAM STACK (RAM)
Pos Val (D) Addr
LOAD COMPILED CODE IN MEMORY
SHOW PROGRAM DATA MEMORY...
REMOVE PROGRAM
REMOVE ALL PROGRAMS
CREATE PROGRAM INSTANCE
DELETE PROGRAM INSTANCE
Program
Instructions
Optimize - Assemble
New Program
Program Name
Pages
Base Address
ADD
Programs
Program List
SAVE...
LOAD...
COPY TO CLIPBOARD
Program Control
CPU View
CPU Help
STEP
RUN
STOP
by instruction
by single tick
Fast
Slow
RESET PROGRAM
SHOW PCB...
Advanced
New CPU
COMPILER...
OS 0...
INPUT OUTPUT...
VIRTUAL OS...
INTERRUPTS...
Registers
Program Stack
Watch
Reg Value
CHANGE
RESET ALL
Show Reg Access Status
Select Register Set Size
32
Type here to search
30°C Sunny
12:23 AM
5/26/2023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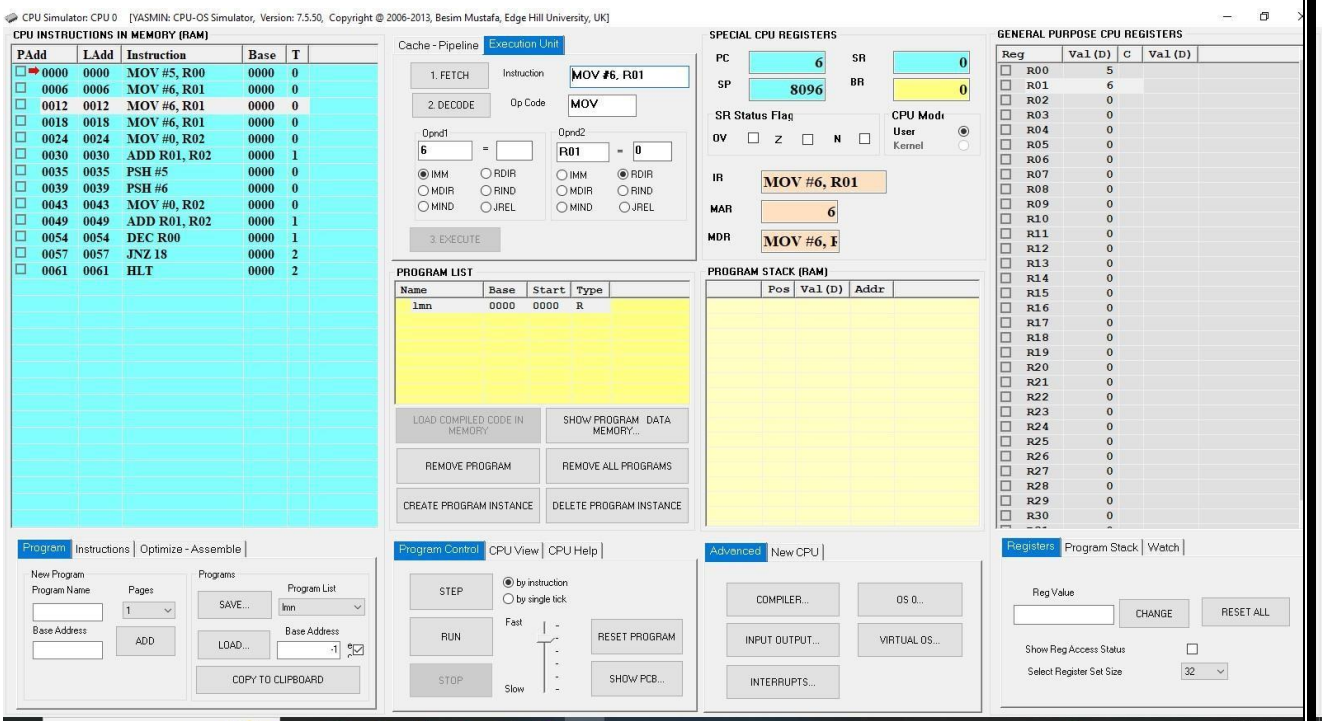
0012 0012 MOV #6, R01 0000 0
0018 0018 MOV #6, R01 0000 0
0024 0024 MOV #0, R02 0000 0
0030 0030 ADD R01, R02 0000 1
0035 0035 PSH #5 0000 0
0039 0039 PSH #6 0000 0
0043 0043 MOV #0, R02 0000 0
0049 0049 ADD R01, R02 0000 1
0054 0054 DEC R00 0000 1
0057 0057 JNZ 18 0000 2
0061 0061 HLT 0000 2
Cache - Pipeline
Execution Unit
1. FETCH
2. DECODE
3. EXECUTE
Instruction
MOV #6, R01
Op Code
MOV
Opnd1
6
Opnd2
R01
0
IMM RDIR MDIR RIND MIND JREL
SPECIAL CPU REGISTERS
PC 6
SP 8096
SR 0
BR 0
SR Status Flag
OV Z N
CPU Mode
User
Kernel
IR MOV #6, R01
MAR 6
MDR MOV #6, R
GENERAL PURPOSE CPU REGISTERS
Reg Val (D) C Val (D)
R00 5
R01 6
R02 0
R03 0
R04 0
R05 0
R06 0
R07 0
R08 0
R09 0
R10 0
R11 0
R12 0
R13 0
R14 0
R15 0
R16 0
R17 0
R18 0
R19 0
R20 0
R21 0
R22 0
R23 0
R24 0
R25 0
R26 0
R27 0
R28 0
R29 0
R30 0
PROGRAM LIST
Name Base Start Type
lmn 0000 0000 R
PROGRAM STACK (RAM)
Pos Val (D) Addr
LOAD COMPILED CODE IN MEMORY
SHOW PROGRAM DATA MEMORY...
REMOVE PROGRAM
REMOVE ALL PROGRAMS
CREATE PROGRAM INSTANCE
DELETE PROGRAM INSTANCE
Program
Instructions
Optimize - Assemble
New Program
Program Name
Pages
Base Address
ADD
Programs
Program List
SAVE...
LOAD...
COPY TO CLIPBOARD
Program Control
CPU View
CPU Help
STEP
RUN
STOP
by instruction
by single tick
Fast
Slow
RESET PROGRAM
SHOW PCB...
Advanced
New CPU
COMPILER...
OS 0...
INPUT OUTPUT...
VIRTUAL OS...
INTERRUPTS...
Registers
Program Stack
Watch
Reg Value
CHANGE
RESET ALL
Show Reg Access Status
Select Register Set Size
32
Type here to search
30°C Sunny
12:23 AM
5/26/2023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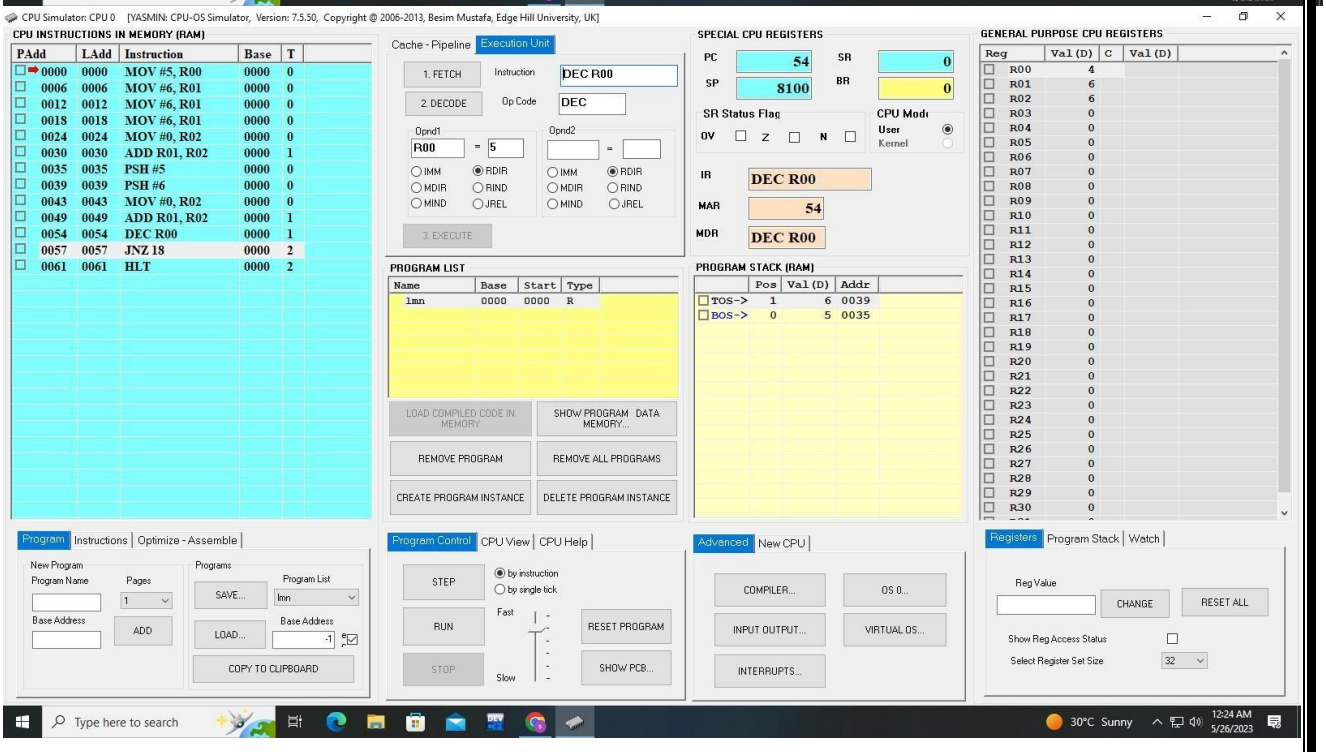
0006 0006 MOV #6, R01 0000 0
0012 0012 MOV #6, R01 0000 0
0018 0018 MOV #6, R01 0000 0
0024 0024 MOV #0, R02 0000 0
0030 0030 ADD R01, R02 0000 1
0035 0035 PSH #5 0000 0
0039 0039 PSH #6 0000 0
0043 0043 MOV #0, R02 0000 0
0049 0049 ADD R01, R02 0000 1
0054 0054 DEC R00 0000 1
0057 0057 JNZ 18 0000 2
0061 0061 HLT 0000 2
Cache - Pipeline
Execution Unit
1. FETCH
Instruction
MOV #6, R01
2. DECODE
Op Code
MOV
Opnd1
6
Opnd2
R01
0
IMM RDIR MDIR RIND MIND JREL
3. EXECUTE
SPECIAL CPU REGISTERS
PC 6
SR 0
SP 8096
BR 0
SR Status Flag
OV Z N
CPU Mode
User
Kernel
IR MOV #6, R01
MAR 6
MDR MOV #6, R
GENERAL PURPOSE CPU REGISTERS
Reg Val (D) C Val (D)
R00 5
R01 6
R02 0
R03 0
R04 0
R05 0
R06 0
R07 0
R08 0
R09 0
R10 0
R11 0
R12 0
R13 0
R14 0
R15 0
R16 0
R17 0
R18 0
R19 0
R20 0
R21 0
R22 0
R23 0
R24 0
R25 0
R26 0
R27 0
R28 0
R29 0
R30 0
PROGRAM LIST
Name Base Start Type
lmn 0000 0000 R
LOAD COMPILED CODE IN MEMORY
SHOW PROGRAM DATA MEMORY...
REMOVE PROGRAM
REMOVE ALL PROGRAMS
CREATE PROGRAM INSTANCE
DELETE PROGRAM INSTANCE
PROGRAM STACK (RAM)
Pos Val (D) Addr
Program Instructions Optimize - Assemble
New Program
Program Name
Pages
Base Address
ADD
Programs
Program List
SAVE...
LOAD...
COPY TO CLIPBOARD
Program Control CPU View CPU Help
STEP
RUN
STOP
by instruction
by single tick
Fast
Slow
RESET PROGRAM
SHOW PCB...
Advanced New CPU
COMPILER...
OS 0...
INPUT OUTPUT...
VIRTUAL OS...
INTERRUPTS...
Registers Program Stack Watch
Reg Value
CHANGE
RESET ALL
Show Reg Access Status
Select Register Set Size
Type here to search
30°C Sunny
12:23 AM
5/26/2023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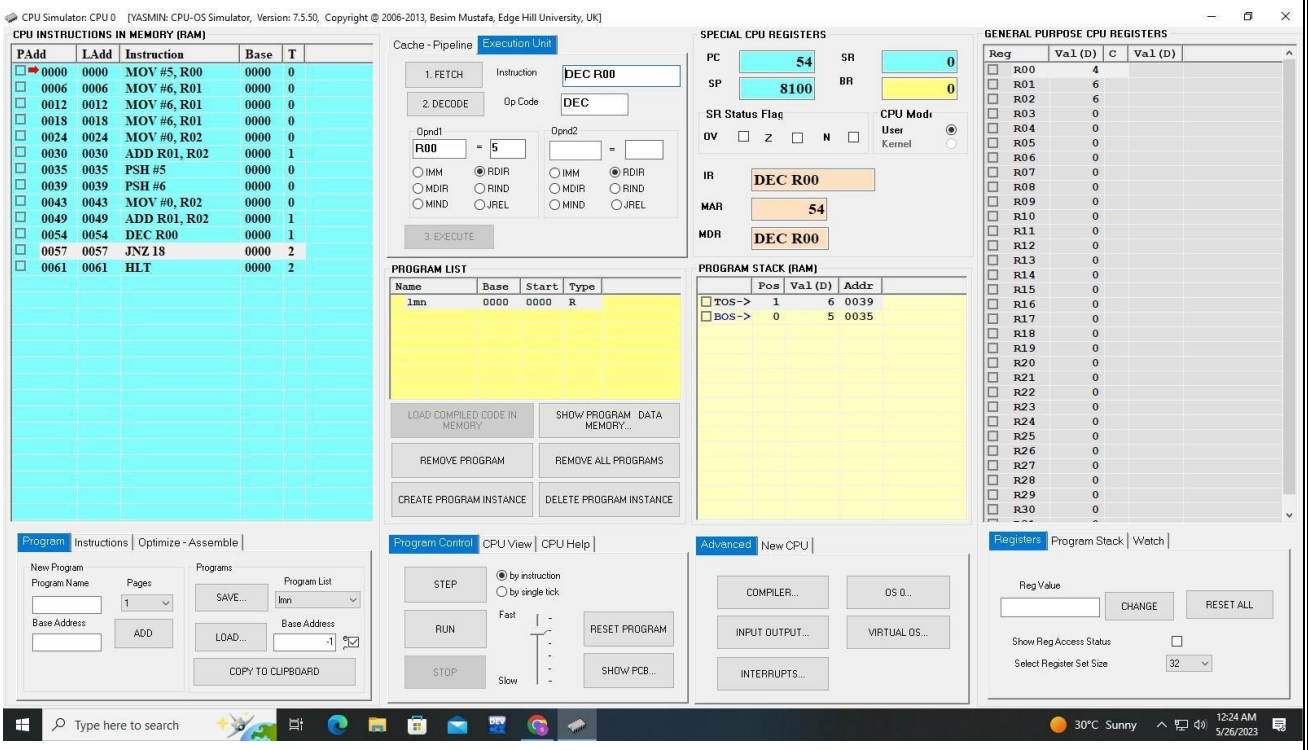
PAdd LAdd Instruction Base T
0000 0000 MOV #5, R00 0000 0
0006 0006 MOV #6, R01 0000 0
0012 0012 MOV #6, R01 0000 0
0018 0018 MOV #6, R01 0000 0
0024 0024 MOV #0, R02 0000 0
0030 0030 ADD R01, R02 0000 1
0035 0035 PSH #5 0000 0
0039 0039 PSH #6 0000 0
0043 0043 MOV #0, R02 0000 0
0049 0049 ADD R01, R02 0000 1
0054 0054 DEC R00 0000 1
0057 0057 JNZ 18 0000 2
0061 0061 HLT 0000 2
Cache - Pipeline
Execution Unit
1. FETCH
Instruction
DEC R00
2. DECODE
Op Code
DEC
Opnd1
R00
5
Opnd2
IMM RDIR MDIR RIND MIND JREL
3. EXECUTE
SPECIAL CPU REGISTERS
PC 54
SR 0
SP 8100
BR 0
SR Status Flag
OV Z N
CPU Mode
User
Kernel
IR DEC R00
MAR 54
MDR DEC R00
GENERAL PURPOSE CPU REGISTERS
Reg Val (D) C Val (D)
R00 4
R01 6
R02 6
R03 0
R04 0
R05 0
R06 0
R07 0
R08 0
R09 0
R10 0
R11 0
R12 0
R13 0
R14 0
R15 0
R16 0
R17 0
R18 0
R19 0
R20 0
R21 0
R22 0
R23 0
R24 0
R25 0
R26 0
R27 0
R28 0
R29 0
R30 0
PROGRAM LIST
Name Base Start Type
lmn 0000 0000 R
LOAD COMPILED CODE IN MEMORY
SHOW PROGRAM DATA MEMORY...
REMOVE PROGRAM
REMOVE ALL PROGRAMS
CREATE PROGRAM INSTANCE
DELETE PROGRAM INSTANCE
PROGRAM STACK (RAM)
Pos Val (D) Addr
TOS-> 1 6 0039
BOS-> 0 5 0035
Program Instructions Optimize - Assemble
New Program
Program Name
Pages
Base Address
ADD
Programs
Program List
SAVE...
LOAD...
COPY TO CLIPBOARD
Program Control CPU View CPU Help
STEP
RUN
STOP
by instruction
by single tick
Fast
Slow
RESET PROGRAM
SHOW PCB...
Advanced New CPU
COMPILER...
OS 0...
INPUT OUTPUT...
VIRTUAL OS...
INTERRUPTS...
Registers Program Stack Watch
Reg Value
CHANGE
RESET ALL
Show Reg Access Status
Select Register Set Size
Type here to search
30°C Sunny
12:24 AM
5/26/2023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PAdd LAdd Instruction Base T
0000 0000 MOV #5, R00 0000 0
0006 0006 MOV #6, R01 0000 0
0012 0012 MOV #6, R01 0000 0
0018 0018 MOV #6, R01 0000 0
0024 0024 MOV #0, R02 0000 0
0030 0030 ADD R01, R02 0000 1
0035 0035 PSH #5 0000 0
0039 0039 PSH #6 0000 0
0043 0043 MOV #0, R02 0000 0
0049 0049 ADD R01, R02 0000 1
0054 0054 DEC R00 0000 1
0057 0057 JNZ 18 0000 2
0061 0061 HLT 0000 2
Cache - Pipeline
Execution Unit
1. FETCH
Instruction
DEC R00
2. DECODE
Op Code
DEC
Opnd1
R00 = 5
Opnd2
IMM RDIR MDIR RIND MIND JREL
3. EXECUTE
SPECIAL CPU REGISTERS
PC 54
SR 0
SP 8100
BR 0
SR Status Flag
OV Z N
CPU Mode
User
Kernel
IR DEC R00
MAR 54
MDR DEC R00
GENERAL PURPOSE CPU REGISTERS
Reg Val (D) C Val (D)
R00 4
R01 6
R02 6
R03 0
R04 0
R05 0
R06 0
R07 0
R08 0
R09 0
R10 0
R11 0
R12 0
R13 0
R14 0
R15 0
R16 0
R17 0
R18 0
R19 0
R20 0
R21 0
R22 0
R23 0
R24 0
R25 0
R26 0
R27 0
R28 0
R29 0
R30 0
PROGRAM LIST
Name Base Start Type
lmn 0000 0000 R
PROGRAM STACK (RAM)
Pos Val (D) Addr
TOS-> 1 6 0039
BOS-> 0 5 0035
LOAD COMPILED CODE IN MEMORY
SHOW PROGRAM DATA MEMORY...
REMOVE PROGRAM
REMOVE ALL PROGRAMS
CREATE PROGRAM INSTANCE
DELETE PROGRAM INSTANCE
Program
Instructions
Optimize - Assemble
New Program
Program Name
Pages
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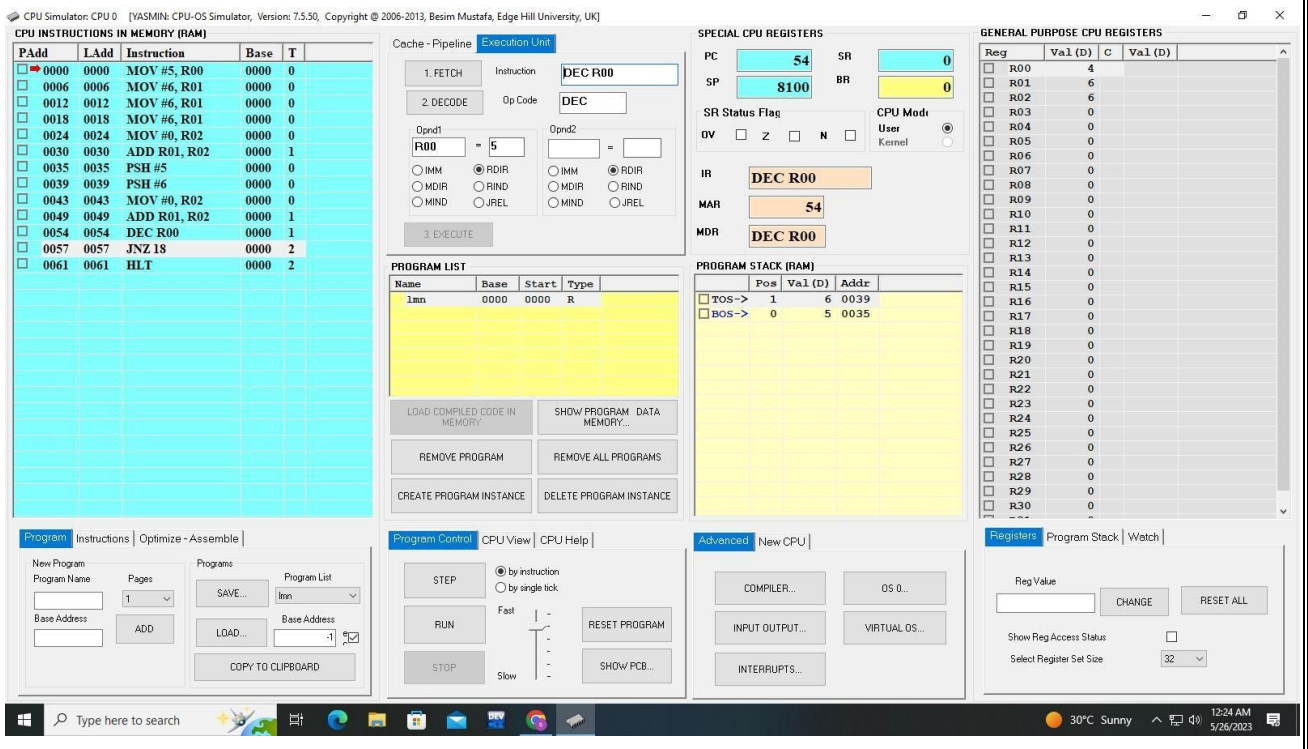
Programs
SAVE...
Program List
lmn
LOAD...
Base Address
COPY TO CLIPBOARD
Program Control
CPU View
CPU Help
STEP
by instruction
by single tick
RUN
Fast
Slow
RESET PROGRAM
STOP
SHOW PCB...
Advanced
New CPU
COMPILER...
OS 0...
INPUT OUTPUT...
VIRTUAL OS...
INTERRUPTS...
Registers
Program Stack
Watch
Reg Value
CHANGE
RESET ALL
Show Reg Access Status
Select Register Set Size
32
Type here to search
30°C Sunny
12:24 AM
5/26/2023


CPU Simulator: CPU 0 [YASMIN: CPU-OS Simulator, Version: 7.5.50, Copyright @ 2006-2013, Besim Mustafa, Edge Hill University, UK]
CPU INSTRUCTIONS IN MEMORY (RAM)
PAdd LAdd Instruction Base T
0000 0000 MOV #5, R00 0000 0
0006 0006 MOV #6, R01 0000 0
0012 0012 MOV #6, R01 0000 0
0018 0018 MOV #6, R01 0000 0
0024 0024 MOV #0, R02 0000 0
0030 0030 ADD R01, R02 0000 1
0035 0035 PSH #5 0000 0
0039 0039 PSH #6 0000 0
0043 0043 MOV #0, R02 0000 0
0049 0049 ADD R01, R02 0000 1
0054 0054 DEC R00 0000 1
0057 0057 JNZ 18 0000 2
0061 0061 HLT 0000 2
Cache - Pipeline
Execution Unit
1. FETCH
Instruction
DEC R00
2. DECODE
Op Code
DEC
Opnd1
R00 = 5
Opnd2
IMM RDIR MDIR RIND MIND JREL
3. EXECUTE
SPECIAL CPU REGISTERS
PC 54
SR 0
SP 8100
BR 0
SR Status Flag
OV Z N
CPU Mode
User
Kernel
IR DEC R00
MAR 54
MDR DEC R00
GENERAL PURPOSE CPU REGISTERS
Reg Val (D) C Val (D)
R00 4
R01 6
R02 6
R03 0
R04 0
R05 0
R06 0
R07 0
R08 0
R09 0
R10 0
R11 0
R12 0
R13 0
R14 0
R15 0
R16 0
R17 0
R18 0
R19 0
R20 0
R21 0
R22 0
R23 0
R24 0
R25 0
R26 0
R27 0
R28 0
R29 0
R30 0
PROGRAM LIST
Name Base Start Type
lmn 0000 0000 R
PROGRAM STACK (RAM)
Pos Val (D) Addr
TOS-> 1 6 0039
BOS-> 0 5 0035
LOAD COMPILED CODE IN MEMORY
SHOW PROGRAM DATA MEMORY...
REMOVE PROGRAM
REMOVE ALL PROGRAMS
CREATE PROGRAM INSTANCE
DELETE PROGRAM INSTANCE
Program
Instructions
Optimize - Assemble
New Program
Program Name
Pages
Base Address
ADD
Programs
SAVE...
Program List
lmn
LOAD...
Base Address
COPY TO CLIPBOARD
Program Control
CPU View
CPU Help
STEP
by instruction
by single tick
RUN
Fast
Slow
RESET PROGRAM
STOP
SHOW PCB...
Advanced
New CPU
COMPILER...
OS 0...
INPUT OUTPUT...
VIRTUAL OS...
INTERRUPTS...
Registers
Program Stack
Watch
Reg Value
CHANGE
RESET ALL
Show Reg Access Status
Select Register Set Size
32
Type here to search
30°C Sunny
12:24 AM
5/26/2023