# Assignment No : 7

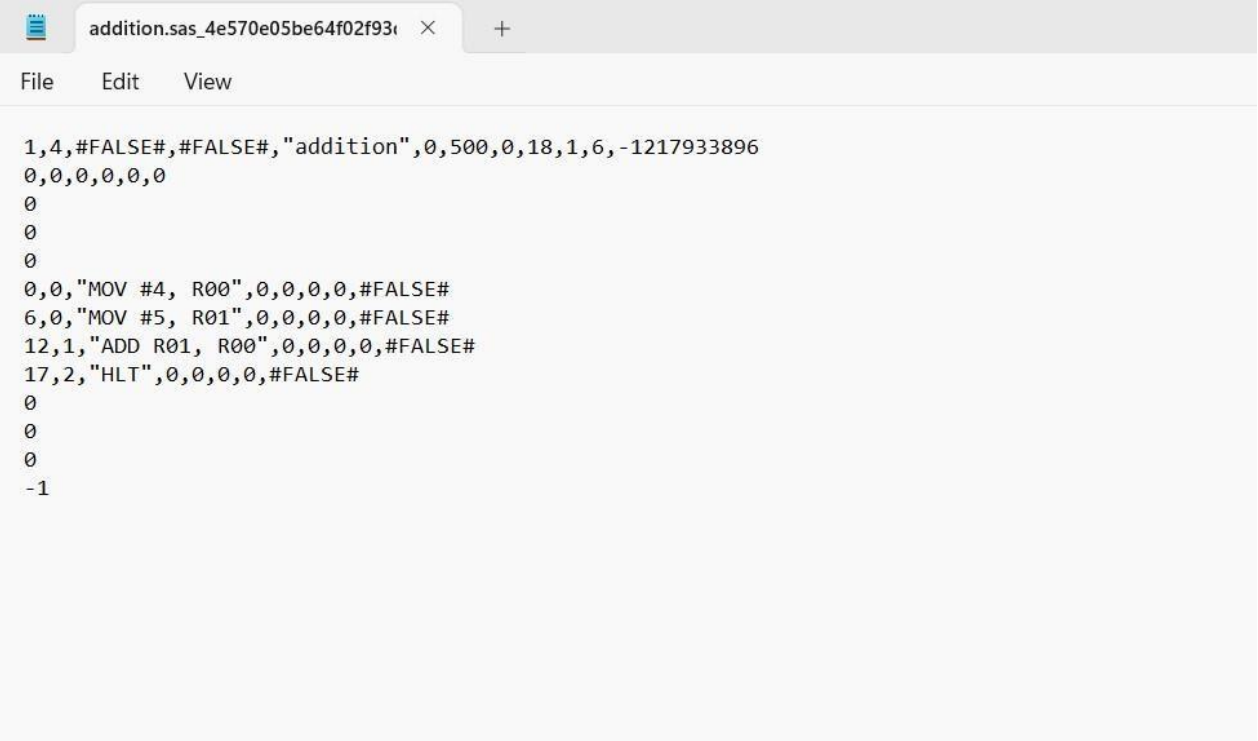
**Name: Pankaj Suresh Harer**

**Roll No. :76**

**PRN No. : 202202040002**

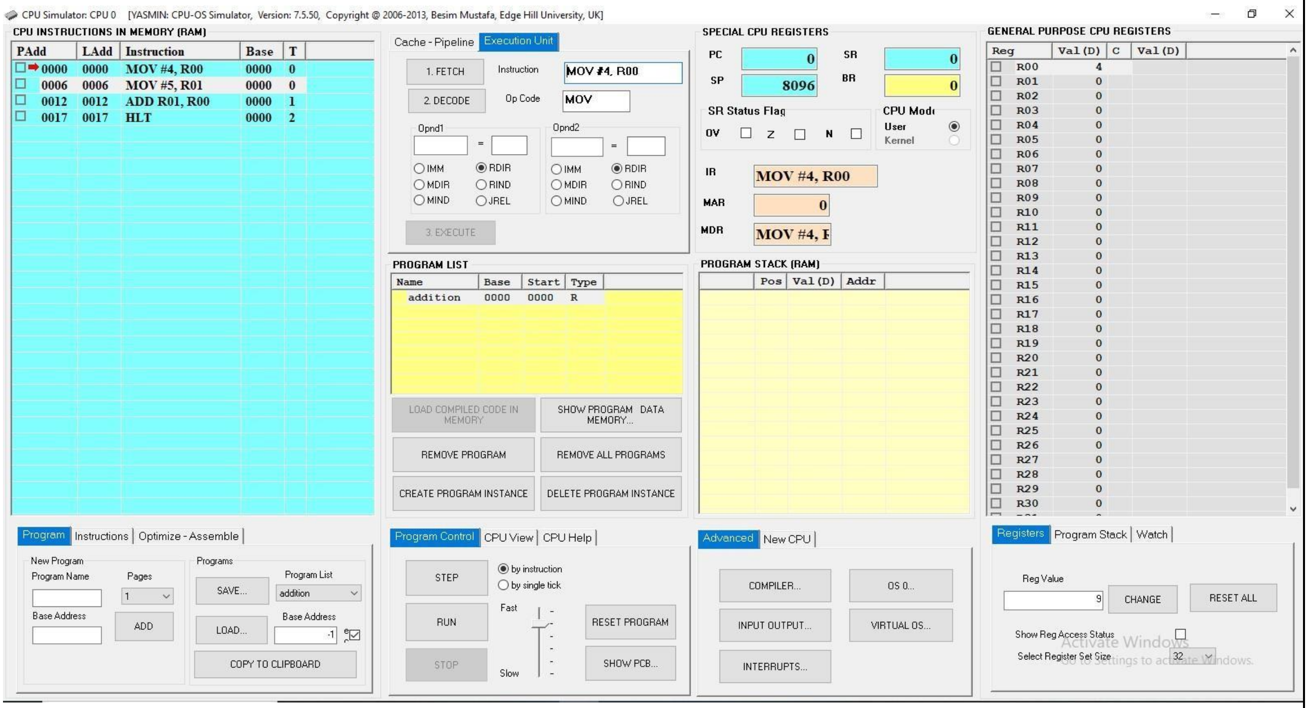
**Batch: A4**

**Problem Statement : Design your ALU using CPU simulator for arithmetic operations.**



```
1,4,#FALSE#,#FALSE#,"addition",0,500,0,18,1,6,-1217933896
0,0,0,0,0,0
0
0
0
0,0,"MOV #4, R00",0,0,0,0,#FALSE#
6,0,"MOV #5, R01",0,0,0,0,#FALSE#
12,1,"ADD R01, R00",0,0,0,0,#FALSE#
17,2,"HLT",0,0,0,0,#FALSE#
0
0
0
-1
```

# OUTPUT :



CPU Simulator: CPU 0 [YASMIN: CPU-OS Simulator, Version: 7.5.50, Copyright @ 2006-2013, Besim Mustafa, Edge Hill University, UK]

CPU INSTRUCTIONS IN MEMORY (RAM)

| PAdd | LAdd | Instruction | Base | T |
|---|---|---|---|---|
| □ ➡ 0000 | 0000 | MOV #4, R00 | 0000 | 0 |
| □ 0006 | 0006 | MOV #5, R01 | 0000 | 0 |
| □ 0012 | 0012 | ADD R01, R00 | 0000 | 1 |
| □ 0017 | 0017 | HLT | 0000 | 2 |

Instruction: MOV #4, R00

Op Code: MOV

Opnd1: ○ IMM ● RDIR ○ MDIR ○ RIND ○ MIND ○ JREL

Opnd2: ○ IMM ● RDIR ○ MDIR ○ RIND ○ MIND ○ JREL

SPECIAL CPU REGISTERS

PC: 0 SR: 0

SP: 8096 BR: 0

SR Status Flag: OV □ Z □ N □

CPU Mode: User ● Kernel ○

IR: MOV #4, R00

MAR: 0

MDR: MOV #4, F

PROGRAM LIST

| Name | Base | Start | Type |
|---|---|---|---|
| addition | 0000 | 0000 | R |

PROGRAM STACK (RAM)

| | Pos | Val (D) | Addr |
|---|---|---|---|

GENERAL PURPOSE CPU REGISTERS

| Reg | Val (D) | C | Val (D) |
|---|---|---|---|
| □ R00 | 4 | | |
| □ R01 | 0 | | |
| □ R02 | 0 | | |
| □ R03 | 0 | | |
| □ R04 | 0 | | |
| □ R05 | 0 | | |
| □ R06 | 0 | | |
| □ R07 | 0 | | |
| □ R08 | 0 | | |
| □ R09 | 0 | | |
| □ R10 | 0 | | |
| □ R11 | 0 | | |
| □ R12 | 0 | | |
| □ R13 | 0 | | |
| □ R14 | 0 | | |
| □ R15 | 0 | | |
| □ R16 | 0 | | |
| □ R17 | 0 | | |
| □ R18 | 0 | | |
| □ R19 | 0 | | |
| □ R20 | 0 | | |
| □ R21 | 0 | | |
| □ R22 | 0 | | |
| □ R23 | 0 | | |
| □ R24 | 0 | | |
| □ R25 | 0 | | |
| □ R26 | 0 | | |
| □ R27 | 0 | | |
| □ R28 | 0 | | |
| □ R29 | 0 | | |
| □ R30 | 0 | | |

New Program: Program Name: Pages: 1 Base Address:

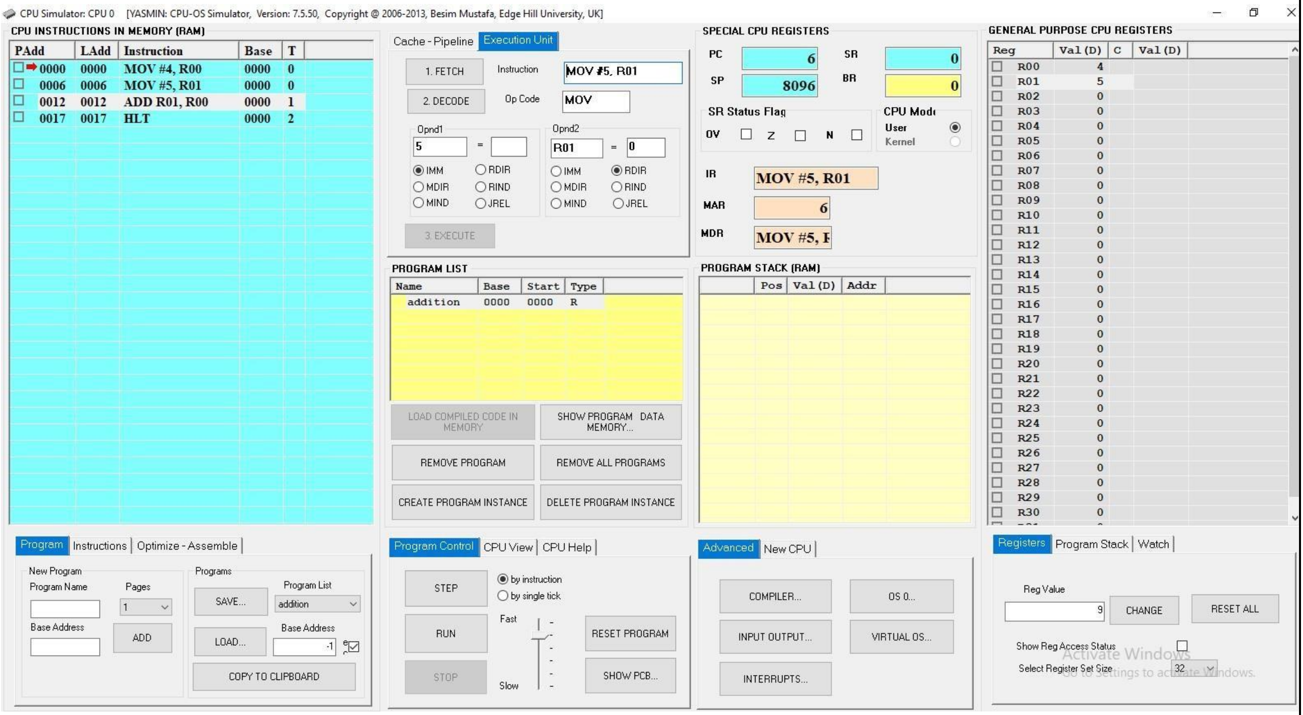
Programs: Program List: addition Base Address: -1 ☑

● by instruction ○ by single tick

Reg Value: 9

Show Reg Access Status □

Select Register Set Size: 32



CPU Simulator: CPU 0 [YASMIN: CPU-OS Simulator, Version: 7.5.50, Copyright @ 2006-2013, Besim Mustafa, Edge Hill University, UK]

CPU INSTRUCTIONS IN MEMORY (RAM)

| PAdd | LAdd | Instruction | Base | T |
|---|---|---|---|---|
| □ 0000 | 0000 | MOV #4, R00 | 0000 | 0 |
| □ 0006 | 0006 | MOV #5, R01 | 0000 | 0 |
| □ 0012 | 0012 | ADD R01, R00 | 0000 | 1 |
| □ 0017 | 0017 | HLT | 0000 | 2 |

Cache - Pipeline | Execution Unit

1. FETCH — Instruction: MOV #5, R01
2. DECODE — Op Code: MOV

Opnd1: 5 = ; ● IMM ○ RDIR ○ MDIR ○ RIND ○ MIND ○ JREL

Opnd2: R01 = 0; ○ IMM ● RDIR ○ MDIR ○ RIND ○ MIND ○ JREL

3. EXECUTE

SPECIAL CPU REGISTERS

PC 6 SR 0
SP 8096 BR 0

SR Status Flag: OV □ Z □ N □

CPU Mode: User ● Kernel ○

IR: MOV #5, R01
MAR: 6
MDR: MOV #5, I

PROGRAM LIST

| Name | Base | Start | Type |
|---|---|---|---|
| addition | 0000 | 0000 | R |

PROGRAM STACK (RAM)

| Pos | Val (D) | Addr |
|---|---|---|

GENERAL PURPOSE CPU REGISTERS

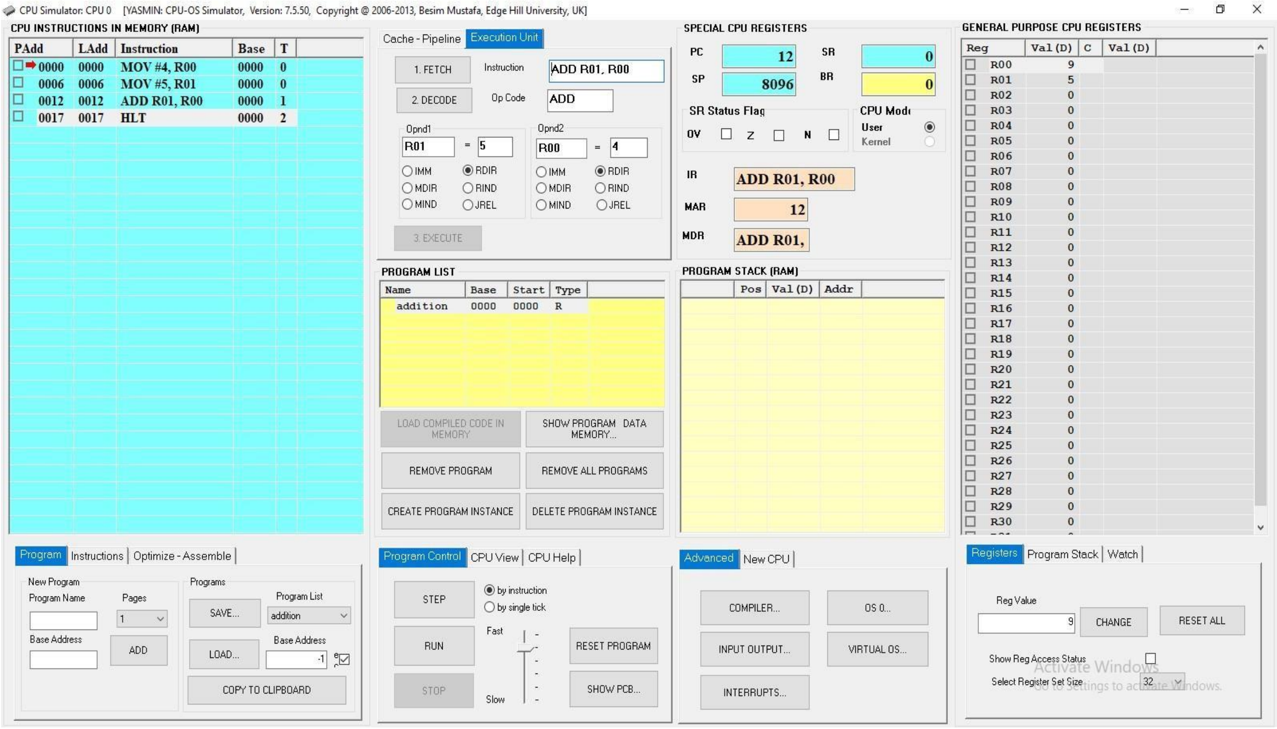
| Reg | Val (D) | C | Val (D) |
|---|---|---|---|
| □ R00 | 4 | | |
| □ R01 | 5 | | |
| □ R02 | 0 | | |
| □ R03 | 0 | | |
| □ R04 | 0 | | |
| □ R05 | 0 | | |
| □ R06 | 0 | | |
| □ R07 | 0 | | |
| □ R08 | 0 | | |
| □ R09 | 0 | | |
| □ R10 | 0 | | |
| □ R11 | 0 | | |
| □ R12 | 0 | | |
| □ R13 | 0 | | |
| □ R14 | 0 | | |
| □ R15 | 0 | | |
| □ R16 | 0 | | |
| □ R17 | 0 | | |
| □ R18 | 0 | | |
| □ R19 | 0 | | |
| □ R20 | 0 | | |
| □ R21 | 0 | | |
| □ R22 | 0 | | |
| □ R23 | 0 | | |
| □ R24 | 0 | | |
| □ R25 | 0 | | |
| □ R26 | 0 | | |
| □ R27 | 0 | | |
| □ R28 | 0 | | |
| □ R29 | 0 | | |
| □ R30 | 0 | | |

Program List: addition; Pages: 1; Base Address: -1

Program Control: ● by instruction ○ by single tick

Reg Value: 9

Select Register Set Size: 32



CPU Simulator: CPU 0 [YASMIN: CPU-OS Simulator, Version: 7.5.50, Copyright @ 2006-2013, Besim Mustafa, Edge Hill University, UK]

CPU INSTRUCTIONS IN MEMORY (RAM)

| PAdd | LAdd | Instruction | Base | T |
|---|---|---|---|---|
| □ 0000 | 0000 | MOV #4, R00 | 0000 | 0 |
| □ 0006 | 0006 | MOV #5, R01 | 0000 | 0 |
| □ 0012 | 0012 | ADD R01, R00 | 0000 | 1 |
| □ 0017 | 0017 | HLT | 0000 | 2 |

Cache - Pipeline | Execution Unit

1. FETCH — Instruction: ADD R01, R00
2. DECODE — Op Code: ADD

Opnd1: R01 = 5; ○ IMM ● RDIR ○ MDIR ○ RIND ○ MIND ○ JREL

Opnd2: R00 = 4; ○ IMM ● RDIR ○ MDIR ○ RIND ○ MIND ○ JREL

3. EXECUTE

SPECIAL CPU REGISTERS

PC 12 SR 0
SP 8096 BR 0

SR Status Flag: OV □ Z □ N □

CPU Mode: User ● Kernel ○

IR: ADD R01, R00
MAR: 12
MDR: ADD R01,

PROGRAM LIST

| Name | Base | Start | Type |
|---|---|---|---|
| addition | 0000 | 0000 | R |

PROGRAM STACK (RAM)

| Pos | Val (D) | Addr |
|---|---|---|

GENERAL PURPOSE CPU REGISTERS

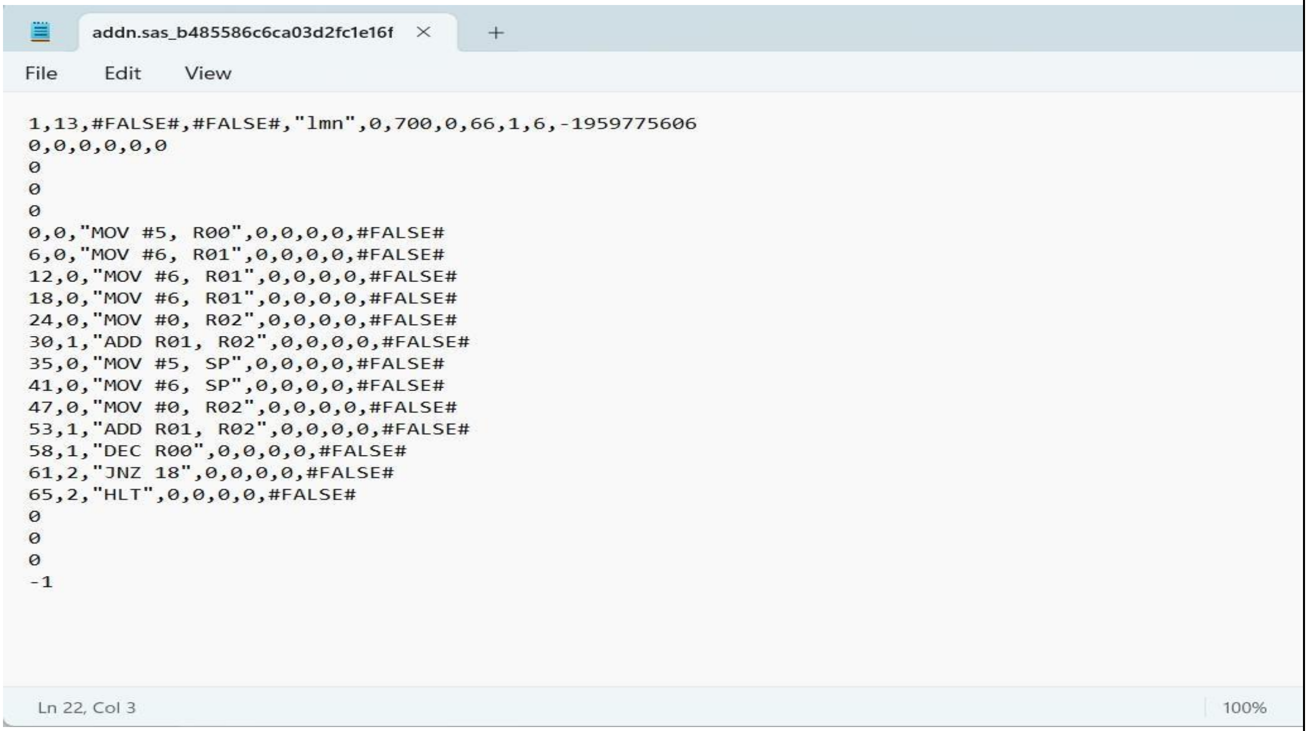
| Reg | Val (D) | C | Val (D) |
|---|---|---|---|
| □ R00 | 9 | | |
| □ R01 | 5 | | |
| □ R02 | 0 | | |
| □ R03 | 0 | | |
| □ R04 | 0 | | |
| □ R05 | 0 | | |
| □ R06 | 0 | | |
| □ R07 | 0 | | |
| □ R08 | 0 | | |
| □ R09 | 0 | | |
| □ R10 | 0 | | |
| □ R11 | 0 | | |
| □ R12 | 0 | | |
| □ R13 | 0 | | |
| □ R14 | 0 | | |
| □ R15 | 0 | | |
| □ R16 | 0 | | |
| □ R17 | 0 | | |
| □ R18 | 0 | | |
| □ R19 | 0 | | |
| □ R20 | 0 | | |
| □ R21 | 0 | | |
| □ R22 | 0 | | |
| □ R23 | 0 | | |
| □ R24 | 0 | | |
| □ R25 | 0 | | |
| □ R26 | 0 | | |
| □ R27 | 0 | | |
| □ R28 | 0 | | |
| □ R29 | 0 | | |
| □ R30 | 0 | | |

Program List: addition; Pages: 1; Base Address: -1

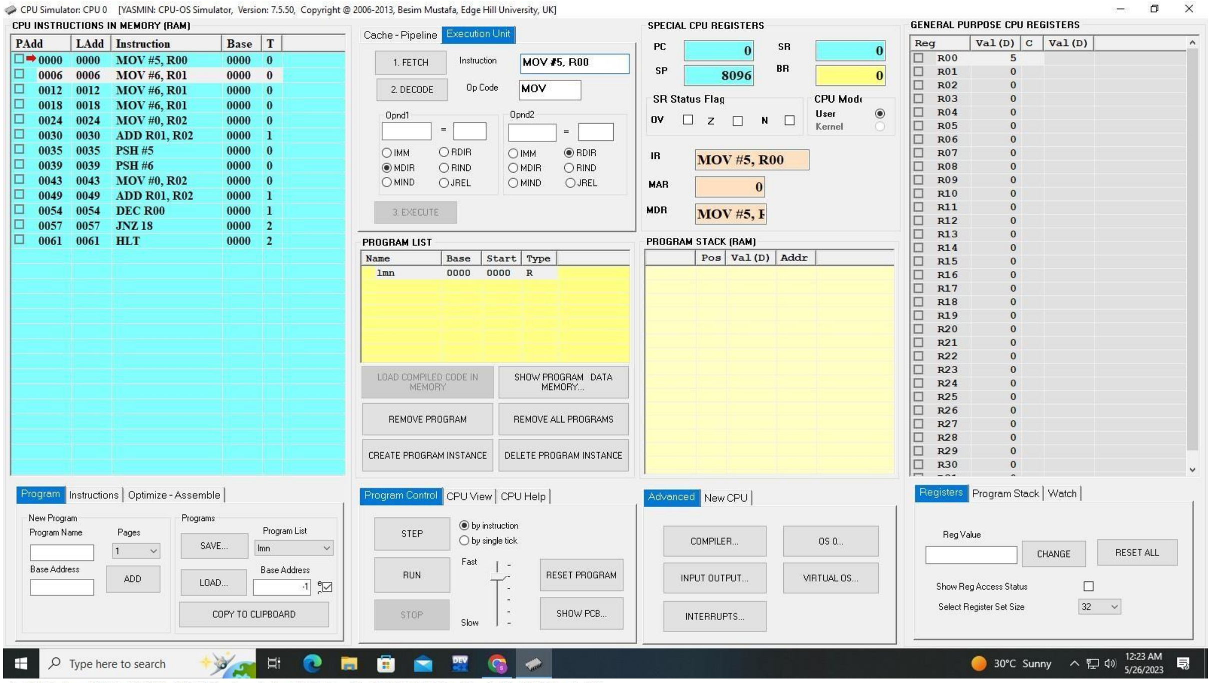
Program Control: ● by instruction ○ by single tick

Reg Value: 9

Select Register Set Size: 32



```
1,13,#FALSE#,#FALSE#,"lmn",0,700,0,66,1,6,-1959775606
0,0,0,0,0,0
0
0
0
0,0,"MOV #5, R00",0,0,0,0,#FALSE#
6,0,"MOV #6, R01",0,0,0,0,#FALSE#
12,0,"MOV #6, R01",0,0,0,0,#FALSE#
18,0,"MOV #6, R01",0,0,0,0,#FALSE#
24,0,"MOV #0, R02",0,0,0,0,#FALSE#
30,1,"ADD R01, R02",0,0,0,0,#FALSE#
35,0,"MOV #5, SP",0,0,0,0,#FALSE#
41,0,"MOV #6, SP",0,0,0,0,#FALSE#
47,0,"MOV #0, R02",0,0,0,0,#FALSE#
53,1,"ADD R01, R02",0,0,0,0,#FALSE#
58,1,"DEC R00",0,0,0,0,#FALSE#
61,2,"JNZ 18",0,0,0,0,#FALSE#
65,2,"HLT",0,0,0,0,#FALSE#
0
0
0
-1
```



CPU Simulator: CPU 0 [YASMIN: CPU-OS Simulator, Version: 7.5.50, Copyright @ 2006-2013, Besim Mustafa, Edge Hill University, UK]

CPU INSTRUCTIONS IN MEMORY (RAM)

| PAdd | LAdd | Instruction | Base | T |
|---|---|---|---|---|
| □ ➡ 0000 | 0000 | MOV #5, R00 | 0000 | 0 |
| □ 0006 | 0006 | MOV #6, R01 | 0000 | 0 |
| □ 0012 | 0012 | MOV #6, R01 | 0000 | 0 |
| □ 0018 | 0018 | MOV #6, R01 | 0000 | 0 |
| □ 0024 | 0024 | MOV #0, R02 | 0000 | 0 |
| □ 0030 | 0030 | ADD R01, R02 | 0000 | 1 |
| □ 0035 | 0035 | PSH #5 | 0000 | 0 |
| □ 0039 | 0039 | PSH #6 | 0000 | 0 |
| □ 0043 | 0043 | MOV #0, R02 | 0000 | 0 |
| □ 0049 | 0049 | ADD R01, R02 | 0000 | 1 |
| □ 0054 | 0054 | DEC R00 | 0000 | 1 |
| □ 0057 | 0057 | JNZ 18 | 0000 | 2 |
| □ 0061 | 0061 | HLT | 0000 | 2 |

Execution Unit

Instruction: MOV #5, R00

Op Code: MOV

Opnd1: ○ IMM ○ RDIR ● MDIR ○ RIND ○ MIND ○ JREL

Opnd2: ○ IMM ● RDIR ○ MDIR ○ RIND ○ MIND ○ JREL

PROGRAM LIST

| Name | Base | Start | Type |
|---|---|---|---|
| lmn | 0000 | 0000 | R |

SPECIAL CPU REGISTERS

PC: 0 SR: 0

SP: 8096 BR: 0

SR Status Flag: OV □ Z □ N □

CPU Mode: User ● Kernel ○

IR: MOV #5, R00

MAR: 0

MDR: MOV #5, I

PROGRAM STACK (RAM)

| | Pos | Val (D) | Addr |
|---|---|---|---|

GENERAL PURPOSE CPU REGISTERS

| Reg | Val (D) | C | Val (D) |
|---|---|---|---|
| □ R00 | 5 | | |
| □ R01 | 0 | | |
| □ R02 | 0 | | |
| □ R03 | 0 | | |
| □ R04 | 0 | | |
| □ R05 | 0 | | |
| □ R06 | 0 | | |
| □ R07 | 0 | | |
| □ R08 | 0 | | |
| □ R09 | 0 | | |
| □ R10 | 0 | | |
| □ R11 | 0 | | |
| □ R12 | 0 | | |
| □ R13 | 0 | | |
| □ R14 | 0 | | |
| □ R15 | 0 | | |
| □ R16 | 0 | | |
| □ R17 | 0 | | |
| □ R18 | 0 | | |
| □ R19 | 0 | | |
| □ R20 | 0 | | |
| □ R21 | 0 | | |
| □ R22 | 0 | | |
| □ R23 | 0 | | |
| □ R24 | 0 | | |
| □ R25 | 0 | | |
| □ R26 | 0 | | |
| □ R27 | 0 | | |
| □ R28 | 0 | | |
| □ R29 | 0 | | |
| □ R30 | 0 | | |

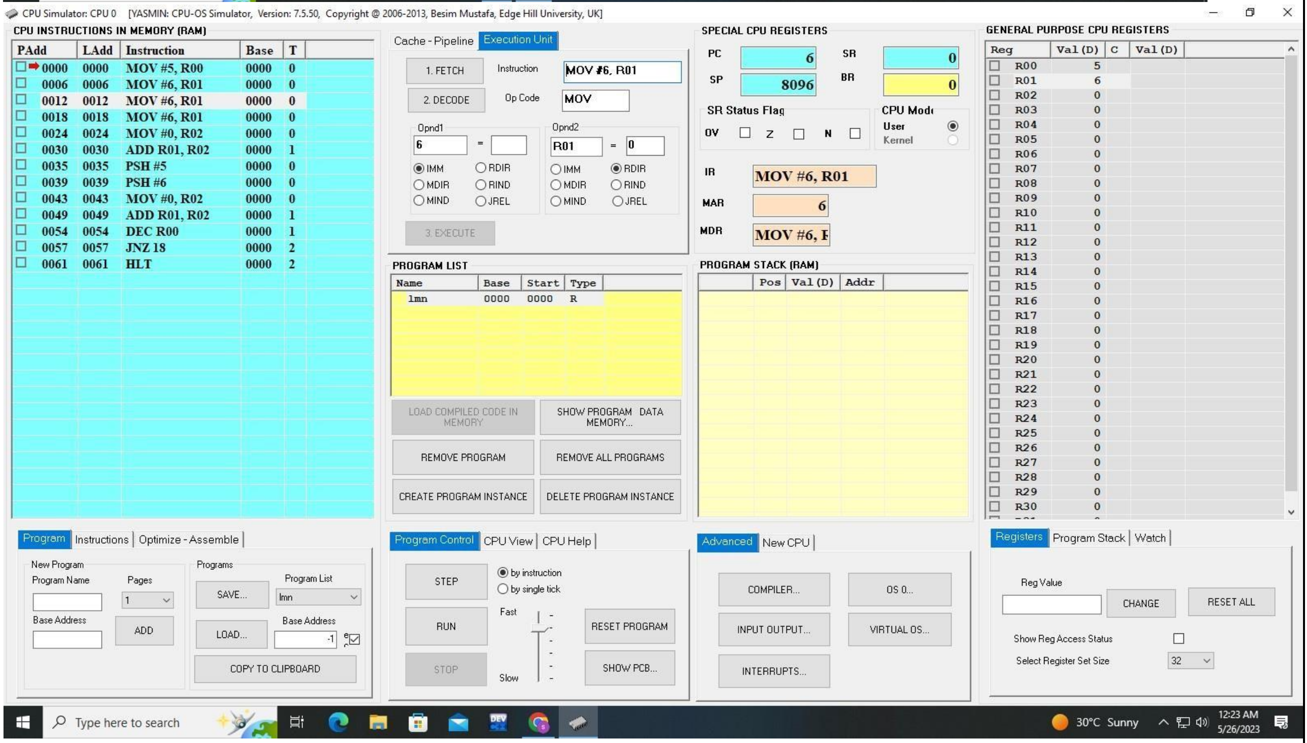
Program List: lmn

Base Address: -1

● by instruction ○ by single tick

Show Reg Access Status □

Select Register Set Size: 32



CPU Simulator: CPU 0 [YASMIN: CPU-OS Simulator, Version: 7.5.50, Copyright @ 2006-2013, Besim Mustafa, Edge Hill University, UK]

CPU INSTRUCTIONS IN MEMORY (RAM)

| PAdd | LAdd | Instruction | Base | T |
|---|---|---|---|---|
| □ ➡ 0000 | 0000 | MOV #5, R00 | 0000 | 0 |
| □ 0006 | 0006 | MOV #6, R01 | 0000 | 0 |
| □ 0012 | 0012 | MOV #6, R01 | 0000 | 0 |
| □ 0018 | 0018 | MOV #6, R01 | 0000 | 0 |
| □ 0024 | 0024 | MOV #0, R02 | 0000 | 0 |
| □ 0030 | 0030 | ADD R01, R02 | 0000 | 1 |
| □ 0035 | 0035 | PSH #5 | 0000 | 0 |
| □ 0039 | 0039 | PSH #6 | 0000 | 0 |
| □ 0043 | 0043 | MOV #0, R02 | 0000 | 0 |
| □ 0049 | 0049 | ADD R01, R02 | 0000 | 1 |
| □ 0054 | 0054 | DEC R00 | 0000 | 1 |
| □ 0057 | 0057 | JNZ 18 | 0000 | 2 |
| □ 0061 | 0061 | HLT | 0000 | 2 |

Execution Unit

Instruction: MOV #6, R01

Op Code: MOV

Opnd1: 6 =

● IMM ○ RDIR ○ MDIR ○ RIND ○ MIND ○ JREL

Opnd2: R01 = 0

○ IMM ● RDIR ○ MDIR ○ RIND ○ MIND ○ JREL

PROGRAM LIST

| Name | Base | Start | Type |
|---|---|---|---|
| lmn | 0000 | 0000 | R |

SPECIAL CPU REGISTERS

PC: 6 SR: 0

SP: 8096 BR: 0

SR Status Flag: OV □ Z □ N □

CPU Mode: User ● Kernel ○

IR: MOV #6, R01

MAR: 6

MDR: MOV #6, I

PROGRAM STACK (RAM)

| | Pos | Val (D) | Addr |
|---|---|---|---|

GENERAL PURPOSE CPU REGISTERS

| Reg | Val (D) | C | Val (D) |
|---|---|---|---|
| □ R00 | 5 | | |
| □ R01 | 6 | | |
| □ R02 | 0 | | |
| □ R03 | 0 | | |
| □ R04 | 0 | | |
| □ R05 | 0 | | |
| □ R06 | 0 | | |
| □ R07 | 0 | | |
| □ R08 | 0 | | |
| □ R09 | 0 | | |
| □ R10 | 0 | | |
| □ R11 | 0 | | |
| □ R12 | 0 | | |
| □ R13 | 0 | | |
| □ R14 | 0 | | |
| □ R15 | 0 | | |
| □ R16 | 0 | | |
| □ R17 | 0 | | |
| □ R18 | 0 | | |
| □ R19 | 0 | | |
| □ R20 | 0 | | |
| □ R21 | 0 | | |
| □ R22 | 0 | | |
| □ R23 | 0 | | |
| □ R24 | 0 | | |
| □ R25 | 0 | | |
| □ R26 | 0 | | |
| □ R27 | 0 | | |
| □ R28 | 0 | | |
| □ R29 | 0 | | |
| □ R30 | 0 | | |

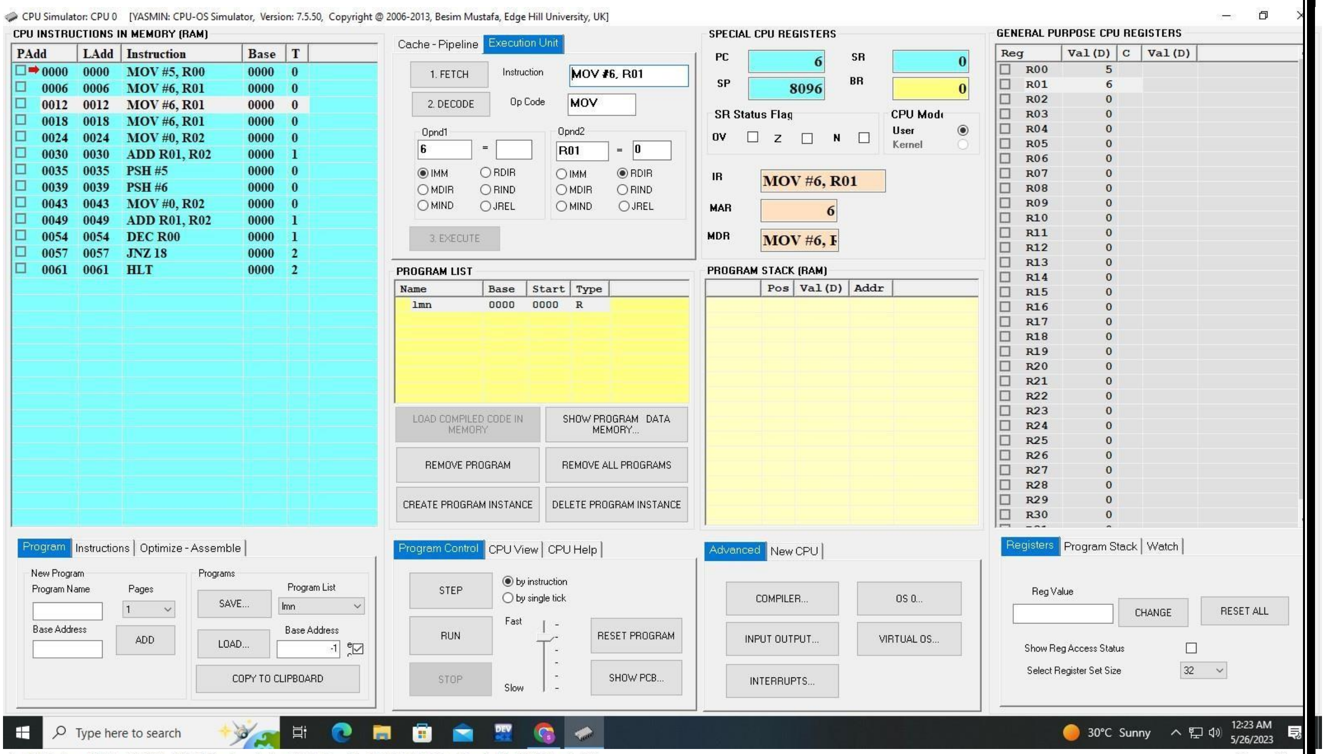
Program List: lmn

Base Address: -1

● by instruction ○ by single tick

Show Reg Access Status □

Select Register Set Size: 32



CPU INSTRUCTIONS IN MEMORY (RAM)

| PAdd | LAdd | Instruction | Base | T |
|---|---|---|---|---|
| ☐ 0000 | 0000 | MOV #5, R00 | 0000 | 0 |
| ☐ 0006 | 0006 | MOV #6, R01 | 0000 | 0 |
| ☐ 0012 | 0012 | MOV #6, R01 | 0000 | 0 |
| ☐ 0018 | 0018 | MOV #6, R01 | 0000 | 0 |
| ☐ 0024 | 0024 | MOV #0, R02 | 0000 | 0 |
| ☐ 0030 | 0030 | ADD R01, R02 | 0000 | 1 |
| ☐ 0035 | 0035 | PSH #5 | 0000 | 0 |
| ☐ 0039 | 0039 | PSH #6 | 0000 | 0 |
| ☐ 0043 | 0043 | MOV #0, R02 | 0000 | 0 |
| ☐ 0049 | 0049 | ADD R01, R02 | 0000 | 1 |
| ☐ 0054 | 0054 | DEC R00 | 0000 | 1 |
| ☐ 0057 | 0057 | JNZ 18 | 0000 | 2 |
| ☐ 0061 | 0061 | HLT | 0000 | 2 |

Instruction: MOV #6, R01
Op Code: MOV
Opnd1: 6 = 
● IMM ○ RDIR ○ MDIR ○ RIND ○ MIND ○ JREL
Opnd2: R01 = 0
○ IMM ● RDIR ○ MDIR ○ RIND ○ MIND ○ JREL

SPECIAL CPU REGISTERS

PC 6 SR 0
SP 8096 BR 0

SR Status Flag: OV ☐ Z ☐ N ☐
CPU Mode: User ● Kernel ○

IR: MOV #6, R01
MAR: 6
MDR: MOV #6, F

PROGRAM LIST

| Name | Base | Start | Type |
|---|---|---|---|
| lmn | 0000 | 0000 | R |

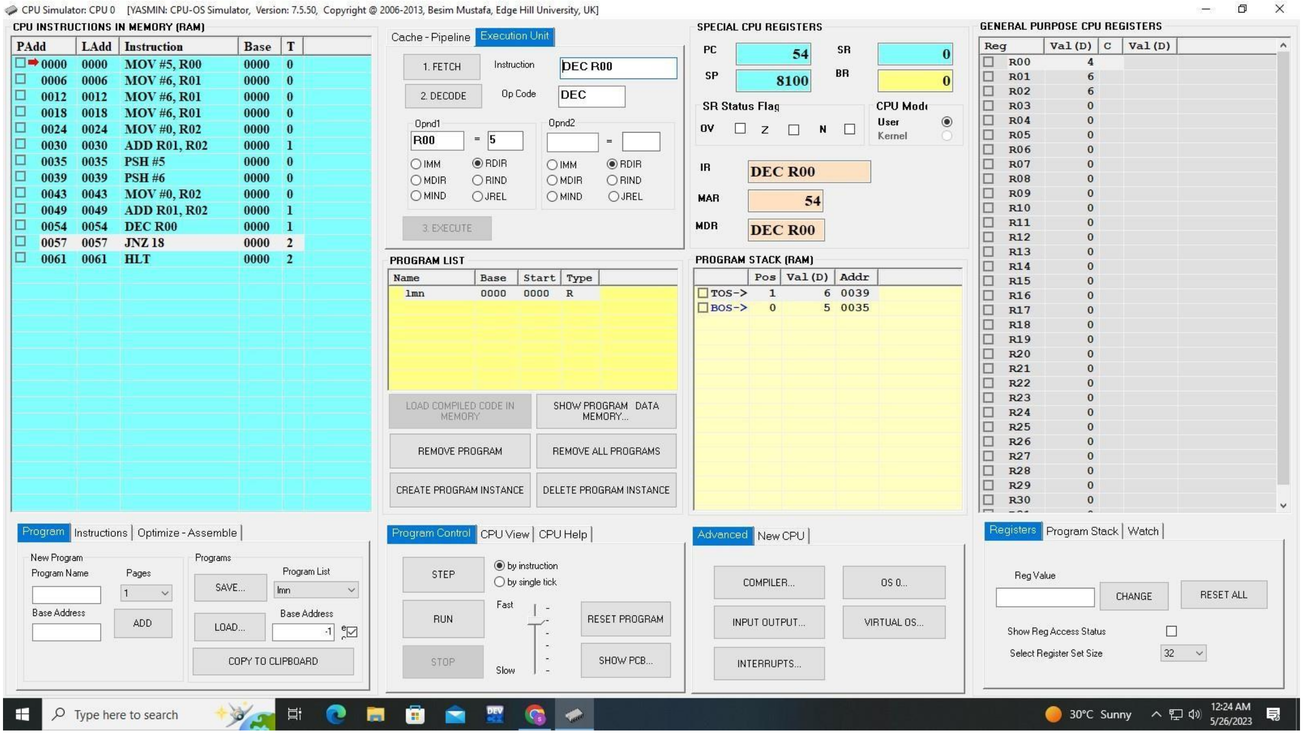
PROGRAM STACK (RAM)

| | Pos | Val (D) | Addr |
|---|---|---|---|

GENERAL PURPOSE CPU REGISTERS

| Reg | Val (D) | C | Val (D) |
|---|---|---|---|
| ☐ R00 | 5 | | |
| ☐ R01 | 6 | | |
| ☐ R02 | 0 | | |
| ☐ R03 | 0 | | |
| ☐ R04 | 0 | | |
| ☐ R05 | 0 | | |
| ☐ R06 | 0 | | |
| ☐ R07 | 0 | | |
| ☐ R08 | 0 | | |
| ☐ R09 | 0 | | |
| ☐ R10 | 0 | | |
| ☐ R11 | 0 | | |
| ☐ R12 | 0 | | |
| ☐ R13 | 0 | | |
| ☐ R14 | 0 | | |
| ☐ R15 | 0 | | |
| ☐ R16 | 0 | | |
| ☐ R17 | 0 | | |
| ☐ R18 | 0 | | |
| ☐ R19 | 0 | | |
| ☐ R20 | 0 | | |
| ☐ R21 | 0 | | |
| ☐ R22 | 0 | | |
| ☐ R23 | 0 | | |
| ☐ R24 | 0 | | |
| ☐ R25 | 0 | | |
| ☐ R26 | 0 | | |
| ☐ R27 | 0 | | |
| ☐ R28 | 0 | | |
| ☐ R29 | 0 | | |
| ☐ R30 | 0 | | |

New Program
Program Name:
Pages: 1
Base Address:
Programs
Program List: lmn
Base Address: -1
● by instruction ○ by single tick
Reg Value:
Show Reg Access Status ☐
Select Register Set Size: 32



CPU INSTRUCTIONS IN MEMORY (RAM)

| PAdd | LAdd | Instruction | Base | T |
|---|---|---|---|---|
| ☐ 0000 | 0000 | MOV #5, R00 | 0000 | 0 |
| ☐ 0006 | 0006 | MOV #6, R01 | 0000 | 0 |
| ☐ 0012 | 0012 | MOV #6, R01 | 0000 | 0 |
| ☐ 0018 | 0018 | MOV #6, R01 | 0000 | 0 |
| ☐ 0024 | 0024 | MOV #0, R02 | 0000 | 0 |
| ☐ 0030 | 0030 | ADD R01, R02 | 0000 | 1 |
| ☐ 0035 | 0035 | PSH #5 | 0000 | 0 |
| ☐ 0039 | 0039 | PSH #6 | 0000 | 0 |
| ☐ 0043 | 0043 | MOV #0, R02 | 0000 | 0 |
| ☐ 0049 | 0049 | ADD R01, R02 | 0000 | 1 |
| ☐ 0054 | 0054 | DEC R00 | 0000 | 1 |
| ☐ 0057 | 0057 | JNZ 18 | 0000 | 2 |
| ☐ 0061 | 0061 | HLT | 0000 | 2 |

Instruction: DEC R00
Op Code: DEC
Opnd1: R00 = 5
○ IMM ● RDIR ○ MDIR ○ RIND ○ MIND ○ JREL
Opnd2: = 
○ IMM ● RDIR ○ MDIR ○ RIND ○ MIND ○ JREL

SPECIAL CPU REGISTERS

PC 54 SR 0
SP 8100 BR 0

SR Status Flag: OV ☐ Z ☐ N ☐
CPU Mode: User ● Kernel ○

IR: DEC R00
MAR: 54
MDR: DEC R00

PROGRAM LIST

| Name | Base | Start | Type |
|---|---|---|---|
| lmn | 0000 | 0000 | R |

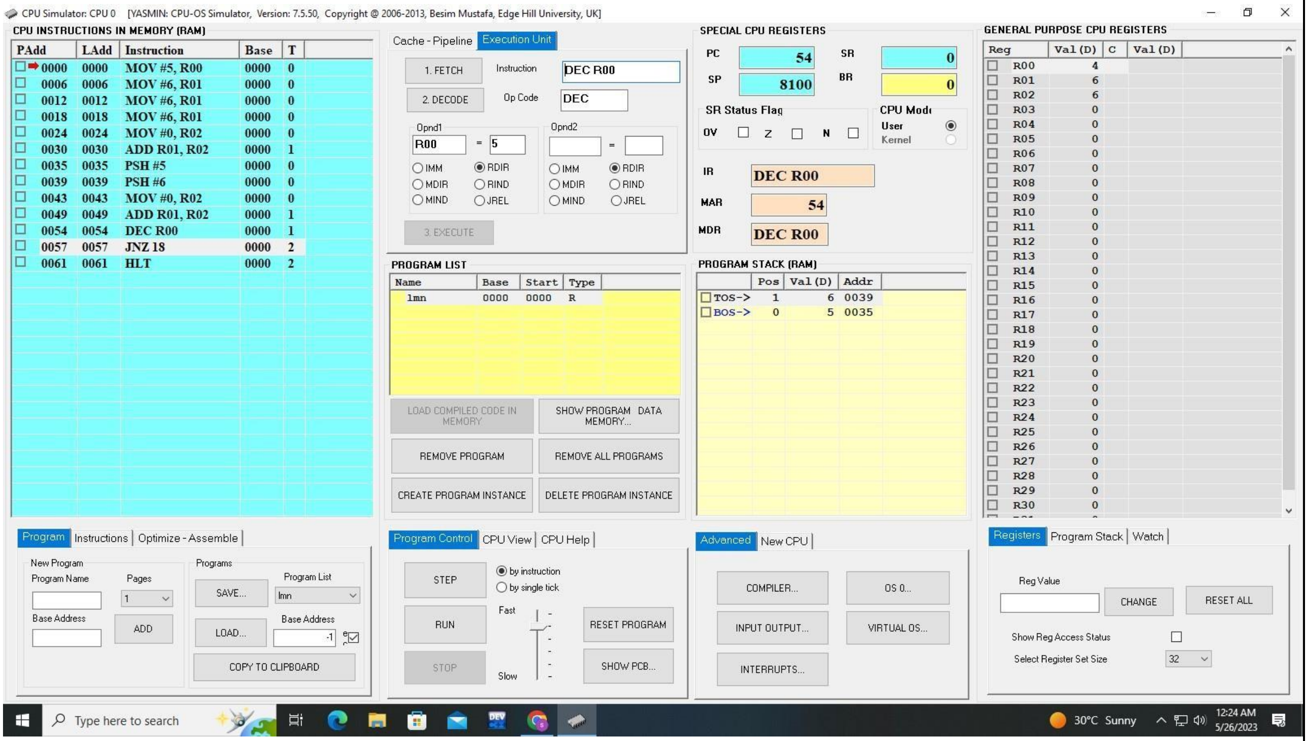
PROGRAM STACK (RAM)

| | Pos | Val (D) | Addr |
|---|---|---|---|
| ☐ TOS-> | 1 | 6 | 0039 |
| ☐ BOS-> | 0 | 5 | 0035 |

GENERAL PURPOSE CPU REGISTERS

| Reg | Val (D) | C | Val (D) |
|---|---|---|---|
| ☐ R00 | 4 | | |
| ☐ R01 | 6 | | |
| ☐ R02 | 6 | | |
| ☐ R03 | 0 | | |
| ☐ R04 | 0 | | |
| ☐ R05 | 0 | | |
| ☐ R06 | 0 | | |
| ☐ R07 | 0 | | |
| ☐ R08 | 0 | | |
| ☐ R09 | 0 | | |
| ☐ R10 | 0 | | |
| ☐ R11 | 0 | | |
| ☐ R12 | 0 | | |
| ☐ R13 | 0 | | |
| ☐ R14 | 0 | | |
| ☐ R15 | 0 | | |
| ☐ R16 | 0 | | |
| ☐ R17 | 0 | | |
| ☐ R18 | 0 | | |
| ☐ R19 | 0 | | |
| ☐ R20 | 0 | | |
| ☐ R21 | 0 | | |
| ☐ R22 | 0 | | |
| ☐ R23 | 0 | | |
| ☐ R24 | 0 | | |
| ☐ R25 | 0 | | |
| ☐ R26 | 0 | | |
| ☐ R27 | 0 | | |
| ☐ R28 | 0 | | |
| ☐ R29 | 0 | | |
| ☐ R30 | 0 | | |

New Program
Program Name:
Pages: 1
Base Address:
Programs
Program List: lmn
Base Address: -1
● by instruction ○ by single tick
Reg Value:
Show Reg Access Status ☐
Select Register Set Size: 32



CPU Simulator: CPU 0 [YASMIN: CPU-OS Simulator, Version: 7.5.50, Copyright @ 2006-2013, Besim Mustafa, Edge Hill University, UK]

CPU INSTRUCTIONS IN MEMORY (RAM)

| PAdd | LAdd | Instruction | Base | T |
|---|---|---|---|---|
| 0000 | 0000 | MOV #5, R00 | 0000 | 0 |
| 0006 | 0006 | MOV #6, R01 | 0000 | 0 |
| 0012 | 0012 | MOV #6, R01 | 0000 | 0 |
| 0018 | 0018 | MOV #6, R01 | 0000 | 0 |
| 0024 | 0024 | MOV #0, R02 | 0000 | 0 |
| 0030 | 0030 | ADD R01, R02 | 0000 | 1 |
| 0035 | 0035 | PSH #5 | 0000 | 0 |
| 0039 | 0039 | PSH #6 | 0000 | 0 |
| 0043 | 0043 | MOV #0, R02 | 0000 | 0 |
| 0049 | 0049 | ADD R01, R02 | 0000 | 1 |
| 0054 | 0054 | DEC R00 | 0000 | 1 |
| 0057 | 0057 | JNZ 18 | 0000 | 2 |
| 0061 | 0061 | HLT | 0000 | 2 |

Cache - Pipeline | Execution Unit

1. FETCH Instruction: DEC R00
2. DECODE Op Code: DEC
Opnd1: R00 = 5 ○ IMM ● RDIR ○ MDIR ○ RIND ○ MIND ○ JREL
Opnd2: = ○ IMM ● RDIR ○ MDIR ○ RIND ○ MIND ○ JREL
3. EXECUTE

SPECIAL CPU REGISTERS

PC 54 SR 0
SP 8100 BR 0

SR Status Flag: OV □ Z □ N □
CPU Mode: User ● Kernel ○

IR: DEC R00
MAR: 54
MDR: DEC R00

PROGRAM LIST

| Name | Base | Start | Type |
|---|---|---|---|
| lmn | 0000 | 0000 | R |

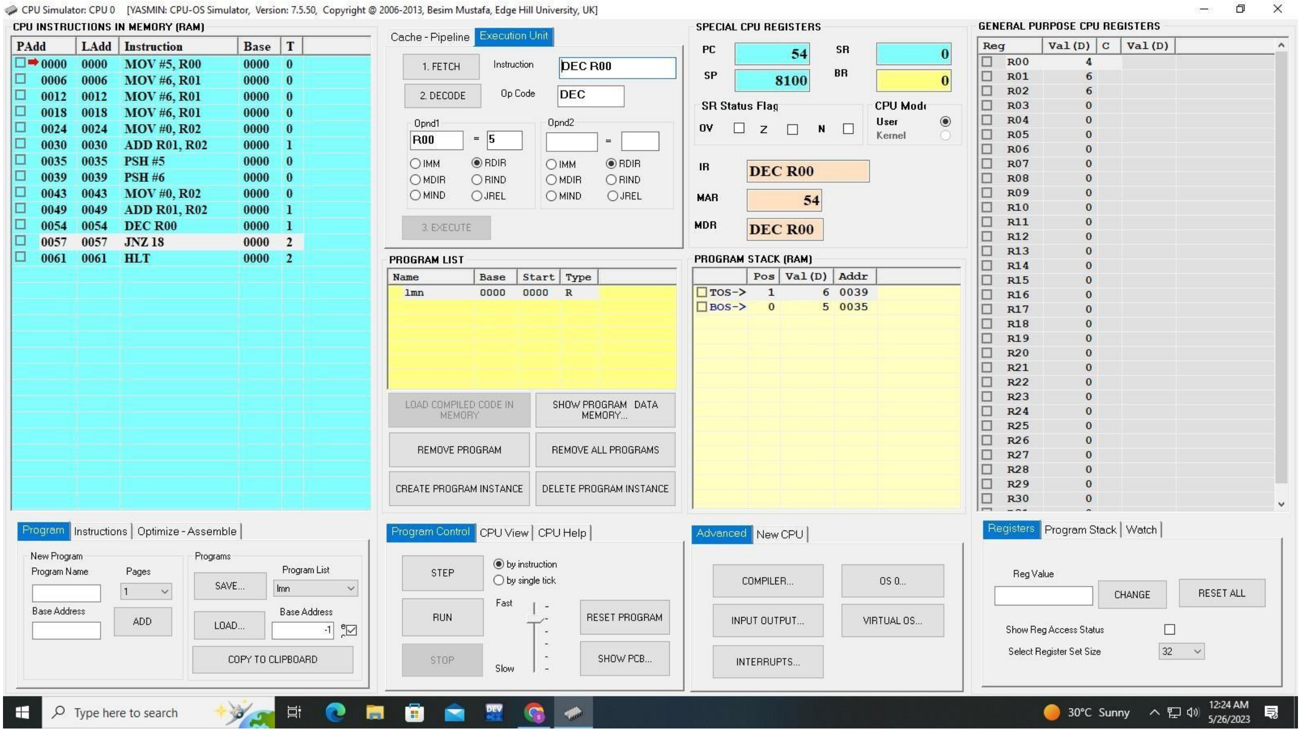
PROGRAM STACK (RAM)

| | Pos | Val (D) | Addr |
|---|---|---|---|
| □ TOS-> | 1 | 6 | 0039 |
| □ BOS-> | 0 | 5 | 0035 |

GENERAL PURPOSE CPU REGISTERS

| Reg | Val (D) | C | Val (D) |
|---|---|---|---|
| R00 | 4 | | |
| R01 | 6 | | |
| R02 | 6 | | |
| R03 | 0 | | |
| R04 | 0 | | |
| R05 | 0 | | |
| R06 | 0 | | |
| R07 | 0 | | |
| R08 | 0 | | |
| R09 | 0 | | |
| R10 | 0 | | |
| R11 | 0 | | |
| R12 | 0 | | |
| R13 | 0 | | |
| R14 | 0 | | |
| R15 | 0 | | |
| R16 | 0 | | |
| R17 | 0 | | |
| R18 | 0 | | |
| R19 | 0 | | |
| R20 | 0 | | |
| R21 | 0 | | |
| R22 | 0 | | |
| R23 | 0 | | |
| R24 | 0 | | |
| R25 | 0 | | |
| R26 | 0 | | |
| R27 | 0 | | |
| R28 | 0 | | |
| R29 | 0 | | |
| R30 | 0 | | |

Program Name: Pages: 1 Program List: lmn Base Address: -1
Select Register Set Size: 32



CPU Simulator: CPU 0 [YASMIN: CPU-OS Simulator, Version: 7.5.50, Copyright @ 2006-2013, Besim Mustafa, Edge Hill University, UK]

CPU INSTRUCTIONS IN MEMORY (RAM)

| PAdd | LAdd | Instruction | Base | T |
|---|---|---|---|---|
| 0000 | 0000 | MOV #5, R00 | 0000 | 0 |
| 0006 | 0006 | MOV #6, R01 | 0000 | 0 |
| 0012 | 0012 | MOV #6, R01 | 0000 | 0 |
| 0018 | 0018 | MOV #6, R01 | 0000 | 0 |
| 0024 | 0024 | MOV #0, R02 | 0000 | 0 |
| 0030 | 0030 | ADD R01, R02 | 0000 | 1 |
| 0035 | 0035 | PSH #5 | 0000 | 0 |
| 0039 | 0039 | PSH #6 | 0000 | 0 |
| 0043 | 0043 | MOV #0, R02 | 0000 | 0 |
| 0049 | 0049 | ADD R01, R02 | 0000 | 1 |
| 0054 | 0054 | DEC R00 | 0000 | 1 |
| 0057 | 0057 | JNZ 18 | 0000 | 2 |
| 0061 | 0061 | HLT | 0000 | 2 |

Cache - Pipeline | Execution Unit

1. FETCH Instruction: DEC R00
2. DECODE Op Code: DEC
Opnd1: R00 = 5 ○ IMM ● RDIR ○ MDIR ○ RIND ○ MIND ○ JREL
Opnd2: = ○ IMM ● RDIR ○ MDIR ○ RIND ○ MIND ○ JREL
3. EXECUTE

SPECIAL CPU REGISTERS

PC 54 SR 0
SP 8100 BR 0

SR Status Flag: OV □ Z □ N □
CPU Mode: User ● Kernel ○

IR: DEC R00
MAR: 54
MDR: DEC R00

PROGRAM LIST

| Name | Base | Start | Type |
|---|---|---|---|
| lmn | 0000 | 0000 | R |

PROGRAM STACK (RAM)

| | Pos | Val (D) | Addr |
|---|---|---|---|
| □ TOS-> | 1 | 6 | 0039 |
| □ BOS-> | 0 | 5 | 0035 |

GENERAL PURPOSE CPU REGISTERS

| Reg | Val (D) | C | Val (D) |
|---|---|---|---|
| R00 | 4 | | |
| R01 | 6 | | |
| R02 | 6 | | |
| R03 | 0 | | |
| R04 | 0 | | |
| R05 | 0 | | |
| R06 | 0 | | |
| R07 | 0 | | |
| R08 | 0 | | |
| R09 | 0 | | |
| R10 | 0 | | |
| R11 | 0 | | |
| R12 | 0 | | |
| R13 | 0 | | |
| R14 | 0 | | |
| R15 | 0 | | |
| R16 | 0 | | |
| R17 | 0 | | |
| R18 | 0 | | |
| R19 | 0 | | |
| R20 | 0 | | |
| R21 | 0 | | |
| R22 | 0 | | |
| R23 | 0 | | |
| R24 | 0 | | |
| R25 | 0 | | |
| R26 | 0 | | |
| R27 | 0 | | |
| R28 | 0 | | |
| R29 | 0 | | |
| R30 | 0 | | |

Program Name: Pages: 1 Program List: lmn Base Address: -1
Select Register Set Size: 32