Lab 10

EE214: Digital Circuits Laboratory

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4 March 2022

1 Aim

Design and Implementation of Asynchronous Down Counters using minimum number of JK Flip-Flops and NAND gates (if any).

2 Summary of the experiment

Design of mod-8 and mod-5 asynchronous down counters using JK Flip-Flops and NAND gates, implementation on the breadboard, then testing and verification using state diagram.

3 Components Used

IC SN74LS76A (JK Flip-Flop), IC 7400 (NAND), Function Generator (Clock Signal), 1 kΩ resistor array, DIP switches, LED displays, breadboard, conducting wires, power supply.

4 Problem Statements

- Design and implement a mod-8 asynchronous down counter. Clearly indicate the minimum number of JK Flip-flops required (if any) and NAND gates required (if any).
- Design and implement a mod-5 asynchronous down counter. Clearly indicate the minimum number of JK Flip-flops required (if any) and NAND gates required (if any).

5 Design Procedure: Circuit Diagrams

Note: Circuit Diagram is included with the snapshots.

6 Circuit and Simulation Snapshots

(Circuit snapshots are included in the later pages of this report.)

7 Design Procedure: State Diagrams

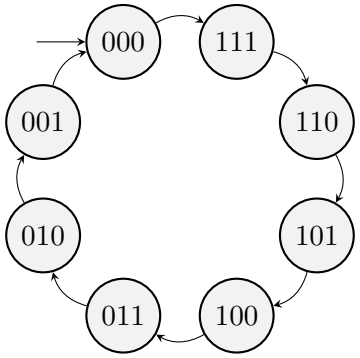

Figure 1: MOD-8 Asynchronous Down Counter

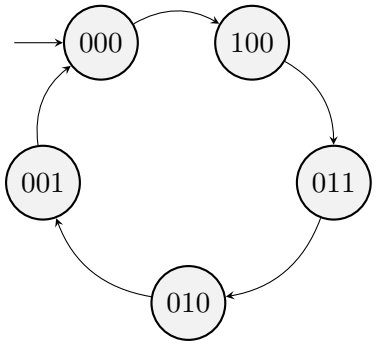

Figure 2: MOD-5 Asynchronous Down Counter

8 Results and Discussions

- For the Mod-8 Asynchronous Down Counter, we used 3 JK Flip-Flops and zero NAND gates. Here, each Flip-Flop handles one bit of the number. (Mod-8 would require all 3-bit numbers)
- For the Mod-5 Asynchronous Down Counter, we used 3 JK Flip-Flops and 1 NAND gate. Here, each Flip-Flop handles one bit of the number, but when the counter goes from 000 to 111, it is forcibly changed to 100; it bypasses the numbers 7, 6, 5 (111, 110, 101) respectively.
- The clock signal should be drawn from the function generator, and should preferably have a peak-to-peak voltage of 5V. The frequency should be about 1Hz, for better observability.
- We must design the circuit in such a manner that testing and debugging goes smoothly.

9 Conclusion

We designed and implemented a Mod-8 Asynchronous Down Counter, and a Mod-5 Asynchronous Down Counter. The outputs obtained could be verified using the state diagram.

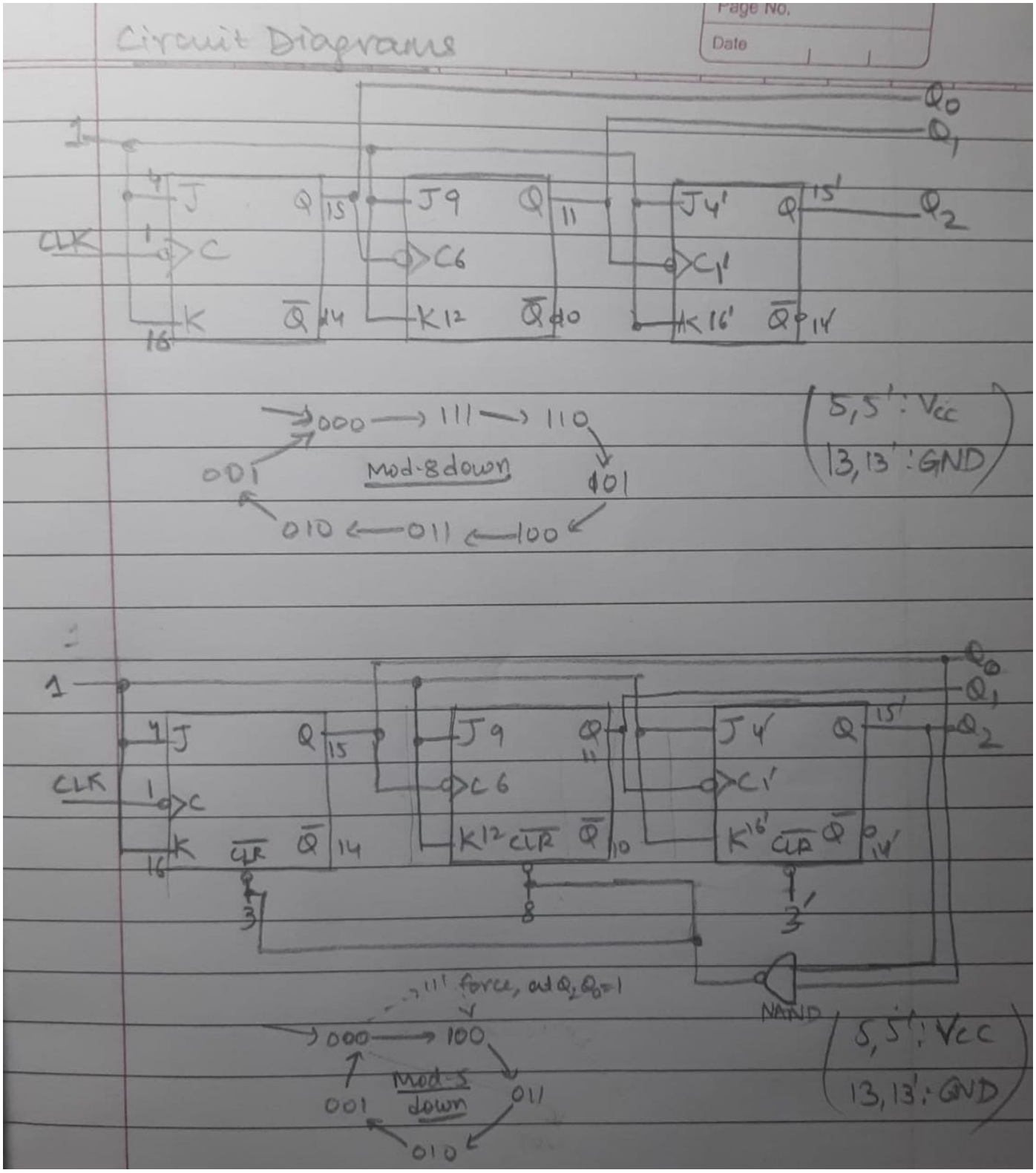

Figure 3: Circuit Diagram

Mod-8 Asynchronous down counter: