

Design Procedure and Circuit Diagram.

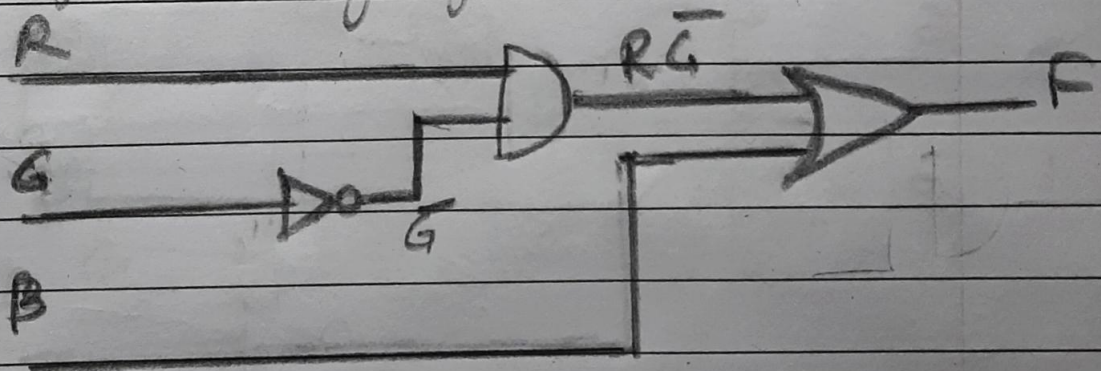
① = open (on)

1 = closed (off)

	GB	$G+B$	$G+\bar{B}$	$\bar{G}+B$	$\bar{G}+\bar{B}$
R	00	01	11	10	
$R=0$	0			0	
$\bar{R}=1$				0	

$$F = (R+B)(\bar{G}+B) \quad (\text{POS form})$$

(a) Using basic logic gates :-



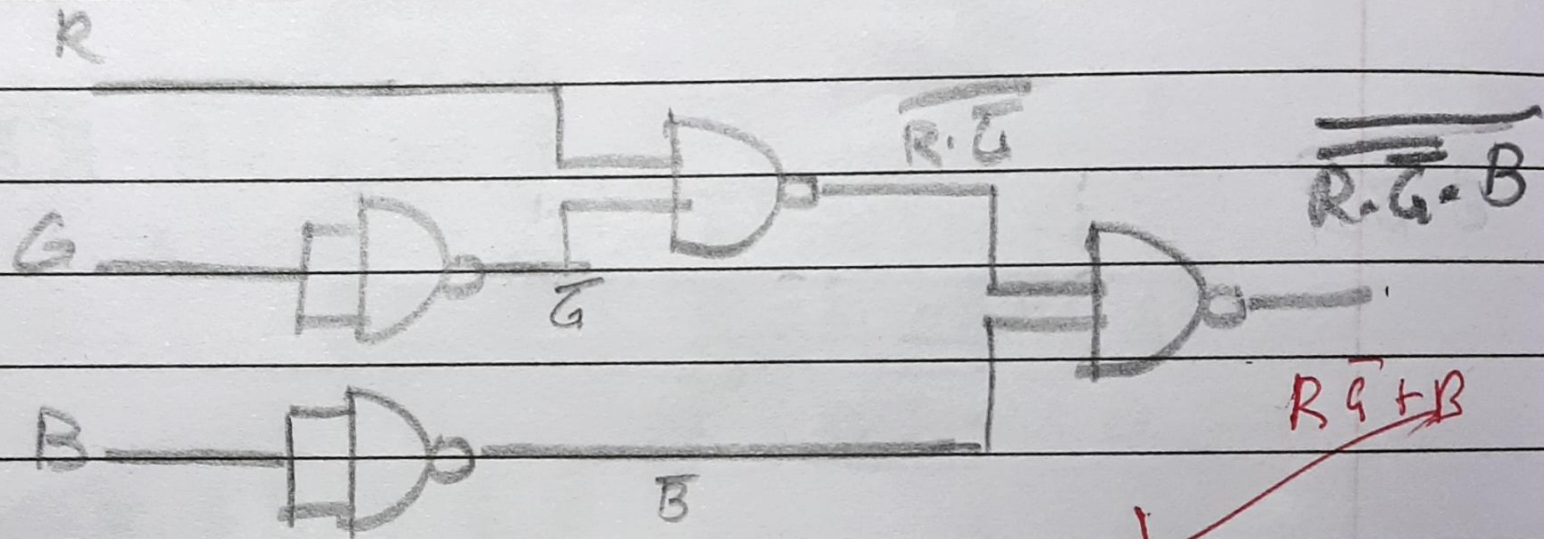
$$F = R\bar{G} + B$$

SGanguly

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$$F = \overline{R\bar{G} + B} = \overline{R\bar{G}} \cdot \bar{B}$$

(b) using NAND.



$R \cdot G \cdot B$

Sengul

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