

LAB 3
Roll No.: 200010003

Aim: Designing logic gates using CMOS (Complementary Metal Oxide Semiconductor) logic.

Summary of the experiment: Study of logic gates using CMOS logic (Digital ICs), verifying their functionality and rigging up of circuits.

Components used: HCC4007UB IC, 1K ohm resistor array, DIP switches, LED displays, breadboard, power supply.

Design Procedure and Circuit Diagram: *(attached below)*

Results and Discussions:

1. We have constructed the required logic gates (AND, OR, XOR, NAND, NOR, XNOR) using CMOS logic, with the help of the HCC4007UB IC. We verified the functionality of the constructed circuit using truth tables of the logic gates.
2. With the use of the CMOS logic family, we have greatly reduced the circuit complexity, and the density of logic functions per chip.

Conclusion:

We constructed logic circuits for the basic (AND, OR), universal (NAND, NOR), and special (XOR, XNOR) logic gates using the CMOS logic family, while verifying their functionality via truth table.

Design Procedure (Truth Table) and circuit Diagrams

Page No.

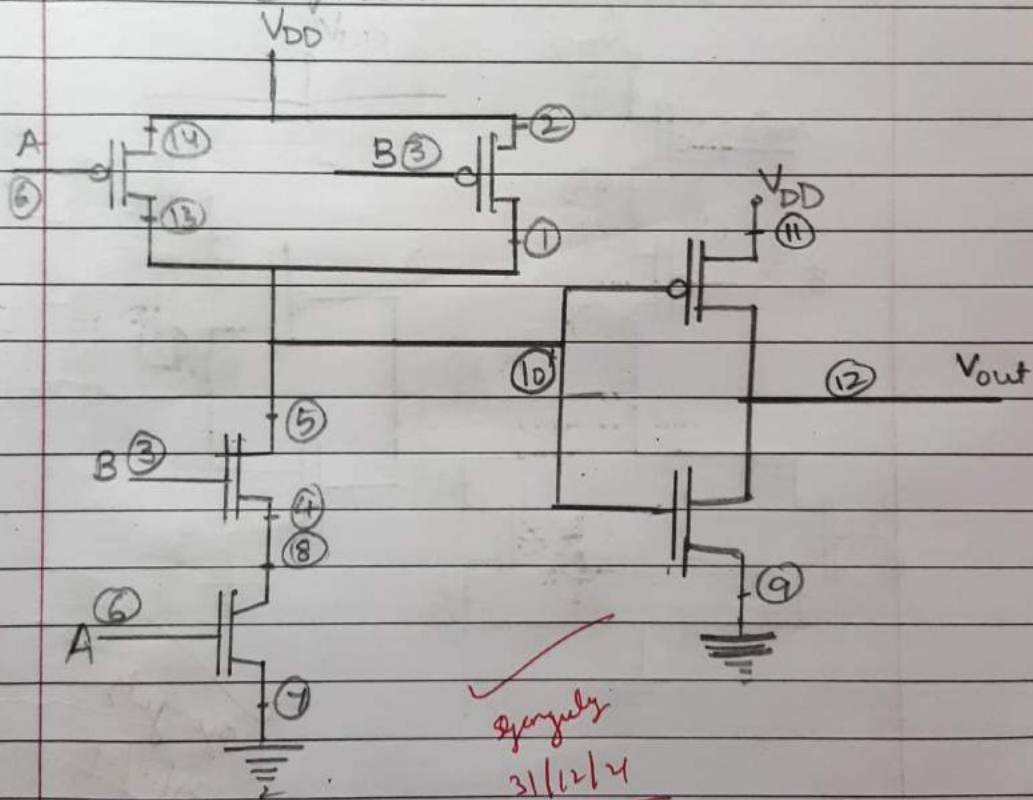
Date

① AND

→ Truth Table

X	Y	$X \cdot Y$
0	0	0
0	1	0
1	0	0
1	1	1

→ Circuit Diagram

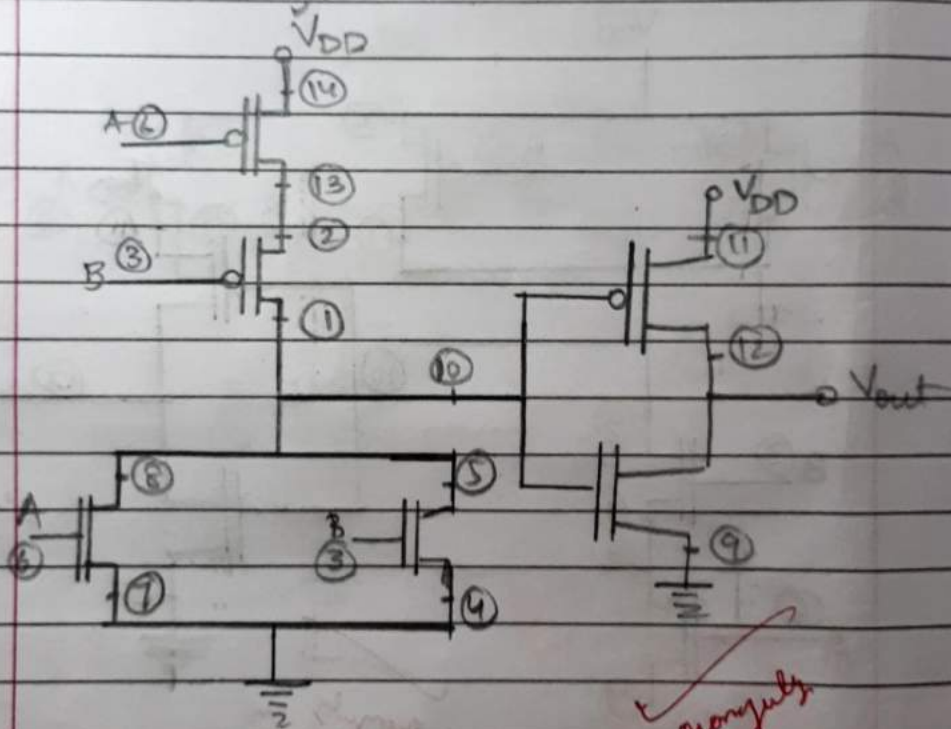


② OR

→ Truth Table

X	Y	X+Y
0	0	0
0	1	1
1	0	1
1	1	1

→ Circuit Diagram



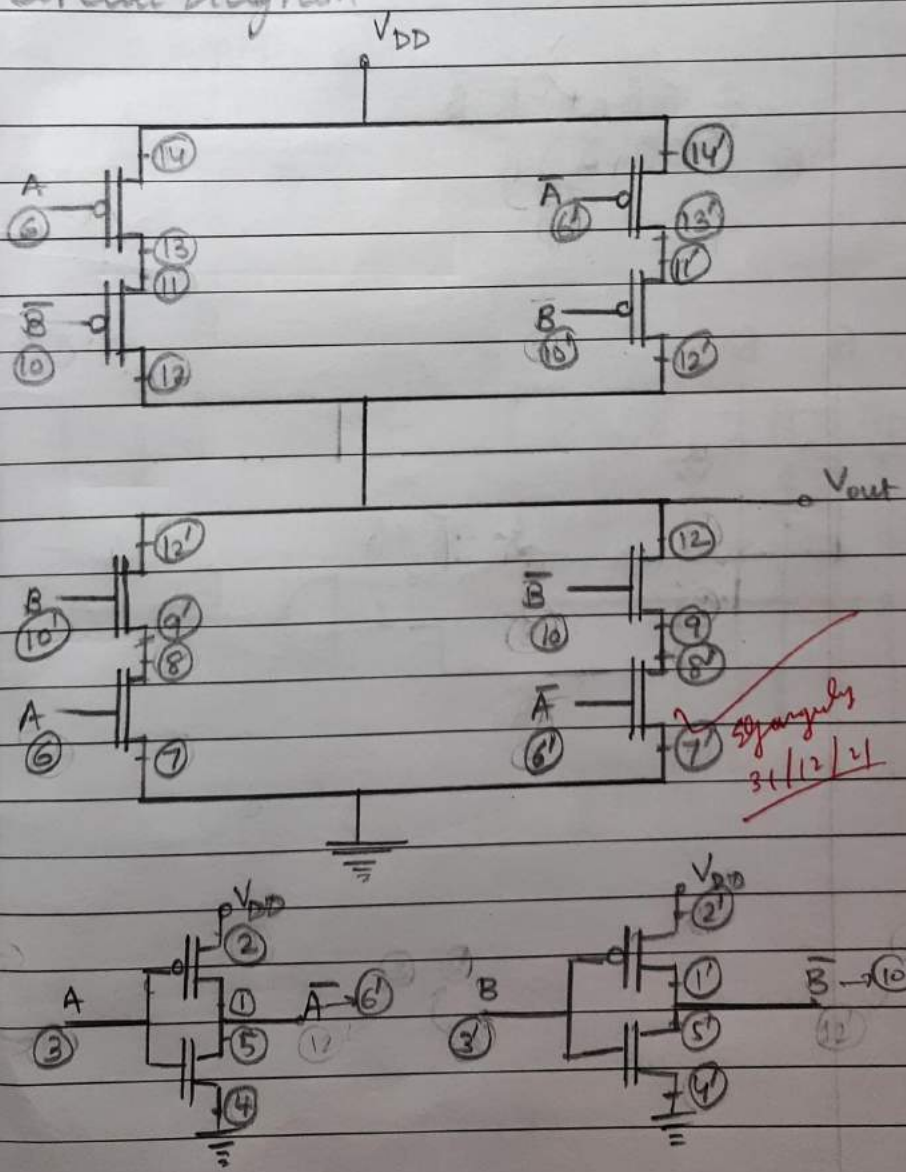
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XOR

→ Truth Table

X	Y	$X \oplus Y = \overline{X}Y + X\overline{Y}$
0	0	0
0	1	1
1	0	1
1	1	0

→ Circuit Diagram

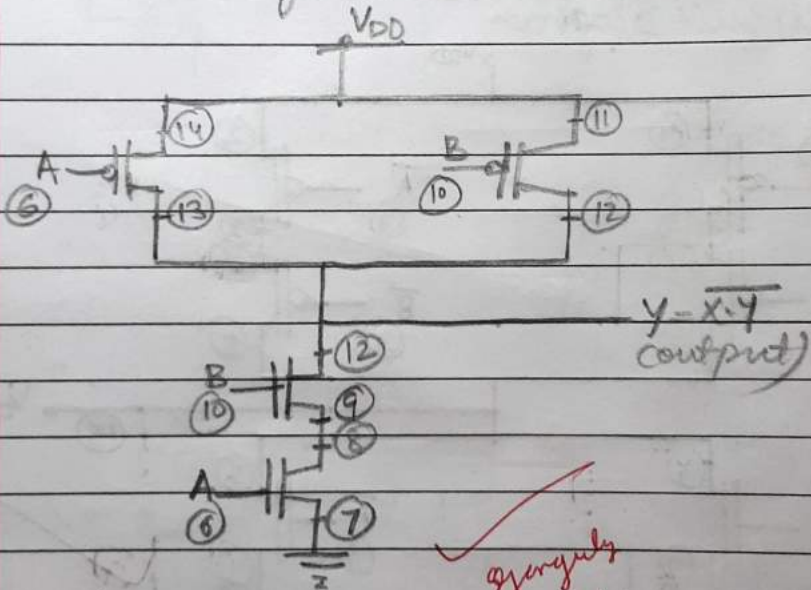


④ NAND

→ Truth Table

X	Y	$\overline{X \cdot Y}$
0	0	1
0	1	1
1	0	1
1	1	0

→ Circuit Diagram



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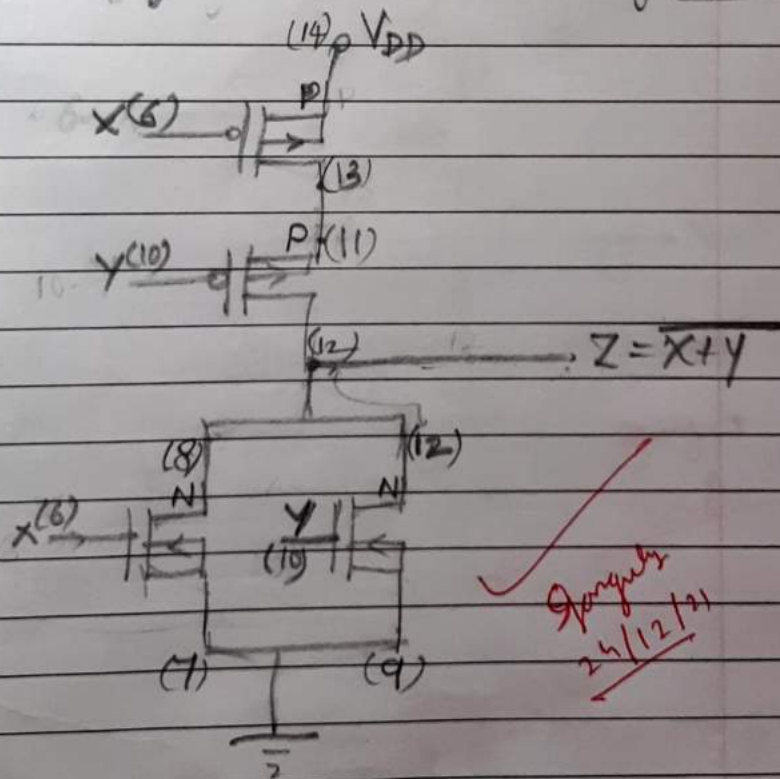
⑤ NOR

→ Truth table

X	Y	$\overline{X+Y} = (X \text{ NOR } Y)$
0	0	1
0	1	0
1	0	0
1	1	0

→ Circuit Diagram (CMOS)

(using IC HCF4007)



X → pin 6
Y → pin 10

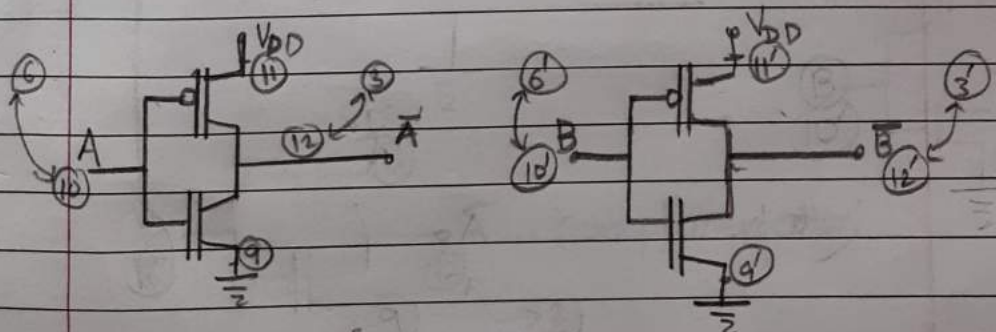
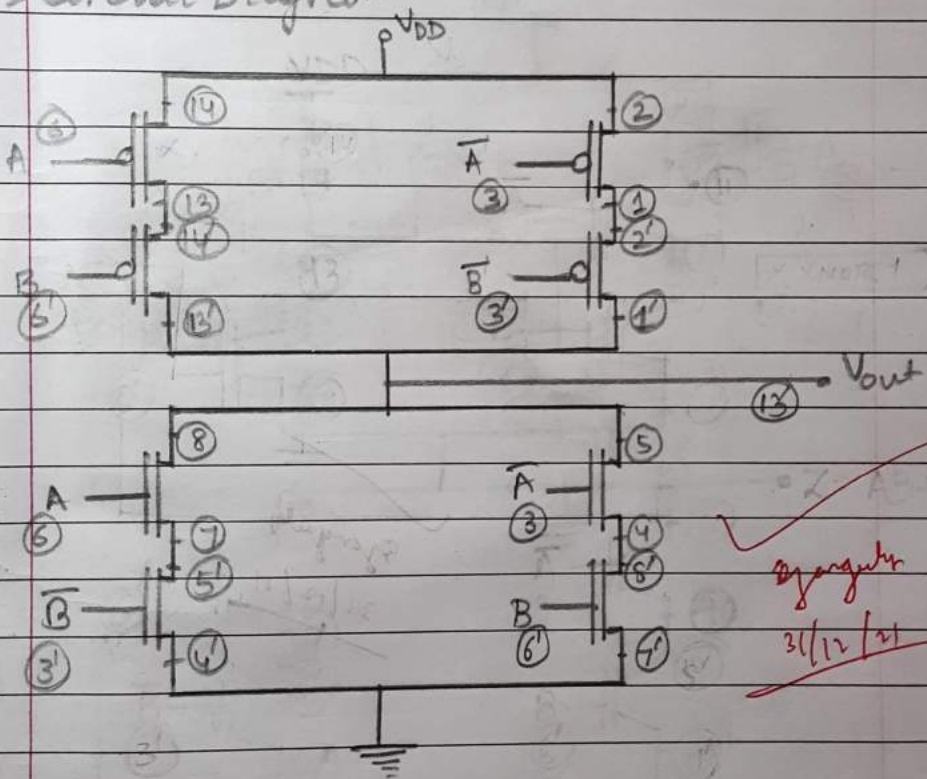
⑥ XNOR

XNOR YNOR

→ Truth Table

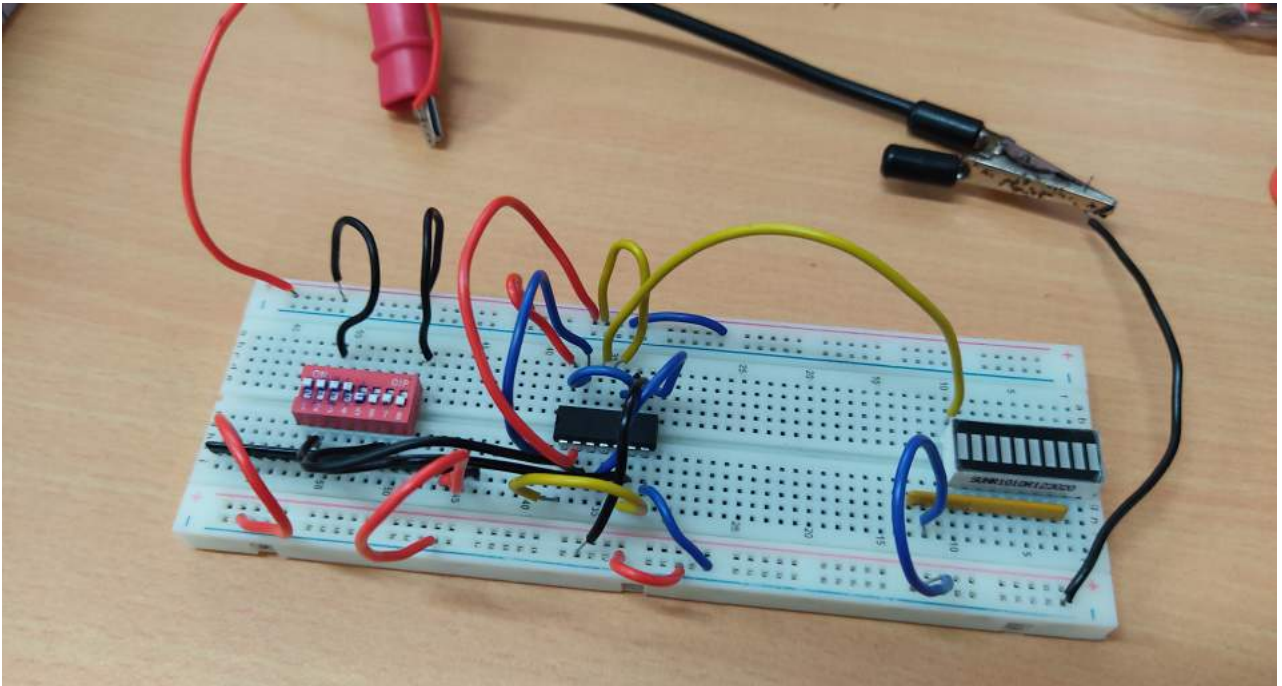
X	Y	$X \odot Y = X \text{ XNOR } Y$ ($X \odot Y = XY + \bar{X}\bar{Y}$)
0	0	1
0	1	0
1	0	0
1	1	1

→ Circuit Diagram

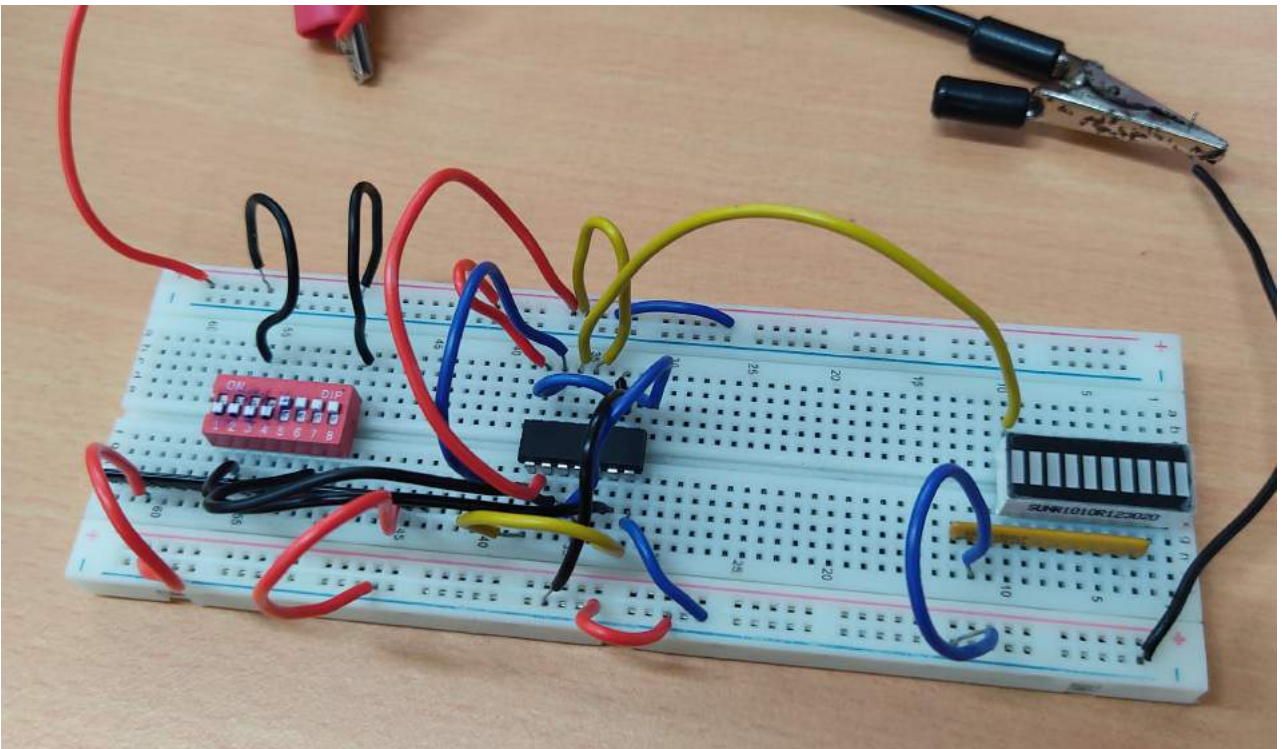


Circuit Snapshots:

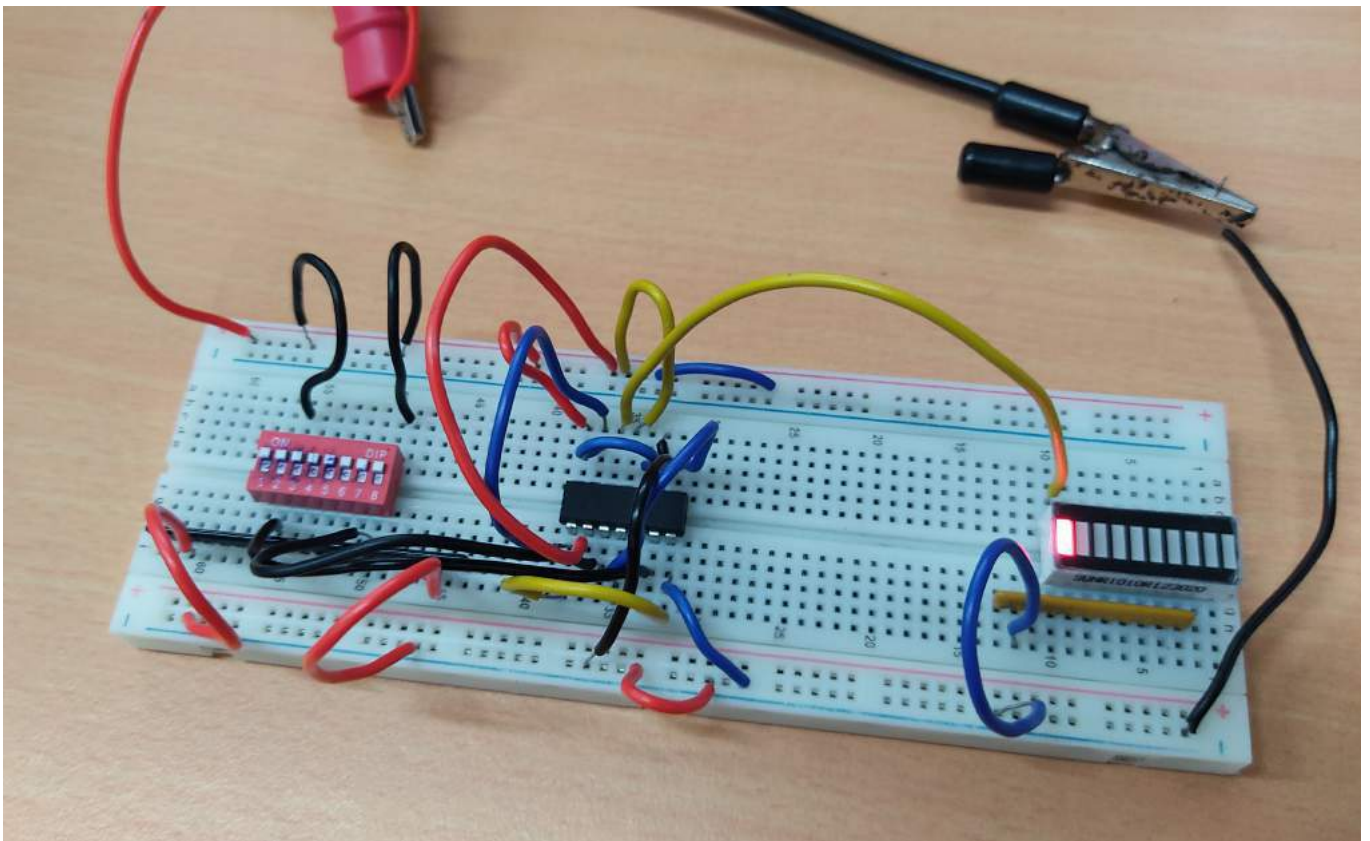
AND:



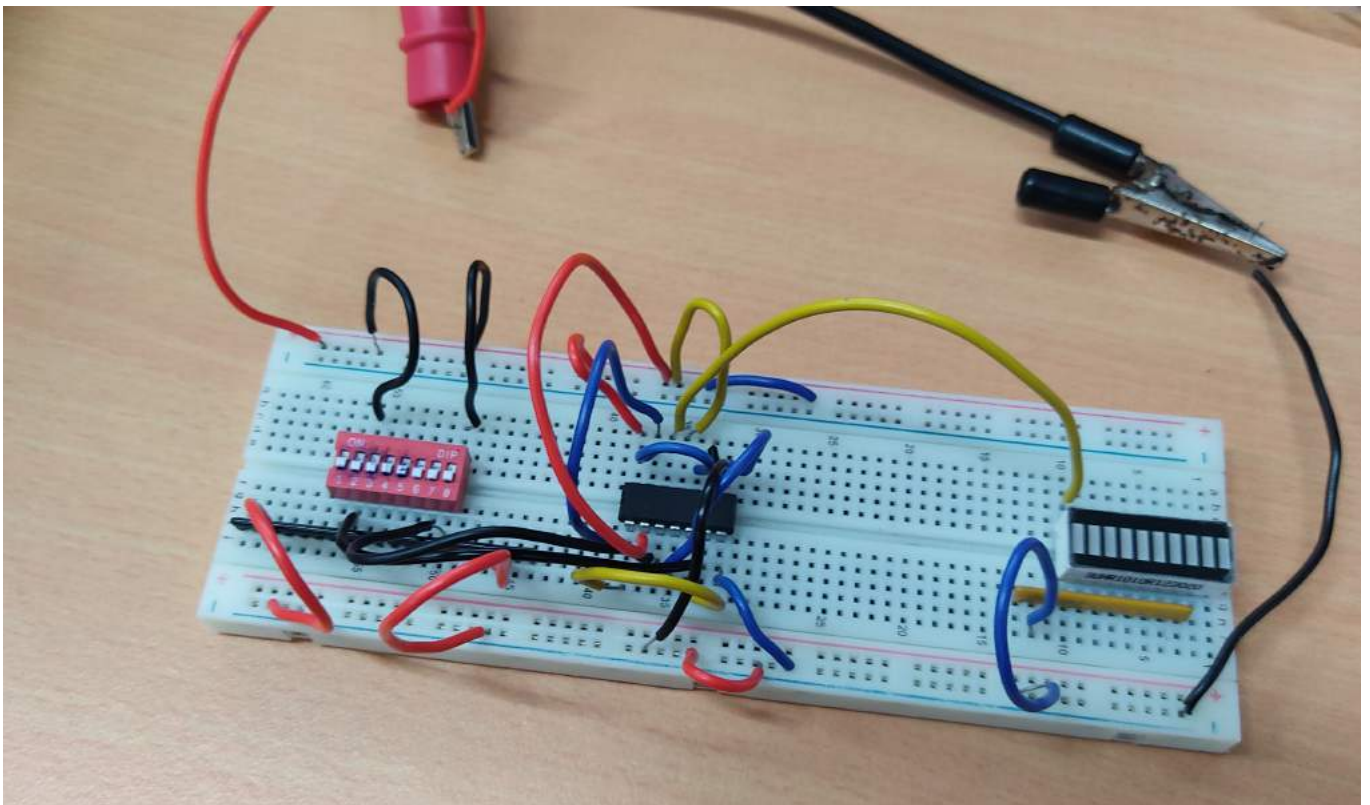
$1_0 \rightarrow 0$



$0_1 \rightarrow 0$

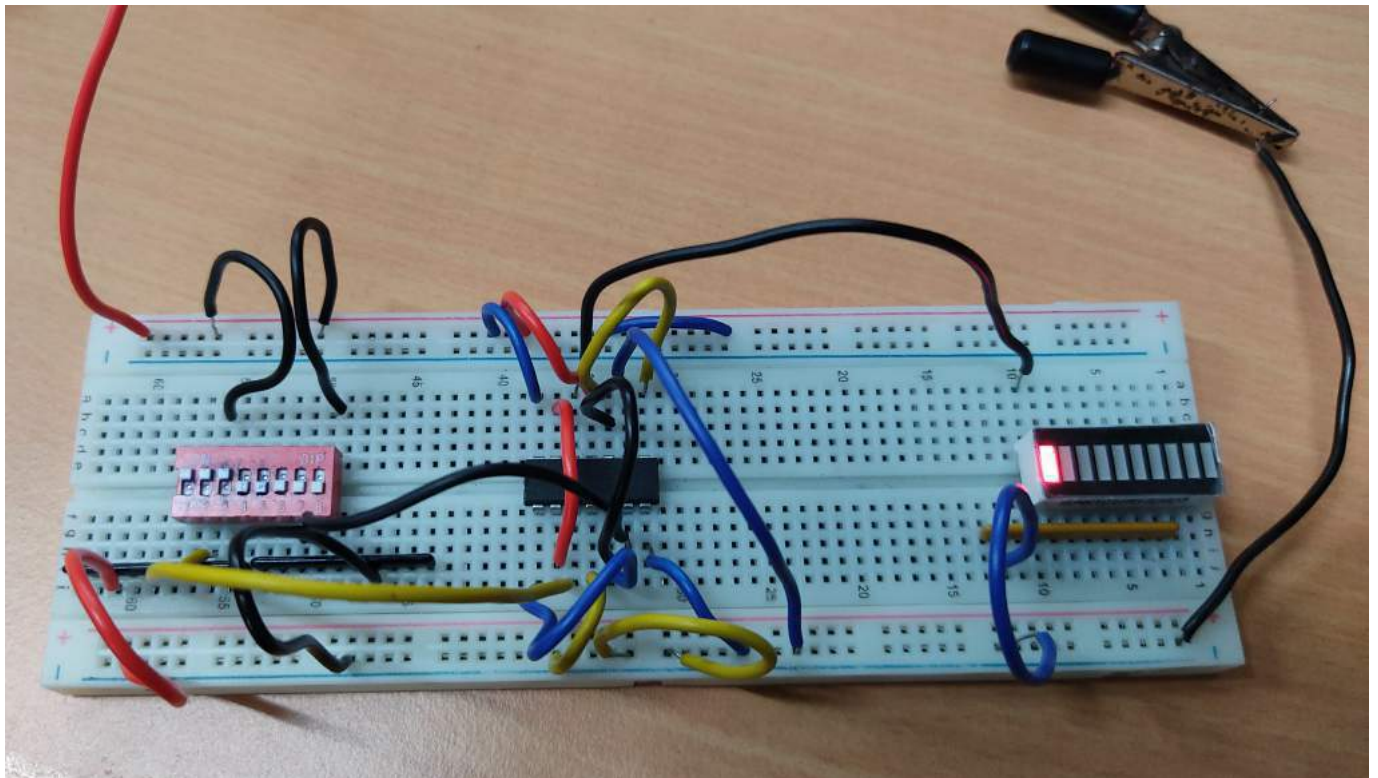


1_1 \rightarrow 1

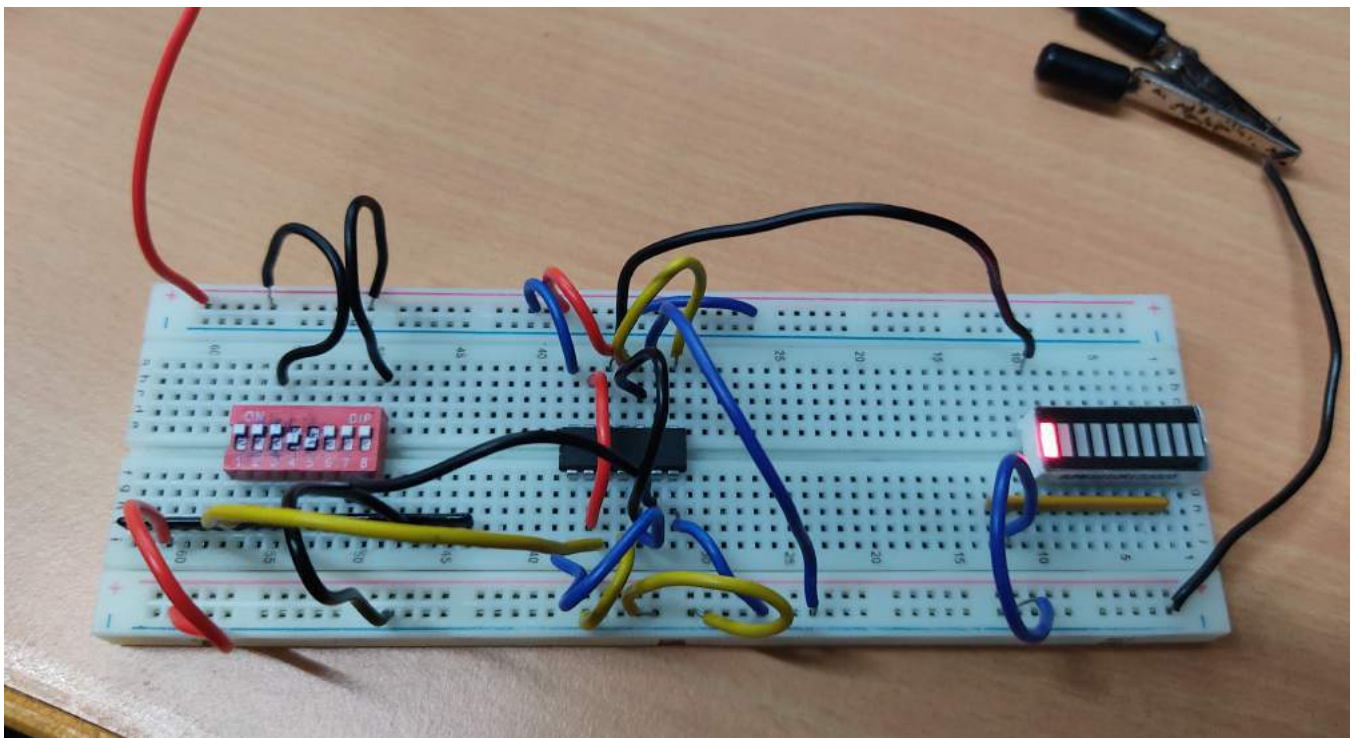


0_0 \rightarrow 0

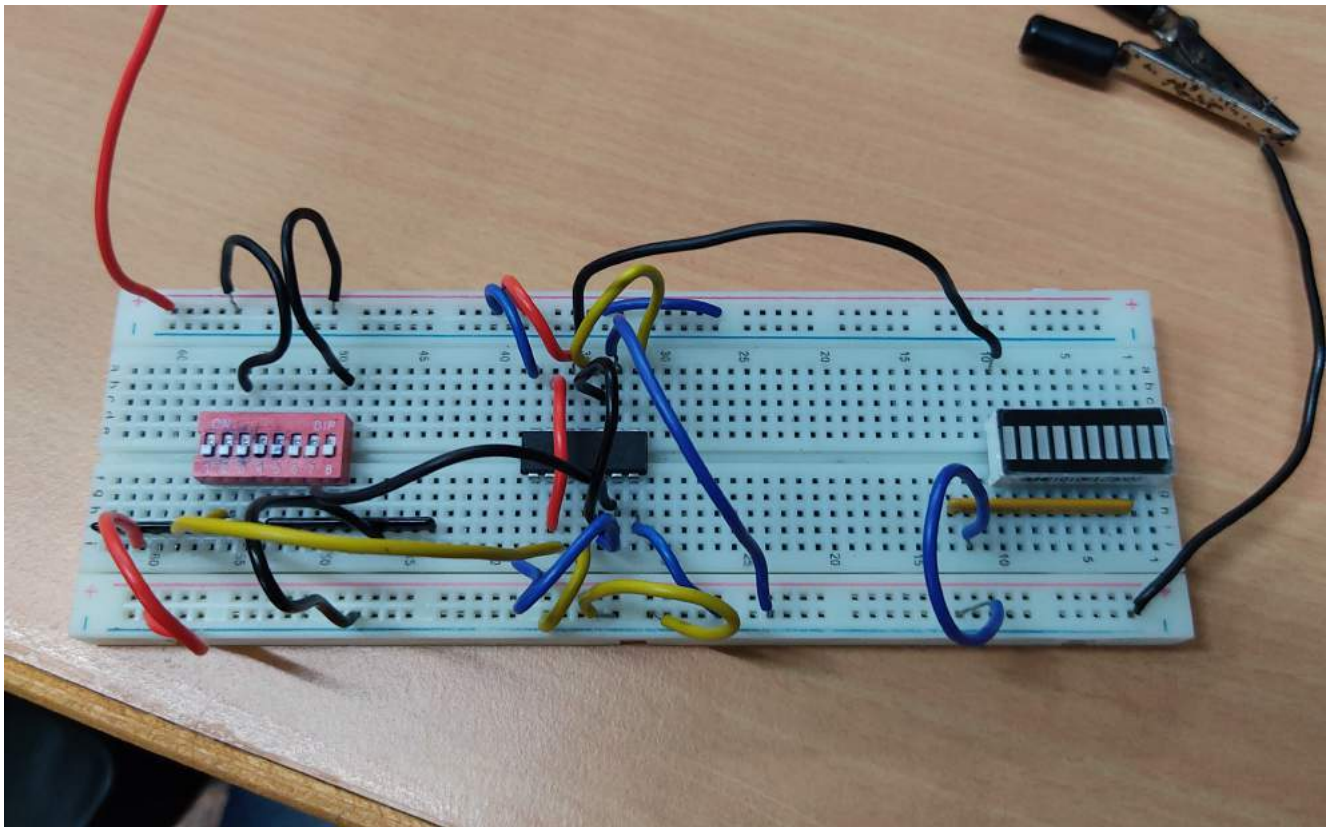
OR:



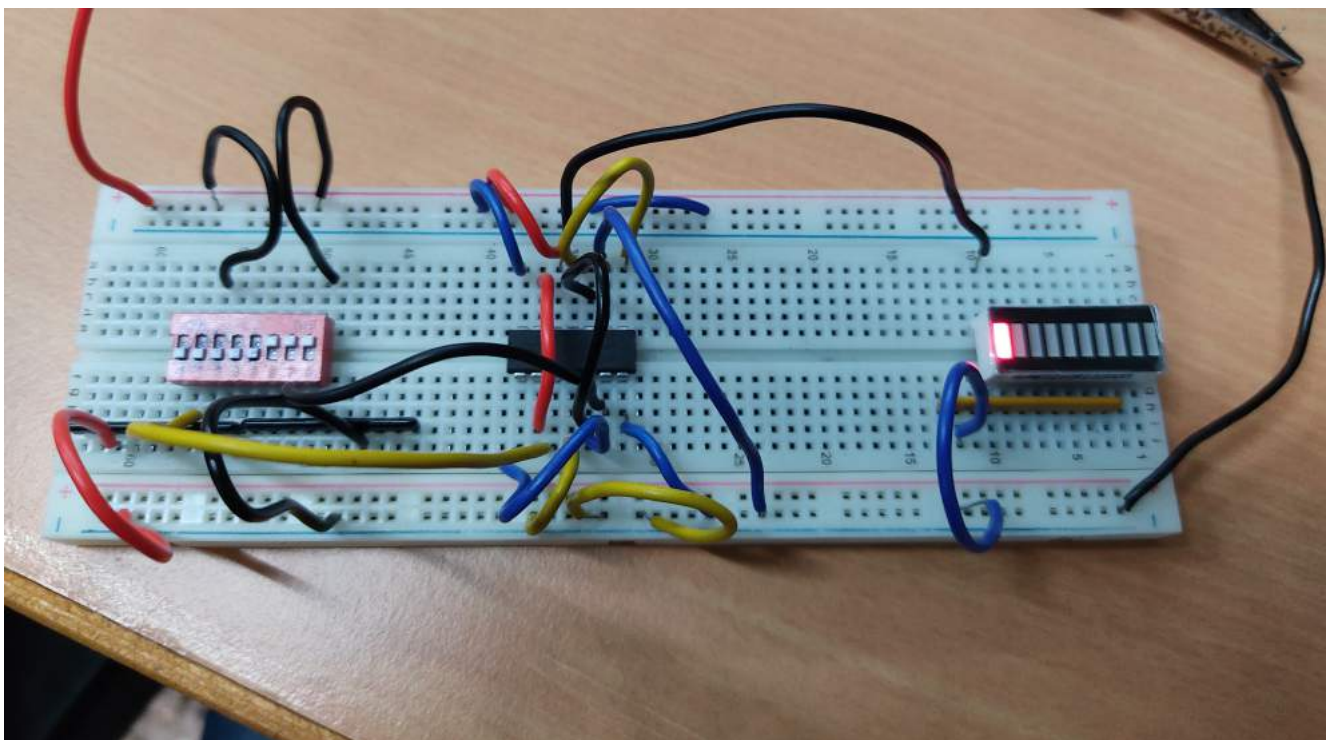
$1_0 \rightarrow 1$



$1_1 \rightarrow 1$

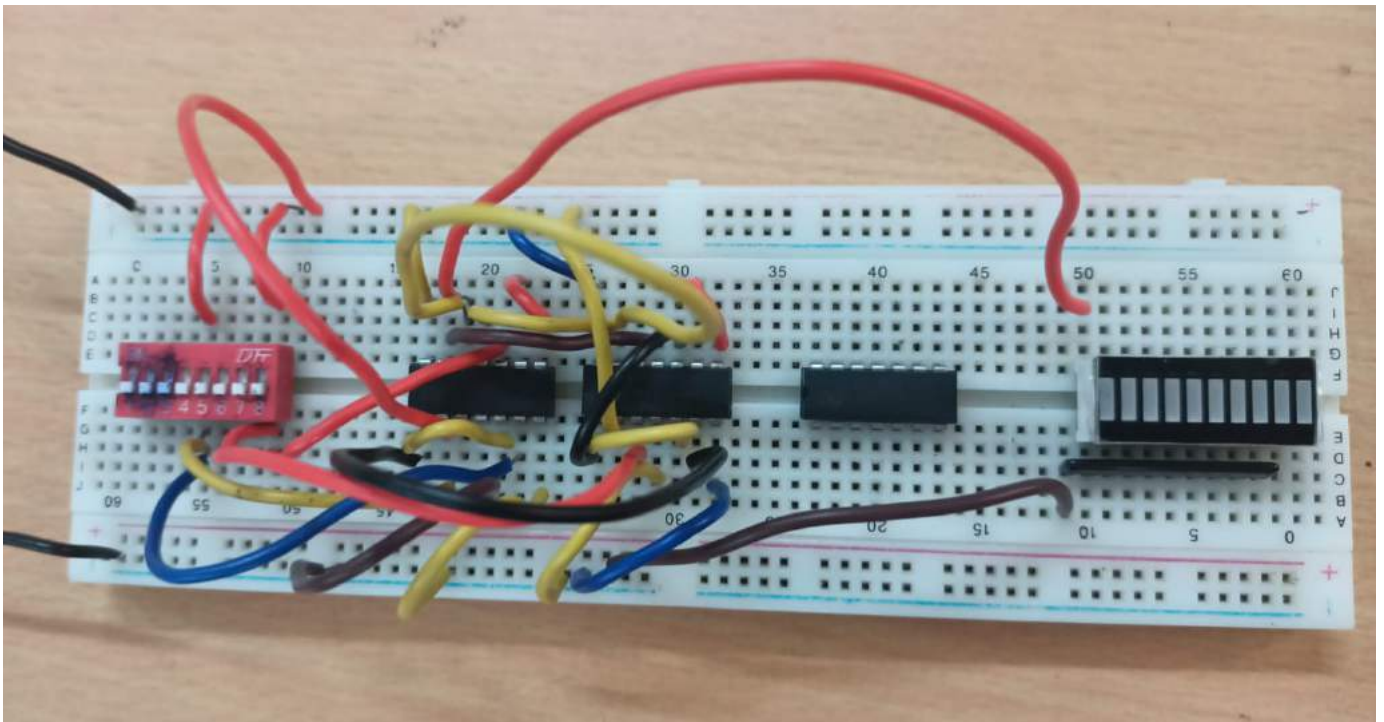


$0_0 \rightarrow 0$

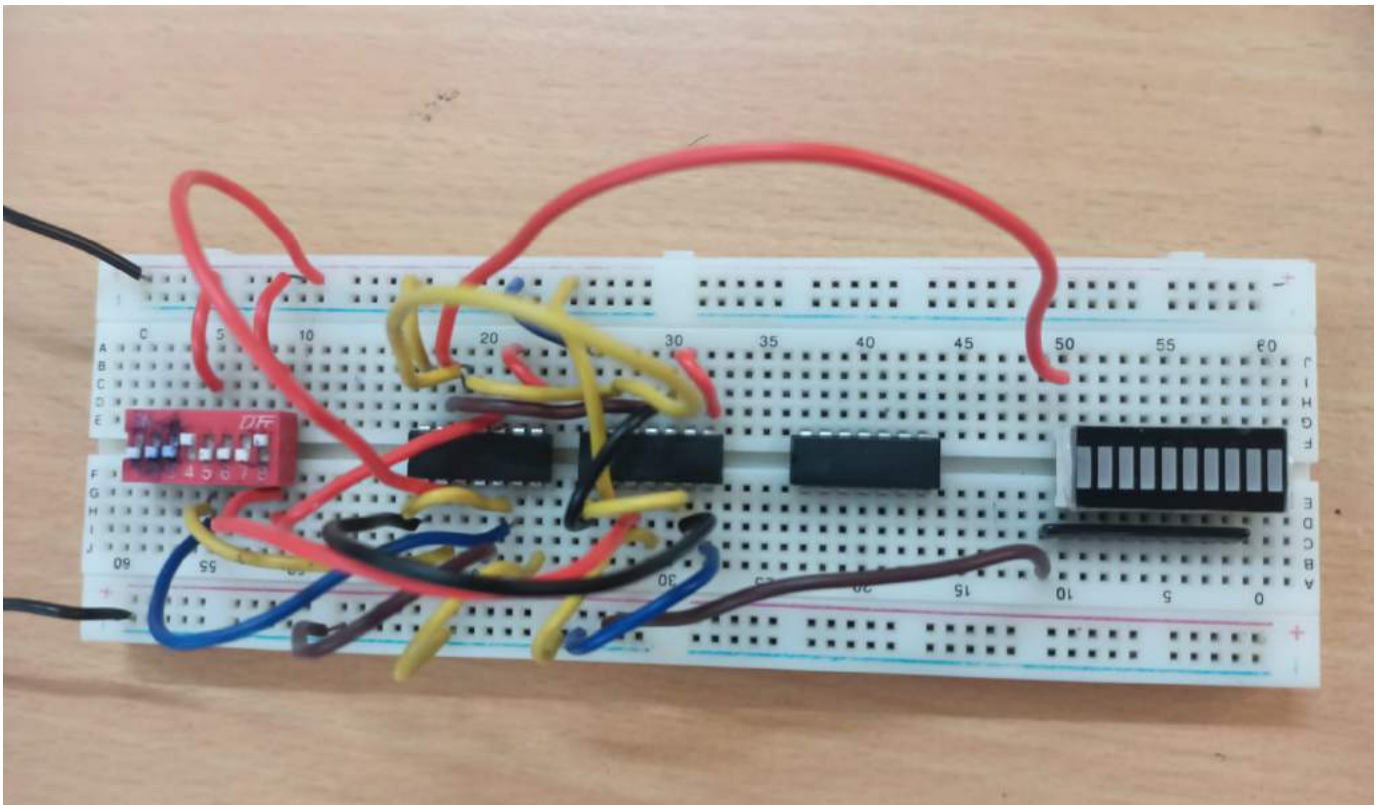


$0_1 \rightarrow 1$

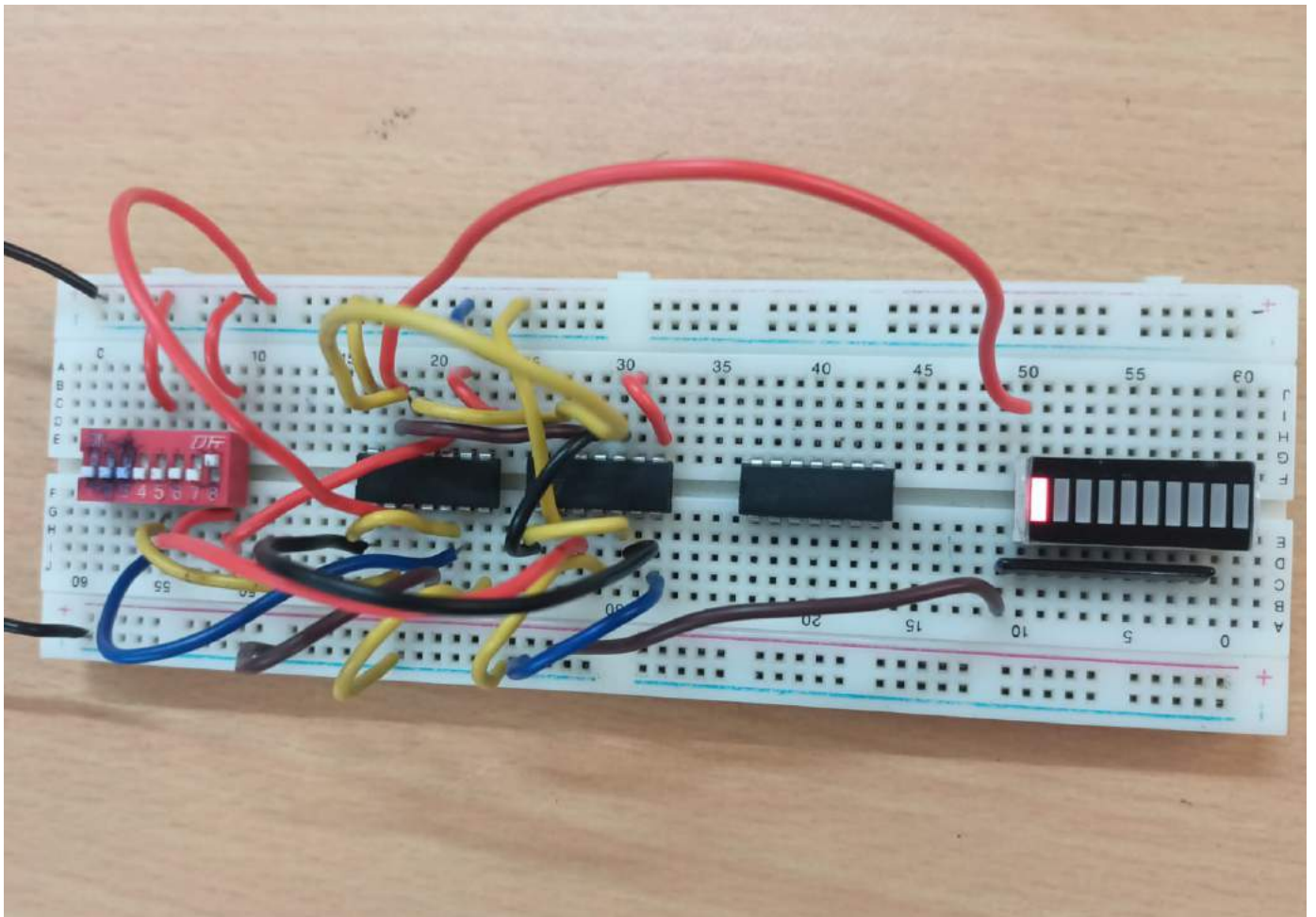
XOR:



$0_0 \rightarrow 0$

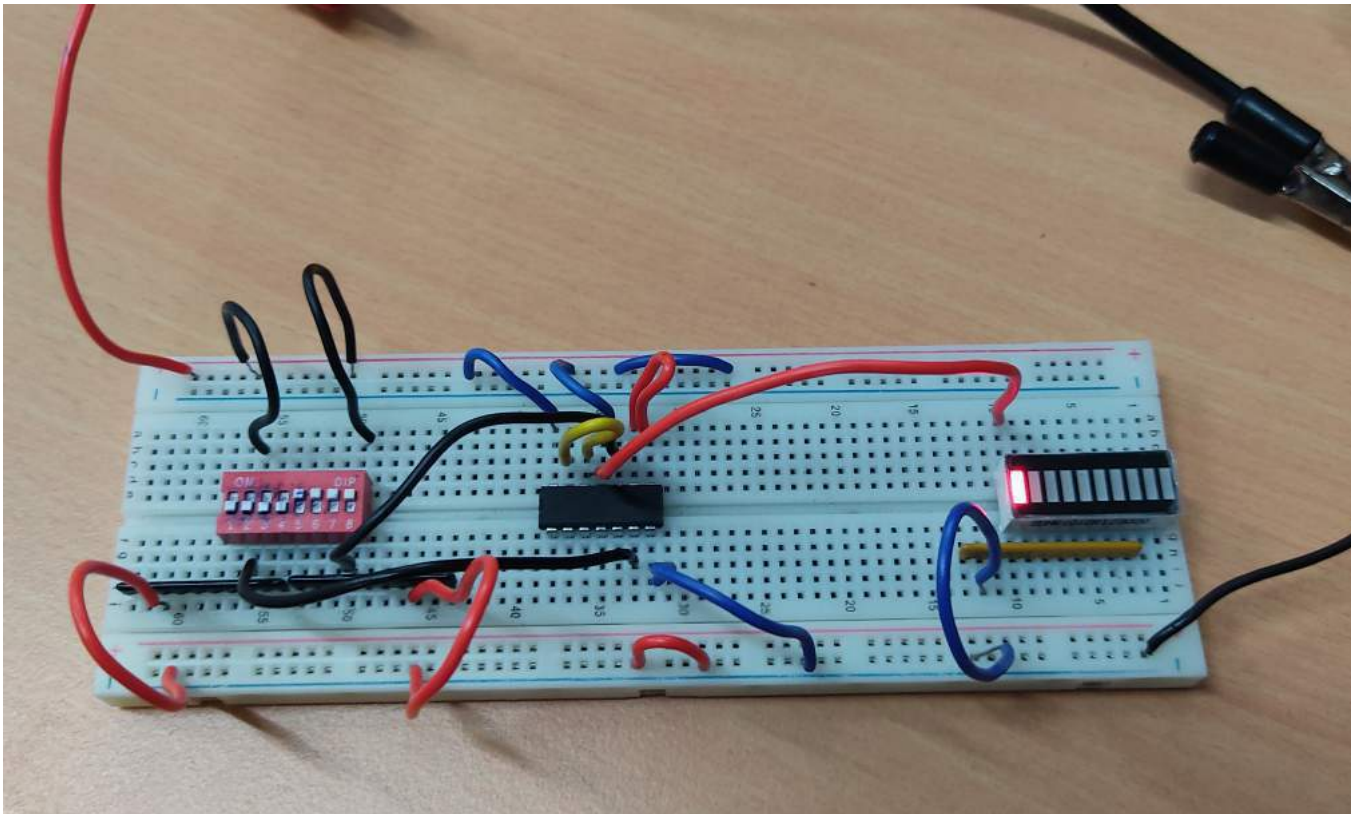


$1_1 \rightarrow 0$

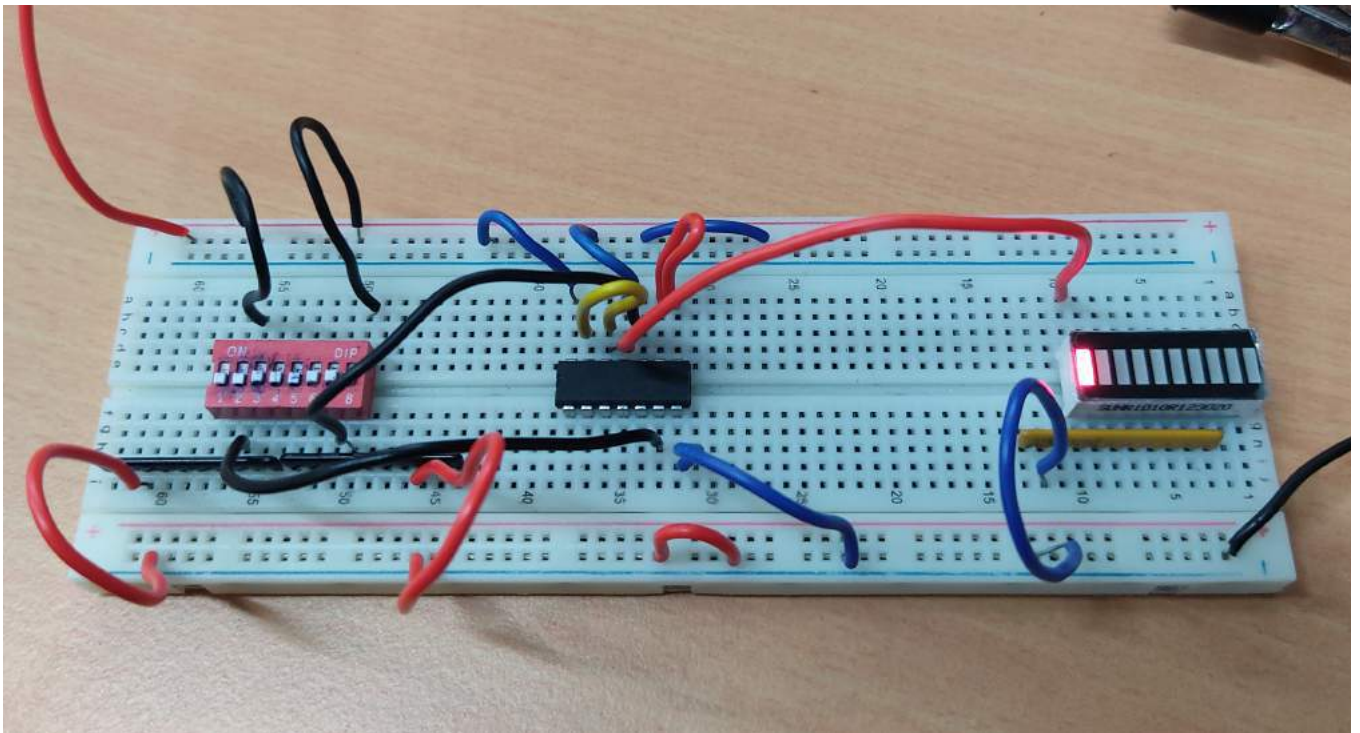


$0_1 \rightarrow 1$

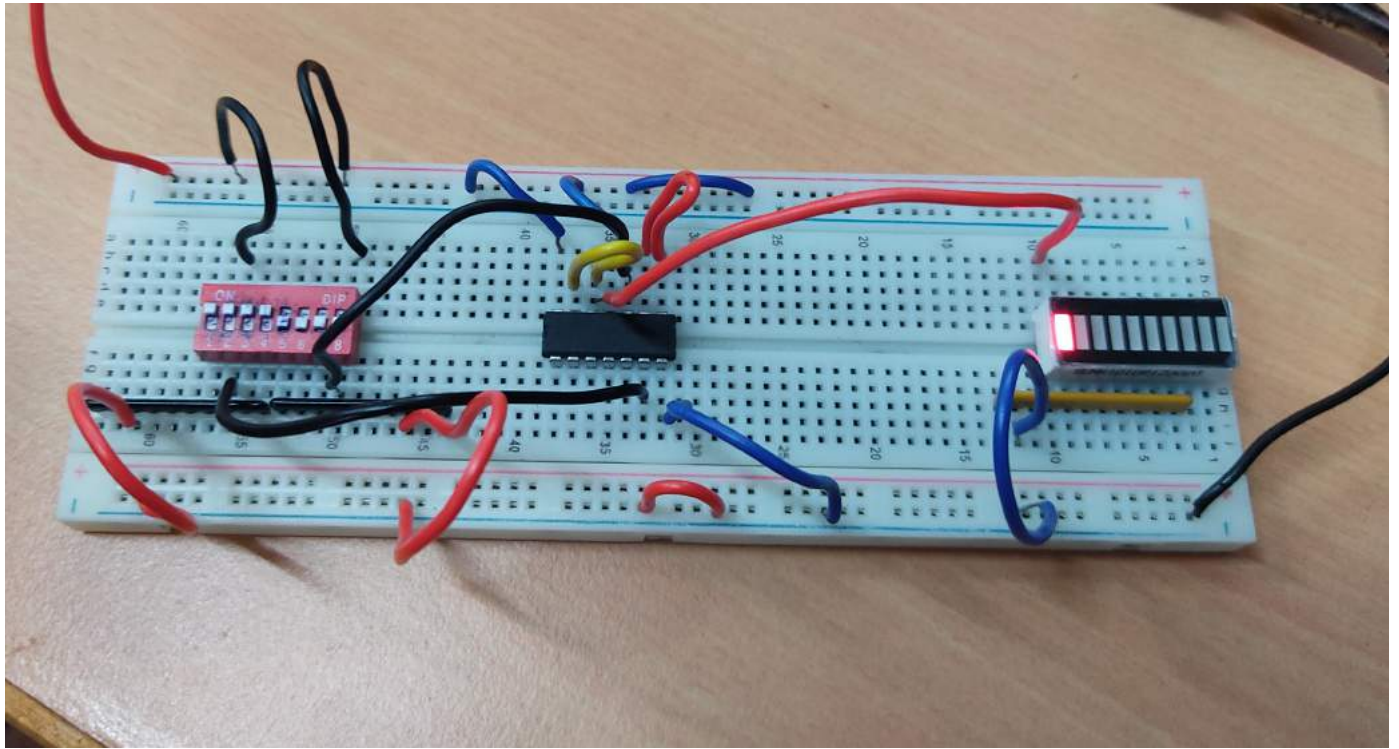
NAND:



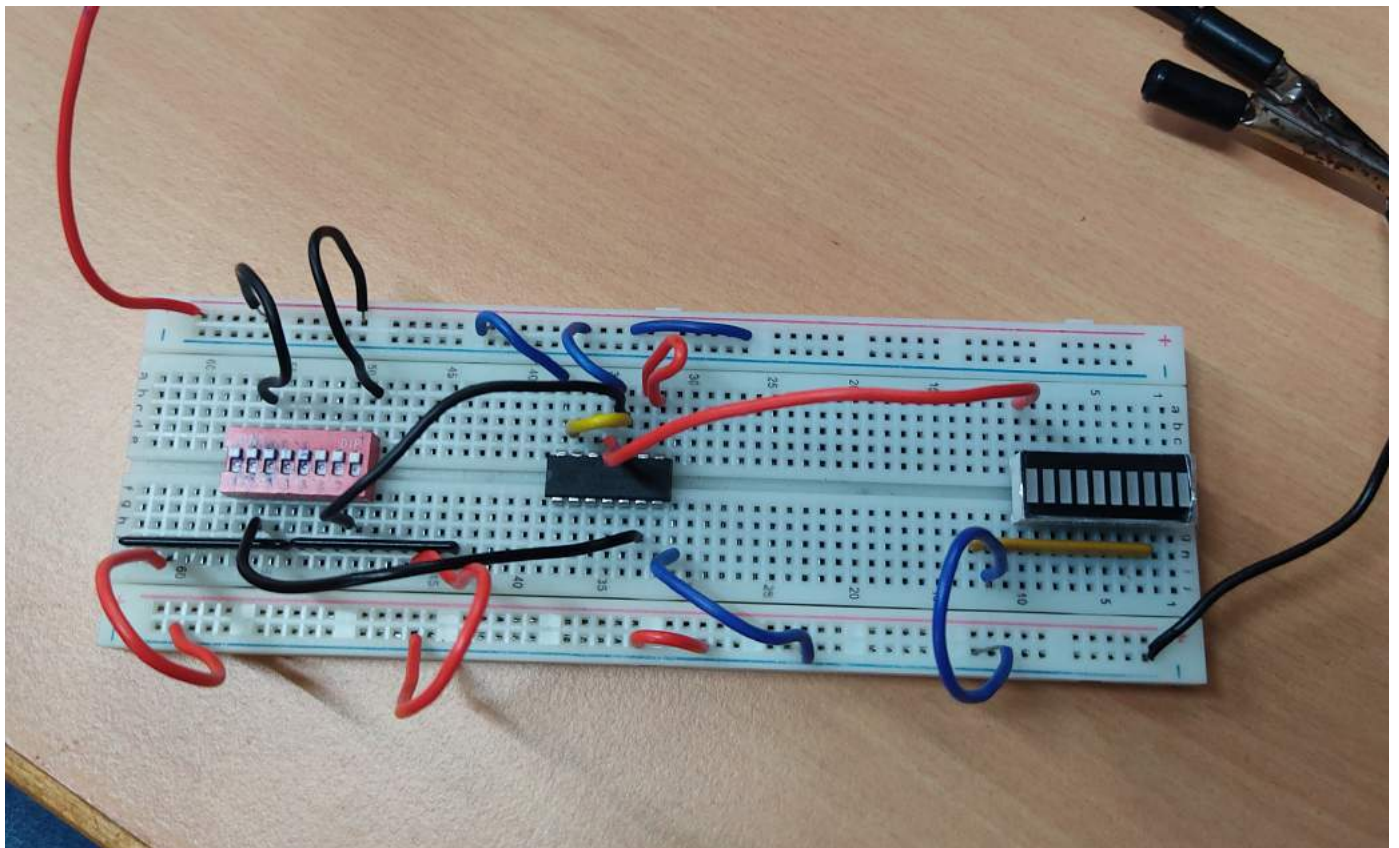
$0_1 \rightarrow 1$



$0_0 \rightarrow 1$

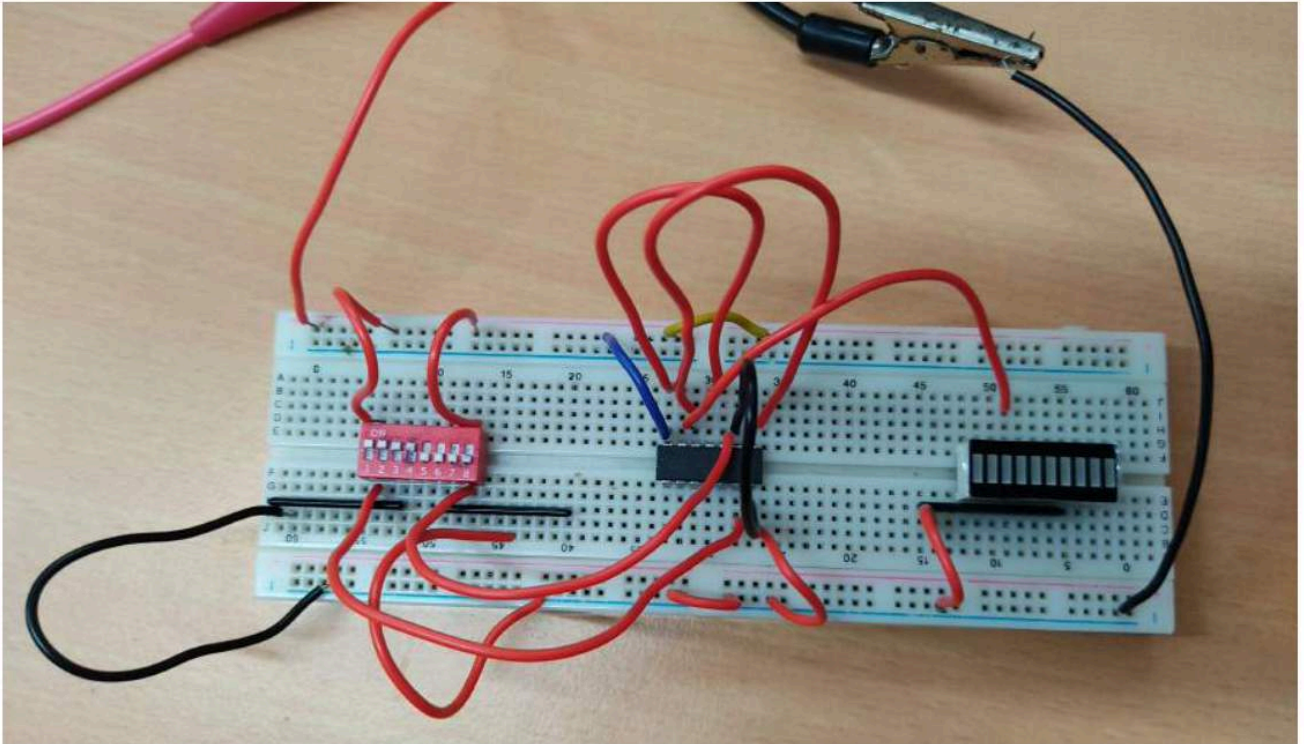
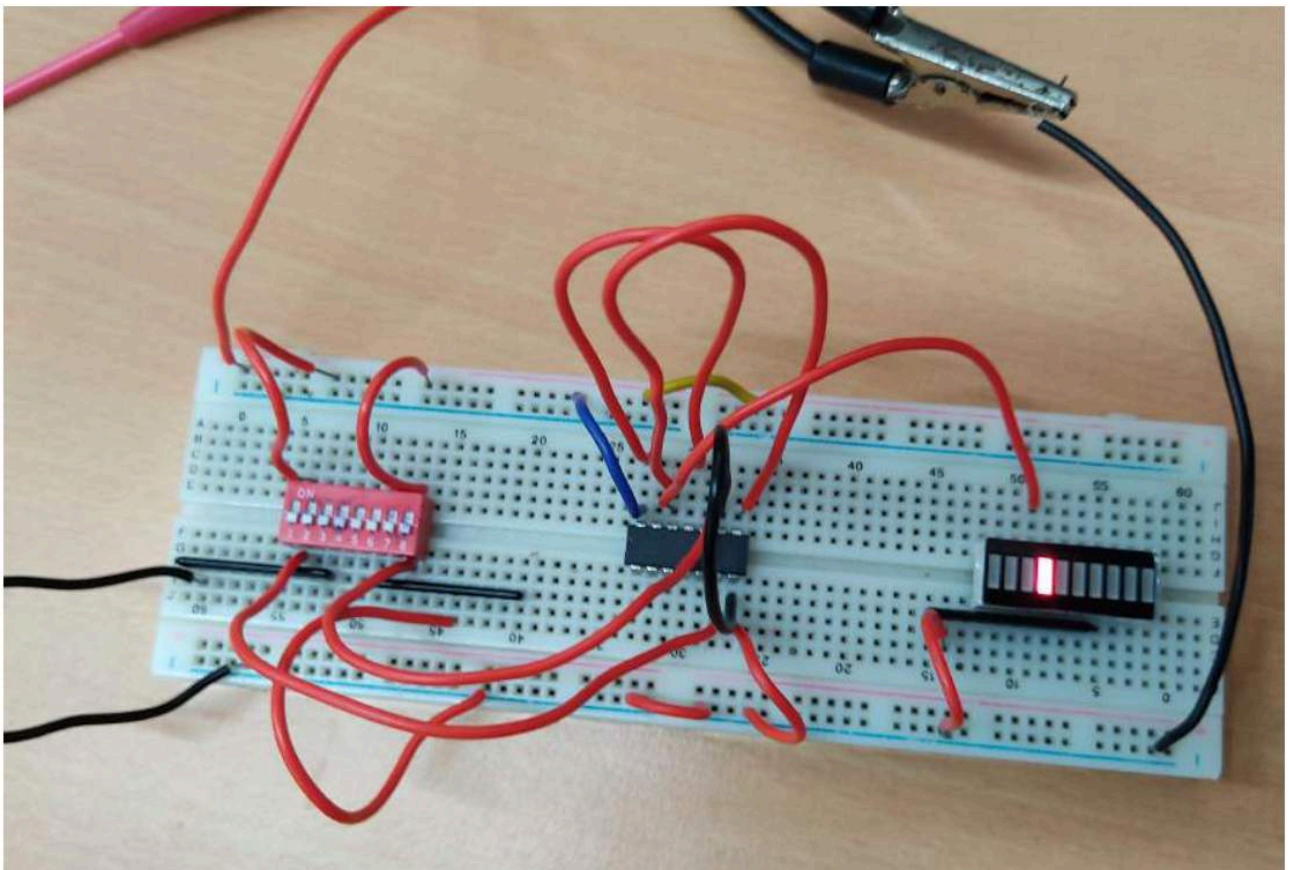


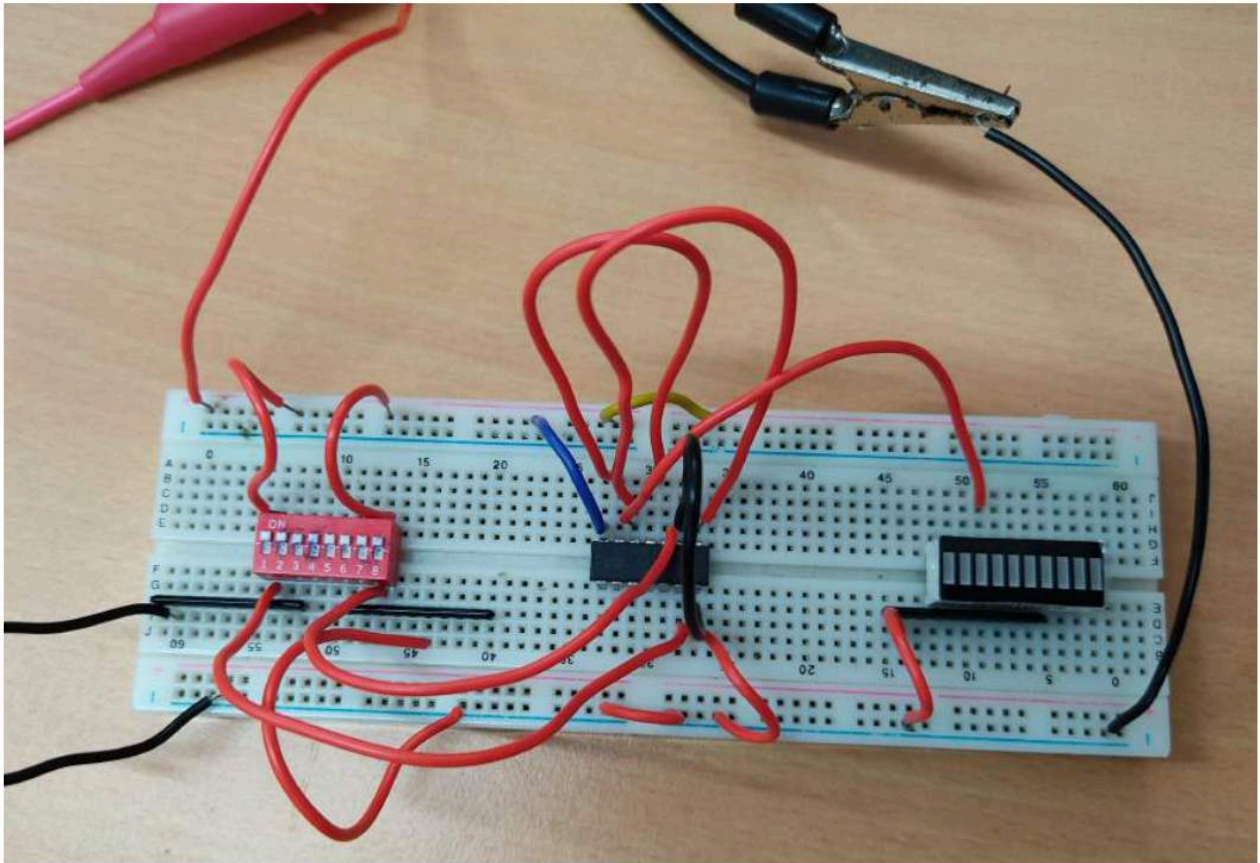
$1_0 \rightarrow 1$



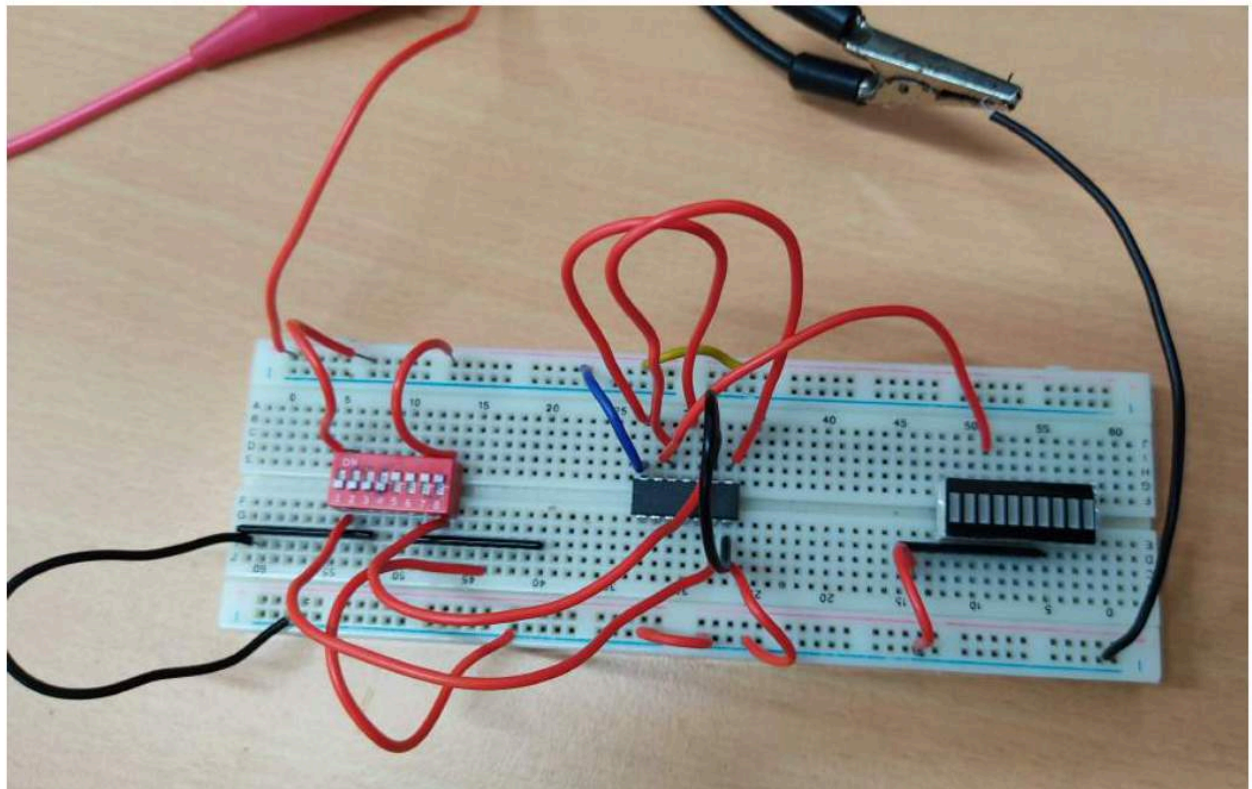
$1_1 \rightarrow 0$

NOR:


$$1_0 \rightarrow 0$$

$$0_0 \rightarrow 1$$

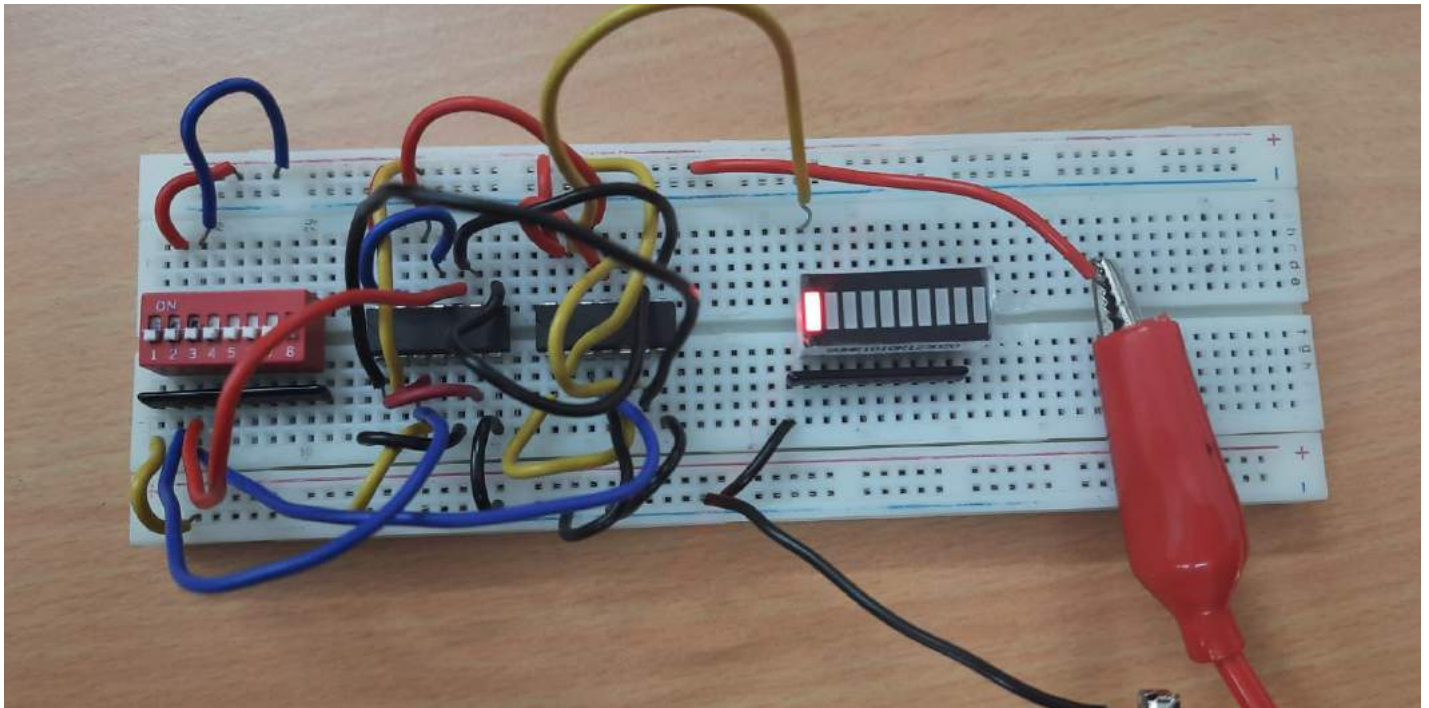


1_1 \rightarrow 0

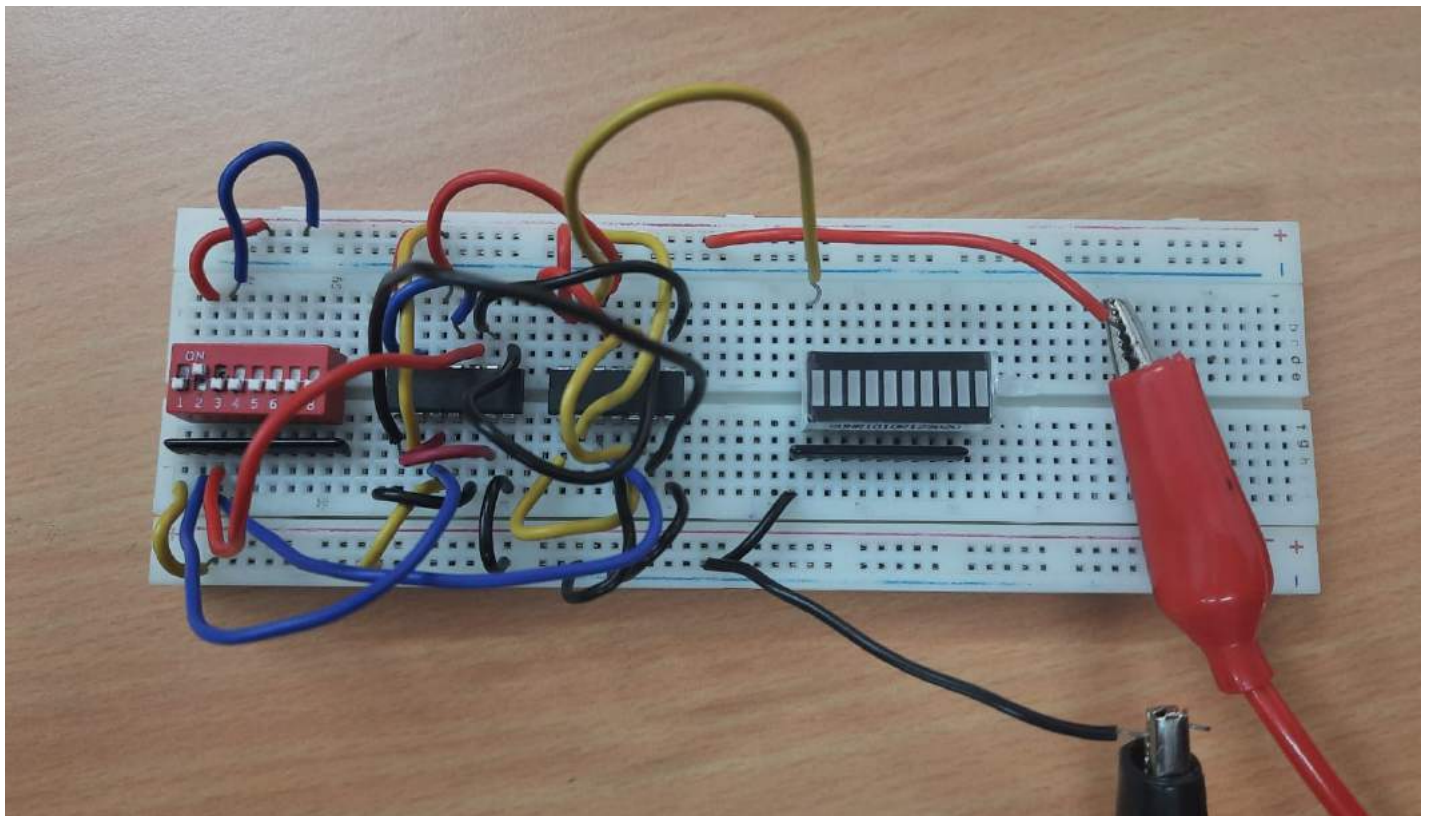


0_1 \rightarrow 0

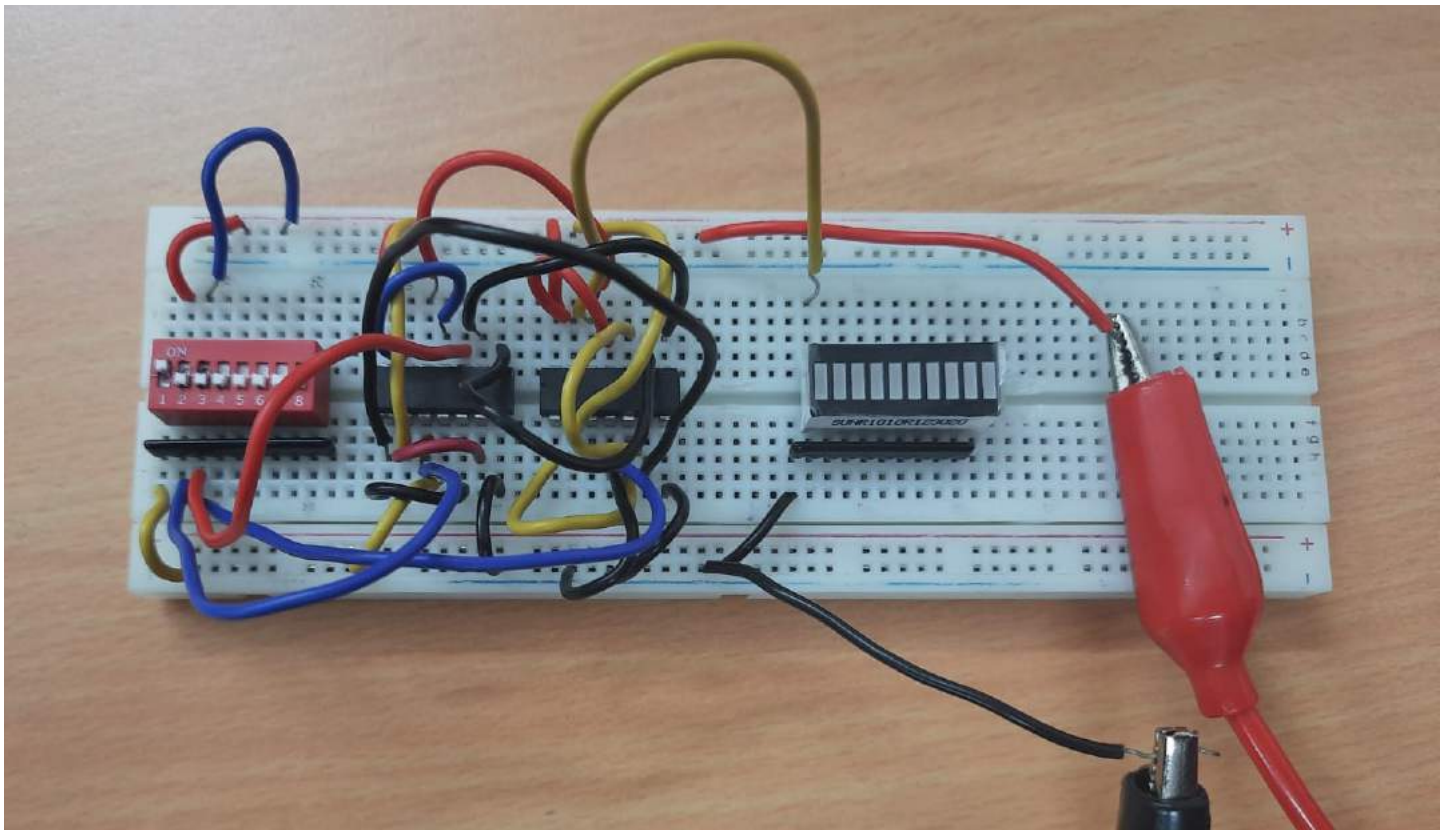
XNOR:



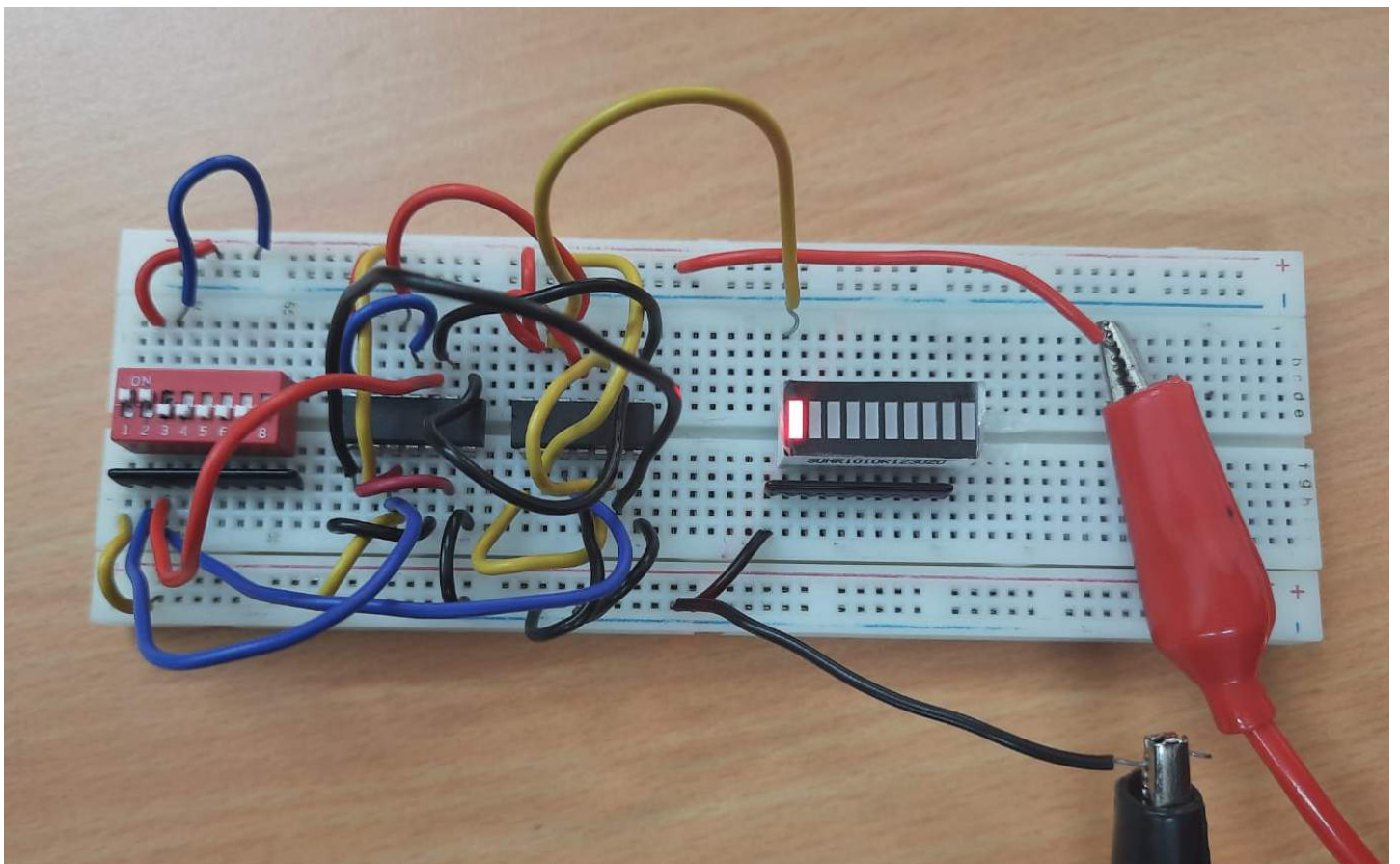
$0_0 \rightarrow 1$



$0_1 \rightarrow 0$



$1_0 \rightarrow 0$



$1_1 \rightarrow 1$