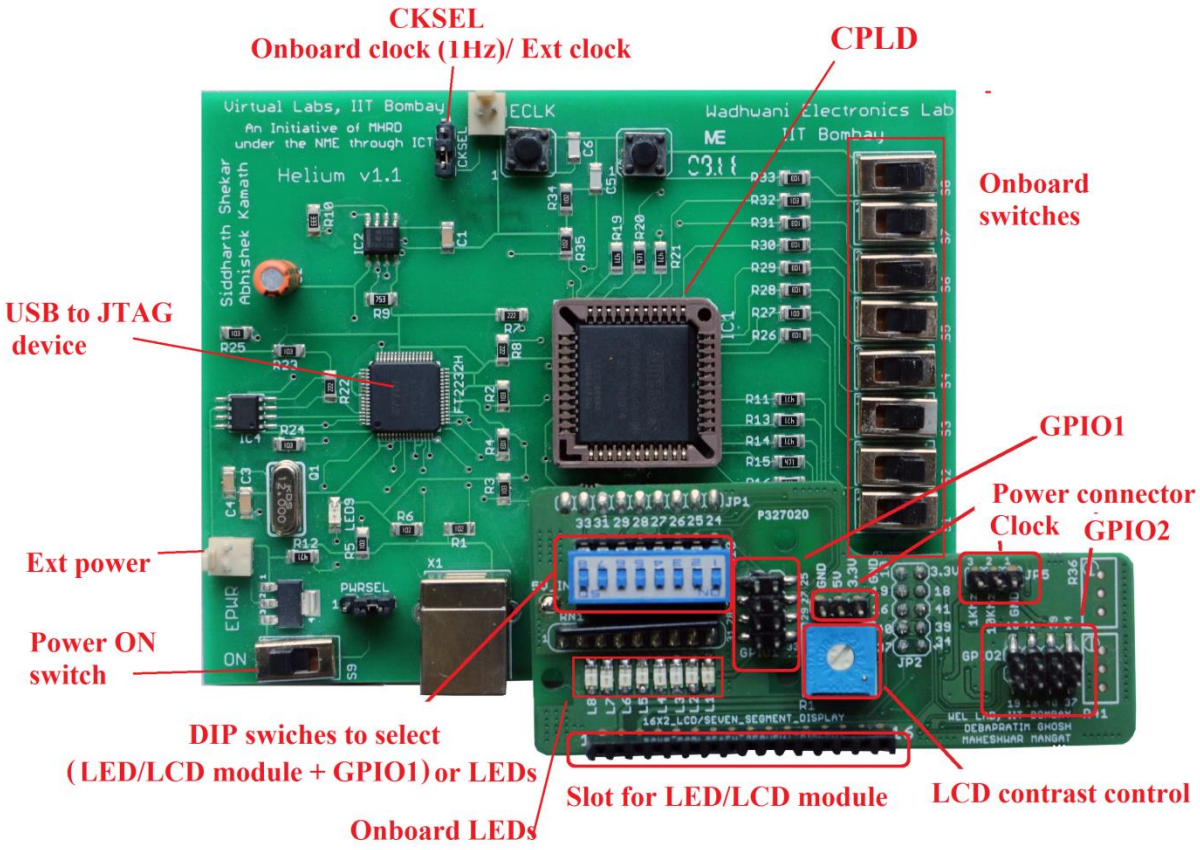
Helium v1.1

User manual Virtual Labs, IIT Bombay
(Wadhwani Electronics Lab)

Features:

- Based on Altera MAX 3000 architecture.
- Device used on board: EPM3064A (1250 usable gates).
- Powered and Programmed through USB.
- 8 inputs (switches) and 8 outputs(LEDs) onboard
- 8 user configurable GPIOs available onboard
- The 8 LEDs output pins can be made available as GPIO1 pins if the DIP switches are turned OFF.
- Onboard clock: 1Hz, 1kHz, and 10kHz available
- Provision for connecting external clock signal

Board details:



Note:

- *Do not touch any IC with your hands as they may be damaged due to electrostatic discharge.*

- *When using an external supply to power the board, use only a single regulated +5V DC supply.*

Main board settings:

Two jumpers need to be set on the board prior to setup.

1. PWRSEL: The power select jumper. It is located close to the USB connector on the board.

Pins	Mode
Pins 1 & 2	Externally powered
Pins 2 & 3	USB powered

The connector for the external supply can be found close to the to the PWRSEL jumper with the power polarities indicated. Use only +5V DC supply for external supply.

2. CKSEL: The clock select jumper. It is located close to the CPLD.

Pins	Mode
Pins 1 & 2	Onboard clock
Pins 2 & 3	External clock

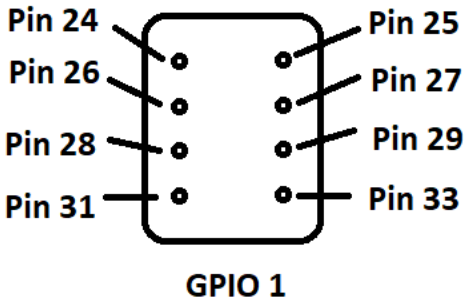
- The onboard clock frequency: 1Hz
- The connector for the external clock (ECLK) can be found close to the to the CKSEL jumper.
- You may connect the clocks from the daughter card (10 KHz & 1 KHz) to the ECLK pins.
- For using the above selected clocks, map your clock input to pin 43 of the CPLD which is the Global Clock of the CPLD.

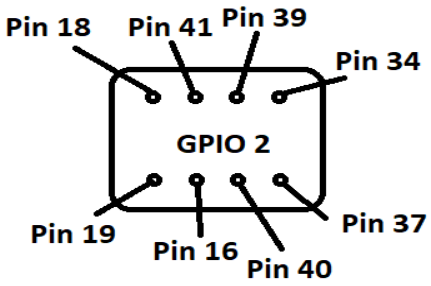
3. Input Configurations Pins

Inputs	Pin No.
SW1	4
SW2	5
SW3	6
SW4	8
SW5	9
SW6	11
SW7	12
SW8	14

Daughter card settings:

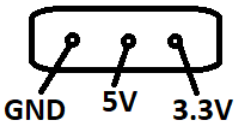
1. GPIO Pins



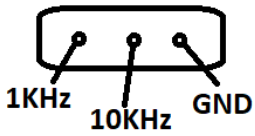


It is recommended to use external power supply of +5V when interfacing external hardware to the board.

2. Power supply



3. Clock Pins



Note: In case of any setup or hold violations in using the on-board clock, pass the clock through a Schmitt trigger before connecting to the CPLD pins.

4. Output Configurations Pins

The CPLD pins are hardwired to the LCD and GPIO pins. For the pins to the used for LED output, the DIP switches on-board should be switched ON. For eg, for LED 1 to be used as an output, the switch above that should be turned ON;if LED 1 and 2 are to be used as output, both of the corresponding switches should be turned ON.

The pins which have been configured as output to LEDs on the board are as follows:

Outputs	Pin No.
LED1	24
LED 2	25
LED 3	26
LED 4	27
LED 5	28
LED 6	29
LED 7	31
LED 8	33

Brief steps for Using Altera Quartus:

1. Create a new project from File >> New Project Wizard.
2. The project name and the top level design entity should have the same name.
3. Follow the onscreen instructions to create a new project. An existing VHDL/ Verilog file can be added to the project if a program file has been already written or else, it may be left blank if you wish to create a new VHDL/ Verilog file in the current project directory.
4. Select the programmable device family as MAX3000A, and EPM3064ALC44-10N from the device list that shows up.
5. Open a new VHDL/ Verilog file and write the program, in case a new file is to be complied.
6. Compile the design and rectify errors, if any.
7. Once the design is compiled, you can choose what pins to assign as input/output from “Pin Planner” under the Assignments tab in the Menu bar. Refer to the last section for the I/O pin configuration.
8. Re-run the compiler and make sure that there are no errors.
9. To generate the ‘.svf’ file, select ‘Programmer’ under the Tools tab in the Menu bar. Check if the device EPM3064ALC44-10N is recognized in the programmer window.
10. Select the file type as ‘.svf’ and click ‘Generate’.

For further details refer manual.

Brief steps for programming the CPLD:

1. Open the JTAG shell in the UrJTAG folder.
2. At the command prompt, type “cable ft2232 vid=0x0403 pid=0x6010”.
3. You will get a message saying “connected to libd2xx”.
4. The “detect” command should identify the CPLD device and display its signature.
5. In case you have other devices connected to the JTAG chain, you can choose the appropriate device by specifying the corresponding part number. This is optional in this case, as only one

device is present in the JTAG chain. Since the CPLD is the only device in the JTAG chain, you can select it by typing the “part 0” command.

6. Type “svf <svf file location> progress” on the command prompt. The file will now be loaded, and the output of the VHDL/ Verilog program may be observed on the board.