

Experiment - 1

Aim: Study of Digital ICs and basic concept components like power supply, DSO etc.

Summary:

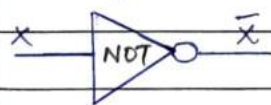
Study of basic digital ICs and verifying their functionality, learning the usage of function generator (FG) and digital storage oscilloscope (DSO), and rigging up of circuits

Components used:

IC 7404, 7408, 7432, 7486, 1k $\Omega$  resistor array, DIP switches, learning usage of function generator breadboard, power supply

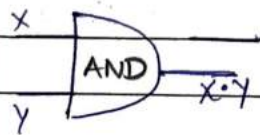
Design Procedure:

→ NOT gate:



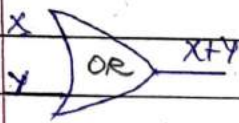
X	$\bar{X}$ = NOT X
0	1
1	0

→ AND gate:



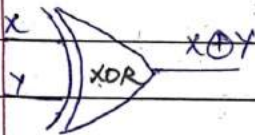
X	Y	$X \cdot Y$ = X AND Y
0	0	0
0	1	0
1	0	0
1	1	1

→ OR gate:



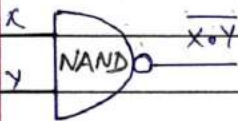
X	Y	$X+Y = X \text{ OR } Y$
0	0	0
0	1	1
1	0	1
1	1	1

→ XOR gate:



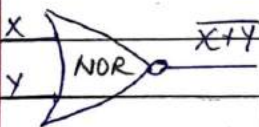
X	Y	$X \oplus Y = X \text{ XOR } Y$
0	0	0
0	1	1
1	0	1
1	1	0

→ NAND gate:



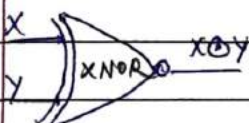
X	Y	$\overline{X \cdot Y} = X \text{ NAND } Y$
0	0	1
0	1	1
1	0	1
1	1	0

→ NOR gate:



X	Y	$\overline{X+Y} = X \text{ NOR } Y$
0	0	1
0	1	0
1	0	0
1	1	0

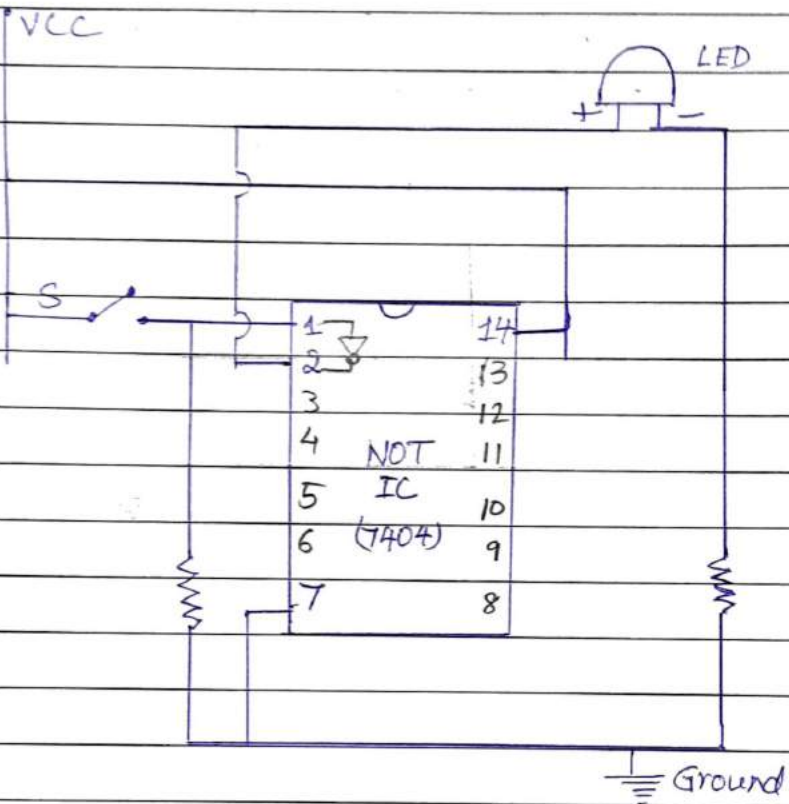
→ XNOR gate:



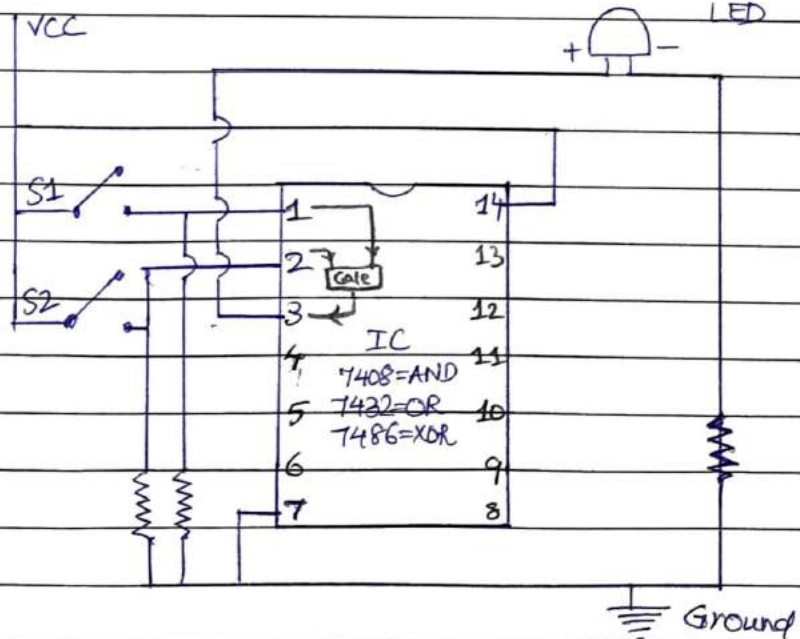
X	Y	$X \odot Y = X \text{ XNOR } Y$
0	0	1
0	1	0
1	0	0
1	1	1

Circuit Diagrams.

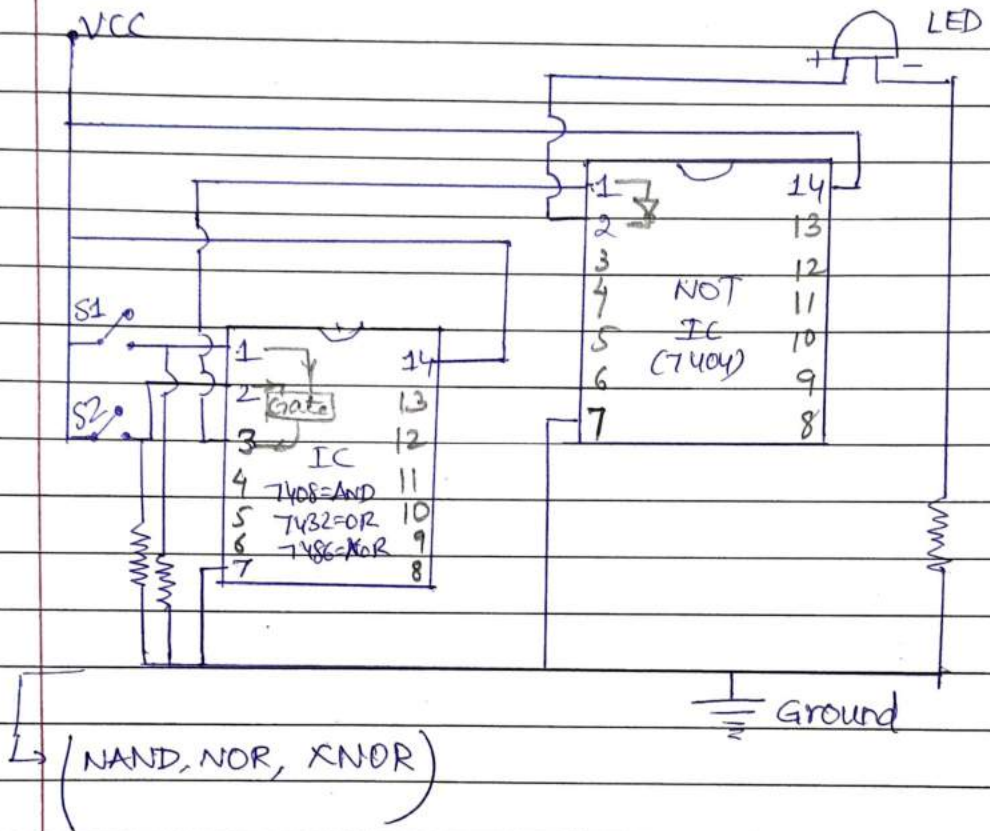
→ NOT.



→ (AND, OR, XOR)







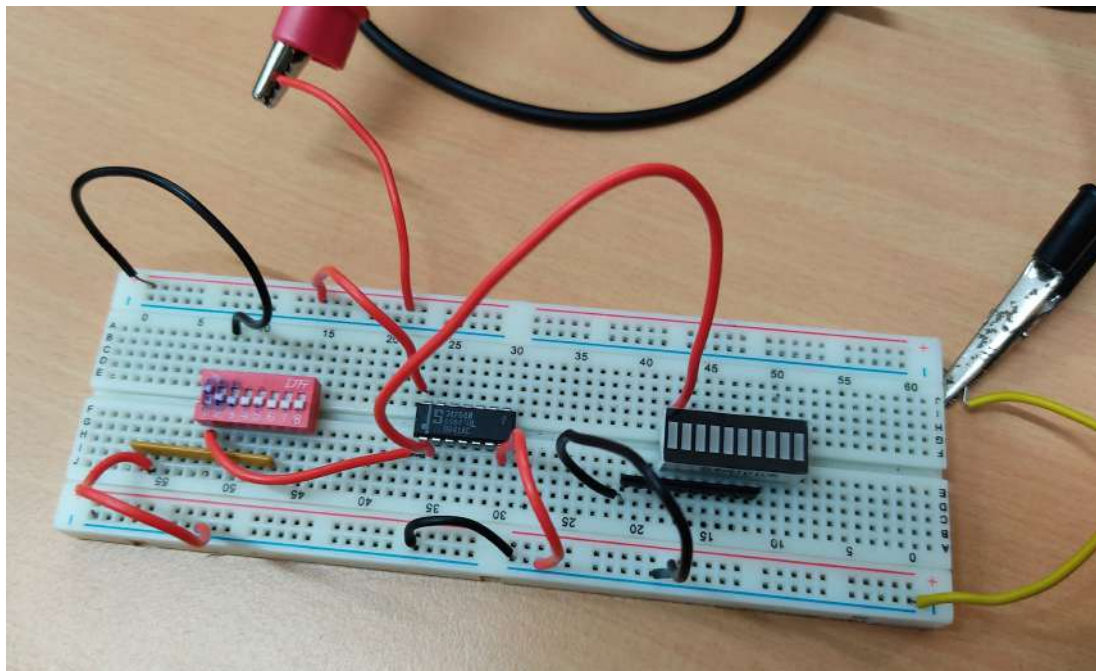
### Results and Discussions.

1. We can verify the outputs obtained using truth tables.
2. We have constructed complex logic gates (NAND, NOR, XNOR) using the more basic logic gates (NOT, AND, OR, XOR)

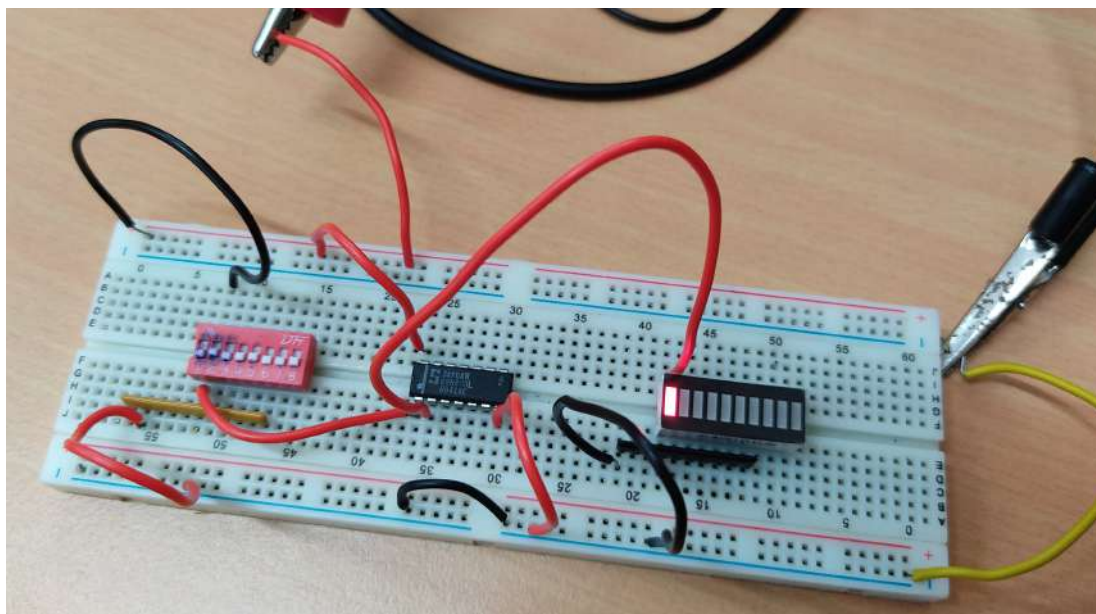
### Conclusion

→ We have verified functionality of basic digital integrated circuits (ICs)

**NOT:**

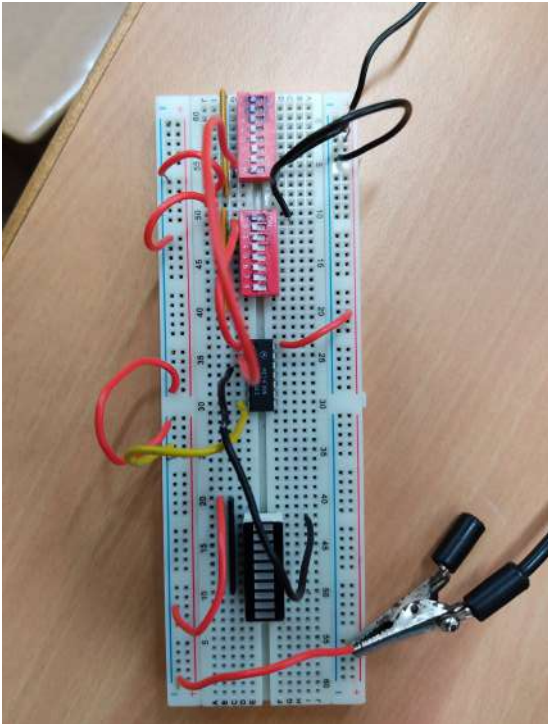


1  $\rightarrow$  0

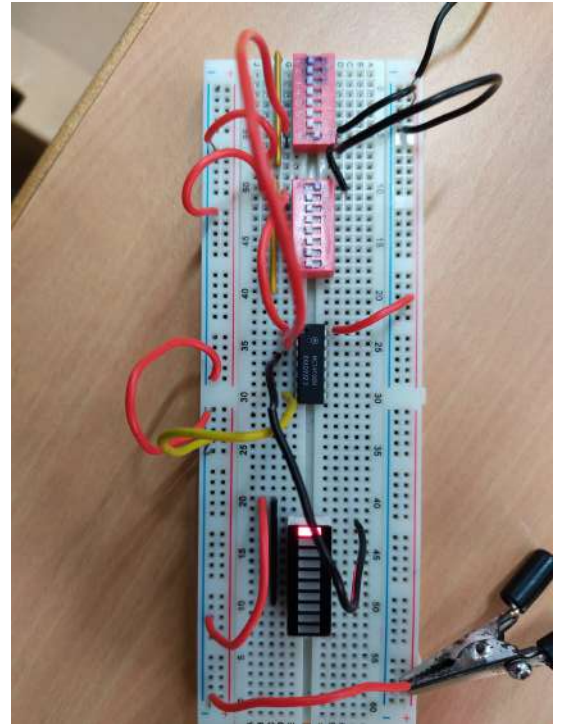


0  $\rightarrow$  1

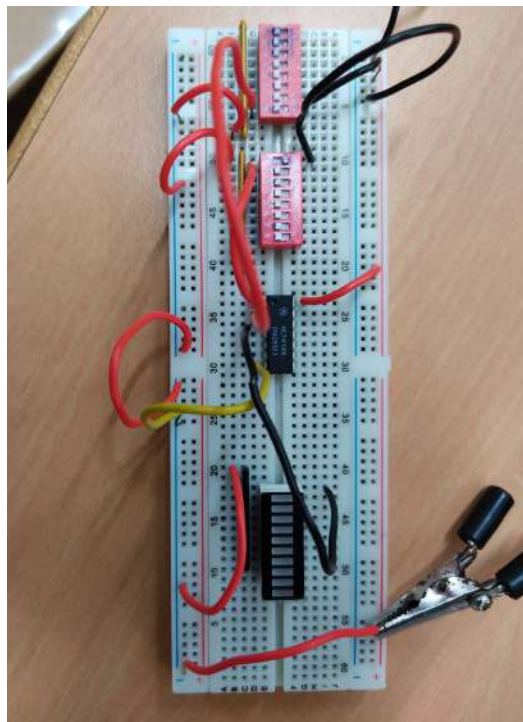
**AND:**



$0_0 \rightarrow 0$



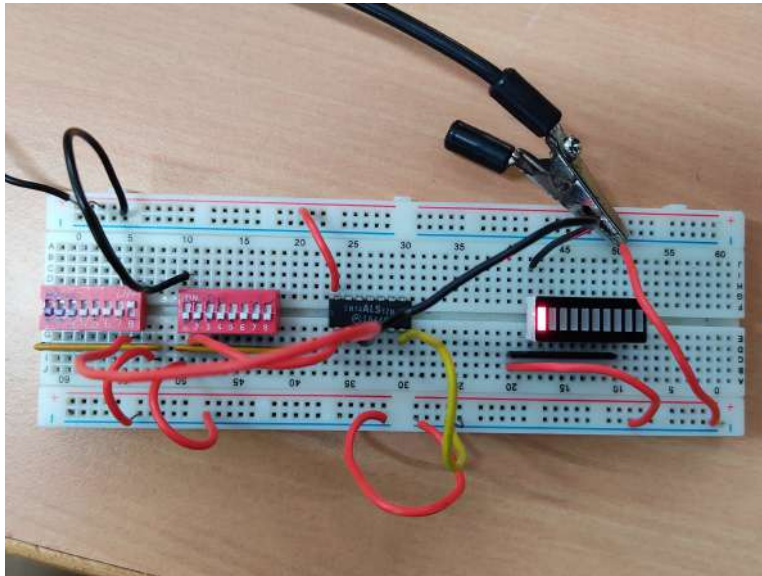
$1_1 \rightarrow 1$



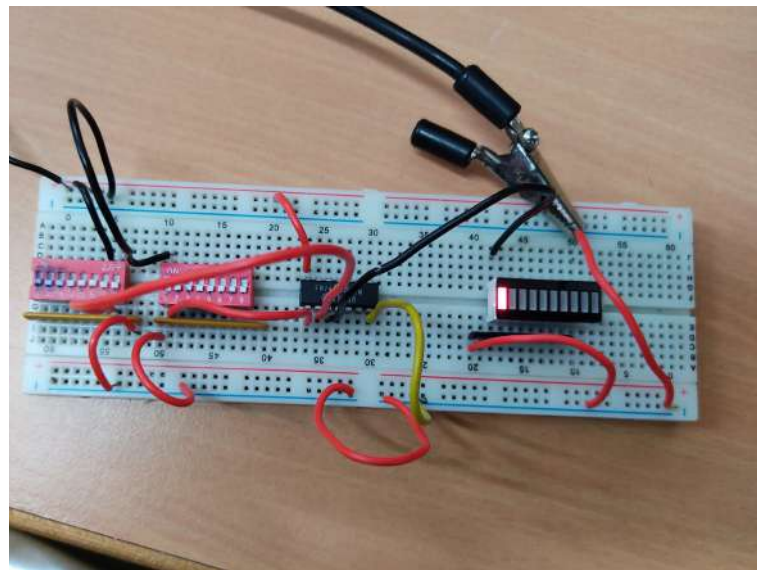
$1_0 \rightarrow 0$



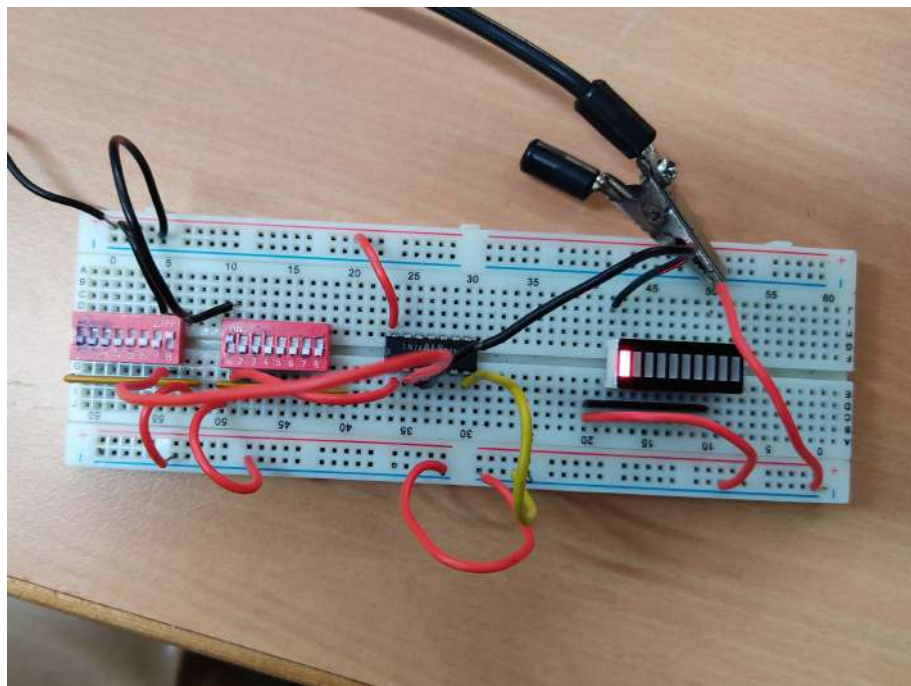
OR:



1\_0  $\rightarrow$  1

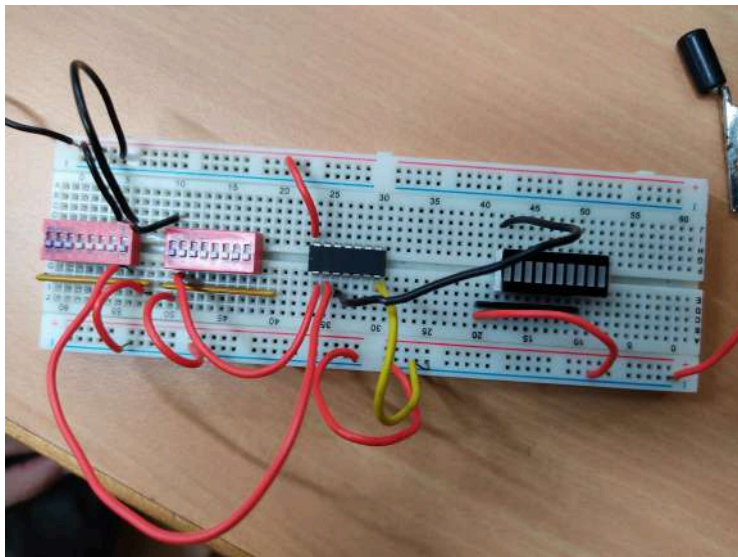


0\_1  $\rightarrow$  1

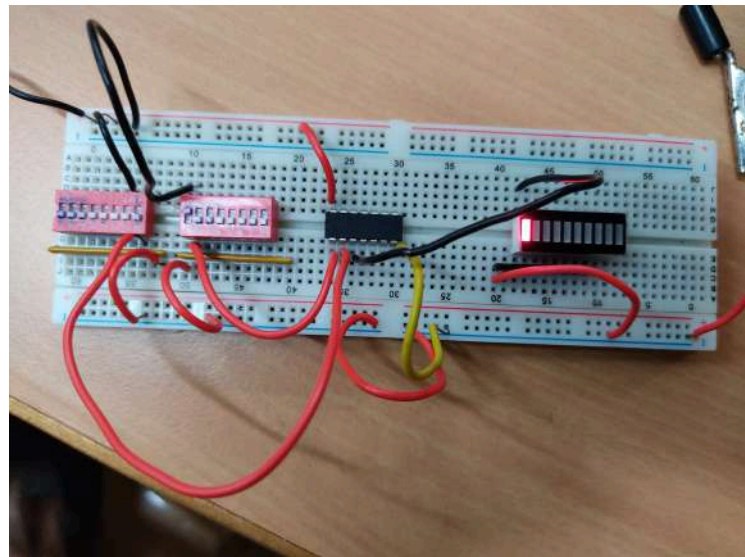


1\_1  $\rightarrow$  1

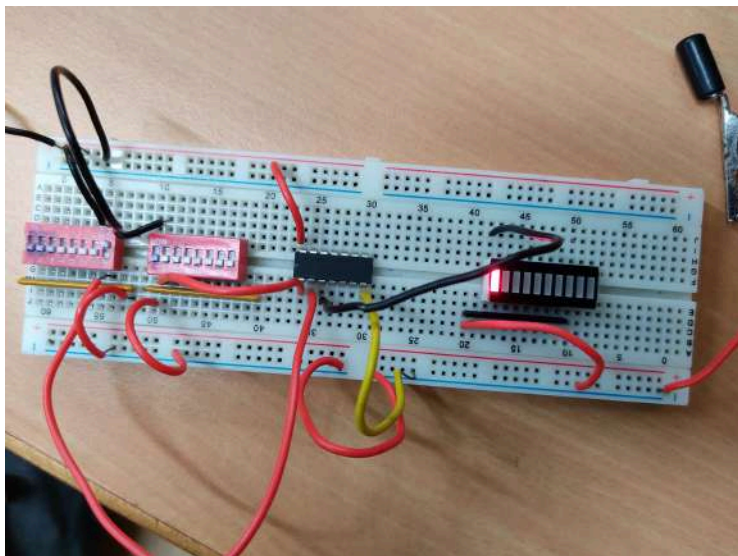
# XOR:



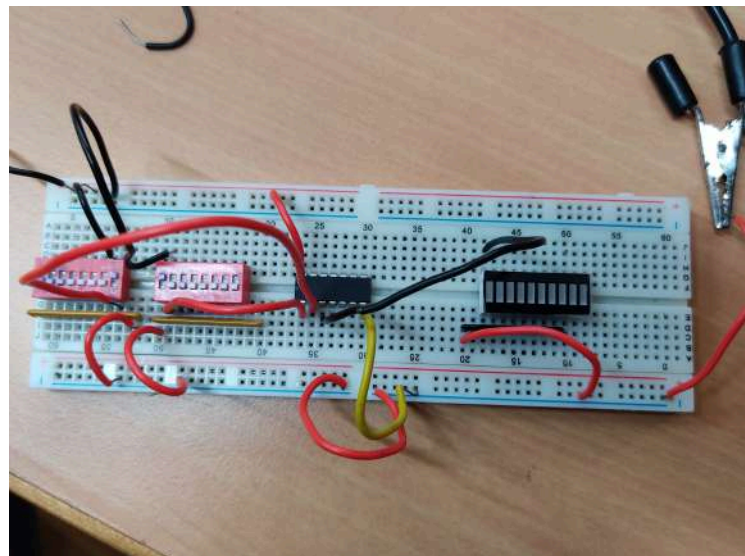
$0_0 \rightarrow 0$



$0_1 \rightarrow 1$



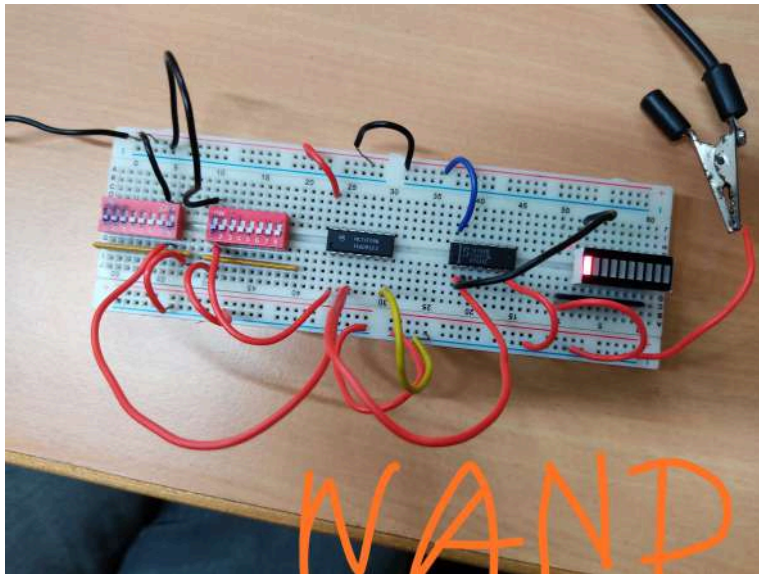
$1_0 \rightarrow 1$



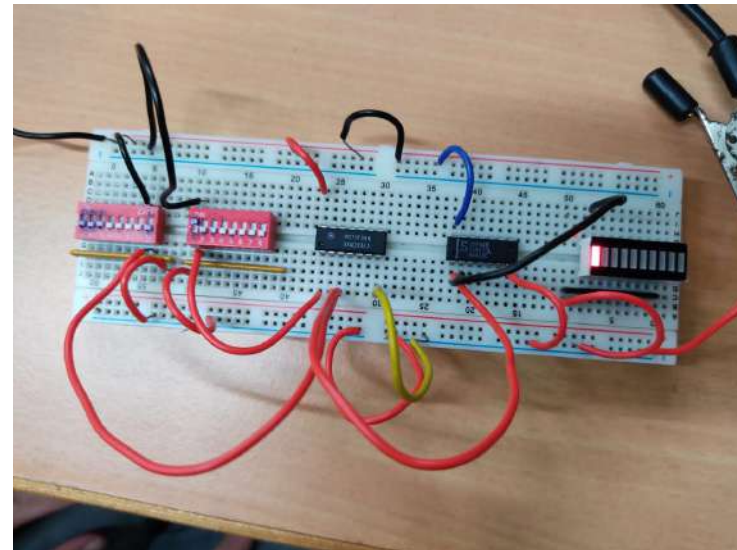
$1_1 \rightarrow 0$



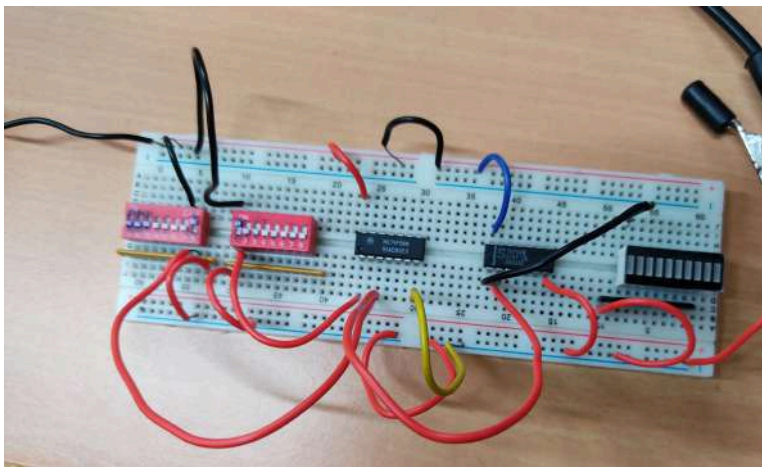
# NAND:



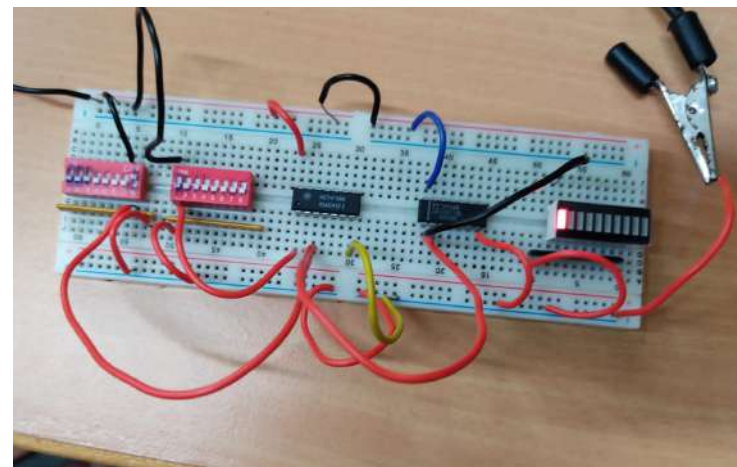
$0_0 \rightarrow 1$



$0_1 \rightarrow 1$

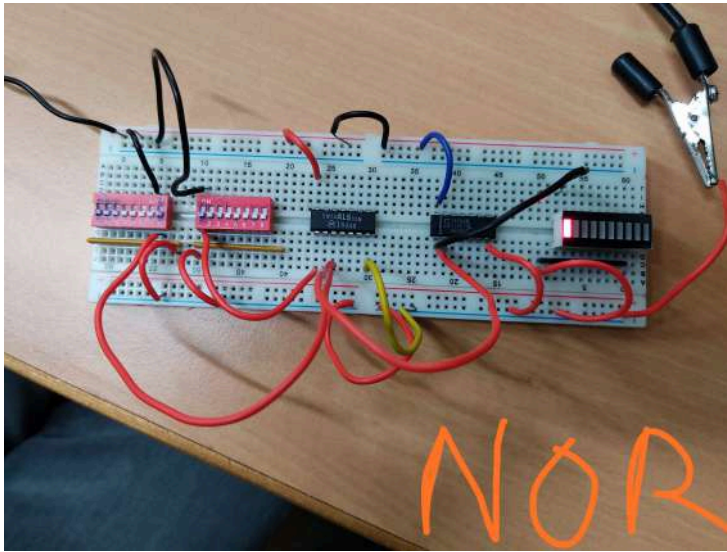


$1_1 \rightarrow 0$

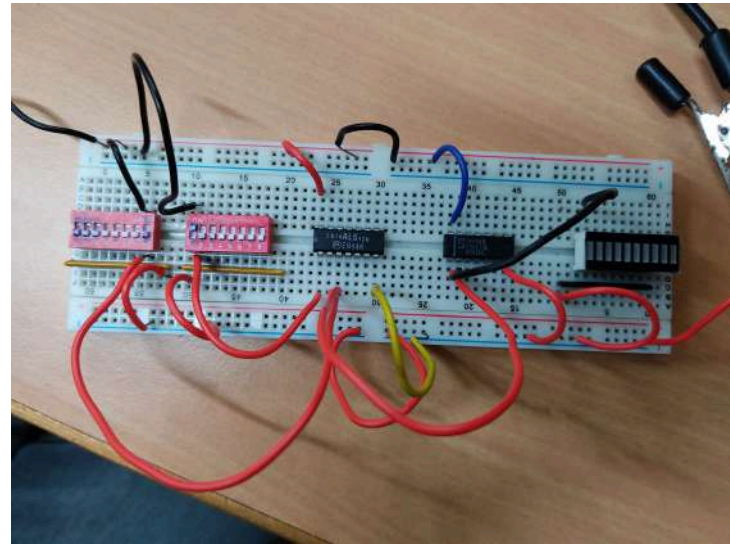


$1_0 \rightarrow 1$

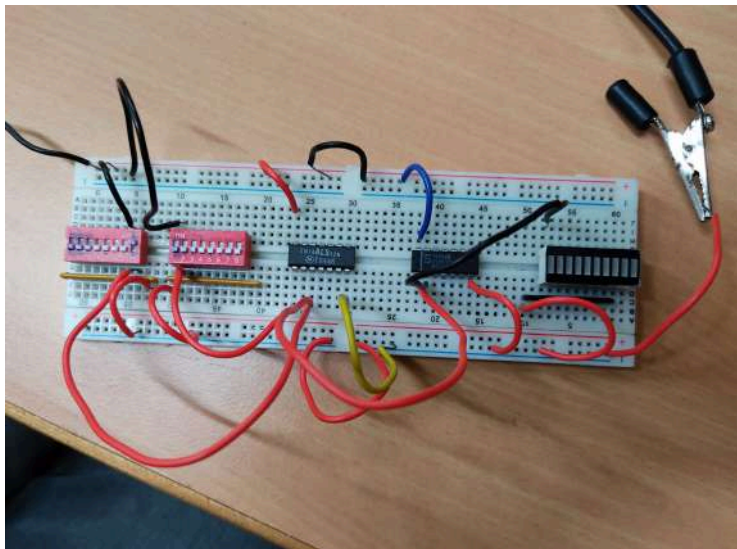
# NOR:



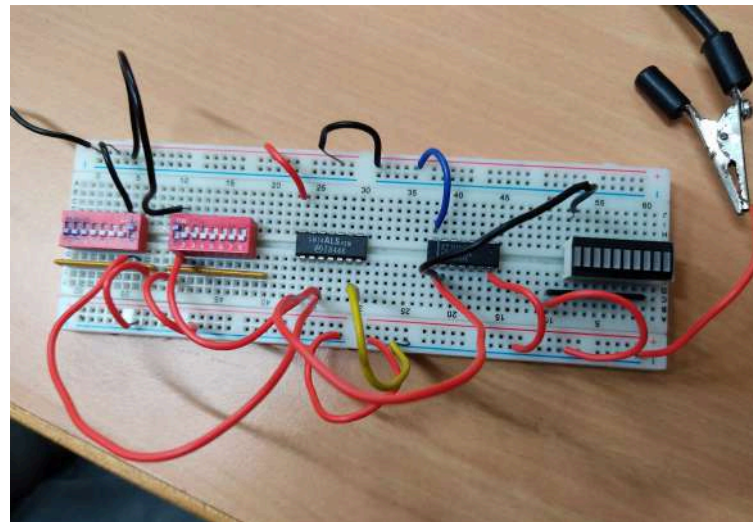
$0_0 \rightarrow 1$



$0_1 \rightarrow 0$



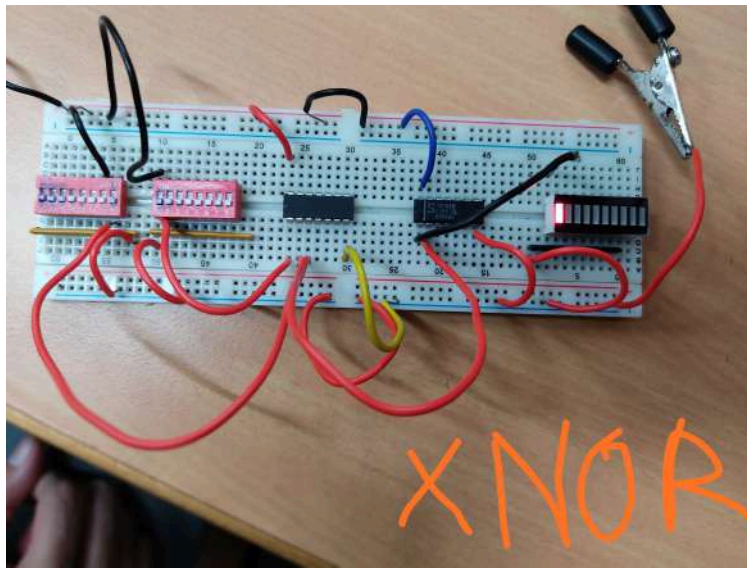
$1_0 \rightarrow 0$



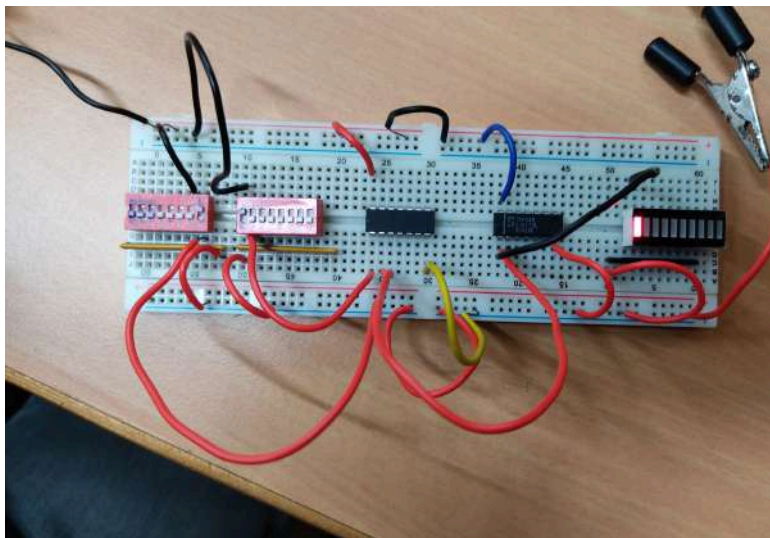
$1_1 \rightarrow 0$



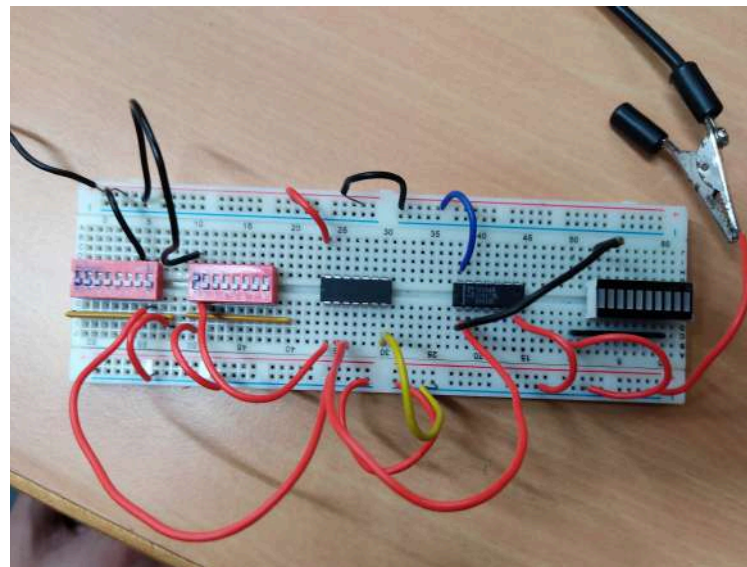
# XNOR:



0\_0  $\rightarrow$  1



1\_1  $\rightarrow$  1



0\_1  $\rightarrow$  0