EE 214: Digital Circuits Laboratory

LAB - 5

Roll No.: 200010003

- **<u>Aim</u>:** Design and Implementation of *Half-Subtractor* circuit using logic gates, and *4-bit Adder-Subtractor* circuit using a full adder.

- **<u>Summary of the experiment</u>:**
    1. Creation of truth table for Half-Subtractor, and obtaining boolean expressions for Difference (D) and Borrow (B).
    2. Design and Implementation of the Half-Subtractor using XOR, NOT, and AND gates.
    3. Design and Implementation of a 4-bit Adder/Subtractor circuit (that uses 2's complement method) using a full adder.

- **<u>Problem Statement:</u>**
    1. Design and implement a Half-Subtractor circuit using a minimum number of 2-input gates.
    2. Familiarize 74LS83 IC and implement a controlled 4-bit Adder/Subtractor circuit which is controlled by signal CTRL using 74LS83 and minimum number of 2-input gates. (CTRL: 0 for Addition and 1 for Subtraction)

- **<u>Components used</u>:** IC 7408, 7404, 7486, 7483, 1 kilo-ohm resistor array, DIP switches, LED displays, breadboard, power supply.

- **<u>Design Procedure, Circuit Diagrams and Snapshots</u>:**

  (attached below)

- **<u>Results and Discussions</u>:**
    1. We constructed a truth table for a Half-Subtractor. Then, we derived the boolean expression for it, and implemented it using the AND, NOT, and XOR logic gates. The outputs obtained were Difference (D) and Borrow (B).
    2. We modified a full-adder into a 4-bit Adder-Subtractor circuit by adding XOR gates at B-inputs, and keeping a CTRL that controls whether the adder obtains B, or 2's complement of B. Keeping C_0 = CTRL ensures that for CTRL = 1, we add 1 to the 1's complement of B, hence obtaining its 2's complement. Also, when CTRL = 0, it makes the XOR gates behave as buffers, and simply allows B to pass.
    3. Subtraction of B from A is the same as adding A to the 2's complement of B. We kept this in mind during the design.

- **<u>Conclusion</u>:**
  We designed and implemented a Half-Subtractor circuit using the basic/special logic gates (AND, NOT, XOR), and verified the outputs obtained using the truth table. We also implemented a 4-bit Adder/Subtractor circuit using IC 7483 (Full Adder), and utilized 2's complement method with the help of XOR gates.

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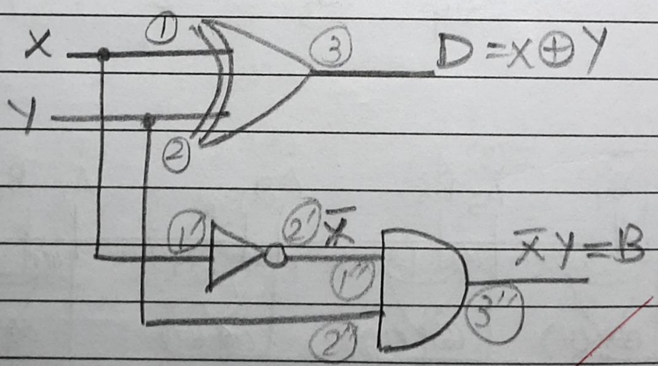
Design Procedure and Circuit Diagram

Half-subtractor (≥ 2 input gates)

X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$D = \overline{X}Y + X\overline{Y} = X \text{ XOR } Y = X \oplus Y$

$B = \overline{X}Y$



(1 XOR gate
1 NOT gate
1 AND gate)

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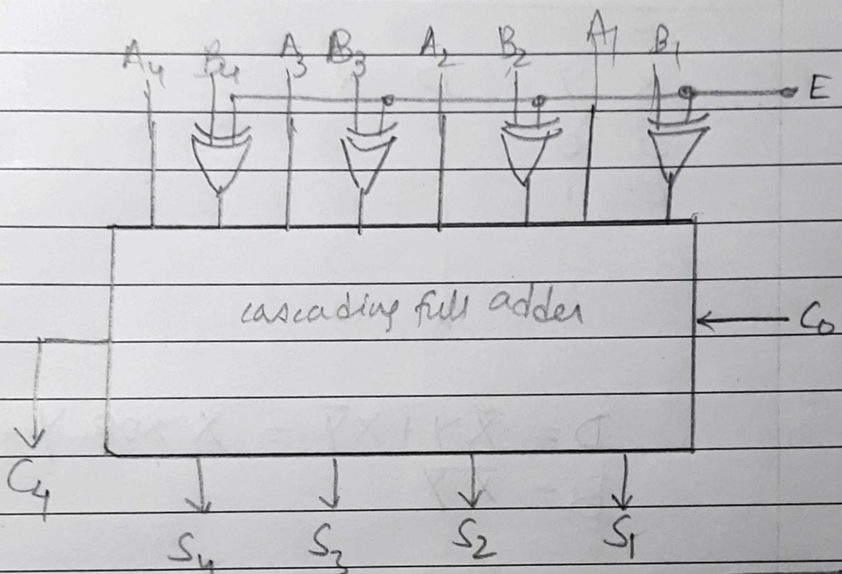
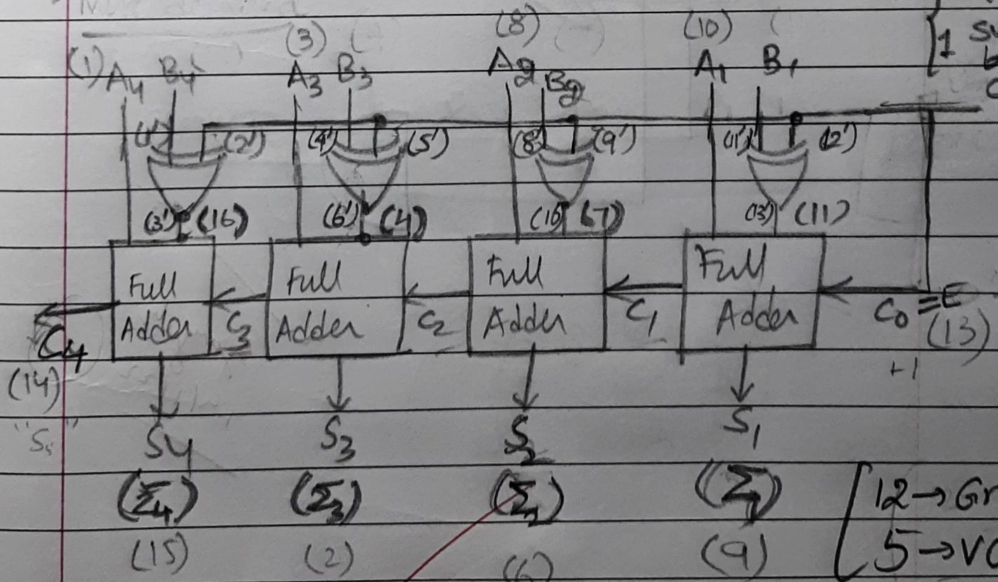
Adder/Subtractor using Full Adder



(E=CTRL)

$E = \begin{cases} 0 & \text{Adder} \\ 1 & \text{subtractor by 2's compl.} \end{cases}$



$\begin{bmatrix} 12 \rightarrow \text{Gnd} \\ 5 \rightarrow \text{VCC} \end{bmatrix}$

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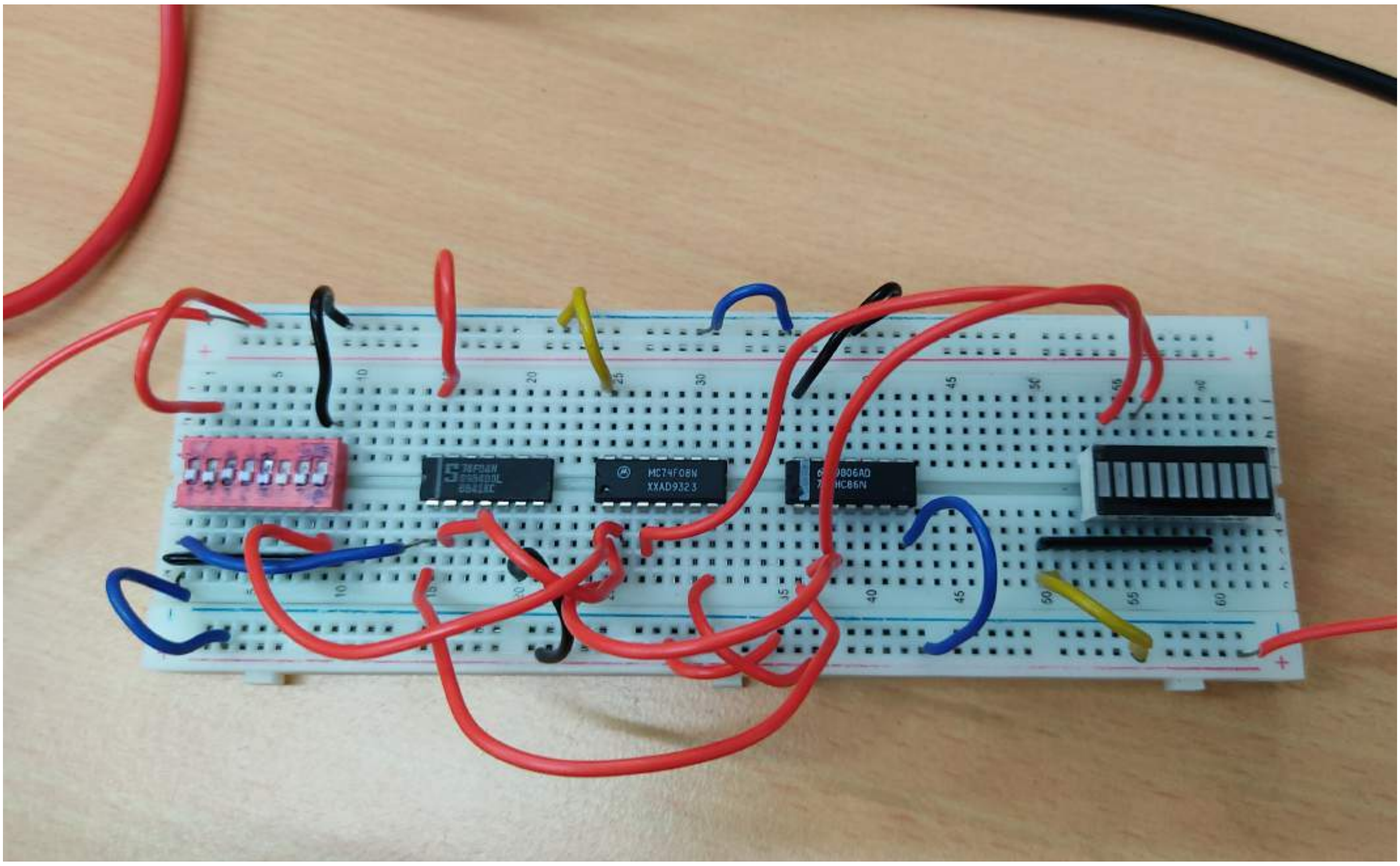
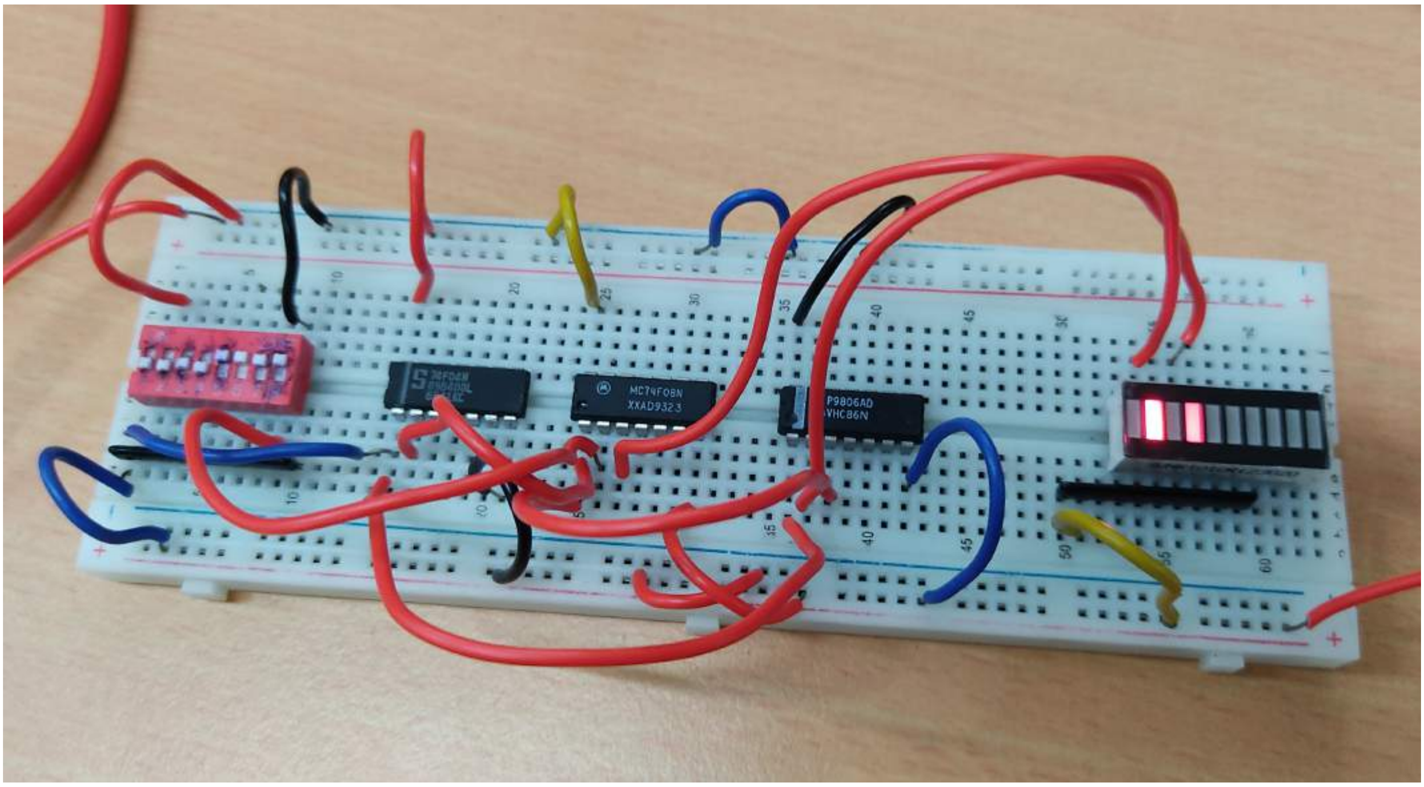
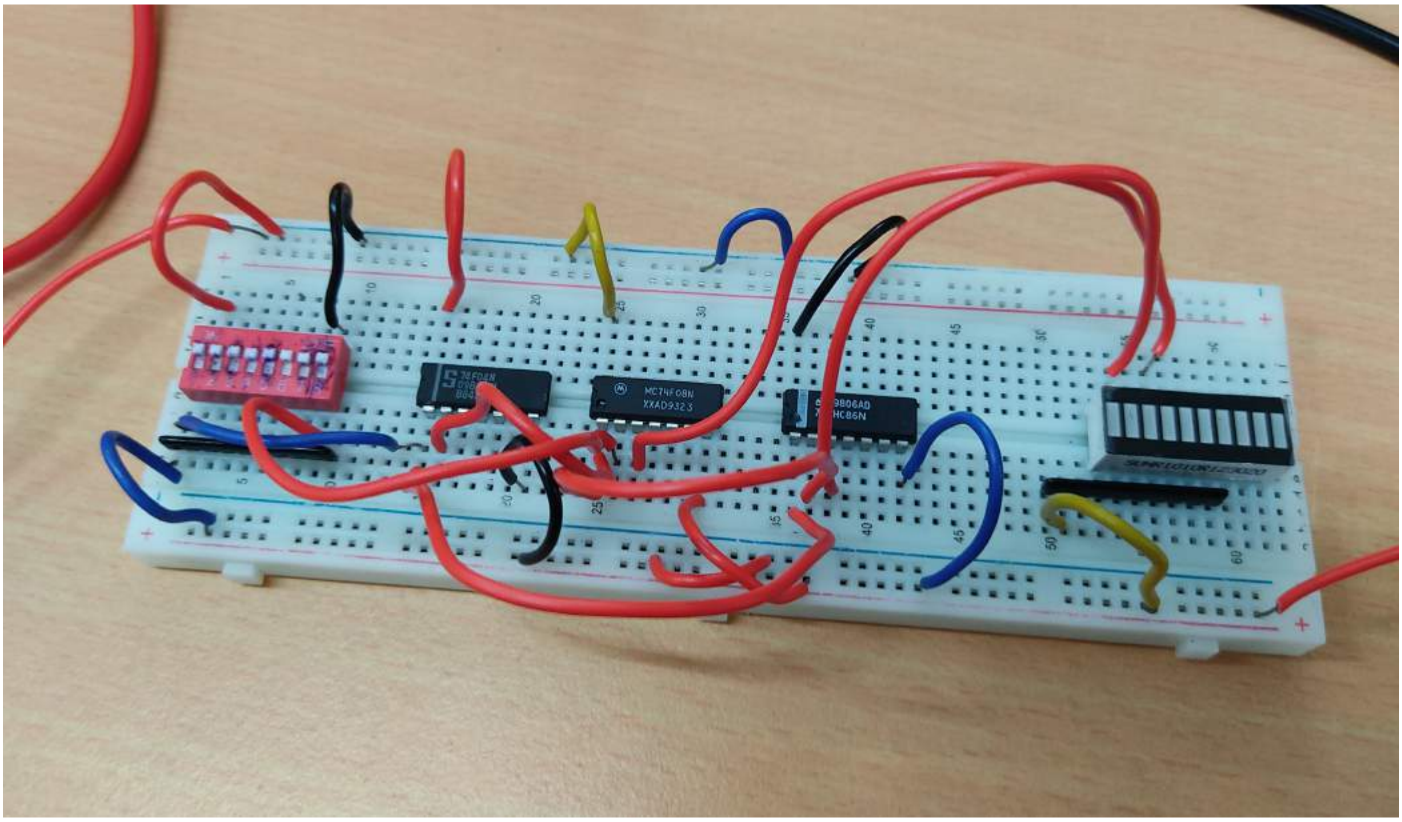
$A + 2\text{'s compl}(B) = A - B$

Circuit Snapshots

Problem 1 : Half-Subtractor



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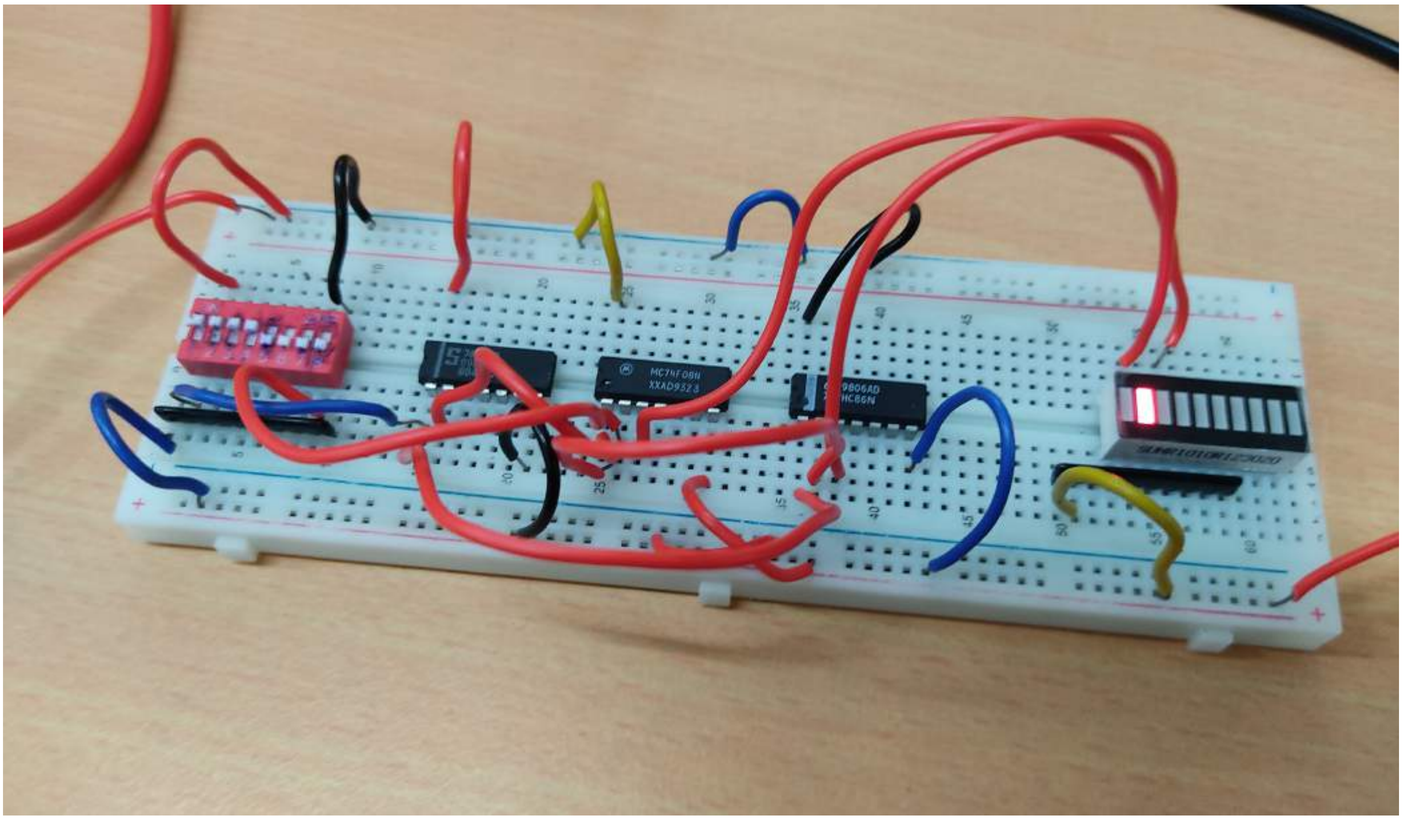
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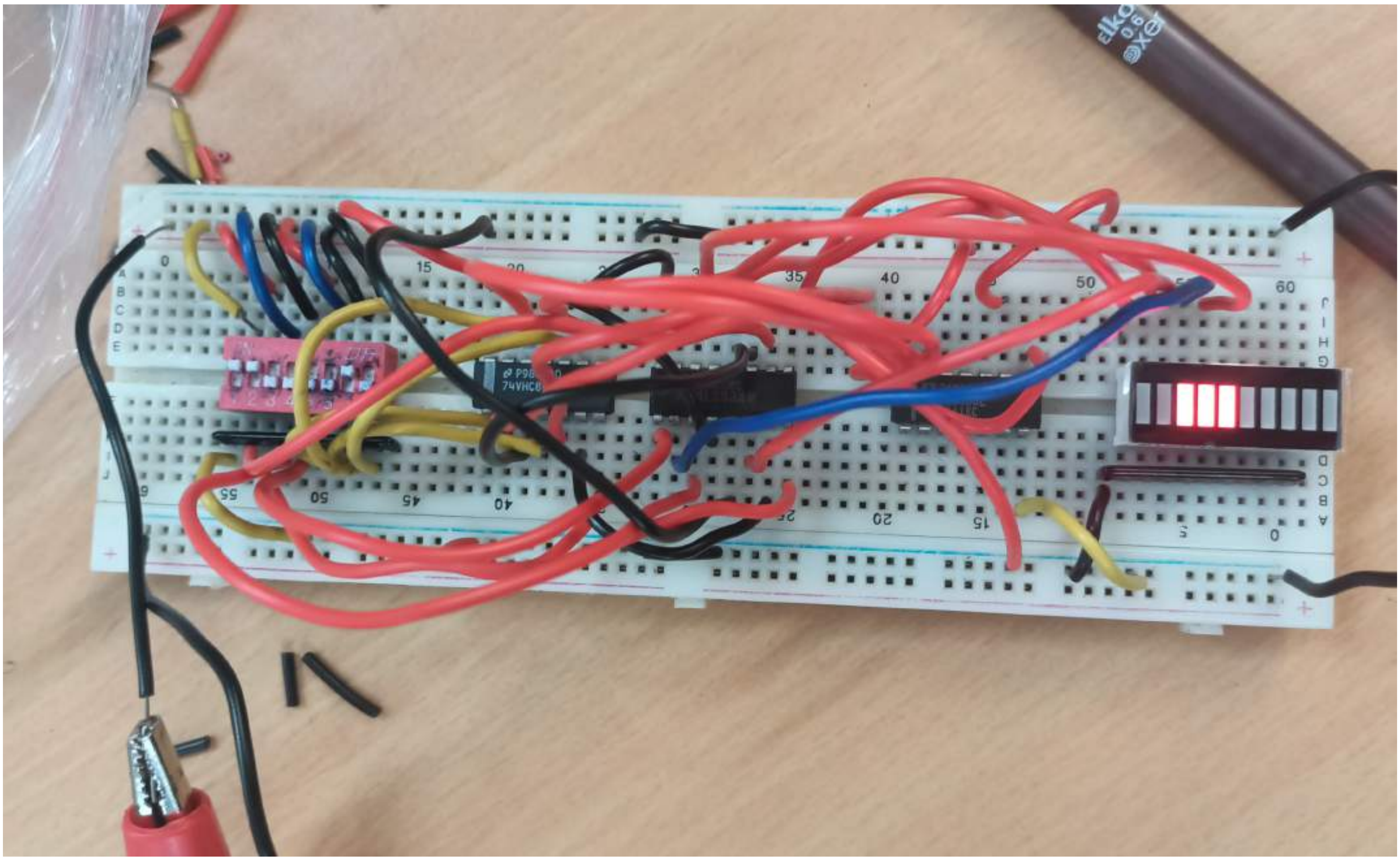
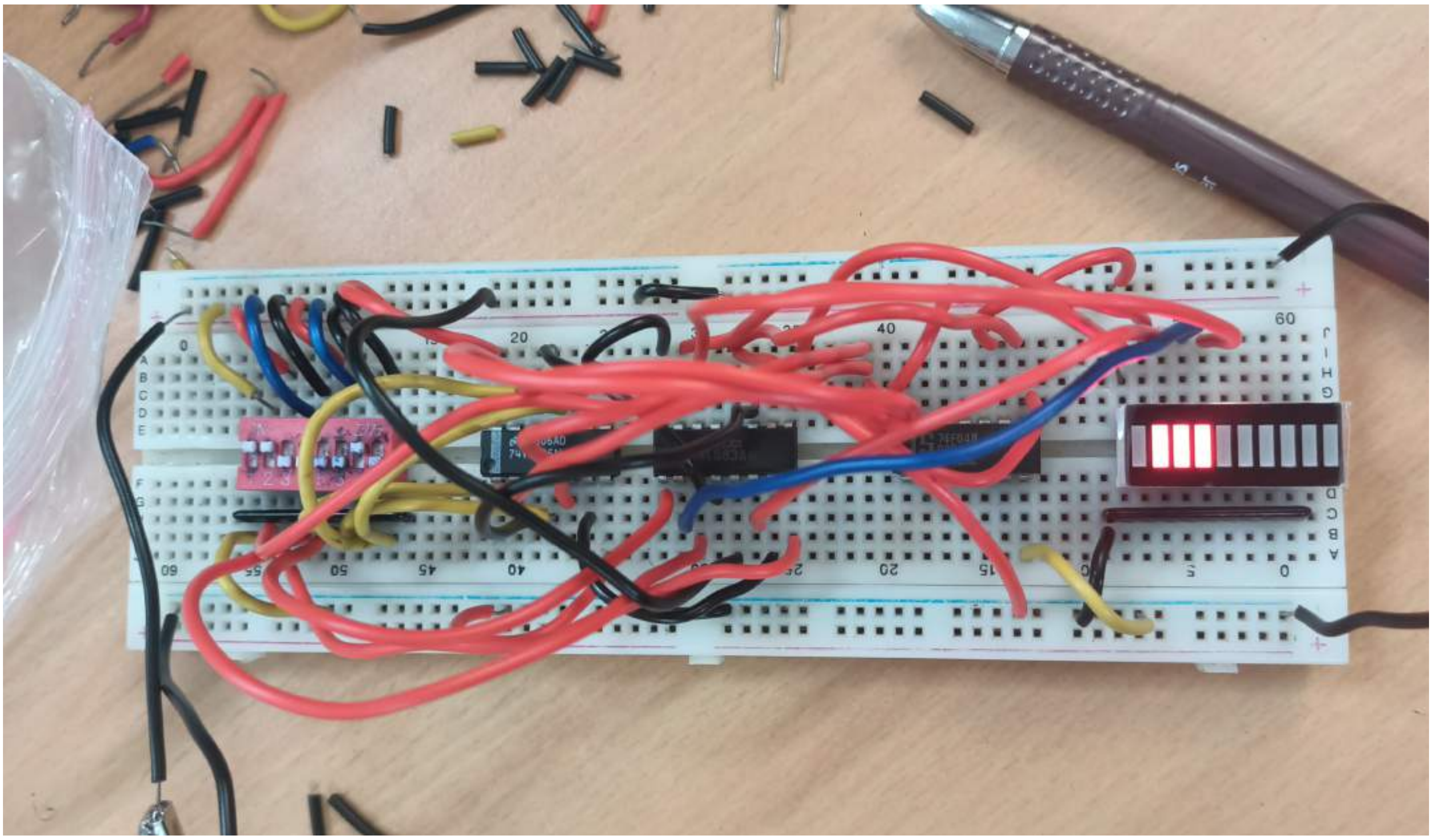
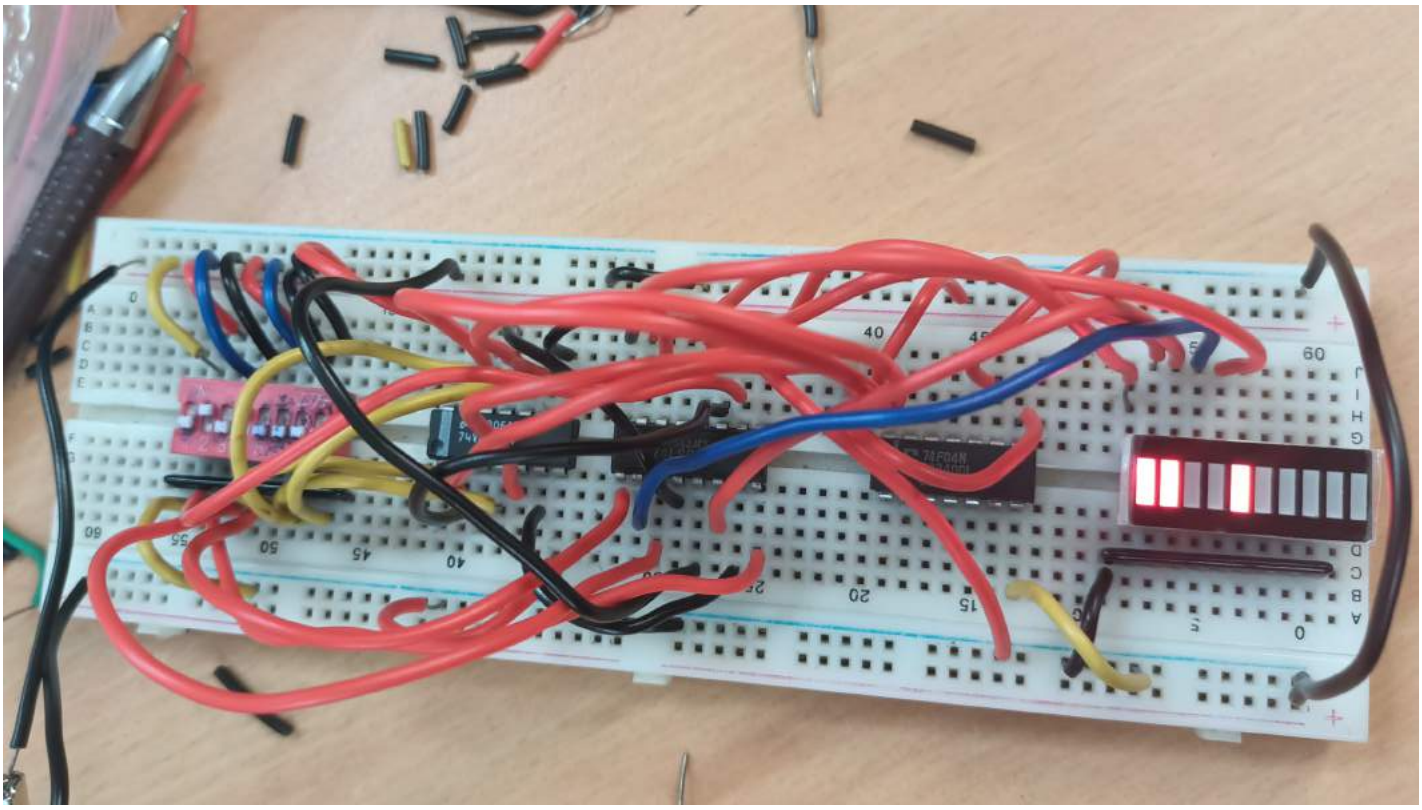
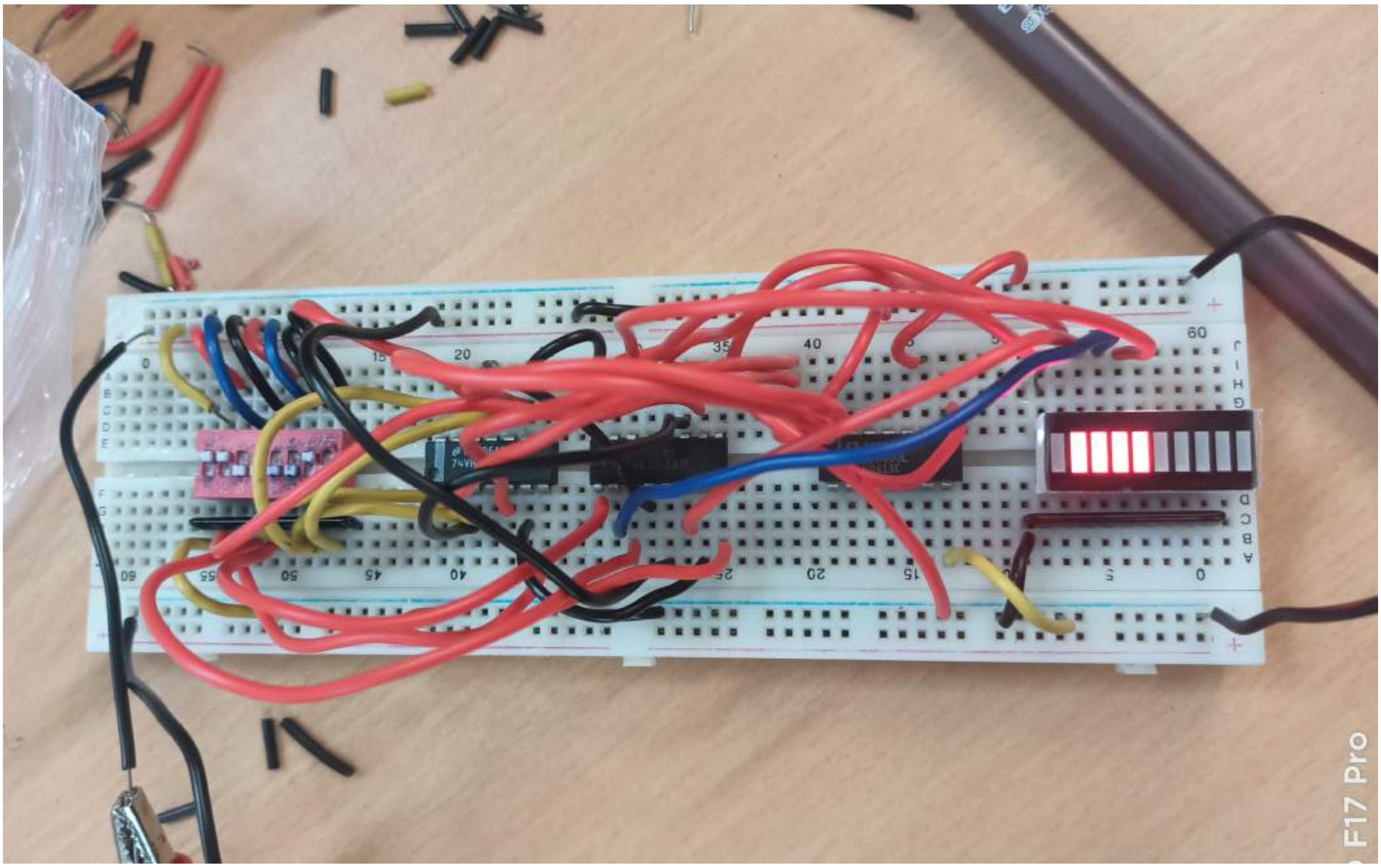
Problem 2 : 4-bit Adder/Subtractor





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