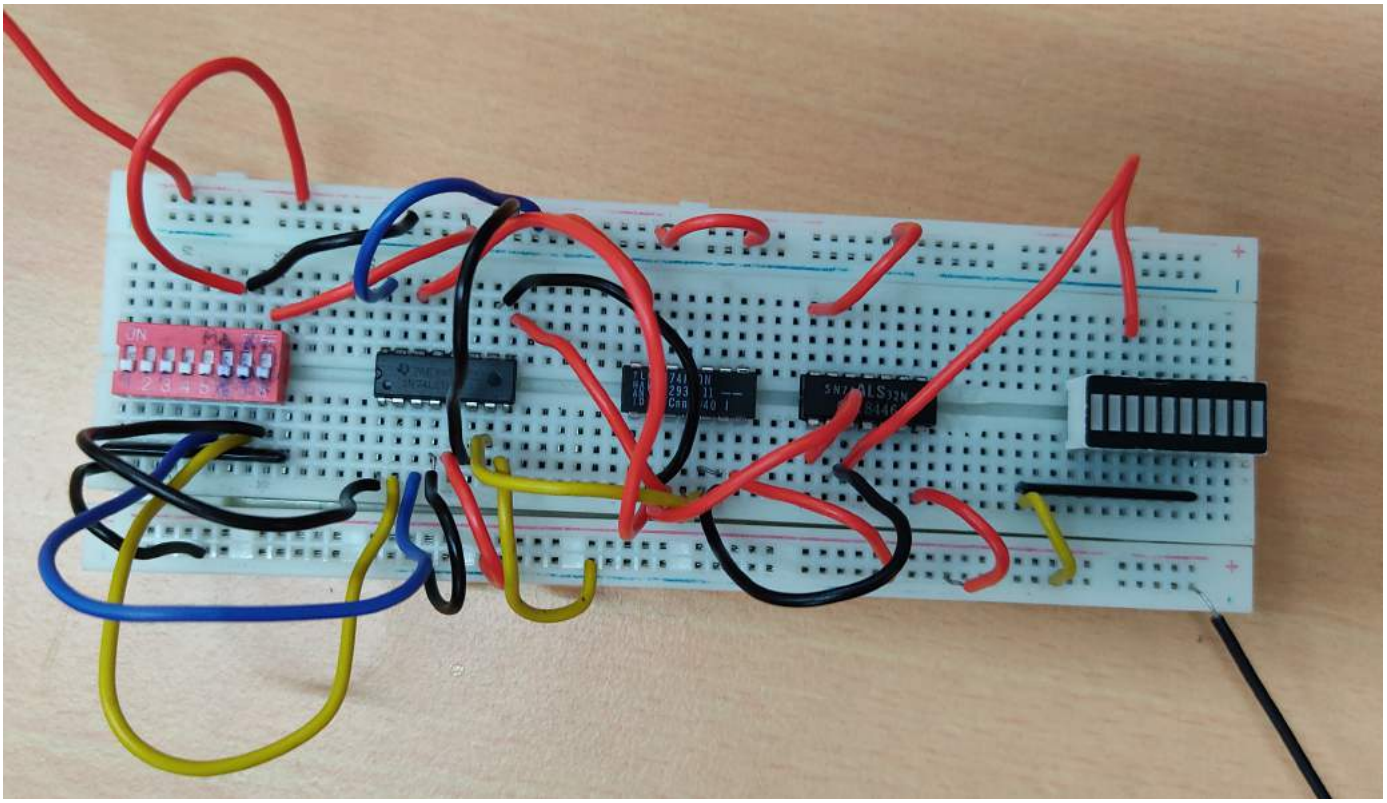
1) Circuit using 3:8 decoder and suitable 2-input logic gates.



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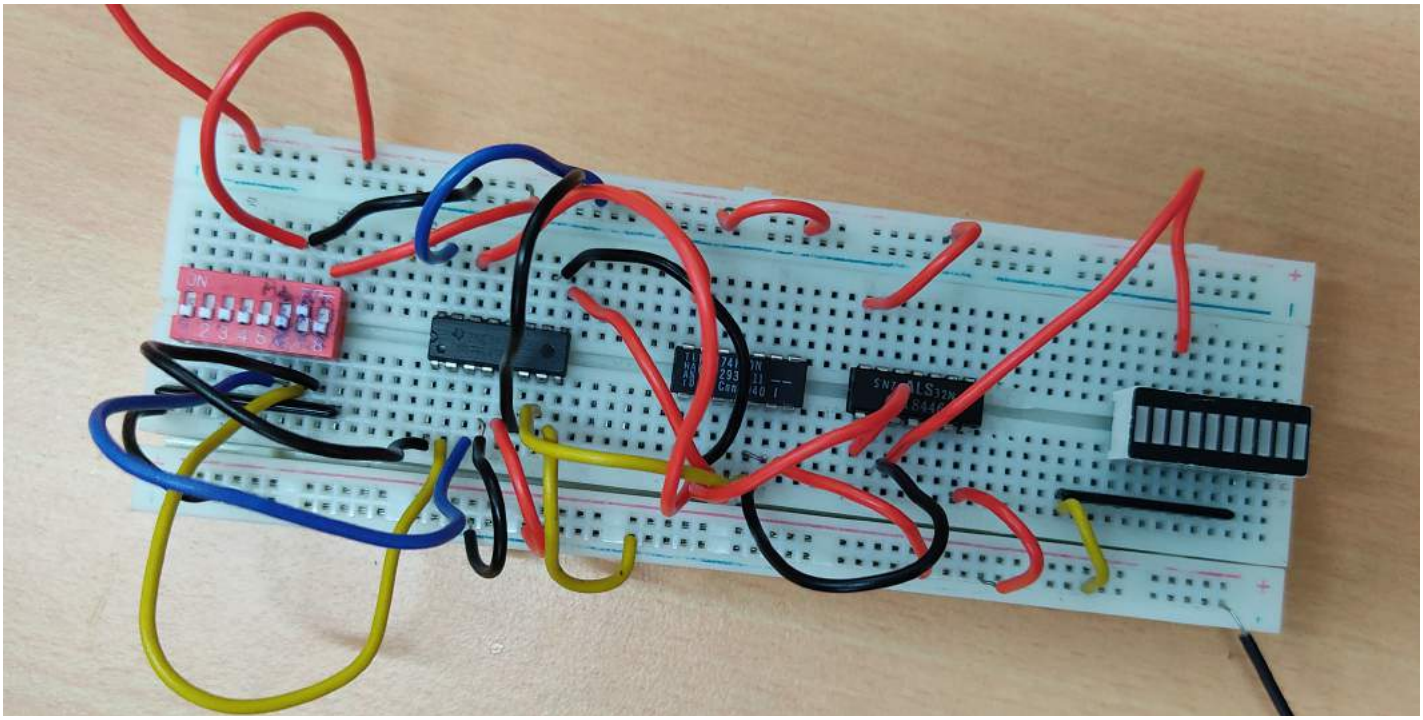

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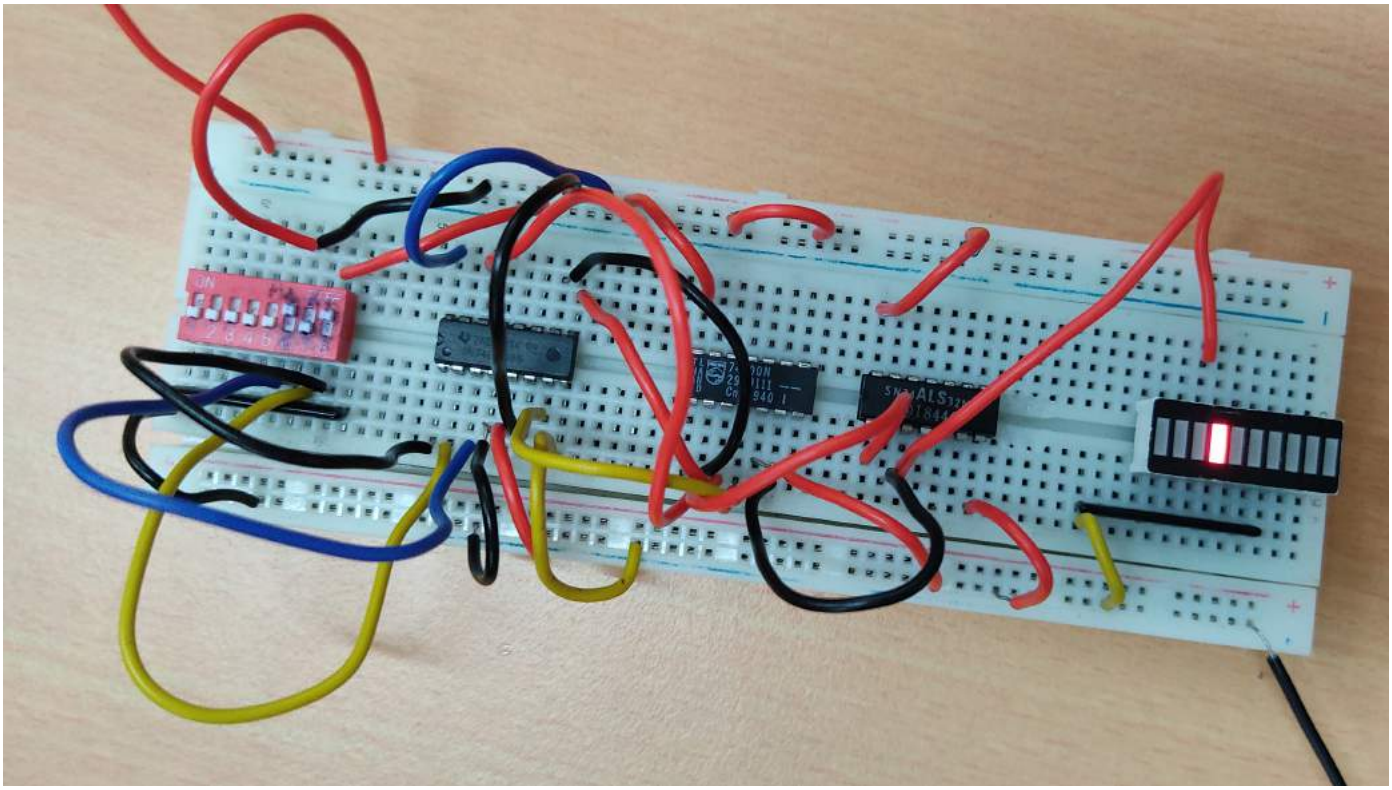

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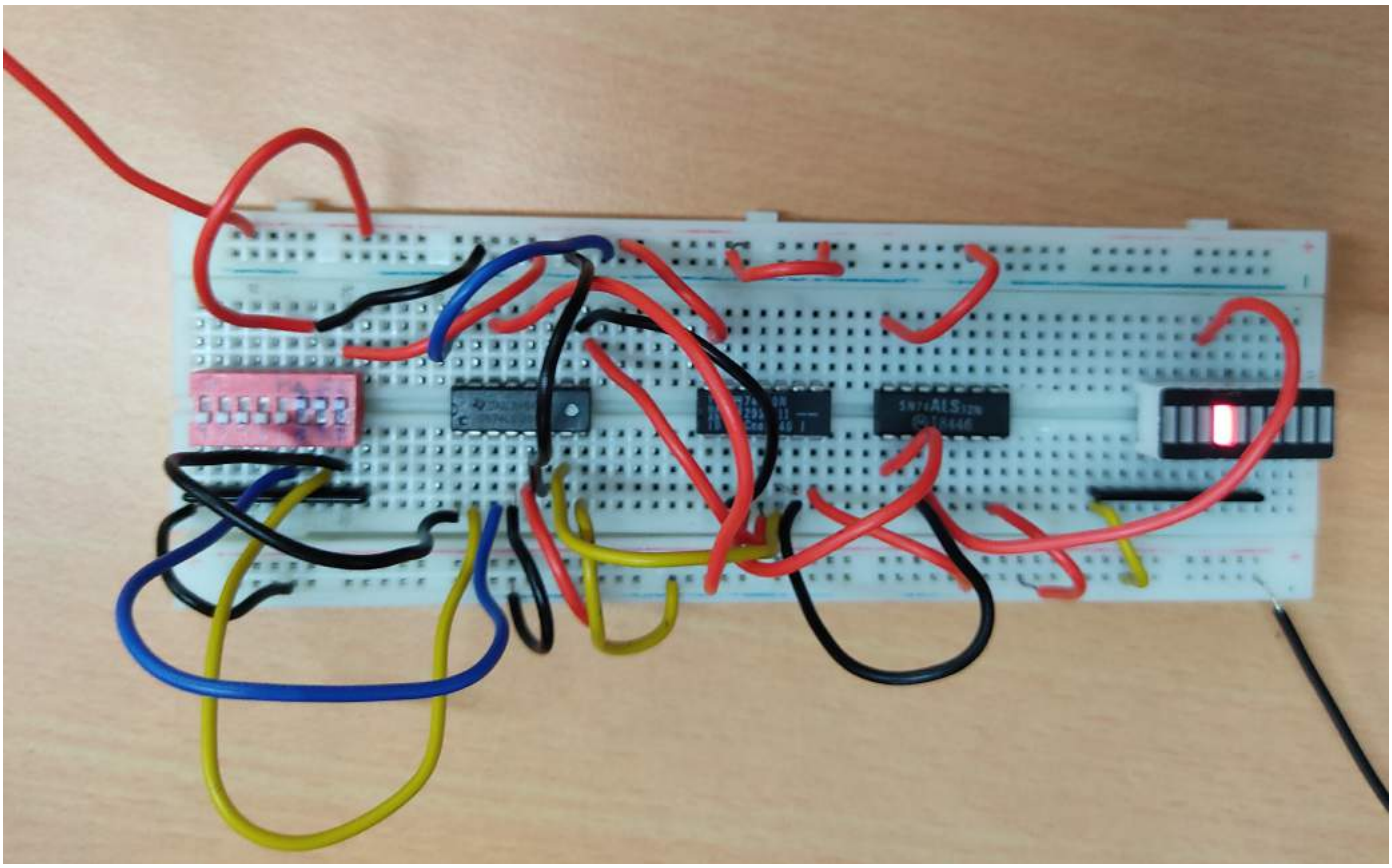

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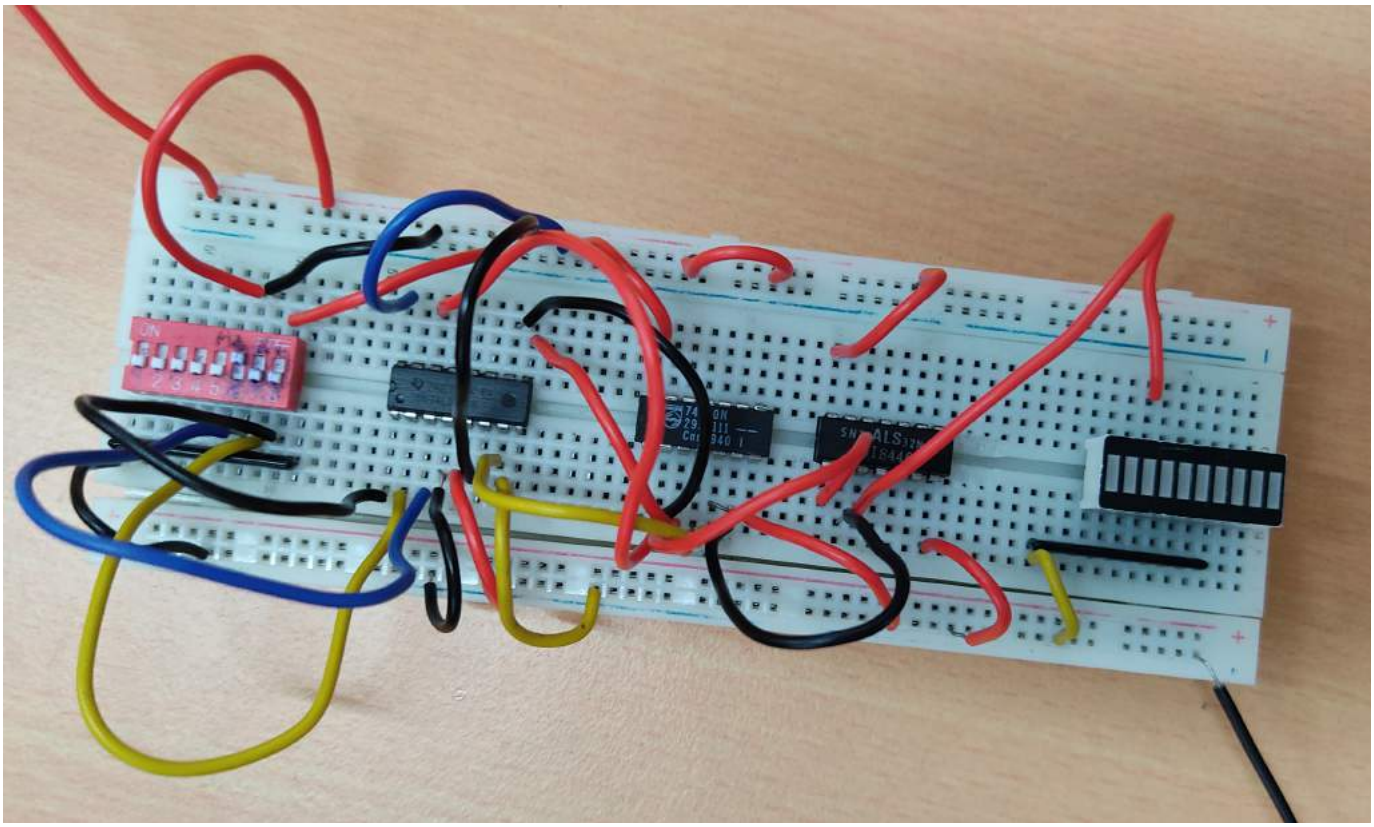

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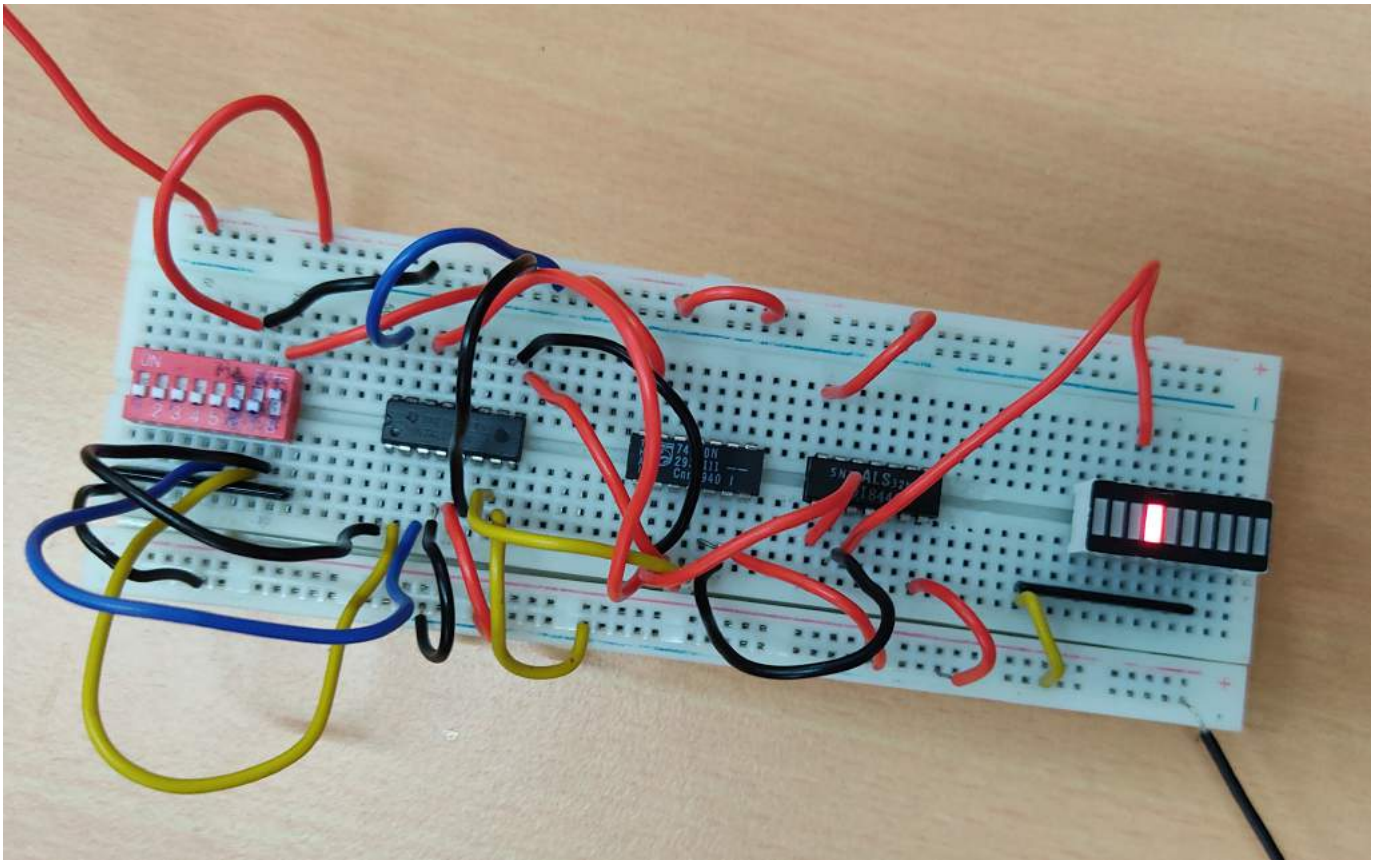

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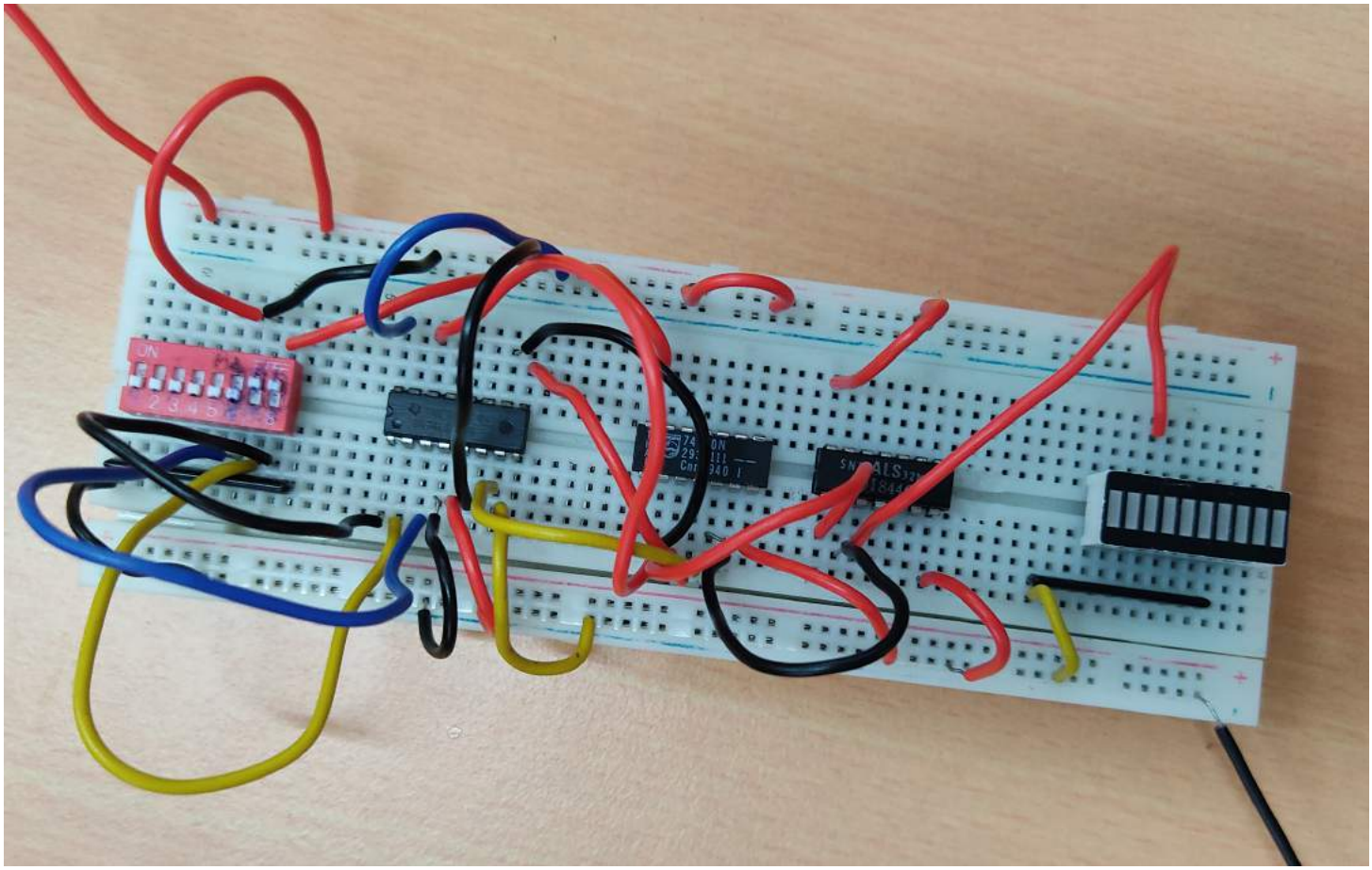

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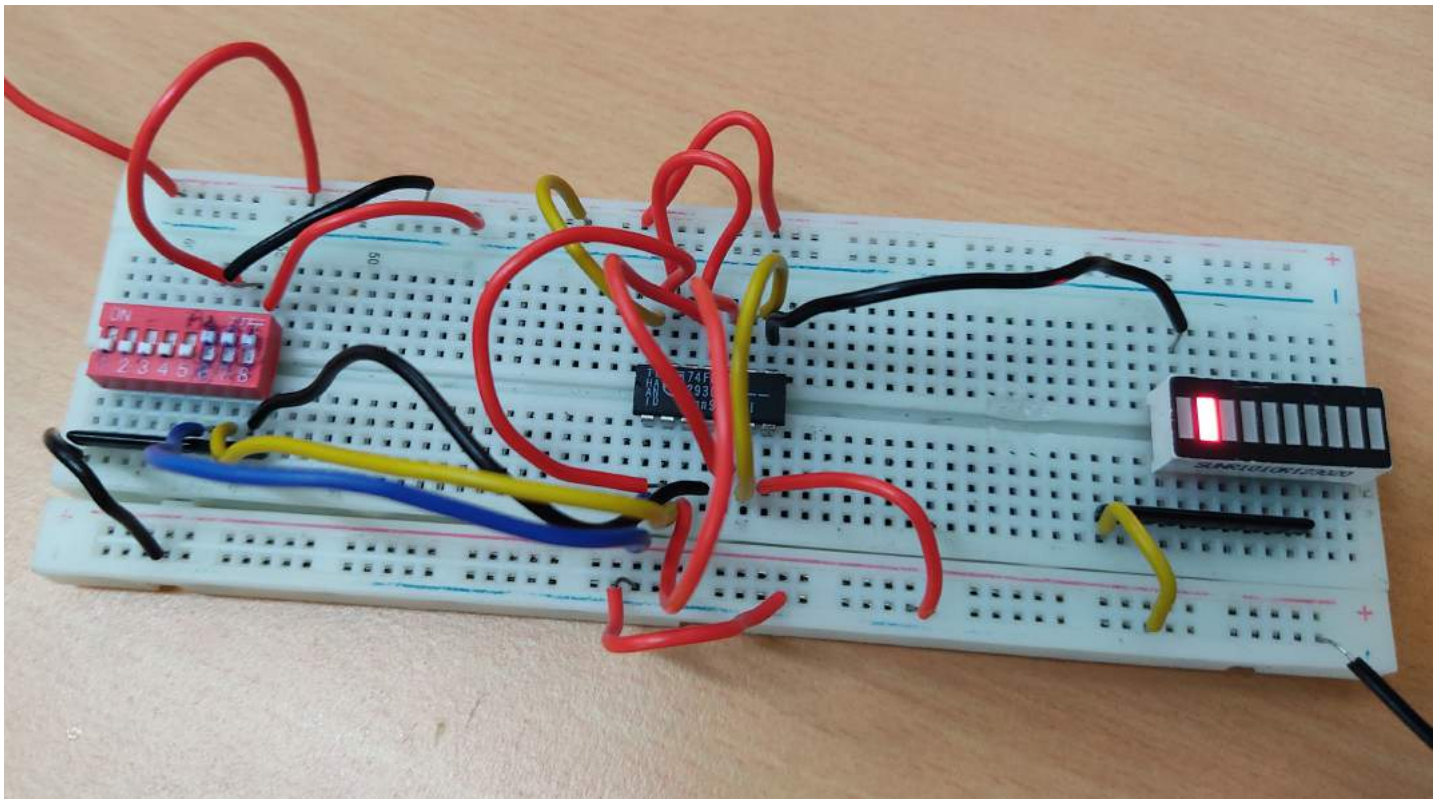
2) Circuit using 2-inputs NAND gates.



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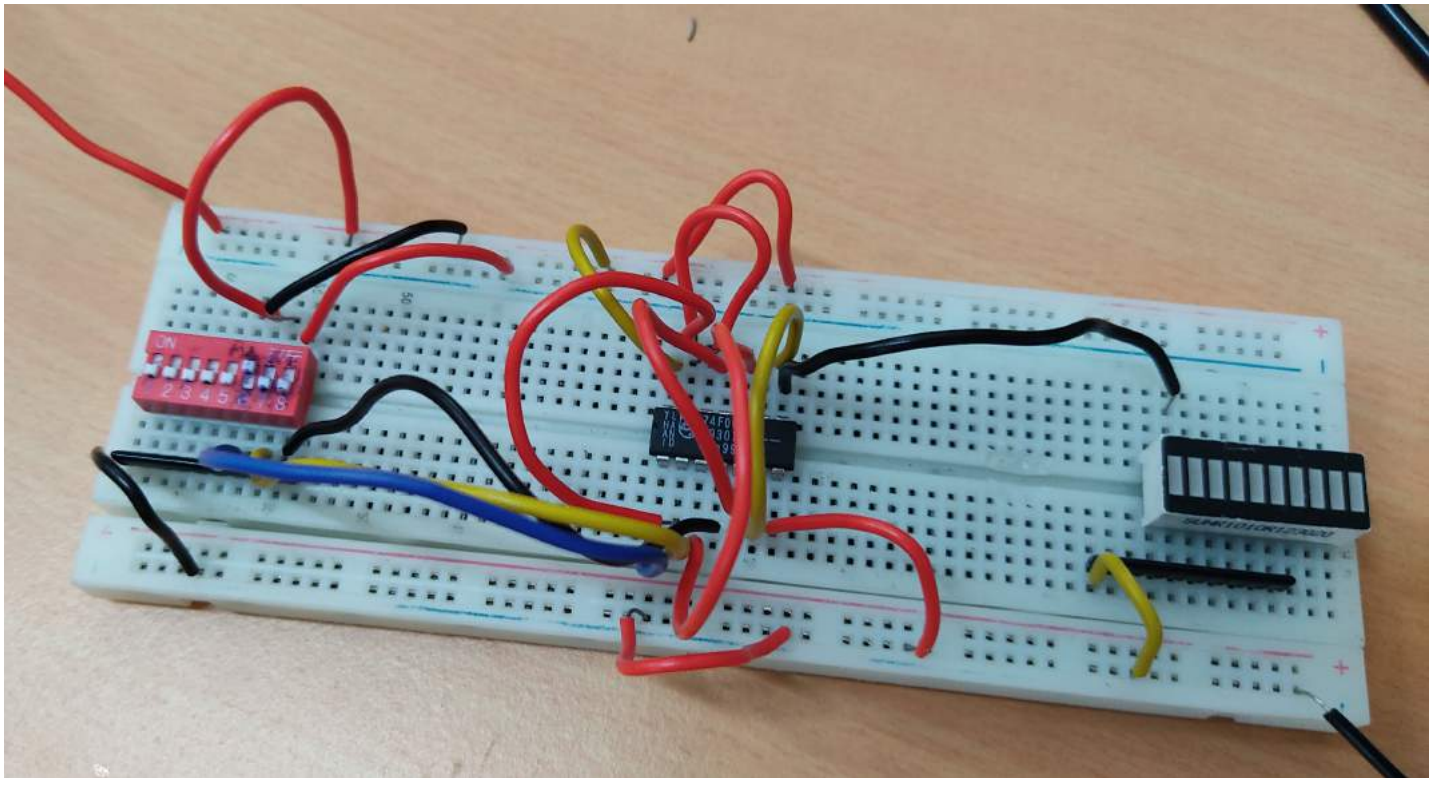

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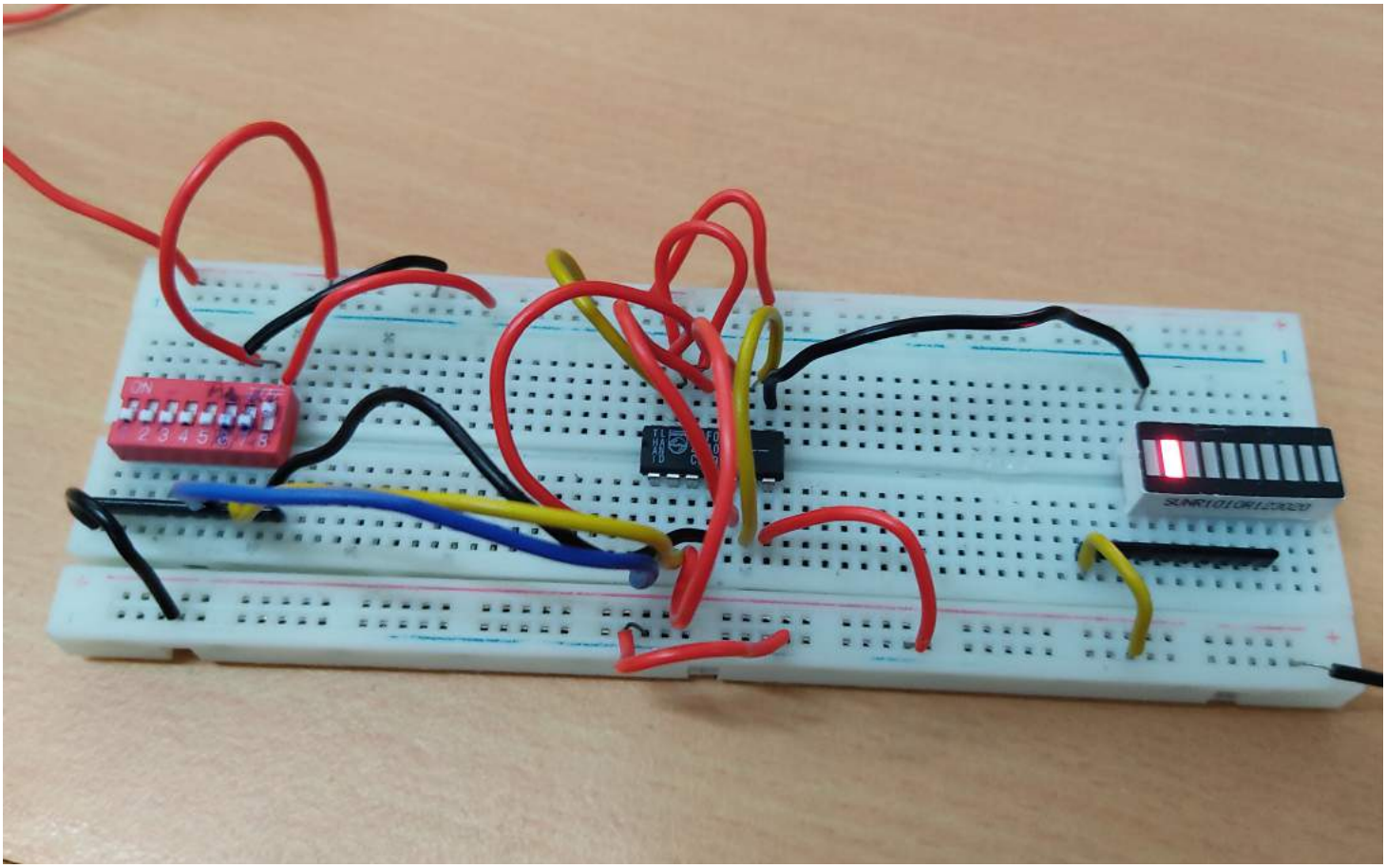

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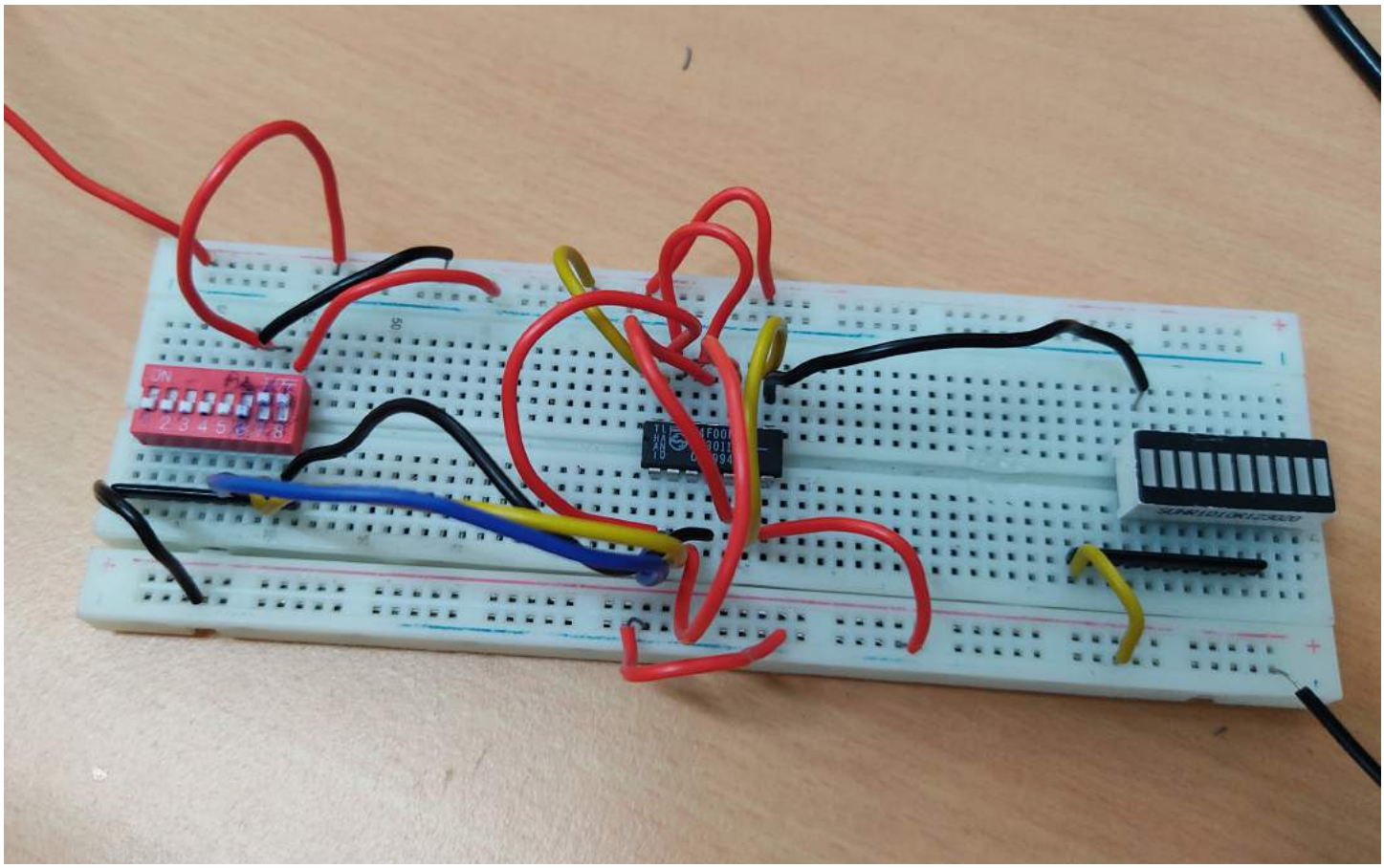

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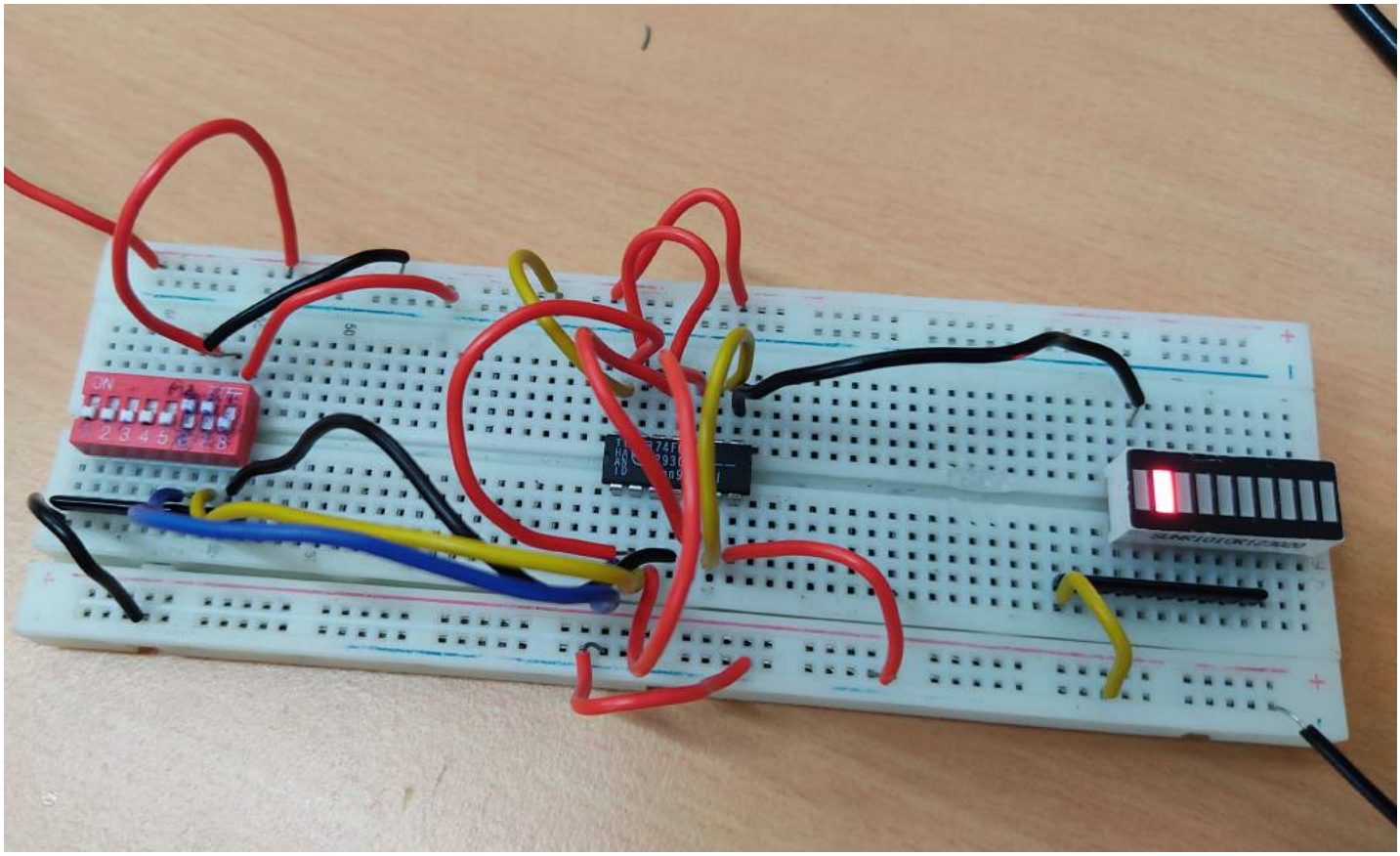

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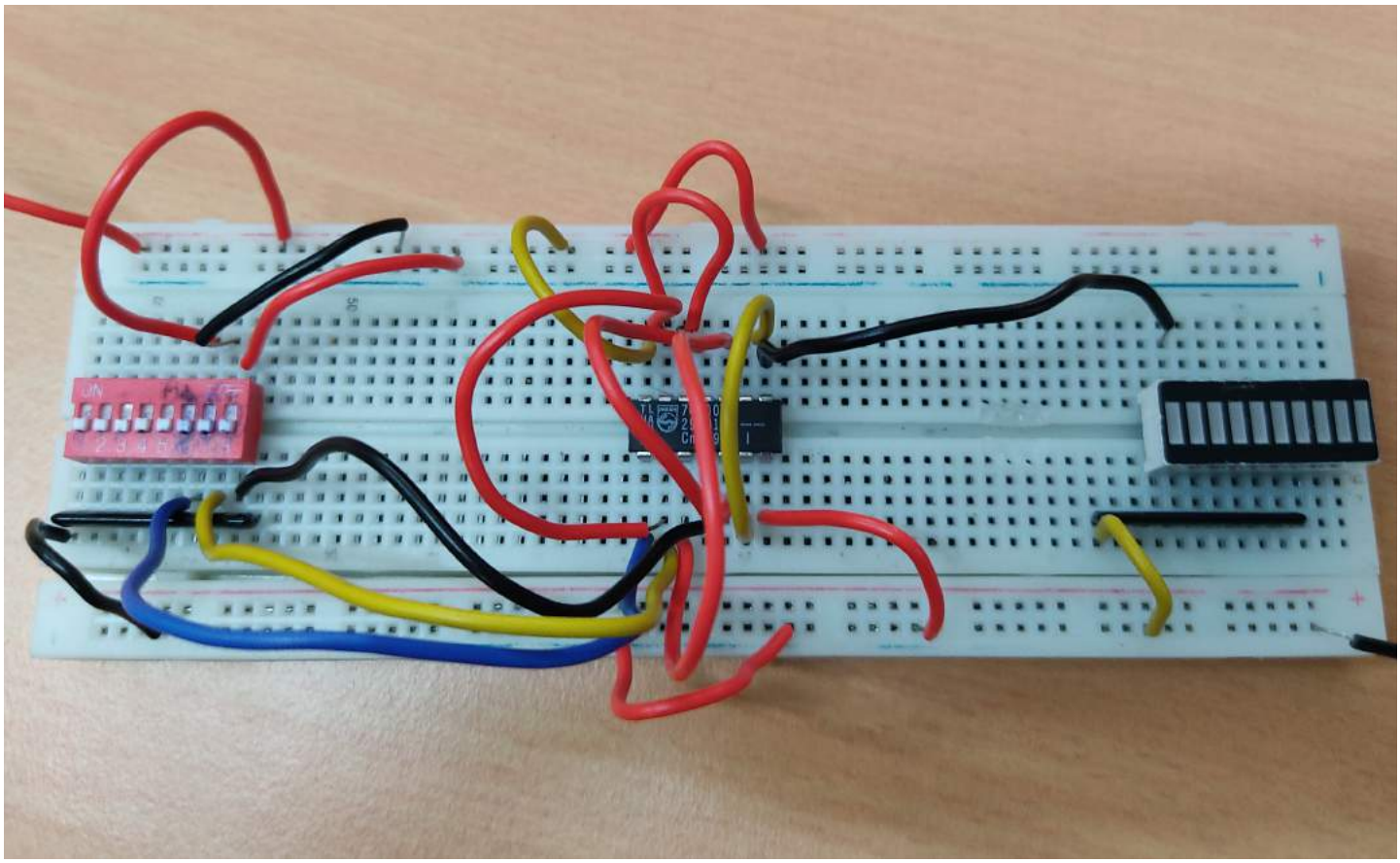

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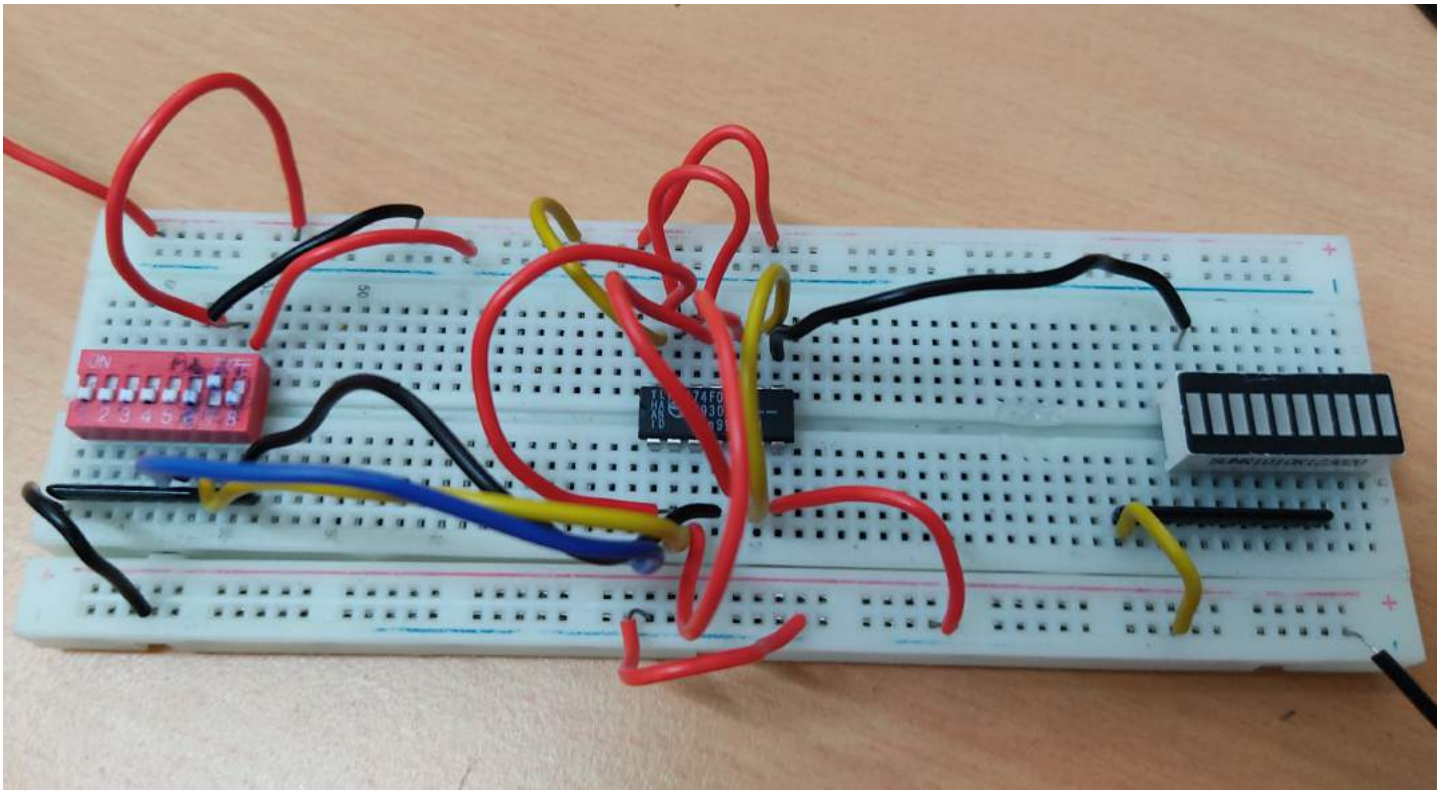

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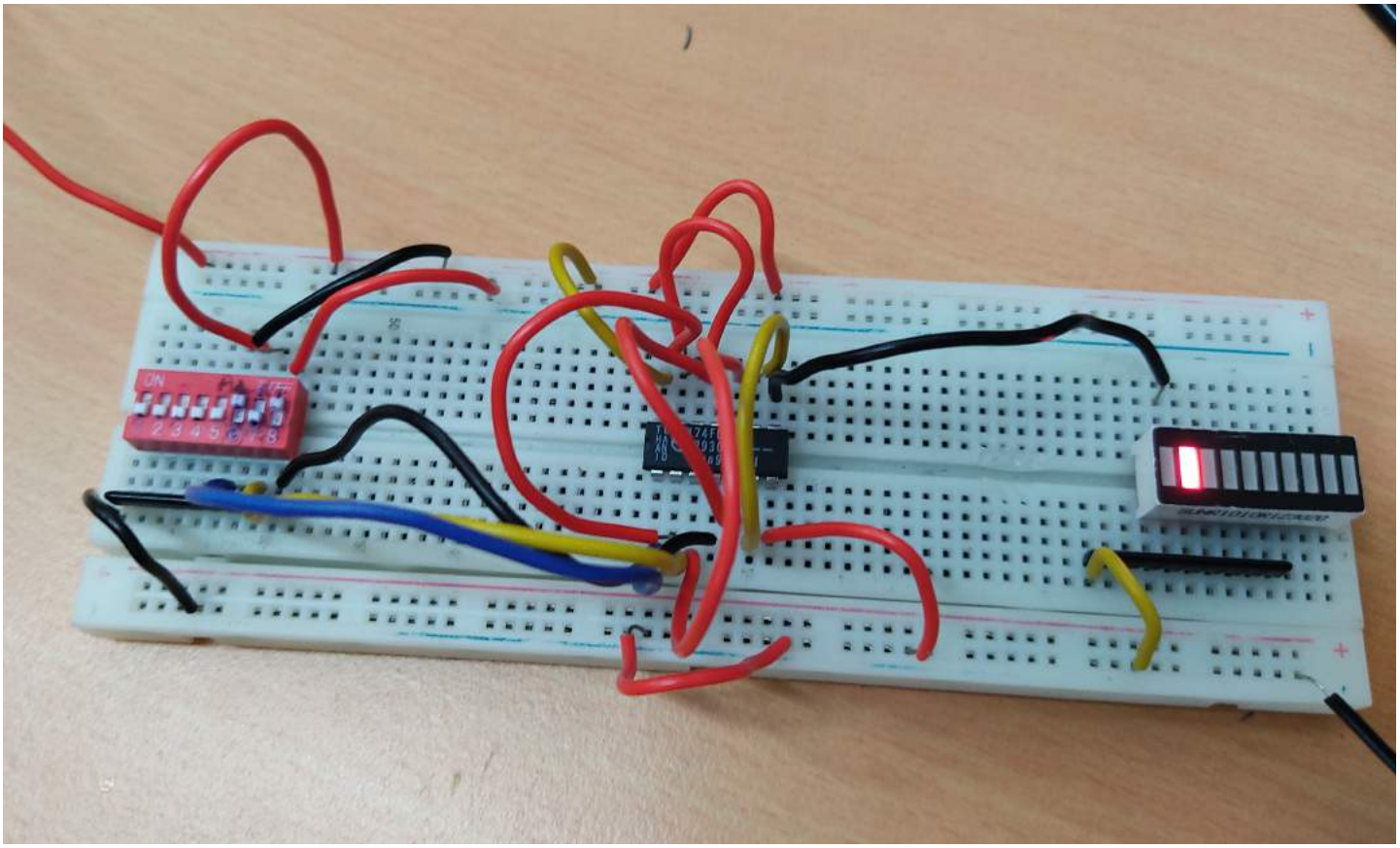

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