

EE 214: Digital Circuits Laboratory

LAB - 4

Roll No.: 200010003

- **Aim:** Realization of Boolean Circuits with Karnaugh Maps (K-maps), using basic and universal logic gates.
- **Summary of the experiment:**
 1. Creation of truth table for the given problem statement
 2. Reduction of Boolean expression using K-Map
 3. Implementation of the logic expression using
 - (a) Basic Logic Gate
 - (b) Universal Logic Gate (NAND)
- **Problem Statement:**

A security system opens and closes the door for the Red (R), Blue (B), and Green (G) colored LED outputs sensed by the controlling unit. The door remains closed for the following conditions:

 - 1) All 3 LEDs are off.
 - 2) Green LED is ON and Blue LED is OFF.
(MSB : Red (R) , LSB : Blue (B))

Implement the logic:

 - a) Using basic gates (AND, OR, NOT).
 - b) Only using NAND.
- **Components used:** IC 7408, 7432, 7404, 7400, 1 kilo-ohm resistor array, DIP switches, LED displays, breadboard, power supply.
- **Design Procedure, Circuit Diagrams and Snapshots:**

(attached below)

- **Results and Discussions:**

1. We constructed a truth table for the given problem statement. Then, we formed and simplified a boolean expression for the logic with the use of Karnaugh maps. The logic was implemented using basic gates, as well as universal gate.
2. Usage of Karnaugh maps greatly reduces the number of components required in the logic circuit, as it highlights the possible simplifications as pairs, quads, and octets.

- **Conclusion:**

We formulated, simplified, and implemented the given logic statement with the help of Karnaugh Map (K-maps), then proceeded to implement it using the basic logic gates (AND, OR, NOT), as well as the universal gate (NAND). The outputs obtained were verified using the truth table.

Design Procedure and Circuit Diagram.

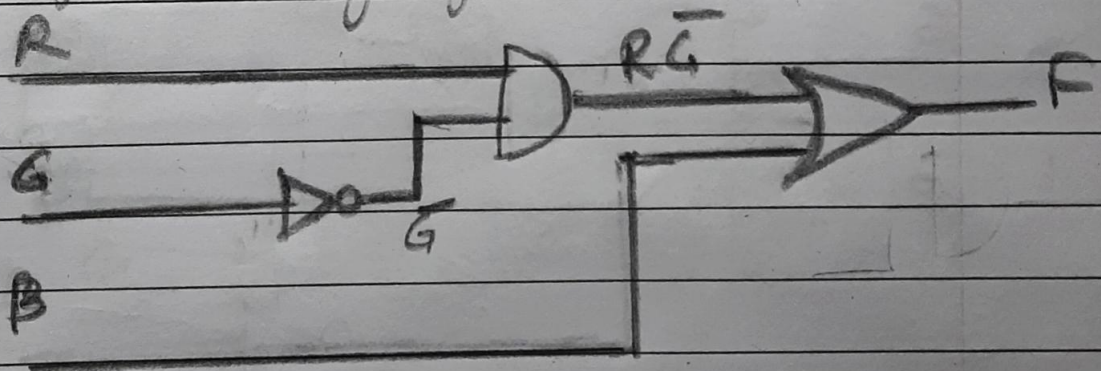
① = open (on)

1 = closed (off)

	GB	$G+B$	$G+\bar{B}$	$\bar{G}+B$	$\bar{G}+\bar{B}$
R	00	01	11	10	
$R=0$	0			0	
$\bar{R}=1$				0	

$$F = (R+B)(\bar{G}+B) \quad (\text{POS form})$$

(a) Using basic logic gates :-



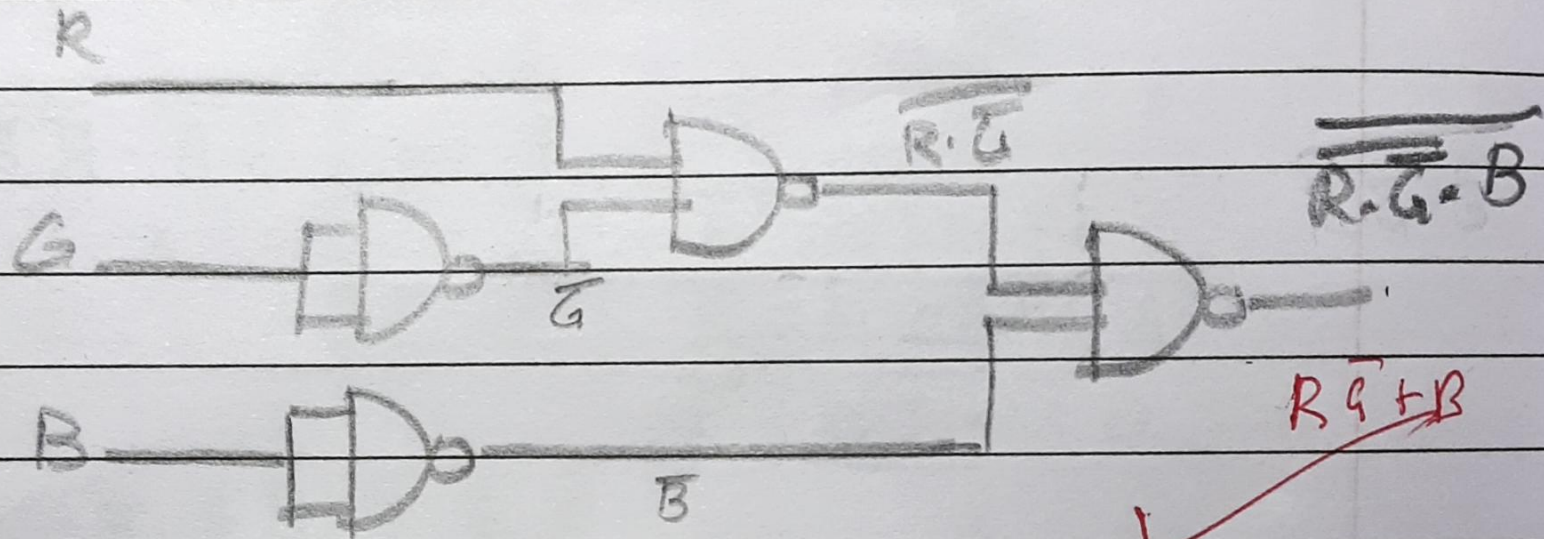
$$F = R\bar{G} + B$$

SGanguly

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$$F = \overline{R\bar{G} + B} = \overline{R\bar{G}} \cdot \bar{B}$$

(b) using NAND.



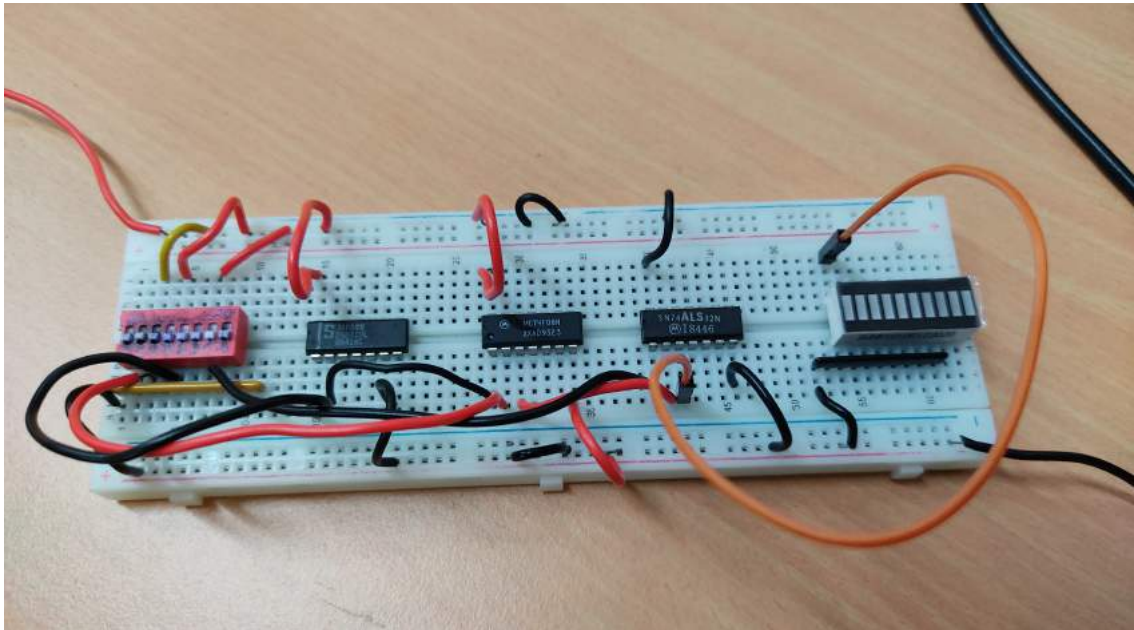
$R \cdot G \cdot B$

Sengul

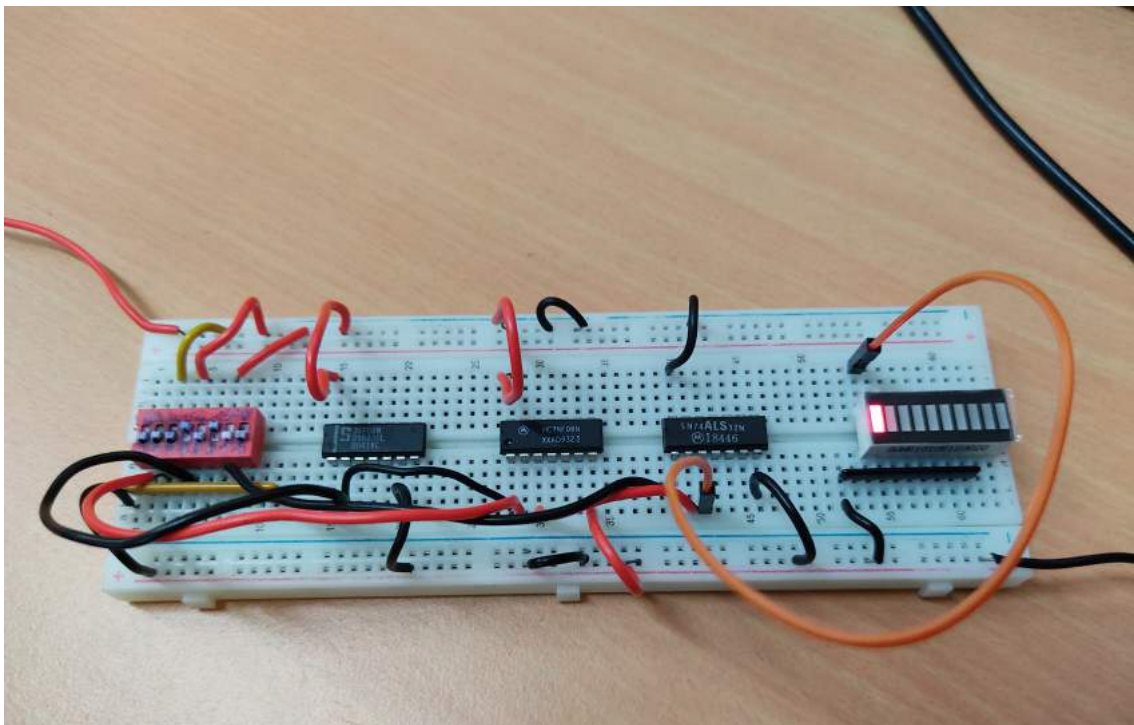
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Circuit Snapshots

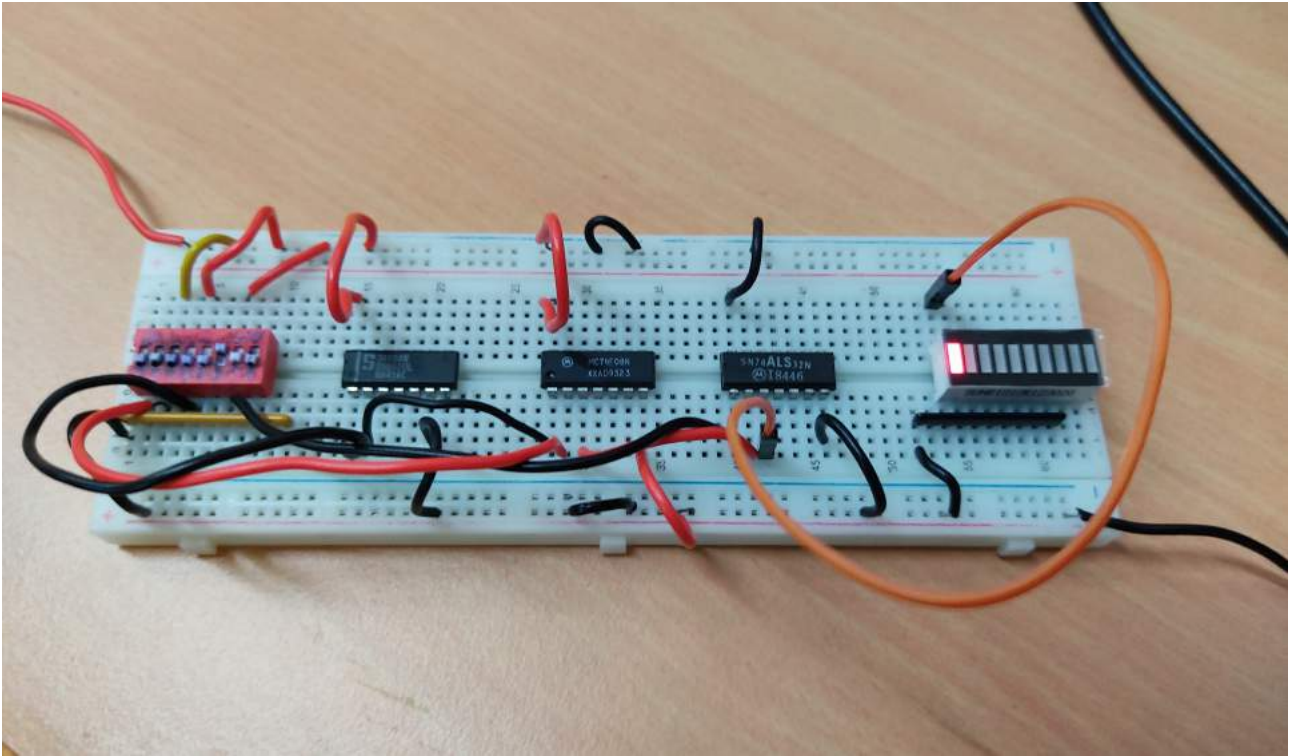
Implementation using Basic gates:



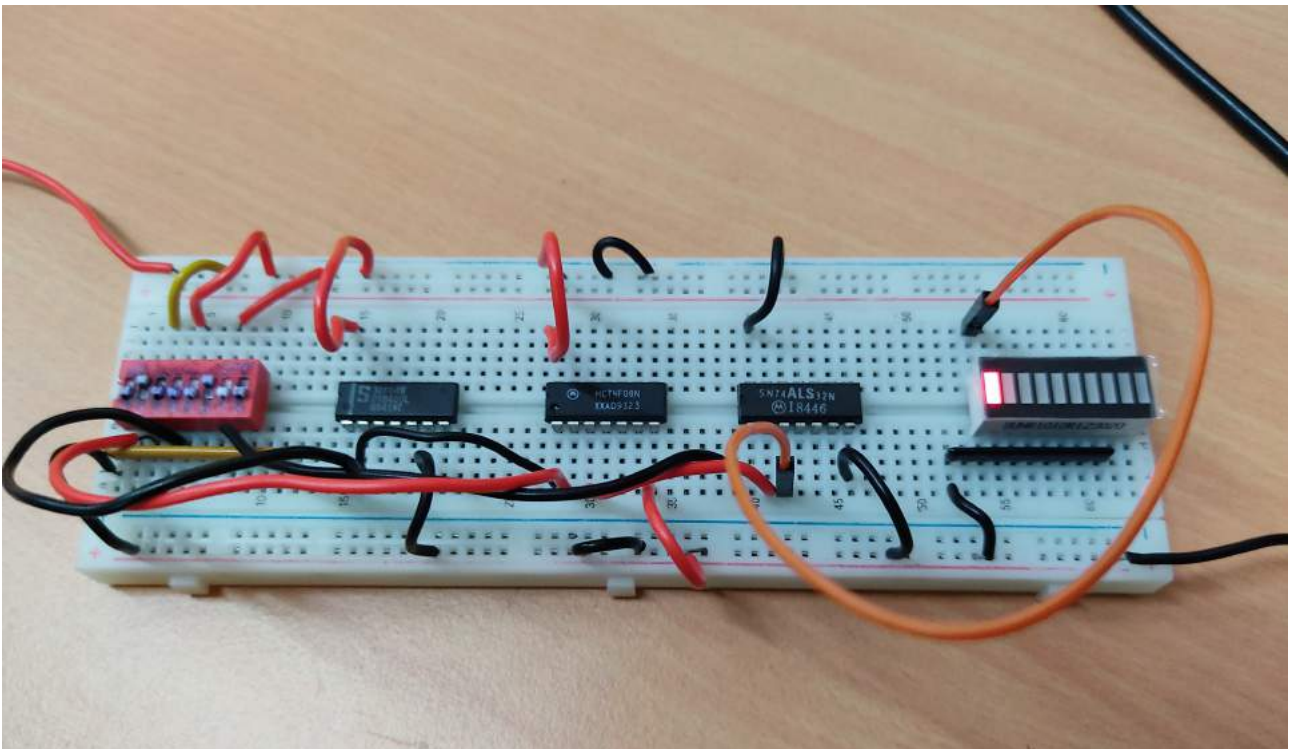
$0_0_0 \rightarrow 0$



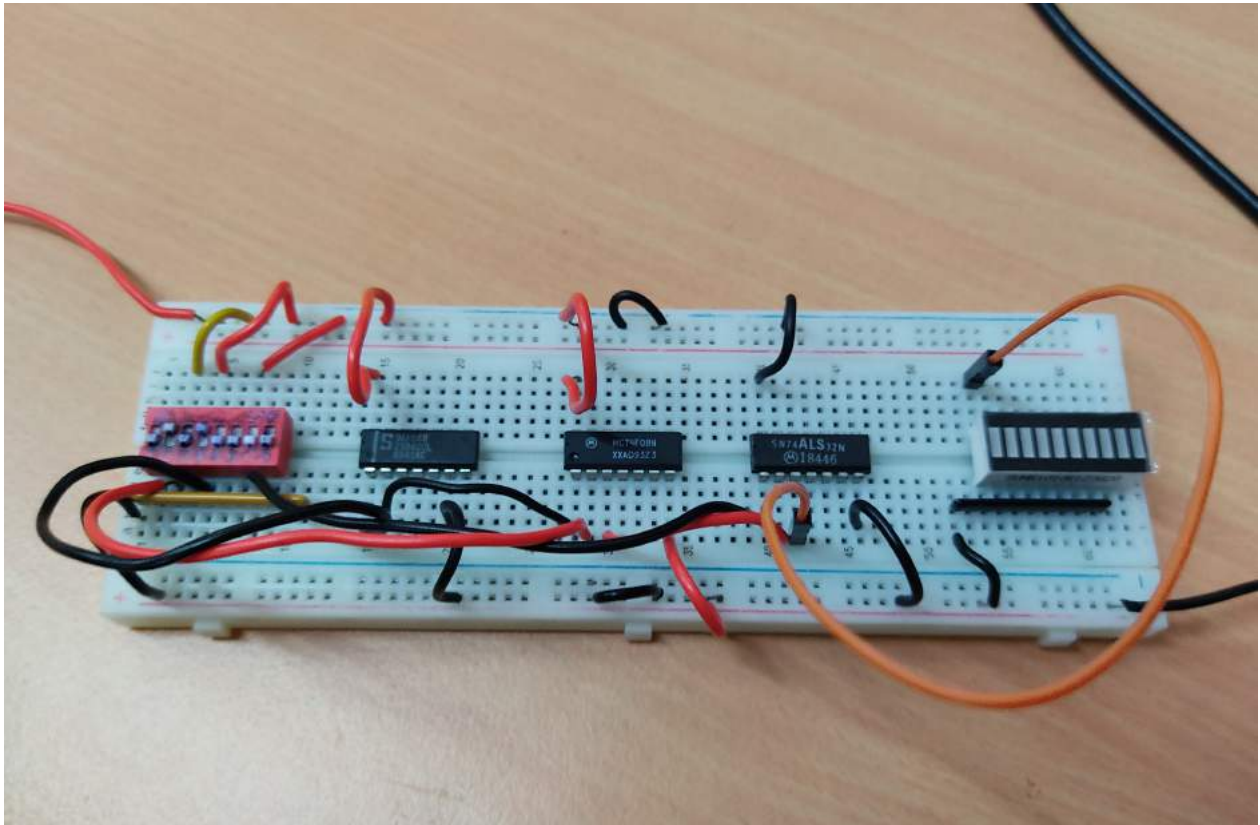
$0_1_1 \rightarrow 1$



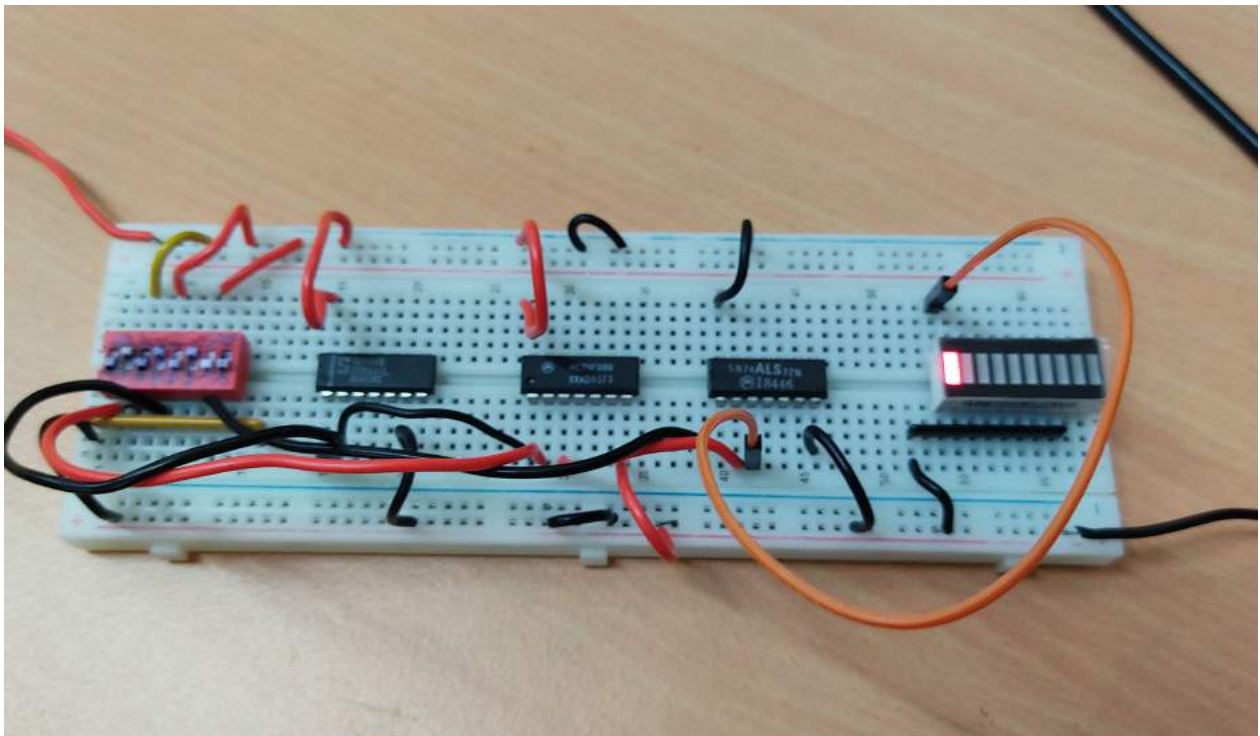
$0_0_1 \rightarrow 1$



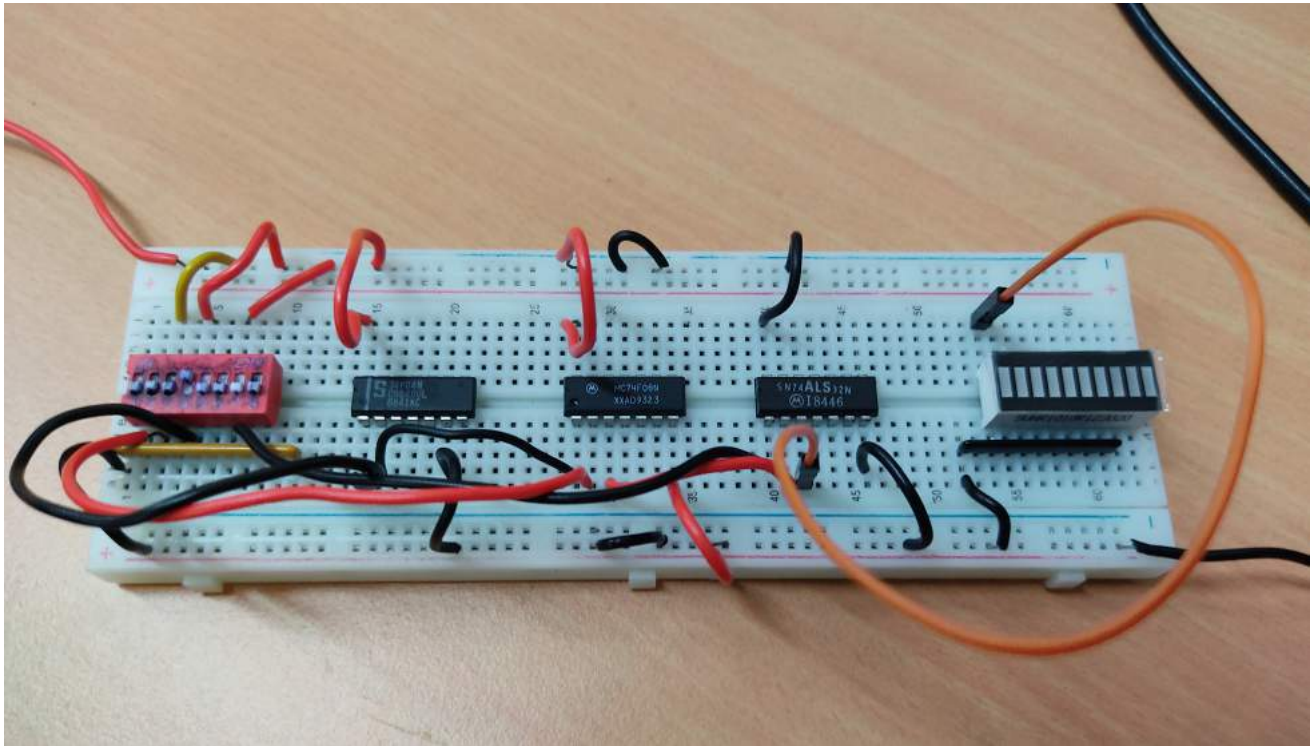
$1_0_1 \rightarrow 1$



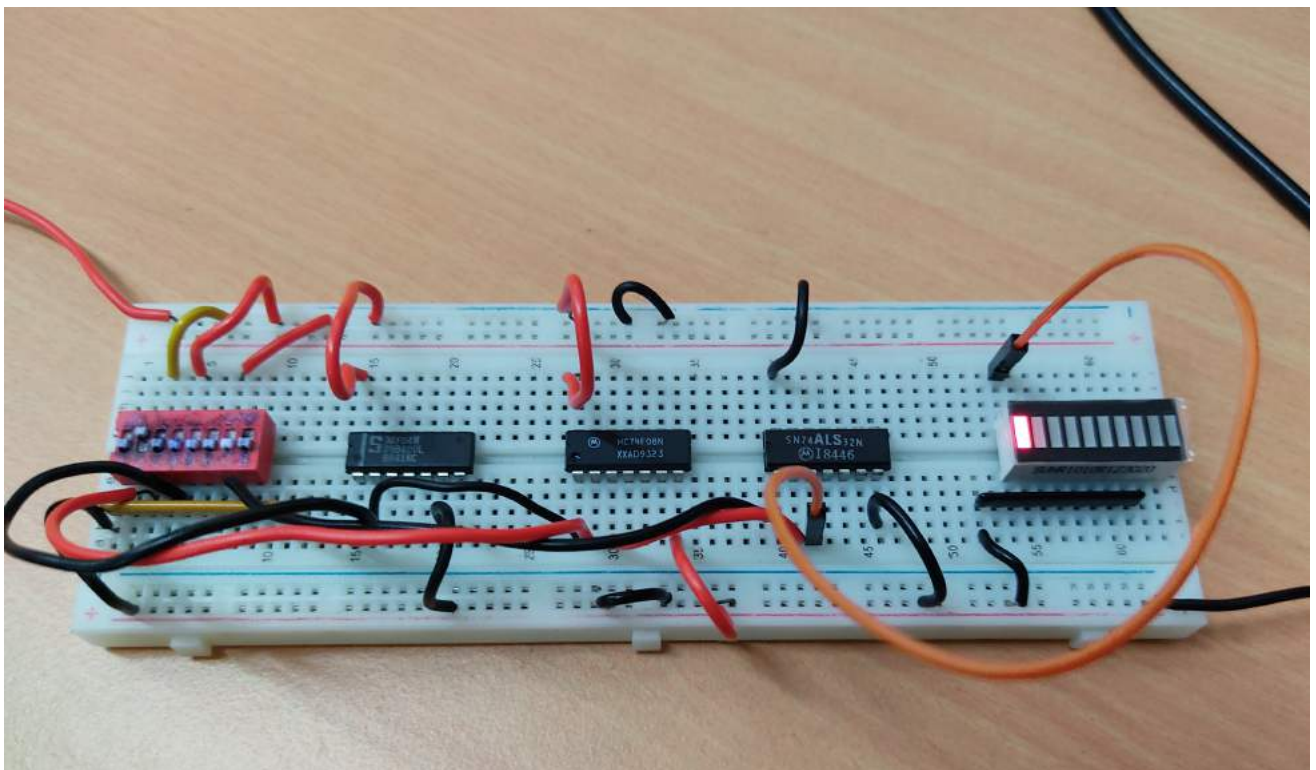
$1_1_0 \rightarrow 0$



$1_1_1 \rightarrow 1$

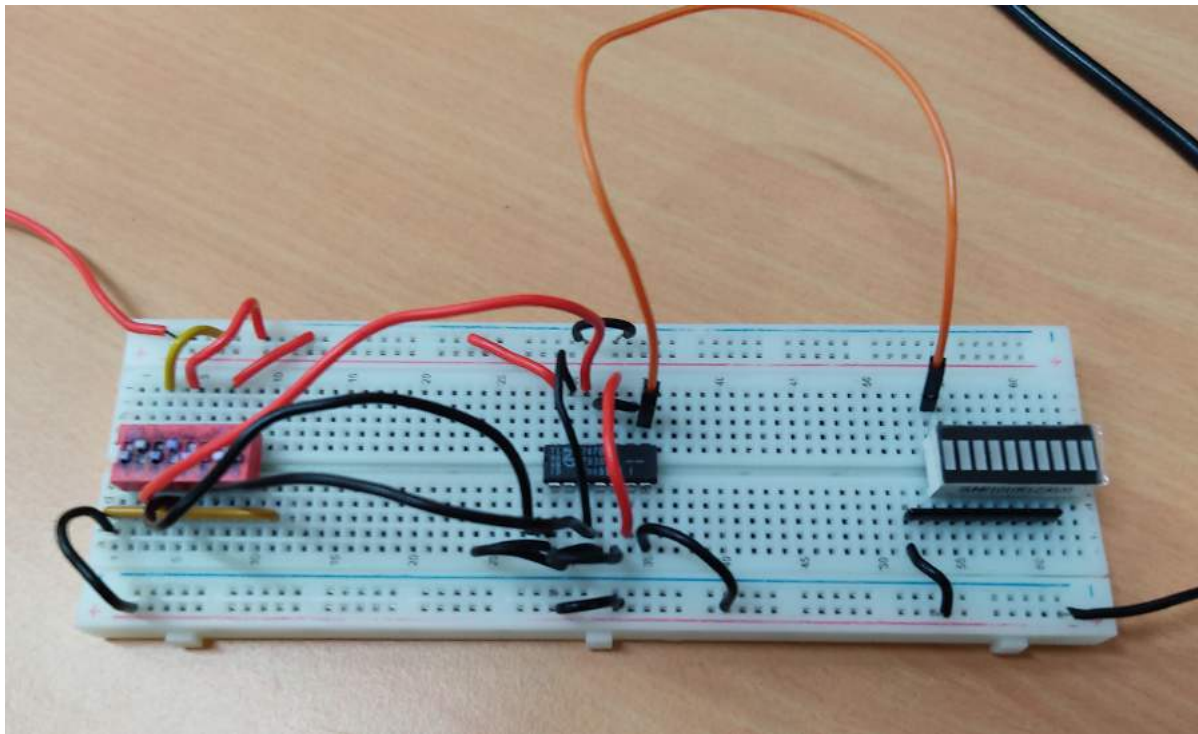


$0_1_0 \rightarrow 0$

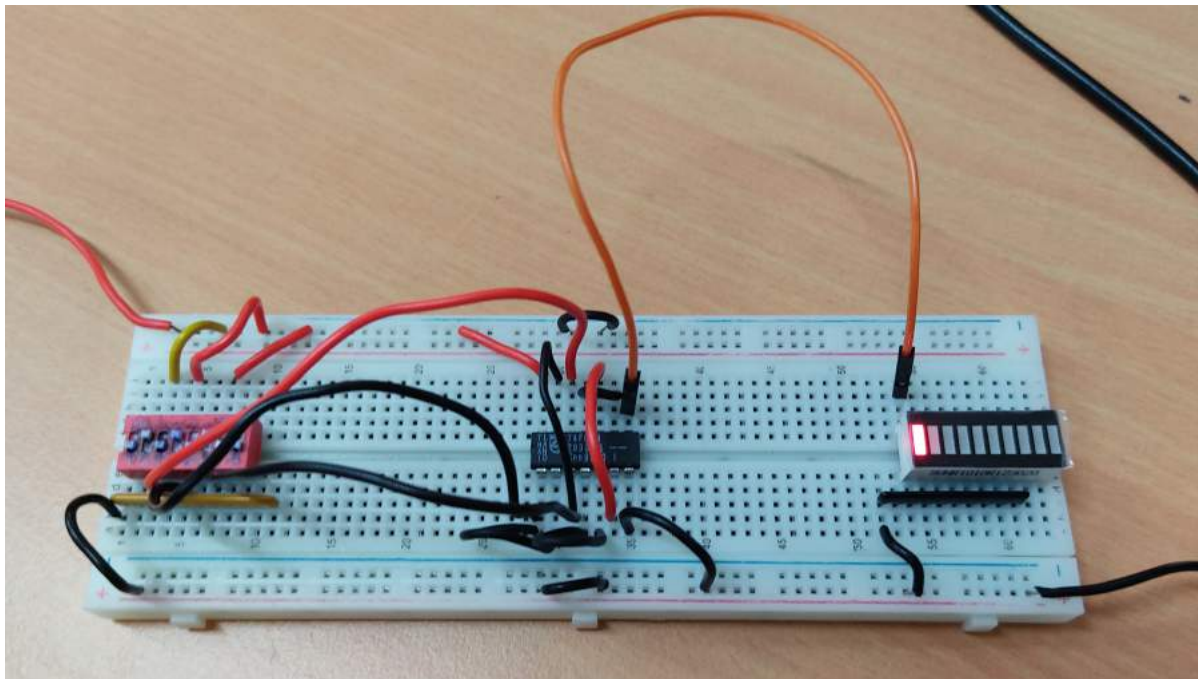


$1_0_0 \rightarrow 1$

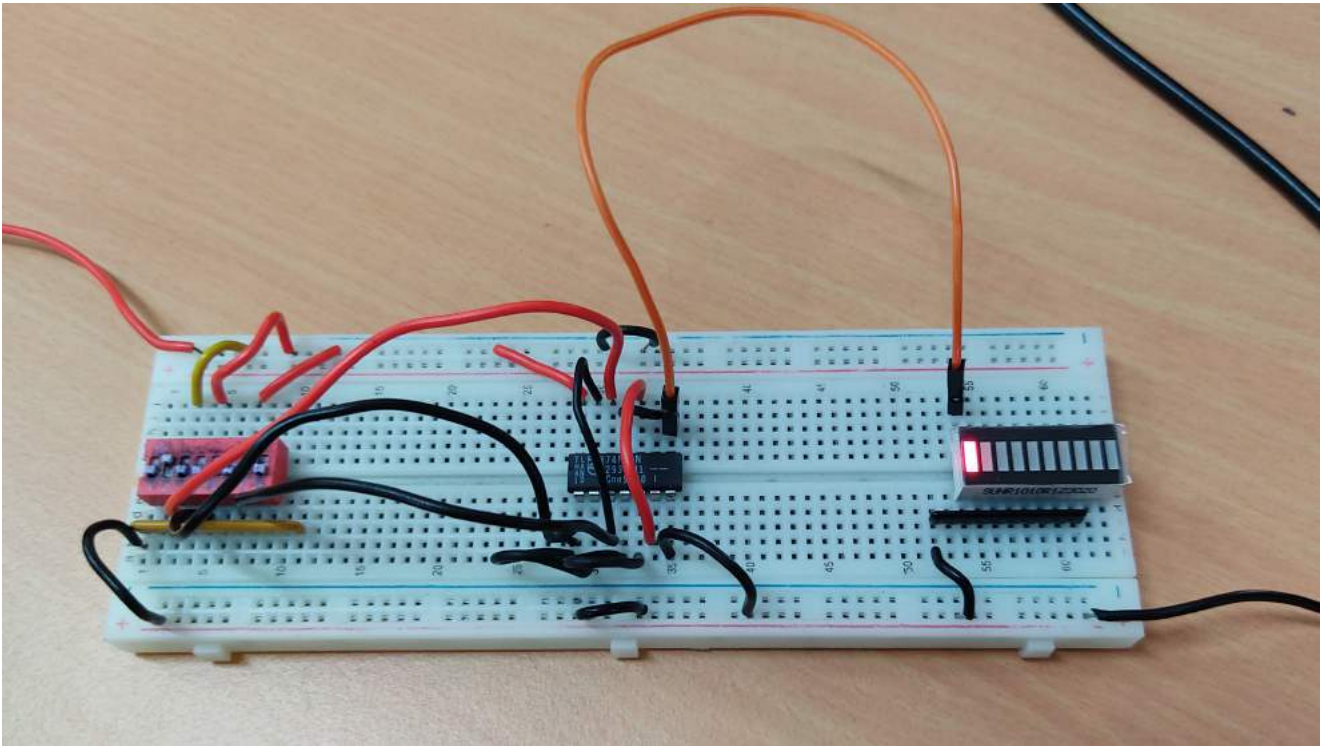
Implementation using NAND gate:



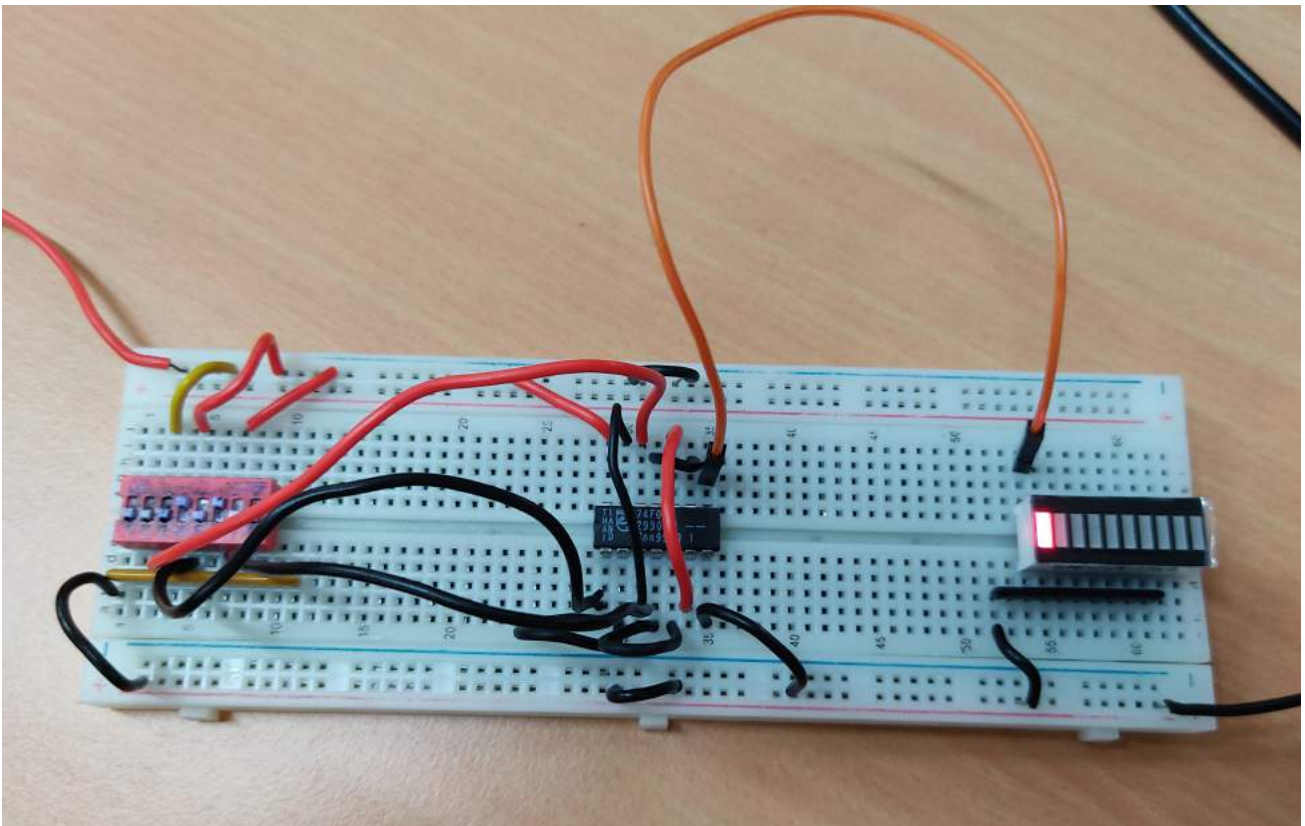
$1_1_0 \rightarrow 0$



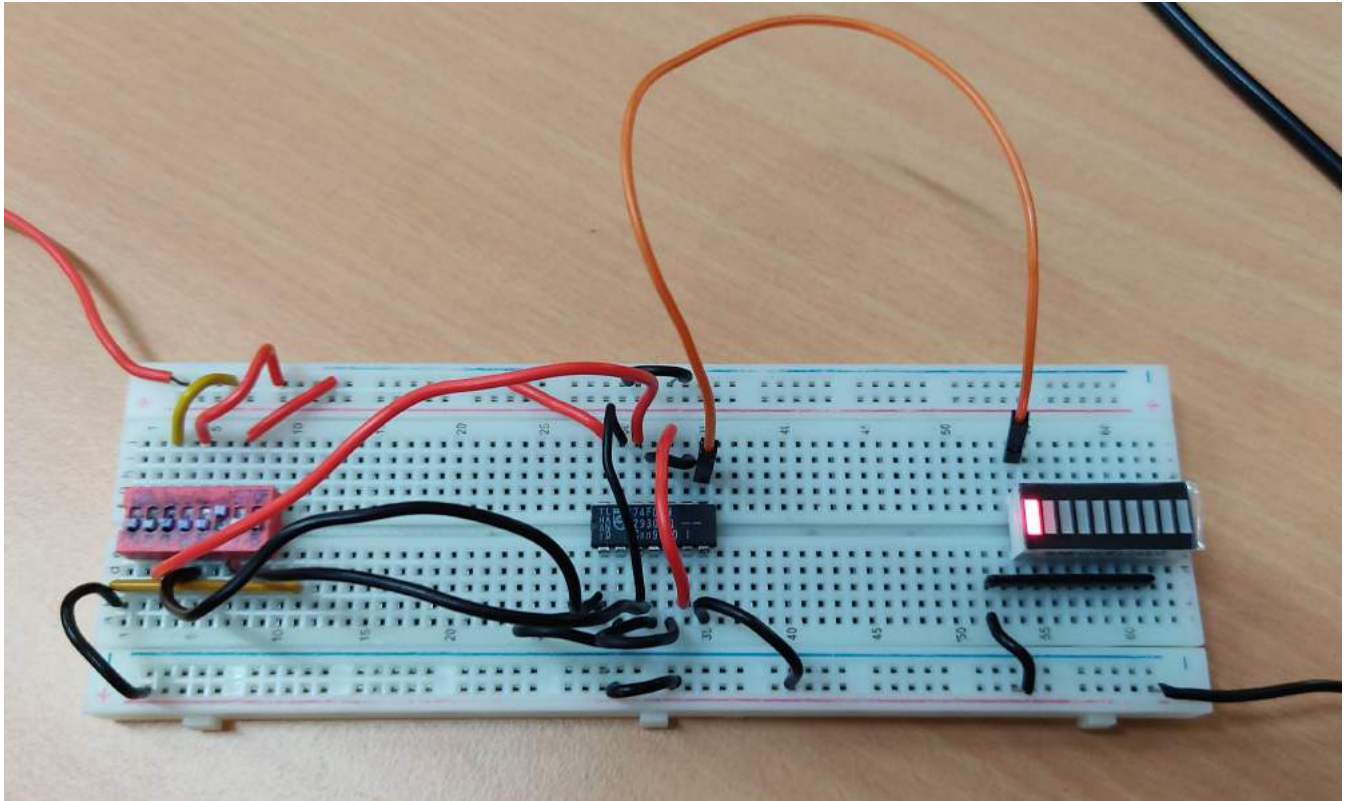
$1_1_1 \rightarrow 1$



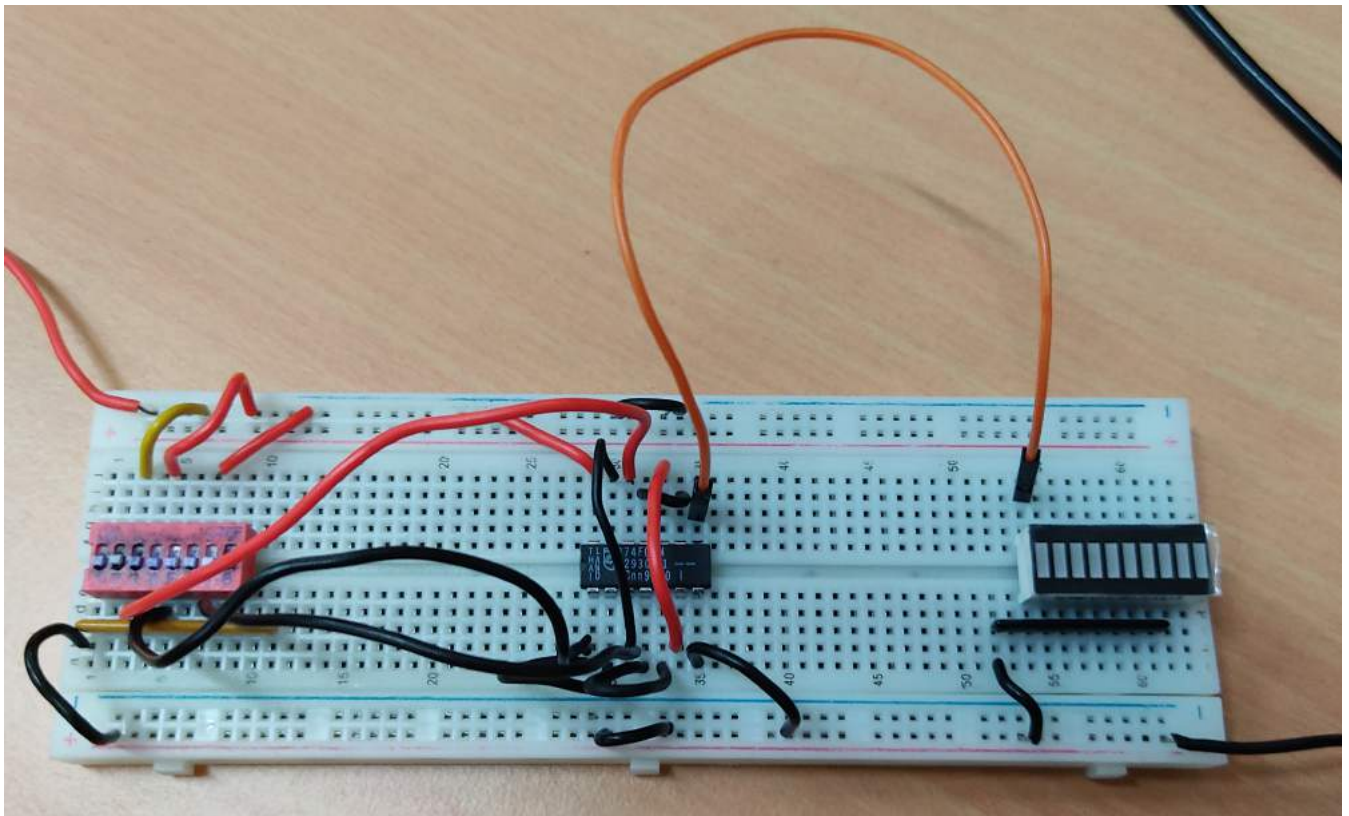
$1_0_0 \rightarrow 1$



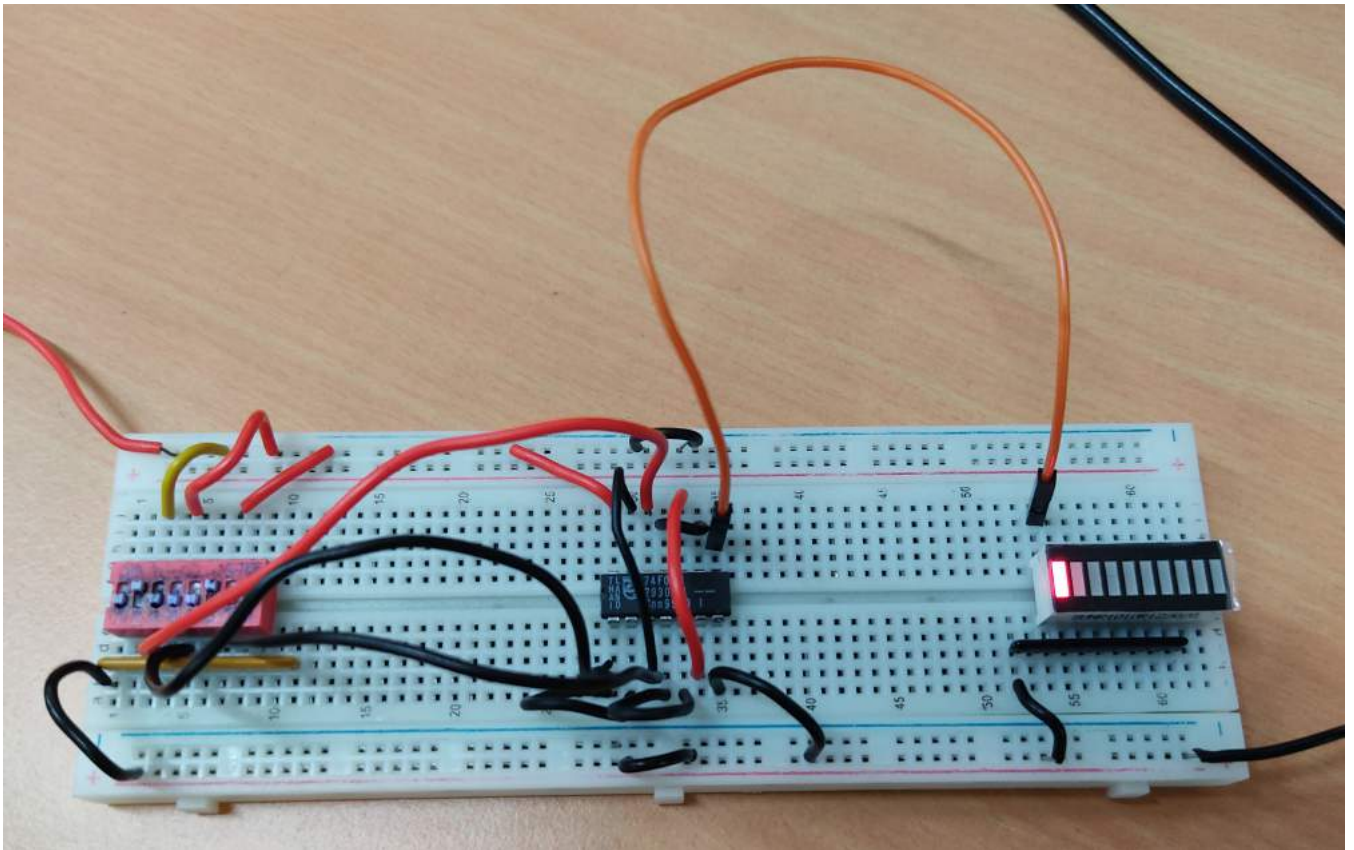
$0_1_1 \rightarrow 1$



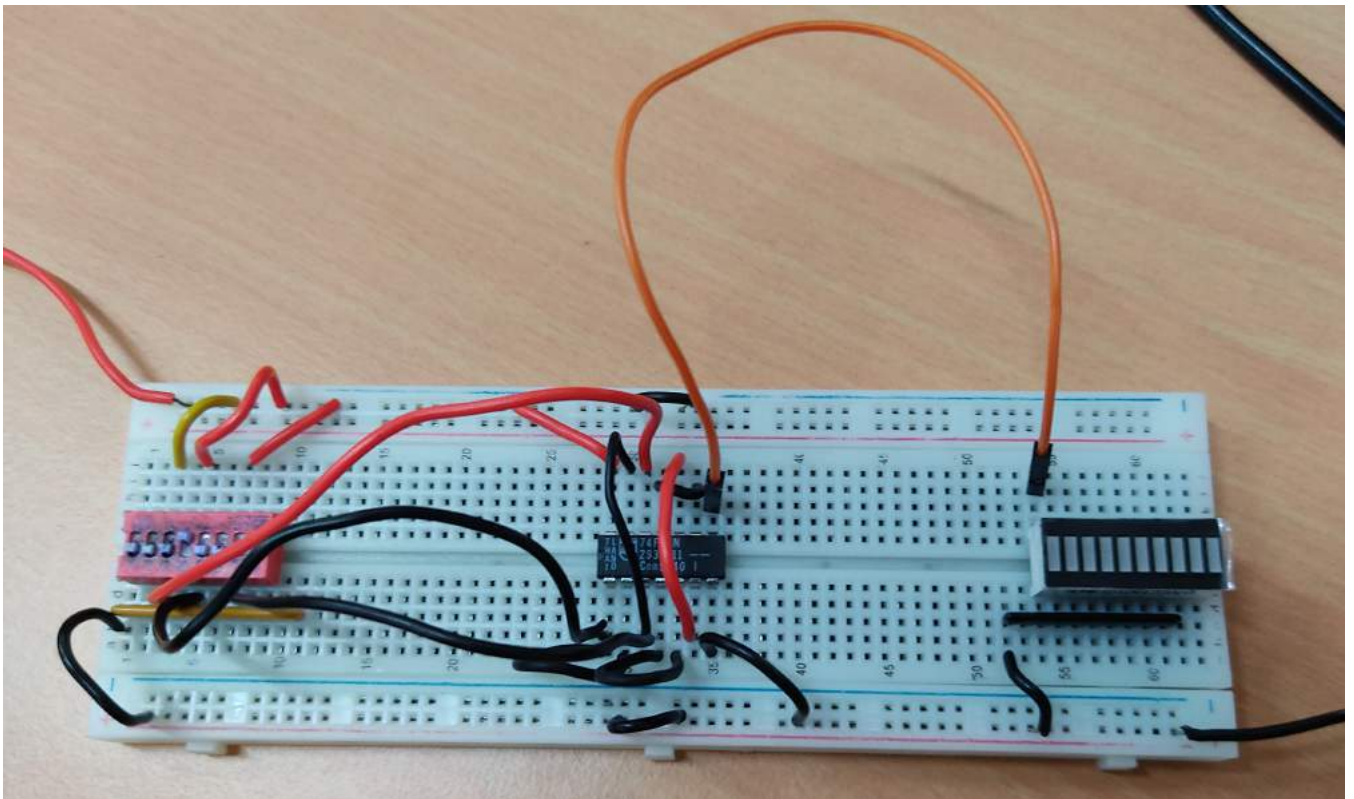
$0_0_1 \rightarrow 1$



$0_0_0 \rightarrow 0$



1_0_1 \rightarrow 1



0_1_0 \rightarrow 0