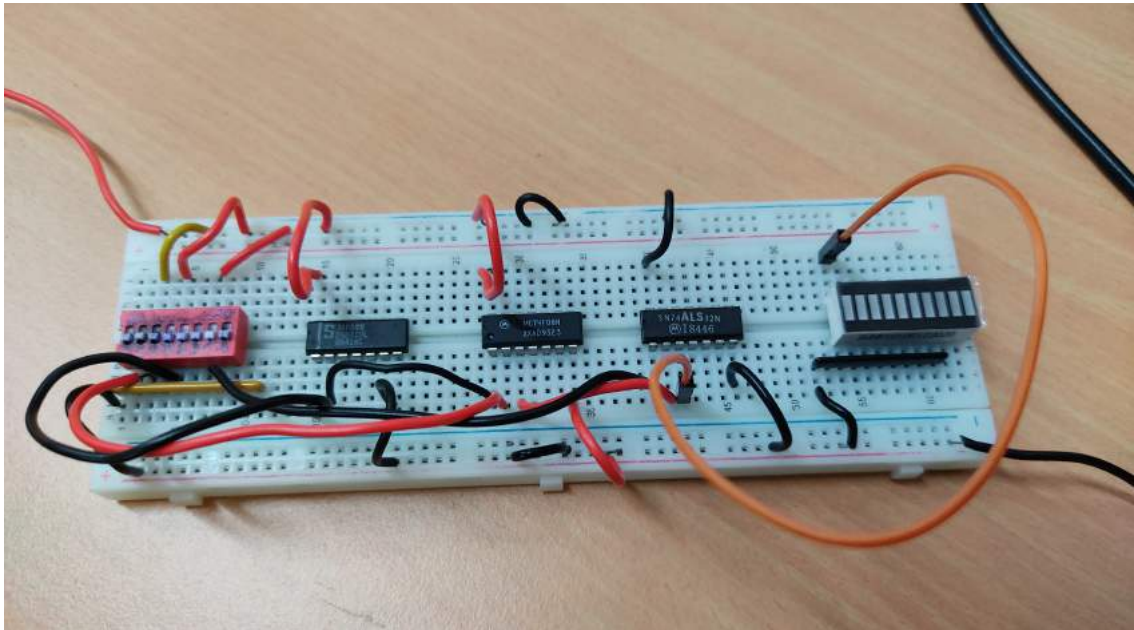
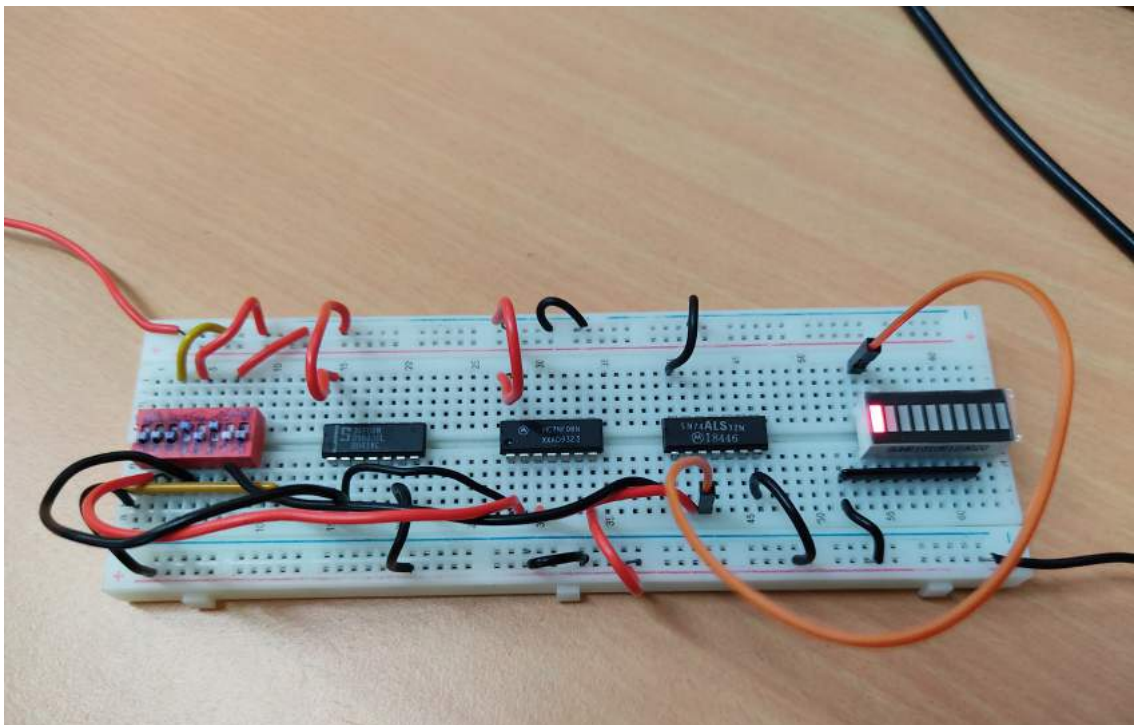


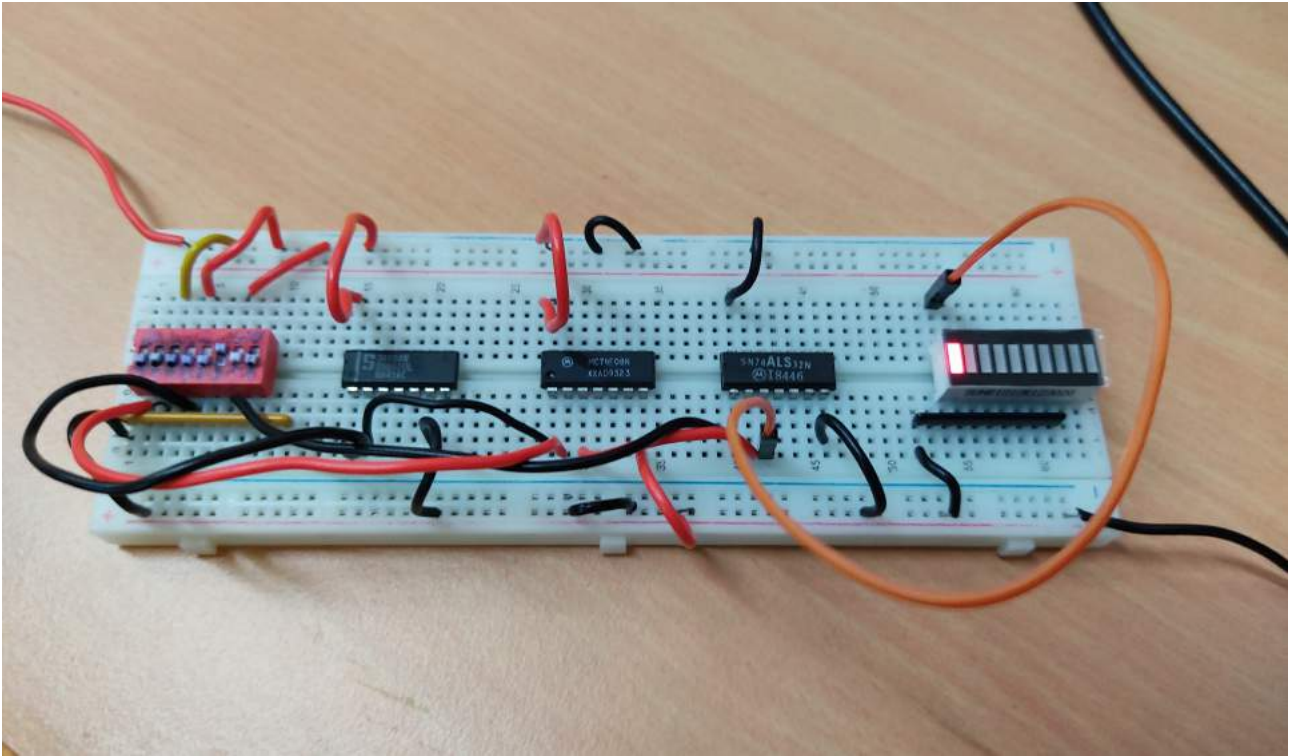
Implementation using Basic gates:



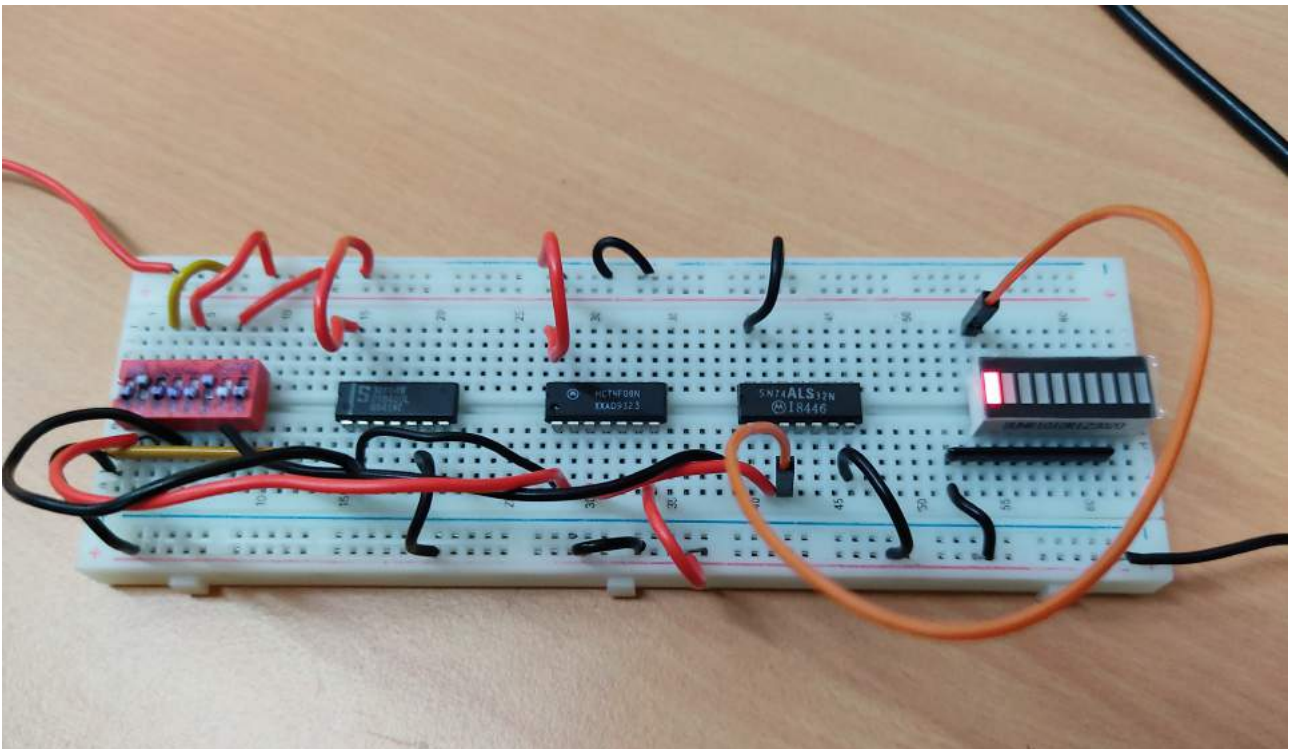
$0_0_0 \rightarrow 0$



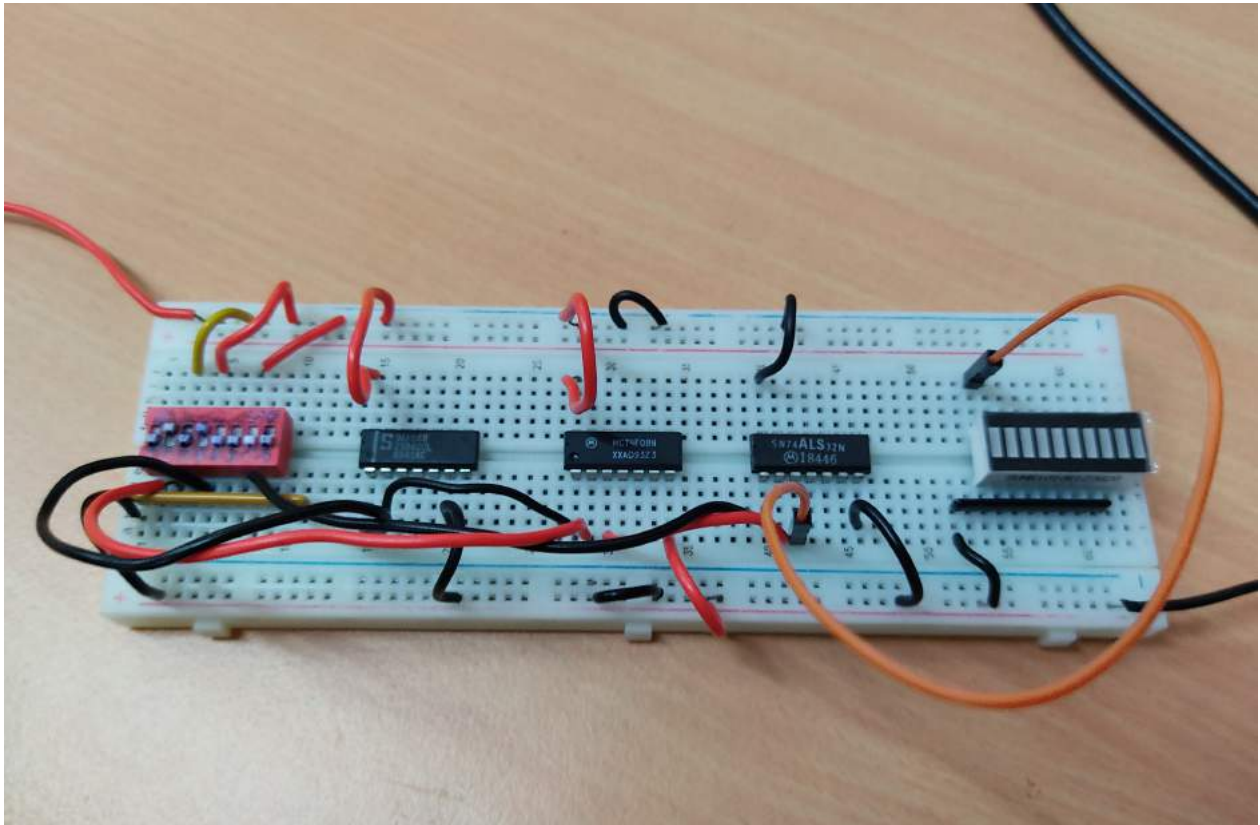
$0_1_1 \rightarrow 1$



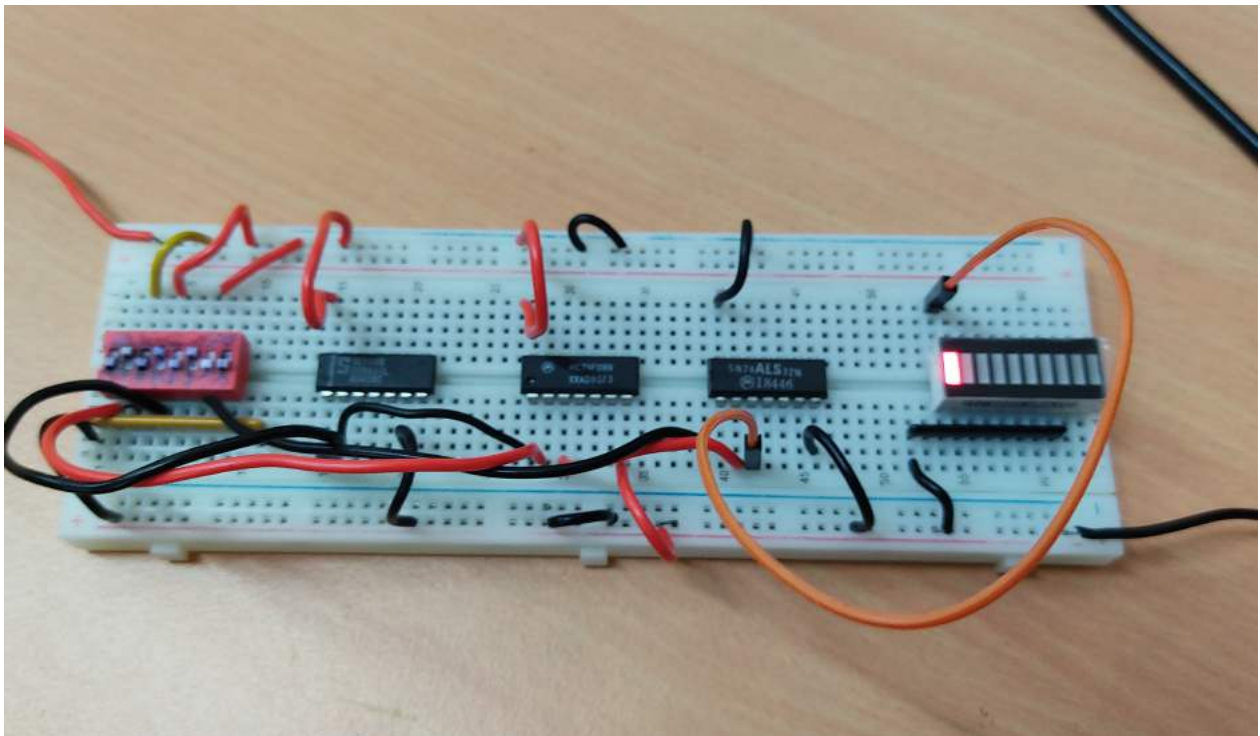
$0_0_1 \rightarrow 1$



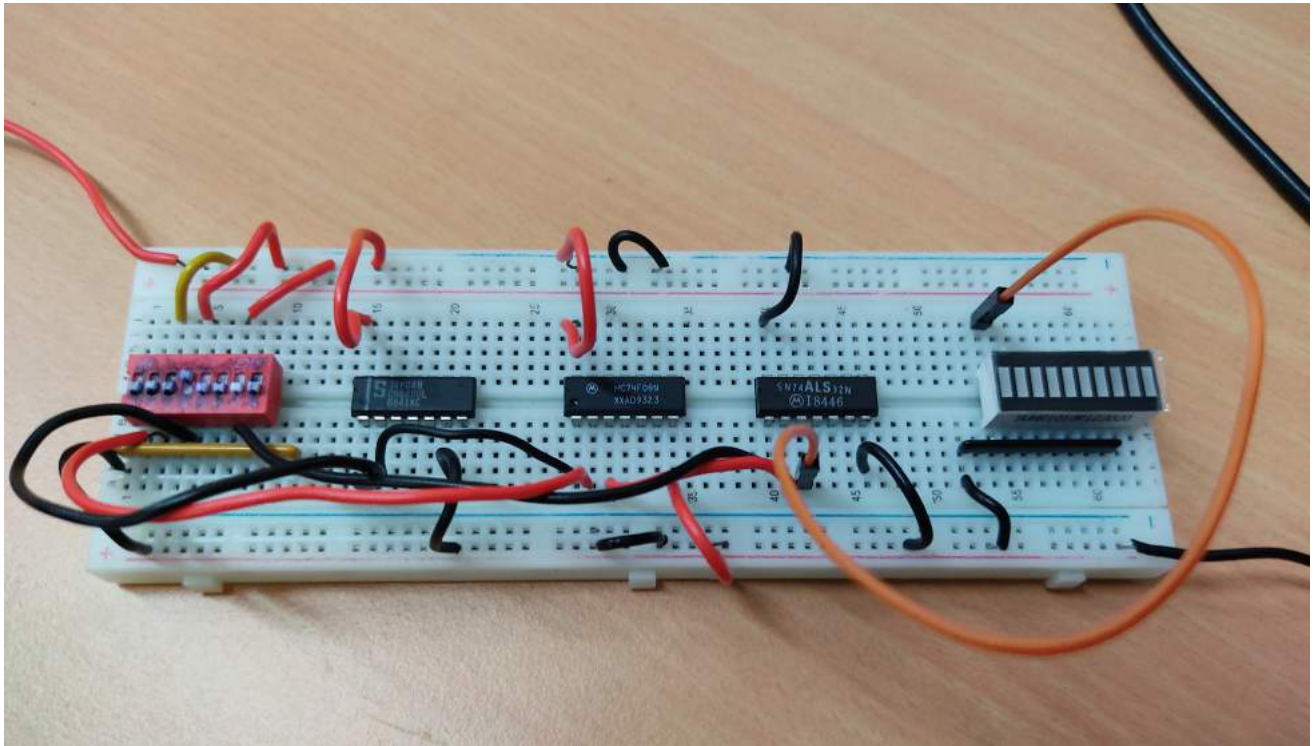
$1_0_1 \rightarrow 1$



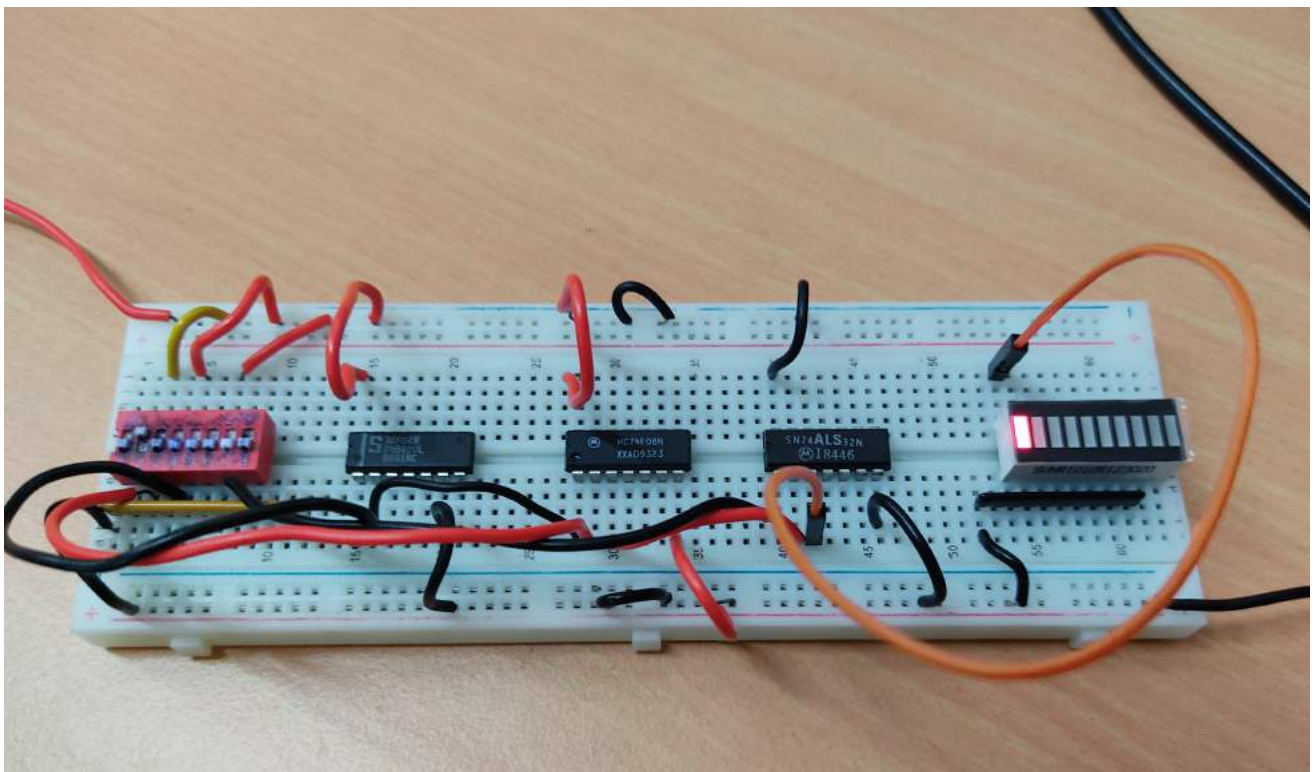
$1_1_0 \rightarrow 0$



$1_1_1 \rightarrow 1$

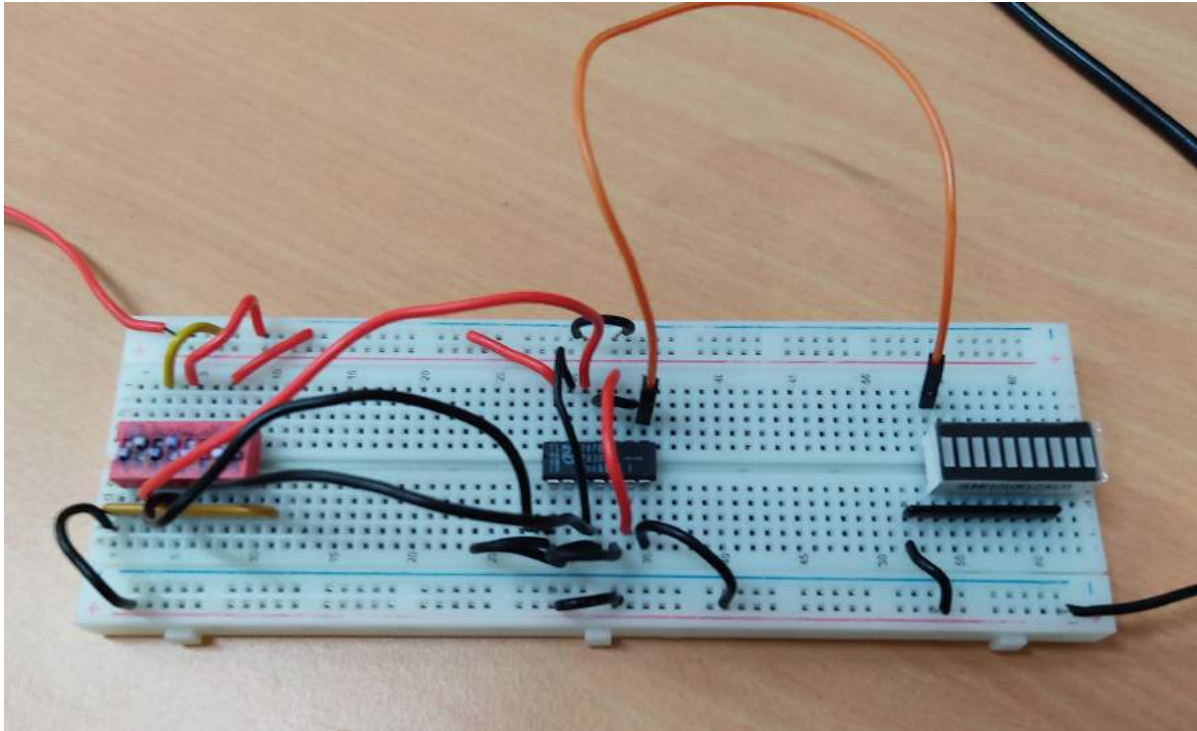


$0_1_0 \rightarrow 0$

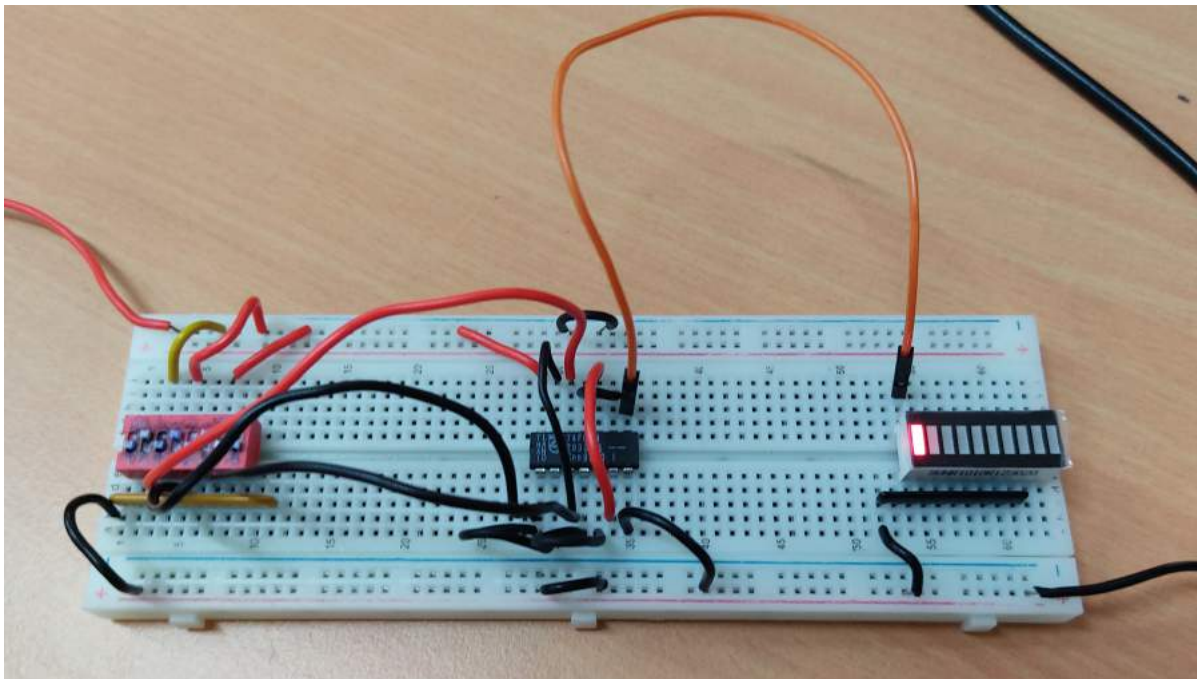


$1_0_0 \rightarrow 1$

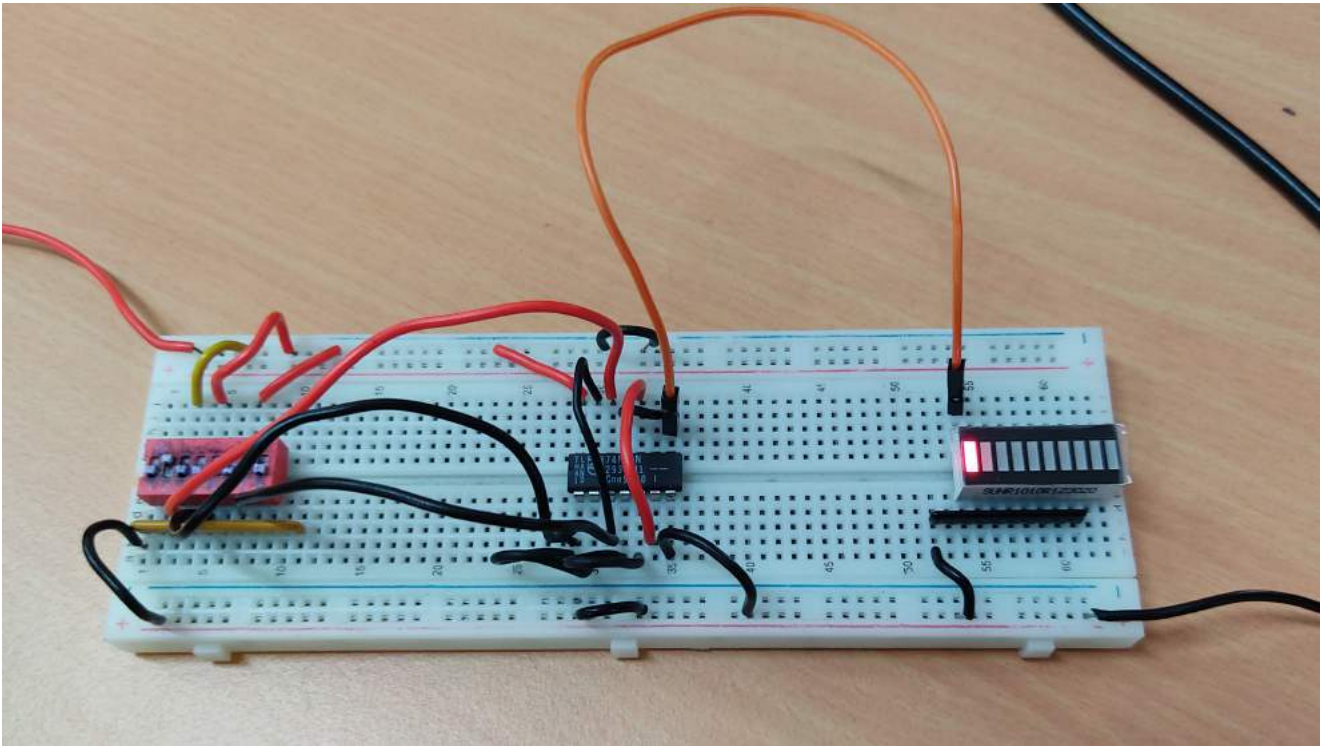
Implementation using NAND gate:



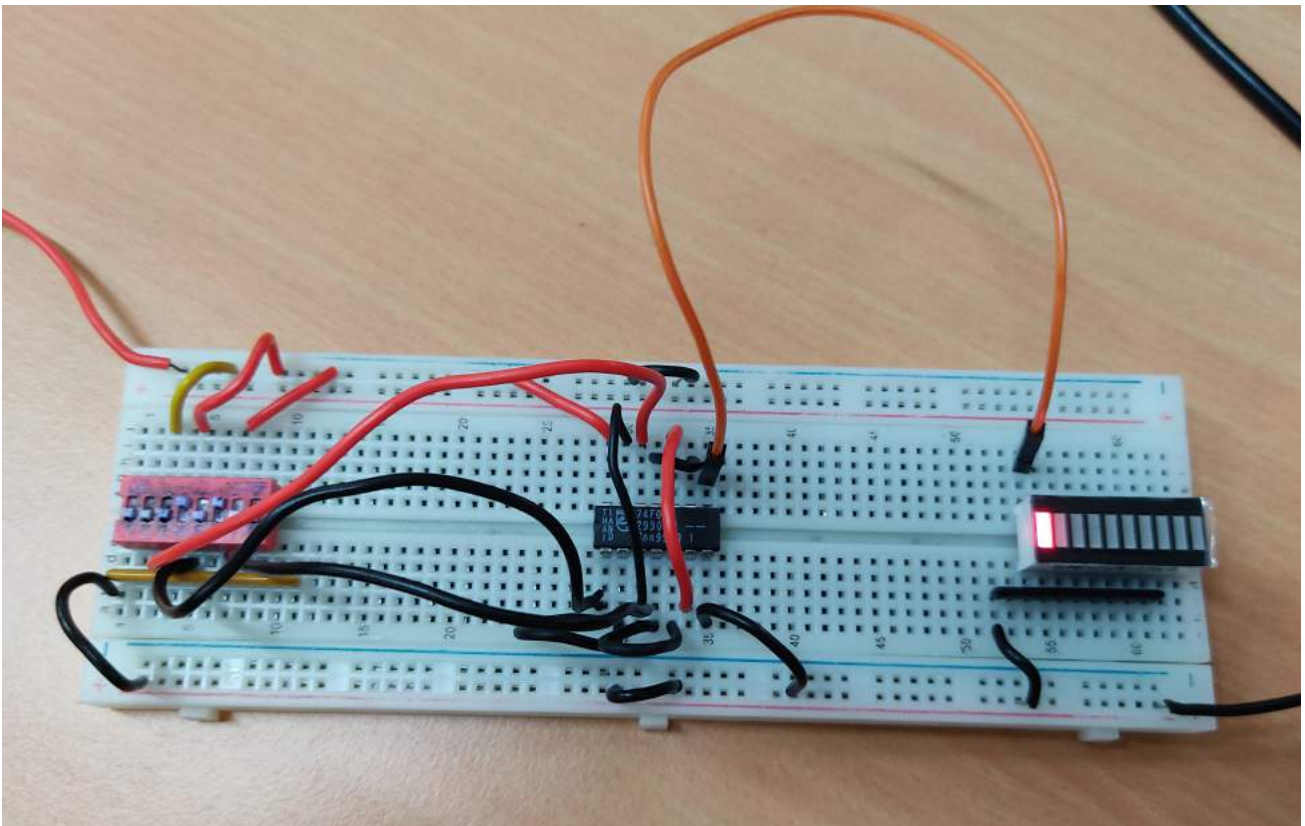
$1_1_0 \rightarrow 0$



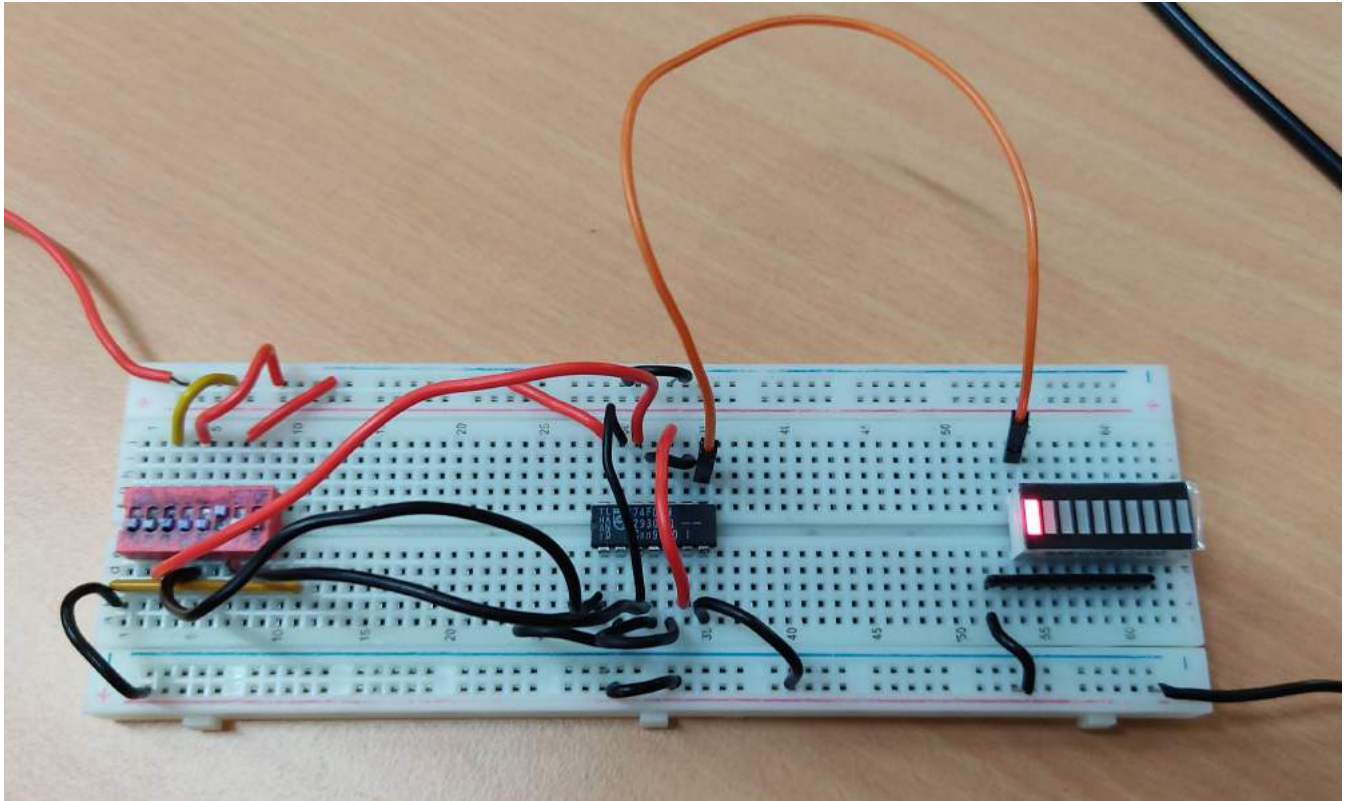
$1_1_1 \rightarrow 1$



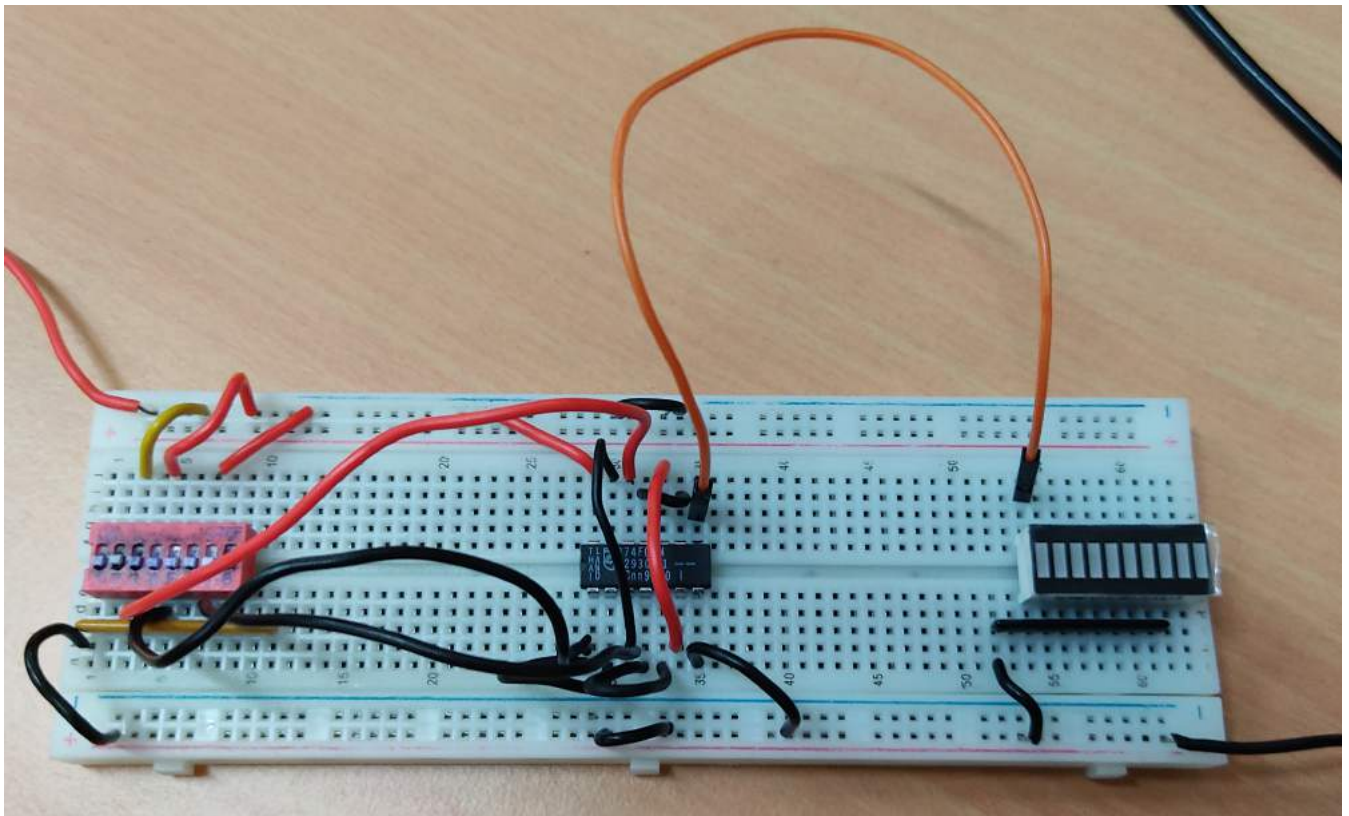
$1_0_0 \rightarrow 1$



$0_1_1 \rightarrow 1$



$0_0_1 \rightarrow 1$



$0_0_0 \rightarrow 0$

