Write clear logic and implement the following codes as per the instructions given

1) Write VHDL code for 3-bit adder/subtractor in structural modelling style. The adder/subtractor operation is controlled by signal 'm'.

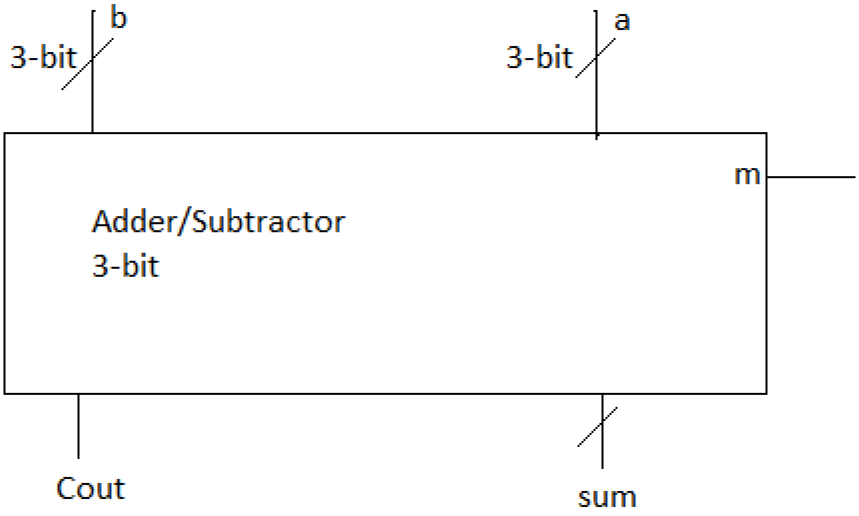

Figure: Representation of Adder-Subtrator circuit

m	**Operation**
0	a+b
1	a-b (2’s complement form)

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;--define the entity with ports
entity adsub_3bit is
port (a : in STD_LOGIC_VECTOR (2 downto 0);
b : in STD_LOGIC_VECTOR (2 downto 0);
m : in STD_LOGIC;
sum :out STD_LOGIC_VECTOR (2 downto 0);
cout : out STD_LOGIC);
end adsub_3bit;

-----DEFINE THE ARCHITECTURE FOR ADDER_SUBTRACTOR
architecture rtl of adsub_3bit is
```

```
--DEFINE THE COMPONENT FULL ADDER USED-----
/**** Write code here ****/
--DEFINE THE INTERMEDIATE SIGNALS IF REQUIRED----
/**** Write code here ****/

-----DEFINE THE FUNCTIONALITY WITH STRUCTURAL MODELING
/**** Write code here ****/
end rtl;
```

--VHDL CODE FOR 1 bit full adder in dataflow must be written in same VHDL file-----

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
--Define input and output ports–
entity fulladder is
port(i1, i2, i3: in bit;
     o1, o2 : out bit);
end fulladder;
--Defining the architecture of full adder in dataflow modelling style—-
architecture b_fa of fulladder is
Begin
o1 <= i1 xor i2 xor i3;
o2 <= (i1 and i2) or ((i1 xor i2) and i3);
end b_fa;
```

—--

2) Write VHDL code for ALU which performs following operation depending on selection lines

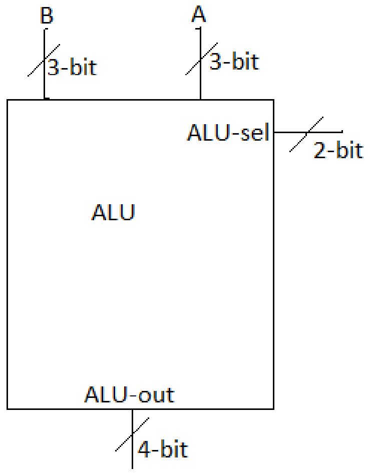

Figure: Representation of ALU based on 2-bit selector line

ALU selector line 1	ALU selector line 2	Operation selected
0	0	A + B
0	1	A - B
1	0	A bitwise and B
1	1	A bitwise xor B

---3 -bit ALU using behavioral modeling ---

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
use ieee.NUMERIC_STD.all;
entity ALU is
Port ( A, B : in STD_LOGIC_VECTOR(2 downto 0); -- 2 inputs 8-bit
          ALU_Sel : in STD_LOGIC_VECTOR(1 downto 0);
          ALU_Out : out STD_LOGIC_VECTOR(3 downto 0));
 end ALU;
/**** Write code here ****/
architecture Behavioral of ALU is
end Behavioral;
----------------------------------------------------------------
-------------------------------
```

3) Write VHDL code for 4:2 priority encodes with active high enable pin

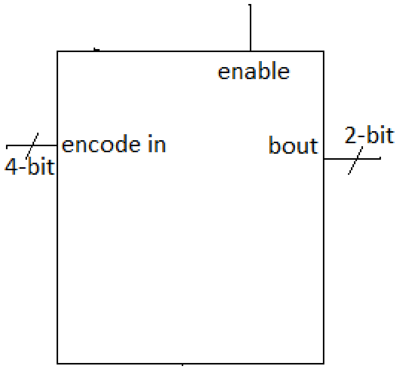

Figure: Representation of Priority encoder

enable	in_0	in_1	in_2	in_3	out_0	out_1
0	X	X	X	X	0	0
1	1	X	X	X	0	0
1	0	1	X	X	0	1
1	0	0	1	X	1	0
1	0	0	0	1	1	1

---------------VHDL CODE FOR 4:2 PRIORITY ENCODER-----

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

-------------port declaration---------------------
entity pri_encoder is
port( encoder_in : in STD_LOGIC_VECTOR(0 downto 3);
 bin_out : out STD_LOGIC_VECTOR(1 downto 0);
enable : in STD_LOGIC );
end pri_encoder;

---------- architecture----------------------
```

```
architecture behavioral of pri_encoder is
/**** Write code here ****/
end behavioral;
```