

CSE batch

- 1) Design and implement a mod-8 asynchronous down counter. Clearly indicate the minimum number of JK Flip-flops required (if any) and NAND gates required (if any).
- 2) Design and implement a mod-5 asynchronous down counter. Clearly indicate the minimum number of JK Flip-flops required (if any) and NAND gates required (if any).