Lab 9

EE214: Digital Circuits Laboratory

B. Siddharth Prabhu
Roll No. 200010003

25 February 2022

1 Aim

Design of a circuit for 4 bit universal shift register, (controlled by a 2 bit control input) that performs the required operation.

2 Summary of the experiment

Design of a 4-bit Universal Shift Register using D-Type Flip-Flops and 4-to-1 Multiplexers, then conducting its implementation on the breadboard. Then, testing and verification of the control input and given operations.

3 Components Used

IC 7474 (D-Type Flip-Flop), IC 74153 (4-to-1 Multiplexer), 1 kilo-ohm resistor array, DIP switches, LED displays, breadboard, conducting wires, power supply.

4 Design Procedure

Input A	Input B	Operation
1	1	Parallel Loading
1	0	Left Shift
0	1	Right Shift
0	0	No Change

Table 1: Operations performed by Universal Shift Register

Note: Circuit Diagram is included with the snapshots.

5 Circuit and Simulation Snapshots

(Circuit snapshots are included in the later pages of this report.)

6 Results and Discussions

- We designed the circuit for a 4-bit Universal Shift Register using D-Type Flip-Flops and 4-to-1 Multiplexers; by first designing the same for 2-bits, then "concatenating" them.
- Before connecting the pins of the chips, one must number them in a hand-drawn circuit so as to ensure systematic and clean circuitry.
- The clock signal should be drawn from the function generator, and should preferably have a peak-to-peak voltage of 5V. The frequency should be about 1Hz, for better observability.
- We must design a circuit in such a manner that testing and debugging goes smoothly.

7 Conclusion

We designed and implemented a 4-bit Universal Shift Register, and then verified the outputs by loading all 1's, then shifting left/right.

DESIGN PROCEDURE

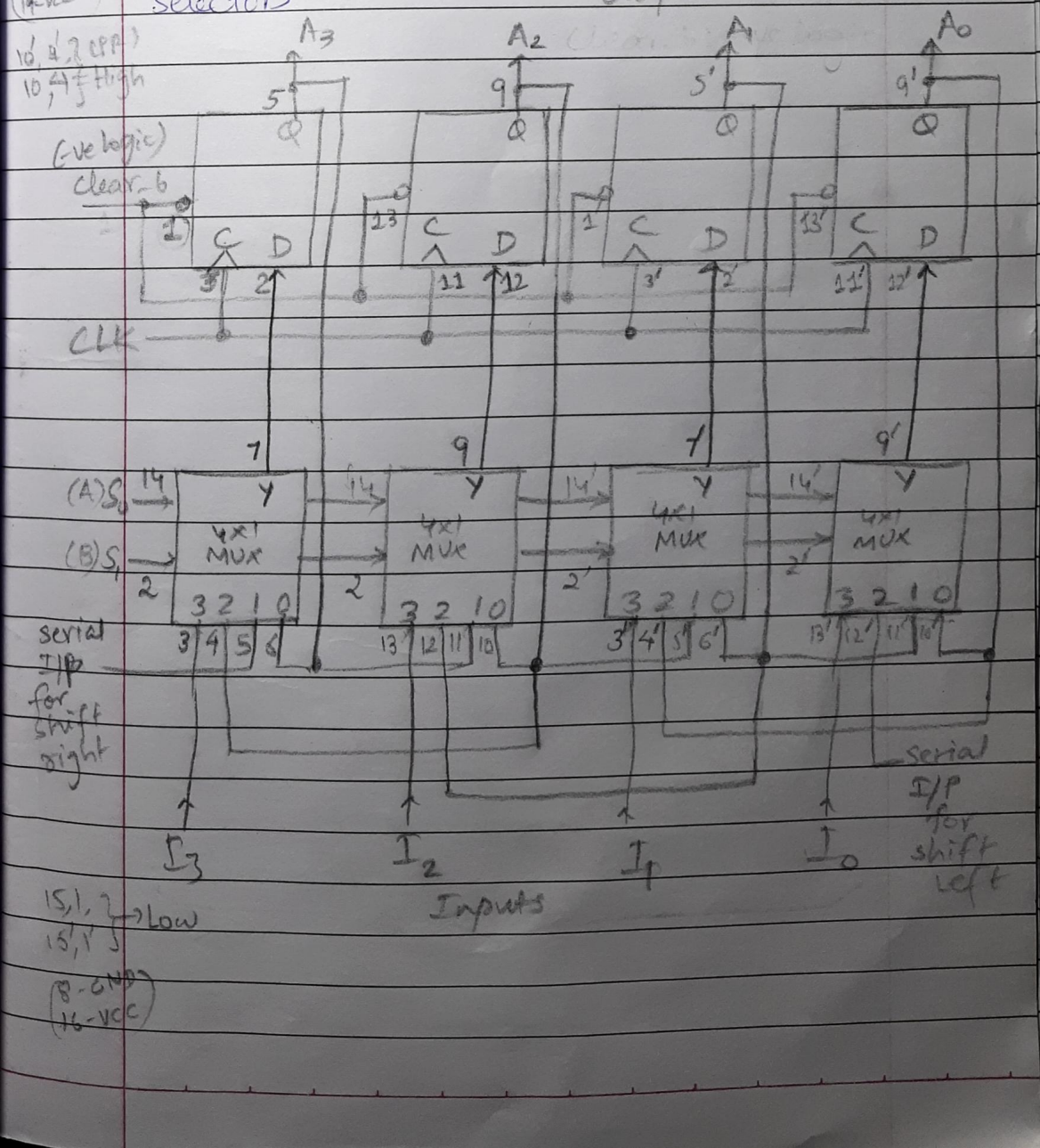
Page No.
Date

UNIVERSAL SHIFT REGISTER

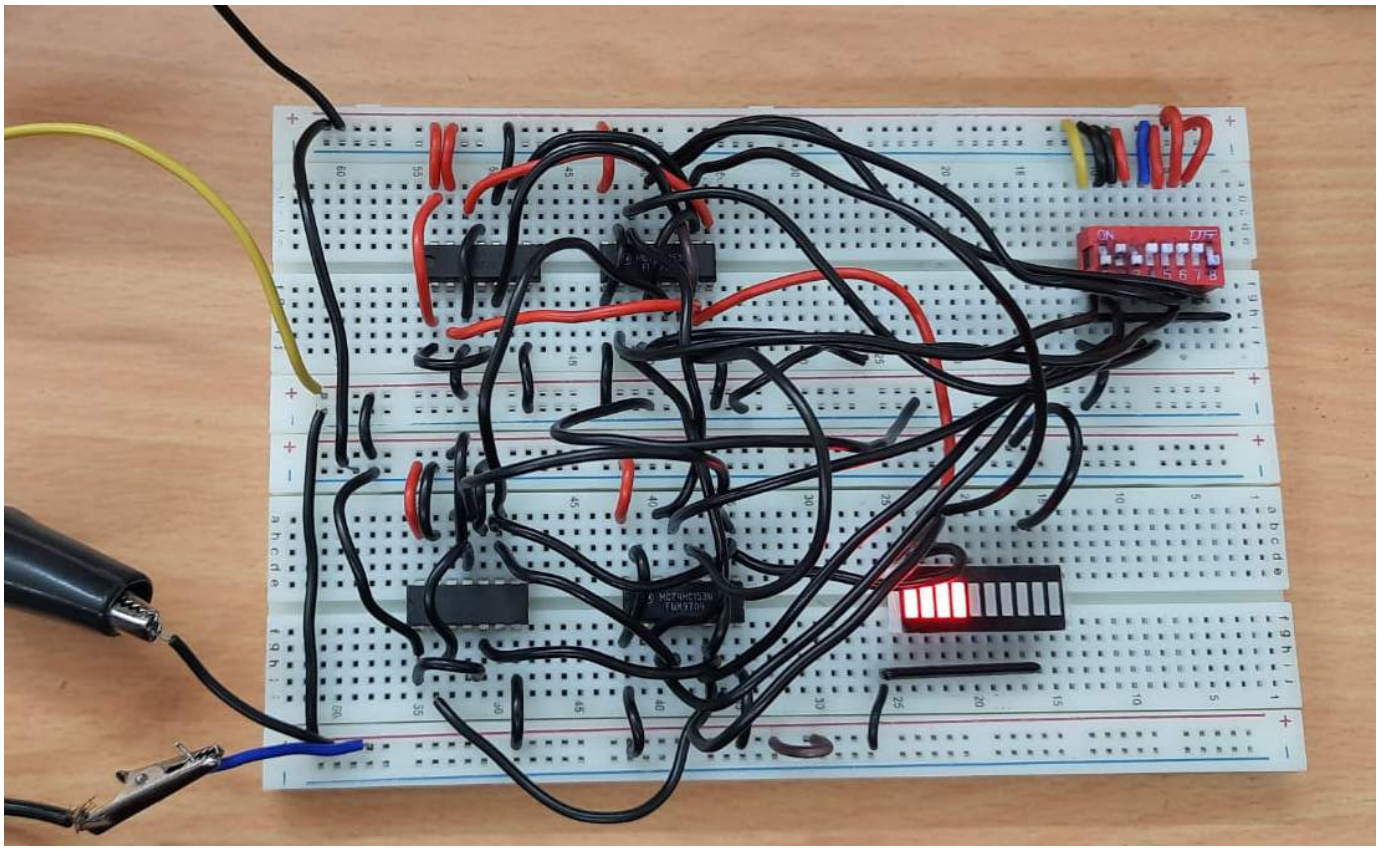
Input		operation
A (S_0)	B (S_1)	
1	1	Parallel Loading
1	0	Left Shift
0	1	Right Shift
0	0	No change

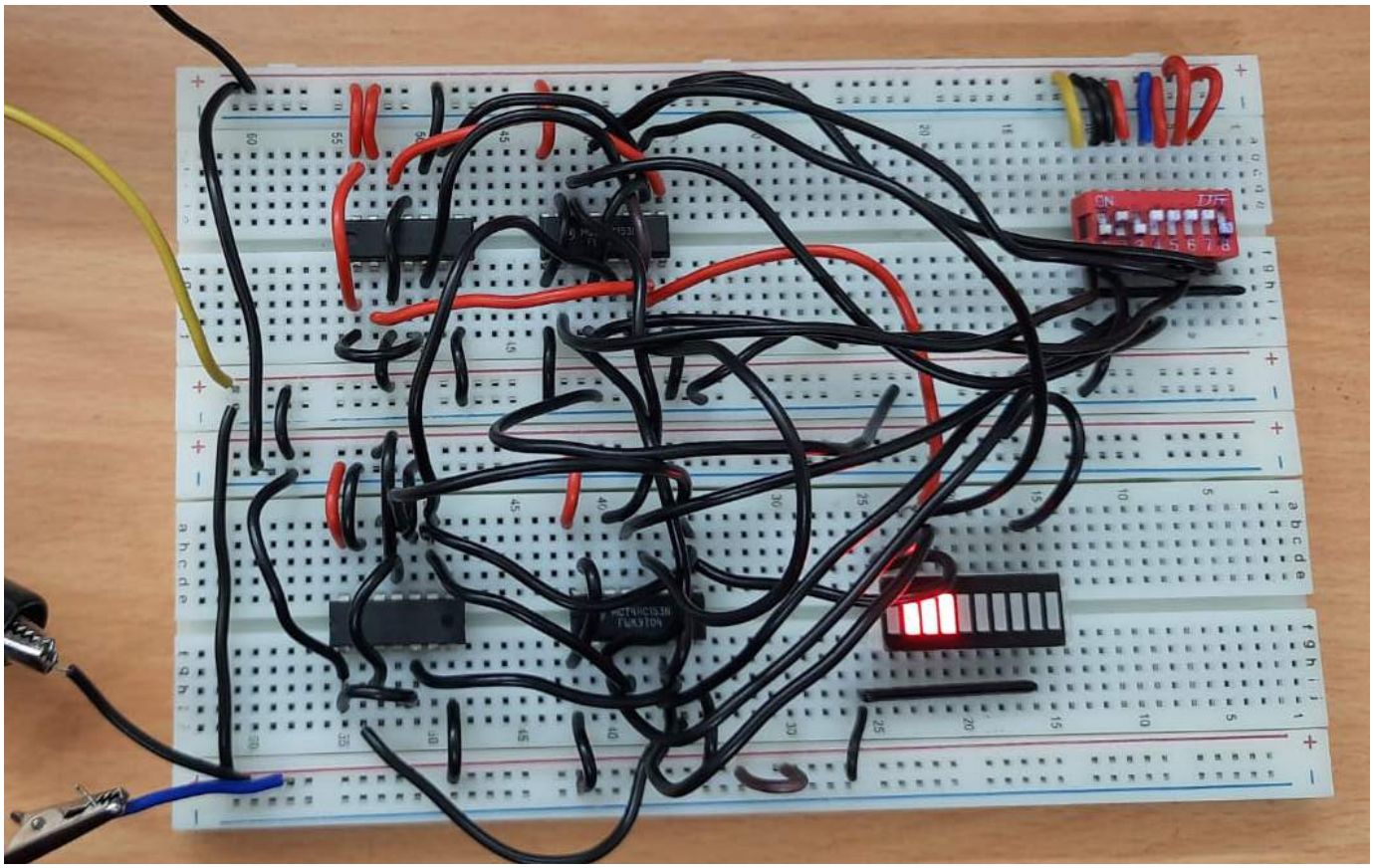
Selectors

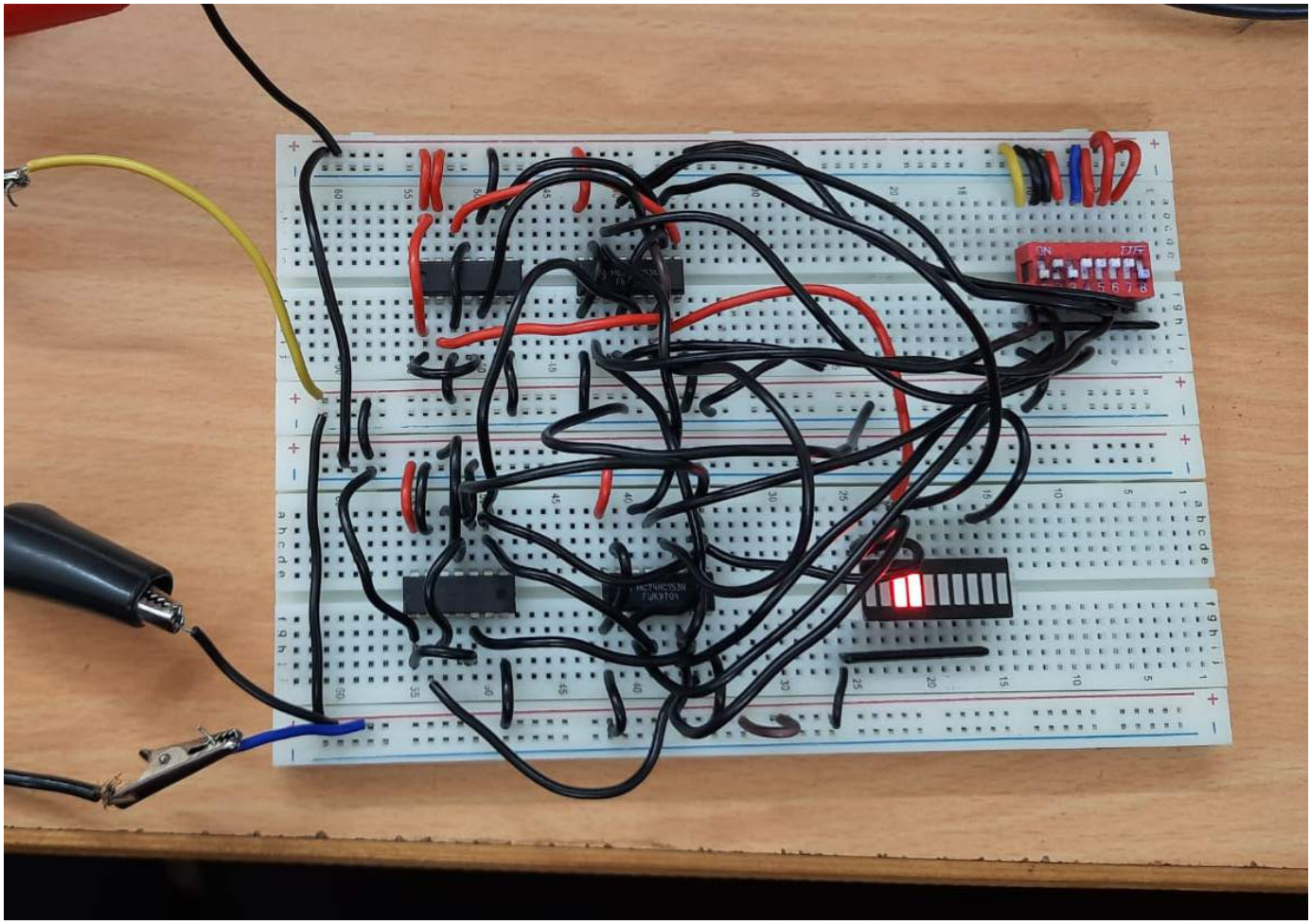
Outputs.

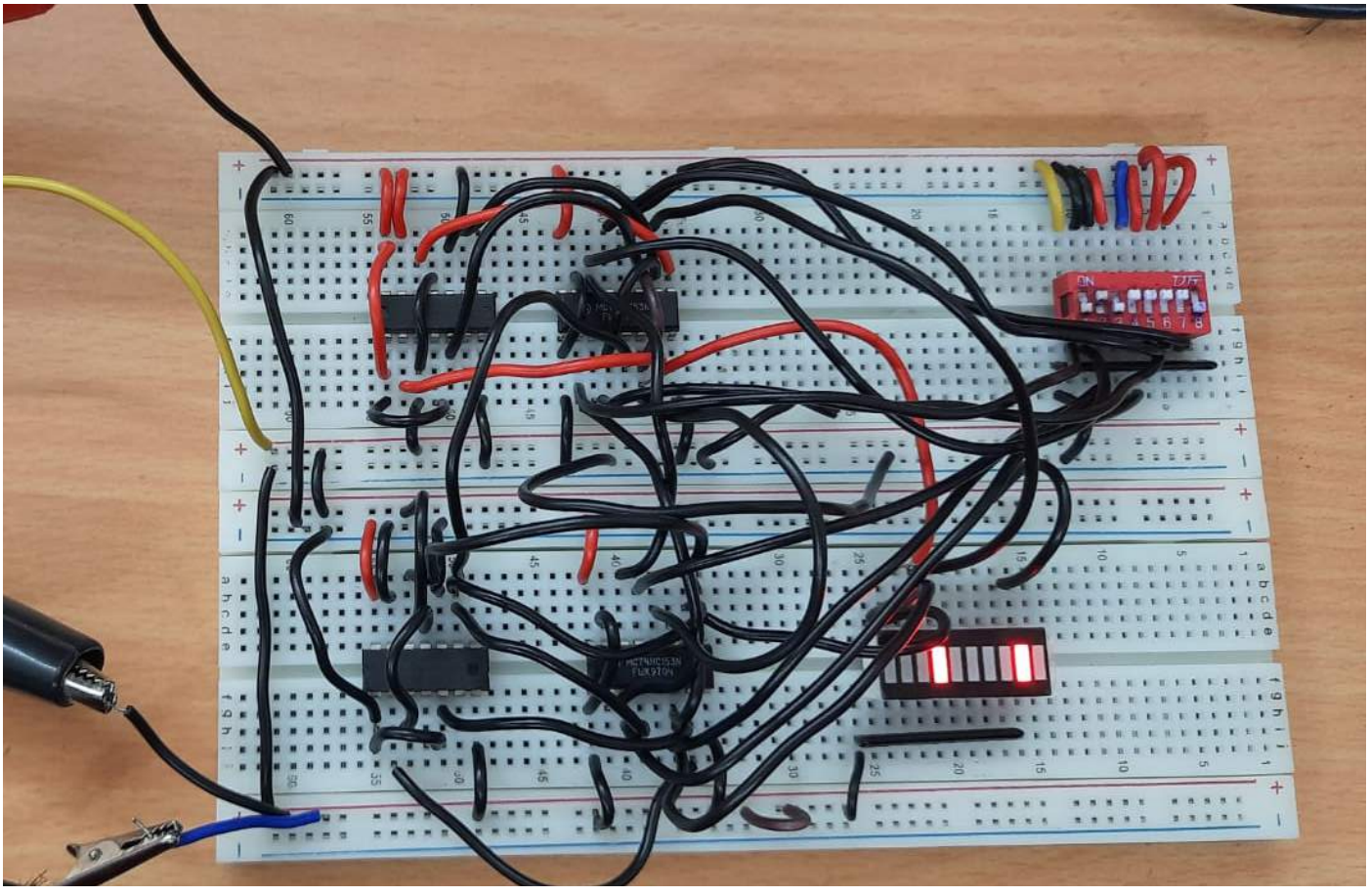


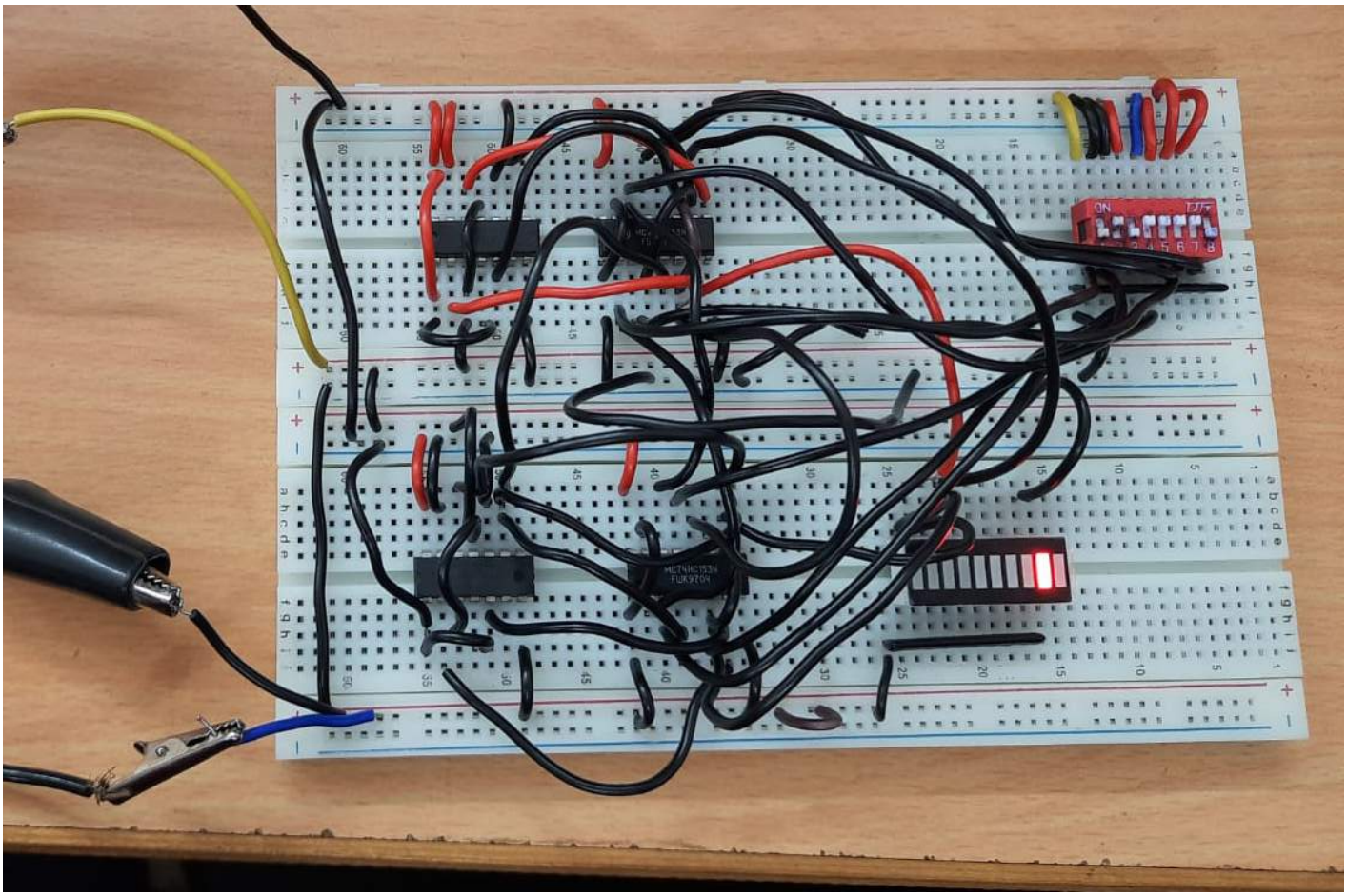
Right Shift (0_1):



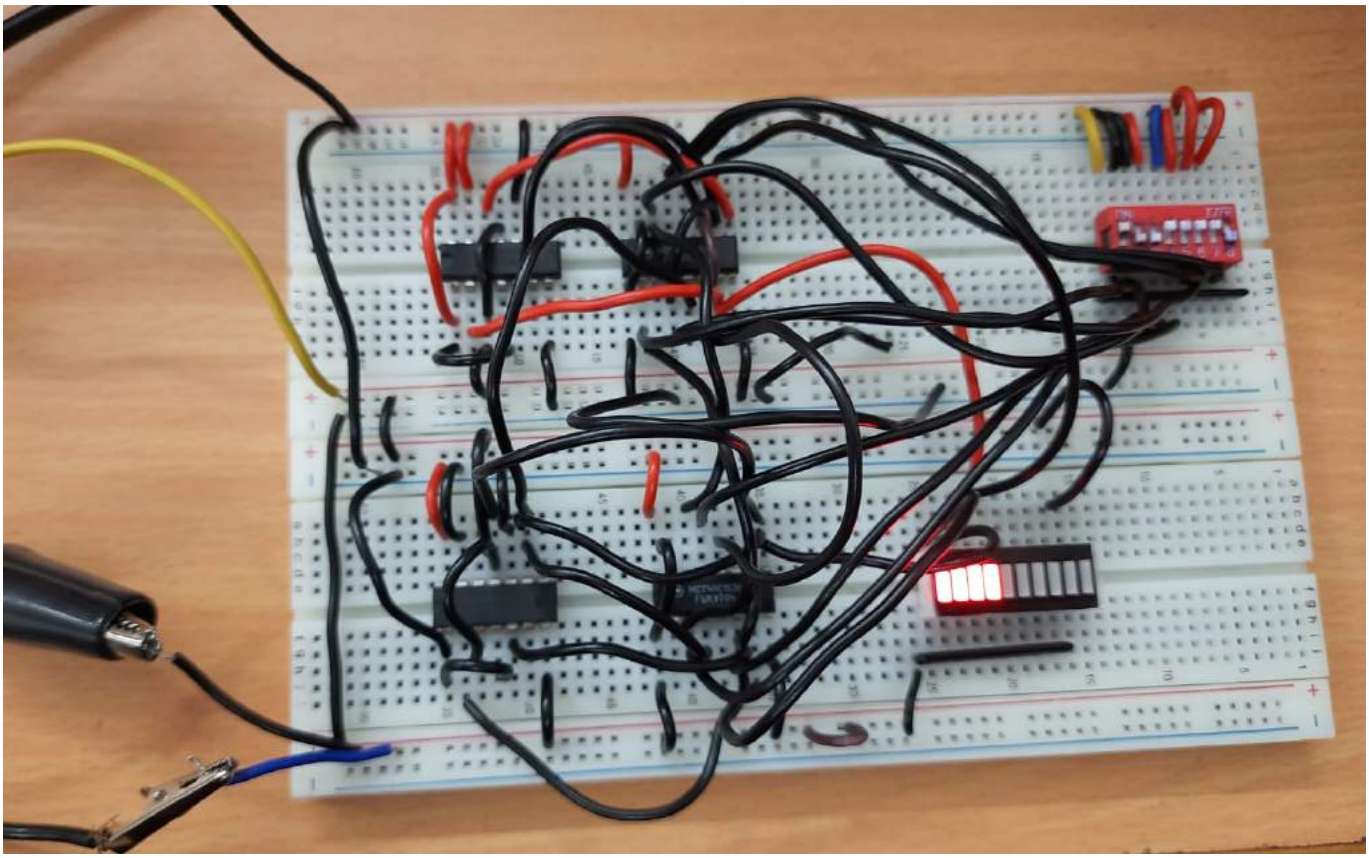


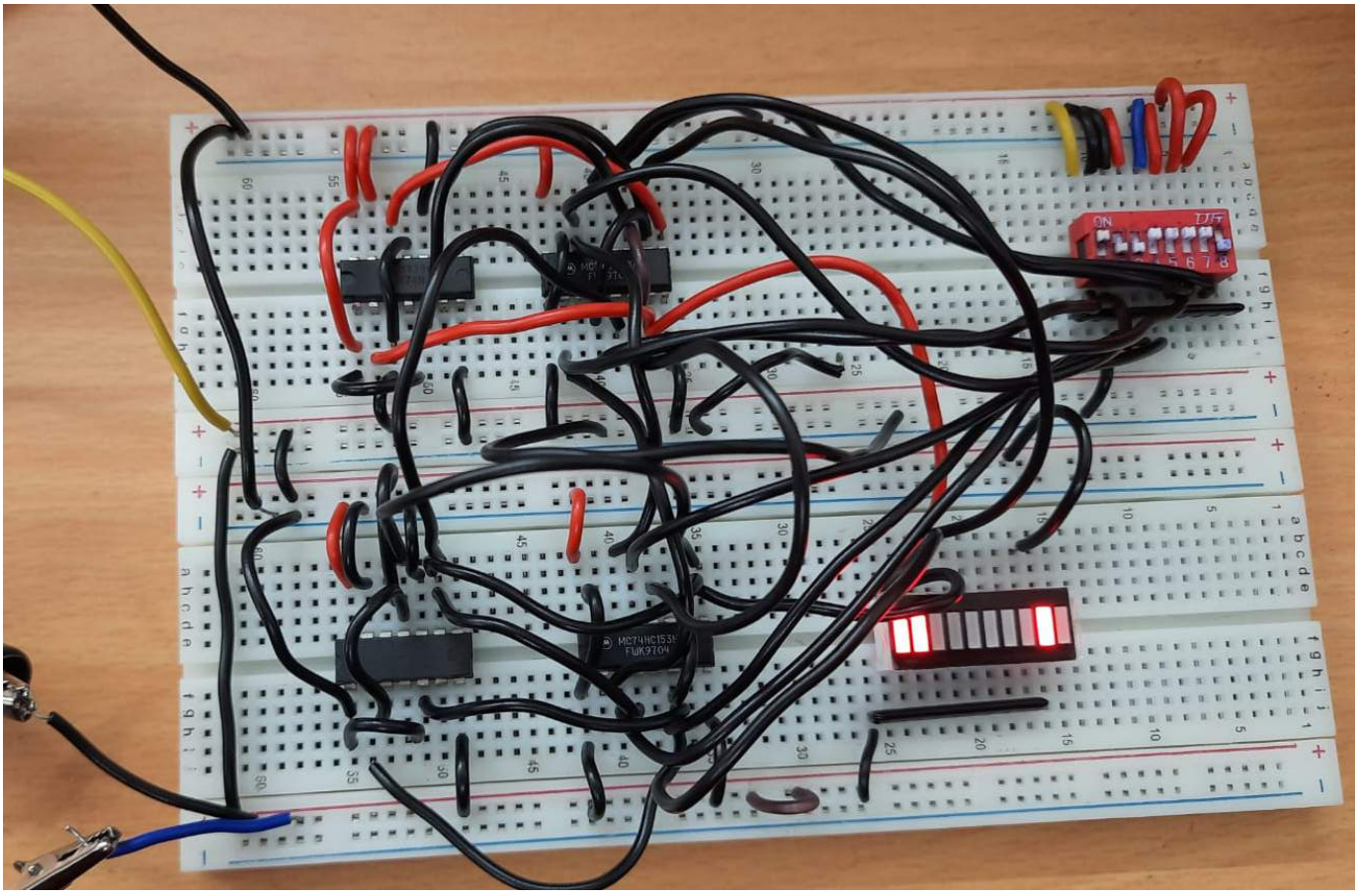


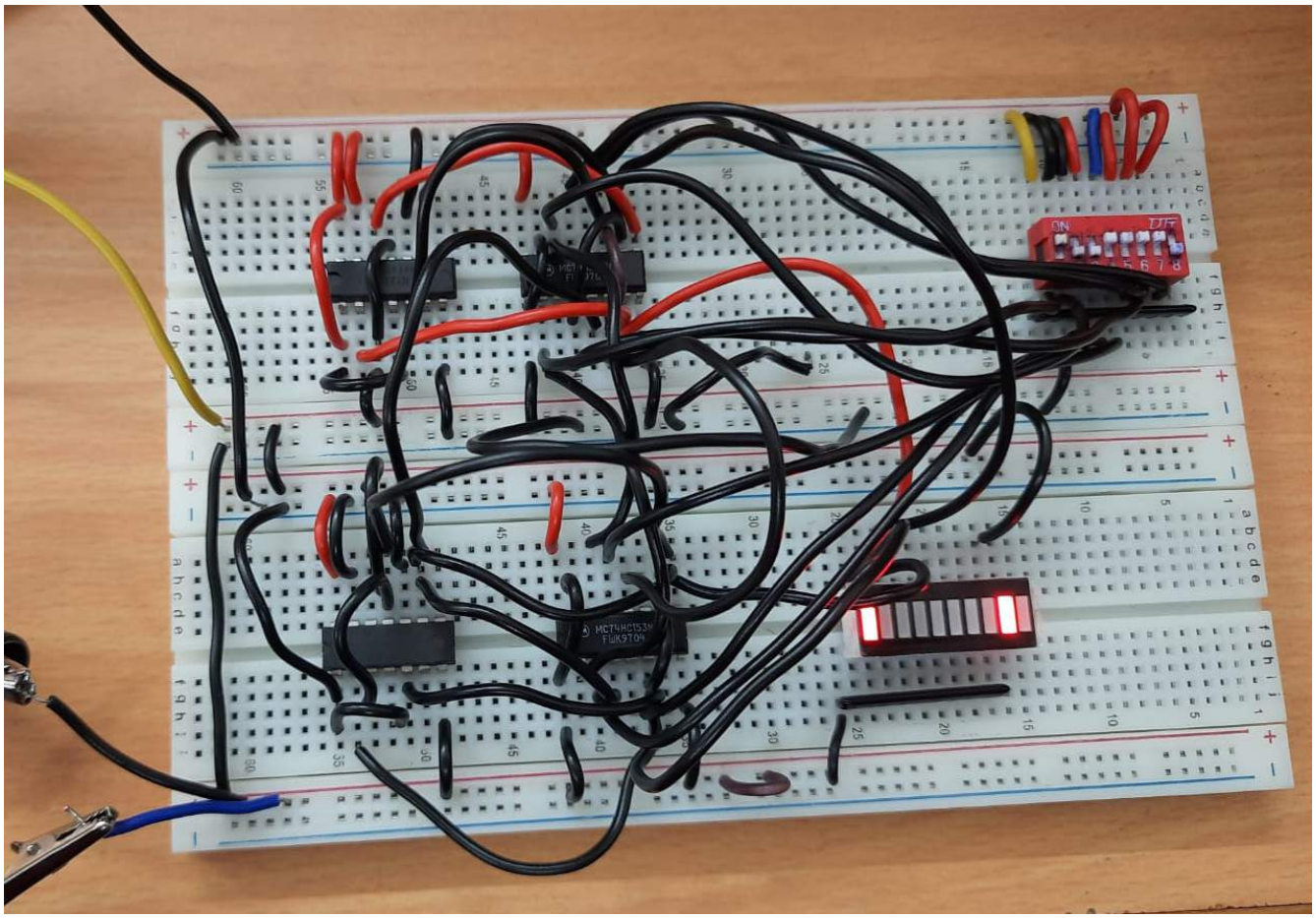


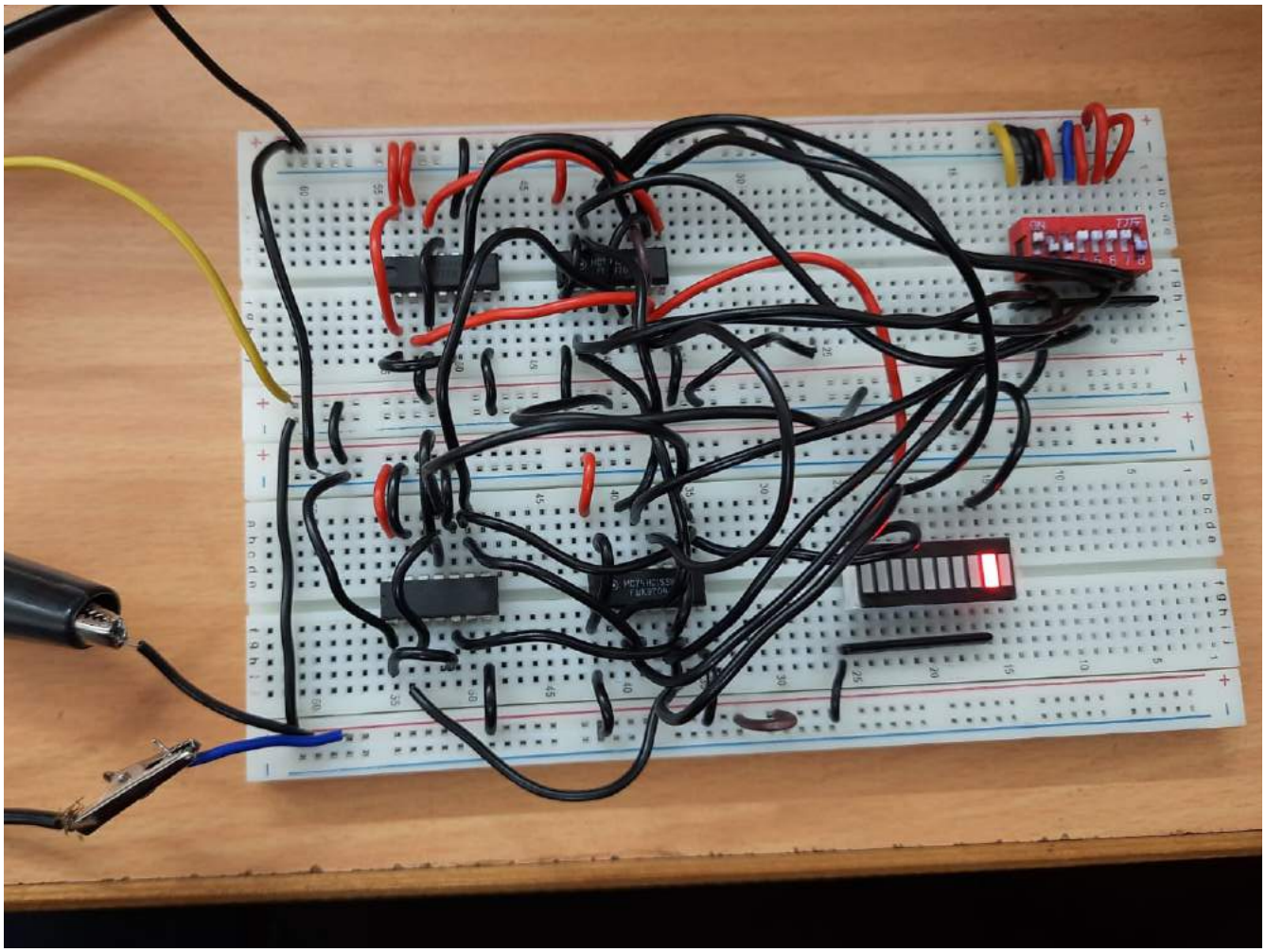

ON
DIP
1 2 3 4 5 6 7 8
MC74HC153N
FUK9704

left shift (1_0):

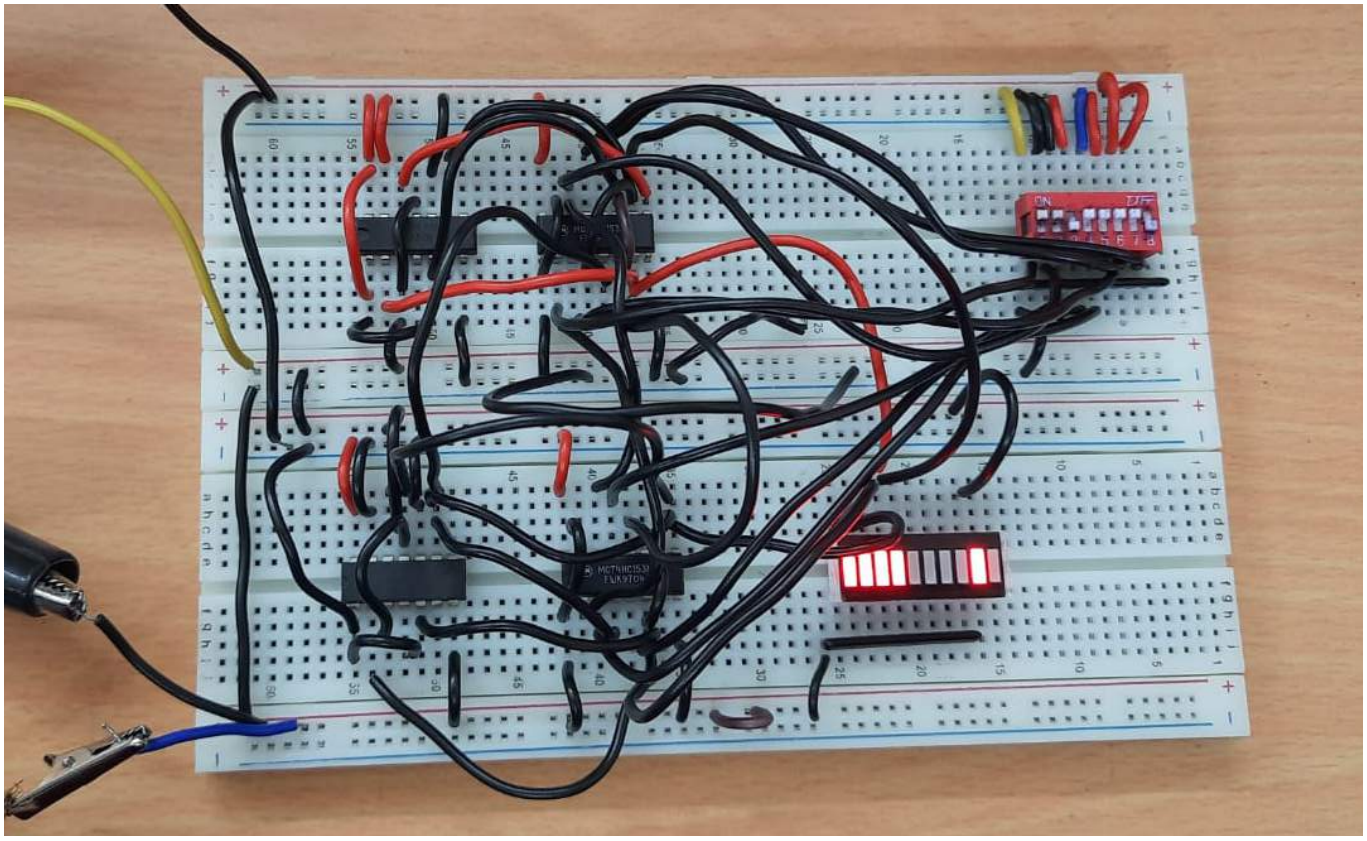


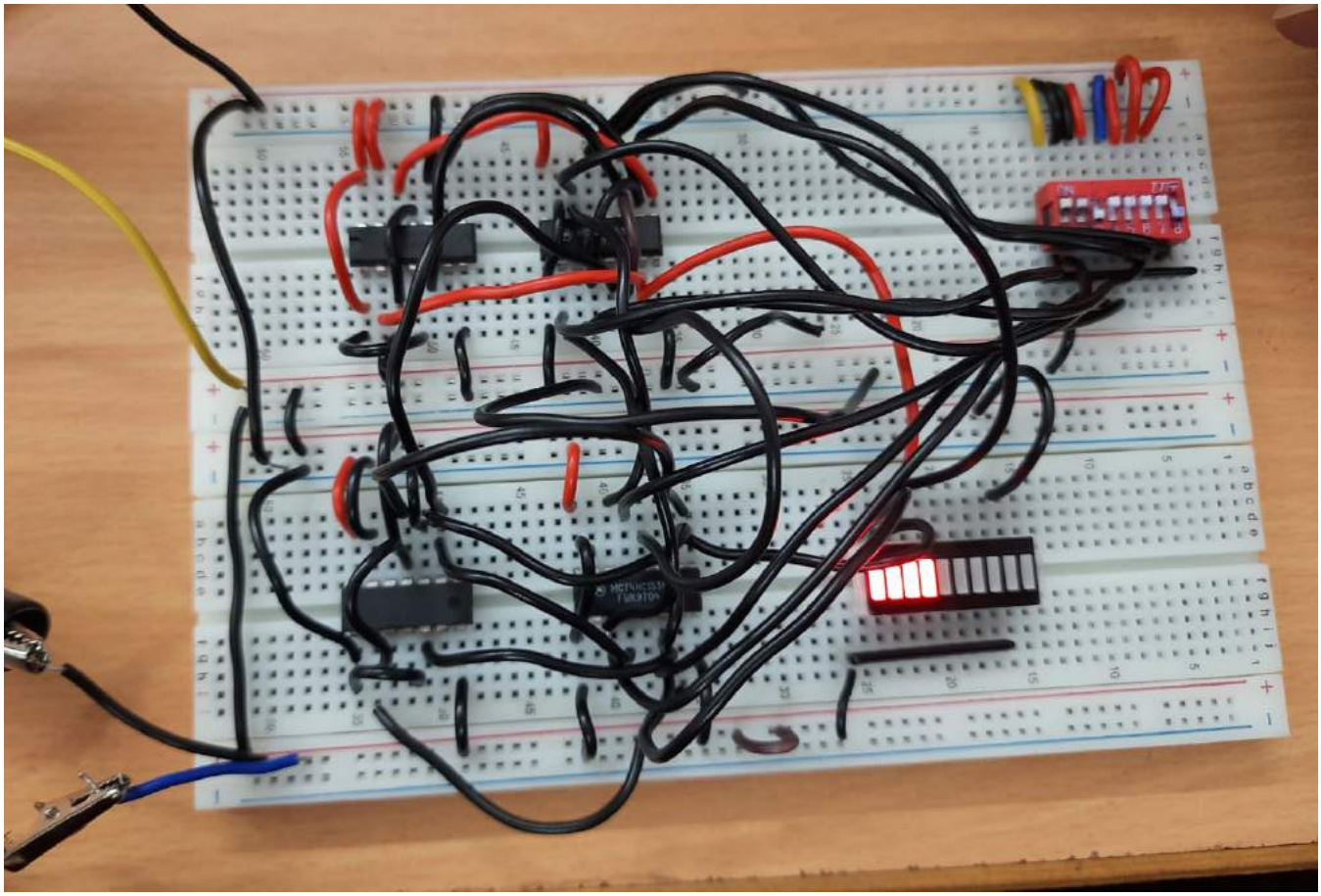






Parallel loading (1_1)





No change (0_0)