

DESIGN PROCEDURE

Page No.

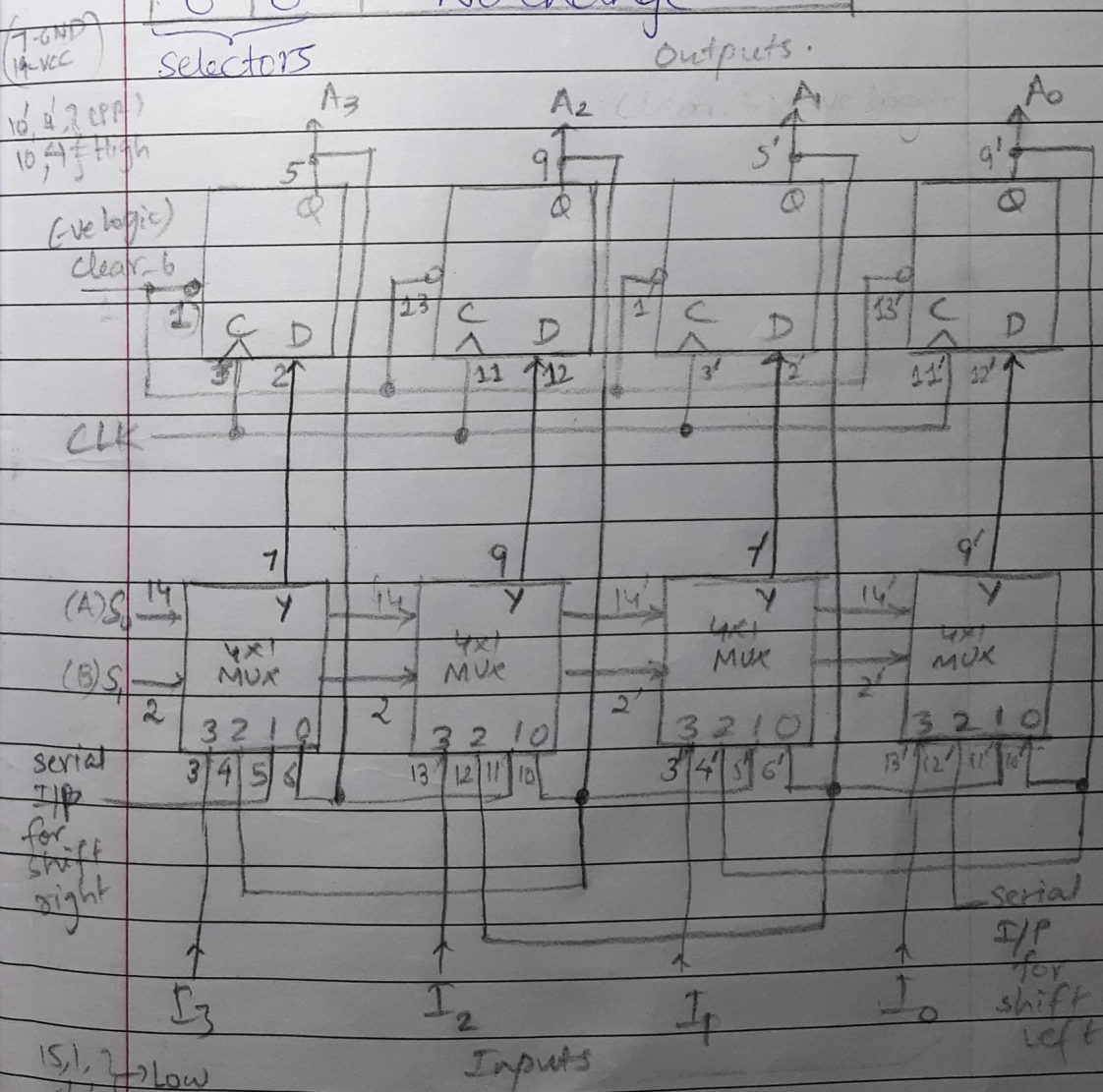
Date

UNIVERSAL SHIFT REGISTER

Input		operation
A(S)	B(S)	
1	1	Parallel Loading
1	0	Left shift
0	1	Right shift
0	0	No change

Selectors S

Outputs.



15, 1, 2 Low

15, 1, 2

(8-GND)
(16-VCC)