



## The Pros and Cons of Consolidating Frequency Sources Using Oscillators and Clock Generators

### Introduction

Typical system design initially focuses on microcontroller (MCU), CPU, memory and I/O components and architectures, and later focuses on how to supply the various clocks required in the system. Complicated systems can end up requiring 10 or more clocks. What is the best way to provide all of those frequencies, given the choice of discrete resonators, crystal oscillators, fanout buffers, clock generators and other timing device options? Board real estate and system cost reductions are made possible by consolidating the timing needs into silicon clock generator components. But does this approach always make sense, and what are the system tradeoffs in terms of board area, cost, system timing margin, noise immunity and electromagnetic interference (EMI)?

### A Typical System Design

Let's say you've finished the architecture of your system and selected the key components. It interfaces to the real world, so there is at least one amplifier, A/D or D/A, some type of human interface, an MCU and/or DSP, memory, a wireless and/or wired Internet connection and associated power management (see Figure 1). The simulated power-up and power-down sequences, signal-to-noise ratios, computation speed, memory bandwidth and power consumption are meeting spec. You're almost ready to go to board layout to simulate the layout parasitics and ensure that they don't disrupt performance. You're also planning to follow layout guidelines to minimize EMI, but because it is difficult to model, you still have your fingers crossed that the system will pass the FCC regulatory limits during EMI testing.

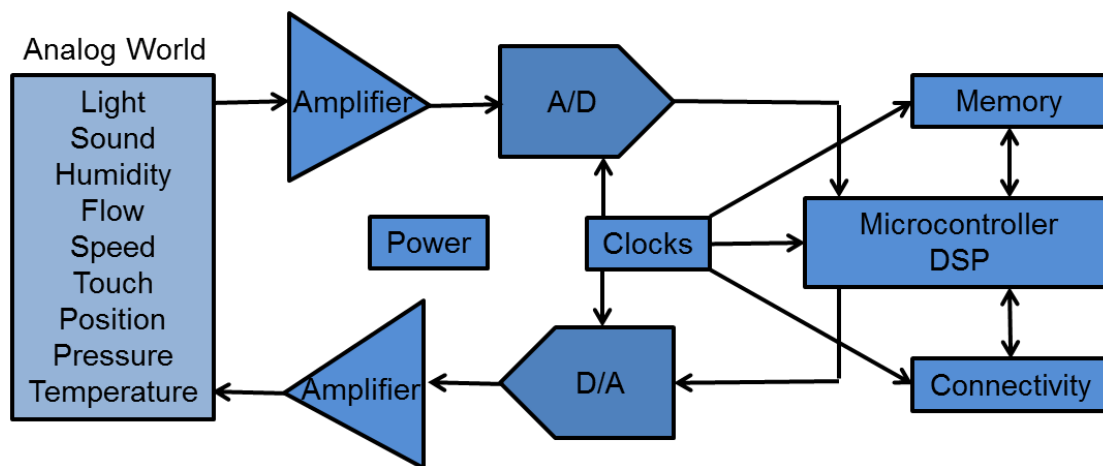


Figure 1. Typical System Design Requiring Frequency Sourcing Selection

### The System Frequency Plan

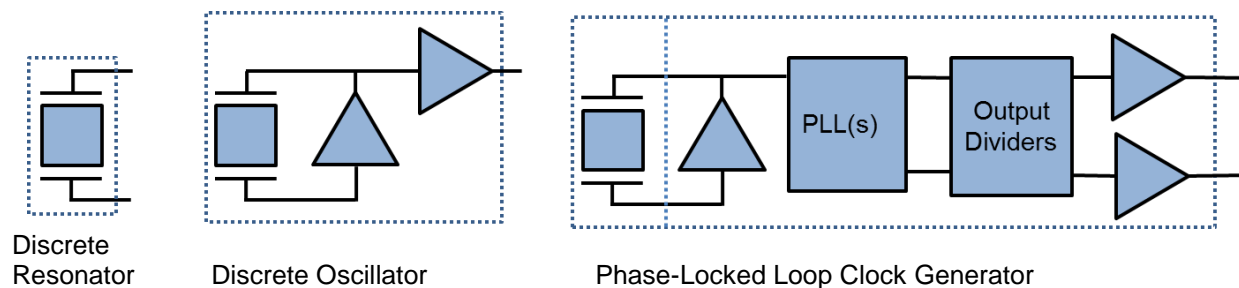
One of the final steps before going to layout is selecting the frequency references for all the components. Some of the devices only have a Clock-IN pin that would require an external oscillator, and some are designed to work with either an external clock or crystal. Your colleague relates a story about trying to debug a crystal oscillator startup problem at a specific temperature and voltage corner in a previous

design. It ultimately turned out to be insufficient crystal oscillator gain when used with a particular crystal and load. You would sure like to avoid that issue! In addition, the quality assurance team warns against the mechanical unreliability of crystals. You count the frequencies needed, eight in total, one for each of the A/D, D/A, MCU, memory, LAN and WLAN components and two for the DSP/SOC. If you could generate all of those frequencies from a single clock generator and route them to the various components, you could save a lot of area and component cost, as well as improve reliability by using a single crystal. But will the system still work? Can the clock generator provide the frequency and signal quality needed for each component, and what other advantages or disadvantages might occur?

If you've ever experienced that uncertainty, you are not alone. It is asked by every conscientious system designer when trying to optimize the frequency generation performance at the lowest total cost including component count, area, manufacturability and reliability. While each system is different, consider the following helpful guidelines for making that decision.

## Frequency Generator Basics

To understand the trade-offs in consolidating frequency sources into clock generators, we need to understand the benefits and limitations of alternative sources, as shown in Figure 2.



**Figure 2. Types of Frequency Sources**

## Discrete Resonators

Discrete resonators are designed to work in conjunction with a semiconductor gain circuit that is connected to both terminals of the resonator. The output of the gain circuit is initially the amplified noise at its input. The piezoelectric and physical properties of the resonator material allow the vibrating resonator to act as an electronic filter, passing the frequency components in its pass-band back to the input of the amplifier. At the pass band frequency where the loop gain is  $>1$  and the phase is 360 degrees, the resonator begins to oscillate, producing a stable frequency source at the amplifier output.

The two most common discrete resonators available are ceramic (typically made of lead-zirconium-titanium or PZT) resonators and quartz crystal (made of silicon dioxide or  $\text{SiO}_2$ ) resonators. The primary difference is that the ceramic resonators are lower cost and much less precise with initial accuracy of  $>5000$  ppm, and they drift significantly with temperature and age ( $\sim 2000$  ppm each in commercial applications). Crystal resonators are more precise, with accuracy of  $<50$  ppm inclusive of temperature and aging for AT cut crystals. Crystal resonators are also used by certain ASICs designed to vary the capacitance on the pins to control small deviations in frequency ( $< \pm 150$  ppm) as a voltage-controlled crystal oscillator (VCXO).

One of the major drawbacks of discrete resonators is the effort and development time required to ensure that the gain circuit, resonator and board layout (all from different manufacturers) are properly matched. The analysis includes verification of reliable startup and accuracy over temperature, process and voltage. In addition, the analysis needs to ensure that the crystal is not overdriven, which would accelerate aging. Furthermore, the lower amplitude and sinusoidal waveform of the external signal results in slow signal edges, which makes discrete resonators more sensitive to external noise. The advantages of discrete

resonators include excellent close-in phase noise, noise within KHz of the resonant frequency and low power consumption.

## Discrete Oscillators

A discrete oscillator combines the semiconductor amplifier mentioned above with a resonator in the same package. A crystal resonator is the most common resonator type, although surface acoustic wave (SAW) resonators and more recently microelectromechanical system (MEMS) resonators are sometimes used. SAW resonators operate at higher frequencies (>400 MHz), and MEMS resonators provide performance similar to that of a crystal with the advantage of being smaller and more shock resistant.

A key advantage of discrete oscillators is that the amplifier, resonator and connection capacitance can be matched in the factory to ensure reliable startup and frequency accuracy independent of board layout. Of course this comes at increased component cost, area and power consumption compared to a discrete resonator. Since only one frequency is generated from most oscillators, systems requiring multiple frequencies are often better served by consolidating frequencies into one or two clock generators when possible.

## Clock Generators

Clock generators, or frequency generators as they are sometimes called, combine the oscillator with one or more phase locked loops (PLLs), output dividers and output buffers. In most cases, the resonators are external, but there is a trend in the industry to include the resonators within the clock generator package to eliminate the disadvantages of discrete resonators outlined above. However, even if the resonator is external, the effort required to match resonators, amplifiers and board layout is greatly reduced since the clock generator only needs one reference to generate all other frequencies. In addition, minimizing the number of discrete resonators will improve system ruggedness and reliability.

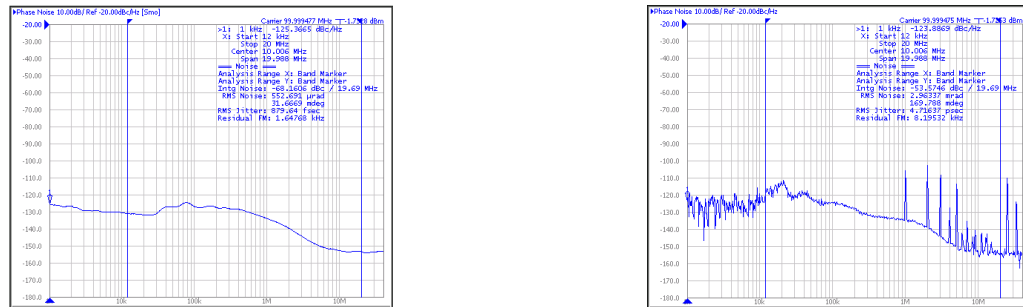
The advantages of consolidating frequencies into a clock generator are many. In addition to the reduced crystal matching effort and improved reliability mentioned above, advanced clock generators typically offer several features that benefit system performance. The output frequency can be changed in real time, which is useful when systems must adapt to various standards around the world (for example PAL vs. NTSC), to accommodate system variations by end user (for example attaching different video monitors), or to accommodate BOM changes used to ensure supply (for example, supporting audio DACs from two suppliers having different sample rates). System clock frequencies also can be varied slightly during system validation or in production testing to ensure sufficient timing margin, and spread spectrum clocking can be employed to reduce costs of EMI suppression.

There are many different types of clock generators, and each is optimized for different performance and cost targets. These differences include:

- PLLs that are based on ring oscillators vs. LC oscillators. (Ring oscillator PLLs typically provide lower cost, power and performance while LC oscillator PLLs provide higher performance at the expense of higher cost and power.)
- Singled-ended CMOS outputs for minimum power vs. differential outputs such as LVPECL, LVDS and HCSL that minimize coupled noise at the expense of higher power consumption.
- Incorporation of automatic gain control on the crystal oscillator to maximize startup gain and then reduce the gain to minimize crystal power dissipation and associated aging vs. a lower cost inverter-based oscillator with an internal or external power limiting resistor.
- Availability of a serial communication interface vs. pre-programmed frequencies and pin-selectable functionality.
- A low number of outputs in smaller packages vs. a high number of outputs in larger packages.
- Allowing mixed voltage supplies to drive different output voltage levels vs. a single supply voltage.



systems. Jitter is the uncertainty or error of a clock edge in time relative to a “perfect” clock signal, and rms phase jitter is the integral of phase noise over a specific frequency band (see Figure 4). A very common rms jitter specification originated for Sonet data transmission applications, and it is specified at <1ps rms over the 12 KHz to 20 MHz frequency band. Since this standard has been around for a few decades, many semiconductor components specify this as a default jitter limit without actually calculating the true system jitter requirement.



LCVCO PLL, <1 ps rms Jitter 12 KHz - 20 MHz

LCVCO PLL, Spurs Coupled from Other Outputs

**Figure 4. LCVCO PLL With and Without Additional Frequency Outputs Enabled**

Table 1 summarizes the advantages and disadvantages of various frequency sources.

**Table 1. Frequency Source Advantages and Limitations**

Frequency Source and Applications	Advantages	Limitations
<b>Ceramic Resonator</b> Low accuracy digital clocking	Low cost (unless many are required)	Low accuracy, 5000 – 20,000 ppm High temp. variation, +/-3000 ppm Fixed frequency, <10 MHz
<b>Crystal Resonator</b> Medium accuracy digital clocking RF references	Low cost when 1 or 2 needed Low power Required for some SoCs with integrated VCXOs	Work to match with amplifier Layout sensitive accuracy, startup Fixed frequency, <50 MHz External noise sensitive Sensitive to shock
<b>Crystal Oscillator</b> High accuracy digital clocking RF references	Reliable startup Accuracy is layout insensitive Single frequency (no cross talk)	Higher cost if >1 needed Higher power >3 mA Board area if >1 needed Single frequency copy Expensive when >100 MHz
<b>Fanout Buffer</b> Multiple copies of same frequency	Multiple frequency copies Level translation Synchronous outputs	Requires input frequency source Crosstalk if different frequencies
<b>Clock Generator, CMOS Ring PLL</b> All digital clocking Systems requiring >2 frequencies, >50 MHz, selectable or spread frequency >50 ps max jitter	Lowest cost for >2 frequencies Reliability (fewer crystals) Selectable frequencies Minimum area and component count >50 MHz frequencies Spread spectrum for EMI reduction Multiple frequency copies	Spurs from crosstalk if multiple frequencies
<b>Clock Generator, LCVCO PLL</b> Systems requiring >2 frequencies, >100 MHz, selectable frequency High-speed transceivers, RF references or sampling <1 ps rms jitter	Medium cost for >2 frequencies Reliability (fewer crystals) Selectable frequencies Minimum area & component count >50 MHz frequencies Multiple frequency copies	Higher power Spurs from crosstalk if multiple frequencies

## Summary

With multiple sources for frequency generation available, it is possible to optimize system clocking requirements for the lowest overall cost while retaining excellent system performance. In some cases only passive resonators are needed, while in many systems, especially those requiring two or more frequencies, the passive resonators are best replaced by silicon timing devices such as clock generators and fanout buffers. In addition to reducing frequency generation and EMI suppression costs, silicon frequency generators offer additional capability for BOM consolidation, system configurability and outgoing test. Find out more about Silicon Labs' oscillators, clock generators and other timing devices at [www.silabs.com/timing](http://www.silabs.com/timing).

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